

Prepare to Leave the Site

External Test Equipment Removal

Perform the procedure in Table 5-1 to disconnect the test equipment and configure the BTS for active service.

Table 5-1: External Test Equipment Removal	
Step	Action
1	Disconnect all external test equipment from all TX and RX connectors at the rear of the frame.
2	Reconnect and visually inspect all TX and RX antenna feed lines at the rear of the frame.



CAUTION

Verify all sector antenna feed lines are connected to the correct ports on the frame. Crossed antenna cables will cause system degradation of call processing.

Reset All Devices

Reset all devices by cycling power before leaving the site. The CBSC configuration data and code loads could be different from data and code on the LMF. By resetting all devices, the CBSC can load the proper data and code when the span is active again.

Updating BTS CAL LMF Files in the CBSC

Updated CAL file information is moved from the LMF Windows environment back to the CBSC which resides in a Unix environment. The procedures that follow detail how to move files from the Windows environment to the CBSC.

Copying CAL files from LMF to a Disk

Follow the procedures in Table 5-2 to copy CAL files from a LMF computer to a 3.5 diskette.

Table 5-2: Copy Files from LMF to a Diskette	
Step	Action
1	Insert a disk into your Windows A drive.
	NOTE If your disk has not been formatted, format it using Windows. The disk must be DOS formatted before copying any files. Consult your Windows/DOS documentation or online helps on how to format diskettes.
2	Click on the Start button and launch the Windows Explorer program from your Programs menu list.

Table 5-2: Copy Files from LMF to a Diskette

Step	Action
3	Click on your C: drive.
4	Double Click on the wlmf folder.
5	Double Click on the CDMA folder.
6	Click on the bts-# folder for the calibration file you want to copy.
7	Drag the BTS-#.cal file to the 3-1/2 floppy (A:) icon on the top left of the screen and release the mouse button.
8	Continue step 6 and 7 until you have copied each file desired and close the Windows Explorer program by selecting Close from the File menu option.

Copying CAL files from diskette to the CBSC

Follow the procedure in Table 5-3 to copy CAL files from a diskette to the CBSC.

Table 5-3: Copy CAL Files From Diskette to the CBSC

Step	Action
1	Log into the CBSC workstation.
2	Place your diskette containing CAL file(s) in the CBSC workstation diskette drive.
3	Enter eject -q and press the Enter key.
4	Enter mount and press the Enter key. Verify that floppy/no_name is displayed. NOTE If the eject command has been previously entered, floppy/no_name will be appended with a <u>number</u> . Use the explicit floppy/no_name reference displayed.
5	Enter cd /floppy/no_name and press the Enter key.
6	Enter ls -lia and press the Enter key. Verify that the bts-#.cal file is on the disk.
7	Enter cd and press the Enter key.
8	Enter pwd and press the Enter key. Verify that you are in your home directory (/home/<name>).
9	Enter dos2unix /floppy/no_name/bts-#.cal bts-#.cal and press the Enter key (where # is the BTS number).
10	Enter ls -l *.cal and press the Enter key. Verify that the CAL file was successfully copied.
11	Enter eject and press the Enter key.
12	Remove the floppy disk from the workstation.

5

BTS Site Span Configuration Verification

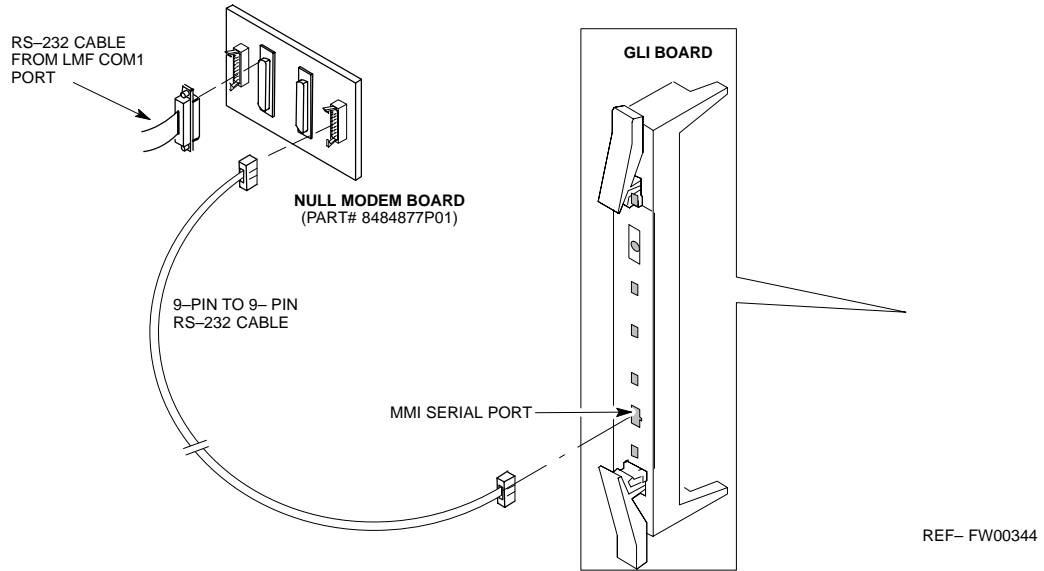
Perform the procedure in Table 5-4 to verify the current Span Framing Format and Line Build Out (LBO) parameters. *ALL* MGLI2/SGLI2 boards in all C-CCP shelves that terminate a T1/E1 span should be verified.

Table 5-4: BTS Span Parameter Configuration

Step	Action
1	Connect a serial cable from the LMF COM1 port (via null modem board) to the front panel of the MGLI2 MMI port (see Figure 5-1).
2	<p>Start an MMI communication session with CSM-1 by using the Windows desktop shortcut icon.</p> <p>NOTE The LMF program must not be running when a Hyperterminal session is started if COM1 is being used for the MMI session.</p>
3	<p>Enter the following MMI command to display the current MGLI2/SGLI2 framing format and line code configuration (in bold type):</p> <p style="padding-left: 40px;">span view <cr></p> <p>Observe a display similar to the options shown below:</p> <pre>COMMAND ACCEPTED: span view The parameter in NVM is set to T1_2. The frame format in flash is set to use T1_2. Equalization: Span A - Default (0-131 feet for T1/J1, 120 Ohm for E1) Span B - Default (0-131 feet for T1/J1, 120 Ohm for E1) Span C - Default (0-131 feet for T1/J1, 120 Ohm for E1) Span D - Default (0-131 feet for T1/J1, 120 Ohm for E1) Span E - Default (0-131 feet for T1/J1, 120 Ohm for E1) Span F - Default (0-131 feet for T1/J1, 120 Ohm for E1) Linkspeed: Default (56K for T1 D4 AMI, 64K otherwise) Currently, the link is running at the default rate The actual rate is 0</pre> <p>NOTE Defaults for span equalization are 0–40 m for T1/J1 spans and 120 Ohm for E1. Default linkspeed is 56K for T1 D4 AMI spans and 64K for all other types. There is no need to change from defaults unless the OMC-R/CBSC span configuration requires it. If the current MGLI2/SGLI2 framing format and line code configuration does not display the correct choice, proceed to Table 5-5.</p>
4	Repeat steps 1 through 3 for all remaining GLIs.
5	Exit the GLI MMI session and HyperTerminal connection by selecting File from the connection window menu bar, and then Exit from the dropdown menu.

Prepare to Leave the Site – continued

Figure 5-1: MGLI2/SGLI2 MMI Port Connection



5

Set BTS Site Span Configuration

Perform the procedure in Table 5-5 to configure the Span Framing Format and Line Build Out (LBO) parameters. *ALL* MGLI2/SGLI2 boards in all C-CCP shelves that terminate a T1/E1 span must be configured.



IMPORTANT

Perform the following procedure *ONLY* if span configurations loaded in the MGLI2/GLI2s do not match those in the OMCR/CBSC data base, *AND ONLY* when the exact configuration data is available. Loading incorrect span configuration data will render the site inoperable.

Table 5-5: Set BTS Span Parameter Configuration

Step	Action
1	If not already done, connect a serial cable from the LMF COM1 port (via null modem board) to the front panel of the MGLI2 MMI port (see Figure 5-1).
2	Start an MMI communication session with CSM-1 by using the Windows desktop shortcut icon (see Table 3-5 on page 3-18).
	<p>NOTE</p> <p>The LMF program must not be running when a Hyperterminal session is started if COM1 is being used for the MMI session.</p>

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Table 5-5: Set BTS Span Parameter Configuration

Step	Action
3	<p><i>If required only</i>, enter the following MMI command for each span line to set the BTS span parameters to match that of the physical spans <i>a–f</i> run to the site:</p> <p>span_config <option#1> <option#2> <option#3> <option#4> <option#5></p> <p><i>option#1</i> = the span to change (a–f)</p> <p><i>option#2</i> = the span type (0–8):</p> <ul style="list-style-type: none"> 0 – E1_1 (HDB3, CCS, CRC-4) 1 – E1_2 (HDB3, CCS) 2 – E1_3 (HDB3, CAS, CRC-4, TS16) 3 – E1_4 (HDB3, CAS, TS16) 4 – T1_1 (AMI, DS1 AT&T D4, without ZCS, 3 to 1 packing, Group 0 unusable) 5 – T1_2 (B8ZS, DS1 AT&T ESF, 4 to 1 packing, 64K link) 6 – J1_1 (B8ZS, J1 AT&T ESF, Japan CRC6, 4 to 1 packing) 7 – J1_2 (B8ZS, J1 AT&T ESF, US CRC6, 4 to 1 packing) 8 – T1_3 (AMI, DS1 AT&T D4, with ZCS, 3 to 1 packing, Group 0 unusable) <p><i>option#3</i> = the link speed (56 or 64) Kbps</p> <p><i>option#4</i> = the span equalization (0–7):</p> <ul style="list-style-type: none"> 0 – T1_6 (T1,J1:long haul) 1 – T1_4 (T1,J1:393–524 feet) 2 – T1_4 (T1,J1:131–262 feet) 3 – E1_75 (E1:75 Ohm) 4 – T1_4 (T1,J1:0–131 feet) 5 – T1_4 (T1,J1:524–655 feet) 6 – T1_4 (T1,J1:262–393 feet) 7 – E1_120 (E1:120 Ohm) <p><i>option#5</i> = the slot that has LAPD channel (0–31)</p> <p><i>Example for setting span configuration to E1_2, 64 Kbps, E1_120–Ohm, LAPD channel 1:</i></p> <pre>span_config a 1 64 7 1 . . span_config f 1 64 7 1</pre> <p><i>Example for setting span configuration to T1_2, 64 Kbps, T1_4 (0–131 feet), LAPD channel 0:</i></p> <pre>span_config a 5 64 4 0 . . span_config f 5 64 4 0</pre> <p>* IMPORTANT</p> <p>Make sure that spans <i>a–f</i> are set to the same span type and link speed. The equalization may be different for each individual span.</p> <p>After executing the span_config command, the affected MGLI2/SGLI2 board MUST be reset and re-loaded for changes to take effect.</p> <p>Although defaults are shown, always consult site specific documentation for span type and rate used at the site.</p>
4	Press the RESET button on the GLI2 for changes to take effect.

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Prepare to Leave the Site – continued

Table 5-5: Set BTS Span Parameter Configuration

Step	Action
5	This completes the site specific BTS Span setup for this GLI. Move the MMI cable to the next SGLI2 and repeat steps 1 and 4 for <i>ALL</i> MGLI2/SGLI2 boards.
6	Terminate the Hyperterm session and disconnect the LMF from the MGLI/SGLI.

Re-connect BTS T1 Spans and Integrated Frame Modem

Before leaving the site, connect any T1 span TELCO connectors which were removed to allow the LMF to control the BTS. Refer to Table 5-6.

Table 5-6: T1/E1 Span/IFM Connections

Step	Action
1	Connect the surge protectors on the 50-pin punch block for the spans.
2	Ensure that the CSU is powered ON .
3	Verify the span status.

5

LMF Removal



CAUTION

DO NOT power down the CDMA LMF without performing the procedure indicated below. Corrupted/lost data files may result, and in some cases, the CDMA LMF may lock up.

Follow the procedures in Table 5-7 to terminate the LMF session and remove the terminal.

Table 5-7: Terminate the LMF Session and Remove the LMF

Step	Action
1	From the CDMA window select File>Exit .
2	From the Windows Task Bar click Start>Shutdown . Click Yes when the Shut Down Windows message appears.
3	Disconnect the LMF terminal Ethernet connector from the BTS cabinet.
4	Disconnect the LMF serial port, the RS-232 to GPIB interface box, and the GPIB cables as required for equipment transport.

Prepare to Leave the Site – continued

Reestablish OMC-R Control/ Verifying T1/E1



IMPORTANT

After all activities at the site have been completed, including disconnecting the LMF, place a phone call to the OMC-R and request the BTS be placed under control of the OMC-R.

Chapter 6: Basic Troubleshooting

Table of Contents

Basic Troubleshooting Overview	
Overview	6-1
Troubleshooting: Installation	
Cannot Log into Cell-Site	6-2
Cannot Communicate to Power Meter	6-2
Cannot Communicate to Communications Analyzer	6-3
Troubleshooting: Download	
Code Download Failure	6-4
Cannot Download DATA to Any Device (Card)	6-4
Cannot ENABLE Device	6-5
LPA Errors	6-5
Troubleshooting: Calibration	
Bay Level Offset Calibration Failure	6-6
Calibration Audit Failure	6-7
Troubleshooting: Transmit ATP	
Forward link problem	6-8
Cannot Perform Txmask Measurement	6-8
Cannot Perform Rho or Pilot Time Offset Measurement	6-8
Cannot Perform Code Domain Power and Noise Floor Measurement .	6-9
Cannot Perform Carrier Measurement	6-9
Troubleshooting: Receive ATP	
Multi-FER Test Failure	6-10
Troubleshooting: CSM Checklist	
Problem Description	6-11
Intermittent 19.6608 MHz Reference Clock/GPS Receiver Operation .	6-11
No GPS Reference Source	6-11
Checksum Failure	6-11
GPS Bad RX Message Type	6-11
CSM Reference Source Configuration Error	6-12
Takes Too Long for CSM to Come INS	6-12
C-CCP Backplane Troubleshooting	6-13
Introduction	6-13
Connector Functionality	6-13
C-CCP Backplane Troubleshooting Procedure	6-14
Digital Control Problems	6-15

Table of Contents – continued

DC Power Problems	6-17
TX and RX Signal Routing Problems	6-19
RFDS – Fault Isolation	
Introduction	6-20
All tests fail	6-20
All RX and TX paths fail	6-20
All tests fail on a single antenna	6-21
Module Front Panel LED Indicators and Connectors	
Module Status Indicators	6-22
LED Status Combinations for All Modules (except GLI2, CSM, BBX2, MCC24E, MCC8E)	6-22
DC/DC Converter LED Status Combinations	6-22
CSM LED Status Combinations	6-23
GLI2 LED Status Combinations	6-25
GLI2 Pushbuttons and Connectors	6-26
BBX LED Status Combinations	6-27
MCC LED Status Combinations	6-27
LPA Shelf LED Status Combinations	6-28
Basic Troubleshooting – Span Control Link	
Span Problems (No Control Link)	6-29

Basic Troubleshooting Overview

Overview

The information in this chapter addresses some of the scenarios likely to be encountered by Customer Field Engineering (CFE) team members. This troubleshooting guide was created as an interim reference document for use in the field. It provides basic “what to do if” basic troubleshooting suggestions when the BTS equipment does not perform per the procedure documented in the manual.

Comments are consolidated from inputs provided by CFEs in the field and information gained from experience in Motorola labs and classrooms.

Troubleshooting: Installation

Cannot Log into Cell-Site

Follow the procedure in Table 6-1 to troubleshoot any Login Failure problem during normal operation.

Table 6-1: Login Failure Troubleshooting Procedure

✓	Step	Action
	1	If MGLI2 LED is solid RED, it implies a hardware failure. Reset MGLI2 by re-seating it. If this persists, install RGLI2 card in MGLI2 slot and retry. A Red LED may also indicate no Ethernet termination at top of frame.
	2	Verify that T1 is disconnected at the Channel Signaling Unit (CSU). If T1 is still connected, verify the CBSC has disabled the BTS.
	3	Try 'ping'ing the MGLI2.
	4	Verify the LMF is connected to the Primary LMF port (LAN A) in front of the BTS.
	5	Verify the LMF was configured properly.
	6	Verify the BTS-LMF cable is RG-58 (flexible black cable of less than 2.5 feet length).
	7	Verify the Ethernet ports are terminated properly.
	8	Verify a T-adaptor is <u>not</u> used on LMF side port if connected to the BTS front LMF primary port.
	9	Try connecting to the I/O panel (back of frame). Use Tri-Ax to BNC adapter at the LMF port for this connection.
	10	Re-boot the CDMA LMF and retry.
	11	Re-seat the MGLI2 and retry.
	12	Verify IP addresses are configured properly.

Cannot Communicate to Power Meter

Follow the procedure in Table 6-2 to troubleshoot a power meter communication failure.

Table 6-2: Troubleshooting a Power Meter Communication Failure

✓	Step	Action
	1	Verify Power Meter is connected to LMF with GPIB adapter.
	2	Verify cable setup as specified in Chapter 3.
	3	Verify the GP-IB address of the Power Meter is set to 13. Refer to Test Equipment setup section of Chapter 3 for details.
	4	Verify that Com1 port is not used by another application.
	5	Verify that the communications analyzer is in Talk&Listen, not Control mode.

Troubleshooting: Installation – continued

Cannot Communicate to Communications Analyzer

Follow the procedure in Table 6-3 to troubleshoot a communication analyzer failure.

Table 6-3: Troubleshooting a Communications Analyzer Communication Failure		
✓	Step	Action
	1	Verify analyzer is connected to LMF with GPIB adapter.
	2	Verify cable setup.
	3	Verify the GPIB address is set to 18.
	4	Verify the GPIB adapter DIP switch settings are correct. Refer to Test Equipment setup section for details.
	5	Verify the GPIB adapter is not locked up. Under normal conditions, only 2 green LEDs must be 'ON' (Power and Ready). If any other LED is continuously 'ON', then power-cycle the GPIB Box and retry.
	6	If a Hyperterm window is open for MMI, close it.
	7	Verify the LMF GPIB address is set to 18
	8	Verify the analyzer is in Talk and Listen not Control mode.

Troubleshooting: Download

Code Download Failure

Follow the procedure in Table 6-4 to troubleshoot any code download failure.

Table 6-4: Troubleshooting Code Download Failure

✓	Step	Action
	1	Verify T1 is disconnected from the BTS at CSU.
	2	Verify LMF can communicate with the BTS device using the Status function.
	3	Communication to MGLI2 must first be established before trying to talk to any other BTS device. MGLI2 must be INS_ACT state (green).
	4	Verify the card is physically present in the cage and powered-up.
	5	If card LED is solid RED, it implies hardware failure. Reset card by re-seating it. If this persists, replace card from another slot & retry. NOTE The card can only be replaced by a card of the same type.
	6	Re-seat card and try again.
	7	If BBX reports a failure message and is OOS_RAM, the code load was OK. Status it.
	8	If the download portion completes and the reset portion fails, reset the device by selecting the device and reset.

6

Cannot Download DATA to Any Device (Card)

Follow the procedure in Table 6-5 to troubleshoot any data download failure.

Table 6-5: Troubleshooting Data Download Failure

✓	Step	Action
	1	Re-seat card and repeat code and data load procedure.
	2	Verify the ROM and RAM code loads are of the same release by statusing the card. Refer to Chapter 3, "Download the BTS" for more information.

Troubleshooting: Download – continued

Cannot ENABLE Device

Before a device can be enabled (placed in-service), it must be in the OOS_RAM state (yellow on the LMF) with data downloaded to the device. The color of the device on the LMF changes to green, once it is enabled.

The three states that devices can be displayed:

- Enabled (green, INS)
- Disabled (yellow, OOS_RAM)
- Reset (blue, OOS_ROM)

Follow the procedure in Table 6-6 to troubleshoot device enable failure.

Table 6-6: Troubleshooting Device Enable (INS) Failure

✓	Step	Action
	1	Re-seat card and repeat code and data load procedure.
	2	If CSM cannot be enabled, verify the CDF file has correct latitude and longitude data for cell site location and GPS sync.
	3	Ensure primary CSM is in INS_ACT state. NOTE MCCs will not go INS without the CSM being INS.
	4	Verify 19.6608 MHz CSM clock; MCCs will not go INS otherwise.
	5	The BBX should not be enabled for ATP tests.
	6	If MCCs give “invalid or no system time,” verify the CSM is enabled.

LPA Errors

Follow the procedure in Table 6-7 to troubleshoot any LPA errors.

Table 6-7: LPA Errors

✓	Step	Action
	1	If LPAs continue to give alarms, even after cycling power at the circuit breakers, then connect an MMI cable to the LPA and set up a Hyperterminal connection. Enter ALARMS in the Hyperterminal window. The resulting LMF display may provide an indication of the problem. (Call Field Support for further assistance.)

Troubleshooting: Calibration

Bay Level Offset Calibration Failure

Follow the procedure in Table 6-8 to troubleshoot a BLO calibration failure.

Table 6-8: Troubleshooting BLO Calibration Failure

✓	Step	Action
	1	Verify the Power Meter is configured correctly (see the test equipment setup section) and connection is made to the proper TX port.
	2	Verify the parameters in the bts-#.cdf file are set correctly for the following bands: For 1900 MHz: BandClass=1; FreqBand=16 For 800 MHz: BandClass=0; FreqBand=8
	3	Verify that no LPA in the sector is in alarm state (flashing red LED). Reset the LPA by pulling the circuit breaker, and after 5 seconds, pushing back in.
	4	Re-calibrate the Power Meter and verify it is calibrated correctly with cal factors from sensor head.
	5	Verify GPIB adapter is not locked up. Under normal conditions, only 2 green LEDs must be 'ON' (Power and Ready). If any other LED is continuously 'ON', power-cycle (turn power off and on) the GPIB Box and retry.
	6	Verify sensor head is functioning properly by checking it with the 1 mW (0 dBm) Power Ref signal.
	7	If communication between the LMF and Power Meter is operational, the Meter display will show "RES :"
	8	Verify the combiner frequency is the same as the test freq/chan.

Troubleshooting: Calibration – continued

Calibration Audit Failure

Follow the procedure in Table 6-9 to troubleshoot a calibration audit failure.

Table 6-9: Troubleshooting Calibration Audit Failure		
✓	Step	Action
	1	Verify Power Meter is configured correctly (refer to the test equipment setup section of chapter 3).
	2	Re-calibrate the Power Meter and verify it is calibrated correctly with cal factors from sensor head.
	3	Verify that no LPA is in alarm state (rapidly flashing red LED). Reset the LPA by pulling the circuit breaker, and, after 5 seconds, pushing back in.
	4	Verify that no sensor head is functioning properly by checking it with the 1 mW (0 dBm) Power Ref signal.
	5	After calibration, the BLO data must be re-loaded to the BBX2s before auditing. Click on the BBX(s) and select Device>Download BLO Re-try the audit.
	6	Verify GPIB adapter is not locked up. Under normal conditions, only 2 green LEDs must be 'ON' (Power and Ready). If any other LED is continuously 'ON', power-cycle (turn power off and on) the GP-IB Box and retry.

Troubleshooting: Transmit ATP

Forward link problem

If the BTS passes the reduced ATP tests but has a forward link problem during normal operation follow the procedure in Table 6-10 to troubleshoot.

Table 6-10: Troubleshooting Forward Link Failure (BTS Passed Reduced ATP)		
✓	Step	Action
	1	Perform these additional TX tests to troubleshoot a forward link problem: <ul style="list-style-type: none">– TX mask– TX rho– TX code domain

Cannot Perform Txmask Measurement

Follow the procedure in Table 6-11 to troubleshoot a TX Mask Measurement failure.

Table 6-11: Troubleshooting TX Mask Measurement Failure		
✓	Step	Action
	1	Verify that TX audit passes for the BBX(s).
	2	If performing manual measurement, verify analyzer setup.
	3	Verify that no LPA in the sector is in alarm state (flashing red LED). Re-set the LPA by pulling the circuit breaker, and, after 5 seconds, pushing it back in.

Cannot Perform Rho or Pilot Time Offset Measurement

Follow the procedure in Table 6-12 to troubleshoot a rho and pilot time offset measurement failure.

Table 6-12: Troubleshooting Rho and Pilot Time Offset Measurement Failure		
✓	Step	Action
	1	Verify presence of RF signal by switching to spectrum analyzer screen.
	2	Verify PN offsets displayed on the analyzer is the same as the PN offset in the CDF file.
	3	Re-load MGLI2 data and repeat the test.
	4	If performing manual measurement, verify analyzer setup.

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Troubleshooting: Transmit ATP – continued

Table 6-12: Troubleshooting Rho and Pilot Time Offset Measurement Failure

✔	Step	Action
	5	Verify that no LPA in the sector is in alarm state (flashing red LED). Reset the LPA by pulling the circuit breaker, and, after 5 seconds, pushing back in.
	6	If Rho value is unstable and varies considerably (e.g. .95,.92,.93), this may indicate that the GPS is still phasing (i.e. trying to reach and maintain 0 freq. error). Go to the freq. bar in the upper right corner of the Rho meter and select Hz. Press <Shift-avg> and enter 10, to obtain an average Rho value. This is an indication the GPS has not stabilized before going <i>INS</i> and may need to be re-initialized.

Cannot Perform Code Domain Power and Noise Floor Measurement

Follow the procedure in Table 6-13 to troubleshoot code domain and noise floor measurement failure.

Table 6-13: Troubleshooting Code Domain Power and Noise Floor Measurement Failure

✔	Step	Action
	1	Verify presence of RF signal by switching to spectrum analyzer screen.
	2	Verify PN offset displayed on analyzer is same as PN offset being used in the CDF file.
	3	Disable and re-enable MCC (one or more MCCs based on extent of failure).

Cannot Perform Carrier Measurement

Follow the procedure in Table 6-14 to troubleshoot carrier measurement failure.


Table 6-14: Troubleshooting Carrier Measurement Failure

✔	Step	Action
	1	Perform the test manually, using the spread CDMA signal. Verify High Stability 10 MHz Rubidium Standard is warmed up (60 minutes) and properly connected to test set-up.

Troubleshooting: Receive ATP

Multi-FER Test Failure

Follow the procedure in Table 6-15 to troubleshoot multi-FER failure.

Table 6-15: Troubleshooting Multi-FER Failure		
	Step	Action
	1	Verify test equipment set up is correct for a FER test.
	2	Verify test equipment is locked to 19.6608 and even second clocks. The yellow LED (REF UNLOCK) must be OFF.
	3	Verify MCCs have been loaded with data and are INS-ACT.
	4	Disable and re-enable the MCC (one or more based on extent of failure).
	5	Disable, re-load code and data, and re-enable MCC (one or more MCCs based on extent of failure).
	6	Verify antenna connections to frame are correct based on the directions messages.

Troubleshooting: CSM Checklist

Problem Description

Many of the Clock Synchronization Manager (CSM) boards may be resolved in the field before sending the boards to the factory for repair. This section describes known CSM problems identified in field returns, some of which are field-repairable. Check these problems before returning suspect CSM boards.

Intermittent 19.6608 MHz Reference Clock/GPS Receiver Operation

If having any problems with CSM board kit numbers, SGLN1145 or SGLN4132, check the suffix with the kit number. If the kit has version “AB,” then replace with version “BC” or higher, and return model AB to the repair center.

No GPS Reference Source

Check the CSM boards for proper hardware configuration. RF-GPS (Local GPS) – CSM kit SGLN1145, which should be installed in Slot 1, has an on-board GPS receiver; while kit SGLN4132, in Slot 2, does not have a GPS receiver.

Remote GPS (R-GPS) – Kit SGLN4132ED or later, which should be installed in both Slot 1 and Slot 2, does not have a GPS receiver. Any incorrectly configured board *must* be returned to the repair center. *Do not attempt to change hardware configuration in the field.* Also, verify the GPS antenna is not damaged and is installed per recommended guidelines.

Checksum Failure

The CSM could have corrupted data in its firmware resulting in a non-executable code. The problem is usually caused by either electrical disturbance, or interruption of data during a download. Attempt another download with no interruptions in the data transfer. Return CSM board back to repair center if the attempt to reload fails.

GPS Bad RX Message Type

This is believed to be caused by a later version of CSM software (3.5 or higher) being downloaded, via LMF, followed by an earlier version of CSM software (3.4 or lower), being downloaded from the CBSC. Download again with CSM software code 3.5 or higher. Return CSM board back to repair center if attempt to reload fails.

Troubleshooting: CSM Checklist – continued

CSM Reference Source Configuration Error

This is caused by incorrect reference source configuration performed in the field by software download. CSM kit SGLN1145 and SGLN4132 must have proper reference sources configured (as shown below) to function correctly.

CSM Kit No.	Hardware Configuration	CSM Slot No.	Reference Source Configuration
SGLN1145	With GPS Receiver	1	Primary = Local GPS Backup = Either LFR or HSO
SGLN4132ED or later	Without GPS Receiver	2	Primary = Remote GPS Backup = Either LFR or HSO

Takes Too Long for CSM to Come INS

This may be caused by a delay in GPS acquisition. Check the accuracy flag status and/or current position. Refer to the GSM system time/GPS and LFR/HSO verification section in Chapter 3. At least 1 satellite should be visible and tracked for the “surveyed” mode and 4 satellites should be visible and tracked for the “estimated” mode. Also, verify correct base site position data used in “surveyed” mode.

C-CCP Backplane Troubleshooting

Introduction

The C-CCP backplane is a multi-layer board that interconnects all the C-CCP modules. The complexity of this board lends itself to possible improper diagnoses when problems occur.

Connector Functionality

The following connector overview describes the major types of backplane connectors along with the functionality of each. This will allow the Cellular Field Engineer (CFE) to:

- Determine which connector(s) is associated with a specific problem type.
- Allow the isolation of problems to a specific cable or connector.

Primary “A” and Redundant “B” ISB (Inter Shelf Bus) connectors

The 40 pin ISB connectors provide an interface bus from the master GLI2 to all other GLI2s in the modem frame. Its basic function is to provide clock synchronization from the master GLI2 to all other GLI2s in the frame.

The ISB is also provides the following functions:

- Groom span line when a single span is used for multiple cages.
- Provide MMI connection to/from the master GLI2 to cell site modem.
- Provide interface between GLI2s and the AMR (for reporting BTS alarms).

Span Line Connector

The span line input is an 8 pin RJ-45 connector that provides a primary and secondary (if used) span line interface to each GLI2 in the C-CCP shelf. The span line is used for MM/EMX switch control of the Master GLI2 and also all the BBX traffic.

Power Input (Return A, B, and C connectors)

Provides a +27 Volt input for use by the power supply modules.

Power Supply Module Interface

Each power supply module has a series of three different connectors to provide the needed inputs/outputs to the C-CCP backplane. These include a VCC/Ground input connector, a Harting style multiple pin interface, and a +15 V/Analog Ground output connector. The Transceiver Power Module converts 27/48 Volts to a regulated +15, +6.5, +5.0 Volts to be used by the C-CCP shelf cards.

GLI2 Connector

This connector consists of a Harting 4SU digital connector and a 6-conductor coaxial connector for RDM distribution. The connectors provide inputs/outputs for the GLI2s in the C-CCP backplane.

GLI2 Ethernet “A” and “B” Connections

These BNC connectors are located on the C–CCP backplane and routed to the GLI2 board. This interface provides all the control and data communications between the master GLI2 and the other GLI2, between gateways, and for the LMF on the LAN.

BBX2 Connector

Each BBX connector consists of a Harting 2SU/1SU digital connector and two 6–conductor coaxial connectors. These connectors provide DC, digital, and RF inputs/outputs for the BBXs in the C–CCP backplane.

CIO Connectors

- RX RF antenna path signal inputs are routed through RX Tri–Filters (on the I/O plate), and via coaxial cables to the two MPC modules – the six “A” (main) signals go to one MPC; the six “B” (diversity) to the other. The MPC outputs the low–noise–amplified signals via the C–CCP backplane to the CIO where the signals are split and sent to the appropriate BBX.
- A digital bus then routes the baseband signal through the BBX, to the backplane, then on to the MCC slots.
- Digital TX antenna path signals originate at the MCC24s. Each output is routed from the MCC slot via the backplane appropriate BBX.
- TX RF path signal originates from the BBX, through the backplane to the CIO, through the CIO, and via multi–conductor coaxial cabling to the LPAs in the LPA shelf.

C–CCP Backplane Troubleshooting Procedure

The following table provides a standard procedure for troubleshooting problems that appear to be related to a defective C–CCP backplane. The table is broken down into possible problems and steps which should be taken in an attempt to find the root cause.



IMPORTANT

It is important to note that all steps be followed before replacing ANY C–CCP backplane.

Digital Control Problems

No GLI2 Control via LMF (all GLI2s)

Follow the procedure in Table 6-16 for problems with GLI2 control.

Table 6-16: No GLI2 Control via LMF (all GLI2s)	
Step	Action
1	Check the ethernet for proper connection, damage, shorts, or opens.
2	Verify C-CCP backplane Shelf ID DIP switch is set correctly.
3	Visually check the master GLI2 connector (both board and backplane) for damage.
4	Replace the master GLI2 with a known good GLI2.

No GLI2 Control through Span Line Connection (All GLI2s)

Follow the procedure in Table 6-17 for problems with GLI2 control.

Table 6-17: No GLI2 Control through Span Line Connection (Both GLI2s)	
Step	Action
1	Verify C-CCP backplane Shelf ID DIP switch is set correctly.
2	Verify that the BTS and GLI2s are correctly configured in the OMCR/CBSC data base.
3	Visually check the master GLI2 connector (both board and backplane) for damage.
4	Replace the master GLI2 with a known good GLI2.
5	Check the span line inputs from the top of the frame to the master GLI2 for proper connection and damage.

MGLI2 Control Good – No Control over Co-located GLI2

Follow the procedure in Table 6-18 for problems with GLI2 control.

Table 6-18: MGLI2 Control Good – No Control over Co-located GLI2	
Step	Action
1	Verify that the BTS and GLI2s are correctly configured in the OMCR CBSC data base.
2	Check the ethernet for proper connection, damage, shorts, or opens.
3	Visually check all GLI2 connectors (both board and backplane) for damage.
4	Replace the remaining GLI2 with a known good GLI2.

No AMR Control (MGLI2 good)

Follow the procedure in Table 6-19 for problems with AMR control.

Table 6-19: MGLI2 Control Good – No Control over AMR	
Step	Action
1	Visually check the master GLI2 connector (both board and backplane) for damage.
2	Replace the master GLI2 with a known good GLI2.
3	Replace the AMR with a known good AMR.

No BBX Control in the Shelf

Follow the procedure in Table 6-20 for problems with co-located GLI2.

Table 6-20: MGLI2 Control Good – No Control over Co-located GLI2s	
Step	Action
1	Visually check all GLI2 connectors (both board and backplane) for damage.
2	Replace the remaining GLI2 with a known good GLI2.
3	Visually check BBX connectors (both board and backplane) for damage.
4	Replace the BBX with a known good BBX.

No (or Missing) Span Line Traffic

Follow the procedure in Table 6-21 for problems with span line traffic.

Table 6-21: BBX Control Good – No (or Missing) Span Line Traffic	
Step	Action
1	Visually check all GLI2 connectors (both board and backplane) for damage.
2	Replace the remaining GLI2 with a known good GLI2.
3	Visually check all span line distribution (both connectors and cables) for damage.
4	If the problem seems to be limited to 1 BBX, replace the BBX with a known good BBX.

No (or Missing) MCC24 Channel Elements

Follow the procedure in Table 6-22 for problems with channel elements.

Table 6-22: No MCC-1X/MCC24E/MCC8E Channel Elements	
Step	Action
1	Verify channel elements on a co-located MCC of the same type (CDF MccType codes: MCC8E = 0; MCC24E = 2; MCC-1X = 3)
2	Check MCC connectors (both module and backplane) for damage.
3	If the problem seems to be limited to one MCC, replace it with a known good MCC of the same type.
4	If no channel elements on any MCC, verify clock reference to CIO.

DC Power Problems



WARNING

Potentially lethal voltage and current levels are routed to the BTS equipment. This test must be carried out with a second person present, acting in a safety role. Remove all rings, jewelry, and wrist watches prior to beginning this test.

No DC Input Voltage to Power Supply Module

Follow the procedure in Table 6-23 for problems with DC input voltage.

Table 6-23: No DC Input Voltage to Power Supply Module

Step	Action
1	Verify DC power is applied to the BTS frame. Verify there are no breakers tripped. * IMPORTANT If a breaker has tripped, remove all modules from the applicable shelf supplied by the breaker and attempt to reset it. <ul style="list-style-type: none"> – If breaker trips again, there is probably a cable or breaker problem within the frame. – If breaker does not trip, there is probably a defective module or sub-assembly within the shelf.
2	Verify that the C-CCP shelf breaker on the BTS frame breaker panel is functional.
3	Use a voltmeter to determine if the input voltage is being routed to the C-CCP backplane by measuring the DC voltage level on the PWR_IN cable. <ul style="list-style-type: none"> – If the voltage is not present, there is probably a cable or breaker problem within the frame. – If the voltage is present at the connector, reconnect and measure the level at the “VCC” power feed clip on the distribution backplane. If the voltage is correct at the power clip, inspect the clip for damage.
4	If everything appears to be correct, visually inspect the power supply module connectors.
5	Replace the power supply module with a known good module.
6	If steps 1 through 4 fail to indicate a problem, the C-CCP backplane failure (possibly an open trace) has occurred.

CCP Backplane Troubleshooting – continued

No DC Voltage (+5, +6.5, or +15 Volts) to a Specific GLI2, BBX2, or Switchboard

Follow the procedure in Table 6-24 for problems with DC input voltage.

Table 6-24: No DC Input Voltage to any C-CCP Shelf Module	
Step	Action
1	Verify steps outlined in Table 6-23 have been performed.
2	Inspect the defective board/module (both board and backplane) connector for damage.
3	Replace suspect board/module with known good board/module.

TX and RX Signal Routing Problems

Follow the procedure in Table 6-25 for problems with DC input voltage.

Table 6-25: No DC Input Voltage to any C-CCP Shelf Module	
Step	Action
1	Inspect all Harting Cable connectors and back-plane connectors for damage in all the affected board slots.
2	Perform steps outlined in the RF path troubleshooting flowchart in this manual.

RFDS – Fault Isolation

Introduction

The RFDS is used to perform Pre-Calibration Verification and Post-Calibration Audits which limit-check the RFDS-generate and reported receive levels of every path from the RFDS through the directional coupler coupled paths. In the event of test failure, refer to the following tables.

All tests fail

Follow the procedure in Table 6-26 for problems with RFDS.

Table 6-26: RFDS Fault Isolation – All tests fail

Step	Action
1	Check the calibration equipment for proper operation by manually setting the signal generator output attenuator to the lowest output power setting and connecting the output port to the spectrum analyzer rf input port.
2	Set the signal generator output attenuator to -90 dBm, and switch on the rf output. Verify that the spectrum analyzer can receive the signal, indicate the correct signal strength, (accounting for the cable insertion loss), and the approximate frequency.
3	Visually inspect RF cabling. Make sure each directional coupler forward and reflected port connects to the RFDS antenna select unit on the RFDS.
4	Check the wiring against the site documentation wiring diagram or the <i>BTS Site Installation</i> manual.
5	Verify RGLI and TSU have been downloaded.
6	Check to see that all RFDS boards show green on the front panel indicators. Visually check (both board and backplane) for damage.
7	Replace any boards that do not show green with known good boards one at a time in the following order. Re-test after each is replaced. <ul style="list-style-type: none">– RFDS ASU board.– RFDS Transceiver board.

All RX and TX paths fail

If every receive or transmit path fails, the problem most likely lies with the rf converter board or the transceiver board. Refer to Table 6-27 for fault isolation procedures.

Table 6-27: RFDS Fault Isolation – All RX and TX paths fail

Step	Action
1	Visually check the master RF converter board (both board and backplane) for damage.
2	Replace the RF converter board with a known good RF converter board.
3	Visually check RXCVR TSU (both board and backplane) for damage.
4	Replace the TSU with a known good TSU.

All tests fail on a single antenna

If all path failures are on one antenna port, forward and/or reflected, follow the procedures in Table 6-28 checks.

Table 6-28: RFDS Fault Isolation – All tests fail on single antenna path	
Step	Action
1	Visually inspect the site interface cabinet internal cabling to the suspect directional coupler antenna port.
2	Verify the forward and reflected ports connect to the correct RFDS antenna select unit positions on the RFDS backplane. Refer to the installation manual for details.
3	Visually check ASU connectors (both board and backplane) for damage.
4	Replace the ASU with a known good ASU.
5	Replace the RF cables between the affected directional coupler and RFDS. NOTE Externally route the cable to bypass suspect segment.

Module Front Panel LED Indicators and Connectors

Module Status Indicators

Each of the non-passive plug-in modules has a bi-color (green & red) LED status indicator located on the module front panel. The indicator is labeled PWR/ALM. If both colors are turned on, the indicator is yellow.

Each plug-in module, except for the fan module, has its own alarm (fault) detection circuitry that controls the state of the PWR/ALM LED.

The fan TACH signal of each fan module is monitored by the AMR. Based on the status of this signal the AMR controls the state of the PWR/ALM LED on the fan module.

LED Status Combinations for All Modules (except GLI2, CSM, BBX2, MCC24E, MCC8E)

PWR/ALM LED

The following list describes the states of the module status indicator.

- Solid GREEN – module operating in a normal (fault free) condition.
- Solid RED – module is operating in a fault (alarm) condition due to electrical hardware failure.

Note that a fault (alarm) indication may or may not be due to a complete module failure and normal service may or may not be reduced or interrupted.

DC/DC Converter LED Status Combinations

The PWR CNVTR has its own alarm (fault) detection circuitry that controls the state of the PWR/ALM LED.

PWR/ALM LED

The following list describes the states of the bi-color LED.

- Solid GREEN – module operating in a normal (fault free) condition.
- Solid RED – module is operating in a fault (alarm) condition due to electrical hardware problem.

CSM LED Status Combinations

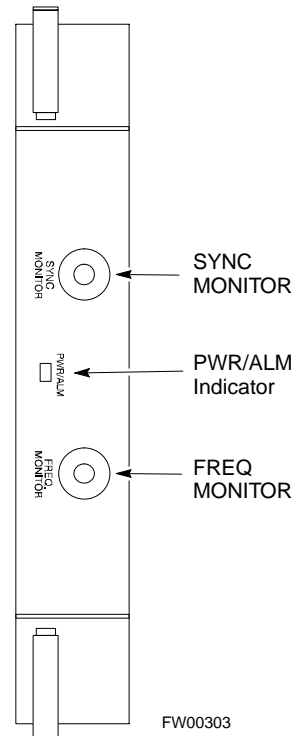
PWR/ALM LED

The CSMs include on-board alarm detection. Hardware and software/firmware alarms are indicated via the front panel indicators.

After the memory tests, the CSM loads OOS-RAM code from the Flash EPROM, if available. If not available, the OOS-ROM code is loaded from the Flash EPROM.

- Solid GREEN – module is INS_ACT or INS_STBY no alarm.
- Solid RED – Initial power up or module is operating in a fault (alarm) condition.
- Slowly Flashing GREEN – OOS_ROM no alarm.
- Long RED/Short GREEN – OOS_ROM alarm.
- Rapidly Flashing GREEN – OOS_RAM no alarm or INS_ACT in DUMB mode.
- Short RED/Short GREEN – OOS_RAM alarm.
- Long GREEN/Short RED – INS_ACT or INS_STBY alarm.
- Off – no DC power or on-board fuse is open.
- Solid YELLOW – After a reset, the CSMs begin to boot. During SRAM test and Flash EPROM code check, the LED is yellow. (If SRAM or Flash EPROM fail, the LED changes to a solid RED and the CSM attempts to reboot.)

Figure 6-1: CSM Front Panel Indicators & Monitor Ports



. . . continued on next page

FREQ Monitor Connector

A test port provided at the CSM front panel via a BNC receptacle allows monitoring of the 19.6608 MHz clock generated by the CSM. When both CSM 1 and CSM 2 are in an in-service (INS) condition, the CSM 2 clock signal frequency is the same as that output by CSM 1.

The clock is a sine wave signal with a minimum amplitude of +2 dBm (800 mVpp) into a 50 Ω load connected to this port.

SYNC Monitor Connector

A test port provided at the CSM front panel via a BNC receptacle allows monitoring of the “Even Second Tick” reference signal generated by the CSMs.

At this port, the reference signal is a TTL active high signal with a pulse width of 153 nanoseconds.

MMI Connector – Only accessible behind front panel. The RS-232 MMI port connector is intended to be used primarily in the development or factory environment, but may be used in the field for debug/maintenance purposes.

GLI2 LED Status Combinations

The GLI2 module has indicators, controls and connectors as described below and shown in Figure 6-2.

The indicators and controls consist of:

- Four LEDs
- One pushbutton

ACTIVE LED

Solid GREEN – GLI2 is active. This means that the GLI2 has shelf control and is providing control of the digital interfaces.

Off – GLI2 is not active (i.e., Standby). The mate GLI2 should be active.

MASTER LED

- Solid GREEN – GLI2 is Master (sometimes referred to as MGLI2).
- Off – GLI2 is non-master (i.e., Slave).

ALARM LED

- Solid RED – GLI2 is in a fault condition or in reset.
- While in reset transition, STATUS LED is OFF while GLI2 is performing ROM boot (about 12 seconds for normal boot).
- While in reset transition, STATUS LED is ON while GLI2 is performing RAM boot (about 4 seconds for normal boot).
- Off – No Alarm.

STATUS LED

- Flashing GREEN– GLI2 is in service (INS), in a stable operating condition.
- On – GLI2 is in OOS RAM state operating downloaded code.
- Off – GLI2 is in OOS ROM state operating boot code.

SPANS LED

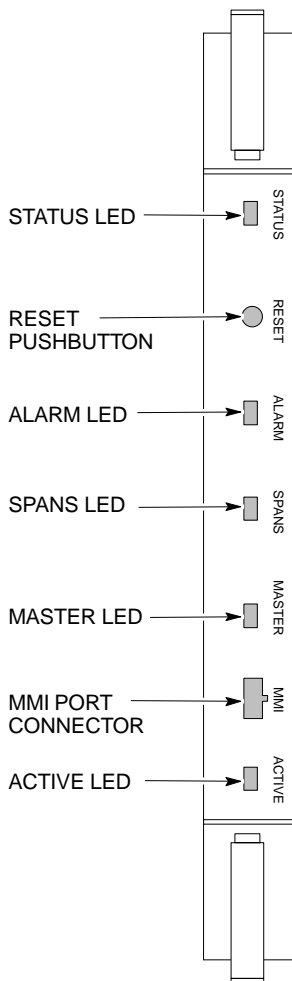
- Solid GREEN – Span line is connected and operating.
- Solid RED – Span line is disconnected or a fault condition exists.

GLI2 Pushbuttons and Connectors

RESET Pushbutton – Depressing the RESET pushbutton causes a partial reset of the CPU and a reset of all board devices. GLI2 will be placed in the OOS_ROM state

MMI Connector – The RS-232MMI port connector is intended to be used primarily in the development or factory environment but may be used in the field for debug/maintenance purposes.

Figure 6-2: GLI2 Front Panel Operating Indicators



LED	OPERATING STATUS
STATUS	OFF – operating normally ON – briefly during power-up when the Alarm LED turns OFF. SLOW GREEN – when the GLI2 is INS (in-service)
RESET	All functions on the GLI2 are reset when pressing and releasing the switch.
ALARM	OFF – operating normally ON – briefly during power-up when the Alarm LED turns OFF. SLOW GREEN – when the GLI2 is INS (in-service)
SPANS	OFF – card is powered down, in initialization, or in standby GREEN – operating normally YELLOW – one or more of the equipped initialized spans is receiving a remote alarm indication signal from the far end RED – one or more of the equipped initialized spans is in an alarm state
MASTER	The pair of GLI2 cards include a redundant status. The card in the top shelf is designated by hardware as the active card; the card in the bottom shelf is in the standby mode. ON – operating normally in active card OFF – operating normally in standby card
MMI PORT CONNECTOR	An RS-232, serial, asynchronous communications link for use as an MMI port. This port supports 300 baud, up to a maximum of 115,200 baud communications.
ACTIVE	Shows the operating status of the redundant cards. The redundant card toggles automatically if the active card is removed or fails ON – active card operating normally OFF – standby card operating normally

FW00225

BBX LED Status Combinations

PWR/ALM LED

The BBX module has its own alarm (fault) detection circuitry that controls the state of the PWR/ALM LED.

The following list describes the states of the bi-color LED:

- Solid GREEN – INS_ACT no alarm
- Solid RED Red – initializing or power-up alarm
- Slowly Flashing GREEN – OOS_ROM no alarm
- Long RED/Short GREEN – OOS_ROM alarm
- Rapidly Flashing GREEN – OOS_RAM no alarm
- Short RED/Short GREEN – OOS_RAM alarm
- Long GREEN/Short RED – INS_ACT alarm

MCC LED Status Combinations

The MCC module has LED indicators and connectors as described below. See Figure 6-3. Note that the figure does not show the connectors as they are concealed by the removable lens.

The LED indicators and their states are as follows:

PWR/ALM LED

- RED – fault on module

ACTIVE LED

- Off – module is inactive, off-line, or not processing traffic.
- Slowly Flashing GREEN – OOS_ROM no alarm.
- Rapidly Flashing Green – OOS_RAM no alarm.
- Solid GREEN – module is INS_ACT, on-line, processing traffic.

PWR/ALM and ACTIVE LEDs

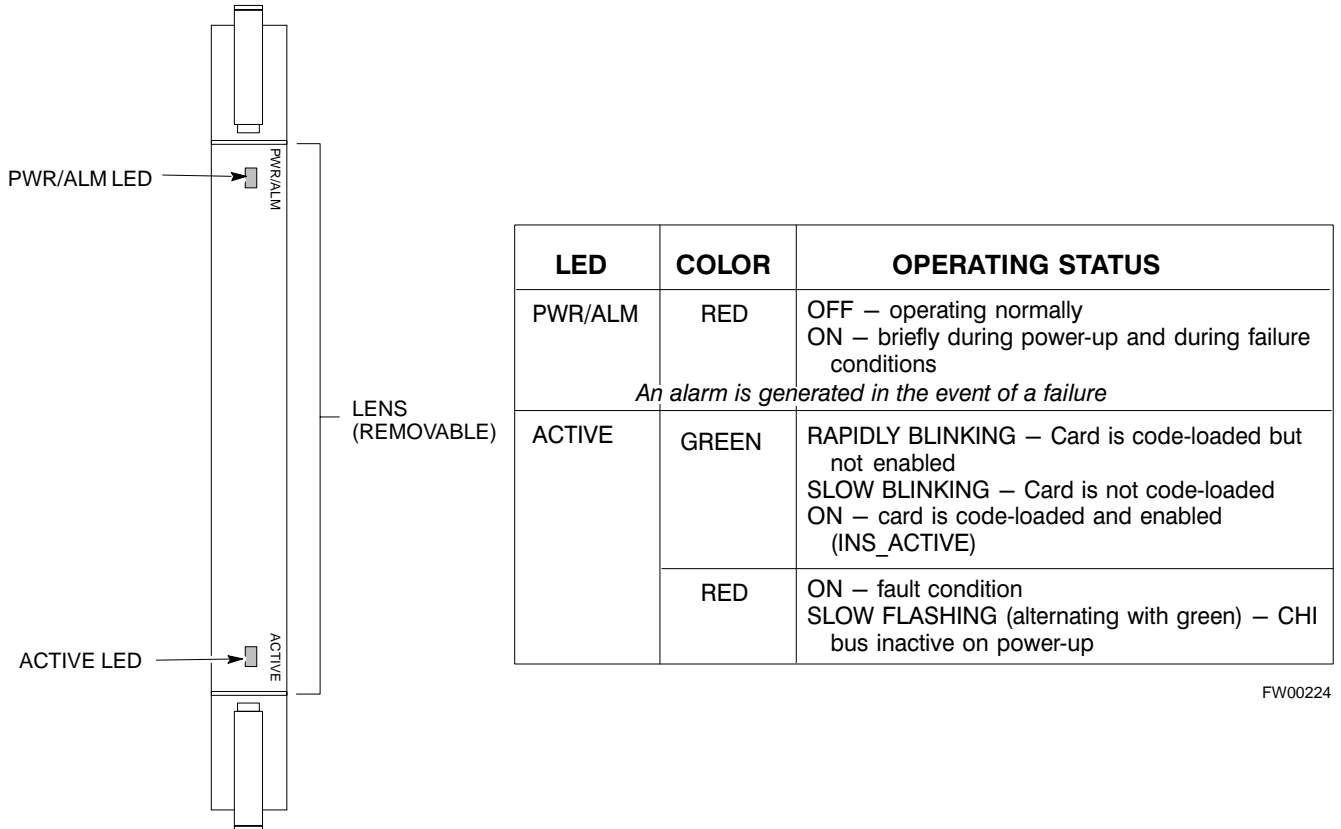
- Solid RED – module is powered but is in reset or the BCP is inactive.

MMI Connectors

- The RS-232 MMI port connector (four-pin) is intended to be used primarily in the development or factory environment but may be used in the field for debugging purposes.
- The RJ-11 ethernet port connector (eight-pin) is intended to be used primarily in the development environment but may be used in the field for high data rate debugging purposes.

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Figure 6-3: MCC24/8E Front Panel LEDs and LED Indicators



FW00224

6

LPA Shelf LED Status Combinations

LPA Module LED

Each LPA module contains a bi-color LED just above the MMI connector on the ETIB module. Interpret this LED as follows:

- GREEN — LPA module is active and is reporting no alarms (Normal condition).
- Flashing GREEN/RED — LPA module is active but is reporting an low input power condition. If no BBX is keyed, this is normal and does not constitute a failure.
- Flashing RED — LPA is in alarm.

Basic Troubleshooting – Span Control Link

Span Problems (No Control Link)

Follow the procedure in Table 6-29 when troubleshooting a control link failure.

Table 6-29: Troubleshooting Control Link Failure

✓	Step	Action
	1	Verify the span settings using the <code>span_view</code> command on the active master GLI2 MMI port. If these are set correctly, verify the <code>edlc</code> parameters using the <code>show</code> command. Any alarms conditions indicate that the span is not operating correctly. <ul style="list-style-type: none">– Try looping back the span line from the DSX panel back to the mobility manager (MM) and verify that the looped signal is good.– Listen for control tone on appropriate timeslot from base site and MM.

Appendix A: Data Sheets
Appendix Content

Appendix A: Optimization (Pre-ATP) Data Sheets

Verification of Test Equipment Used	A-1
Site Checklist	A-2
Preliminary Operations	A-2
Pre-Power and Initial Power Tests	A-3
General Optimization Checklist	A-4
GPS Receiver Operation	A-5
LFR Receiver Operation	A-6
LPA IM Reduction	A-7
TX BLO / Power Output Verification for 3-Sector Configurations ...	A-8
TX BLO / Power Output Verification for 6-Sector Configurations ...	A-13
TX Antenna VSWR	A-15
RX Antenna VSWR	A-16
Alarm Verification	A-16
C-CCP Shelf	A-16
LPAs	A-17

Appendix A: Optimization (Pre-ATP) Data Sheets – continued

Site Checklist

Table A-2: Site Checklist			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Deliveries	Per established procedures	
<input type="checkbox"/>	Floor Plan	Verified	
<input type="checkbox"/>	Inter Frame Cables:		
<input type="checkbox"/>	Ethernet	Per procedure	
<input type="checkbox"/>	Frame Ground	Per procedure	
<input type="checkbox"/>	Power	Per procedure	
<input type="checkbox"/>	Factory Data:		
<input type="checkbox"/>	BBX	Per procedure	
<input type="checkbox"/>	Test Panel	Per procedure	
<input type="checkbox"/>	RFDS	Per procedure	
<input type="checkbox"/>	Site Temperature		
<input type="checkbox"/>	Dress Covers/Brackets		

Preliminary Operations

Table A-3: Preliminary Operations			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Shelf ID Dip Switches	Per site equipage	
<input type="checkbox"/>	Ethernet LAN verification	Verified per procedure	

Comments: _____

Pre-Power and Initial Power Tests

Table A3a: Pre-power Checklist			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Pre-power-up tests	Verify power supply output voltage at the top of each BTS frame is within specifications	
<input type="checkbox"/>	Internal Cables:		
<input type="checkbox"/>	ISB (all cages)	verified	
<input type="checkbox"/>	CSM (all cages)	verified	
<input type="checkbox"/>	Power (all cages)	verified	
	Ethernet Connectors		
<input type="checkbox"/>	LAN A ohms	verified	
<input type="checkbox"/>	LAN B ohms	verified	
<input type="checkbox"/>	LAN A shield	isolated	
<input type="checkbox"/>	LAN B shield	isolated	
<input type="checkbox"/>	Ethernet Boots	installed	
<input type="checkbox"/>	Air Impedance Cage (single cage)	installed	
<input type="checkbox"/>	Initial power-up tests	Verify power supply output voltage at the top of each BTS frame is within specifications:	

Comments: _____

Appendix A: Optimization (Pre-ATP) Data Sheets – continued

General Optimization Checklist

Table A3b: Pre-power Checklist			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	LEDs	illuminated	
<input type="checkbox"/>	Frame fans	operational	
<input type="checkbox"/>	LMF to BTS Connection		
<input type="checkbox"/>	Preparing the LMF	per procedure	
<input type="checkbox"/>	Log into the LMF PC	per procedure	
<input type="checkbox"/>	Create site specific BTS directory	per procedure	
<input type="checkbox"/>	Download device loads	per procedure	
<input type="checkbox"/>	Ping LAN A	per procedure	
<input type="checkbox"/>	Ping LAN B	per procedure	
<input type="checkbox"/>	Download/Enable MGLI2s	per procedure	
<input type="checkbox"/>	Download/Enable GLI2s	per procedure	
<input type="checkbox"/>	Set Site Span Configuration	per procedure	
<input type="checkbox"/>	Download CSMs	per procedure	
<input type="checkbox"/>	Enable CSMs	per procedure	
<input type="checkbox"/>	Enable CSMs	per procedure	
<input type="checkbox"/>	Download/Enable MCCs*	per procedure	
<input type="checkbox"/>	Download BBXs*	per procedure	
<input type="checkbox"/>	Download TSU (in RFDS) Program TSU NAM	per procedure	
<input type="checkbox"/>	Test Set Calibration	per procedure	

*MCCs may be MCC8Es, MCC24s or MCC-1Xs. BBXs may be BBXs or BBX-1Xs

Comments: _____

GPS Receiver Operation

Table A-4: GPS Receiver Operation			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	GPS Receiver Control Task State: tracking satellites	Verify parameter	
<input type="checkbox"/>	Initial Position Accuracy:	Verify Estimated or Surveyed	
<input type="checkbox"/>	Current Position: lat lon height	RECORD in msec and cm also convert to deg min sec	
<input type="checkbox"/>	Current Position: satellites tracked Estimated: (>4) satellites tracked,(>4) satellites visible Surveyed: (≥1) satellite tracked,(>4) satellites visible	Verify parameter as appropriate:	
<input type="checkbox"/>	GPS Receiver Status:Current Dilution of Precision (PDOP or HDOP): (<30)	Verify parameter	
<input type="checkbox"/>	Current reference source: Number: 0; Status: Good; Valid: Yes	Verify parameter	

Comments: _____

Appendix A: Optimization (Pre-ATP) Data Sheets – continued

LFR Receiver Operation

Table A-5: LFR Receiver Operation			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Station call letters M X Y Z assignment.	as specified in site documentation	
<input type="checkbox"/>	SN ratio is > 8 dB		
<input type="checkbox"/>	LFR Task State: 1fr locked to station xxxx	Verify parameter	
<input type="checkbox"/>	Current reference source: Number: 1; Status: Good; Valid: Yes	Verify parameter	

Comments: _____

LPA IM Reduction

Table A-6: LPA IM Reduction							
OK	Parameter					Specification	Comments
	LPA #	CARRIER					
		4:1 & 2:1 3-Sector	2:1 6-Sector	Dual BP 3-Sector	Dual BP 6-Sector		
<input type="checkbox"/>	1A	C1	C1	C1	C1	No Alarms	
<input type="checkbox"/>	1B	C1	C1	C1	C1	No Alarms	
<input type="checkbox"/>	1C	C1	C1	C1	C1	No Alarms	
<input type="checkbox"/>	1D	C1	C1	C1	C1	No Alarms	
<input type="checkbox"/>	2A	C2	C2	C2		No Alarms	
<input type="checkbox"/>	2B	C2	C2	C2		No Alarms	
<input type="checkbox"/>	2C	C2	C2	C2		No Alarms	
<input type="checkbox"/>	2D	C2	C2	C2		No Alarms	
<input type="checkbox"/>	3A	C3	C1		C1	No Alarms	
<input type="checkbox"/>	3B	C3	C1		C1	No Alarms	
<input type="checkbox"/>	3C	C3	C1		C1	No Alarms	
<input type="checkbox"/>	3D	C3	C1		C1	No Alarms	
<input type="checkbox"/>	4A	C4	C2			No Alarms	
<input type="checkbox"/>	4B	C4	C2			No Alarms	
<input type="checkbox"/>	4C	C4	C2			No Alarms	
<input type="checkbox"/>	4D	C4	C2			No Alarms	

Comments: _____

Appendix A: Optimization (Pre-ATP) Data Sheets – continued

**TX Bay Level Offset / Power
Output Verification for
3-Sector Configurations**

- 1-Carrier**
- 2-Carrier Non-adjacent Channels**
- 4-Carrier Non-adjacent Channels**

Table A-7: TX BLO Calibration (3-Sector: 1-Carrier, 2-Carrier and 4-Carrier Non-adjacent Channels)

OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibrate carrier 1	TX Bay Level Offset = 37 dB (± 4 dB) prior to calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibrate carrier 2	TX Bay Level Offset = 37 dB (± 4 dB) prior to calibration	BBX-7, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibrate carrier 3	TX Bay Level Offset = 37 dB (± 4 dB) prior to calibration	BBX-4, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-5, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-6, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibrate carrier 4	TX Bay Level Offset = 37 dB (± 4 dB) prior to calibration	BBX-10, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-11, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-12, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB

... continued on next page

Table A-7: TX BLO Calibration (3-Sector: 1-Carrier, 2-Carrier and 4-Carrier Non-adjacent Channels)

OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibration Audit carrier 1	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 2	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-7, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 3	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-4, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-5, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-6, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 4	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-10, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-11, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-12, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB

Comments: _____

Appendix A: Optimization (Pre-ATP) Data Sheets – continued

2-Carrier Adjacent Channel

Table A-8: TX Bay Level Offset Calibration (3-Sector: 2-Carrier Adjacent Channels)			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibrate carrier 1	TX Bay Level Offset = 42 dB (typical), 38 dB (minimum) prior to calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibrate carrier 2	TX Bay Level Offset = 42 dB (typical), 38 dB (minimum) prior to calibration	BBX-7, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 1	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 2	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-7, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB

Comments: _____

3-Carrier Adjacent Channels
4-Carrier Adjacent Channels

Table A-9: TX Bay Level Offset Calibration (3-Sector: 3 or 4-Carrier Adjacent Channels)

OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibrate carrier 1	TX Bay Level Offset = 37 dB before calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibrate carrier 2	TX Bay Level Offset = 37 dB before calibration	BBX-7, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibrate carrier 3	TX Bay Level Offset = 37 dB before calibration	BBX-4, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-5, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-6, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB
<input type="checkbox"/>	Calibrate carrier 4	TX Bay Level Offset = 37 dB before calibration	BBX-10, ANT-4 = ___ dB BBX-3, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-11, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-12, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 1	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB

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Appendix A: Optimization (Pre-ATP) Data Sheets – continued

Table A-9: TX Bay Level Offset Calibration (3-Sector: 3 or 4-Carrier Adjacent Channels)			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibration Audit carrier 2	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-7, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 3	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-4, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-5, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-6, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 4	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-10, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-11, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-12, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB

Comments: _____

**TX Bay Level Offset / Power
Output Verification for
6-Sector Configurations**

**1-Carrier
2-Carrier Non-adjacent Channels**

Table A-10: TX BLO Calibration (6-Sector: 1-Carrier, 2-Carrier Non-adjacent Channels)			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibrate carrier 1	TX Bay Level Offset = 42 dB (typical), 38 dB (minimum) prior to calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>			BBX-4, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-5, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-6, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB
<input type="checkbox"/>	Calibrate carrier 2	TX Bay Level Offset = 42 dB (typical), 38 dB (minimum) prior to calibration	BBX-7, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>			BBX-10, ANT-4 = ___ dB BBX-3, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-11, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-12, ANT-6 = ___ dB BBX-r, ANT-5 = ___ dB

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Appendix A: Optimization (Pre-ATP) Data Sheets – continued

Table A-10: TX BLO Calibration (6-Sector: 1-Carrier, 2-Carrier Non-adjacent Channels)			
OK	Parameter	Specification	Comments
<input type="checkbox"/>	Calibration Audit carrier 1	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-1, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-2, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-3, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>			BBX-4, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-5, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-6, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB
<input type="checkbox"/>	Calibration Audit carrier 2	0 dB (± 0.5 dB) for gain set resolution post calibration	BBX-7, ANT-1 = ___ dB BBX-r, ANT-1 = ___ dB
<input type="checkbox"/>			BBX-8, ANT-2 = ___ dB BBX-r, ANT-2 = ___ dB
<input type="checkbox"/>			BBX-9, ANT-3 = ___ dB BBX-r, ANT-3 = ___ dB
<input type="checkbox"/>			BBX-10, ANT-4 = ___ dB BBX-r, ANT-4 = ___ dB
<input type="checkbox"/>			BBX-11, ANT-5 = ___ dB BBX-r, ANT-5 = ___ dB
<input type="checkbox"/>			BBX-12, ANT-6 = ___ dB BBX-r, ANT-6 = ___ dB

Comments: _____

TX Antenna VSWR

Table A-11: TX Antenna VSWR			
OK	Parameter	Specification	Data
<input type="checkbox"/>	VSWR – Antenna 1	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 2	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 3	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 4	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 5	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 6	< (1.5 : 1)	

Comments: _____

Appendix A: Optimization (Pre-ATP) Data Sheets – continued

RX Antenna VSWR

Table A-12: RX Antenna VSWR			
OK	Parameter	Specification	Data
<input type="checkbox"/>	VSWR – Antenna 1	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 2	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 3	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 4	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 5	< (1.5 : 1)	
<input type="checkbox"/>	VSWR – Antenna 6	< (1.5 : 1)	

Comments: _____

Alarm Verification

Table A-13: CDI Alarm Input Verification			
OK	Parameter	Specification	Data
<input type="checkbox"/>	Verify CDI alarm input operation per Table 3-1.	BTS Relay #XX – Contact Alarm Sets/Clears	

Comments: _____

Appendix A: Site Serial Number Check List



Date _____

Site _____

C-CCP Shelf

Site I/O A & B

C-CCP Shelf

CSM-1

CSM-2

HSO

CCD-1

CCD-2

AMR-1

AMR-2

MPC-1

MPC-2

Fans 1-3

GLI2-1

GLI2-2

BBX-1

BBX-2

BBX-3

BBX-4

BBX-5

BBX-6

BBX-7

BBX-8

BBX-9

BBX-10

BBX-11

BBX-12

BBX-r

MCC-1

MCC-2

MCC-3

MCC-4

MCC-5

MCC-6

MCC-7

MCC-8

MCC-9

MCC-10

Appendix A: Site Serial Number Check List – continued

CIO _____
SWITCH _____
PS-1 _____
PS-2 _____
PS-3 _____

LPAs

LPA 1A _____
LPA 1B _____
LPA 1C _____
LPA 1D _____
LPA 2A _____
LPA 2B _____
LPA 2C _____
LPA 2D _____
LPA 3A _____
LPA 3B _____
LPA 3C _____
LPA 3D _____
LPA 4A _____
LPA 4B _____
LPA 4C _____
LPA 4D _____

Appendix B: FRU Optimization/ATP Test Matrix



Appendix Content

Appendix B: FRU Optimization/ATP Test Matrix	B-1
Usage & Background	B-1
Detailed Optimization/ATP Test Matrix	B-2

FRU Optimization/ATP Test Matrix

Usage & Background

Periodic maintenance of a site may also mandate re-optimization of specific portions of the site. An outline of some basic guidelines is included in the following tables.



IMPORTANT

Re-optimization steps listed for any assembly detailed in the tables below must be performed *anytime* an RF cable associated with it is replaced.

Detailed Optimization/ATP Test Matrix

Table B-1 outlines in more detail the tests that would need to be performed if one of the BTS components were to fail and be replaced. It is also assumed that all modules are placed OOS-ROM via the LMF until full redundancy of all applicable modules is implemented.

The following guidelines should also be noted when using this table.



IMPORTANT

Not every procedure required to bring the site back in service is indicated in Table B-1. It is meant to be used as a guideline **ONLY**. The table assumes that the user is familiar enough with the BTS Optimization/ATP procedure to understand which test equipment set ups, calibrations, and BTS site preparation will be required before performing the Table # procedures referenced.

Various passive BTS components (such as the DRDCs, filter; etc.) only require a TX calibration audit to be performed in lieu of a full path calibration. If the TX path calibration audit fails, the entire RF path calibration will need to be repeated. If the RF path calibration fails, further troubleshooting is warranted.

Whenever any C-CCP BACKPLANE is replaced, it is assumed that only power to the C-CCP shelf being replaced is turned off via the breaker supplying that shelf.

NOTE

If any significant change in signal level results from any component being replaced in the RX or TX signal flow paths, it would be identified by re-running the RX and TX calibration audit command.

When the CIO is replaced, the C-CCP shelf remains powered up. The BBX boards may need to be removed, then re-installed into their

FRU Optimization/ATP Test Matrix – continued

original slots, and re-downloaded (code and BLO data). RX and TX calibration audits should then be performed.

Table B-1: SC 4812ET BTS Optimization and ATP Test Matrix

Doc Tbl #	Description	DRDC or TRDC	RX Cables	TX Cables	MPC / EMPC	CIO	SCCP Shelf Assembly (Backplane)	BBX2/BBX-1X	MCC24E/MCC8E/MCC-1X	CSM/GPS	LFR	HSO/HSOX	50-pair Punchblock w/RGPS	RGD/20-pair Punchblock w/RGD	CCD Card	GLI2	ETIB or Associated Cables	LPAC Cable	LPA or LPA Trunking Module	LPA Bandpass Filter or Combiner	Switch Card	RFDS cables	RFDS	
Table 3-20/ Table 3-21/	Download Code/Data						•	•	•	•						•							•	
Table 3-23	Enable CSMs						•			•			•	•			∞							
Table 3-26	GPS & HSO Initialization / Verification						•			•	•	•	•	•	•		∞							
Table 3-27	LFR Initialization / Verification						•				•				•									
Table 3-41	TX Path Calibration	4	4			1	1	4								*		3	3	4	7			
Table 3-42	Download Offsets to BBX	4						1	4							*								
Table 3-43	TX Path Audit	4	4			1	1	4								*			3	4	7			
Table 3-52	RFDS Path Calibration and Offset Data Download	6	5	4	5	1	1	6								*			3	4		6	6	
Table 4-1	Spectral Purity TX Mask	4					1	4								*			*	*	*			
Table 4-1	Waveform Quality (rho)	4				*	1	4		*					*	*	1		*	*				
Table 4-1	Pilot Time Offset	4				*	1	4		*					*	*			*	*				
Table 4-1	Code Domain Power / Noise Floor	4						1	4	8	8	8			8	*			*	*				
Table 4-1	FER Test	5	5	5	2	2	5	8	8	8					8	*					7			
Table 3-54/ Table 3-63	Alarm Tests																•							

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Table B-1: SC 4812ET BTS Optimization and ATP Test Matrix

Doc Tbl #	Description	DRDC or TRDC	RX Cables	TX Cables	MPC / EMPC	CIO	SCCP Shelf Assembly (Backplane)	BBX2/BBX-1X	MCC24E/MCC8E/MCC-1X	CSM/GPS	LFR	HSO/HSOX	50-pair Punchblock w/RGPS	RGD/20-pair Punchblock w/RGD	CCD Card	GLI2	ETIB or Associated Cables	LPAC Cable	LPA or LPA Trunking Module	LPA Bandpass Filter or Combiner	Switch Card	RFDS cables	RFDS
OPTIMIZATION AND TEST LEGEND:																							
<ul style="list-style-type: none"> ● Required * Perform if determined necessary for additional fault isolation, repair assurance, or required for site certification. ** Replace power supply modules one at a time so that power to the C-CCP shelf is not interrupted. If power to the shelf is lost, all cards in the shelf must be downloaded again. <ol style="list-style-type: none"> 1. Perform on all carrier and sector TX paths to the C-CCP cage. 2. Perform on all carrier and sector RX paths to the C-CCP cage. 3. Perform on all primary and redundant TX paths of the affected carrier. 4. Perform on the affected carrier and sector TX path(s) (BBXR replacement affects <i>all</i> carrier and sector TX paths) 5. Perform on the affected carrier and sector RX path(s) (BBXR replacement affects <i>all</i> carrier RX paths) 6. Perform on <i>all RF paths</i> of the affected carrier and sector (RFDS replacement affects all carriers) 7. Perform with <i>redundant BBX</i> for <i>at least</i> one sector on one carrier. 8. Verify performance by performing on one sector of one carrier only. 9. Perform only if RGD/RGPS, LFR antenna, or HSO or LFR expansion was installed 10. Verify performance by performing testing on one sector of <i>each</i> carrier. 																							



Appendix C: BBX Gain Set Point vs. BTS Output Considerations

Appendix Content

Usage & Background	C-1
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Appendix C: BBX Gain Set Point vs. BTS Output Considerations

Usage & Background

Table C-1 outlines the relationship between the *total* of all code domain channel element gain settings (digital root sum of the squares) and the BBX Gain Set Point between 33.0 dBm and 44.0 dBm. The resultant RF output (as measured at the top of the BTS in dBm) is shown in the table. The table assumes that the BBX Bay Level Offset (BLO) values have been calculated.

As an illustration, consider a BBX keyed up to produce a CDMA carrier with only the Pilot channel (no MCCs forward link enabled). Pilot gain is set to 262. In this case, the BBX Gain Set Point is shown to correlate exactly to the actual RF output anywhere in the 33 to 44 dBm output range. (This is the level used to calibrate the BTS).



Table C-1: BBX Gain Set Point vs. Actual BTS Output (in dBm)

dBm↗ Gain↘	44	43	42	41	40	39	38	37	36	35	34	33
541	–	–	–	–	–	–	–	43.3	42.3	41.3	40.3	39.3
533	–	–	–	–	–	–	–	43.2	42.2	41.2	40.2	39.2
525	–	–	–	–	–	–	–	43	42	41	40	39
517	–	–	–	–	–	–	–	42.9	41.9	40.9	39.9	38.9
509	–	–	–	–	–	–	–	42.8	41.8	40.8	39.8	38.8
501	–	–	–	–	–	–	–	42.6	41.6	40.6	39.6	38.6
493	–	–	–	–	–	–	43.5	42.5	41.5	40.5	39.5	38.5
485	–	–	–	–	–	–	43.4	42.4	41.4	40.4	39.4	38.4
477	–	–	–	–	–	–	43.2	42.2	41.2	40.2	39.2	38.2
469	–	–	–	–	–	–	43.1	42.1	41.1	40.1	39.1	38.1
461	–	–	–	–	–	–	42.9	41.9	40.9	39.9	38.9	37.9
453	–	–	–	–	–	–	42.8	41.8	40.8	39.8	38.8	37.8
445	–	–	–	–	–	43.6	42.6	41.6	40.6	39.6	38.6	37.6
437	–	–	–	–	–	43.4	42.4	41.4	40.4	39.4	38.4	37.4
429	–	–	–	–	–	43.3	42.3	41.3	40.3	39.3	38.3	37.3
421	–	–	–	–	–	43.1	42.1	41.1	40.1	39.1	38.1	37.1
413	–	–	–	–	–	43	42	41	40	39	38	37
405	–	–	–	–	–	42.8	41.8	40.8	39.8	38.8	37.8	36.8
397	–	–	–	–	43.6	42.6	41.6	40.6	39.6	38.6	37.6	36.6
389	–	–	–	–	43.4	42.4	41.4	40.4	39.4	38.4	37.4	36.4

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Appendix C: BBX2 Gain Set Point vs. BTS Output Considerations – continued

Table C-1: BBX Gain Set Point vs. Actual BTS Output (in dBm)

dBm↗ Gain↘	44	43	42	41	40	39	38	37	36	35	34	33
381	–	–	–	–	43.3	42.3	41.3	40.3	39.3	38.3	37.3	36.3
374	–	–	–	–	43.1	42.1	41.1	40.1	39.1	38.1	37.1	36.1
366	–	–	–	–	42.9	41.9	40.9	39.9	38.9	37.9	36.9	35.9
358	–	–	–	–	42.7	41.7	40.7	39.7	38.7	37.7	36.7	35.7
350	–	–	–	43.5	42.5	41.5	40.5	39.5	38.5	37.5	36.5	35.5
342	–	–	–	43.3	42.3	41.3	40.3	39.3	38.3	37.3	36.3	35.3
334	–	–	–	43.1	42.1	41.1	40.1	39.1	38.1	37.1	36.1	35.1
326	–	–	–	42.9	41.9	40.9	39.9	38.9	37.9	36.9	35.9	34.9
318	–	–	–	42.7	41.7	40.7	39.7	38.7	37.7	36.7	35.7	34.7
310	–	–	43.5	42.5	41.5	40.5	39.5	38.5	37.5	36.5	35.5	34.5
302	–	–	43.2	42.2	41.2	40.2	39.2	38.2	37.2	36.2	35.2	34.2
294	–	–	43	42	41	40	39	38	37	36	35	34
286	–	–	42.8	41.8	40.8	39.8	38.8	37.8	36.8	35.8	34.8	33.8
278	–	43.5	42.5	41.5	40.5	39.5	38.5	37.5	36.5	35.5	34.5	33.5
270	–	43.3	42.3	41.3	40.3	39.3	38.3	37.3	36.3	35.3	34.3	33.3
262	–	43	42	41	40	39	38	37	36	35	34	33
254	–	42.7	41.7	40.7	39.7	38.7	37.7	36.7	35.7	34.7	33.7	32.7
246	43.4	42.4	41.4	40.4	39.4	38.4	37.4	36.4	35.4	34.4	33.4	32.4
238	43.2	42.2	41.2	40.2	39.2	38.2	37.2	36.2	35.2	34.2	33.2	32.2
230	42.9	41.9	40.9	39.9	38.9	37.9	36.9	35.9	34.9	33.9	32.9	31.9
222	42.6	41.6	40.6	39.6	38.6	37.6	36.6	35.6	34.6	33.6	32.6	31.6
214	42.2	41.2	40.2	39.2	38.2	37.2	36.2	35.2	34.2	33.2	32.2	31.2

Appendix D: CDMA Operating Frequency Information

Appendix Content

1900 MHz PCS Channels	D-1
Calculating 1900 MHz Center Frequencies	D-2
800 MHz CDMA Channels	D-4
Calculating 800 MHz Center Frequencies	D-4



CDMA Operating Frequency Programming Information – North American PCS Bands

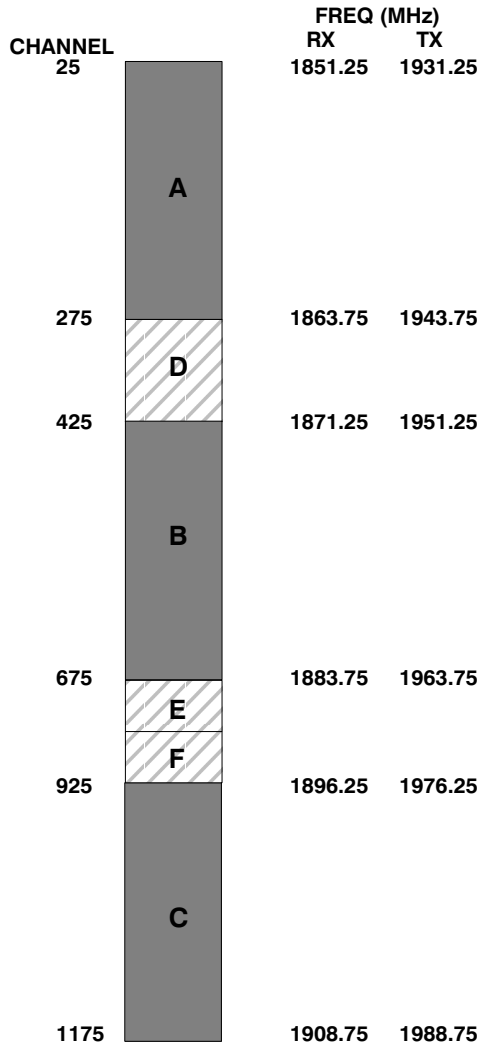
Introduction

Programming of each of the BTS BBX synthesizers is performed by the BTS GLIs via the CHI bus. This programming data determines the transmit and receive transceiver operating frequencies (channels) for each BBX2.

1900 MHz PCS Channels

Figure D-1 shows the valid channels for the North American PCS 1900 MHz frequency spectrum. There are 10 CDMA wireline or non-wireline band channels used in a CDMA system (unique per customer operating system).

Figure D-1: North America PCS Frequency Spectrum (CDMA Allocation)



FW00463



CDMA Operating Frequency Programming Information – North American Bands – continued

Calculating 1900 MHz Center Frequencies

Table D-1 shows selected 1900 MHz CDMA candidate operating channels, listed in both decimal and hexadecimal, and the corresponding transmit, and receive frequencies. Center frequencies (in MHz) for channels not shown in the table may be calculated as follows:

- $TX = 1930 + 0.05 * \text{Channel\#}$
Example: Channel 262
 $TX = 1930 + 0.05 * 262 = 1943.10 \text{ MHz}$
- $RX = TX - 80$
Example: Channel 262
 $RX = 1943.10 - 80 = 1863.10 \text{ MHz}$

Actual frequencies used depend on customer CDMA system frequency plan.

Each CDMA channel requires a 1.77 MHz frequency segment. The actual CDMA carrier is 1.23 MHz wide, with a 0.27 MHz guard band on both sides of the carrier.

Minimum frequency separation required between any CDMA carrier and the nearest NAMPS/AMPS carrier is 900 kHz (center-to-center).

Table D-1: 1900 MHz TX and RX Frequency vs. Channel

Channel Number		Transmit Frequency (MHz) Center Frequency	Receive Frequency (MHz) Center Frequency
Decimal	Hex		
25	0019	1931.25	1851.25
50	0032	1932.50	1852.50
75	004B	1933.75	1853.75
100	0064	1935.00	1855.00
125	007D	1936.25	1856.25
150	0096	1937.50	1857.50
175	00AF	1938.75	1858.75
200	00C8	1940.00	1860.00
225	00E1	1941.25	1861.25
250	00FA	1942.50	1862.50
275	0113	1943.75	1863.75
300	012C	1945.00	1865.00
325	0145	1946.25	1866.25
350	015E	1947.50	1867.50
375	0177	1948.75	1868.75
400	0190	1950.00	1870.00
425	01A9	1951.25	1871.25
450	01C2	1952.50	1872.50
475	01DB	1953.75	1873.75
500	01F4	1955.00	1875.00
525	020D	1956.25	1876.25
550	0226	1957.50	1877.50
575	023F	1958.75	1878.75

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CDMA Operating Frequency Programming Information – North American Bands – continued

Table D-1: 1900 MHz TX and RX Frequency vs. Channel

Channel Number		Transmit Frequency (MHz)	Receive Frequency (MHz)
Decimal	Hex	Center Frequency	Center Frequency
600	0258	1960.00	1880.00
625	0271	1961.25	1881.25
650	028A	1962.50	1882.50
675	02A3	1963.75	1883.75
700	02BC	1965.00	1885.00
725	02D5	1966.25	1886.25
750	02EE	1967.50	1887.50
775	0307	1968.75	1888.75
800	0320	1970.00	1890.00
825	0339	1971.25	1891.25
850	0352	1972.50	1892.50
875	036B	1973.75	1893.75
900	0384	1975.00	1895.00
925	039D	1976.25	1896.25
950	03B6	1977.50	1897.50
975	03CF	1978.75	1898.75
1000	03E8	1980.00	1900.00
1025	0401	1981.25	1901.25
1050	041A	1982.50	1902.50
1075	0433	1983.75	1903.75
1100	044C	1985.00	1905.00
1125	0465	1986.25	1906.25
1150	047E	1987.50	1807.50
1175	0497	1988.75	1908.75

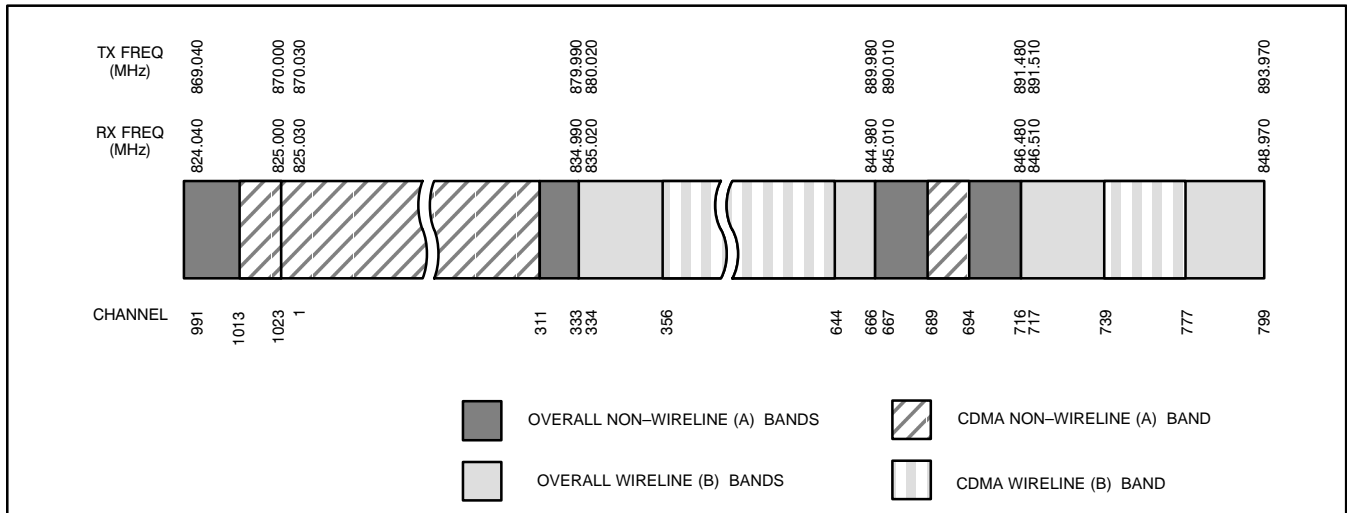
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CDMA Operating Frequency Programming Information – North American Bands – continued

800 MHz CDMA Channels

Figure D-2 shows the valid channels for the North American cellular telephone frequency spectrum. There are 10 CDMA wireline or non-wireline band channels used in a CDMA system (unique per customer operating system).

Figure D-2: North American Cellular Telephone System Frequency Spectrum (CDMA Allocation).



FW00402

Calculating 800 MHz Center Frequencies

Table D-2 shows selected 800 MHz CDMA candidate operating channels, listed in both decimal and hexadecimal, and the corresponding transmit, and receive frequencies. Center frequencies (in MHz) for channels not shown in the table may be calculated as follows:

- Channels 1–777
 $TX = 870 + 0.03 * \text{Channel\#}$
Example: Channel 262
 $TX = 870 + 0.03 * 262 = 877.86 \text{ MHz}$
- Channels 1013–1023
 $TX = 870 + 0.03 * (\text{Channel\#} - 1023)$
Example: Channel 1015
 $TX = 870 + 0.03 * (1015 - 1023) = 869.76 \text{ MHz}$
- $RX = TX - 45 \text{ MHz}$
Example: Channel 262
 $RX = 877.86 - 45 = 832.86 \text{ MHz}$

Table D-2: 800 MHz TX and RX Frequency vs. Channel

Channel Number		Transmit Frequency (MHz) Center Frequency	Receive Frequency (MHz) Center Frequency
Decimal	Hex		
1	0001	870.0300	825.0300
25	0019	870.7500	825.7500

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CDMA Operating Frequency Programming Information – North American Bands – continued

Table D-2: 800 MHz TX and RX Frequency vs. Channel

Channel Number		Transmit Frequency (MHz) Center Frequency	Receive Frequency (MHz) Center Frequency
Decimal	Hex		
50	0032	871.5000	826.5000
75	004B	872.2500	827.2500
100	0064	873.0000	828.0000
125	007D	873.7500	828.7500
150	0096	874.5000	829.5000
175	00AF	875.2500	830.2500
200	00C8	876.0000	831.0000
225	00E1	876.7500	831.7500
250	00FA	877.5000	832.5000
275	0113	878.2500	833.2500
300	012C	879.0000	834.0000
325	0145	879.7500	834.7500
350	015E	880.5000	835.5000
375	0177	881.2500	836.2500
400	0190	882.0000	837.0000
425	01A9	882.7500	837.7500
450	01C2	883.5000	838.5000
475	01DB	884.2500	839.2500
500	01F4	885.0000	840.0000
525	020D	885.7500	840.7500
550	0226	886.5000	841.5000
575	023F	887.2500	842.2500
600	0258	888.0000	843.0000
625	0271	888.7500	843.7500
650	028A	889.5000	844.5000
675	02A3	890.2500	845.2500
700	02BC	891.0000	846.0000
725	02D5	891.7500	846.7500
750	02EE	892.5000	847.5000
775	0307	893.2500	848.2500
NOTE			
Channel numbers 778 through 1012 are not used.			
1013	03F5	869.7000	824.7000
1023	03FF	870.0000	825.0000

D

Appendix E: PN Offset/I & Q Offset Register Programming Information

Appendix Content

PN Offset Background	E-1
PN Offset Usage	E-1



Appendix E: PN Offset Programming Information

PN Offset Background

All channel elements transmitted from a BTS in a particular 1.25 MHz CDMA channel are orthonogonally spread by 1 of 64 possible Walsh code functions; additionally, they are also spread by a quadrature pair of PN sequences unique to each sector.

Overall, the mobile uses this to differentiate multiple signals transmitted from the same BTS (and surrounding BTS) sectors, and to synchronize to the next strongest sector.

The PN offset per sector is stored on the BBXs, where the corresponding I & Q registers reside.

The PN offset values are determined on a per BTS/per sector(antenna) basis as determined by the appropriate cdf file content. A breakdown of this information is found in Table E-1.

PN Offset Usage

There are three basic RF chip delays currently in use. It is important to determine what RF chip delay is valid to be able to test the BTS functionality. This can be done by ascertaining if the CDF file `FineTxAdj` value was set to “on” when the MCC was downloaded with “image data”. The `FineTxAdj` value is used to compensate for the processing delay (approximately 20 μ S) in the BTS using any type of mobile meeting IS-97 specifications.

Observe the following guidelines:

- If the `FineTxAdj` value in the cdf file is 101 (65 HEX), the `FineTxAdj` has not been set. The I and Q values from the 0 table MUST be used.

If the `FineTxAdj` value in the cdf file is 213 (D5 HEX), `FineTxAdj` has been set for the *14 chip table*.

- If the `FineTxAdj` value in the cdf file is 197 (C5 HEX), `FineTxAdj` has been set for the *13 chip table*.



IMPORTANT

CDF file I and Q values can be represented in DECIMAL or HEX. If using HEX, add 0x before the HEX value. If necessary, convert HEX values in Table E-1 to decimal before comparing them to cdf file I & Q value assignments.

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- If you are using a Qualcomm mobile, use the I and Q values from the 13 chip delay table.
- If you are using a mobile that does not have the 1 chip offset problem, (any mobile meeting the IS-97 specification), use the 14 chip delay table.



IMPORTANT

If the wrong I and Q values are used with the wrong `FineTxAdj` parameter, system timing problems will occur. This will cause the energy transmitted to be “smeared” over several Walsh codes (instead of the single Walsh code that it was assigned to), causing erratic operation. Evidence of smearing is usually identified by Walsh channels not at correct levels or present when not selected in the Code Domain Power Test.

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)
0	17523	23459	4473	5BA3	29673	25581	73E9	63ED	4096	4096	1000	1000
1	32292	32589	7E24	7F4D	16146	29082	3F12	719A	9167	1571	23CF	0623
2	4700	17398	125C	43F6	2350	8699	092E	21FB	22417	7484	5791	1D3C
3	14406	26333	3846	66DD	7203	32082	1C23	7D52	966	6319	03C6	18AF
4	14899	4011	3A33	0FAB	19657	18921	4CC9	49E9	14189	2447	376D	098F
5	17025	2256	4281	08D0	28816	1128	7090	0468	29150	24441	71DE	5F79
6	14745	18651	3999	48DB	19740	27217	4D1C	6A51	18245	27351	4745	6AD7
7	2783	1094	0ADF	0446	21695	547	54BF	0223	1716	23613	06B4	5C3D
8	5832	21202	16C8	52D2	2916	10601	0B64	2969	11915	29008	2E8B	7150
9	12407	13841	3077	3611	18923	21812	49EB	5534	20981	5643	51F5	160B
10	31295	31767	7A3F	7C17	27855	28727	6CCF	7037	24694	28085	6076	6DB5
11	7581	18890	1D9D	49CA	24350	9445	5F1E	24E5	11865	18200	2E59	4718
12	18523	30999	485B	7917	30205	29367	75FD	72B7	6385	21138	18F1	5292
13	29920	22420	74E0	5794	14960	11210	3A70	2BCA	27896	21937	6CF8	55B1
14	25184	20168	6260	4EC8	12592	10084	3130	2764	25240	25222	6298	6286
15	26282	12354	66AA	3042	13141	6177	3355	1821	30877	109	789D	006D
16	30623	11187	779F	2BB3	27167	23525	6A1F	5BE5	30618	6028	779A	178C
17	15540	11834	3CB4	2E3A	7770	5917	1E5A	171D	26373	22034	6705	5612
18	23026	10395	59F2	289B	11513	23153	2CF9	5A71	314	15069	013A	3ADD
19	20019	28035	4E33	6D83	30409	30973	76C9	78FD	17518	4671	446E	123F
20	4050	27399	0FD2	6B07	2025	31679	07E9	7BBF	21927	30434	55A7	76E2
21	1557	22087	0615	5647	21210	25887	52DA	651F	2245	11615	08C5	2D5F
22	30262	2077	7636	081D	15131	18994	3B1B	4A32	18105	19838	46B9	4D7E
23	18000	13758	4650	35BE	9000	6879	2328	1ADF	8792	14713	2258	3979
24	20056	11778	4E58	2E02	10028	5889	272C	1701	21440	241	53C0	00F1
25	12143	3543	2F6F	0DD7	18023	18647	4667	48D7	15493	24083	3C85	5E13
26	17437	7184	441D	1C10	29662	3592	73DE	0E08	26677	7621	6835	1DC5
27	17438	2362	441E	093A	8719	1181	220F	049D	11299	19144	2C23	4AC8
28	5102	25840	13EE	64F0	2551	12920	09F7	3278	12081	1047	2F31	0417
29	9302	12177	2456	2F91	4651	23028	122B	59F4	23833	26152	5D19	6628
30	17154	10402	4302	28A2	8577	5201	2181	1451	20281	22402	4F39	5782
31	5198	1917	144E	077D	2599	19842	0A27	4D82	10676	21255	29B4	5307
32	4606	17708	11FE	452C	2303	8854	08FF	2296	16981	30179	4255	75E3
33	24804	10630	60E4	2986	12402	5315	3072	14C3	31964	7408	7CDC	1CF0
34	17180	6812	431C	1A9C	8590	3406	218E	0D4E	26913	115	6921	0073
35	10507	14350	290B	380E	17749	7175	4555	1C07	14080	1591	3700	0637
36	10157	10999	27AD	2AF7	16902	23367	4206	5B47	23842	1006	5D22	03EE
37	23850	25003	5D2A	61AB	11925	32489	2E95	7EE9	27197	32263	6A3D	7E07
38	31425	2652	7AC1	0A5C	27824	1326	6CB0	052E	22933	1332	5995	0534
39	4075	19898	0FEB	4DBA	22053	9949	5625	26DD	30220	12636	760C	315C
40	10030	2010	272E	07DA	5015	1005	1397	03ED	12443	4099	309B	1003
41	16984	25936	4258	6550	8492	12968	212C	32A8	19854	386	4D8E	0182
42	14225	28531	3791	6F73	18968	31109	4A18	7985	14842	29231	39FA	722F
43	26519	11952	6797	2EB0	25115	5976	621B	1758	15006	25711	3A9E	646F
44	27775	31947	6C7F	7CCB	26607	28761	67EF	7059	702	10913	02BE	2AA1
45	30100	25589	7594	63F5	15050	32710	3ACA	7FC6	21373	8132	537D	1FC4
46	7922	11345	1EF2	2C51	3961	22548	0F79	5814	23874	20844	5D42	516C
47	14199	28198	3777	6E26	19051	14099	4A6B	3713	3468	13150	0D8C	335E
48	17637	13947	44E5	367B	29602	21761	73A2	5501	31323	18184	7A5B	4708
49	23081	8462	5A29	210E	31940	4231	7CC4	1087	29266	19066	7252	4A7A
50	5099	9595	13EB	257B	22565	23681	5825	5C81	16554	29963	40AA	750B

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)
51	32743	4670	7FE7	123E	28195	2335	6E23	091F	22575	6605	582F	19CD
52	7114	14672	1BCA	3950	3557	7336	0DE5	1CA8	31456	29417	7AE0	72E9
53	7699	29415	1E13	72E7	24281	30543	5ED9	774F	8148	22993	1FD4	59D1
54	19339	20610	4B8B	5082	29717	10305	7415	2841	19043	27657	4A63	6C09
55	28212	6479	6E34	194F	14106	17051	371A	429B	25438	5468	635E	155C
56	29587	10957	7393	2ACD	26649	23386	6819	5B5A	10938	8821	2ABA	2275
57	19715	18426	4D03	47FA	30545	9213	7751	23FD	2311	20773	0907	5125
58	14901	22726	3A35	58C6	19658	11363	4CCA	2C63	7392	4920	1CE0	1338
59	20160	5247	4EC0	147F	10080	17411	2760	4403	30714	5756	77FA	167C
60	22249	29953	56E9	7501	31396	29884	7AA4	74BC	180	28088	00B4	6DB8
61	26582	5796	67D6	16A4	13291	2898	33EB	0B52	8948	740	22F4	02E4
62	7153	16829	1BF1	41BD	23592	28386	5C28	6EE2	16432	23397	4030	5B65
63	15127	4528	3B17	11B0	19547	2264	4C5B	08D8	9622	19492	2596	4C24
64	15274	5415	3BAA	1527	7637	17583	1DD5	44AF	7524	26451	1D64	6753
65	23149	10294	5A6D	2836	31974	5147	7CE6	141B	1443	30666	05A3	77CA
66	16340	17046	3FD4	4296	8170	8523	1FEA	214B	1810	15088	0712	3AF0
67	27052	7846	69AC	1EA6	13526	3923	34D6	0F53	6941	26131	1B1D	6613
68	13519	10762	34CF	2A0A	19383	5381	4BB7	1505	3238	15969	0CA6	3E61
69	10620	13814	297C	35F6	5310	6907	14BE	1AFB	8141	24101	1FCD	5E25
70	15978	16854	3E6A	41D6	7989	8427	1F35	20EB	10408	12762	28A8	31DA
71	27966	795	6D3E	031B	13983	20401	369F	4FB1	18826	19997	498A	4E1D
72	12479	9774	30BF	262E	18831	4887	498F	1317	22705	22971	58B1	59BB
73	1536	24291	0600	5EE3	768	24909	0300	614D	3879	12560	0F27	3110
74	3199	3172	0C7F	0C64	22511	1586	57EF	0632	21359	31213	536F	79ED
75	4549	2229	11C5	08B5	22834	19046	5932	4A66	30853	18780	7885	495C
76	17888	21283	45E0	5323	8944	26541	22F0	67AD	18078	16353	469E	3FE1
77	13117	16905	333D	4209	18510	28472	484E	6F38	15910	12055	3E26	2F17
78	7506	7062	1D52	1B96	3753	3531	0EA9	0DCB	20989	30396	51FD	76BC
79	27626	7532	6BEA	1D6C	13813	3766	35F5	0EB6	28810	24388	708A	5F44
80	31109	25575	7985	63E7	27922	32719	6D12	7FCF	30759	1555	7827	0613
81	29755	14244	743B	37A4	27597	7122	6BCD	1BD2	18899	13316	49D3	3404
82	26711	28053	6857	6D95	26107	30966	65FB	78F6	7739	31073	1E3B	7961
83	20397	30408	4FAD	76C8	30214	15204	7606	3B64	6279	6187	1887	182B
84	18608	5094	48B0	13E6	9304	2547	2458	09F3	9968	21644	26F0	548C
85	7391	16222	1CDF	3F5E	24511	8111	5FBF	1FAF	8571	9289	217B	2449
86	23168	7159	5A80	1BF7	11584	17351	2D40	43C7	4143	4624	102F	1210
87	23466	174	5BAA	00AE	11733	87	2DD5	0057	19637	467	4CB5	01D3
88	15932	25530	3E3C	63BA	7966	12765	1F1E	31DD	11867	18133	2E5B	46D5
89	25798	2320	64C6	0910	12899	1160	3263	0488	7374	1532	1CCE	05FC
90	28134	23113	6DE6	5A49	14067	25368	36F3	6318	10423	1457	28B7	05B1
91	28024	23985	6D78	5DB1	14012	24804	36BC	60E4	9984	9197	2700	23ED
92	6335	2604	18BF	0A2C	23951	1302	5D8F	0516	7445	13451	1D15	348B
93	21508	1826	5404	0722	10754	913	2A02	0391	4133	25785	1025	64B9
94	26338	30853	66E2	7885	13169	29310	3371	727E	22646	4087	5876	0FF7
95	17186	15699	4322	3D53	8593	20629	2191	5095	15466	31190	3C6A	79D6
96	22462	2589	57BE	0A1D	11231	19250	2BDF	4B32	2164	8383	0874	20BF
97	3908	25000	0F44	61A8	1954	12500	07A2	30D4	16380	12995	3FFC	32C3
98	25390	18163	632E	46F3	12695	27973	3197	6D45	15008	27438	3AA0	6B2E
99	27891	12555	6CF3	310B	26537	22201	67A9	56B9	31755	9297	7C0B	2451
100	9620	8670	2594	21DE	4810	4335	12CA	10EF	31636	1676	7B94	068C

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q
101	6491	1290	195B	050A	23933	645	5D7D	0285	25414	12596	6346	3134
102	16876	4407	41EC	1137	8438	18087	20F6	46A7	7102	19975	1BBE	4E07
103	17034	1163	428A	048B	8517	19577	2145	4C79	20516	20026	5024	4E3A
104	32405	12215	7E95	2FB7	28314	23015	6E9A	59E7	19495	8958	4C27	22FE
105	27417	7253	6B19	1C55	25692	16406	645C	4016	17182	19143	431E	4AC7
106	8382	8978	20BE	2312	4191	4489	105F	1189	11572	17142	2D34	42F6
107	5624	25547	15F8	63CB	2812	32729	0AFC	7FD9	25570	19670	63E2	4CD6
108	1424	3130	0590	0C3A	712	1565	02C8	061D	6322	30191	18B2	75EF
109	13034	31406	32EA	7AAE	6517	15703	1975	3D57	8009	5822	1F49	16BE
110	15682	6222	3D42	184E	7841	3111	1EA1	0C27	26708	22076	6854	563C
111	27101	20340	69DD	4F74	25918	10170	653E	27BA	6237	606	185D	025E
112	8521	25094	2149	6206	16756	12547	4174	3103	32520	9741	7F08	260D
113	30232	23380	7618	5B54	15116	11690	3B0C	2DAA	31627	9116	7B8B	239C
114	6429	10926	191D	2AAE	23902	5463	5D5E	1557	3532	12705	0DCC	31A1
115	27116	22821	69EC	5925	13558	25262	34F6	62AE	24090	17502	5E1A	445E
116	4238	31634	108E	7B92	2119	15817	0847	3DC9	20262	18952	4F26	4A08
117	5128	4403	1408	1133	2564	18085	0A04	46A5	18238	15502	473E	3C8E
118	14846	689	39FE	02B1	7423	20324	1CFF	4F64	2033	17819	07F1	459B
119	13024	27045	32E0	69A5	6512	31470	1970	7AEE	25566	4370	63DE	1112
120	10625	27557	2981	6BA5	17680	31726	4510	7BEE	25144	31955	6238	7CD3
121	31724	16307	7BEC	3FB3	15862	20965	3DF6	51E5	29679	30569	73EF	7769
122	13811	22338	35F3	5742	19241	11169	4B29	2BA1	5064	7350	13C8	1CB6
123	24915	27550	6153	6B9E	24953	13775	6179	35CF	27623	26356	6BE7	66F4
124	1213	22096	04BD	5650	21390	11048	538E	2B28	13000	32189	32C8	7DBD
125	2290	23136	08F2	5A60	1145	11568	0479	2D30	31373	1601	7A8D	0641
126	31551	12199	7B3F	2FA7	27727	23023	6C4F	59EF	13096	19537	3328	4C51
127	12088	1213	2F38	04BD	6044	19554	179C	4C62	26395	25667	671B	6443
128	7722	936	1E2A	03A8	3861	468	0F15	01D4	15487	4415	3C7F	113F
129	27312	6272	6AB0	1880	13656	3136	3558	0C40	29245	2303	723D	08FF
130	23130	32446	5A5A	7EBE	11565	16223	2D2D	3F5F	26729	16362	6869	3FEA
131	594	13555	0252	34F3	297	21573	0129	5445	12568	28620	3118	6FCC
132	25804	8789	64CC	2255	12902	24342	3266	5F16	24665	6736	6059	1A50
133	31013	24821	7925	60F5	27970	32326	6D42	7E46	8923	2777	22DB	0AD9
134	32585	21068	7F49	524C	28276	10534	6E74	2926	19634	24331	4CB2	5F0B
135	3077	31891	0C05	7C93	22482	28789	57D2	7075	29141	9042	71D5	2352
136	17231	5321	434F	14C9	28791	17496	7077	4458	73	107	0049	006B
137	31554	551	7B42	0227	15777	20271	3DA1	4F2F	26482	4779	6772	12AB
138	8764	12115	223C	2F53	4382	22933	111E	5995	6397	13065	18FD	3309
139	15375	4902	3C0F	1326	20439	2451	4FD7	0993	29818	30421	747A	76D5
140	13428	1991	3474	07C7	6714	19935	1A3A	4DDF	8153	20210	1FD9	4EF2
141	17658	14404	44FA	3844	8829	7202	227D	1C22	302	5651	012E	1613
142	13475	17982	34A3	463E	19329	8991	4B81	231F	28136	31017	6DE8	7929
143	22095	19566	564F	4C6E	31479	9783	7AF7	2637	29125	30719	71C5	77FF
144	24805	2970	60E5	0B9A	24994	1485	61A2	05CD	8625	23104	21B1	5A40
145	4307	23055	10D3	5A0F	22969	25403	59B9	633B	26671	7799	682F	1E77
146	23292	15158	5AFC	3B36	11646	7579	2D7E	1D9B	6424	17865	1918	45C9
147	1377	29094	0561	71A6	21344	14547	5360	38D3	12893	26951	325D	6947
148	28654	653	6FEE	028D	14327	20346	37F7	4F7A	18502	25073	4846	61F1
149	6350	19155	18CE	4AD3	3175	27477	0C67	6B55	7765	32381	1E55	7E7D
150	16770	23588	4182	5C24	8385	11794	20C1	2E12	25483	16581	638B	40C5

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q
151	14726	10878	3986	2A7E	7363	5439	1CC3	153F	15408	32087	3C30	7D57
152	25685	31060	6455	7954	25594	15530	63FA	3CAA	6414	97	190E	0061
153	21356	30875	536C	789B	10678	29297	29B6	7271	8164	7618	1FE4	1DC2
154	12149	11496	2F75	2CE8	18026	5748	466A	1674	10347	93	286B	005D
155	28966	24545	7126	5FE1	14483	25036	3893	61CC	29369	16052	72B9	3EB4
156	22898	9586	5972	2572	11449	4793	2CB9	12B9	10389	14300	2895	37DC
157	1713	20984	06B1	51F8	21128	10492	5288	28FC	24783	11129	60CF	2B79
158	30010	30389	753A	76B5	15005	30054	3A9D	7566	18400	6602	47E0	19CA
159	2365	7298	093D	1C82	21838	3649	554E	0E41	22135	14460	5677	387C
160	27179	18934	6A2B	49F6	25797	9467	64C5	24FB	4625	25458	1211	6372
161	29740	23137	742C	5A61	14870	25356	3A16	630C	22346	15869	574A	3DFD
162	5665	24597	1621	6015	23232	32310	5AC0	7E36	2545	27047	09F1	69A7
163	23671	23301	5C77	5B05	32747	25534	7FEB	63BE	7786	26808	1E6A	68B8
164	1680	7764	0690	1E54	840	3882	0348	0F2A	20209	7354	4EF1	1CBA
165	25861	14518	6505	38B6	25426	7259	6352	1C5B	26414	27834	672E	6CBA
166	25712	21634	6470	5482	12856	10817	3238	2A41	1478	11250	05C6	2BF2
167	19245	11546	4B2D	2D1A	29766	5773	7446	168D	15122	552	3B12	0228
168	26887	26454	6907	6756	25939	13227	6553	33AB	24603	27058	601B	69B2
169	30897	15938	78B1	3E42	28040	7969	6D88	1F21	677	14808	02A5	39D8
170	11496	9050	2CE8	235A	5748	4525	1674	11AD	13705	9642	3589	25AA
171	1278	3103	04FE	0C1F	639	18483	027F	4833	13273	32253	33D9	7DFD
172	31555	758	7B43	02F6	27761	379	6C71	017B	14879	26081	3A1F	65E1
173	29171	16528	71F3	4090	26921	8264	6929	2048	6643	21184	19F3	52C0
174	20472	20375	4FF8	4F97	10236	27127	27FC	69F7	23138	11748	5A62	2DE4
175	5816	10208	16B8	27E0	2908	5104	0B5C	13F0	28838	32676	70A6	7FA4
176	30270	17698	763E	4522	15135	8849	3B1F	2291	9045	2425	2355	0979
177	22188	8405	56AC	20D5	11094	24150	2B56	5E56	10792	19455	2A28	4BFF
178	6182	28634	1826	6FDA	3091	14317	0C13	37ED	25666	19889	6442	4DB1
179	32333	1951	7E4D	079F	28406	19955	6EF6	4DF3	11546	18177	2D1A	4701
180	14046	20344	36DE	4F78	7023	10172	1B6F	27BC	15535	2492	3CAF	09BC
181	15873	26696	3E01	6848	20176	13348	4ED0	3424	16134	15086	3F06	3AEE
182	19843	3355	4D83	0D1B	30481	18609	7711	48B1	8360	30632	20A8	77A8
183	29367	11975	72B7	2EC7	26763	22879	688B	595F	14401	27549	3841	6B9D
184	13352	31942	3428	7CC6	6676	15971	1A14	3E63	26045	6911	65BD	1AFF
185	22977	9737	59C1	2609	32048	23864	7D30	5D38	24070	9937	5E06	26D1
186	31691	9638	7BCB	25A6	27701	4819	6C35	12D3	30300	2467	765C	09A3
187	10637	30643	298D	77B3	17686	30181	4516	75E5	13602	25831	3522	64E7
188	25454	13230	636E	33AE	12727	6615	31B7	19D7	32679	32236	7FA7	7DEC
189	18610	22185	48B2	56A9	9305	25960	2459	6568	16267	12987	3F8B	32BB
190	6368	2055	18E0	0807	3184	19007	0C70	4A3F	9063	11714	2367	2DC2
191	7887	8767	1ECF	223F	24247	24355	5EB7	5F23	19487	19283	4C1F	4B53
192	7730	15852	1E32	3DEC	3865	7926	0F19	1EF6	12778	11542	31EA	2D16
193	23476	16125	5BB4	3EFD	11738	20802	2DDA	5142	27309	27928	6AAD	6D18
194	889	6074	0379	17BA	20588	3037	506C	0BDD	12527	26637	30EF	680D
195	21141	31245	5295	7A0D	30874	29498	789A	733A	953	10035	03B9	2733
196	20520	15880	5028	3E08	10260	7940	2814	1F04	15958	10748	3E56	29FC
197	21669	20371	54A5	4F93	31618	27125	7B82	69F5	6068	24429	17B4	5F6D
198	15967	8666	3E5F	21DA	20223	4333	4EFF	10ED	23577	29701	5C19	7405
199	21639	816	5487	0330	31635	408	7B93	0198	32156	14997	7D9C	3A95
200	31120	22309	7990	5725	15560	26030	3CC8	65AE	32709	32235	7FC5	7DEB

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q
201	3698	29563	0E72	737B	1849	30593	0739	7781	23557	30766	5C05	782E
202	16322	13078	3FC2	3316	8161	6539	1FE1	198B	17638	5985	44E6	1761
203	17429	10460	4415	28DC	29658	5230	73DA	146E	3545	6823	0DD9	1AA7
204	21730	17590	54E2	44B6	10865	8795	2A71	225B	9299	20973	2453	51ED
205	17808	20277	4590	4F35	8904	27046	22C8	69A6	6323	10197	18B3	27D5
206	30068	19988	7574	4E14	15034	9994	3ABA	270A	19590	9618	4C86	2592
207	12737	6781	31C1	1A7D	18736	17154	4930	4302	7075	22705	1BA3	58B1
208	28241	32501	6E51	7EF5	26360	28998	66F8	7146	14993	5234	3A91	1472
209	20371	6024	4F93	1788	30233	3012	7619	0BC4	19916	12541	4DCC	30FD
210	13829	20520	3605	5028	19154	10260	4AD2	2814	6532	8019	1984	1F53
211	13366	31951	3436	7CCF	6683	28763	1A1B	705B	17317	22568	43A5	5828
212	25732	26063	6484	65CF	12866	31963	3242	7CDB	16562	5221	40B2	1465
213	19864	27203	4D98	6A43	9932	31517	26CC	7B1D	26923	25216	692B	6280
214	5187	6614	1443	19D6	23537	3307	5BF1	0CEB	9155	1354	23C3	054A
215	23219	10970	5AB3	2ADA	31881	5485	7C89	156D	20243	29335	4F13	7297
216	28242	5511	6E52	1587	14121	17663	3729	44FF	32391	6682	7E87	1A1A
217	6243	17119	1863	42DF	24033	28499	5DE1	6F53	20190	26128	4EDE	6610
218	445	16064	01BD	3EC0	20750	8032	510E	1F60	27564	29390	6BAC	72CE
219	21346	31614	5362	7B7E	10673	15807	29B1	3DBF	20869	8852	5185	2294
220	13256	4660	33C8	1234	6628	2330	19E4	091A	9791	6110	263F	17DE
221	18472	13881	4828	3639	9236	21792	2414	5520	714	11847	02CA	2E47
222	25945	16819	6559	41B3	25468	28389	637C	6EE5	7498	10239	1D4A	27FF
223	31051	6371	794B	18E3	28021	16973	6D75	424D	23278	6955	5AEE	1B2B
224	1093	24673	0445	6061	21490	32268	53F2	7E0C	8358	10897	20A6	2A91
225	5829	6055	16C5	17A7	23218	17903	5AB2	45EF	9468	14076	24FC	36FC
226	31546	10009	7B3A	2719	15773	23984	3D9D	5DB0	23731	12450	5CB3	30A2
227	29833	5957	7489	1745	27540	17822	6B94	459E	25133	8954	622D	22FA
228	18146	11597	46E2	2D4D	9073	22682	2371	589A	2470	19709	09A6	4CFD
229	24813	22155	60ED	568B	24998	25977	61A6	6579	17501	1252	445D	04E4
230	47	15050	002F	3ACA	20935	7525	51C7	1D65	24671	15142	605F	3B26
231	3202	16450	0C82	4042	1601	8225	0641	2021	11930	26958	2E9A	694E
232	21571	27899	5443	6CFB	31729	30785	7BF1	7841	9154	8759	23C2	2237
233	7469	2016	1D2D	07E0	24390	1008	5F46	03F0	7388	12696	1CDC	3198
234	25297	17153	62D1	4301	24760	28604	60B8	6FBC	3440	11936	0D70	2EA0
235	8175	15849	1FEF	3DE9	24103	20680	5E27	50C8	27666	25635	6C12	6423
236	28519	30581	6F67	7775	26211	30086	6663	7586	22888	17231	5968	434F
237	4991	3600	137F	0E10	22639	1800	586F	0708	13194	22298	338A	571A
238	7907	4097	1EE3	1001	24225	17980	5EA1	463C	26710	7330	6856	1CA2
239	17728	671	4540	029F	8864	20339	22A0	4F73	7266	30758	1C62	7826
240	14415	20774	384F	5126	19959	10387	4DF7	2893	15175	6933	3B47	1B15
241	30976	24471	7900	5F97	15488	25079	3C80	61F7	15891	2810	3E13	0AFA
242	26376	27341	6708	6ACD	13188	31578	3384	7B5A	26692	8820	6844	2274
243	19063	19388	4A77	4BEC	29931	9694	74EB	25DE	14757	7831	39A5	1E97
244	19160	25278	4AD8	62BE	9580	12639	256C	315F	28757	19584	7055	4C80
245	3800	9505	0ED8	2521	1900	23724	076C	5CAC	31342	2944	7A6E	0B80
246	8307	26143	2073	661F	16873	32051	41E9	7D33	19435	19854	4BEB	4D8E
247	12918	13359	3276	342F	6459	21547	193B	542B	2437	10456	0985	28D8
248	19642	2154	4CBA	086A	9821	1077	265D	0435	20573	17036	505D	428C
249	24873	13747	6129	35B3	24900	21733	6144	54E5	18781	2343	495D	0927
250	22071	27646	5637	6BFE	31435	13823	7ACB	35FF	18948	14820	4A04	39E4

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)
251	13904	1056	3650	0420	6952	528	1B28	0210	23393	1756	5B61	06DC
252	27198	1413	6A3E	0585	13599	19710	351F	4CFE	5619	19068	15F3	4A7C
253	3685	3311	0E65	0CEF	22242	18507	56E2	484B	17052	28716	429C	702C
254	16820	4951	41B4	1357	8410	18327	20DA	4797	21292	31958	532C	7CD6
255	22479	749	57CF	02ED	31287	20298	7A37	4F4A	2868	16097	0B34	3EE1
256	6850	6307	1AC2	18A3	3425	17005	0D61	426D	19538	1308	4C52	051C
257	15434	961	3C4A	03C1	7717	20444	1E25	4FDC	24294	3320	5EE6	0CF8
258	19332	2358	4B84	0936	9666	1179	25C2	049B	22895	16682	596F	412A
259	8518	28350	2146	6EBE	4259	14175	10A3	375F	27652	6388	6C04	18F4
260	14698	31198	396A	79DE	7349	15599	1CB5	3CEF	29905	12828	74D1	321C
261	21476	11467	53E4	2CCB	10738	22617	29F2	5859	21415	3518	53A7	0DBE
262	30475	8862	770B	229E	27221	4431	6A55	114F	1210	3494	04BA	0DA6
263	23984	6327	5DB0	18B7	11992	16999	2ED8	4267	22396	6458	577C	193A
264	1912	7443	0778	1D13	956	16565	03BC	40B5	26552	10717	67B8	29DD
265	26735	28574	686F	6F9E	26087	14287	65E7	37CF	24829	8463	60FD	210F
266	15705	25093	3D59	6205	20348	32574	4F7C	7F3E	8663	27337	21D7	6AC9
267	3881	6139	0F29	17FB	22084	17857	5644	45C1	991	19846	03DF	4D86
268	20434	22047	4FD2	561F	10217	25907	27E9	6533	21926	9388	55A6	24AC
269	16779	32545	418B	7F21	28949	29100	7115	71AC	23306	21201	5B0A	52D1
270	31413	7112	7AB5	1BC8	27786	3556	6C8A	0DE4	13646	31422	354E	7ABE
271	16860	28535	41DC	6F77	8430	31111	20EE	7987	148	166	0094	00A6
272	8322	10378	2082	288A	4161	5189	1041	1445	24836	28622	6104	6FCE
273	28530	15065	6F72	3AD9	14265	21328	37B9	5350	24202	6477	5E8A	194D
274	26934	5125	6936	1405	13467	17470	349B	443E	9820	10704	265C	29D0
275	18806	12528	4976	30F0	9403	6264	24BB	1878	12939	25843	328B	64F3
276	20216	23215	4EF8	5AAF	10108	25451	277C	636B	2364	25406	093C	633E
277	9245	20959	241D	51DF	17374	26323	43DE	66D3	14820	21523	39E4	5413
278	8271	3568	204F	0DF0	16887	1784	41F7	06F8	2011	8569	07DB	2179
279	18684	26453	48FC	6755	9342	32150	247E	7D96	13549	9590	34ED	2576
280	8220	29421	201C	72ED	4110	30538	100E	774A	28339	22466	6EB3	57C2
281	6837	24555	1AB5	5FEB	23690	25033	5C8A	61C9	25759	12455	649F	30A7
282	9613	10779	258D	2A1B	17174	23345	4316	5B31	11116	27506	2B6C	6B72
283	31632	25260	7B90	62AC	15816	12630	3DC8	3156	31448	21847	7AD8	5557
284	27448	16084	6B38	3ED4	13724	8042	359C	1F6A	27936	28392	6D20	6EE8
285	12417	26028	3081	65AC	18832	13014	4990	32D6	3578	1969	0DFA	07B1
286	30901	29852	78B5	749C	28042	14926	6D8A	3A4E	12371	30715	3053	77FB
287	9366	14978	2496	3A82	4683	7489	124B	1D41	12721	23674	31B1	5C7A
288	12225	12182	2FC1	2F96	17968	6091	4630	17CB	10264	22629	2818	5865
289	21458	25143	53D2	6237	10729	32551	29E9	7F27	25344	12857	6300	3239
290	6466	15838	1942	3DDE	3233	7919	0CA1	1EEF	13246	30182	33BE	75E6
291	8999	5336	2327	14D8	16451	2668	4043	0A6C	544	21880	0220	5578
292	26718	21885	685E	557D	13359	25730	342F	6482	9914	6617	26BA	19D9
293	3230	20561	0C9E	5051	1615	26132	064F	6614	4601	27707	11F9	6C3B
294	27961	30097	6D39	7591	26444	29940	674C	74F4	16234	16249	3F6A	3F79
295	28465	21877	6F31	5575	26184	25734	6648	6486	24475	24754	5F9B	60B2
296	6791	23589	1A87	5C25	23699	24622	5C93	602E	26318	31609	66CE	7B79
297	17338	26060	43BA	65CC	8669	13030	21DD	32E6	6224	22689	1850	58A1
298	11832	9964	2E38	26EC	5916	4982	171C	1376	13381	3226	3445	0C9A
299	11407	25959	2C8F	6567	18327	31887	4797	7C8F	30013	4167	753D	1047
300	15553	3294	3CC1	0CDE	20400	1647	4FB0	066F	22195	25624	56B3	6418

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)
301	17418	30173	440A	75DD	8709	29906	2205	74D2	30380	10924	76AC	2AAC
302	14952	15515	3A68	3C9B	7476	20593	1D34	5071	15337	23096	3BE9	5A38
303	52	5371	0034	14FB	26	17473	001A	4441	10716	22683	29DC	589B
304	27254	10242	6A76	2802	13627	5121	353B	1401	13592	10955	3518	2ACB
305	15064	28052	3AD8	6D9A	7532	14026	1D6C	36CA	2412	17117	096C	42DD
306	10942	14714	2ABE	397A	5471	7357	155F	1CBD	15453	15837	3C5D	3DD
307	377	19550	0179	4C5E	20844	9775	516C	262F	13810	22647	35F2	5877
308	14303	8866	37DF	22A2	19007	4433	4A3F	1151	12956	10700	329C	29CC
309	24427	15297	5F6B	3BC1	32357	21468	7E65	53DC	30538	30293	774A	7655
310	26629	10898	6805	2A92	26066	5449	65D2	1549	10814	5579	2A3E	15CB
311	20011	31315	4E2B	7A53	30405	29461	76C5	7315	18939	11057	49FB	2B31
312	16086	19475	3ED6	4C13	8043	26677	1F6B	6835	19767	30238	4D37	761E
313	24374	1278	5F36	04FE	12187	639	2F9B	027F	20547	14000	5043	36B0
314	9969	11431	26F1	2CA7	17064	22639	42A8	586F	29720	22860	7418	594C
315	29364	31392	72B4	7AA0	14682	15696	395A	3D50	31831	27172	7C57	6A24
316	25560	4381	63D8	111D	12780	18098	31EC	46B2	26287	307	66AF	0133
317	28281	14898	6E79	3A32	26348	7449	66EC	1D19	11310	20380	2C2E	4F9C
318	7327	23959	1C9F	5D97	24479	24823	5F9F	60F7	25724	26427	647C	673B
319	32449	16091	7EC1	3EDB	28336	20817	6EB0	5151	21423	10702	53AF	29CE
320	26334	9037	66DE	234D	13167	24474	336F	5F9A	5190	30024	1446	7548
321	14760	24162	39A8	5E62	7380	12081	1CD4	2F31	258	14018	0102	36C2
322	15128	6383	3B18	18EF	7564	16971	1D8C	424B	13978	4297	369A	10C9
323	29912	27183	74D8	6A2F	14956	31531	3A6C	7B2B	4670	13938	123E	3672
324	4244	16872	1094	41E8	2122	8436	084A	20F4	23496	25288	5BC8	62C8
325	8499	9072	2133	2370	16713	4536	4149	11B8	23986	27294	5DB2	6A9E
326	9362	12966	2492	32A6	4681	6483	1249	1953	839	31835	0347	7C5B
327	10175	28886	27BF	70D6	16911	14443	420F	386B	11296	8228	2C20	2024
328	30957	25118	78ED	621E	28070	12559	6DA6	310F	30913	12745	78C1	31C9
329	12755	20424	31D3	4FC8	18745	10212	4939	27E4	27297	6746	6AA1	1A5A
330	19350	6729	4B96	1A49	9675	17176	25CB	4318	10349	1456	286D	05B0
331	1153	20983	0481	51F7	21392	26311	5390	66C7	32504	27743	7EF8	6C5F
332	29304	12372	7278	3054	14652	6186	393C	182A	18405	27443	47E5	6B33
333	6041	13948	1799	367C	23068	6974	5A1C	1B3E	3526	31045	0DC6	7945
334	21668	27547	54A4	6B9B	10834	31729	2A52	7BF1	19161	12225	4AD9	2FC1
335	28048	8152	6D90	1FD8	14024	4076	36C8	0FEC	23831	21482	5D17	53EA
336	10096	17354	2770	43CA	5048	8677	13B8	21E5	21380	14678	5384	3956
337	23388	17835	5B5C	45AB	11694	27881	2DAE	6CE9	4282	30656	10BA	77C0
338	15542	14378	3CB6	382A	7771	7189	1E5B	1C15	32382	13721	7E7E	3599
339	24013	7453	5DCD	1D1D	32566	16562	7F36	40B2	806	21831	0326	5547
340	2684	26317	0A7C	66CD	1342	32090	053E	7D5A	6238	30208	185E	7600
341	19018	5955	4A4A	1743	9509	17821	2525	459D	10488	9995	28F8	270B
342	25501	10346	639D	286A	24606	5173	601E	1435	19507	3248	4C33	0CB0
343	4489	13200	1189	3390	22804	6600	5914	19C8	27288	12030	6A98	2EFE
344	31011	30402	7923	76C2	27969	15201	6D41	3B61	2390	5688	0956	1638
345	29448	7311	7308	1C8F	14724	16507	3984	407B	19094	2082	4A96	0822
346	25461	3082	6375	0C0A	24682	1541	606A	0605	13860	23143	3624	5A67
347	11846	21398	2E46	5396	5923	10699	1723	29CB	9225	25906	2409	6532
348	30331	31104	767B	7980	27373	15552	6AED	3CC0	2505	15902	09C9	3E1E
349	10588	24272	295C	5ED0	5294	12136	14AE	2F68	27806	21084	6C9E	525C
350	32154	27123	7D9A	69F3	16077	31429	3ECD	7AC5	2408	25723	0968	647B

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q	I (Dec.)	Q	I (Hex.)	Q
351	29572	5578	7384	15CA	14786	2789	39C2	0AE5	13347	13427	3423	3473
352	13173	25731	3375	6483	18538	31869	486A	7C7D	7885	31084	1ECD	796C
353	10735	10662	29EF	29A6	17703	5331	4527	14D3	6669	24023	1A0D	5DD7
354	224	11084	00E0	2B4C	112	5542	0070	15A6	8187	23931	1FFB	5D7B
355	12083	31098	2F33	797A	17993	15549	4649	3CBD	18145	15836	46E1	3DDC
356	22822	16408	5926	4018	11411	8204	2C93	200C	14109	6085	371D	17C5
357	2934	6362	0B76	18DA	1467	3181	05BB	0C6D	14231	30324	3797	7674
358	27692	2719	6C2C	0A9F	13846	19315	3616	4B73	27606	27561	6BD6	6BA9
359	10205	14732	27DD	398C	16958	7366	423E	1CC6	783	13821	030F	35FD
360	7011	22744	1B63	58D8	23649	11372	5C61	2C6C	6301	269	189D	010D
361	22098	1476	5652	05C4	11049	738	2B29	02E2	5067	28663	13CB	6FF7
362	2640	8445	0A50	20FD	1320	24130	0528	5E42	15383	29619	3C17	73B3
363	4408	21118	1138	527E	2204	10559	089C	293F	1392	2043	0570	07FB
364	102	22198	0066	56B6	51	11099	0033	2B5B	7641	6962	1DD9	1B32
365	27632	22030	6BF0	560E	13816	11015	35F8	2B07	25700	29119	6464	71BF
366	19646	10363	4CBE	287B	9823	23041	265F	5A01	25259	22947	62AB	59A3
367	26967	25802	6957	64CA	25979	12901	657B	3265	19813	9612	4D65	258C
368	32008	2496	7D08	09C0	16004	1248	3E84	04E0	20933	18698	51C5	490A
369	7873	31288	1EC1	7A38	24240	15644	5EB0	3D1C	638	16782	027E	418E
370	655	24248	028F	5EB8	20631	12124	5097	2F5C	16318	29735	3FBE	7427
371	25274	14327	62BA	37F7	12637	21959	315D	55C7	6878	2136	1ADE	0858
372	16210	23154	3F52	5A72	8105	11577	1FA9	2D39	1328	8086	0530	1F96
373	11631	13394	2D6F	3452	18279	6697	4767	1A29	14744	10553	3998	2939
374	8535	1806	2157	070E	16763	903	417B	0387	22800	11900	5910	2E7C
375	19293	17179	4B5D	431B	29822	28593	747E	6FB1	25919	19996	653F	4E1C
376	12110	10856	2F4E	2A68	6055	5428	17A7	1534	4795	5641	12BB	1609
377	21538	25755	5422	649B	10769	31857	2A11	7C71	18683	28328	48FB	6EA8
378	10579	15674	2953	3D3A	17785	7837	4579	1E9D	32658	25617	7F92	6411
379	13032	7083	32E8	1BAB	6516	17385	1974	43E9	1586	26986	0632	696A
380	14717	29096	397D	71A8	19822	14548	4D6E	38D4	27208	5597	6A48	15DD
381	11666	3038	2D92	0BDE	5833	1519	16C9	05EF	17517	14078	446D	36FE
382	25809	16277	64D1	3F95	25528	20982	63B8	51F6	599	13247	0257	33BF
383	5008	25525	1390	63B5	2504	32742	09C8	7FE6	16253	499	3F7D	01F3
384	32418	20465	7EA2	4FF1	16209	27076	3F51	69C4	8685	30469	21ED	7705
385	22175	28855	569F	70B7	31391	30311	7A9F	7667	29972	17544	7514	4488
386	11742	32732	2DDE	7FDC	5871	16366	16EF	3FEE	22128	28510	5670	6F5E
387	22546	20373	5812	4F95	11273	27126	2C09	69F6	19871	23196	4D9F	5A9C
388	21413	9469	53A5	24FD	30722	23618	7802	5C42	19405	13384	4BCD	3448
389	133	26155	0085	662B	20882	32041	5192	7D29	17972	4239	4634	108F
390	4915	6957	1333	1B2D	22601	17322	5849	43AA	8599	20725	2197	50F5
391	8736	12214	2220	2FB6	4368	6107	1110	17DB	10142	6466	279E	1942
392	1397	21479	0575	53E7	21354	26575	536A	67CF	26834	28465	68D2	6F31
393	18024	31914	4668	7CAA	9012	15957	2334	3E55	23710	19981	5C9E	4E0D
394	15532	32311	3CAC	7E37	7766	28967	1E56	7127	27280	16723	6A90	4153
395	26870	11276	68F6	2C0C	13435	5638	347B	1606	6570	4522	19AA	11AA
396	5904	20626	1710	5092	2952	10313	0B88	2849	7400	678	1CE8	02A6
397	24341	423	5F15	01A7	32346	20207	7E5A	4EEF	26374	15320	6706	3BD8
398	13041	2679	32F1	0A77	18600	19207	48A8	4B07	22218	29116	56CA	71BC
399	23478	15537	5BB6	3CB1	11739	20580	2DDB	5064	29654	5388	73D6	150C
400	1862	10818	0746	2A42	931	5409	03A3	1521	13043	22845	32F3	593D

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)
401	5850	23074	16DA	5A22	2925	11537	0B6D	2D11	24457	28430	5F89	6F0E
402	5552	20250	15B0	4F1A	2776	10125	0AD8	278D	17161	8660	4309	21D4
403	12589	14629	312D	3925	18758	21166	4946	52AE	21314	2659	5342	0A63
404	23008	29175	59E0	71F7	11504	30407	2CF0	76C7	28728	8803	7038	2263
405	27636	13943	6BF4	3677	13818	21767	35FA	5507	22162	19690	5692	4CEA
406	17600	11072	44C0	2B40	8800	5536	2260	15A0	26259	22169	6693	5699
407	17000	29492	4268	7334	8500	14746	2134	399A	22180	8511	56A4	213F
408	21913	5719	5599	1657	31516	17687	7B1C	4517	2266	17393	08DA	43F1
409	30320	7347	7670	1CB3	15160	16485	3B38	4065	10291	11336	2833	2C48
410	28240	12156	6E50	2F7C	14120	6078	3728	17BE	26620	13576	67FC	3508
411	7260	25623	1C5C	6417	3630	31799	0E2E	7C37	19650	22820	4CC2	5924
412	17906	27725	45F2	6C4D	8953	30746	22F9	781A	14236	13344	379C	3420
413	5882	28870	16FA	70C6	2941	14435	0B7D	3863	11482	20107	2CDA	4E8B
414	22080	31478	5640	7AF6	11040	15739	2B20	3D7B	25289	8013	62C9	1F4D
415	12183	28530	2F97	6F72	17947	14265	461B	37B9	12011	18835	2EEB	4993
416	23082	24834	5A2A	6102	11541	12417	2D15	3081	13892	16793	3644	4199
417	17435	9075	441B	2373	29661	24453	73DD	5F85	17336	9818	43B8	265A
418	18527	32265	485F	7E09	30207	28984	75FF	7138	10759	4673	2A07	1241
419	31902	3175	7C9E	0C67	15951	18447	3E4F	480F	26816	13609	68C0	3529
420	18783	17434	495F	441A	30079	8717	757F	220D	31065	10054	7959	2746
421	20027	12178	4E3B	2F92	30413	6089	76CD	17C9	8578	10988	2182	2AEC
422	7982	25613	1F2E	640D	3991	31802	0F97	7C3A	24023	14744	5DD7	3998
423	20587	31692	506B	7BCC	31205	15846	79E5	3DE6	16199	17930	3F47	460A
424	10004	25384	2714	6328	5002	12692	138A	3194	22310	25452	5726	636C
425	13459	18908	3493	49DC	19353	9454	4B99	24EE	30402	11334	76C2	2C46
426	13383	25816	3447	64D8	19443	12908	4BF3	326C	16613	15451	40E5	3C5B
427	28930	4661	7102	1235	14465	18214	3881	4726	13084	11362	331C	2C62
428	4860	31115	12FC	798B	2430	29433	097E	72F9	3437	2993	0D6D	0BB1
429	13108	7691	3334	1E0B	6554	16697	199A	4139	1703	11012	06A7	2B04
430	24161	1311	5E61	051F	32480	19635	7EE0	4CB3	22659	5806	5883	16AE
431	20067	16471	4E63	4057	30433	28183	76E1	6E17	26896	20180	6910	4ED4
432	2667	15771	0A6B	3D9B	21733	20721	54E5	50F1	1735	8932	06C7	22E4
433	13372	16112	343C	3EF0	6686	8056	1A1E	1F78	16178	23878	3F32	5D46
434	28743	21062	7047	5246	27123	10531	69F3	2923	19166	20760	4ADE	5118
435	24489	29690	5FA9	73FA	32260	14845	7E04	39FD	665	32764	0299	7FFC
436	249	10141	00F9	279D	20908	24050	51AC	5DF2	20227	32325	4F03	7E45
437	19960	19014	4DF8	4A46	9980	9507	26FC	2523	24447	25993	5F7F	6589
438	29682	22141	73F2	567D	14841	25858	39F9	6502	16771	3268	4183	0CC4
439	31101	11852	797D	2E4C	28014	5926	6D6E	1726	27209	25180	6A49	625C
440	27148	26404	6A0C	6724	13574	13202	3506	3392	6050	12149	17A2	2F75
441	26706	30663	6852	77C7	13353	30175	3429	75DF	29088	10193	71A0	27D1
442	5148	32524	141C	7F0C	2574	16262	0A0E	3F86	7601	9128	1DB1	23A8
443	4216	28644	1078	6FE4	2108	14322	083C	37F2	4905	7843	1329	1EA3
444	5762	10228	1682	27F4	2881	5114	0B41	13FA	5915	25474	171B	6382
445	245	23536	00F5	5BF0	20906	11768	51AA	2DF8	6169	11356	1819	235C
446	21882	18045	557A	467D	10941	27906	2ABD	6D02	21303	11226	5337	2BDA
447	3763	25441	0EB3	6361	22153	32652	5689	7F8C	28096	16268	6DC0	3F8C
448	206	27066	00CE	69BA	103	13533	0067	34DD	8905	14491	22C9	389B
449	28798	13740	707E	35AC	14399	6870	383F	1AD6	26997	8366	6975	20AE
450	32402	13815	7E92	35F7	16201	21703	3F49	54C7	15047	26009	3AC7	6599

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay				13-Chip Delay				0-Chip Delay			
	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)	I (Dec.)	Q (Dec.)	I (Hex.)	Q (Hex.)
451	13463	3684	3497	0E64	19355	1842	4B9B	0732	17460	5164	4434	142C
452	15417	23715	3C39	5CA3	20428	24685	4FCC	606D	17629	17126	44DD	42E6
453	23101	15314	5A3D	3BD2	31950	7657	7CCE	1DE9	10461	21566	28DD	543E
454	14957	32469	3A6D	7ED5	19686	29014	4CE6	7156	21618	21845	5472	5555
455	23429	9816	5B85	2658	31762	4908	7C12	132C	11498	28149	2CEA	6DF5
456	12990	4444	32BE	115C	6495	2222	195F	08AE	193	9400	00C1	24B8
457	12421	5664	3085	1620	18834	2832	4992	0B10	16140	19459	3F0C	4C03
458	28875	7358	70CB	1CBE	27061	3679	69B5	0E5F	13419	7190	346B	1C16
459	4009	27264	0FA9	6A80	22020	13632	5604	3540	10864	3101	2A70	0C1D
460	1872	28128	0750	6DE0	936	14064	03A8	36F0	28935	491	7107	01EB
461	15203	30168	3B63	75D8	19553	15084	4C61	3AEC	18765	25497	494D	6399
462	30109	29971	759D	7513	27422	29877	6B1E	74B5	27644	29807	6BFC	746F
463	24001	3409	5DC1	0D51	32560	18580	7F30	4894	21564	26508	543C	678C
464	4862	16910	12FE	420E	2431	8455	097F	2107	5142	4442	1416	115A
465	14091	20739	370B	5103	19029	26301	4A55	66BD	1211	4871	04BB	1307
466	6702	10191	1A2E	27CF	3351	24027	0D17	5DDB	1203	31141	04B3	79A5
467	3067	12819	0BFB	3213	21549	22325	542D	5735	5199	9864	144F	2688
468	28643	19295	6FE3	4B5F	26145	27539	6621	6B93	16945	12589	4231	312D
469	21379	10072	5383	2758	30737	5036	7811	13AC	4883	5417	1313	1529
470	20276	15191	4F34	3B57	10138	21399	279A	5397	25040	8549	61D0	2165
471	25337	27748	62F9	6C64	24748	13874	60AC	3632	7119	14288	1BCF	37D0
472	19683	720	4CE3	02D0	30625	360	77A1	0168	17826	8503	45A2	2137
473	10147	29799	27A3	7467	16897	29711	4201	740F	4931	20357	1343	4F85
474	16791	27640	4197	6BF8	28955	13820	711B	35FC	25705	15381	6469	3C15
475	17359	263	43CF	0107	28727	20159	7037	4EBF	10726	18065	29E6	4691
476	13248	24734	33C0	609E	6624	12367	19E0	304F	17363	24678	43D3	6066
477	22740	16615	58D4	40E7	11370	28239	2C6A	6E4F	2746	23858	0ABA	5D32
478	13095	20378	3327	4F9A	18499	10189	4843	27CD	10952	7610	2AC8	1DBA
479	10345	25116	2869	621C	17892	12558	45E4	310E	19313	18097	4B71	46B1
480	30342	19669	7686	4CD5	15171	26710	3B43	6856	29756	20918	743C	51B6
481	27866	14656	6CDA	3940	13933	7328	366D	1CA0	14297	7238	37D9	1C46
482	9559	27151	2557	6A0F	17275	31547	437B	7B3B	21290	30549	532A	7755
483	8808	28728	2268	7038	4404	14364	1134	381C	1909	16320	0775	3FC0
484	12744	25092	31C8	6204	6372	12546	18E4	3102	8994	20853	2322	5175
485	11618	22601	2D62	5849	5809	25112	16B1	6218	13295	26736	33EF	6870
486	27162	2471	6A1A	09A7	13581	19183	350D	4AEF	21590	10327	5456	2857
487	17899	25309	45EB	62DD	29477	32594	7325	7F52	26468	24404	6764	5F54
488	29745	15358	7431	3BFE	27592	7679	6BC8	1DFE	13636	7931	3544	1EFB
489	31892	17739	7C94	454B	15946	27801	3E4A	6C99	5207	5310	1457	14BE
490	23964	12643	5D9C	3163	11982	22157	2ECE	568D	29493	554	7335	022A
491	23562	32730	5C0A	7FDA	11781	16365	2E05	3FED	18992	27311	4A30	6AAF
492	2964	19122	0B94	4AB2	1482	9561	05CA	2559	12567	6865	3117	1AD1
493	18208	16870	4720	41E6	9104	8435	2390	20F3	12075	7762	2F2B	1E52
494	15028	10787	3AB4	2A23	7514	23341	1D5A	5B2D	26658	15761	6822	3D91
495	21901	18400	558D	47E0	31510	9200	7B16	23F0	21077	12697	5255	3199
496	24566	20295	5FF6	4F47	12283	27039	2FFB	699F	15595	24850	3CEB	6112
497	18994	1937	4A32	0791	9497	19956	2519	4DF4	4921	15259	1339	3B9B
498	13608	17963	3528	462B	6804	27945	1A94	6D29	14051	24243	36E3	5EB3
499	27492	7438	6B64	1D0E	13746	3719	35B2	0E87	5956	30508	1744	772C
500	11706	12938	2DBA	328A	5853	6469	16DD	1945	21202	13982	52D2	369E

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Appendix E: PN Offset Programming Information – continued

Table E-1: PnMaskI and PnMaskQ Values for PilotPn

Pilot PN	14-Chip Delay		13-Chip Delay				0-Chip Delay					
	I (Dec.)	Q	I	Q	I	Q	I	Q	I	Q		
			(Hex.)		(Dec.)		(Hex.)	(Dec.)		(Hex.)		
501	14301	19272	37DD	4B48	19006	9636	4A3E	25A4	11239	25039	2BE7	61CF
502	23380	29989	5B54	7525	11690	29870	2DAA	74AE	30038	24086	7556	5E16
503	11338	8526	2C4A	214E	5669	4263	1625	10A7	30222	21581	760E	544D
504	2995	18139	0BB3	46DB	21513	27985	5409	6D51	13476	21346	34A4	5362
505	23390	3247	5B5E	0CAF	11695	18539	2DAF	486B	2497	28187	09C1	6E1B
506	14473	28919	3889	70F7	19860	30279	4D94	7647	31842	23231	7C62	5ABF
507	6530	7292	1982	1C7C	3265	3646	0CC1	0E3E	24342	18743	5F16	4937
508	20452	20740	4FE4	5104	10226	10370	27F2	2882	25857	11594	6501	2D4A
509	12226	27994	2FC2	6D5A	6113	13997	17E1	36AD	27662	7198	6C0E	1C1E
510	1058	2224	0422	08B0	529	1112	0211	0458	24594	105	6012	0069
511	12026	6827	2EFA	1AAB	6013	17257	177D	4369	16790	4534	4196	11B6

E

Appendix F: Test Equipment Preparation

Appendix Content

Test Equipment Preparation	
Purpose	F-1
HP8921A Test Equipment Connections	F-1
HP8921A System Connectivity Test	F-5
Setting HP8921A and HP83236A/B GPIB Address	F-6
Pretest Setup for HP8921A	F-6
Pretest Setup for HP8935	F-6
Advantest R3465 Connection	F-7
R3465 GPIB Address & Clock setup	F-9
Pretest Setup for Advantest R3465	F-9
Agilent E4406A/E4432B Test Equipment Interconnection	F-10
Manual Cable Calibration	
Calibrating Test Cable Setup using HP PCS Interface (HP83236)	F-11
Calibrating Test Cable Setup using Advantest R3465	F-15
Calibrating HP 437 Power Meter	F-18



Test Equipment Preparation

Purpose

This appendix provides information on setting up the HP8921 with PCS interface, the HP8935 and the Advantest R3465. The Cybertest test set doesn't require any setup.

HP8921A Test Equipment Connections

Table F-1 depicts the rear panels of the HP 8921A test equipment as configured to perform automatic tests. All test equipment is controlled by the LMF via an IEEE-488/GPIB bus. The LMF expects each piece of test equipment to have a factory-set GPIB address (refer to Table F-4). If there is a communications problem between the LMF and any piece of test equipment, you should verify that the GPIB addresses have been set correctly and that the GPIB cables are firmly connected to the test equipment.

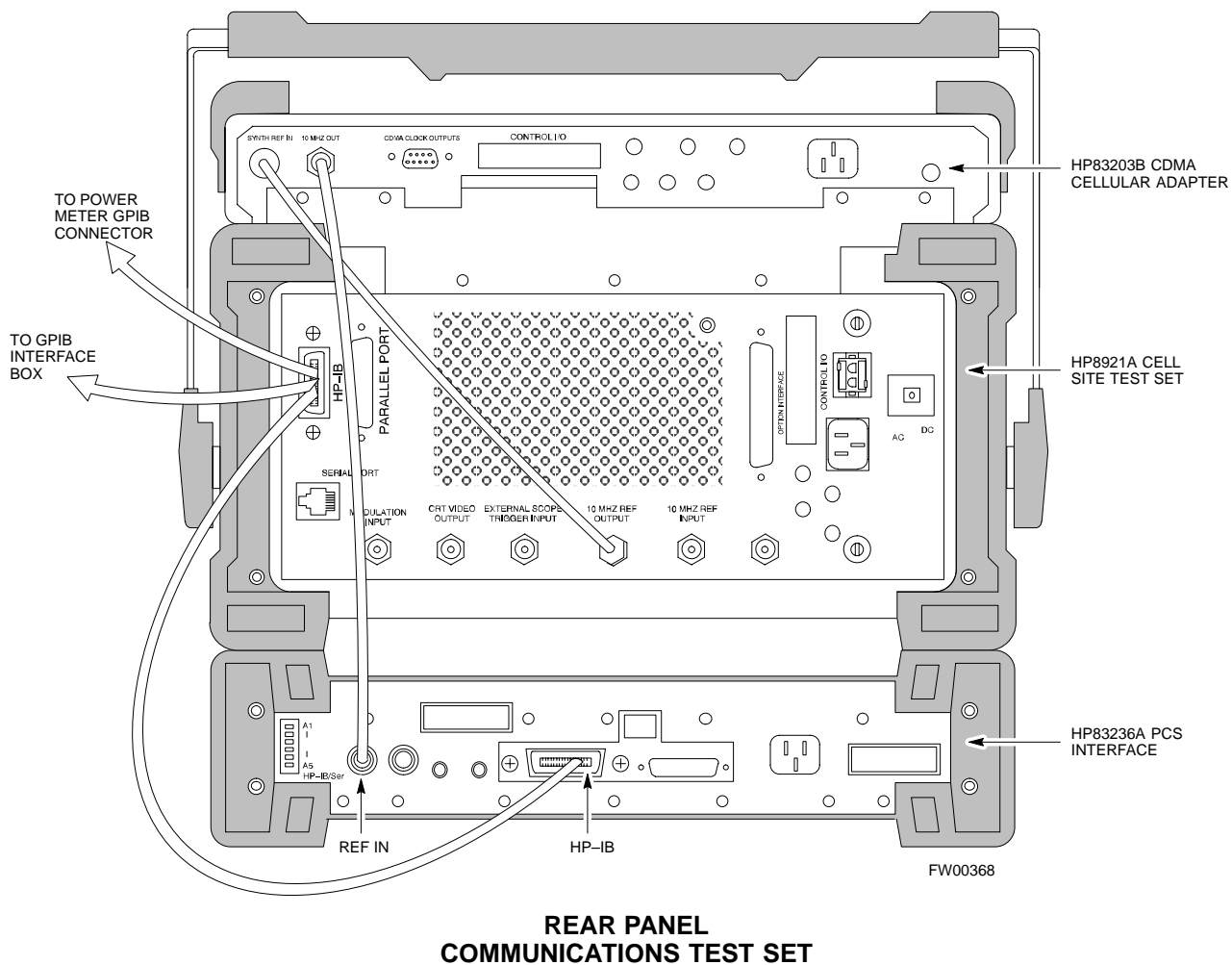
Figure F-1 shows the connections when **not using** an external 10 MHz Rubidium reference.

Table F-1: HP8921A/600 Communications Test Set Rear Panel Connections Without Rubidium

From Test Set:	To Interface:		Connector Type
	8921A	83203B CDMA	
CW RF OUT	CW RF IN		SMC-female – SMC-female
114.3 MHZ IF OUT	114.3 MHZ IF IN		SMC-female – SMC-female
IQ RF IN	IQ RF OUT		SMC-female – SMC-female
DET OUT	AUX DSP IN		SMC-female – SMC-female
CONTROL I/O	CONTROL I/O		45-pin custom BUS
10 MHZ OUT	SYNTH REF IN		BNC-male – BNC-male
HPIB INTERFACE		HPIB INTERFACE	HPIB cable
	10 MHZ OUT	REF IN	BNC-male – BNC-male

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Figure F-1: HP8921A/600 Cables Connection for 10 MHz Signal and GPIB without Rubidium



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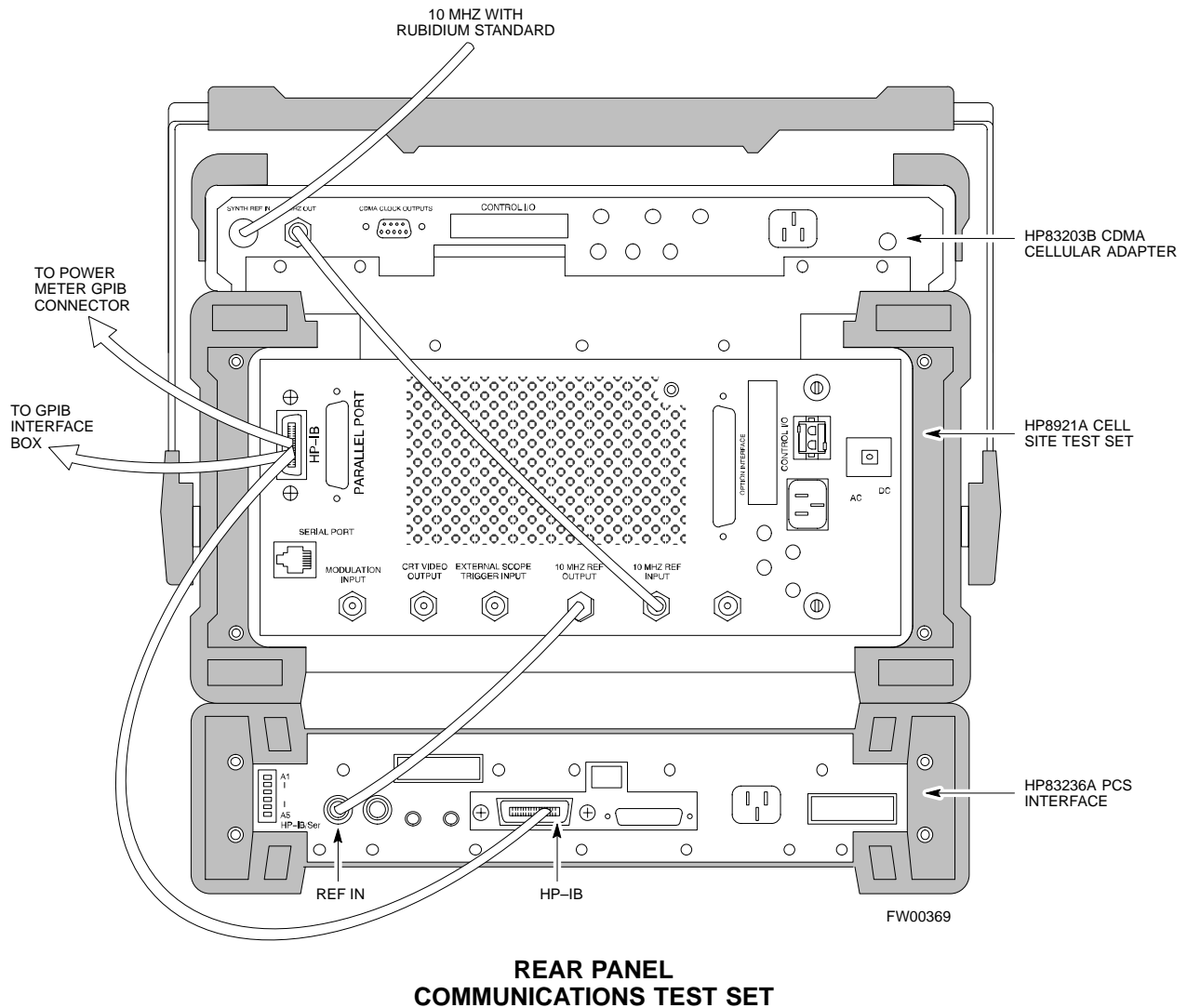
Test Equipment Preparation – continued

Figure F-2 shows the connections **when using** an external 10 MHz Rubidium reference.

Table F-2: HP8921A/600 Communications Test Set Rear Panel Connections With Rubidium			
From Test Set:	To Interface:		Connector Type
8921A	83203B CDMA	83236A PCS	
CW RF OUT	CW RF IN		SMC–female – SMC–female
114.3 MHZ IF OUT	114.3 MHZ IF IN		SMC–female – SMC–female
IQ RF IN	IQ RF OUT		SMC–female – SMC–female
DET OUT	AUX DSP IN		SMC–female – SMC–female
CONTROL I/O	CONTROL I/O		45–pin custom BUS
10 MHZ OUT		REF IN	BNC–male – BNC–male
HPIB INTERFACE		HPIB INTERFACE	HPIB cable
10 MHZ INPUT	10 MHZ OUT		BNC–male – BNC–male

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■

Figure F-2: HP8921A Cables Connection for 10 MHz Signal and GPIB with Rubidium



F

Test Equipment Preparation – continued

HP8921A System Connectivity Test

Follow the steps in Table F-3 to verify that the connections between the PCS Interface and the HP8921A are correct and cables are intact. The software also performs basic functionality checks of each instrument.



IMPORTANT

Disconnect other GPIB devices, especially system controllers, from the system before running the connectivity software.

Table F-3: System Connectivity

Step	Action
	* IMPORTANT – Perform this procedure <i>after</i> test equipment has been allowed to warm-up and stabilize for a <i>minimum of 60 minutes</i> .
1	Insert HP 83236A Manual Control/System card into memory card slot.
2	Press the [PRESET] pushbutton.
3	Press the Screen Control [TESTS] pushbutton to display the “Tests” Main Menu screen.
4	Position the cursor at Select Procedure Location and select it by pressing the cursor control knob. In the Choices selection box, select Card .
5	Position the cursor at Select Procedure Filename and select it by pressing the cursor control knob. In the Choices selection box, select SYS_CONN .
6	Position the cursor at RUN TEST and select it. The software will prompt you through the connectivity setup.
7	Do the following when the test is complete, <ul style="list-style-type: none">• position cursor on STOP TEST and select it• OR press the [K5] pushbutton.
8	To return to the main menu, press the [K5] pushbutton.
9	Press the [PRESET] pushbutton.

Test Equipment Preparation – continued

Setting HP8921A and HP83236A/B GPIB Address

Follow the steps in Table F-4 to set the HP8921A GPIB address.

Table F-4: Setting HP8921A GPIB Address	
Step	Action
1	If you have not already done so, turn the HP8921A power on.
2	Verify that the GPIB addresses are set correctly. <ul style="list-style-type: none">• HP8921A HP-IB Adrs = 18, accessed by pushing LOCAL and selecting More and I/O Configure on the HP8921A/600. (Consult test equipment OEM documentation for additional info as required).• HP83236A (or B) PCS Interface GPIB address=19. Set dip switches as follows:<ul style="list-style-type: none">– A1=1, A2=1, A3=0, A4=0, A5=1, HP-IB/Ser = 1

Pretest Setup for HP8921A

Before the HP8921A CDMA analyzer is used for LMF controlled testing it must be set up correctly for automatic testing.

Table F-5: Pretest Setup for HP8921A	
Step	Action
1	Unplug the memory card if it is plugged in.
2	Press the CURSOR CONTROL knob.
3	Position the cursor at IO CONFIG (under To Screen and More) and select it.
4	Select Mode and set for Talk&Lstn .

Pretest Setup for HP8935

Before the HP8935 CDMA analyzer is used for LMF controlled testing it must be set up correctly for automatic testing.

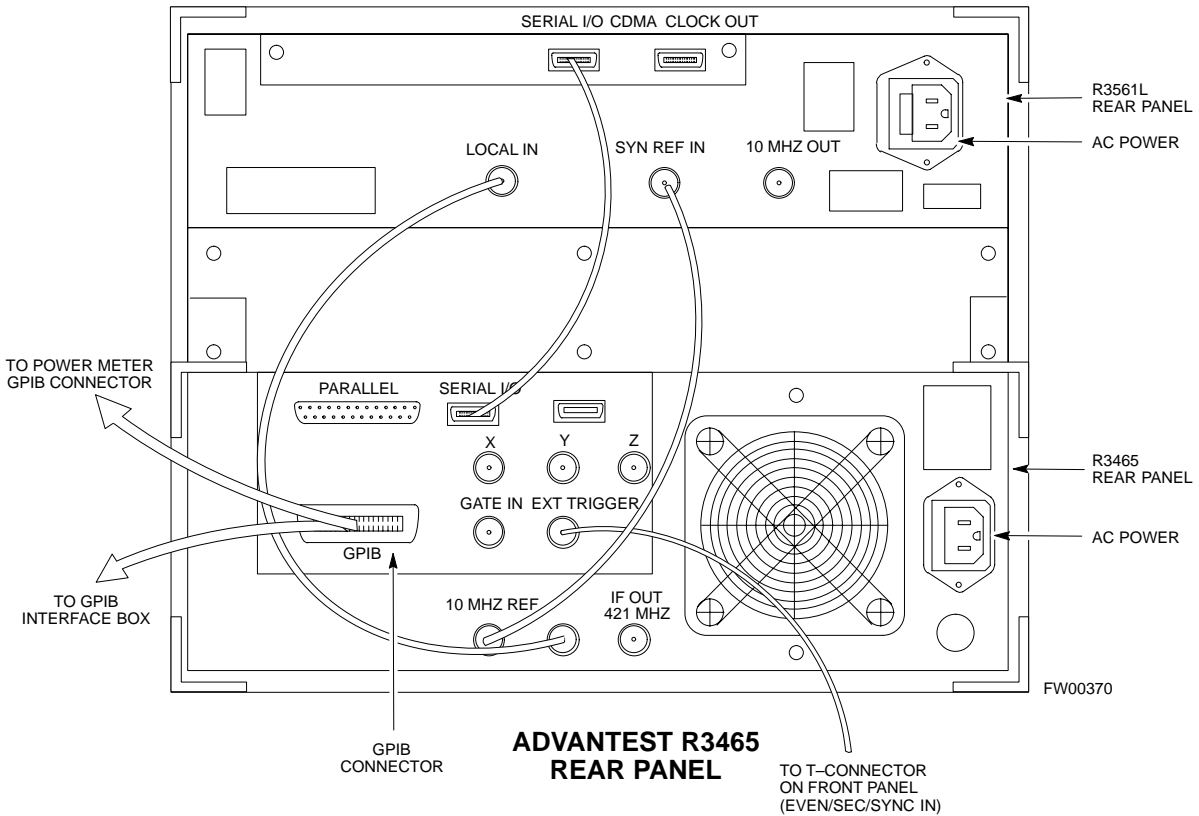
Table F-6: Pretest Setup for HP8935	
Step	Action
1	Unplug the memory card if it is plugged in.
2	Press the Shift button and then press the I/O Config button.
3	Press the Push to Select knob.
4	Position the cursor at IO CONFIG and select it.
5	Select Mode and set for Talk&Lstn .

Advantest R3465 Connection

The following diagram depicts the rear panels of the Advantest test equipment as configured to perform automatic tests. All test equipment is controlled by the LMF via an IEEE-488/GPIB bus. The LMF expects each piece of test equipment to have a factory-set GPIB address (refer to Table F-7). If there is a communications problem between the LMF and any piece of test equipment, you should verify that the GPIB addresses have been set correctly and that the GPIB cables are firmly connected to the test equipment.

Figure F-3 shows the connections when **not using** an external 10 MHz Rubidium reference.

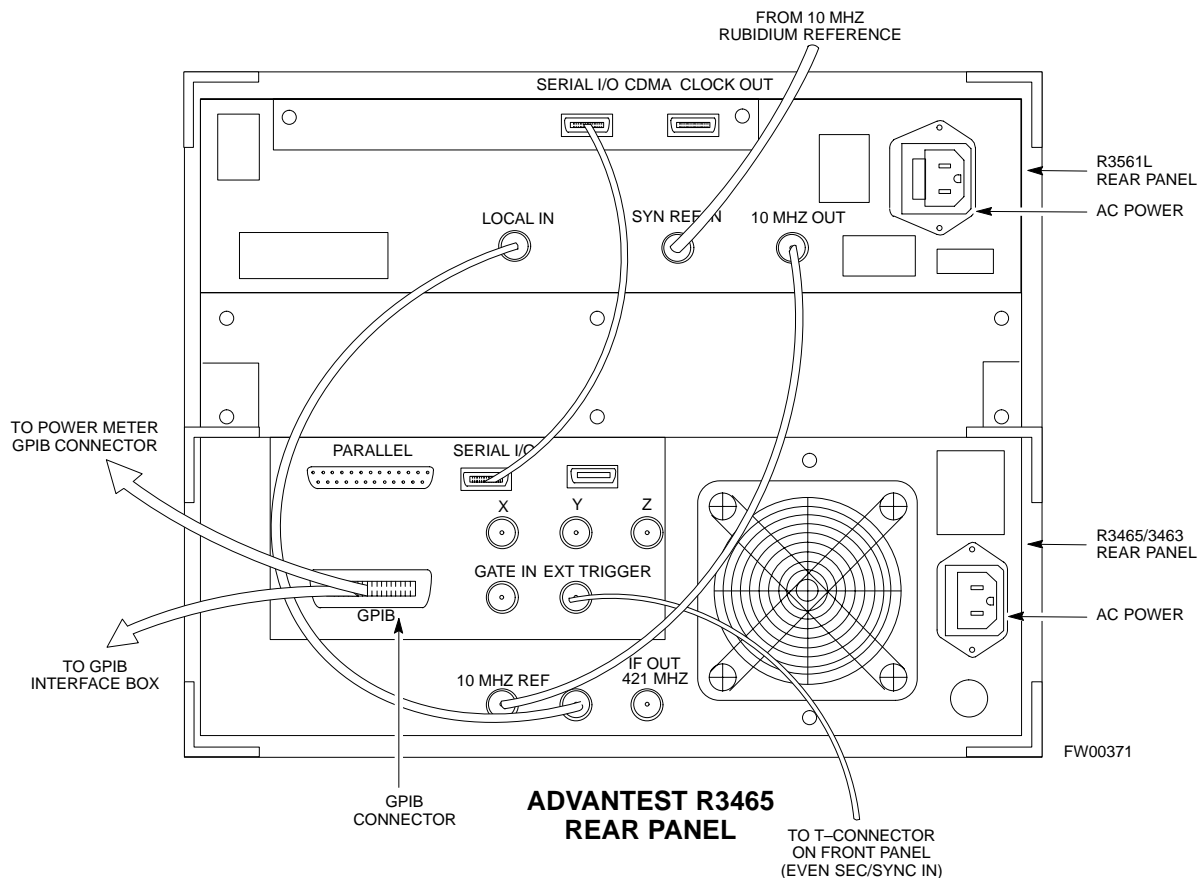
Figure F-3: Cable Connections for Test Set without 10 MHz Rubidium Standard



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Figure F-4 shows the connections when **using** an external 10 MHz Rubidium reference.

Figure F-4: Cable Connections for Test Set with 10 MHz Rubidium Standard



F

Test Equipment Preparation – continued

R3465 GPIB Address & Clock setup

Follow the steps in Table F-7 to set the GPIB address and clock for the **Advantest** R3465 equipment.

Table F-7: Advantest R3465 GPIB Address and Clock Setup	
Step	Action
1	<p>Communications test set GPIB address=18 (<i>perform the following to view/set as required</i>)</p> <p>Perform the following to set the standard parameters on the test set:</p> <ul style="list-style-type: none"> • Push the SHIFT then PRESET pushbutton (just below the CRT display). • Push the LCL pushbutton (CW in Measurement just below the CRT display) <ul style="list-style-type: none"> – Push the GPIB and Others CRT menu key to view the current address. – <i>If required</i>, change GPIB address to 18 (<i>rotate the vernier knob to set, push the vernier knob to enter</i>)
2	<p>Verify the current Date and Time in upper/right of the CRT display (<i>perform the following to set if required</i>)</p> <p>Communications test set GPIB address=18 (<i>perform the following to view/set as required</i>)</p> <ul style="list-style-type: none"> • Push the Date/Time CRT menu key • <i>If required</i>, change to correct Date/Time (<i>rotate the vernier knob to select and set, push the vernier knob to enter</i>) • Push the SHIFT then PRESET pushbutton (just below the CRT display).

Pretest Setup for Advantest R3465

Before the Advantest R3465 analyzer is used for LMF controlled testing it must be set up correctly for automatic testing.

Table F-8: Pretest Setup for Advantest R3465	
Step	Action
1	Press the SHIFT button so the LED next to it is illuminated.
2	Press the RESET button.