

IST8310 User Manual v1.5

Confidential Information



IST8310 Driver Settings

- I²C default (CAD0, CAD1 floating) slave address: 0Eh(7-bit) / 1Ch(8-bit)
- Register initial settings (to be set in Stand-by mode) :
 - 1) Write 24h into 0x41h \leq 16 times internal average setup (low noise mode)
 - 2) Write C0h into 0x42h \leq Set/Reset pulse duration setup
- Read Process :
 - 1) Write 0Ah into 0x01h (Single Measurement Mode)
 - 2) Wait 6ms (minimum waiting time for 16 times internal average setup)
 - 3) Read sequential 6 bytes from 0x03h, which are: X_{Low} , X_{High} , Y_{Low} , Y_{High} , Z_{Low} , Z_{high} and construct X, Y, Z output raw data
 - 4) [Do Cross-axis Compensation process \(page 3~4\)](#)
 - 5) *Do software average (page 5, optional)*
 - 6) Rep1)~4) or 5)

Confidential Information

Cross-Axis Compensation Flow

Read the cross-axis data (Hex, 2's complement, LSB) from 8310's registers 0x9Ch~0xADh

Data Processing :

1. Combine every 2 bytes to construct 9 cross-axis raw data
2. Hex to Dec
3. Multiply by a constant $M=3/20$

Get "transformation matrix" A (3 x 3) based on page 4's information

Multiply "transformation matrix A" by "IST8310 3-axis output raw data"

(A x Raw Data)

Cross-axis compensation finished, get orthogonal 3-axis output data (Dec, mili-Gauss)

Cross-Axis Compensation

Compensation Formula :

$$A = \begin{pmatrix} 50 & 0 & 0 \\ 0 & 50 & 0 \\ 0 & 0 & 50 \end{pmatrix} \times \begin{pmatrix} X_{11} & X_{21} & X_{31} \\ X_{12} & X_{22} & X_{32} \\ X_{13} & X_{23} & X_{33} \end{pmatrix}^{-1}$$

$X_{11} \sim X_{33}$ are stored in 8310's registers, from 9Ch~ADh; each 2 bytes represents one cross-axis data (Hex, 2's complement, LSB) ◦

A: Cross-axis transformation matrix

$X_{11} \sim X_{33}$: Cross-axis data obtained in 8310 FT process.

Y_{ab} to X_{ab} process :

1. Combine every 2 bytes to form 9 cross-axis raw data (Y_{ab})
2. Hex to Dec
3. Multiply by a constant $M=3/20$

$X_{11} = Y_{11} * M$, $X_{12} = Y_{12} * M$, $X_{13} = Y_{13} * M$, and so on...

Parameter Y_{ab} (to be processed to X_{ab})	Register Addresses (Low Byte, High Byte)
Y_{11}	9C 9D
Y_{12}	9E 9F
Y_{13}	A0 A1
Y_{21}	A2 A3
Y_{22}	A4 A5
Y_{23}	A6 A7
Y_{31}	A8 A9
Y_{32}	AA AB
Y_{33}	AC AD

IST8310 Software Average Method (Optional)

- Average Method:

$$X_{avg1}=(X_m+X_{m-1}+X_{m-2}+X_{m-3})/4,$$

$$X_{avg2}=(X_{m-1}+X_{m-2}+X_{m-3}+X_{m-4})/4,$$

$$X_{avg3}=(X_{m-2}+X_{m-3}+X_{m-4}+X_{m-5})/4,$$

and so on...

(Use 4 sequential data to construct a new data)

* $X_m, X_{m-1}, X_{m-2}, X_{m-3}, X_{m-4}, X_{m-5}$ are sequential orthogonal 3-axis output data .

* $X_{avg1}, X_{avg2}, X_{avg3}$ are the final data feed to your processor.

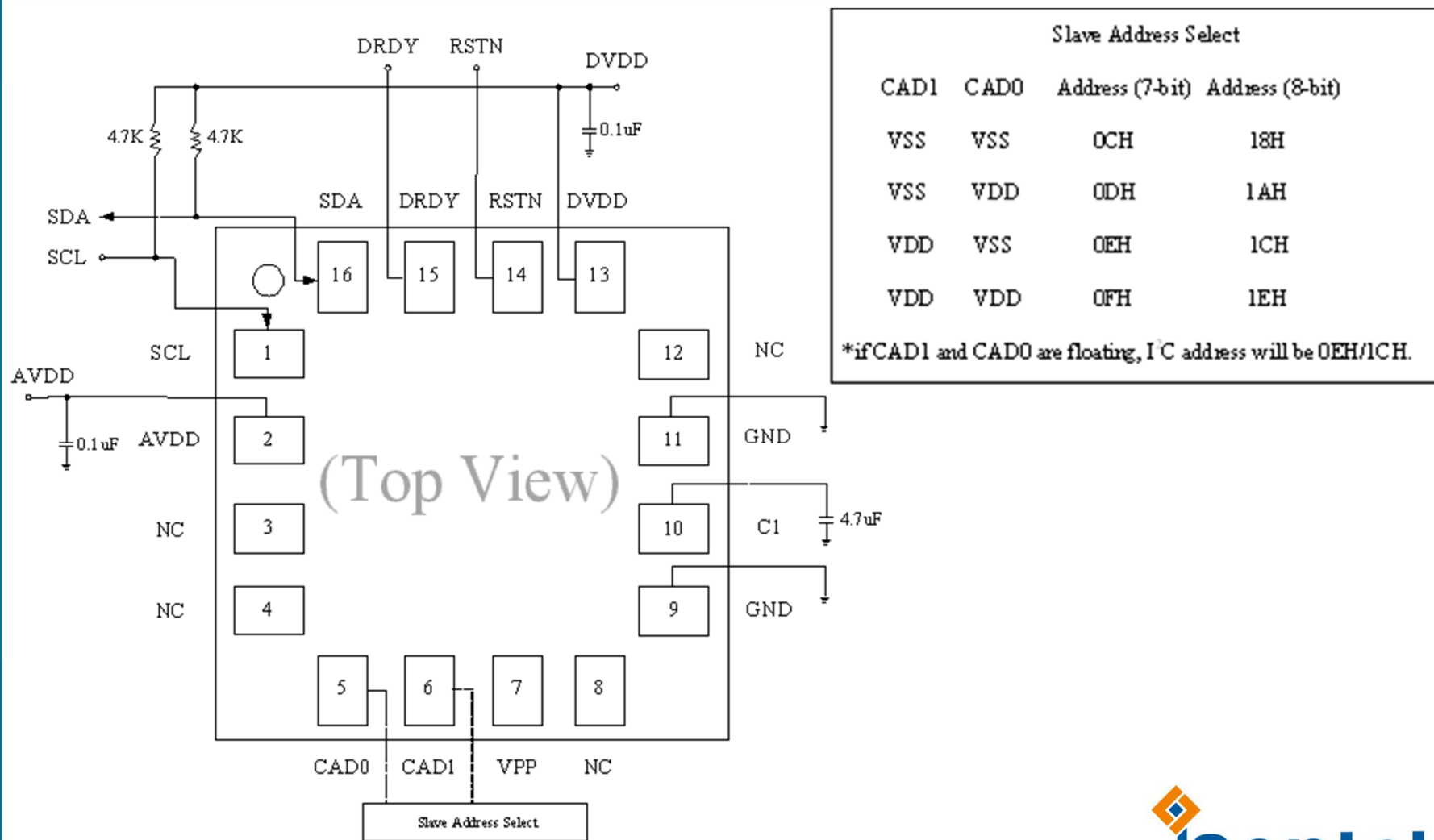
IST8310 Pin Table

Pin	Name	Function
1	SCL	I ² C serial clock
2	AVDD	Analog supply voltage, 1.72~3.6V
3	NC	Not use
4	NC	Not use
5	CAD0	I ² C slave address
6	CAD1	I ² C slave address
7	VPP	Test pin, floating connection is suggested
8	NC	Not use
9	VSS	GND
10	C1	Set/Reset function, 4.7uF
11	VSS	GND
12	NC	Not use
13	DVDD	Digital supply voltage, 1.72~3.6V
14	RSTN	Reset pin, resets registers by setting it to "Low". Internally pulled to "High" as default. MCU connection is suggested.
15	DRDY	Data ready indication, output pin only
16	SDA	I ² C serial data

Data from IST8310 datasheet.

Confidential Information

IST8310 Application Circuit



Slave Address Select			
CAD1	CAD0	Address (7-bit)	Address (8-bit)
VSS	VSS	0CH	18H
VSS	VDD	0DH	1AH
VDD	VSS	0EH	1CH
VDD	VDD	0FH	1EH

*if CAD1 and CAD0 are floating, I²C address will be 0EH/1CH.

Data from IST8310 datasheet.

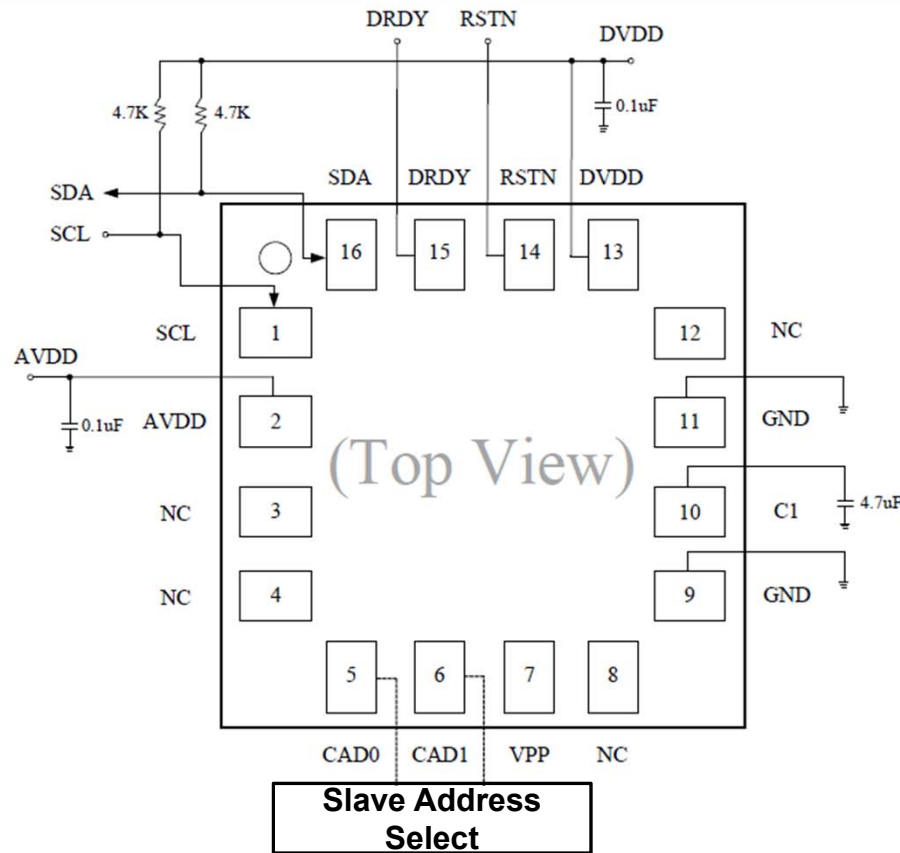
Confidential Information

Pin-to-Pin Information to HMC5883L/5983

IST8310 p2p to HMC5883L/5983 (1/2)

Pin No.	IST8310	HMC5883L	HMC5983	Comments
1	SCL	SCL	SCL/SPI_SCK	IST8310 doesn't support SPI, otherwise compatible.
2	AVDD	VDD	VDD	Compatible (IST8310:1.72~3.6V; HMC5x83L: 2.16~3.6V)
3	NC	NC	NC	Compatible
4	NC	S1	SPI_CS	Compatible (IST8310 doesn't care, no connection inside)
5	CAD0	NC	SPI_SDO	Compatible (IST8310 slave address select, see page 5)
6	CAD1	NC	I ² C/~SPI	Compatible (IST8310 slave address select, see page 5)
7	VPP	NC	NC	Compatible (VPP pin can be connected to GND or floating)
8	NC	SETP	SETP	Compatible (IST8310 doesn't care, no connection inside)
9	VSS	GND	SoC	Compatible (for HMC5893, keep SoC signal = "0")
10	C1	C1	C1	Compatible
11	VSS	GND	GND	Compatible
12	NC	SETC	SETC	Compatible (IST8310 doesn't care, no connection inside)
13	DVDD	VDDIO	VDDIO	Compatible
14	RSTN	NC	NC	Compatible (RSTN pin can be connected to MCU or floating)
15	DRDY	DRDY	DRDY	Compatible
16	SDA	SDA	SDA/SPI_SDI	IST8310 doesn't support SPI, otherwise compatible.

IST8310 p2p to HMC5883L/5983 (2/2)



PN	Pin 6	Pin 5	i2c Address
HMC5883L	NC	NC	0EH / 1CH
HMC5983	VDD	NC	0EH / 1CH

Slave Address Select			
CAD1	CAD0	Address (7-bit)	Address (8-bit)
VSS	VSS	0CH	18H
VSS	VDD	0DH	1AH
VDD	VSS	0EH	1CH
VDD	VDD	0FH	1EH

*if CAD1 and CAD0 are floating, I²C address will be 0EH/1CH.

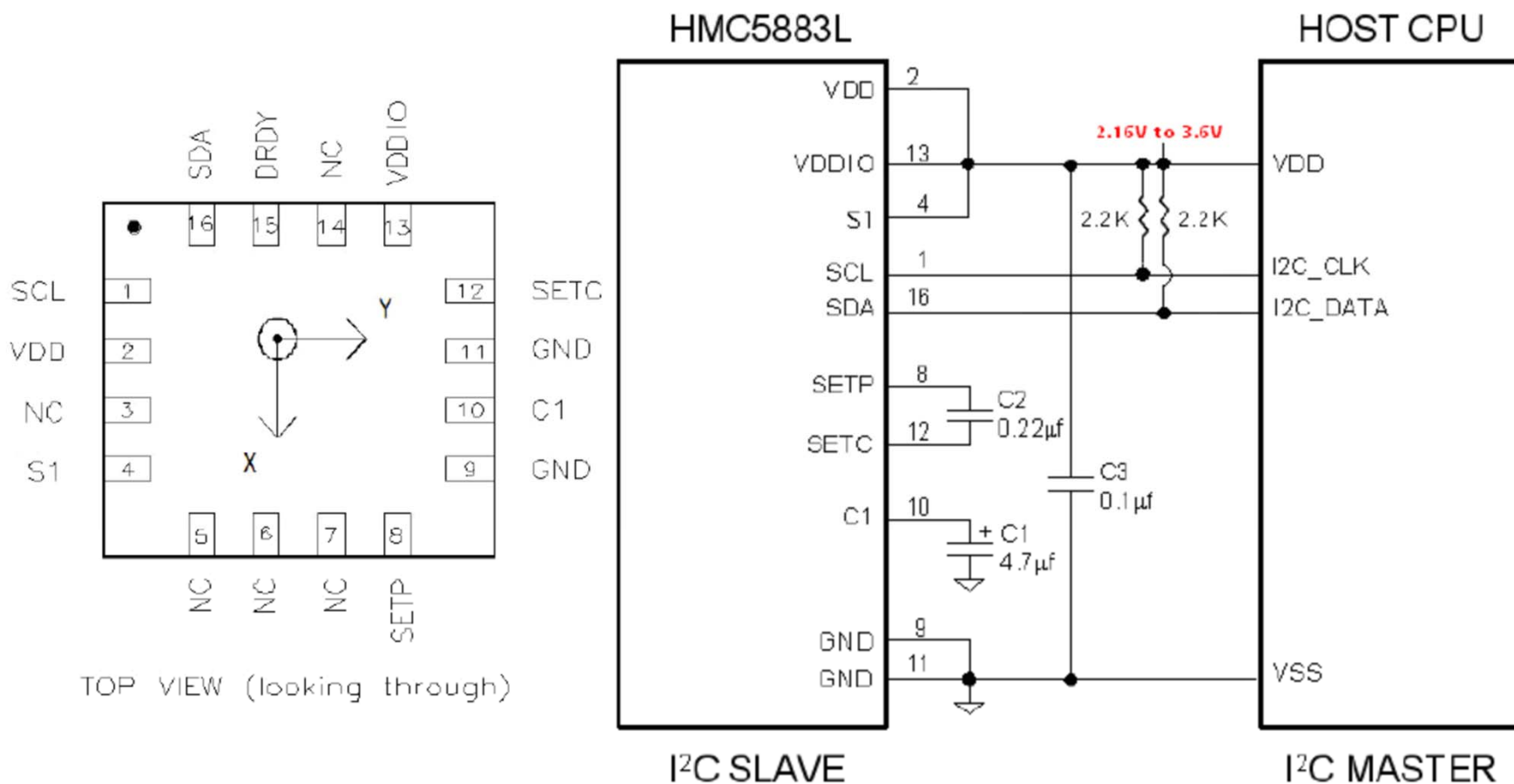
- ***I²C slave address is 0EH(7-bit)/ 1CH(8-bit) when you mount IST8310 onto HMC5883L/5983's PCB.***
- ***Nothing else needs to be taken care of.***

Reference Information

HMC5883L Pin Table

Pin	Name	Description
1	SCL	Serial Clock – I ² C Master/Slave Clock
2	VDD	Power Supply (2.16V to 3.6V)
3	NC	Not to be Connected
4	S1	Tie to VDDIO
5	NC	Not to be Connected
6	NC	Not to be Connected
7	NC	Not to be Connected
8	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection
9	GND	Supply Ground
10	C1	Reservoir Capacitor (C1) Connection
11	GND	Supply Ground
12	SETC	S/R Capacitor (C2) Connection – Driver Side
13	VDDIO	IO Power Supply (1.71V to VDD)
14	NC	Not to be Connected
15	DRDY	Data Ready, Interrupt Pin. Internally pulled high. Optional connection. Low for 250 μ sec when data is placed in the data output registers.
16	SDA	Serial Data – I ² C Master/Slave Data

HMC5883L Application Circuit



Data from HMC5883L datasheet.

Confidential Information

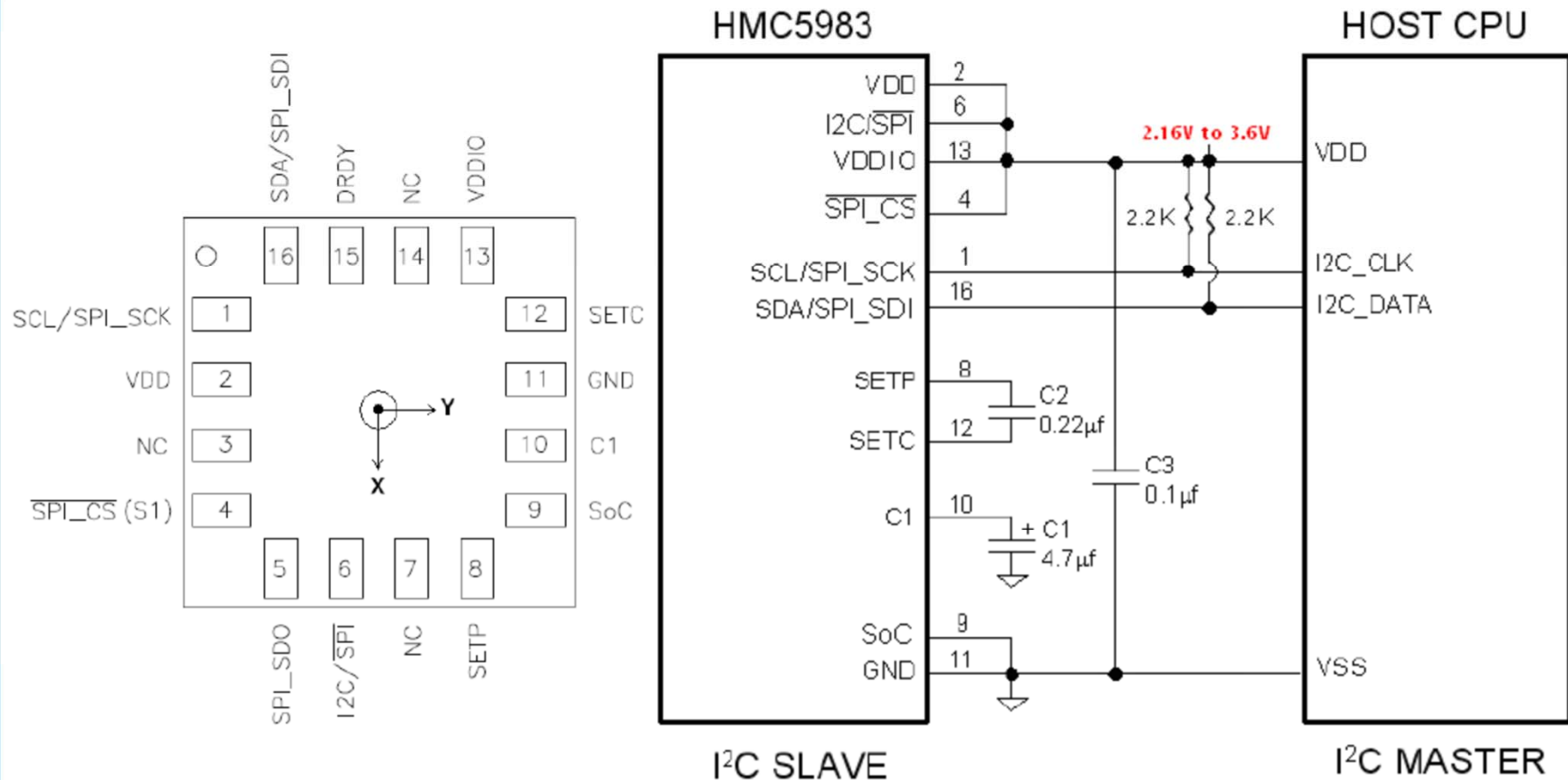
HMC5983 Pin Table

Pin	Name	Description
1	SCL/SPI_SCK	Serial Clock – I ² C Master/Slave Clock or SPI Serial Clock
2	VDD	Power Supply (2.16V to 3.6V)
3	NC	Not to be Connected
4	SPI_CS	Chip Select line for SPI (active low). Tie to VDDIO for I ² C Interface
5	SPI_SDO	SPI Serial Data Out
6	I ² C /~SPI	I ² C / SPI selection pin. Connect to VDD for I ² C (Also connect SPI_CS to VDDIO). Connect to GND for SPI.
7	NC	Not to be Connected
8	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection
9	SoC	Start of Conversion (leading edge active) Connect to Ground when this function/pad is not used in application.
10	C1	Reservoir Capacitor (C1) Connection
11	GND	Supply Ground
12	SETC	S/R Capacitor (C2) Connection – Driver Side
13	VDDIO	IO Power Supply (1.71V to VDD)
14	NC	Not to be Connected. No internal connection.
15	DRDY	Data Ready, Interrupt Pin. Internally pulled high. Optional connection. Low for >200 µsec when data are placed in the data output registers.
16	SDA/SPI_SDI	Serial Data – I ² C Master/Slave Data or SPI Serial Data In or SPI Serial Data I/O (SDI/O) for 3-wire interface

Data from HMC5983 datasheet.

Confidential Information

HMC5983 Application Circuit



Data from HMC5983 datasheet.

Confidential Information