Laboratory Manual

ECEN-325 Electronics

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Contents

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We would like to thank TAMU Qatar for the financial support while this lab manual is being constantly updated. We are thankful to National Instruments for generous donations of several NI Elvis Workstations.

Add comments on how to improve the lab manual. All suggestions and comments are welcome. Give them to your TA or send them by email to jsilva@ece.tamu.edu.

Lab 1: Network Analysis and Bode plots

Objectives:
The purpose of the lab is to investigate the frequency response of a passive filter and learn the fundamentals about circuit design and analysis in the frequency domain.

List of Equipment required:

a. Protoboard
b. Capacitors
c. Resistors
d. Oscilloscope
e. Function generator
f. Frequency counter
g. Digital Multimeter

Introduction

Frequency domain representation

The frequency response is a representation of the system's response to sinusoidal inputs at varying frequencies; it is defined as the magnitude ratio and phase difference between the input and output signals. If the frequency of the source in a circuit is used as a reference, it is possible to have a complete analysis in the frequency domain and time domains. Frequency domain analysis is easier than time domain analysis because differential equations used in the time domain are mapped into linear equations that are function of the frequency variable $s\ (\sigma+j\omega)$. It is important to obtain the frequency response of a circuit because we can predict its response to any input signal.

Filters are important blocks in communication and instrumentation systems. They are widely used in radio receivers, power supply circuits, and noise reduction systems. There are four general types of filters: Low-pass filters (LPF) that pass low frequency signals and reject high frequency components; Band-pass filters (BPF) that pass signals within a certain frequency range; High-pass filter (HPF) pass high frequency signals and rejects low frequency components; and Band-Reject (Stop) filters that reject signals that have frequencies within a certain band.

In this laboratory experiment we will plot the frequency response of a network by analyzing RC passive filters. We can characterize the filter by two features of the frequency response:

1. The difference between the magnitude of the output and input signals (given by the amplitude ratio)
2. The time lag or lead between input and output signals (given by the phase shift)

To plot the frequency response, many frequencies are used and the value of the transfer function at these frequencies is computed. A particularly important method of displaying frequency response data is the Bode plot. A Bode plot is the representation of the magnitude and phase of $H(s)$. $H(s)$ is the transfer function of a system, and $s = \sigma + j\omega$ where ω is the frequency variable in rad/s.

Phase measurement
The phase angle can be calculated by determining the time shift Δt. To determine Δt, display the input and output sine waves on the two channels of the oscilloscope simultaneously and calculate the phase difference as follows,

$$\text{Phase difference (in degrees)} = 360\ \frac{\Delta t}{T}$$

where Δt is the time-shift of the zero crossing of the two signals, and T is the signal's period. This is illustrated in Fig. 1.

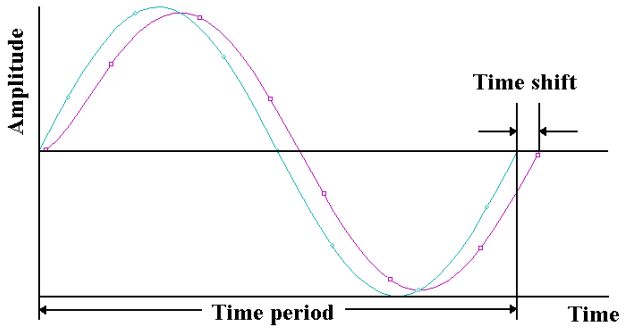


Fig. 1. Phase difference

Pre-laboratory exercise

1. For the circuit shown in Fig. 2, derive the transfer function for v_o/v_{in} in terms of *R and C*, and find the expressions for the magnitude and phase responses. Express the transfer function in the form

$$\frac{v_o}{v_{in}} = \frac{1}{1+\frac{s}{\omega_p}}$$

where ω_p is the pole frequency location in rad/sec.

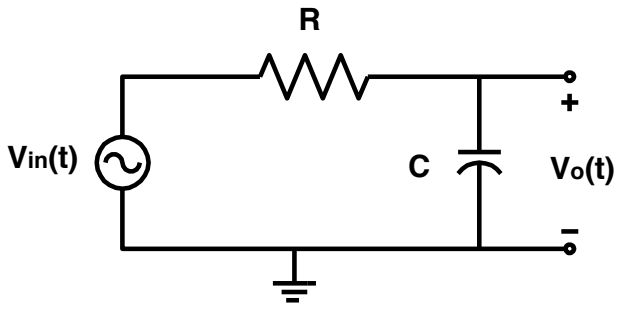


Fig. 2. First order low-pass filter

2. The corner frequency of the low-pass filter is defined as the frequency at which the magnitude of the gain is $1/\sqrt{2} = 0.707$. This is also called the half power frequency (since $0.707^2 = 0.5$), and the -3dB frequency since $20\log_{10}(0.707) = -3$ dB. Find the corner frequency, in terms of R and C, in both rad/s and Hz.
3. For $C = 47$ nF, find R so that the -3 dB frequency is 3.3 kHz. Draw the Bode plots.
4. Simulate the low pass filter circuit using a Spice simulator. Compare the simulation results with your calculation. Attach the magnitude and phase simulation results.
5. For the circuit shown in Fig. 3, derive the transfer function for v_o/v_{in} in terms of R_i and C_i, and find the expressions for the magnitude and phase responses. Express the transfer function in the form

$$\frac{v_o}{v_{in}} = \frac{1}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

where ω_{p1} and ω_{p2} are the pole frequency locations (in rad/s) in terms of R_i and C.
6. Design (find component values) a passive second-order low pass filter such as the one shown in Fig. 3. Determine R_1 and R_2 for $C = 47$ nF. The first pole is at 1 kHz and the second pole is at 4 kHz. You must use a circuit simulator to verify your design.
7. Draw the bode plots and compare them to the magnitude and phase simulation results from PSpice.

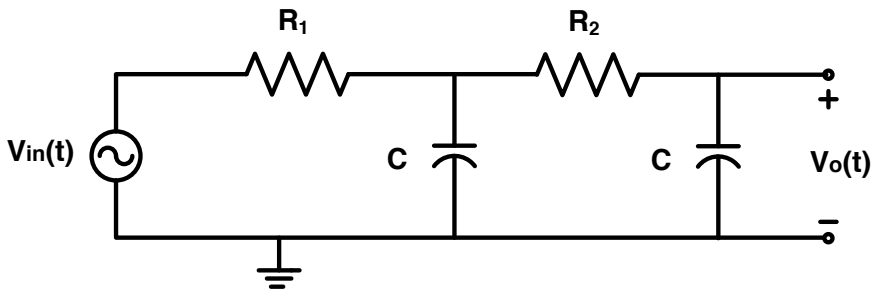


Fig. 3. Second order low pass filter

Lab Measurement:

Part A. First order low pass filter

1. Build the circuit shown in Fig. 2 with the values of *R* and *C* you choose in the pre lab. Apply a 6 Vpp sinusoidal signal from the function generator to the input and use the high Z option on your signal source (ask you TA for assistance).
2. Connect channel 1 of the oscilloscope across $v_{in}(t)$ and channel 2 across $v_o(t)$. Set the oscilloscope to display both inputs vs. time by pressing CH1 and CH2. Keep the generator voltage constant. Use the cursors on the oscilloscope to measure the amplitude ratio v_o/v_{in} and the phase difference between v_o and v_{in} for at least 10 different frequencies in the range $0.1\,f_{-3dB}$ and $10\,f_{-3dB}$, including f_{-3dB}. Measuring the phase shift is an accurate method of determining the 3-dB frequency. What is the phase shift at f_{-3dB}?

Part B. Noise Filtering

1. Noise is modeled as a high frequency, small amplitude signal that is superimposed onto an ideal sine wave. A low pass filter can attenuate the high frequency noise while preserving the wanted signal.
2. Start the *ArbWave* software;
3. Generate a sine wave. Select a *sine* wave using the *Waveforms* icon;
4. Add noise to signal. Select the *edit* icon and use the *select all* utility, then select the *math* icon, choose the *add* utility. In the add function box, select the standard wave option. Next select the *noise* waveform and adjust it to 0.3 V. In the *add* function box, choose the *fit amplitude* option;
5. Send the noisy waveform to the signal generator. Use *I/O* icon and select *send waveform*. Adjust the amplitude of the signal to 6 Vpp, and the frequency to 0.25 kHz;
6. Apply this signal to your low-pass filter and observe the input and output signals;
7. Take a screen shot of both the noisy and filtered signals on the oscilloscope.

Part C. Second order low pass filter

1. Build the circuit shown in Fig. 3 with *R* and *C* you found in the pre lab. Apply a 6 Vpp sinusoid from the function generator to the input.
2. Find the 3-dB signal-attenuation frequency f_{-3dB} and 40 dB signal-attenuation frequency f_{-40dB}.

Lab Report:

1. Present clearly all your results. Plot the magnitude and phase responses on the semi-log graph; see your lecture notes or textbook for some examples.
2. Describe and comment on the differences you found in both first- and second-order low pass filters; consider both magnitude and phase characteristics.
3. Compare the hand-calculated, PSpice simulated and measured results. Comment on possible reasons for any differences between them.
4. Discuss the noise filtering operation of the low-pass filter.
5. Include some conclusions.

Lab 2: Introduction to NI Elvis Environment.

Objectives:

The purpose of this laboratory is to introduce the NI Elvis design and prototyping environment. Basic operations provided by Elvis such as digital Multimeter, function generator, oscilloscope and bode analyzer are explained. Passive RC high pass and second-order low pass filter circuits are characterized using NI Elvis.

List of Equipment required:

a. NI Elvis bench top workspace.
b. NI Elvis Digital Multimeter Soft Panel Instrument (SFP).
c. NI Elvis Function Generator SFP.
d. NI Elvis Oscilloscope SFP.
e. Bode Analyzer SFP.
f. Resistors: different values.
g. Capacitors: different values.

Introduction:

The National Instruments Educational Laboratory Virtual Instrumentation Suite (NI ELVIS) is a LabVIEW and computer based design and prototyping environment. NI ELVIS consists of a custom-designed bench top workstation, a prototyping board, a multifunction data acquisition device, and LabVIEW based virtual instruments. This combination provides an integrated, modular instrumentation platform that has comparable functionality to the DMM, Oscilloscope, Function Generator, and Power Supply found on the laboratory workbench.

Fig. 1. NI Elvis System

The NI ELVIS Workstation can be controlled either via manual dials on the stations or through software virtual instruments. The NI ELVIS software suite contains virtual instruments that enable the NI ELVIS workstation to perform functions similar to a number of much more expensive instruments. This environment consists of the following two components:

1. Bench top hardware workspace for building circuits.
2. NI Elvis Software interface consisting of Soft Front Panel (SFP) instruments.

The NI Elvis software also includes additional Lab view VIs for custom control and access to the features of NI Elvis hardware workspace.

We will complete the following tasks in this lab:

- *Part A*. Using Digital Multimeter Soft Panel (SFP) to measure electronic component properties.
- *Part B*. Using Function Generator SFP and Oscilloscope SFP for characterizing a RC high pass filter.
- *Part C*. Using Bode Analyzer SFP for characterizing a RC high pass filter.
- *Part D*. Using NI Elvis to characterize the RC high pass circuits designed in the pre lab.

Pre-laboratory exercise:

No pre-laboratory exercises are required for Parts A, B, and C. Please complete the following pre-laboratory exercises for Part D.

1. For the circuit shown in Fig. 2A, derive the transfer function for v_o/v_{in} in terms of R and C**,** and find the expressions for the magnitude and phase responses. Express your results in the form

$$\frac{v_o}{v_{in}} = \frac{\frac{s}{\omega_p}}{1+\frac{s}{\omega_p}} = \frac{s}{\omega_p + s}$$

where ω_p is the pole frequency location in rad/s

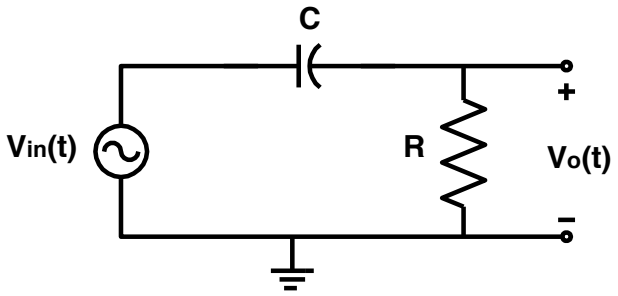


Fig. 2A. First order high pass filter (integrator)

2. For C = 47 nF, find R so that pole frequency location is 3.3 kHz.
3. Draw the Bode plot and compare it to the magnitude and phase simulations from PSpice.

Lab Measurement:

Part A. Measuring Component Values using NI Elvis Digital Multimeter

Complete the following steps to measure the value of a resistor using NI Elvis environment.

1. First ensure that the Power Supply to the prototype board has been switched off. (Refer to Fig. 2). Note that the system power is switched on. The system power switch is located at the back of the prototyping station.

Fig. 2. NI ELVIS Bench top workstation.

2. Insert the resistor on the prototype board.
3. Connect the two terminals of the resistor between V and COM terminals as shown in Fig. 4. banana jack connections (refer to Fig. 4).

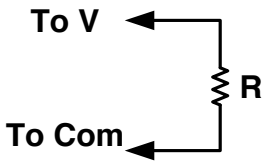


Fig. 3. Using Digital Multimeter SFP to measure value of a resistor.

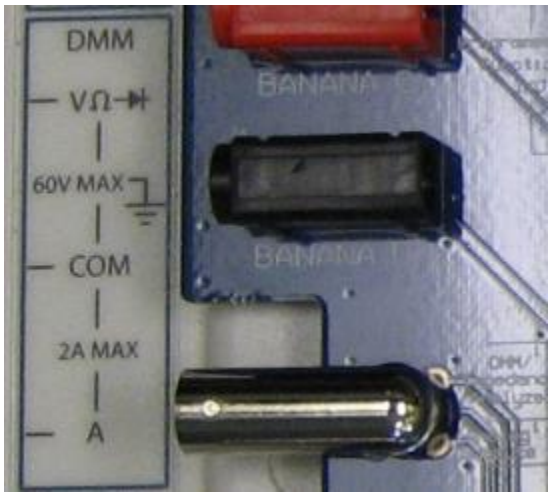


Fig. 4. DMM Ports on the Elvis Prototype Board.

4. Connect the two terminals of capacitor between DUT+ and DUT- terminals on the proto board. Refer to Figs. 5 and 6.

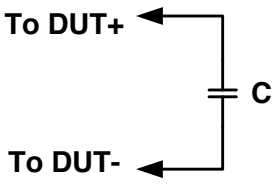


Fig. 5. Using Digital Multimeter SFP to measure value of a resistor

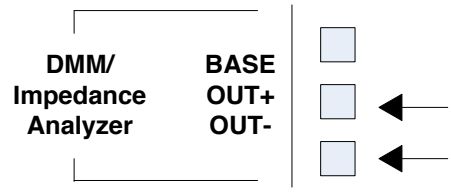


Fig. 6. DMM Ports on the Elvis Prototype Board.

5. Apply power to the proto board by switching the Prototype Board Power switch to the up position. The three indicator LEDs +15V, -15V and +5V should now be lit as show in Fig. 7.

Fig. 7. Elvis Protoboard supply LEDs.

6. Go to the program menu on your computer and launch NI ElvisSmx Instrument Launcher in the NI ElvisSmx program. The interface should appear on your screen as shown in Fig. 8. This interface shows all the Virtual Soft Front Panels (SFP) available in NI Elvis.

Fig. 8. NI Elvis Software interface.

7. Click on the Digital Multimeter (DMM). This SFP can be used for a variety of operations.
8. A message box will open prompting you to use the Null operation for ensuring accuracy in DMM measurements. Read the message and click OK.
9. Click the Null button.
10. Click the Ohm button to use the Digital Voltmeter function (DMM-Ohm) to measure the value of the resistor. If the Function Generator is in manual mode, the resistance and capacitance buttons are disabled. In order to control these buttons using the SFP, ensure that the manual mode is turned off on the workstation. Once the measurement is successful the output should appear as shown in Fig. 9. You have now successfully used the resistor ohm-meter with the NI Elvis SFP.

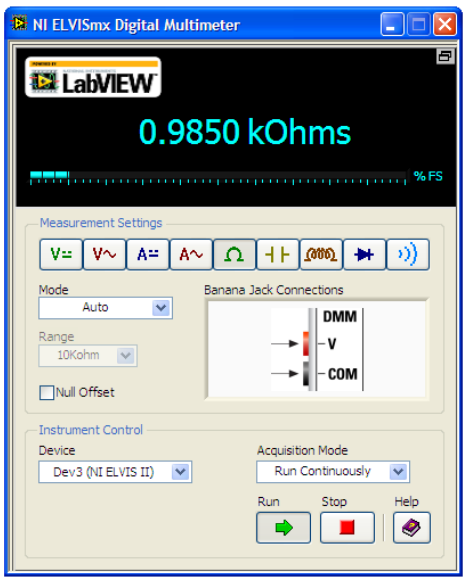


Fig. 9. Digital Multimeter SFP indicating the resistor's value

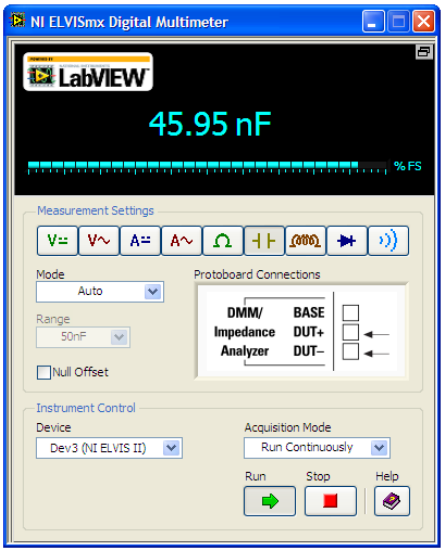


Fig. 10. Digital Multimeter SFP indicating the capacitor's value.

11. We now continue to measure value of a capacitor.
12. Switch off the Prototype Board Power. Close the Digital Multimeter SFP.
13. Replace the 1 kΩ resistor with the capacitor.
14. Switch on the Prototype Board Power. Launch the Digital Multimeter SFP.
15. Click the Null Button.
16. Click the Capacitance button to use the Digital Capacitance Meter function to measure the value of the capacitor. Once the measurement is successful the output should appear as show in Fig. 10.

Part B. Analog RC Filter Analysis using Function Generator and oscilloscope

This section provides an introduction to using NI Elvis for AC characterization of a simple RC low pass filter. We will characterize the simple RC filter that we designed in Lab 1. The R and C values should for this low pass filter should be the same as what we used in Lab 1.

1. Ensure that the Prototype Board Power is switched off.
2. Connect the RC filter circuit on the proto board as shown in Fig. 11. The input signal for the filter is obtained between 'FGEN' and 'GROUND' pins. The input signal is also connected to Analog Channel-0 (between AI1+/AI1-) and the output signal across the capacitor is connected to Analog Channel-1 (AI0+/AI0-). Connections on the Analog Channels 0 and 1 are used for oscilloscope SFP as further explained in the following steps.

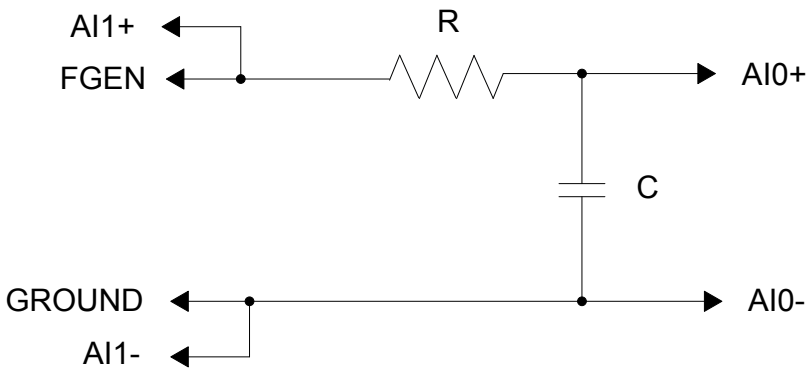


Fig. 11. RC Filter connectivity for AC Characterization.

3. Apply power to the proto board by switching the Prototype Board Power switch to the up position.
4. Go to the program menu on your computer and launch the NI Elvis.
5. From NI Elvis instrument launcher, click on "Function Generator" (FGEN). Ensure that the manual mode is turned off on the workstation so that all the buttons on the function generator window are not disabled. The initial function generator should appear as shown in Fig. 12.

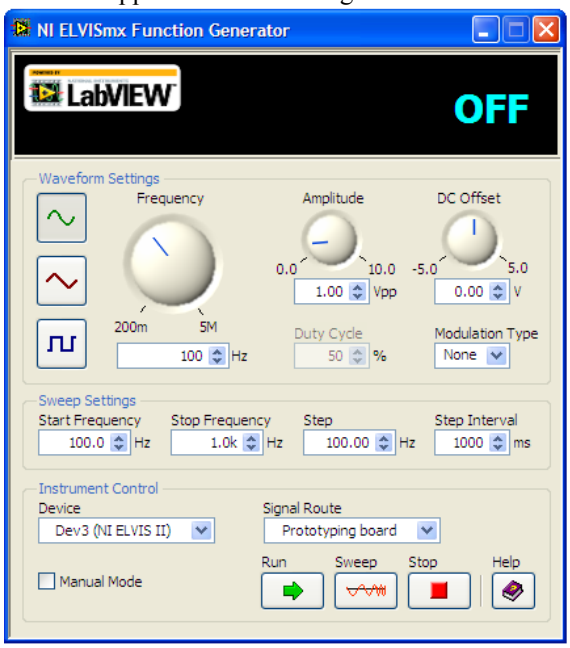


Fig 12. Uninitialized Function generator.

As shown in Fig. 12 and Fig. 13, SFP can be used to:

- Set the Frequency.
- Select the waveform type (Sine, Square or Triangular).
- Select the waveform amplitude (Peak).
- Select the DC offset of the waveform.

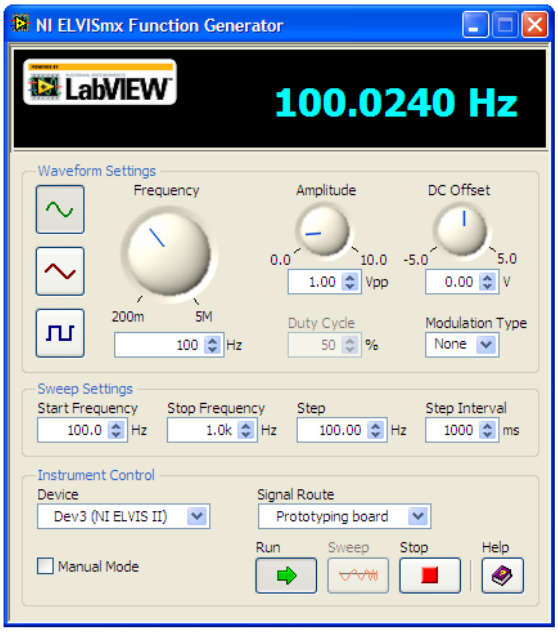


Fig. 13. Function Generator set to produce a 100 Hz sine wave with 1 V amplitude.

6. Use these settings to obtain a 100 Hz sine wave with peak amplitude of 1 V and DC offset of 0 V. Note that this signal will be applied to the RC low pass filter. The function generator SFP should now appear as shown in Fig. 13.
7. From NI Elvis instrument launcher, click on "Scope." The oscilloscope SFP is similar to most oscilloscopes, but NI Elvis oscilloscope can automatically connect to variety of inputs. The initial oscilloscope SFP without any signals should appear as shown in Fig. 14.

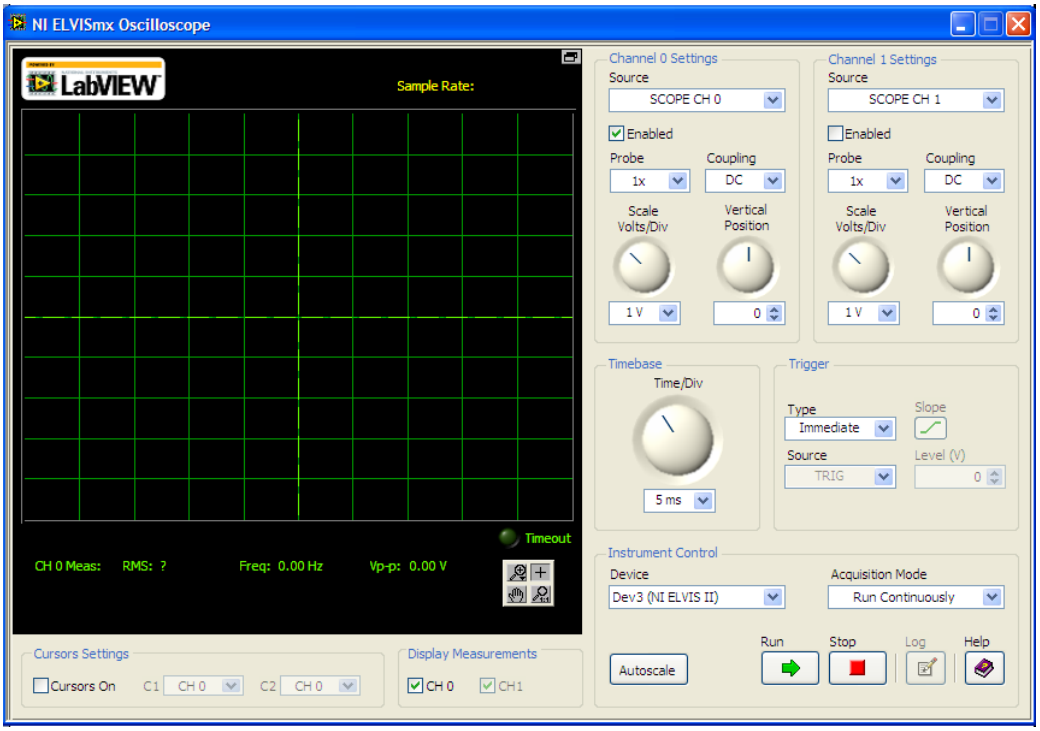


Fig. 14. NI Elvis Oscilloscope interface.

8. The input to the RC circuit is connected to FUNC_OUT port on the prototype board. This input is also connected the Analog Channel-0 (AI1+/AI1-). So, select AI1 in the source pull down list.
9. Click on Auto scale for the amplitude display setting of the signal.
10. This input signal originates from FUNC_OUT. The corresponding SYNC signal is TRIG. In TRIGGER section, select TRIG option. The output should now appear as shown in Fig. 15. This is the input signal for our RC circuit.
11. Now select the output signal on Channel 1 of the oscilloscope SFP. First enable channel 1 by clicking the ON button under Channel 1. Now select AI0 from the Source drop-down list and click on Auto scale. You should now be able to see both input and output on the oscilloscope output. Vertical positions of signals on Channel A and B can be separately adjusted using the vertical position knob.
12. You can change the frequency of the input signal on the FGEN SFP to see the corresponding change on the oscilloscope.
13. Cursors can also be used on the Oscilloscope SFP by clicking the Cursor button to ON. An example measurement using two cursors C1 and C2 to measure the phase shift is shown in Fig. 16.

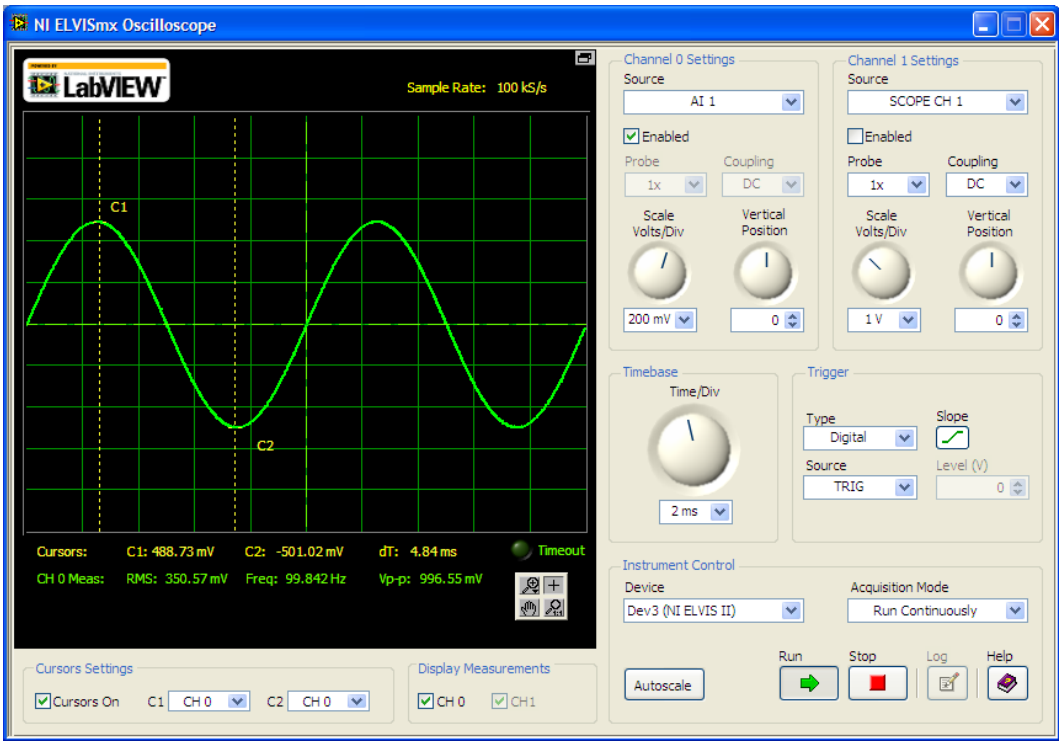


Fig. 15. NI Elvis Oscilloscope showing the input waveform on Channel 0.

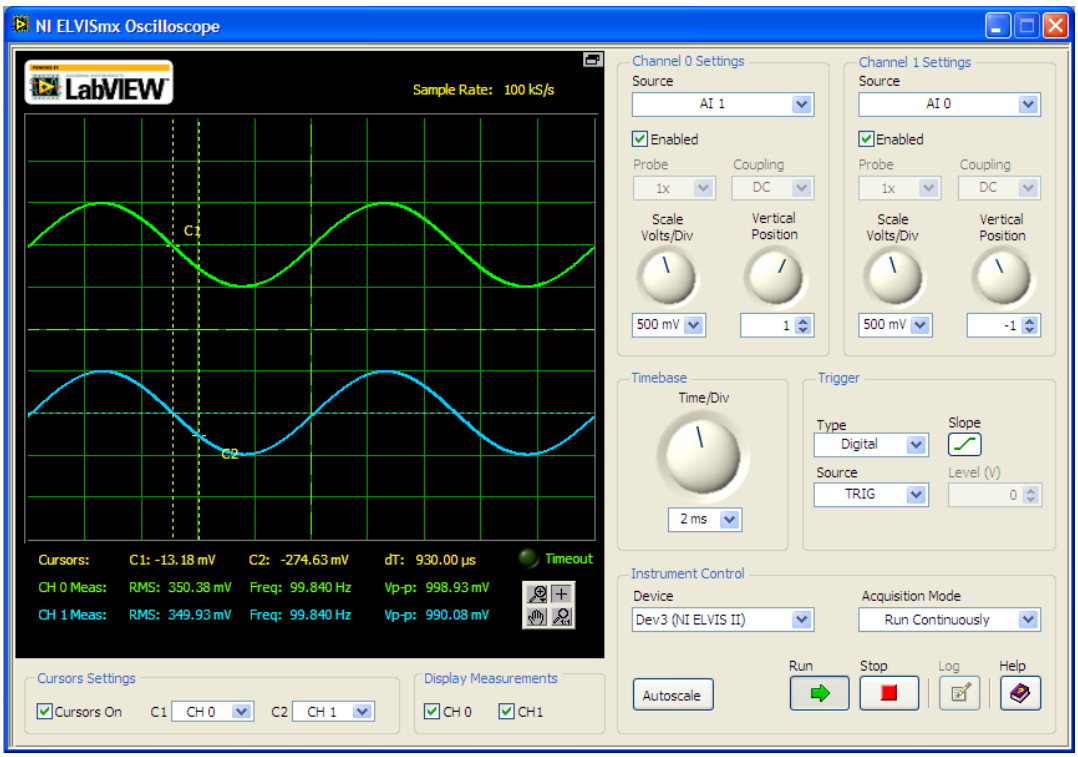


Fig. 16. NI Elvis Oscilloscope showing both input and output on two channels.

14. RMS, Frequency, and Amplitude (Peak-to-peak) measurements are shown at the bottom of the screen.
15. Switch off the supply to the prototype board once the analysis is over.

As explained in this section, we used the function generator (FGEN) and oscilloscope SFP to analyze a RC filter. In this setup:

- The input signal to the filter is provided through the Function generator SFP.
- The input signal to the filter is available on Channel-0 of the oscilloscope (through AI1).
- The output signal of the filter is available on Channel-1 of the oscilloscope (through AI0).
- The trigger source for the oscilloscope is available through TRIG.

By varying the input frequency to the filter, we can obtain the 3-dB bandwidth of the filter using the oscilloscope measurements.

Part C. Analog RC filter analysis using the Bode Analyzer:

NI Elvis has a bode analyzer SFP which facilitates automatic bode plot generation of a given circuit. Complete the following steps to obtain the Magnitude and Phase response of the RC filter:

1. Retain the circuit configuration from the previous section. Note that the circuit should be setup as shown in Fig. 11.
2. Ensure that the connections are correct and switch the prototype board power to ON position.
3. From the NI Elvis instrument Launcher, select Bode (Bode Analyzer). The initial Bode Analyzer SFP should appear as shown in Fig. 17.

Fig. 17. Uninitialized NI Elvis Bode Analyzer window.

4. The Bode analyzer controls the input signal to the circuit from the FUNC_OUT ports. The output signal to be analyzed should be connected to Analog Channel 1 (between AI0+/AI0-). The input signal should also be connected to Analog channel 0 (between AI1+/AI1-).

5. Bode analyzer provides the flexibility to automatically scan the input signal frequency over a range specified by Start/Stop frequency values. The incremental value used during this frequency scan can also be set to a specific value. All these controls can be seen in Fig. 17. The Bode analyzer will not work while FGEN is ON.
6. For analyzing the RC low pass filter, make the following settings on the Bode analyzer SFP.
   - Start frequency: 10 Hz.
   - Stop frequency: 200 kHz.
   - 40 steps per decade (increasing the number of steps improves the accuracy of the measurement).
   - In the Display section, set Y-scale to Auto.
   - Click on RUN.
7. Once the analysis is complete, the output should appear as shown in Fig. 18.
8. In the Fig. 18, the cursor has been placed to measure the 3-dB frequency. This can be achieved by clicking on the Cursors button to "ON" and dragging the cursor using the left mouse button on the plot to the desired position. The cursor can also be shifted to the desired position using the two diamond shaped buttons in the Cursor Position.

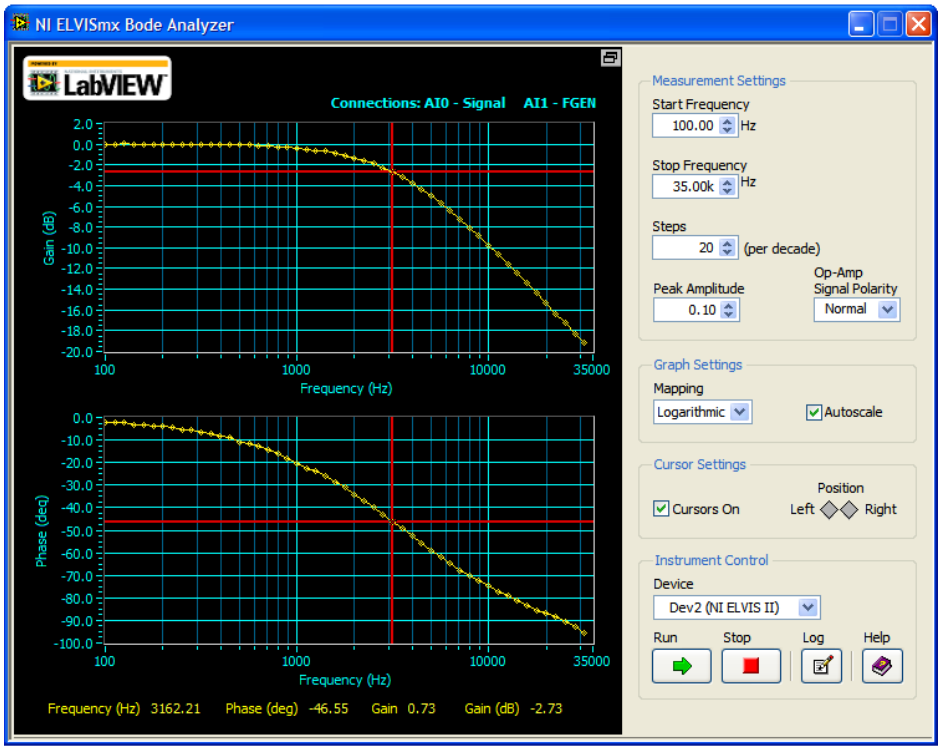


Fig. 18. Bode Analyzer output and measuring the 3dB frequency using cursors.

Part D. RC filter characterization using NI Elvis:

1. Build the second order RC low pass circuit shown in Fig. 3 in Lab 1using the *R* and *C* values that were obtained in Lab 1. Obtain the frequency response of the filter using the bode analyzer SFP as shown in part C.
2. Build the RC high pass circuit shown in Fig. 2A using the *R* and *C* values designed in the pre-laboratory exercise. Obtain the frequency response of the filter using the bode analyzer SFP as shown in part C.

Lab Report:

1. Provide a brief introduction to basic capabilities of the NI Elvis prototype environment.
2. Provide a description of the frequency response obtained for the two circuits (including the screen shots of frequency response plots) obtained in part D of the lab.
3. Describe and comment on the differences (if any) between the frequency responses plots obtained previously using the traditional function generators and oscilloscopes to the results obtained using NI Elvis.
4. Describe and comment on the differences between first order low pass and high pass filters; consider both magnitude and phase characteristics.

Lab 3: Operational Amplifiers-Part I

Objectives:

The purpose of the laboratory is to study the properties of the fundamental amplifier building blocks using commercially available Operational Amplifiers. Inverting and non-inverting amplifiers will be investigated.

List of Equipment required:

a. Dual Trace Oscilloscope
b. Function Generator
c. ±7 V DC Power Supply
d. Digital Multimeter
e. A Protoboard
f. Resistors: different values
g. Capacitors: different values
h. Two 741 Operational Amplifiers
i. NI Elvis environment and Dynamic Signal Analyzer SFP.

Introduction

Practical devices are non-ideal. You can find information about the specifications and performance measures from the manufacture's data sheet. It is an important skill for an engineer to obtain relevant analytical data from data sheets. Data sheets are generally arranged in three main sections:

1. A *General Descriptive* section, which summarizes the important properties of a device, pin-out diagram and equivalent circuit diagrams;
2. A *Maximum Rating* section, which defines the safe limits of device operation;
3. An *Electrical Characteristics* section, which gives information about the ranges of performance for most of the important device parameters. This section usually includes graphical and tabular presentations. The graphs often repeat the data from the tables but give more detailed information. Sometimes the vendors provide test circuits.

Some specifications listed as *typical* are not verified by tests by the manufacturer. Only *minimum* and *maximum* specifications are binding.
In this lab some specifications of the Opamp will be measured. Before that, please be sure to consult the manufacturer's data sheets first.

The time-domain graph of a signal shows how a signal changes with time; a frequency-domain graph shows how much of the signal lies within each given frequency band. A signal can be converted between the time and frequency domains using mathematical transforms. The Fourier transform decomposes a function into a sum of sine waves which have different frequencies. The spectrum of frequency components is the frequency domain representation of the signal. The fast Fourier Transform (FFT) computes the discrete Fourier Transform (DFT). A DFT decomposes a sequence of values into components of different frequencies.

Opamp parameters

The Opamp is one of the most widely used devices in electronic instrumentation and analog integrated circuits design. There are many parameters to be considered for a simple Opamp. In this lab, only a few parameters are briefly discussed and studied. The information about the parameters below can be found in the data sheet.

Power Supplies: The most frequently used supplies are: ±15 V, ±12 V, ±10 V and ±5 V. In all our labs we will use ±7 V supplies for all the op amp circuits. Never exceed the specified power supply limit.

Input Resistance and Output Resistance: The input resistance looking into the two input terminals of the Opamp is ideally infinite. For a real 741 Opamp, it is about 2 MΩ. The finite input resistance of the Opamp must be taken into account, but it is especially critical if the impedances of the components attached to the Opamp inputs are comparable with its input impedance. The output resistance on the other hand is ideally zero. For a real 741 Opamp, it is about 75 Ω. The finite output resistance of the Opamp must be taken into account in analysis and design of networks if it is comparable with the resistance of components directly connected to the output of the Opamp.

Output Offset Voltage and Input Offset Voltage: When the Opamp input signal is zero, the output should be zero. However, in practice, it is not the case. For a real 741, the output voltage is typically around 2 mV when the inputs are connected to the analog ground (grounded inputs). This offset is called the output offset voltage. This voltage is divided by the open-loop gain of Opamp to get the equivalent input offset voltage.

Input Offset Current: The ideal Opamp has an infinite input resistance and draws no current from the inputs. In the real 741, each input draws a small amount of DC current because of the finite input resistance. The difference between the current drawn into the positive and negative input terminal is called the input offset current.

Open Loop Voltage Gain: The open loop voltage gain is the Opamp's gain when an input signal is applied and feedback is not used. The gain is ideally infinite, but in a real case it is finite; for the 741 the DC gain is around 200,000 V/V (around 106 dB). The gain also depends on frequency and other parameters.

Gain Bandwidth Product: The open loop gain of the Opamp depends on the frequency. It decreases as the frequency increases. So, the Opamp is less efficient at high frequencies. However, the product of open loop DC gain and the -3 dB frequency (bandwidth) is a constant. This is defined as the Gain-Bandwidth product GBW. For a real 741, GBW is about 1.2 MHz.

Slew Rate: An ideal Opamp is able to follow the input signal no matter how quickly the input changes because the Opamp has an infinite frequency response. In a real 741, the output rise and fall transients cannot exceed a maximum slope; the maximum rate of change of the output voltage as a function of time is called the slew rate. Applying signals with transients that exceed this limit results in distorted output signals. The slew rate can be measured by applying a large square waveform at the input. The frequency of the input signal should be increased until the output becomes a triangular waveform. The slope of the triangular waveform is the slew rate.

Handling Opamps: Picking up an IC package by your hand could destroy the circuit inside due to the static voltage discharge. Always wear a ground-strap so that static voltage does not accumulate.

Pre-laboratory exercise

1. Read the data sheet for 741 Opamp and write down the typical values of the following parameters:
   - Supply Voltage
   - Power Consumption
   - Input Resistance
   - Input Offset Voltage
   - Output Resistance
   - Input Offset Current
   - Voltage Gain
   - Bandwidth
   - Slew Rate
2. For the circuit in Fig. 1, derive the voltage gain expression at low frequencies (DC gain) assuming the Opamp is ideal.

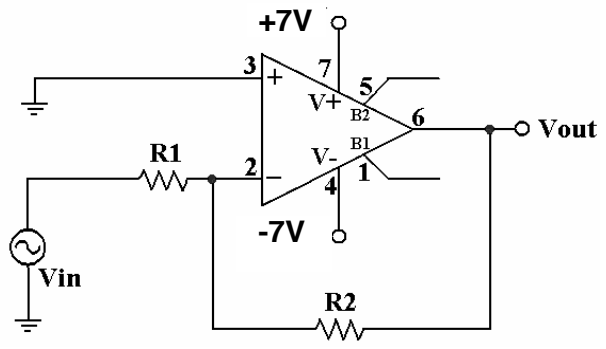


Fig. 1. Inverting Amplifier Configuration

3. Choose R_2 for a gain of –5 if R_1 = 10 kΩ. Use the uA741 PSpice Opamp model to verify your result using a DC source of 1 V.
4. For the circuit shown in Fig. 2, derive the equation for the voltage gain at low frequencies (DC gain) assuming that the Opamp is ideal.

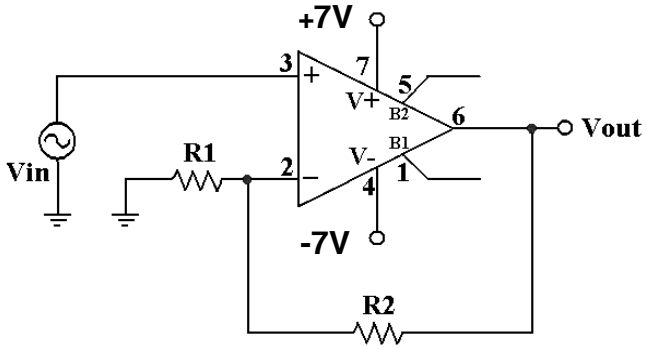


Fig. 2. Non-inverting Amplifier Configuration

5. Choose R_2 for a gain of 5 if R_1 = 10 kΩ. Use PSpice to verify your result.
6. What's the voltage DC gain of the circuit shown in Fig. 3? Verify your answer using PSpice.

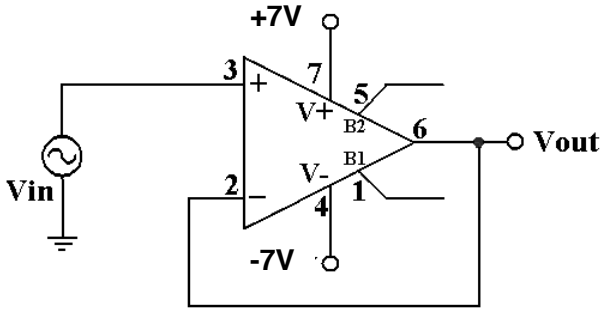


Fig. 3. Voltage Follower Configuration

Lab Measurement:

Part A. Input Offset Current Measurement.

1. Connect the circuit in Fig. 4 and use the dual power supply ±7 V. Measure the resistor values accurately before you connect them. Measure the voltages across the two 250 kΩ resistors. Connect the Opamp output to ground.

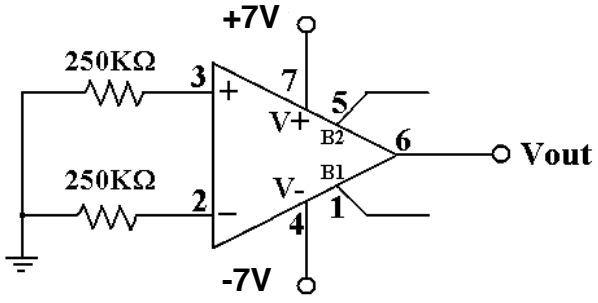


Fig. 4. Offset Current Measurement Configuration

2. Use Ohm's law to calculate the DC input currents. The difference between the current into positive and negative input terminals is the input offset current.

Part B. DC Offset Voltage Measurement.

1. Turn the power supplies off. Connect the circuit as shown in Fig. 5 with the values of R_1 and R_2 you calculated in the pre lab for Fig. 2. Then make sure that you have powered the chip with the dual power supply. For this measurement, the non-inverting input of the Opamp is grounded. Use the Digital Multimeter to measure the output voltage. This is the output offset voltage.

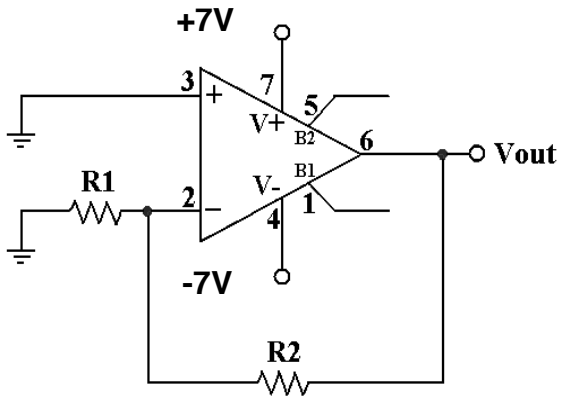


Fig. 5. Offset Voltage Measurement Configuration

2. The input offset voltage of the Opamp can be calculated by dividing the output offset voltage by the circuit's gain, which is $1+R_2/R_1$ for the circuit shown in Fig. 5.
3. To minimize the offset voltage, turn off the power supply first and connect a 20 kΩ potentiometer (pot) to pins 1 and 5 as shown in Fig. 6. Be sure to connect the center tap of the pot to the –7 V supply. Turn on the power supply and use the pot to zero the Opamp's output. This is how offset voltage is compensated.

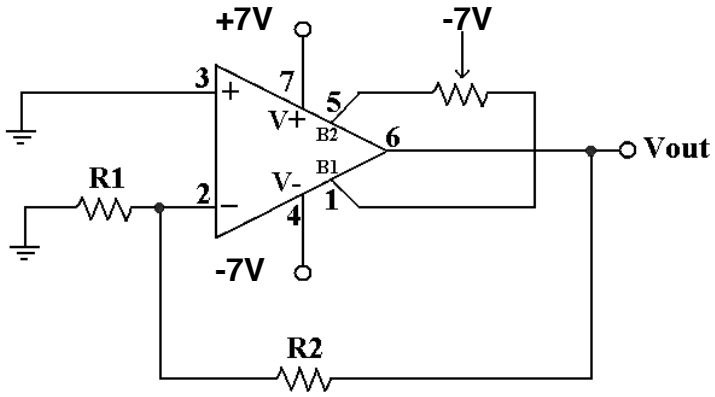


Fig. 6. Elimination of offset voltage

Part C. Inverting Amplifier

1. Retain the potentiometer setting and do not change the connections to Pins 1, 5, and 7. Connect the circuit as shown in Fig. 1 using the component values that were calculated in the pre lab. Turn off the power supply. Apply a 1 Vpp 1 kHz sine wave to the Opamp inverting terminal through R_1 as shown Fig. 1. Display the input and output on the oscilloscope. Note that you need to verify the peak-to-peak voltage using the oscilloscope. Measure V_{out} and compute the closed loop gain. While measuring the output signal on the scope, make sure that the output signal is displayed completely (not clipped).

2. Increase the input signal by small increments up to 3 Vpp. Measure and record the maximum value of the input amplitude before distortion occurs at the output. Obtain a screenshot of the distorted output waveform.
3. With the input at 2.5 Vpp, perform a distortion analysis by activating the mathematical function and selecting the FFT screen analysis. The FFT analysis can be activated using the "Math Menu" button on the oscilloscope. Adjust the base-time to have 0.5 kHz per division and 10 dB/division in the Y-axis. Measure the difference between the fundamental component at 1 kHz and the ones at 2 kHz and 3 kHz.
4. With the input at 2 Vpp, connect the input to channel 1 of the oscilloscope and the output to channel 2. Switch the oscilloscope to XY mode. XY mode is in Diplay -> Format. Use DC coupling to both channels and adjust the volts/divisions knobs to display the transfer characteristic V_{out} vs. V_{in}. Be sure that the upper and lower limits of V_{out} are displayed on the screen. Disconnect the external trigger input fed from the function generator to the oscilloscope to obtain the transfer characteristic. To show the upper and lower limits, increase the input voltage until the Opamp saturates. Measure and record the precise voltage values of the upper and lower limits. Explain your results.
5. The slope of the line around 0 V input is the small signal gain of the inverting amplifier. Take two points on the line to find y_2, y_1, x_2 and x_1, then compute the voltage gain as $(y_2-y_1)/(x_2-x_1)$.

Part D. Inverting Amplifier Distortion analysis using NI Elvis Dynamic Signal Analyzer SFP.

In this section we will use the NI Elvis dynamic signal analyzer SFP to perform distortion analysis for the Opamp inverting amplifier shown in Fig. 1.

1. First ensure that the power supply to the Elvis prototype board has been switched off.
2. Connect the circuit shown in Fig. 1. Do not change the potentiometer setting.
3. Connect the output of the amplifier (Vout in Fig. 1.) to AI0+ on the prototype board.
4. Connect the ground signal to AI0- on the NI Elvis prototype board. The output of the amplifier should be connected to any one of the NI Elvis Analog Channels. We have picked Analog Channel 0 (*AI0+/AI0-)* in this exercise.
5. The input of the amplifier should be connected to the function generator on the bench (as in Part C) not the NI Elvis FUNC_OUT output. Connect the Elvis ground (pin 53) to circuit ground.
6. Turn on the ±7 V the supplies to the Opamp.
7. Apply a 1 Vpp 1 kHz signal from the function generator.
8. Go the program menu on your computer and launch the NI Elvis program. Once the NI Elvis software Elvis interface appears on your screen, Click on the Dynamic Signal Analyzer (DSA) button to launch the DSA SFP.

9. On the Dynamic Signal Analyzer SFP, we can make the following changes to the settings:

    - Select AI0 as the source channel.
    - Select Voltage Range to be ± 10 V.
    - Since the input frequency is 1 kHz, we select 5000 Hz as frequency span (to observe at least 5 harmonic tones).
    - Increase the resolution to 3200. Higher the resolution yields better accuracy.
    - Set scale to Auto.
    - Turn the Markers ON and position the markers at the desired frequency tones. Use the left mouse button to grab and move the markers. Alternatively, you can use the marker position button controls.

After completing these steps, the output should appear as shown in Fig. 7.

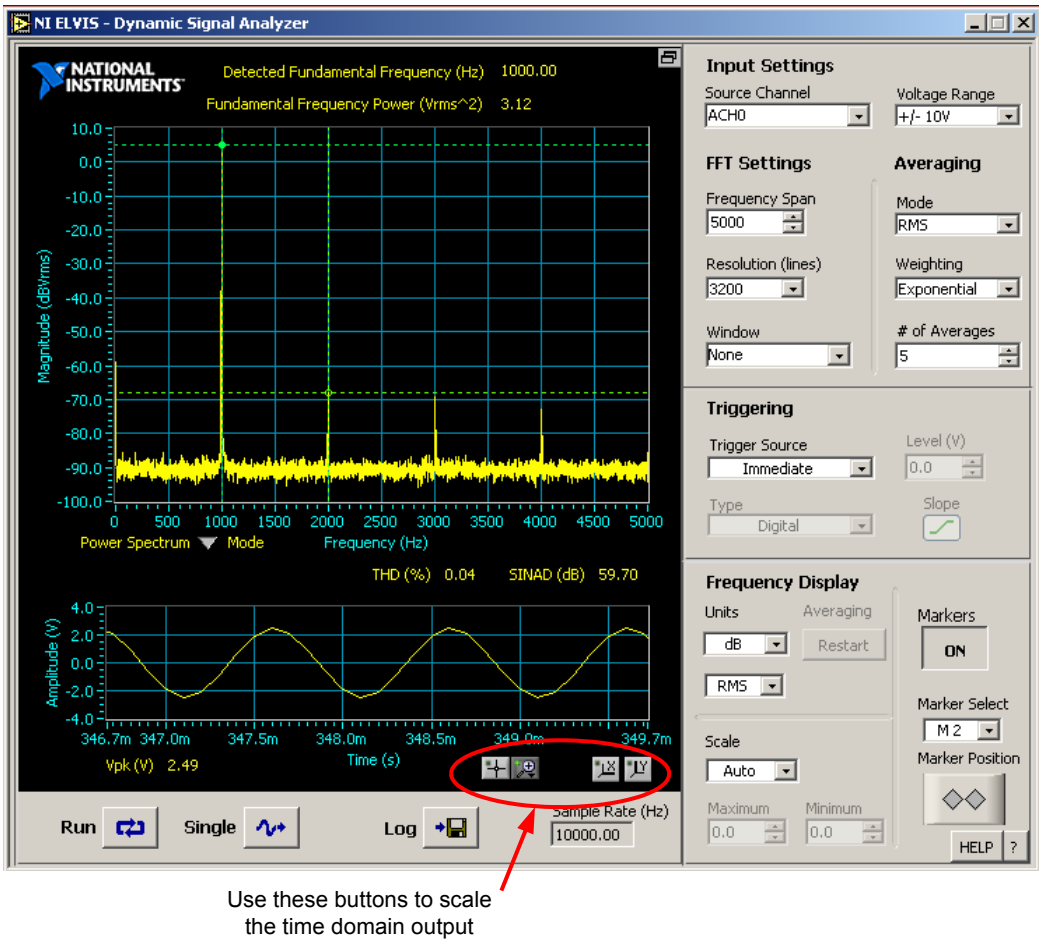


Fig 7. NI Elvis Dynamic Signal Analyzer output for inverting amplifier (Gain 5 V/V) output with 1 V pp input.

10. As shown Fig. 7,
    - The output voltage (Vout) on channels AI0+/AI0- is 2.5 V peak. This is as expected since the inverting amplifier has a gain of 5 V/V with an input of 1 V pp.
    - The frequency spectrum of the output signal is also shown in the above figure. The spectrum shows output signal amplitude in dBVrms scale at 1 kHz, 2 kHz, and 3 kHz with decreasing values.
    - The dBVrms (RMS value in decibels) for a given voltage Vrms can be calculated as: 20 log10(Vrms). Inverting amplifier produces an output of 2.5 Vpeak. This corresponds to an RMS value of 2.5* 0.7 which is around 1.75 V. This value in dBVrms can be calculated as: 20 log10(1.75) = 4.86 dBVrms. As it can be seen from the plot, output contains a 1 kHz signal with this exact dBVrms value.
    - Tones shown at 2 kHz, 3 kHz and 4 kHz have considerably smaller dBVrms values. The Signal-to-Noise-And-Distortion (SINAD) is also indicated on the plot as around 59.7 dB.

11. Increase the input signal amplitude up to 3 Vpp to obtain the distortion measurements and screen shots from the Dynamic signal analyzer.
12. Remember that the op amp is powered by supplies at ±7 V. So, the output would saturate at values below 14 Vpp. You can calculate the input signal level for such outputs and observe the distortion performance around that input amplitude.
13. More details regarding NI Elvis DSA FFT settings can be obtained using the Help Button shown on the screen in Fig. 7.

Part E. Non-inverting Amplifier

1. Keep the connection between pin 1 and pin 5 untouched and connect the circuit shown in Fig. 2. Use the values of R_1 and R_2 you calculated in the pre lab. Do not change the potentiometer setting.
2. Use a 1 Vpp 1 kHz sine wave for your input.
3. Repeat steps 2 through 6 of Part C.
4. Repeat the steps outlined in Part D to obtain the distortion performance of the non-inverting amplifier.

Lab Report:

1. Tabulate all of the parameters measured in the lab. Look up the same parameters on a data sheet for the 741 Opamp. Calculate and list the differences between your measurement and specified values given by the manufacturer.
2. Provide the plots that you obtained in Parts C, D and E. Discuss the data in each measurement.
3. For parts C and E, compare the following four items: (1) PSpice simulated gain, (2) the theoretical gain, using the measured value of resistors, (3) the ratio of v_{out}/v_{in}, using the waveform amplitudes and (4) the slope of the transfer characteristic.
4. Discuss the results of distortion measurements from sections D and E.
5. Explain how using the pot can null the offset voltage (Bonus).
6. Is it possible to get a gain of less than unity using a non-inverting amplifier configuration? If yes, sketch a circuit. You may use PSpice to verify your design.
7. Conclusion.

Lab 4: Operational Amplifier-Part II

Objectives:

The purpose of the lab is to study some of the advanced Opamp configurations commonly found in practical applications. The circuits studied will include the summing amplifier, the differential amplifier and the instrumentation amplifier.

List of Equipment required:

a. Protoboard
b. Capacitors
c. Resistors
d. Oscilloscope
e. Function generator
f. Digital Multimeter
g. 741 Operation amplifiers

Introduction

Summing Amplifier: An inverting amplifier can be modified to accommodate multiple input signals as shown in Fig. 1. Since the circuit is linear, the output voltage can easily be found by applying the superposition principle: the output voltage is a weighted sum of the two input signals. The weighting factor is determined by applying one of the input signals while the other is grounded and analyzing the resulting circuit. Since the circuit is linear, the analysis is repeated for the other input, and the final result is the addition of both signals. The advantage of this approach is that we can easily recognize the effect of each signal on the circuit's performance, and the overall output can be obtained in most of the cases by inspection. For the circuit shown below, the following equation results:

$$V_{out} = -\left(\frac{R_3}{R_1}V_{in1} + \frac{R_3}{R_2}V_{in2}\right)$$

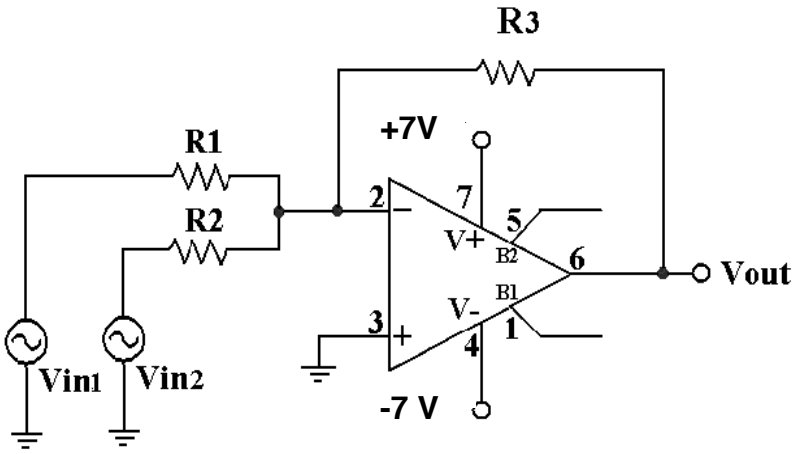


Fig 1. Summing amplifier circuit

The summing amplifier can be extended to have any number of input signals. Consider that a two bit digital signal is applied to the input in the above circuit. A analog voltage appears at the output that is determined by the binary input. So a more general configuration based on this circuit can be used to build digital-to-analog converters (DAC).

Differential amplifier: The differential amplifier is designed to amplify the difference of the two inputs. The simplest configuration is shown in Fig. 2.

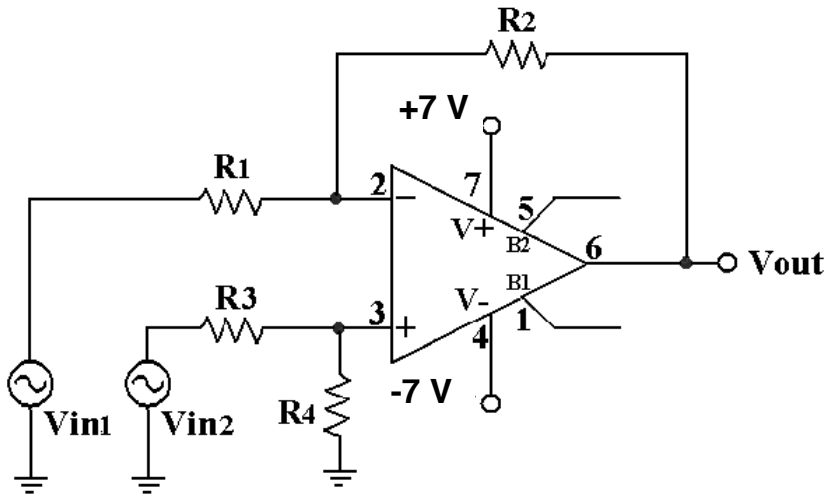


Fig 2. Differential amplifier circuit

If the resistor values are chosen such that $R_2 / R_1 = R_4 / R_3$, then the output of the amplifier is given by:

$$V_{out} = \frac{R_2}{R_1}\left(V_{in2} - V_{in1}\right)$$

This expression shows that the amplifier amplifies the difference between the two input signals v_{in1}-v_{in2} and rejects the common mode input signals; $v_{out}=0$ if $v_{in1}=v_{in2}$. Therefore, the differential amplifier is used in very noisy environment to reject common noise that appears at both inputs. When the same signal is applied to both inputs, the voltage gain in this case is denoted as common-mode gain A_{CM}; for the case of the ideal differential amplifier $A_{CM}=0$. The common-mode rejection ratio is defined as,

$$CMRR = \frac{A_{DM}\left(\text{differential - mode gain}\right)}{A_{CM}\left(\text{common - mode gain}\right)}$$

Substituting common-mode gain equal zero in the above expression, the common-mode rejection ratio is given by

$$CMRR \to \infty$$

In practice, resistors have a tolerance of typically 5%, and the common-mode gain will not be zero, and the CMRR will not be infinite.

Instrumentation amplifier: The instrumentation amplifier is a differential amplifier that has high input impedance and the capability of gain adjustment through the variation of a single resistor. A commonly used instrumentation amplifier is shown in Fig. 3.

The voltage drop across R_{gain} equals the voltage difference of the two input signals. Therefore, the current through R_{gain} caused by the voltage drop must flow through the two "R" resistors above and below R_{gain}. It has been shown in class that the output is given by

$$V_{out} = (V_2 - V_1)\left(1 + \frac{2R}{R_{gain}}\right)$$

Though this configuration looks cumbersome to build a differential amplifier, the circuit has several properties that make it very attractive. It presents high input impedance at both terminals because the inputs connect into noninverting terminals. Also a single resistor R_{gain} can be used to adjust the voltage gain.

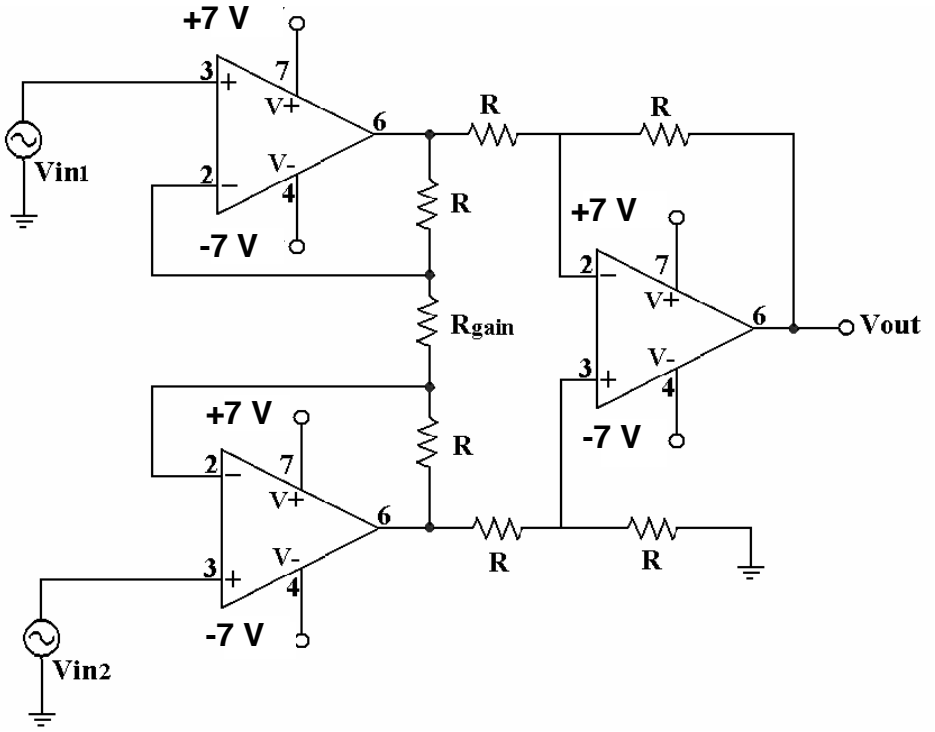


Fig. 3. Typical instrumentation amplifier circuit

Pre-laboratory exercise

1. For the summing amplifier in Fig. 1 with power supplies ±7 V, choose R_2 to have $V_{out} = -(V_{in1} + 2V_{in2})$ if $R_1 = R_3 = 10\,k\Omega$.
2. Use PSpice to verify your hand-calculation and confirm that the circuit operates as a summing amplifier.
3. For the differential amplifier in Fig. 2 with power supplies ±7 V, choose R_1 to have $V_{out} = V_{in2} - V_{in1}$ if $R_2 = R_3 = R_4 = 10\,k\Omega$.
4. Use PSpice to verify your hand-calculations and confirm that the circuit operates as a differential amplifier.
5. Use PSpice to check the common-mode gain and CMRR.
6. For the instrumentation amplifier in Fig. 3 with power supplies ±7 V, choose R to have $V_{out} = 2(V_{in2} - V_{in1})$ if $R_{gain} = 20\,k\Omega$.
7. Use PSpice to verify your hand-calculations and confirm that the circuit operates as an instrumentation amplifier.

Lab Measurement:

Part A. Summing amplifier

1. Connect the circuit in Fig. 1, and use the component values determined in the pre lab. The dual power supply is ±7 V.
2. Apply a 1k Hz, 2 Vpp sine wave to input 1 and a 2 V DC voltage from the power supply for input 2. Make accurate sketches of the input and output waveforms on the same axis in time domain. The oscilloscope's input should be "DC" coupled.

3. Get a hardcopy output from the scope display with input and output waveforms to confirm that the circuit is a summing amplifier.
4. Use the DC offset on your function generator to raise the DC input voltage until clipping at the output is observed. Sketch the waveforms.

Part B. Differential amplifier

1. Connect the circuit in Fig. 2, and use the component values determined in the pre lab. The dual power supply is ±7 V.
2. Apply a 1k Hz, 2 Vpp sine wave to input 1 and a 2 V DC voltage from the power supply for input 2. Make accurate sketches of the input and output waveforms on the same axis in time domain. The oscilloscope's input should be "DC" coupled.
3. Get a hardcopy output from the scope display with input and output waveforms to confirm that the circuit is a differential amplifier.
4. Apply a 1k Hz, 2 Vpp sine wave to input 1 and connect input 2 to ground. Measure $A_D=v_{out}/v_{in}$. Compare your results with the theoretical value using actual measured values for the resistors.
5. Apply a 1k Hz, 2 Vpp sine wave to both inputs. Measure $A_{cm}=v_{out}/v_{in}$. Compare to the theoretical value using actual measured values for the resistors.
6. Compute the common mode rejection ratio CMRR.

Part C. Instrumentation amplifier

1. Connect the circuit in Fig. 3, and use the component values determined in the pre lab. Use the dual power supply of ±7 V.
2. Apply a 1k Hz, 1Vpp sine wave to input 1 and a 1 V DC voltage from the power supply for input 2. Make accurate sketches of the input and output waveforms on the same axis in time domain. The oscilloscope's input should be "DC" coupled.
3. Get a hardcopy output from the scope display with input and output waveforms to confirm that the circuit operates as an instrumentation amplifier where the output voltage is a linear combination of the input waveforms.

Lab Report:

1. Provide the plots you get in Part A, B, and C. Discuss the data in each measurement.
2. For parts A, B and C compare the following three items: (1) PSpice simulated gain, (2) the theoretical gain, using the measured value of resistors, (3) the ratio of v_{out}/v_{in} using the waveform amplitudes.

Lab 5: Operational Amplifier-Part III

Objectives:

The purpose of the lab is to study some of the Opamp configurations commonly found in practical applications and also investigate the non-idealities of the Opamp like finite Gain Bandwidth product and Slew rate limitations. The circuits studied will include an integrator, a differentiator, a non-inverting amplifier and a unity gain buffer.

List of Equipment required:

a. Dual Trace Oscilloscope
b. Function Generator
c. ±7 V DC Power Supply
d. Digital Multimeter
e. A Protoboard
f. Resistors: different values
g. Capacitors: different values
h. Three 741 Operational Amplifiers
i. NI Elvis prototype station and relevant Soft Panel Instruments (SFP).

Introduction

This laboratory deals with several amplifier circuits. Each of the circuits in the lab requires some thinking to understand how the circuit works and its practical limitations.

Integrator: The circuit in Fig. 1 is the lossless inverting integrator. As the name suggests, the circuit generates an output signal that corresponds to the integral of the input signal over time. The circuit can be analyzed using the standard Op-amp analysis techniques mentioned in class.

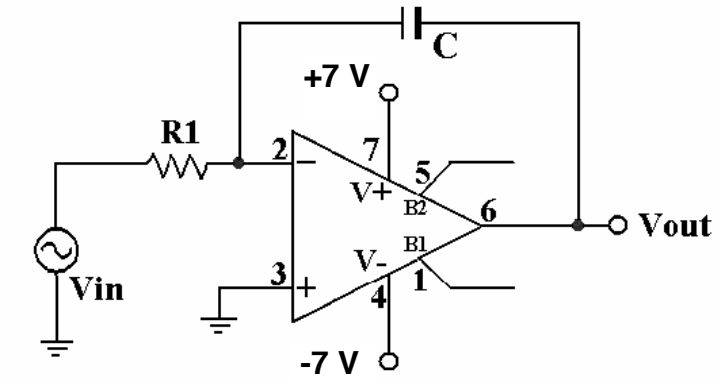


Fig 1. Inverting integrator circuit

In the frequency domain, the output voltage is described as:

$$V_{out} = -\frac{1}{sR_1C}V_{in}$$

The output is directly proportional to the integral (1/s term) of the input signal, and a steadily changing output voltage is produced for a constant amplitude sinusoidal input voltage. Notice that the DC gain (s=0) at the output is theoretically infinite; hence any small DC signal at the input will saturate the Opamp output over time. In a real integrator circuit, a large resistor in parallel with the capacitor is required to prevent the capacitor from storing charge due to offset currents and voltages at the input. This configuration is known as "lossy" integrator or a first order low-pass circuit, which is shown in Fig. 2.

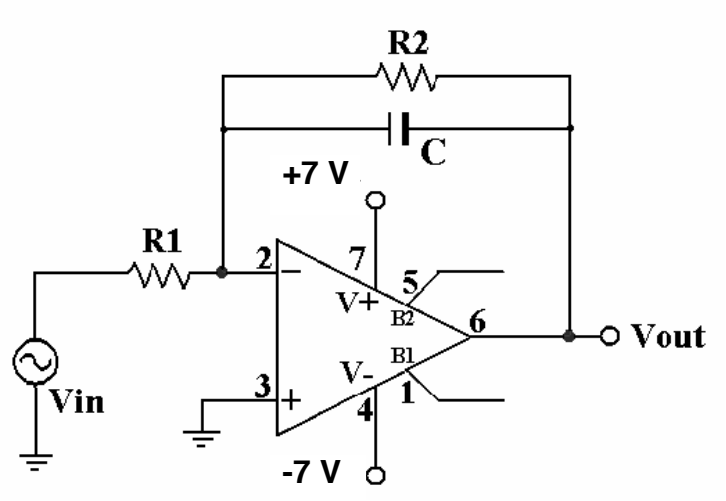


Fig 2. Lossy integrator circuit

The output voltage is now given by the following expression

$$V_{out} = -\frac{R_2 / R_1}{1 + sR_2C} V_{in}$$

The DC gain is now finite and determined by the ratio of the two resistors.

Differentiator: As the counterpart of the integrator, the differentiator differentiates the input signal. This configuration is shown in Fig. 3.

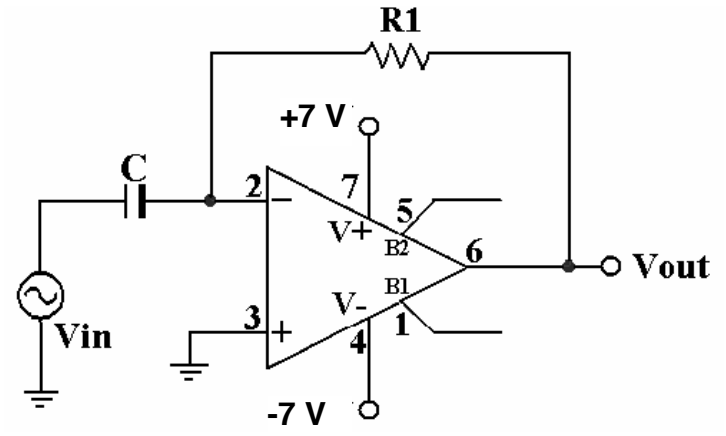


Fig 3. Inverting differentiator circuit

Using the typical linear circuit analysis techniques, the output can be obtained as

$$V_{out} = -sCR_1 V_{in}$$

The output is proportional to the derivative (s term), and the output voltage increases monotonically as the frequency increases. Fig. 4 shows the circuit configuration for a commonly used pseudo-differentiator or high pass filter.

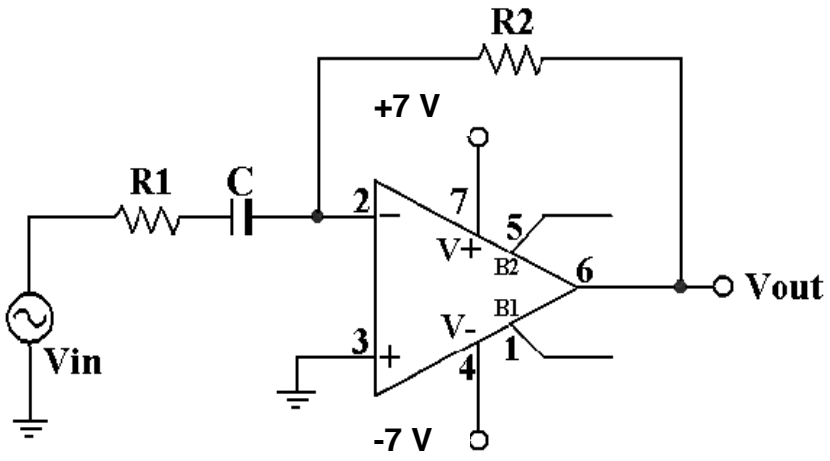


Fig 4. First order high pass filter (pseudo-differentiator) circuit

The output voltage in this case is found as

$$V_{out} = -\left(\frac{R_2}{R_1}\right)\frac{s}{s + \frac{1}{R_1 C}}V_{in}$$

Usually the integrators handle signals "better" than differentiators since important signals for the integrators are located at low-frequencies while differentiators process the high frequency signals. However, due to the limited high frequency capabilities of the devices it is hard to process properly the high frequency signals. In most of the practical systems, integrators are used instead of differentiators.

Non Idealities of the Opamp:

1. Finite Gain Bandwidth (GBW) Product: The open loop gain of the Opamp is frequency dependent, decreases when frequency increases following the roll-off of a single pole system, making it less efficient at high frequencies. However, the product of open loop DC gain and the 3-dB frequency (bandwidth) is a constant, which is defined as the Gain-Bandwidth product GBW. For a real 741, GBW is about 1.2M Hz. Finite GBW of the Opamp limits the bandwidth of closed loop inverting or non-inverting amplifier configurations.

Assuming a finite GBW of w_t, the frequency dependent gain of the non-inverting amplifier shown in Fig. 5 is given by

$$\frac{V_{out}}{V_{in}} = \frac{G_o}{\left(1 + \frac{s}{\omega_o}\right)}$$

where G_o is the DC gain of the amplifier given by $(1+R_2/R_1)$ and ω_o is ω_t/G_o.

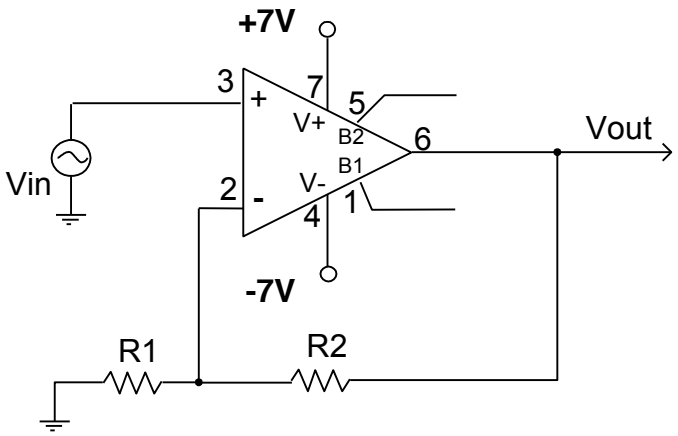


Fig. 5: Non-inverting Amplifier configuration.

2. Slew Rate: An ideal Opamp is capable of following the input signal no matter how fast the input changes because it has an infinite frequency response. In a real 741, the output rise/fall transient cannot exceed a maximum slope; the maximum rate of change of the output voltage as a function of time is called the slew rate. Applying signals with transients that exceed this limit results in distorted output signals. To avoid distortion due to slew rate limitations maximum rate of change of output must be kept less than the slew rate specifications of the Opamp. The slew-rate can be measured by applying a large square waveform at the input. The frequency of the input signal should be increased until the output becomes a triangular waveform. The slope of the triangular waveform is the slew rate.

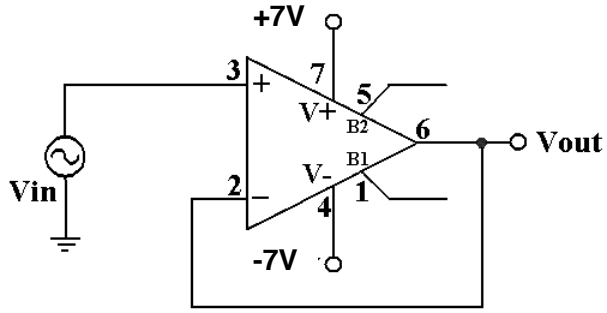


Fig. 6. Unity Gain Buffer Configuration.

Pre-laboratory exercise

1. For the lossy integrator in Fig. 2 with power supplies ±7 V, and assuming the Opamp is ideal, derive the time-domain equation for the output in terms of the input. Show that the circuit performs as an integrator.
2. Choose R_1 to have a low-frequency gain of -20 if $R_2 = 20$ kΩ and C = 0.2 μF.
3. Use PSpice to verify your results and confirm that this circuit is an integrator for $\omega >> 1/R_2C$.
4. For the first order high-pass filter shown in Fig. 4 with power supplies ±7V, and assuming the Opamp is ideal, derive the time-domain equation of the output in terms of the input. Show that the circuit performs the function of a differentiator.
5. Choose R_2 to have a high-frequency gain of -20 if $R_1 = 1$k Ω and C = 33 nF.
6. Use PSpice to verify your results and confirm that this circuit operates as a differentiator for $\omega << 1/R_1C$. Notice that at higher frequencies, the slew-rate limit of the amplifier dominates the circuit performance as the input amplitude increases. Make transient simulations for f = 1k Hz, 10k Hz and 100k Hz. Set the amplitude of the input signal to 0.5 Vpp.

7. Consider a non-inverting amplifier shown in Fig. 5. Assuming R_1 = 1K, find the value of the resistor R_2 to get an amplifier with a DC gain of 61. Verify your design with PSpice AC simulations. What is the simulated 3-dB bandwidth of the amplifier? Repeat the PSpice AC simulations when the value of R_2 is adjusted to obtain a gain of 31 and 91.
8. Simulate the unity gain buffer configuration shown in Fig. 6 with a load of 2k in parallel with 100 pF at the output. Assume a sinusoidal input of 10 Vpp at 15kHz. Obtain the maximum dV_{out}/dt of the output signal and find the frequency at which this Opamp will enter the slew rate conditions.

Lab Measurement:

Part A. Lossy integrator configuration

1. Connect the circuit in Fig. 2, and use the component values determined in the pre lab. The dual power supply is ±7 V.
2. Apply a 1k Hz, 0.3Vpp sinusoid to the input. Make accurate sketches of the input and output waveforms on the same axis in the time domain. The oscilloscope's input should be "AC" coupled.
3. Get a hardcopy output from the scope display with input and output waveforms to confirm that the circuit is an integrator.
4. Vary the frequency of the input from about 10 Hz to 10k Hz. Record the magnitude and phase response at several frequencies. Take three to five points per decade of frequency.
5. Bode plot analyzer can also be used to obtain the frequency response of this integrator circuit. The procedure to be followed is similar to the procedure outlined in lab-2. Make the settings on the Bode Analyzer SFP and follow the steps briefly outlined below (for more details refer to Part C of lab-2 exercise):
   - Input to the integrator circuit should be from FGEN and GROUND ports on the prototype board.
   - Input should also be connected to analog channel 1 between AI1+/AI1- pins.
   - Output from the integrator should be connected to analog channel 0 between AI0+/AI0- pins.
   - On the bode analyzer SFP, set start frequency below the cutoff frequency of the integrator.
   - Set the end frequency at least much higher (3-4 decades) than the cut off frequency.
   - Choose 40 steps per decade.
   - FGEN output peak amplitude should be selected carefully. Remember that the lossy active RC integrator has a large low frequency gain (-20). Since the op amp outputs saturate near the supply rails (±7V), input level has to be kept low enough not to saturate the output to obtain correct results from the bode analyzer.
   - Set the Y scale to Auto.
   - Use the cursors in the SFP to obtain the 3-dB frequency.
6. Use the run button on the SFP to obtain the magnitude and phase response for the integrator.
7. Repeat steps 2 and 3 for a 1 kHz square wave. Explain your results.
8. Now change the input back to sinusoid as in step 2. Remove the resistor R2. What happened to the output signal? Explain what you observe on the oscilloscope.

Part B. First order high-pass filter

1. Connect the circuit in Fig. 4, and use the component values determined in the pre lab. The dual power supply is ±7V.
2. Apply a 1 kHz, 0.3 Vpp sinusoidal signal at the input. Make accurate sketches of the input and output waveforms on the same axis in time domain. The oscilloscope's input should be "AC" coupled.
3. Get a hardcopy output from the scope display with input and output waveforms to confirm that the circuit is a differentiator.
4. Vary the frequency of the input from about 100 Hz to 20 kHz. Record the magnitude and phase response at several frequencies. Take three to five points per decade of frequency.
5. Use the bode analyzer (as outlined in Part A) to obtain the magnitude and phase response for the high pass filter.
6. Repeat step 2 and 3 for a 0.5 Vpp, 1 kHz triangular wave.

Part C. Finite Gain Bandwidth Limitations in Opamps

1. The non-inverting amplifier designed in the pre lab (as shown in Fig. 5) will be used to understand the finite GBW limitation of the Opamps. Since the gain of the non-inverting amplifier is very large (around 61 or 35 dB), very small DC offsets in the amplifier will produce large DC output offset voltage. Hence we will use offset calibration scheme (used earlier in Lab 3, Fig. 6) to calibrate the Opamp offsets. So, connect the circuit as shown in Fig. 7.
2. You would also notice that we have used AC coupling from the NI Elvis signal source to the Opamp input in Fig. 7. This eliminates the DC offsets coming from the signal source and only the AC voltage swing generated by the signal generator (from Elvis) will be applied to the Opamp input terminal. The ac coupling circuit behaves like a high pass circuit with a corner frequency of around 1.6 Hz and will be transparent for higher frequency (> 1.6 Hz) operation. The potentiometer (**20k**) as shown in Fig. 7 between terminals 1 and 5 is for offset calibration. Make sure the viper of the potentiometer is connected to -7V supply. We will use this potentiometer to trim the offsets coming from the Opamp.

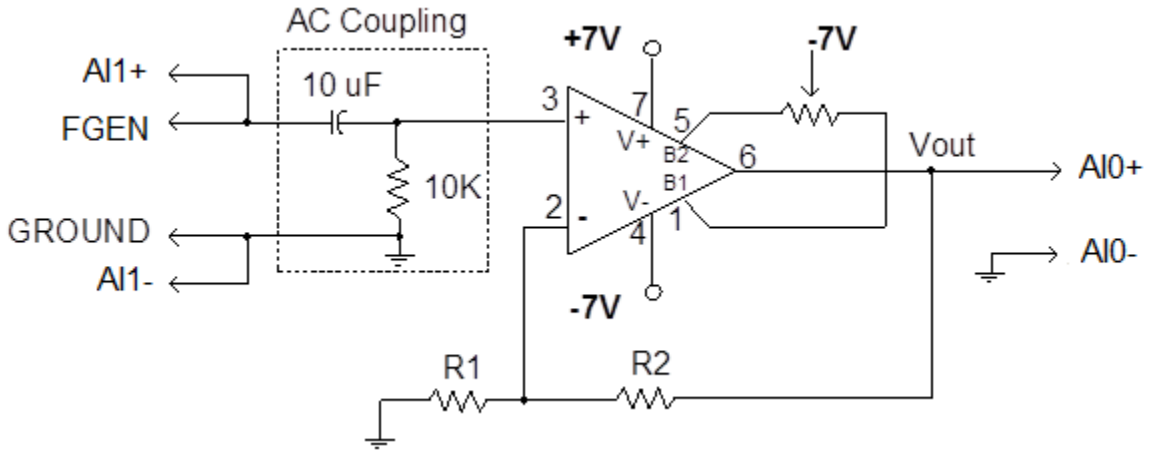


Fig. 7. Non inverting amplifier with AC coupled input and offset compensation resistor

3. Connect the inputs of the circuit to function generator (FGEN/GROUND) and to Elvis channel AI1+/AI1- as shown. Connect the output of the amplifier to Elvis channel AI0+/AI0-.
4. Use the function generator SFP from NI Elvis to generate a 1 KHz sine wave with peak amplitude equal to 100 mV and zero DC offset.
5. Use the oscilloscope SFP from Elvis to observe both the input and the output on channels AI1 and AI0 respectively. Now adjust the 20k potentiometer to balance the output waveform to be around 0 V as close as possible. As the 20k potentiometer is adjusted the waveform on Channel B should move to be as close as possible to being symmetric around zero DC voltage. This is shown in Fig. 8. Now we have calibrated the DC offsets of the Opamp.

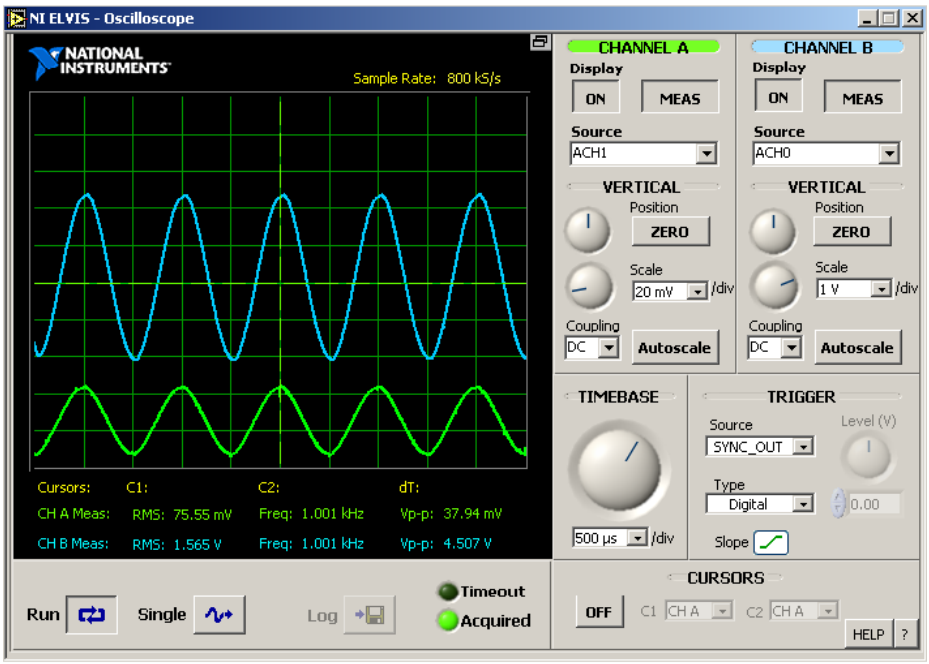


Fig. 8. Oscilloscope output with output on AI0+/AI0- trimmed to have close to zero DC offset.

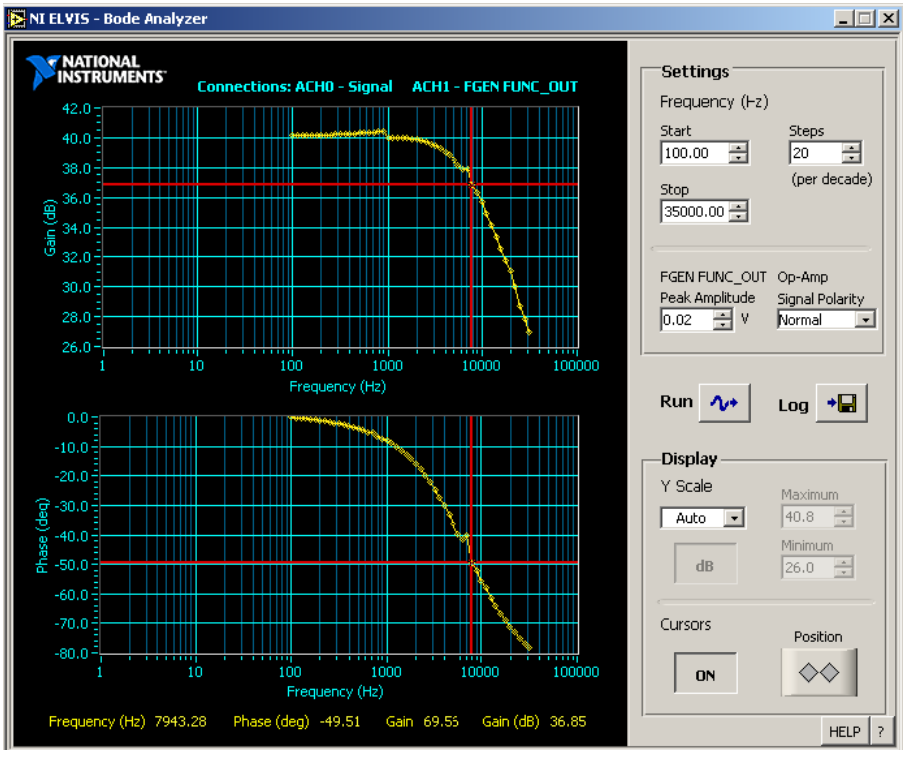


Fig. 9. Bode Analyzer output showing amplifiers low frequency gain and finite bandwidth.

6. Keep the same setup and use the bode analyzer SFP to obtain the frequency response of the amplifier. Choose the following settings on the bode analyzer SFP:
   - Start frequency to 100 Hz and stop frequency to 200 kHz.

- Peak input amplitude of 100 mV.
- Steps to 40 per decade.
- Display section, set Y-scale to Auto.
- Click on RUN.

7. Output should appear as shown in Fig. 9. From this analysis note the 3-dB bandwidth of the amplifier.
8. Keep the 20 k potentiometer position unchanged and repeat bode analysis by replacing the feedback resistor values for gains of 31 and 91. Obtain the bode plots for the amplifier frequency response in these plots.

Part D. Slew Rate Limitations in Opamps

1. Keep the offset calibration potentiometer connection between pins 1 and 5 unchanged.
2. Remove the AC coupling C-R network at the input terminals.
3. Reconnect the circuit as a unity gain buffer as shown in Fig. 6. At the output node, connect a load resistor of 2k in parallel with 100 pF capacitor.
4. Apply a 1k Hz, 10 Vpp square wave. Make sure the function generator is set to Hi-Z state. Display the output on the oscilloscope. Gradually increase the frequency and observe output response. Eventually the output waveform becomes triangular. Measure and record the slope of the output; that value is the Opamp slew rate for that load.
5. Apply a 1k Hz, 10 Vpp sine wave. Again, make sure the function generator is in Hi-Z state. Display the output on the oscilloscope. Gradually increase the frequency and observe the output. Eventually the sine wave output turns into a triangular wave which indicates the slew rate distortion produced by the voltage follower. Find the frequency beyond which the output is distorted by slew rate limitation of the Opamp.

Lab Report:

1. Provide the plots you get in Part A, B, C and D. Discuss the data in each measurement.
2. For part A, with the experimental observation, explain the function of the resistor R_2.
3. For parts A and B, plot the magnitude responses and compare it with the plots generated by using PSpice.
4. For part C, compare the Gain Bandwidth product obtained from the data sheet with the PSpice simulations and lab measurements.
5. For part D, compare the Slew Rate performance obtained from the data sheet with the PSpice simulations and lab measurements.
6. Provide conclusions.

Lab 6: Introduction to Diodes

Objectives:

The purpose of this laboratory exercise is to investigate the basic properties and characteristics of semi-conductor diodes. I-V characteristics, switching characteristics, and rectification properties are examined, leading to the construction of a practical DC power supply.

List of Components and Equipment

a. Dual Trace Oscilloscope
b. Function Generator
c. Digital Multimeter
d. Two Independent DC Power Supplies
e. 1N4006/1N4148 Si Diodes
f. 1N34A/60 Germanium Diode
g. Resistors: 10 Ω, 100 Ω, 500 Ω, 1 kΩ and 10 kΩ
h. Capacitors: 10 μF (50 volt), 100 μF (50 volt)
i. Protoboard

Introduction

The objective of this laboratory exercise is to gain familiarity with the characteristics of semiconductor diodes. The diode functions as a rectifier, allowing current to flow in one direction only, similar to a one-way water valve. A semiconductor diode consists of a junction formed by contact between p-type and n-type semiconductor material. The terminal connected to the p-type material is called the anode, and the terminal connected to the n-type is called the cathode. On most diodes, the cathode is marked by a band on the body of the device. See Fig. 1.

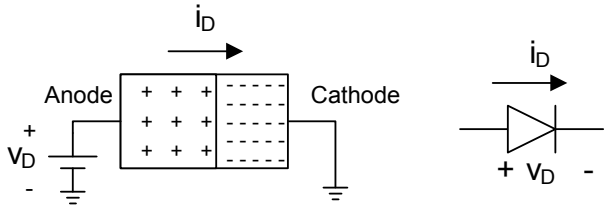


Fig. 1. Semiconductor Diode

When the anode is at a higher voltage than the cathode, the diode is forward biased, and current will flow through the diode from the anode to the cathode. When the anode is at a lower voltage than the cathode, the diode is reverse biased, and very little current will flow. The current flowing through the diode can be expressed as

$$i_D = I_s \cdot \left(\exp\left(\frac{v_D}{nV_T} \right) - 1 \right) \cong I_s \exp\left(\frac{v_D}{nV_T} \right)$$

where i_D and v_D are the current through the diode and voltage drop across the diode respectively, as shown in Fig 1, V_T is the thermal voltage which is around 26 mV at room temperature, I_s is the saturation diffusion current which is a constant dependent on the diode's geometry and material, and n is a fitting constant between 1 and 2 (for our study we will always use n = 1 for simplicity, unless specified otherwise).

The diode's characteristics will be measured in this lab. The experiment will then go through a sequence of steps that will lead to the construction of a practical DC power supply. Such a supply is important since most of the active devices used in electronic circuits require a source of DC power. Although this could be supplied by batteries, it is often more convenient to obtain power from the AC line (house current, 60 Hz, 115 V_{RMS}). The conversion of AC to the required DC voltage is done by a power supply (Fig. 2).

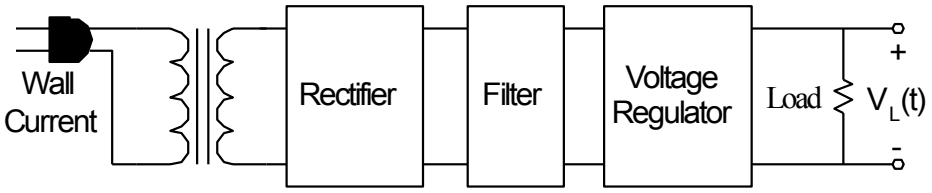
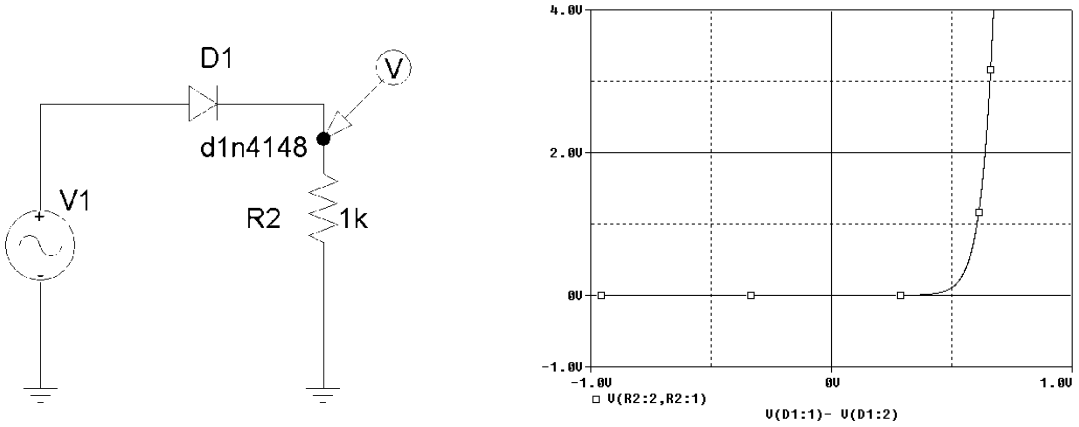


Fig 2.Block diagram of a typical DC power supply

The AC voltage is first passed through a transformer to step it down to a lower voltage, then rectified using diodes. The resulting DC voltage is pulsating and hence is then filtered to remove or reduce the ripple component, producing a constant DC voltage. Additional circuitry may be added to provide voltage regulation so that the desired voltage is maintained, independent of the load current drawn.

Diode I-V Characteristics: to examine the I-V characteristics of a diode one can setup a test circuit like that shown in Fig 3(a). Measure the voltage drop across the diode (V_D) and across the resistor (RI_D) for different values of V1 (note carefully the polarities of the measured voltage drops, and the current now being scaled up by the resistor value). The resulting measurement points should lie on the line shown in Fig 3(b), which clearly shows the exponential relationship previously given for the diode current.



(a) (b)

Fig 3. (a) Diode Test Circuit for I-V Characteristic in PSpice and (b) Resulting Waveform

Full Wave Bridge Rectifier: The circuit shown in Fig. 4 is a full wave rectifier. As discussed in class, the resistor shown in the circuit conducts current during both the positive and negative cycles of the sinusoidal input. Note that the peak voltage drop across the resistor is $Vm - 2V_D$, where Vm is the maximum amplitude of the sinusoidal input and V_D is the voltage drop across the diode.

To build the circuit shown in Fig. 4, the trigger from the function generator to the oscilloscope must be disconnected. Also, DC couple the output to the oscilloscope to see the rectified output average and peak-peak values.

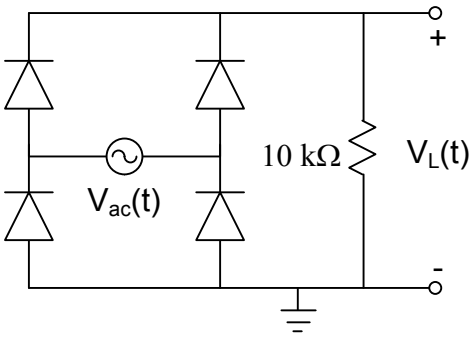


Fig 4. Full Wave Bridge Rectifier

DC Power Supply: In class experiment you observed the rectification property diodes. Fig. 5 shows how the half wave rectifier circuit may be modified by the addition of a single-capacitor filter. Analysis of the circuit indicates that when the diode is conducting, the capacitor will charge up to approximately the source peak voltage. When the diode shuts off, current from the now discharging capacitor will continue to supply the load so that the load voltage will be maintained somewhat until the next charging cycle.

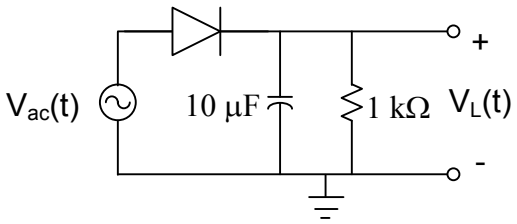


Fig 5. Unregulated DC Power Supply

The change in DC (average) load voltage as the load current varies is measured in terms of the quantity called voltage regulation, defined as:

$$Percent\ \text{Re}gulation = \frac{V_{noload} - V_{full-load}}{V_{full-load}} \times 100$$

A good power supply should have a low percent regulation, indicating that the voltage seen by the load is fairly independent of the current drawn by that load. For the circuit in Fig. 5, the full load situation corresponds to the current drawn when the load resistance is 1 kΩ. The no load condition is an open circuit ($I_{RL} = 0$) for $R_L = \infty$.

Pre-laboratory exercise

1. Using PSpice, set up the circuit shown in Fig 3(a). Perform a DC sweet analysis for the source V1 from -1 to 1 V. To do that, in the menu bar go to Analysis --> Setup --> check DC sweep- -> DC sweep --> choose voltage source as your variable type, and input the source name. Then choose linear sweep and set you start and end values. Use an increment of at most 5mV. Note: since the added source is an AC source, initialize its configurable parameters to 0. Otherwise, you will receive error messages and the simulation will not run.
2. The resulting waveform will have the voltage drop across the resistor on the Y-axis and the swept voltage on the X-axis. To obtain the waveform in Fig 3(b), you will need to modify the parameter for the X-axis. To do so, double click on the X-axis --> Axis Variable. In the trace expression, select the node potential V(D1:1), insert a – sign, then select the node potential V(D1:2) --> OK. Your waveform should now resemble Fig 3(b). Attach the waveform to your pre-lab report. What is the approximate ON voltage of the diode?
3. Modify the source parameters (VAMPL to 5 V, FREQ to 1 k). Perform a Transient analysis. To do so, in the menu bar go to Analysis --> Setup --> check Transient --> Transient --> use a final time of 10 m, and a step

ceiling of at most 10 u. From the resulting waveform, what is the peak voltage across the Resistor and how does it compare to the amplitude of the voltage source? Explain any differences.

4. Repeat the simulation in step 3 with a capacitor in parallel to the resistor, for capacitor values of 1 μF, 10 μF and 100 μF. Attach all resulting waveforms to your pre lab and comment on your results. What is the effect of the capacitor value on the performance?
5. Construct the circuit of Fig 4 in PSpice. Run a transient simulation using a sinusoidal source with 5 V amplitude and 1 kHz frequency. Plot the voltage drop across the resistor and include it in your report. What is the peak voltage drop across the resistor? How does the circuit performance differ from the one in step 3?

Lab Measurement:

Part A – Diode I-V Characteristics

The I-V characteristics of a diode can be displayed directly on the oscilloscope using XY mode and the circuit shown in Fig. 6. The voltage across the resistor is used as the Y input, and the voltage across the diode v_D is used as the X input. Thus a voltage $100*I_D$ will be the vertical axis, and v_D will be the horizontal axis. It must be noted that the voltage units of the vertical scale should be divided by 100 to obtain the diode current in amperes.

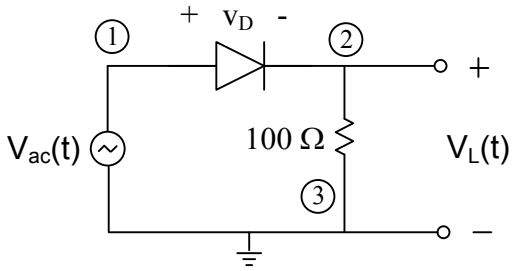


Fig. 6. Circuit for I-V Characteristic Measurement

On most oscilloscopes the X and Y inputs have a common terminal. If this is the case, v_D and v_R cannot be displayed directly as described. However, if the common (ground) terminal of the scope inputs are connected to node 2, the vertical input connected to node 3 and horizontal connected to node 1, the desired characteristics can be obtained by inverting the vertical input voltage (a switch on the oscilloscope). Before using the XY mode, the DC values of the X and Y channels should be aligned to get an accurate I-V curve.

The triangle-wave voltage supply will force the diode to go into the forward and reverse biased states. If the frequency of the source is fast enough we will observe a continuous graph of I_D vs v_D being traced on the scope.

1. Construct the circuit shown in Fig. 6, using the 1N4006 or 1N4148 silicon diode.
2. Obtain a screen shot of the I-V characteristics of the diode. Always start these measurements with the input voltage set to zero, and slowly increase the voltage so that excessive current will not damage the diode. *Also select an input frequency that allows a continuous display of the I-V curve*. The maximum value of the allowable current I_D can be found on the data sheet. For this experiment limit the maximum current to approximately 50 mA.
3. The goal of this step is to plot the I-V characteristics of *both* the 1N4006/1N4148 silicon diode and the 1N34A/60 germanium diode on the same graph. This may be accomplished by executing the following procedures:

- Assemble the circuit in step 2, and obtain a plot of the IV characteristic for the diode.
- On the oscilloscope, press the save key and select the “Save Waveform” option, and select Ref A, B, C, or D.
- Remove the input signal $v_i(t)$ from the circuit. This is for your safety.
- Remove the silicon diode, and replace it with the germanium diode and reapply the input signal.
- On the oscilloscope, press the save key and select the “Save Waveform” option, and select Ref A, B, C, or D.

- The saved data can be viewed by press the Ref. Menu button. Your work should resemble Fig. 7.

Be sure to note the significant features distinguishing the characteristics of the silicon and the germanium diodes, specifically the "turn on" voltage. This measurement can be made with the oscilloscope cursors.

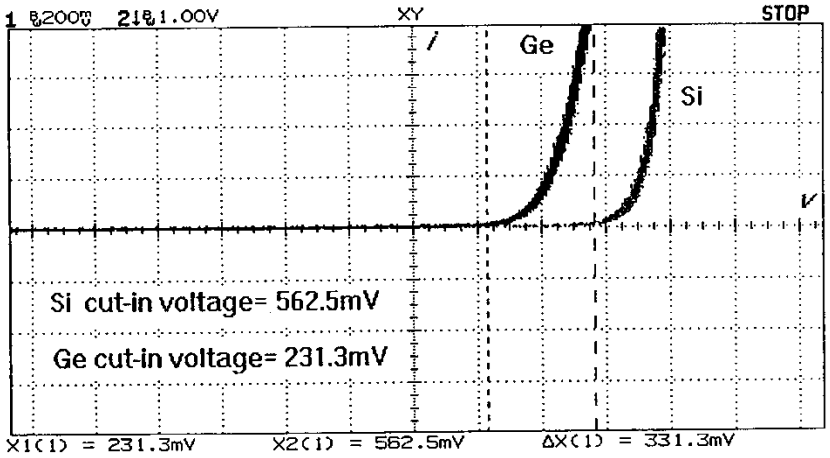


Fig. 7. Graph Illustrating the Differences between the Si and Ge Diodes

Part B – Full Wave Bridge Rectifier

1. Connect the circuit shown in Fig. 4 with a 100 Hz 16 V_{pp} sinusoidal input. Pay careful attention to the polarities of the diodes in the bridge. For this circuit the function generator will need to be isolated from ground because $v_{ac}(t)$ and $v_L(t)$ are referenced to different places. Disconnect the external trigger input fed from the function generator to the oscilloscope. In addition note that $v_{ac}(t)$ and $v_L(t)$ cannot be simultaneously displayed. Be sure the channel measuring v_L is set on the DC coupling with zero DC offset.
2. Observe and obtain oscilloscope plots of $v_{ac}(t)$ and $v_L(t)$, on the same graph. You are expected to follow the procedures for plotting two waveforms as discussed in Part A of this experiment. Be sure to preserve the phase relationship between the two voltages.
3. Find the value of the DC component of the rectified signal (i.e. find the average value of the output.)
4. Find $v_{i,,peak}$ and $v_{o,peak}$.

Part C – DC Power Supply

CAUTION: electrolytic capacitors are polarized. If not oriented correctly (denoted by the +) they will not work, and may explode. .

1. Connect the circuit shown in Fig. 5. Set $v_{ac}(t)$ to 19 V_{pp} at 60 Hz. Observe on the oscilloscope simultaneously the waveforms of $v_{ac}(t)$ and $v_L(t)$ vs time. Be sure that the channel measuring $v_L(t)$ is using the DC coupling. Obtain screen shots of the waveforms. Find the DC component (average value) of $v_L(t)$.
2. The peak-to-peak ripple voltage is the amount of variation from a constant DC value that is present in the load voltage. Ideally, in a good power supply this voltage should be zero. Measure the peak-to-peak ripple voltage of the circuit of Fig. 5. To accurately execute this procedure, bear in mind that the ripple voltage can be considered to be an AC signal. Therefore measure the ripple component using an AC coupling. Since the ripple component is small, you may need to adjust the volts/div on the oscilloscope (i.e. expand the scale). Your work should resemble Fig. 8Obtain a screen shot of the resulting waveform.
3. Replace the 10 μF capacitor with a 100 μF capacitor and repeat steps 1 and 2. Note the change in the load voltage. Also find the DC component of $v_L(t)$ and the peak-to-peak ripple voltage. How does the capacitor value affect the performance?
4. Determine the percent regulation for the circuit of Fig. 5 with C = 100 μF. The DC (or average) load voltage can be measured using the multimeter set on DC volts.

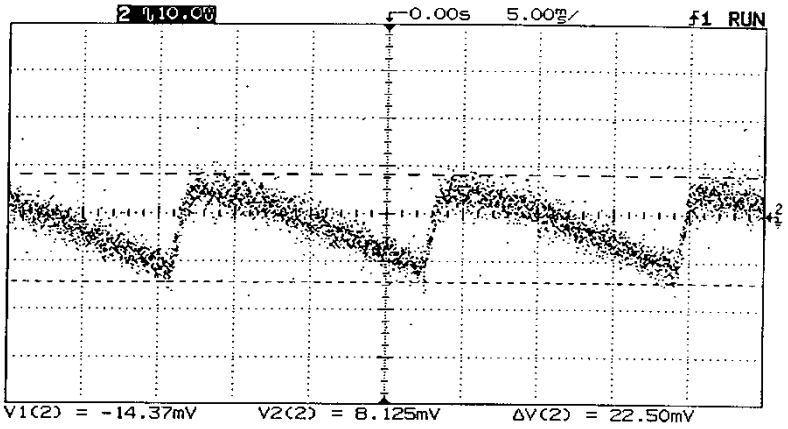


Fig. 8. AC Ripple Component

Lab Report:

1. Attach the oscilloscope plots of the I-V characteristics of the Si diode and the Ge diode obtained in part A. Discuss significant differences.
2. Discuss the constant voltage drop across the diode when it is forward biased, and how it affects the maximum output voltage. Also discuss the voltage swing across the diode as the input goes through its negative half cycle.
3. For the full wave bridge rectifier given in part B, identify which diodes are forward biased when the input goes through its *positive half cycle*, and which diodes are forward biased when the input completes its *negative half cycle*.
4. According to your experimental data, what was the average value of $V_o(t)$ in Part B?
5. Is the current flowing in the load resistor in Fig. 6 *bidirectional* or *unidirectional*?
6. For Part C, compare the ripple voltages of the following: (1) power supply with C = 100 μF, and (2) power supply with C = 10 μF.

Lab 7: Characterization of the BJT

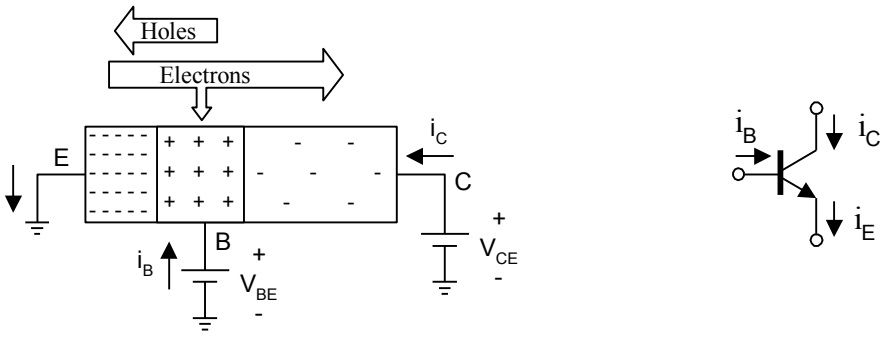
Objectives:

The purpose of the lab is to measure the DC operating point of a single transistor amplifier and extract the most important AC parameters of an NPN bipolar transistor.

List of Components and Equipment

a. Dual Trace Oscilloscope
b. Function Generator
c. Digital Multimeter
d. Frequency counter
e. Dual Power Supply
f. 2N2222 transistor
g. 1 potentiometer of 100 kΩ
h. Resistors
i. Protoboard

The symbol of an NPN-BJT transistor is shown in Fig. 1. Because the relationship between i_C and v_{BE} is exponential, the collector current varies drastically as the base-emitter voltage changes. A small current i_B flows into the base terminal because v_{BE} varies; usually it is a small fraction of the collector current i_C. The ratio of i_C to i_B the current gain of the transistor, and it is called β. The value of β varies significantly with temperature, and it can be different between two transistors of the same type; see textbooks and/or lecture notes.



(a) (b)

Fig. 1. (a) NPN Transistor and (b) its symbol.

The bipolar junction transistor (BJT) has three regions of operation:

1. *Cutoff Region*: If both base-emitter and base-collector junctions are reverse biased, the BJT transistor enters the cutoff region. All terminal currents are extremely small, and the transistor is off.
2. *Active Region*: The base-emitter junction must be forward biased, and the base-collector junction must be reverse biased to make a BJT transistor operate in the active region. The active region is used to design a linear amplifier.
3. *Saturation Region*: When both the base-emitter and collector-base junctions are forward biased, the BJT transistor enters the saturation region.

In this lab, the circuit is designed so that the BJT transistor operates in the Active region. The base-emitter voltage determines the collector current; it is computed as follows

$$I_C = I_S\left(\exp\left(\frac{v_{BE}}{nV_T}\right)-1\right) \tag{1}$$

where I_S is the saturation current for the emitter terminal, V_T is the thermal voltage and n is a fitting parameter whose value is within 1 and 2. At room temperature (300 K), the thermal voltage is roughly 26m V. Another fundamental equation of the bipolar device is

$$i_E = i_C + i_B \tag{2}$$

A very useful parameter is the collector-base DC forward current gain defined as follows

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \tag{3}$$

Where $\alpha = I_C/I_E$.

The AC forward current gain is accordingly defined as

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} \tag{4}$$

for a constant value of $V_{CE} > V_{CESAT}$.

Unless otherwise specified, β will stand for β_{DC} for our lab purposes.

DC Characteristics of the BJT: The transistor's I_C-V_{BE} curve is obtained by sweeping the base-emitter voltage; this plot is known as the DC input characteristics of the bipolar transistor. If the base-emitter junction is forward biased then the collector current is determined by (1), as depicted in the following figure.

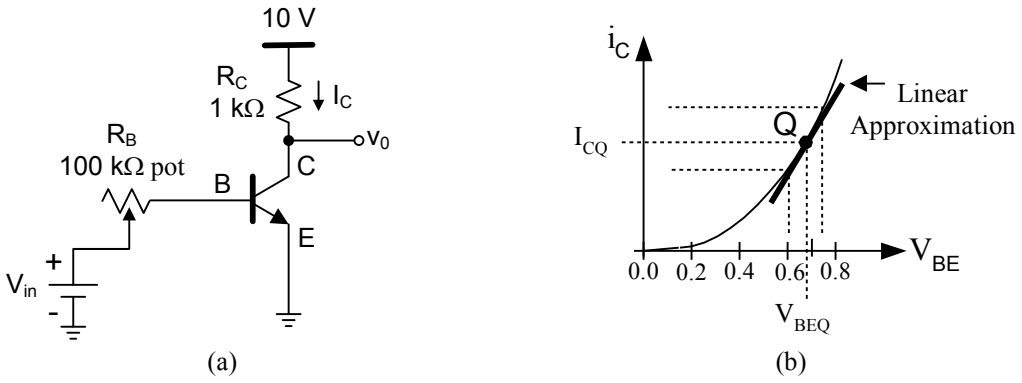


Fig. 2. (a) BJT transistor circuit 1 and (b) input characteristics for the BJT if $V_{CE}>V_{CESAT}$

For base-emitter voltages below 0.5 V, the collector current is very small, typically less than 1 μA. It will be evident in the next sections that the BJT is often operated with larger collector currents and base-emitter voltages; e.g. $V_{BE} >$ 0.5 V. When a base-emitter voltage is selected, the collector current is fixed; the operating (quiescent) point Q is therefore determined by V_{BEQ} and I_{CQ}. The derivative of this function evaluated at the operation point Q is defined as the small signal transconductance, computed from Fig. 2 as:

$$g_m = \left.\frac{\Delta i_C}{\Delta v_{be}}\right|_Q = \left.\frac{I_S}{nV_{th}} \exp\left(\frac{v_{BE}}{nV_T}\right)\right|_Q \cong \frac{I_{CQ}}{nV_T} \tag{6}$$

For a given V_{BEQ}, the collector-emitter voltage can also be swept leading to the transistor's output characteristics shown in Fig. 3. For small V_{CE} (< 300 mV), the potential is not large enough to attract the carriers traveling from the emitter to the base terminal, and the collector current is very small. If V_{BE} increases, the collector current increases following the exponential rule given by (1). The slope of one of the curves determines the output conductance, obtained as

$$g_o = \left.\frac{\Delta i_C}{\Delta v_{ce}}\right|_Q \cong \frac{I_{CQ}}{V_A} \tag{7}$$

where the early voltage V_A is a fitting parameter. For IC transistors it could be in the range of 30-50V, but for discrete transistor V_A could be in the range of 100 V.

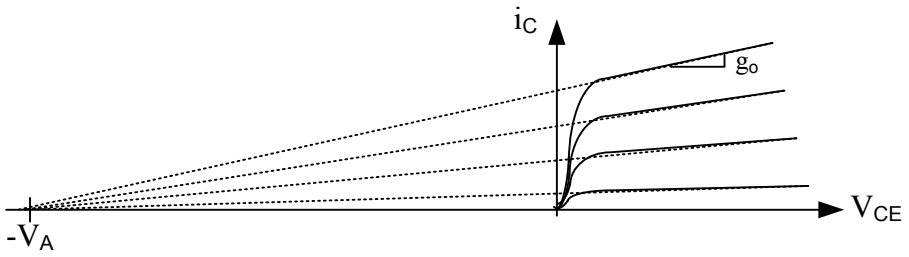


Fig. 3. Transistor's output characteristics for a family of V_{BE} voltages. $V_{BE0}<V_{BE1}<...<V_{BE3}$.

Pre-laboratory exercise

1. Obtain the value of I_S from a simple simulation of the transistor: using the setup of Fig 4, excluding the resistors, apply $V_{BB} = 0.65$ V, measure I_C while $V_{CE} > 0.5$ V and use equation 1. Assume that n = 1. Use the Q2N2222 BJT in the simulation.

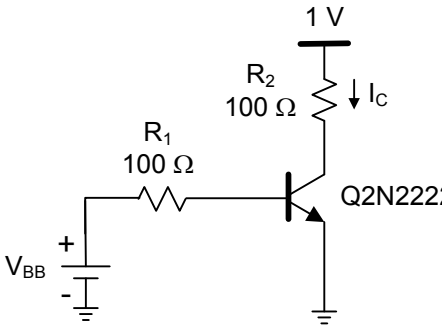


Fig. 4. BJT transistor circuit 2

2. For the circuit in Fig. 2(a), compute the current I_B and I_C, and the voltage V_C for at least 5 input voltages within the range $V_{BE(on)} < V_{in} < 1$V, use $R_B = 100$ kΩ.
3. For the circuit in Fig. 2(a), if the V_{BE} was set to 0.1 V, what would you expect for the value of V_C?
4. Construct the circuit shown in Fig. 4 in PSpice. Place a current marker on the collector of the Q2N2222. Run a DC Sweep on the V_{BB} voltage source to generate the input characteristics. Do a linear sweep starting at 0 V and ending at 2 V with a linear increment of 5 mV. Modify the x-axis variable to be the V_{BE} voltage, not V_{BB}. Comment on your results for all regions of the plot.
5. Repeat step 5 using a current marker at the base of the Q2N2222. Find the input impedance by evaluating the slope around $V_{BE} = 0.65$V; $R_{in} = R_{be} = \Delta v_{be}/\Delta i_b$.
6. Construct the circuit in Fig. 5 in PSpice. Place a current marker on the collector of the Q2N2222. A second DC Sweep is required to generate the output characteristics. First select DC Sweep and set it up for sweeping V_{CE} from 0 V to 6 V with linear increments of 5 mV. Then select Nested Sweep and set that up for sweeping I_B from 0 μA to 50 μA with linear increments of 5 μA. Make sure to select *Enable Nested Sweep*.

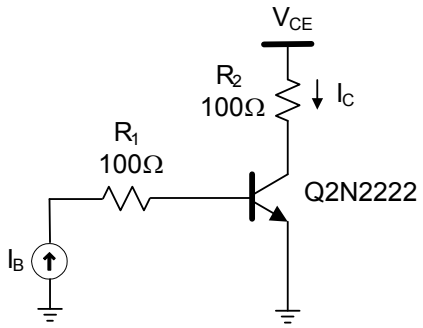


Fig. 5. BJT transistor circuit 3

7. Find the output impedance $R_o = \Delta v_{ce}/\Delta i_c$ from the output characteristics plot.
8. Set V_{CE} shown in Fig. 5 to 5 V and do a linear sweep starting at 0 and ending at 30 μA with a linear increment of 5 μA. Find the DC and AC current gain β_{DC} and β_{ac} of the transistor. Remember, β_{DC} and β_{ac} are defined by (3) and (4), respectively.

Lab Measurement:

1. Measure the actual values of R_c (1 kΩ) and R_b (100 kΩ pot) resistors that will be used in the lab.
2. Connect the circuit in Fig. 2(a). The power supply is 10 V.
3. Set the pot to 10 kΩ. Set V_{in} to 2 V and adjust the potentiometer so that the voltage across R_c is 5 V. Measure the voltage across R_b (remember to measure any new values for Rb if changed). Use Ohm's Law and the actual values of R_c and R_b to compute I_B and I_C.
4. Use the equation (3) of the current gain to compute β.
5. The value of β varies with temperature. Keep V_{in} so that the voltage across R_c is 5 V, and warm the transistor by putting your thumb on the package while observing V_C.
6. Set the potentiometer to its maximum resistance and sweep V_{in} from 0 V to 4 V. Sweep V_{BE} from 0.4 V to 0.7 V with linear increments of 50 mV (use finer increments if necessary). For every value of V_{BE}, measure and record V_{BE}, V_{CE}, I_B and I_C. Use the ammeter to measure I_B. To measure the value of R_b, remove the pot from the circuit. Hint, if V_{in} reaches 4 V before V_{BE} reaches 0.7 V, fix V_{in} at 2 V and reduce the potentiometer resistance. Explain why this works.

Lab Report:

1. Use the data you got in step 1 and 3 of the experiment to compute β.
2. With the experimental observation in step 5, comment on how β is related to the temperature of transistor.
3. Graph the data you collected in step 6 of the experiment. Place V_{in} on the X-axis, and plot V_{BE} and V_C as function of V_{in}. If the collected data has enough points, the plot will show the transition between cutoff and active, and between active and saturation regions. Hint, you might want to use two different Y-axis scales, one for V_{BE} and the other for V_C.
4. Plot I_C (Y axis) as a function of I_B (X axis).
5. From the previous results, find the input impedance, transconductance and β as function of the collector current.
6. Compare your measured results with PSpice simulations
7. Conclusion.

Lab 8: BJT Amplifiers: Basic configurations

Objectives:

The purpose of the lab is to examine the properties of the BJT amplifier configurations and investigate their small signal performance. This laboratory will emphasize the measurement of the operating point,, input and output impedances, and voltage gain of common-emitter and common-collector topologies.

List of Equipment required:

a. Dual Trace Oscilloscope
b. Function Generator
c. Digital Multimeter
d. Dual Power Supply
e. 2N2222 transistor
ϕ. 1 potentiometer of 1 MΩ
g. Resistors
h. Capacitor
i. Protoboard

Introduction

The most commonly used small signal models of the BJT are shown in Fig. 1. It can be shown that both models are equivalent and lead to the same results. Once an operating point is fixed, the AC parameters can be found according to the following expressions:

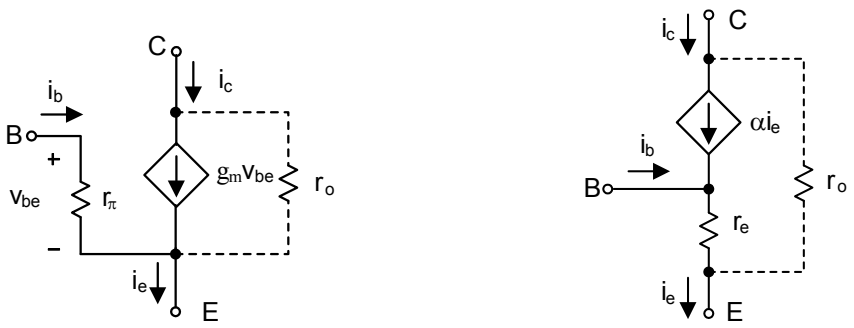


Fig. 1. Small signal models for the BJT: (a) π-hybrid model and (b) T-model

$$r_\pi = \left.\frac{\partial v_{be}}{\partial i_b}\right|_Q = \frac{V_T}{I_{BQ}}$$

$$g_m = \left.\frac{\partial i_c}{\partial v_{be}}\right|_Q = \frac{I_{CQ}}{V_T}$$

$$g_o = \frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_Q = \frac{I_{CQ}}{V_A}$$

$$g_e = \frac{1}{r_e} = \left.\frac{\partial i_E}{\partial v_{BE}}\right|_Q = \frac{I_{EQ}}{V_T}$$

There are three basic BJT amplifier configurations: common-emitter, common-base and common-collector. Each configuration exhibits certain characteristics that make it desirable in certain circuit applications. Table 1 shows a qualitative comparison of the topologies:

Table 1. The comparison of basic BJT amplifier configurations

Characteristic	Common-emitter	Common-base	Common-collector
Input/output phase difference	180°	0°	0°
Input impedance	Medium	Low	Medium
Output impedance	High	High	Low
Voltage gain	Medium	Medium	< 1
Current gain	High	< 1	High

Pre-laboratory exercise

1. Assume the transistor you will use has a β of 155 and V_{BE}(on) = 0.65 V. For the circuit in Fig. 2, calculate the overall resistance (R_B and pot) such that I_C = 1 mA.

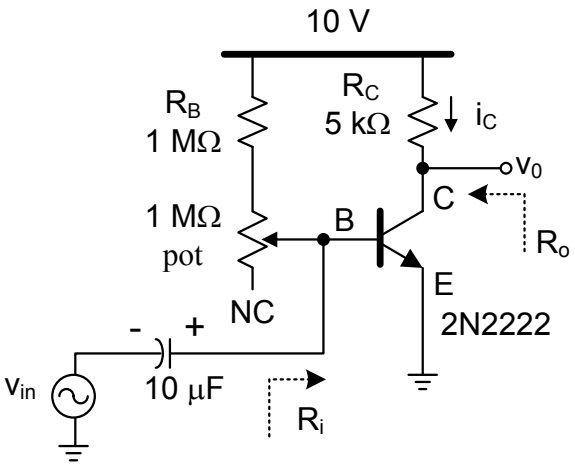


Fig. 2. BJT transistor circuit 1

2. Compute the voltage V_C.
3. Find the values for the input impedance R_i, output impedance R_o and small signal transconductance g_m.
4. Find the value of the small signal voltage gain.
5. Construct the circuit in Fig. 2 in PSpice and find the small signal parameters g_m and r_o. Compare PSpice results and calculations. Explain the differences, if any.
6. Find the value of the resistors for the circuit shown in Fig. 3 so that the magnitude of the small signal voltage gain is 40 dB and the DC collector current is 1 mA. Let β = 155. Determine the values of R_{B1} and R_{B2} so that $R_{B1}||R_{B2}$ > 100 kΩ. First, check the operating point of your design and verify that the voltage gain is approximately given by $-g_mR_C = -\alpha R_C/r_e$. Compute the values of the input impedance at the base and the output impedance at the collector.
7. Note that V_{CE} for the transistor needs to be ≥ 1.3 V. Based on the swing considerations at the output of the amplifier (at the operating point) determine the value of R_E. Based on this information and V_{BE} we can derive the values of R_{B1} and R_{B2}.
8. Construct the circuit in Fig. 3 in PSpice and compare the simulated results and calculations. Explain the differences if any. Also, plot the frequency response over the range and find the low frequency and high frequency poles (adjust the frequency range until you see a lower and upper –3dB frequencies).
9. Find the magnitude of the small signal voltage gain for the circuit shown in Fig. 4 so that I_c = 1 mA. Select the resistors lumped to the base such that the collector current is 1 mA and $R_{B1}||R_{B2}$ > 50 kΩ. First, check the operating point of your design and verify that the voltage gain is approximately given by $g_m(R_L||1/g_m) = R_L/(r_e + R_L)$. Compute the values for the input impedance at the base and the output impedance.
10. Construct the circuit in Fig. 4 in PSpice and compare the simulated results (input impedance, output impedance and voltage gain) with calculations. Explain any differences. Also, obtain the frequency response of Fig. 4 and find the low frequency and high frequency poles.

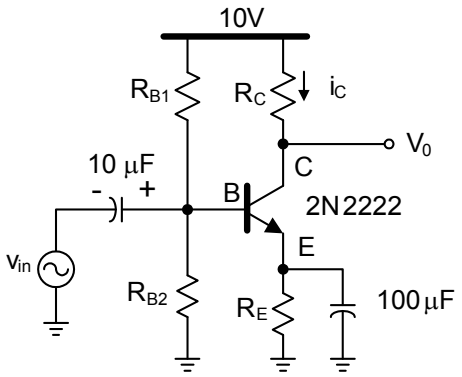


Fig. 3. Common-emitter configuration

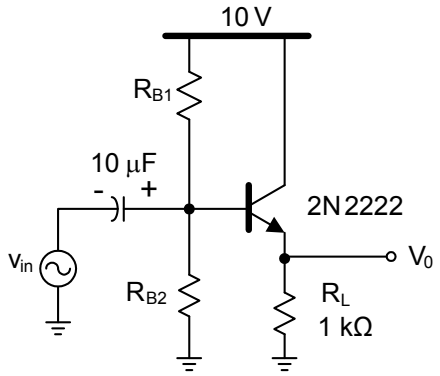


Fig. 4. Common-collector configuration

Lab Measurement:

Part A.

1. Measure the actual values of R_c (10 kΩ) and R_b (1 MΩ) resistors that will be used in the first part of the lab.
2. Connect the circuit in Fig. 2. The power supply is 10 V.
3. Adjust the potentiometer so that the voltage across R_c is 5 V. Measure the voltage across R_b. Use Ohm's Law and the actual values of R_c and R_b to compute I_B and I_C. Compute the value of β.
4. Adjust the potentiometer to vary I_C from 0.6 mA to 1.6 mA in 0.2 mA steps. Add another 1 MΩ resistor in series with R_B if you cannot lower I_C to 0.6 mA while adjusting the pot. Add the 1 MΩ resistor in parallel with R_B to raise I_C to 1.6 mA while adjusting the pot. Record I_C, I_B, V_C, and V_C for each step. Calculate β, r_e, r_π and g_m.
5. To characterize the amplifier shown in Fig. 3,, apply a sinusoidal signal of 10 kHz and amplitude of 10 mV at the input of the amplifier. You may have to use a resistive voltage divider to reduce the amplitude of the signal provided by the signal generator if that cannot be as small as 10 mV. This setup is shown in Fig. 5. Use R_1 = 400 Ω and R_2 = 50 Ω. For R_{B1}, R_{B2}, R_C and R_E use the values computed in the pre-lab. Put the function generator in the 50 Ω impedance mode (not Hi-Z). The 50 Ω shown in Fig. 5 is internal to the function generator. Do not place an external 50 Ω resistor.

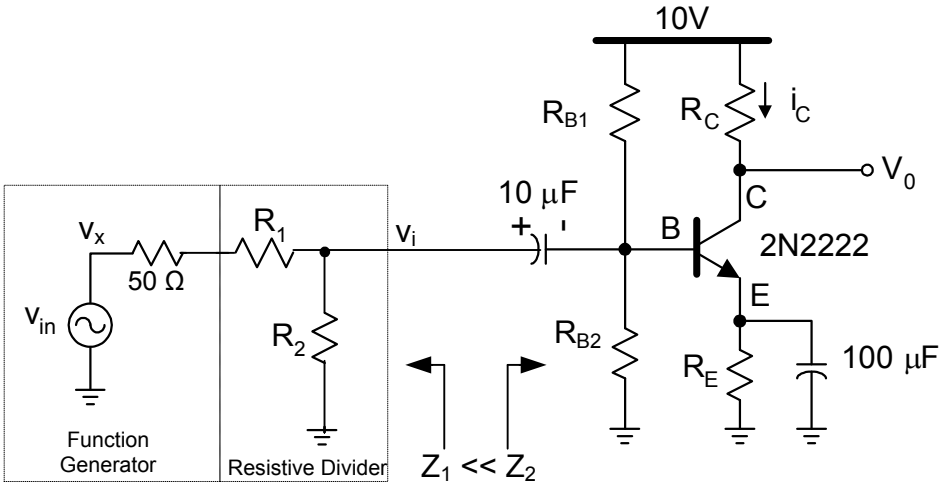


Fig. 5. BJT CE amplifier Lab setup.

6. Sweep the frequency of the input signal and find the low and high -3dB frequencies (if possible). Compare these values with the ones obtained from PSpice and comment on the differences if any.
7. Distortion Analysis of the common emitter amplifier can be performed using the NI Elvis Dynamic signal analyzer. Specific steps to perform distortion measurements are outlined in Part B (below). It is advisable to complete the Part B before you disconnect the circuit and proceed to steps 9, 10 and 11.
8. Construct the circuit shown in Fig. 4; use the resistor values computed in the pre lab and be sure you verify these values using PSpice simulations.
9. Apply a sinusoidal signal of 1 kHz and amplitude of 100 mV at the input of the amplifier. Measure the input impedance, output impedance and small signal gain. Question: how you can experimentally measure the output impedance? Hint: disconnect the signal generator and ground the input capacitor. Apply the signal generator at the output through a blocking capacitor and measure the applied AC voltage and the AC current.
10. Sweep the frequency of the input signal and find the low and high -3dB frequencies (if possible). Compare these values with the ones obtained from PSpice and comment on the differences if any.

Part B. Distortion Analysis of the BJT Common Emitter amplifier

In this section, the BJT CE amplifier (shown in Fig. 5) is used to perform distortion measurements. The common emitter amplifier has been designed with a small signal voltage gain of 40 dB, which is 100 V/V. The amplifier is connected to supply rails between +10V and Ground. Also the voltage swing at the collector terminal is limited within a certain range (based Quiescent Voltage at the Collector in your design). It can be very easily seen that with a gain of 100 V/V, a small input amplitude at the base of the transistor can easily saturate the output of the amplifier and considerably distort the output. So, we attenuate the signal from the function generator using a resistor divider before connecting it to the base terminal of the transistor. The following steps outline how to measure the distortion performance of such a configuration.

1. We will use the circuit configuration shown in Fig. 5. The 50 Ω shown in Fig. 5 is internal to the function generator. Do not place an external 50 Ω resistor. We will use $R_1 = 400\ \Omega$ and $R_2 = 50\ \Omega$ to give us a division ratio of 0.1 from v_x to v_i.
2. Output Vo should be connected to one of the analog channels on the NI Elvis proto board. Use Analog channel 0 (between AI0+/AI0-) for this purpose. Vo is connected to AI0+ while GROUND is connected to AI0-.
3. Turn the proto board supply to the ON position.
4. Set the function generator to the minimum possible amplitude output (50 mVpp). Set the input frequency to 10 kHz. At this setting the voltage level at V_i should be approximately 5 mV peak. If this is not the case, then adjust the values of R_1 and R_2 so that V_i is 5 mV peak.

Be careful when calculating the output peak voltage obtained using the function generator and the resistor divider circuit in Fig. 5. When the function generator's output impedance is50 Ω, the voltage produced *inside the function generator (V_{IN} Fig.) is twice the value indicated on the display*. You need to calculate the voltage produced at V_i accordingly. So when the function generator displays the output to be 50 mVpp, V_i can be calculated as:

$$V_i = 100\ mV * \frac{1}{10} = 10\ mV_{pp} = 5\ mV_{peak}$$

5. The distortion components produced by a BJT CE amplifier depends on the ratio of peak voltage level at the base of the transistor to thermal voltage (V_T). With V_i set to 5 mV, this ratio is approximately 0.2.
6. Launch NI Elvis and Dynamic Signal Analyzer (DSA) SFP and select AI0 as the input source.
7. Select appropriate range for the output amplitude. For more details on settings and understanding output amplitude levels (dBVrms) in the DSA SFP, refer to *Part D* section of Lab 3.
8. Once proper settings are selected in the DSA SFP, output should appear as shown in Fig.Fig. 6. The output shown in Fig. 6 is for input amplitude level (V_i) of 10 mV peak.
9. Obtain distortion performance results for input V_i increasing up to V_T in small increments.

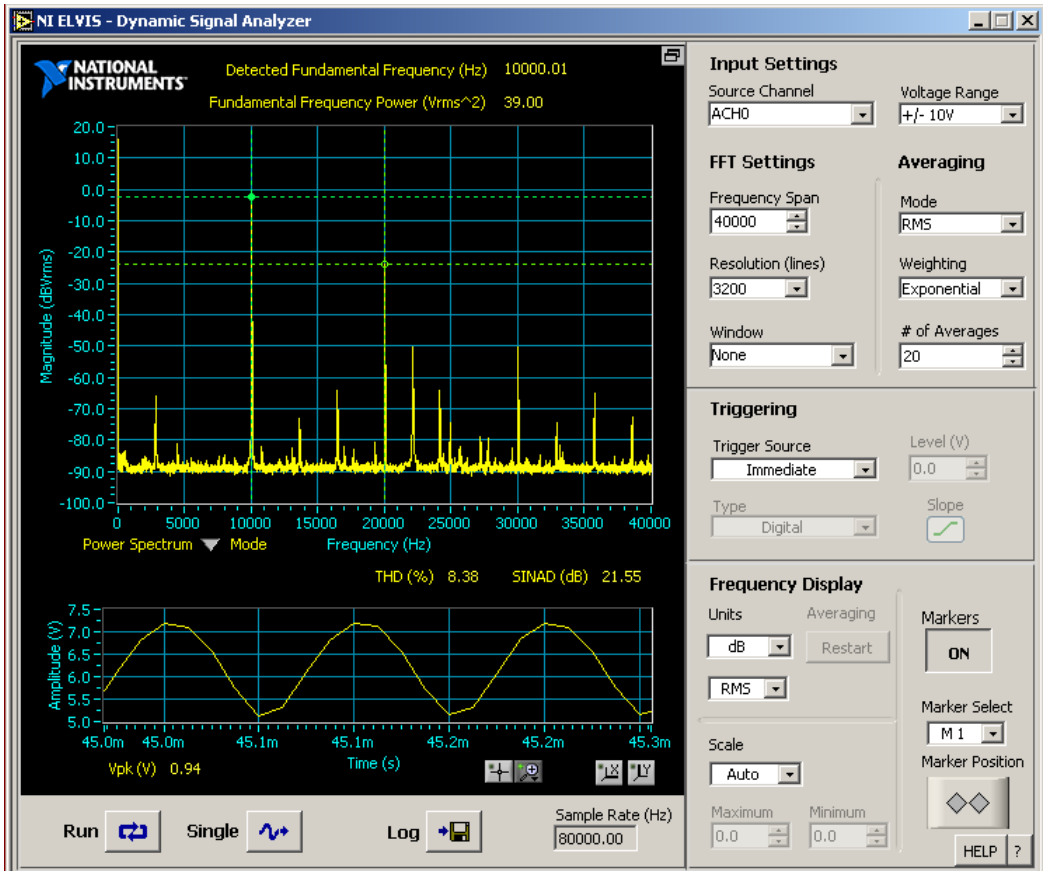


Fig. 6. Output signal distortion measurement of CE Amplifier using NI Elvis DSA. Input signal level V_i = 10 mV peak. Amplifier gain is approximately 40 dB. The expected output voltage is 1 Vpeak.

Lab Report:

1. Use the data from step 3 of the experiment to compute β.

2. Graph the data you collected in step 4 of the experiment. Plot the small signal parameters r_π and g_m as function of I_C. Compare the value of these parameters for $I_C = 1$ mA with PSpice simulations.
3. Use the voltage measurements from steps 5 and 6 of the experiment to compute the input impedance and small signal voltage gain. Report the -3 dB frequencies. Compare your experimental results with PSpice results.
4. Use the voltage measurements from steps 9 and 10 of the experiment to compute the input impedance, output impedance and small signal voltage gain. Report the -3 dB frequencies. Compare your measurements with PSpice results.
5. Comment on the distortion analysis of the Common Emitter configurations. How does the output distortion level vary as the input base emitter voltage is increased in comparison to the thermal voltage V_T? Include screen shots from your measurements.
6. Conclusion.

Lab 9: BJT amplifiers: Design project

Objectives:

The purpose of this experiment is to design a two-stage BJT amplifier, and to use in a unified manner the most relevant design concepts such as small voltage gain, input and output impedance. Design specifications are as follows:

- V_{cc} = 10 V
- Input impedance (AC) > 10 kΩ
- Small signal voltage gain A_v = -10 V/V, when loaded
- Load resistance of 100 Ω
- AC coupled input and output
- Circuit performance insensitive to changes in β
- Output voltage swing > 2 Vpp.
- Discrete components (i.e. transistors, resistors) only; no integrated circuits allowed.

Alternatively, your instructor or TA may provide different specifications.

Pre laboratory Exercise:

To meet the specifications, two stages might be needed. The first stage is an amplifier that is able to achieve input impedance and gain specifications. The last stage could be a buffer to couple the amplifier's output to the load impedance. Design your circuit prior to the laboratory period, and simulate it using PSpice.

- First check the DC operating point (currents and voltages in relevant branches and nodes) and modify your design if any DC node voltage or branch current is significantly different than the desired value. Then perform AC and transient simulations, and fast Fourier analysis to check the amplifier's linearity.
- Use PSpice to verify your calculations; take advantage of the information provided in the output file: impedances and transconductances, currents and voltages and more information is available.
- Check your calculations and gain factors by using AC analysis. Construct your circuit stage by stage, and test the gain of each one individually.
- Measure the input impedance of the different stages; take into account the effects of input impedance of the next stage on the gain of the actual stage.
- Once you are satisfied with the results, connect the next stage and proceed accordingly. Determine the DC gain and the low and high -3dB frequencies.
- Measure the distortion of the circuit by setting the amplitude of the input signal at 100 mVpp and 1 kHz. Increase the input signal up to 200 mVpp, and measure the harmonic distortion components at the output using the FFT option available in Spice.
- Compare your calculations with PSpice simulations.
- Discuss in advance your design progress with the laboratory instructor or course instructor.

Lab Measurement:

Elvis Bode Analyzer should be used to plot the AC magnitude and phase response of the Amplifier. Please check the upper frequency limit and the bandwidth limitations of the Elvis Bode Analyzer installed on your system before using Elvis for this purpose. Instructors or TAs may adjust the frequency response specifications of the amplifier to meet the bandwidth limitations of the Bode Analyzer SFP. Once your design has been approved by the instructor, construct the circuit and perform the following tests:

- Check the DC bias of 'Q' point: I_{BQ}, I_{CQ}, V_{CEQ} and voltage in other nodes.
- Measure the AC voltage gain and determine the low and high -3 dB frequencies.
- Measure the input and output impedances (Hint: see previous experiment).
- Determine how sensitive the above parameters are to change with β. You must use different transistors to do this.

- Increase the input signal up to 200 mVpp, and measure the harmonic distortion components at the output using the FFT option available in the oscilloscope's math option.
- Use Elvis to obtain the AC response of the amplifier. Magnitude and phase response plots can be easily obtained using the Elvis Bode Analyzer SFP as indicated in the previous labs.
- Also use the Dynamic signal analyzer from NI Elvis to obtain the distortion performance of the amplifier. Select the input amplitude and amplitude settings on the NI Elvis SFP accordingly. The procedure for making these settings can be found in the previous labs.
- Compare the experimental results with PSpice simulations.

If any of the measurements do not meet the given specifications, you must modify your design until they do.

Lab Report:

1. State the objective of this experiment.
2. Discuss your design procedure in detail. State any and all assumptions, and give the relevant design equations.
3. Give the AC voltage gain of your circuit. Did you have to modify your circuit to meet this specification? Find the low and high frequency corners, and justify these values.
4. Give the AC input and output resistances of your circuit. Did you have to modify your circuit to meet this specification? Explain how you measured it.
   - Does the input resistance depend on the amplitude of the AC signal?
   - How does the calculated theoretical input impedance compare with your measured impedance?
5. Discuss in detail how and why your circuit is insensitive to changes in β.
6. If any part of your design was unable to meet the specifications, explain why.
7. Is the small signal model used for your design equations valid for all input amplitudes? Why or why not?

Lab 10: Characterization of the MOS transistor

Objectives:

The purpose of the lab is to characterize the MOS transistor and to experimentally find the I-V characteristics, threshold voltage, small signal transconductance and output impedance.

List of Components and Equipment

a. Dual Trace Oscilloscope
b. Function Generator
c. Digital Multimeter
d. Dual Power Supply
e. CD4007 MOS transistor
f. 2N7000 n-channel Power MOS transistor
γ. 1 potentiometer of 10 kΩ
h. Miscellaneous resistors
i. Capacitor
j. Protoboard

Procedure:

The objective of this laboratory is to characterize and bias the MOSFET. A MOSFET can be characterized by several parameters, such as β and V_t. Fig. 1(a) shows the output and transconductance characteristics of an n-channel MOSFET and illustrates how β_n and V_{tn} characterize the MOSFET. The large signal model for the n-channel MOSFET is given as follows:

Saturation (active) region:

$$I_D = \frac{\beta_n}{2}(v_{GS} - V_{tn})^2(1 + \lambda_n v_{DS}), \qquad 0 < v_{GS} - V_{tn} < v_{DS}$$

Triode region:

$$I_D = \beta_n\left[(v_{GS} - V_{tn})v_{DS} - \left(\frac{v_{DS}^2}{2}\right)\right](1 + \lambda_n v_{DS}), \qquad v_{DS} < (v_{GS} - V_{tn})$$

where:

$$\beta_n = k_n' W/L$$

where β_n is the transconductance gain factor; μ_n is the mobility of the carriers in the channel, C_{ox} is the capacitance per square micrometer and W and L are the width and length of the transistor's gate. λ_n is the channel modulation parameter. For a first-order approximation, it can be considered zero.

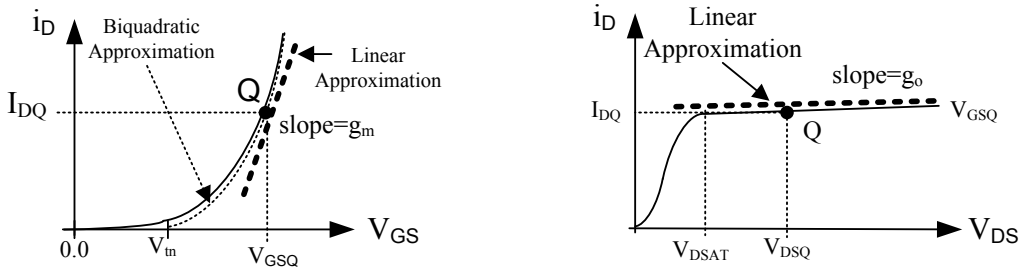


Fig.1 MOSFET characteristics: (a) input and (b) output.

Like the BJT, the operating point Q is determined by V_{GSQ} and I_{DQ}. The derivative of the drain current evaluated at the operation point Q is defined as the small signal transconductance, computed as:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_Q = \beta_n \left(V_{GSQ} - V_{tn}\right)$$

For a given V_{GSQ}, the drain-source voltage can also be swept leading to the transistor's output characteristics shown in Fig. 1(b). The slope of the curve determines the transistor's output conductance, obtained as

$$g_o = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q \cong \lambda_n I_{DQ}$$

Pre-laboratory exercise

A simple biasing scheme for the n-channel MOSFET is shown in Fig. 2. Use V_{DD} = 10 V. Find β_n, λ_n and V_{tn}. For PSpice simulations, your TA or instructor will provide you with the necessary model files and a guide on adding them to PSpice.

1. Set up your circuit in PSpice as shown in Fig. 2(a) using first the CD4007 MOS transistor.
2. To find V_{tn} and β_n, sweep V_{GS} from 0 to 5 V using increments of 1 mV with a nested sweep of V_{DS} from 3 to 5 V using increments of 0.5V. This will generate a series of I_D-V_{GS} characteristic plots similar to the one in Fig. 1(a). Use these plots to find the approximate value V_{tn} and β_n.
3. From the plots you generated in step 2, find the transistor's g_m around V_{GS} = 3 V. Does the g_m change for different values of V_{DS}? Explain.
4. Using the same setup as in step 2. sweep V_{DS} from 0 to 5 V using increments of 1 mV with a nested sweep of V_{GS} from 1 to 5 V using increments of 0.5 V. This will generate a series of I_D-V_{DS} characteristic plots similar to the one in Fig. 1(b). Use these plots to find an approximate value for λ_n.
5. Repeat steps 1-4 for the 2N7000 MOS transistor.

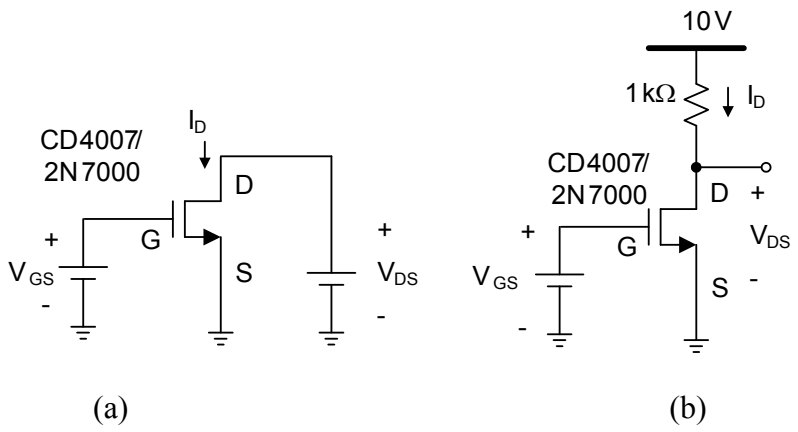


Fig. 2. (a) PSpice simulations setup (b) Schematic used for measuring the n-channel MOS transistor characteristics and small signal parameters.

Unfortunately, the biasing scheme of Fig. 2 is very sensitive to changes in the MOSFET characteristics because there is no means of stabilizing the biasing point. A better biasing scheme is shown in Fig. 3. In this circuit, an increase in the drain current causes an increase in the source voltage. If the gate voltage is constant, then the value of V_{GS} decreases opposing the original increase in drain current causing the bias point to be stabilized. There is an inherent feedback mechanism behind the source resistance R_s.

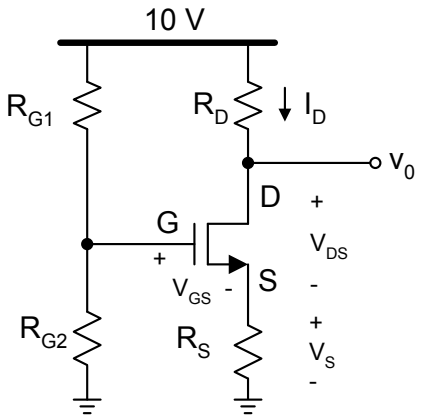


Fig. 3. MOSFET based amplifier: circuit 2

6. Construct the circuit shown in Fig. 3 in PSpice using the CD4007 MOSFET. Using the parameters found in the previous steps, find the resistors such that the transistor is biased at $I_D = 1$ mA and $V_{DS} = 2$ V, and $R_D/R_S = 10$. The parallel combination of R_{G1} and R_{G2} should be greater than 100 kΩ. For your calculations you can ignore λ_n. Simulate your results. Repeat for the 2N7000 MOSFET with $I_D = 20$ mA and keep all other requirements the same.

CAUTION: MOSFETs have extremely high input impedances and can be damaged by the accumulation of excess static charge. To avoid possible damage, the following procedures are suggested:

- Wrap the device in aluminum foil when not being used or stick the leads of the MOSFET in conducting foam.
- Handle the MOSFET by the case and avoid touching the leads.
- Do not insert or remove MOSFETs from a circuit with the power on (this suggestion is good practice for all types of electronic devices).

Lab Measurement:

NOTE: When you use the CD4007, short the B (bulk) terminal to ground.

WARNING: Handle the 2N7000 power transistor with care; it is very sensitive and capable of delivering large currents

Part A

1. Using the CD4007, connect the circuit of Fig. 2(b); the 1 kΩ resistor will limit I_D to 10 mA and keep the V_{DS} voltage greater than or equal to V_{GS} for a wide range. Sweep V_{GS} from 0 V up to a voltage such that $I_D = 5$ mA. Record the results for at least 20 different values with emphasis around the expected V_{tn}. Plot the results in the I_D-V_{GS} plane.
2. Select the V_{GS} that gives you $I_D = 1$ mA, sweep V_{DD} from 0 to 10 V, and measure V_{DS}. Compute the I_D and V_{DS} for at least 20 different values of V_{DD} with emphasis in the lower range (0 -1V) and plot the results in the I_D-V_{DS} plane.
3. From step 1, find approximate values for V_{tn}, β_n and g_m. From step 2, find approximate values for V_{tn}, β_n and λ_n.
4. Repeat steps 1-3 using 2N7000. Change the resistor to a tenth of its original value. Try to obtain currents that are ten times larger than those used for the CD4007N. Compare the results and comment on the differences.

Part B

1. Using the CD4007, connect the circuit of Fig. 3 and use the values obtained in the pre-lab. Measure the operating point (I_D, V_S and V_D) and compare these values with PSpice results. Comment on any differences;

how do you explain them? Try using a pot (10~25 kΩ) between R_{G1} and R_{G2} with the middle terminal connected to the MOS gate. Explain why this works better than using two fixed values for R_{G1} and R_{G2}.

2. Repeat 1 using the 2N7000. Compare and comment on the results.
3. Compare the I_D and V_S that were obtained from the circuit in Fig. 3 to the values that were obtained using the circuit in Fig. 2(b).

Lab Report:

1. Compare the values of β_n and V_{tn} as measured from the output and transconductance characteristics in part A. Which are more accurate?
2. Compare your measured values of I_{DQ}, V_{DSQ}, and V_{GSQ} for each of the biasing circuits in Part A and B.
3. Compare the change in I_{DQ} between the two different MOSFETs.
4. From your measurements, estimate a value for λ_n.
5. What happens if the parallel combination of the gate biasing resistors in Fig. 3 was smaller than 100 kΩ?
6. Conclusion

Lab 11: CMOS Amplifier configurations

Objective:

The purpose of the lab is to examine the properties of the MOS amplifier configurations, and to investigate their small signal performance. This laboratory will emphasize the measurement of the operating point (I_{DQ}, V_{GSQ} and V_{DSQ}), input and output impedances and voltage gain of common-source and common-drain topologies.

List of Equipment required:

a. Dual Trace Oscilloscope
b. Function Generator
c. Digital Multimeter
d. Dual Power Supply
e. CD4007 MOS transistor
f. 2N7000 n-channel MOS transistor
g. 1 potentiometer of 1 MΩ
h. Resistors
i. Capacitors
j. Protoboard
k. Relevant NI Elvis SFPs.

Introduction

The most commonly used small signal models of the MOSFET are shown in Fig. 1. It can be shown that both models are equivalent and lead to the same results.

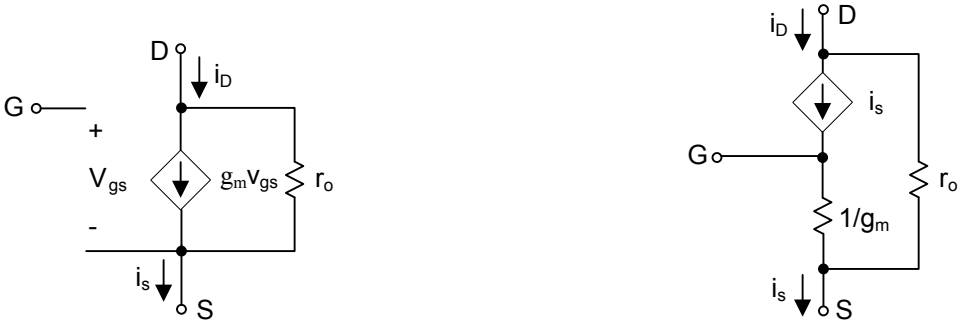


Fig. 1. Small signal models for the BJT: (a) π-hybrid model and (b) T-model

Once an operating point is fixed, the AC parameters can be found according to the following expressions:

$$r_o = \left.\frac{\partial v_{ds}}{\partial i_d}\right|_Q \cong \frac{1}{\lambda I_{DQ}}$$

$$g_m = \left.\frac{\partial i_d}{\partial v_{gs}}\right|_Q = \frac{2\mathrm{I}_{DQ}}{(V_{GSQ} - V_t)} = \sqrt{2\beta \mathrm{I}_{DQ}} = \beta(V_{GSQ} - V_t)$$

$$\beta = k' W/L$$

Similar to its BJT counterpart, there are three basic MOS amplifier configurations: common-source, common-gate and common-drain. Each configuration exhibits certain characteristics that make it desirable in certain circuit applications. Table 1 shows a qualitative comparison of the topologies:

Table 1. The comparison of basic MOS amplifier configurations

Characteristic	Common-source	Common-gate	Common-drain
Input/output phase difference	180°	0°	0°
Input impedance	High	Low	High
Output impedance	High	High	Low
Voltage gain	Medium	Medium	< 1
Current gain	High	< 1	High

Pre-laboratory exercise

1. For the circuit in Fig. 2, use the parameters you extracted from the previous lab for the CD4007 and calculate all resistor values and voltages so that $I_D = 1$ mA and $V_D = 5$ V.

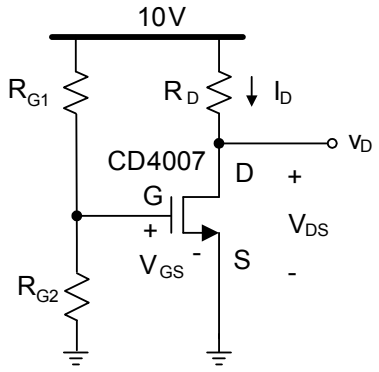


Fig. 2. MOS transistor circuit

2. Find the values for the input impedance, output impedance and small signal transconductance.
3. Find the value of the small signal voltage gain.
4. Construct the circuit in Fig. 2 in PSpice and find the small signal parameters r_o and g_m. Compare PSpice results and calculations. Explain any differences.
5. Find the value of the resistors for the circuit shown in Fig. 3 (use the CD4007) so that the magnitude of the small signal voltage gain is 20 dB and $I_D = 0.5$ mA. Make sure the transistor operates in the saturation region. Select the values of R_{G1} and R_{G2} so that $R_{G1}||R_{G2} > 100$ kΩ. Check the operating point of your design and verify that the voltage gain is approximately given by $-g_m R_D$. Compute the values for the input impedance and output impedance.
6. Construct the circuit in Fig. 3 in PSpice and compare the simulated results and calculations. Explain any differences.
7. Plot the frequency response of the circuit shown in Fig. 3,and find the low and high frequency poles.
8. For the circuit in Fig. 4, use the parameters you extracted in the previous lab for the 2N7000 and find the values of I_D and the resistors so that the magnitude of the small signal voltage gain is greater than -2 dB. Select the values of R_{G1} and R_{G2} so that $R_{G1}||R_{G2} > 100$ kΩ. Check the operating point of your design and verify that the voltage gain is approximately given by $g_m(R_L||1/g_m)$. Compute the values for the input impedance and output impedance.
9. Construct the circuit in Fig. 4 in PSpice and determine the input impedance, output impedance and voltage gain. Compare these values with the calculated values. Explain any differences.
10. Measure the frequency response of the circuit in Fig. 4 and find the low and high frequency poles.

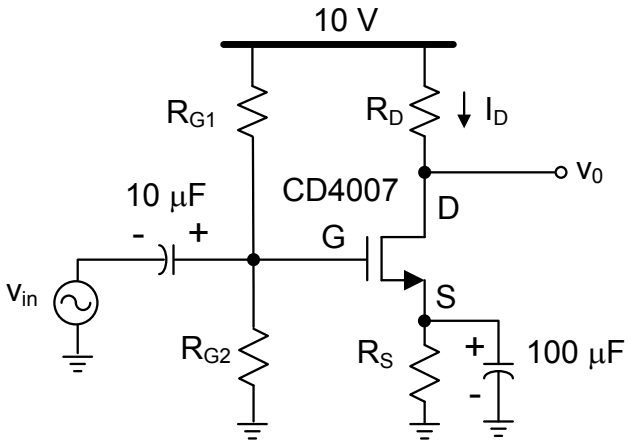


Fig. 3. Common-source configuration

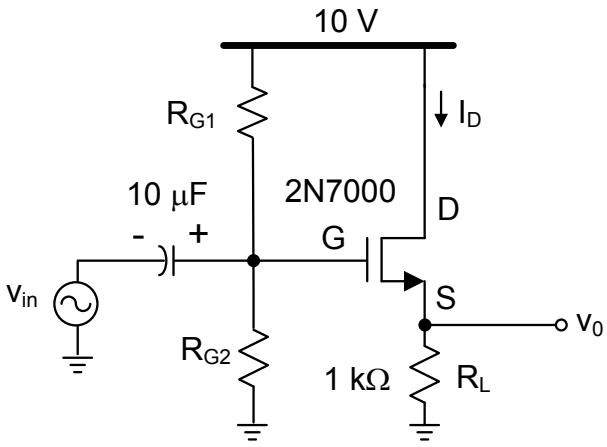


Fig. 4. Common-drain configuration

Lab Measurement:

1. Connect the circuit in Fig. 2 using the resistor values you calculated in the pre lab.
2. Use a potentiometer to set the voltage across R_D to 5 V and I_D to 1 mA
3. The value of V_t varies with temperature. Keep the potentiometer setting so that the voltage across R_D is 5 V. Warm the transistor by touching the package and observe V_D.
4. Adjust the potentiometer to change V_{GS} from 1V to 3V and measure I_D. Take at least 20 measurements with emphasis around and beyond the expected V_t. Plot these results and the g_m.
5. Construct the circuit shown in Fig. 3. Use the resistor values computed in the pre-lab. Verify the component values using PSpice.
6. Apply a sinusoidal input signal with frequency and amplitude of 10 kHz and 10 mV, respectively. Measure the input impedance and the small signal gain.
7. Remove the capacitor that is connected to the source of the MOSFET and measure the voltage gain. Explain any differences.
8. Reconnect the capacitor to the source of the MOSFET. Sweep the frequency of the input signal and find the low and high -3 dB frequencies. Compare these values with the ones obtained from PSpice and comment on any differences.

9. Use the NI Elvis distortion analyzer (DSA) SFP to obtain the distortion performance of the common source configuration. Details regarding how to set up the experiment to obtain these measurements are explained in Part B of Lab 8 (for the Common Emitter configuration).
10. Construct the circuit shown in Fig. 4.Use the resistor values computed in the pre-lab and verify these values using PSpice. A potentiometer might be need to achieve the required bias voltage.
11. Apply a sinusoidal signal with frequency and amplitude of 1 kHz 100 mV, respectively. Measure the input impedance, output impedance, and small signal voltage gain.
12. Sweep the frequency of the input signal and find the low and high -3 dB frequencies. Compare these values with the ones obtained from PSpice and comment on any differences.
13. Use the NI Elvis distortion analyzer (DSA) SFP to obtain the distortion performance of the common drain configuration.

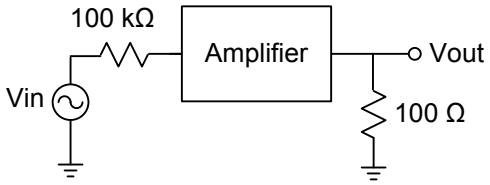
Lab Report:

1. Use the results from steps 1, 2 and 4,and comment on the PSpice and experimental approximation for the small signal transconductance g_m.
2. With the experimental observation in step 3, comment on how V_t is related to the temperature of transistor.
3. Use the voltage measurements from steps 6, 7, and 8 to compute the input impedance and small signal voltage gain. Report the -3 dB frequencies. Compare your experimental results with PSpice results.
4. Use the voltage measurements from steps 10 and 11 to compute the input impedance, output impedance, and small signal voltage gain. Report the -3 dB frequencies. Compare your measurements with PSpice results.
5. Conclusion.

Lab 12: CMOS amplifiers: Design project

Objectives:
The purpose of this experiment is to design a multi-stage CMOS amplifier. Your instructor may provide different specifications.

Design a multi-stage amplifier for the application shown below. The amplifier must drive a load of 100 Ω.. So, a low impedance output stage is needed (less than 100 Ω). The maximum input signal is 100 mVpp, and the peak voltage at the output is 2 V. The amplifier's low frequency –3 dB corner must be below 50 Hz (audio applications); the high frequency -3 dB corner frequency must be beyond 20 kHz. In order to meet the specifications, 2or 3 stages might be necessary. Combine different amplifier topologies as necessary. Avoid large attenuation factors at the input. In practical applications this is avoided because your circuit would become more sensitive to noise. The 100 kΩ resistor represents the sensor's (microphone) impedance.



Use the following specifications:

- V_{DD} = 10 V
- Amplifier's input impedance (AC) > 1 MΩ
- Small signal voltage gain $|A_v|$ = 40 V/V
- Load resistance of 100 Ω
- AC coupled input and output
- Circuit performance insensitive to temperature and V_t variations
- Output voltage swing of 4 Vpp.
- Discrete components (i.e. transistors, resistors, capacitors) only; no integrated circuits allowed
- You may use any combination of CD4007 and 2N7000 MOS transistors in your design

Pre laboratory Exercise:
Frequency response (AC simulations) and transient simulations (fast Fourier analysis for checking amplifier's linear range) must be performed.

- Check the DC bias point and measure currents and voltages in relevant branches and nodes. Use PSpice to verify your calculations. Take advantage of the information provided in the output file: impedances and transconductances, currents and voltages and more information is available.
- Check your calculations and gain factors by using AC analysis. Construct your circuit stage by stage, and test the gain of each one individually.
- Measure the input impedance of the different stages; take into account the effects of input impedance of the next stage on the gain of the actual stage.
- Once you are satisfied with the results, connect the next stage and proceed accordingly. Determine the DC gain and the low and high -3dB frequencies.
- Measure the distortion of the circuit by setting the amplitude of the input signal at 100 mVpp and 1 kHz. Increases the input signal up to 200 mVpp and measure the harmonic distortion components at the output using the FFT option available in PSpice.
- Compare your calculations with PSpice simulations.
- Discuss in advance your design progress with the laboratory instructor or course instructor.

Lab Measurement:

Build the circuit that you designed in the pre lab. Use a 100 Ω resistor as a load and the signal generator at the input. You must include the 100 kΩ resistor in your experiment. Do not complicate your setup unless you are sure that everything is properly connected and the operating points are correct.

Follow these guidelines.

- Use blocking capacitors at the input and output of your amplifier; the operating points will not be affected by input source and load impedance. You may also use blocking capacitors between the stages to isolate the operating point of each stage.
- Before you connect the input signal, check the operating point of the active devices: currents and voltages. Compare these vales with the simulated ones. If the values differ by more than 20%, discuss this with your TA.
- Once the operating points are adjusted, inject a single with amplitude and frequency of 100 mVpp and 1 kHz, respectively. Analyze the signal in relevant nodes. Record your results and compare them with the simulated ones.
- Sweep the frequency of the input signal from 20 Hz to 50 kHz and find the passband gain, low frequency and high frequency –3 dB frequencies. Compare these results with the results from PSpice simulations; justify your results.
- Use Elvis to obtain the AC response of the amplifier.
- Determine how sensitive the amplifier is by changing the transistors. Monitor the circuit's behavior.
- Set the frequency at 1 kHz and perform FFT analysis using the math options available in the oscilloscope. Measure the second and third harmonic distortion components and compare them with PSpice results.
- Increase the amplitude of the input signal and measure the harmonic distortion components of the signals at relevant nodes. Repeat this procedure for 100 mVpp, 150 mVpp, 200 mVpp and 300 mVpp, and plot the results.
- Use the Dynamic Signal Analyzer SFP from NI Elvis to obtain the distortion and THD performance of the amplifier.

If any of the measurements do not meet the given specifications, you must modify your design until they do.

Lab Report:

Include the following items:

- Your design considerations and design procedure.
- Calculations and final values used. Justify any approximations.
- Determine the operating point for all stages and justification of the gain associated to each stage. DC analysis is needed Show the values for transconductances and resistors.
- Apply an AC signal and show the signal gain at relevant nodes of the amplifier. Show the passband gain, low frequency and high frequency –3 dB frequencies, and justify your results
- Apply a 100mVpp sine wave signal and analyze the waveforms in relevant nodes. Compare the gain measured in this simulation with the ones obtained in the AC analysis and explain any differences. Use the FFT option for measuring the harmonic distortion components of the signals at relevant nodes. Report the harmonic distortion plots. Justify your results.
- Include Fourier analysis of the output waveform. Harmonic distortion components must be less than -30 dB for a 100 mVpp input.

Add conclusions to your report. Include screen shots from NI Elvis measurements in your report.

