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Commodore 1541 Troubleshooting & Repair Guide

Michael G. Peltier

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Warranty Warning

Commodore Electronics, Limited, and the author advise that any attempt to repair or modify the VIC-1541 during the warranty period will void the factory warranty.

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Michael G. Peltier

To my children, Joshua, Matthew, and Rachel

Introduction

This book provides troubleshooting and repair instructions for the VIC-1541 series disk drives, Models 1540, 1541, and 1542. When the text is referring to all three models, the nomenclature VIC-1541 will be used. If the text refers to a disk drive by model number, the information applies only to that model.

Chapter 1, "Description of the VIC-1541," explains briefly what a VIC-1541 is and examines the anatomy of a floppy disk. If you would like to get your hands on the insides of your VIC-1541, read Section 1.3, "Inside the VIC-1541." This section provides instructions for disassembling the VIC-1541. The text familiarizes you with each of the subassemblies as they are removed. It also gives instructions for changing the device number and reassembling the parts.

Chapter 2, "Theory of Operation," is designed to help you understand "how it works." Three levels of the theory of operation are provided, each based on a block diagram. The first level of theory is general and oversimplified. The second level goes a little deeper, but although functions of major circuits are discussed, level 2 is still simplified. The third level analyzes the major circuits discussed in level 2, using a detailed block diagram for each circuit.

A fourth level of theory of operation is provided in Chapter 7, "Advanced Theory of Operation." This theory is discussed on a component level, using the circuit schematic instead of a block diagram.

Chapter 3, "Alignment," provides instructions for proper adjustment of your disk rpm's, track No. 1 stop, and read/write head alignment. In Section 3.3, "Read/Write Head Alignment," two methods of alignment are presented. One procedure is a shop-quality alignment. For those who do not have access to a reference disk or dual-trace oscilloscope, a second alignment procedure is provided. This procedure only requires a screwdriver, voltmeter, and the homemade video detector that is described in Appendix B. Although not shop-quality because of a lack of accurate reference, this emergency procedure will get your drive working. Guidance in selecting a reference is also provided. Chapter 3 also introduces a utility program which can exercise the mechanical functions of the drive for test purposes.

Chapter 4, "Preventive Maintenance," provides suggestions to promote long disk drive and disk life. Also covered is periodic maintenance. Section 4.3, "Cleaning the Read/Write Head," has two head-cleaning procedures. One procedure requires a head-cleaning disk. The other procedure covers manual cleaning of the read/write head.

Chapter 5, "Basic Troubleshooting and Repair," explains how to troubleshoot the VIC-1541, solving some problems while focusing other solutions on a group of parts using a flowchart. Several options are given to repair the disk drive. One of the options is to troubleshoot further using Chapter 6, "Advanced Troubleshooting and Repair." Chapter 6 provides a continuation of the flowchart begun in Chapter 5. Using test equipment and these flowcharts, the problem is further narrowed down to a smaller group of parts.

Finally, five appendices are provided. Appendix A provides detailed technical data including interconnect diagrams, schematics, parts layouts, and parts lists. Appendix B gives instructions for fabricating a video detector used in the emergency head alignment procedures. Appendix C contains MOS handling instructions. Appendix D illustrates standard IC pin numbering. Appendix E describes the custom disk controller IC which is used in Models 1541 and 1542.

CHAPTER 1

Description of the VIC-1541

If you are interested in repairing or maintaining your VIC-1541 disk drive, you probably already know basically what a disk drive is and what it is used for. For the benefit of the novice who may have a few questions about the basics, I will describe the VIC-1541 and its uses here.

1.1 WHAT IS A VIC-1541?

The VIC-1541 disk drive is a mass storage peripheral which can store or recall information from a removable floppy disk. When connected to the Commodore 64 or VIC 20, the VIC-1541 gives the computer the capability to "file" information on the floppy disk. Without this file capability, your computer cannot perform such useful work as word processing or database management. Also, program storage and retrieval is much faster and easier when using the disk drive in lieu of the Datasette recorder.

Three versions of the VIC-1541 have been produced by Commodore; they can be seen in Figs. 1-1 through 1-3. Although these disk drives closely resemble each other, their internal differences are substantial. All three versions of the VIC-1541 have the same controls, indicators, connectors, and command sets. Table 1-1 describes the controls, indicators, and connectors.

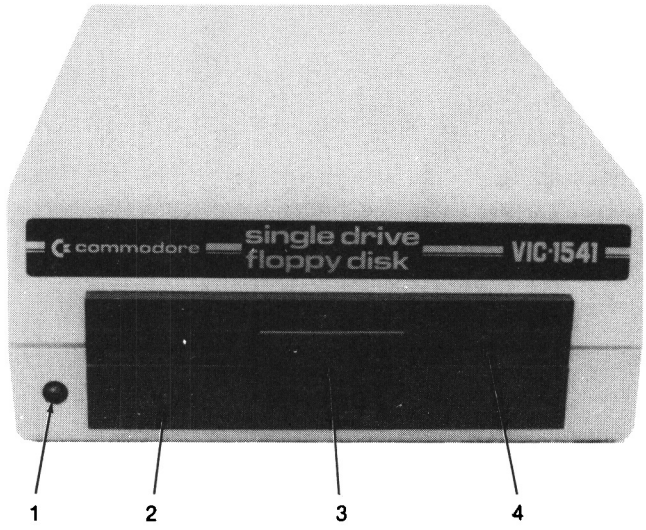


Fig. 1-1. Front view of Model 1540.

Note: All three versions of the VIC-1541 have "1541" printed on their fronts. Model 1540 has "VIC-1541" and "single drive floppy disk." Models 1541 and 1542 both have "1541" on their fronts. Model 1542, however, has a twist-type disk latch on the left-hand side of the disk slot, as can be seen in Fig. 1-3. Because some versions of Model 1540 use the same housing as Models 1541 and 1542, it is necessary to refer to the parts layout drawings in Appendix A to determine exactly which model you have.

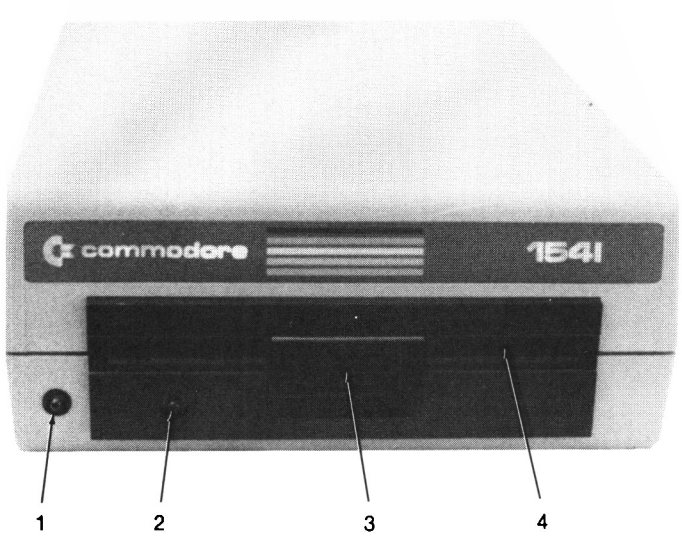


Fig. 1-2. Front view of Model 1541.

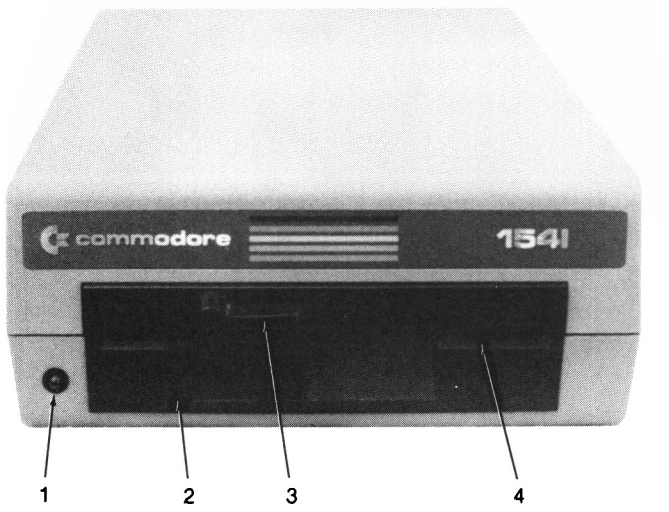


Fig. 1-3. Front view of Model 1542.

Table 1-1. Description of Controls, Indicators, and Connectors

ITEM	FIGURE	CONTROL, INDICATOR, OR CONNECTOR
1	1-1, 1-2, 1-3	Power LED
2	1-1, 1-2, 1-3	Access/Error LED
3	1-1, 1-2, 1-3	Disk Latch
4	1-1, 1-2, 1-3	Disk Slot
5	1-4	Power Switch
6	1-4	AC Line Cord Connector
7	1-4	Fuse Holder
8	1-4	Serial Bus Connector
9	1-4	Serial Bus Connector

The power LED (Item 1), when illuminated, indicates that the VIC-1541 is turned on. The access/error LED (Item 2) indicates when the VIC-1541 is being accessed. *Never* remove the floppy disk when this LED is continuously illuminated. An error condition is indicated when the access/error LED is flashing, in which case the disk may be removed.

The disk latch (Item 3) holds the floppy disk in place. On the 1540 and 1541, the disk is held in place by pressing down on the latch. To release the floppy disk, push the latch in; the disk will then be ejected. On the 1542, the floppy disk is held in place by turning the latch clockwise. It is released by turning the latch counterclockwise. The floppy disk is not ejected on the 1542. The user inserts the floppy disk into the disk slot (Item 4), as shown in Fig. 1-5.

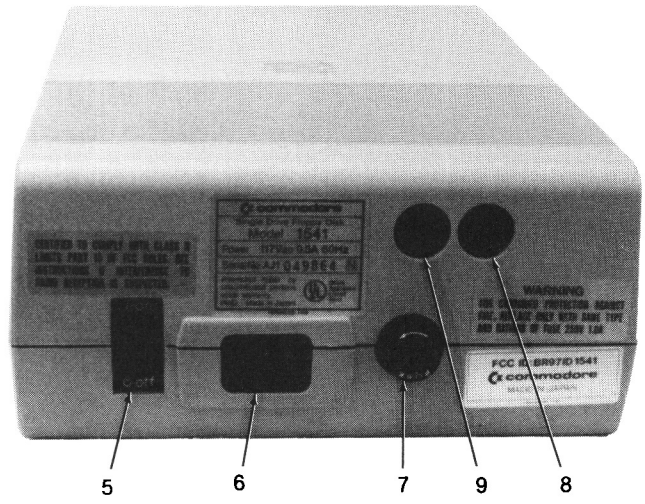


Fig. 1-4. Rear view of VIC-1541.

The backs of all three models are identical in appearance and function (see Fig. 1-4). The power switch (Item 5) is used to turn the disk drive on and off. Depressing the top portion of the switch turns the disk drive on; depressing the bottom portion of the switch turns the disk drive off. The ac line cord is plugged into the ac line cord connector (Item 6). The fuse holder (Item 7) houses the ac line fuse. The fuse may be changed by unscrewing (counterclockwise) the cap of the fuse holder using a Phillips or common screwdriver. The fuse may then be removed and replaced with a 1.0 ampere fuse only.

To replace the cap of the fuse holder, rotate the cap clockwise using a screwdriver. Do not overtighten the cap or the fuse holder may be damaged.

WARNING

- *Never* attempt to change the fuse with the ac line cord installed.
- *Always* install fuse of correct size and rating; failure to do so may result in fire and/or personal injury.

The two serial bus connectors (Items 8 and 9) are used to connect the VIC-1541 to the computer and other serial bus peripherals. Both connectors are electrically identical. They are wired in parallel.

1.2 ANATOMY OF A FLOPPY DISK

A floppy disk is illustrated in Fig. 1-5 and its parts are enumerated in Table 1-2.

Table 1-2. Anatomy of a Floppy Disk

ITEM	FIGURE	DESCRIPTION
10	1-5B	Disk
11	1-5B	Jacket
12	1-5A	Index Cutout
13	1-5B	Index Hole
14	1-5A	Read/Write Slot
15	1-5A	Write Protect Notch

The floppy disk consists of a Mylar disk (Item 10) inside a jacket (Item 11). The disk has a magnetic coating similar to the magnetic coating on audio tape cassettes or videotape. The recording and playback principles involved are identical to those of magnetic tape. The shape of the disk is more convenient than magnetic tape, because each piece of information passes the vicinity of the head 300 times per minute. This allows random access of the information on the disk. Data is physically stored in rings on the bottom surface of the disk. These rings are called *tracks*. There are 35 tracks on each disk. Each track is further divided into sectors. The inner tracks contain 17 sectors while the outer tracks contain 21 sectors. Each sector contains sync, identification, track number, sector number, and checksum information; collectively called a *header*. Following the header are 254 bytes of data, a checksum, and, optionally, next track and sector pointers; collectively called a *block*. Track No. 18 is used for housekeeping purposes (i.e., the directory and block availability map).

The jacket (Item 11) has several cutouts in it. The index cutout (Item 12) and index hole (Item 13) serve no purpose on the VIC-1541. Most other disk drives use these holes to locate sector 1 by detecting when the index hole lines up with the index cutout. This is not necessary on the VIC-1541 since all the track and sector numbers are written in the headers on the disk.

The read/write slot (Item 14) allows the recording head (called the read/write head) to touch the disk. A similar slot is cut on the opposite side of the floppy disk. The write protect notch (Item 15) is provided as a means of protecting the disk against accidental erasure or overwriting. If the write protect notch is left uncovered, writing to the floppy disk is permitted. If the write protect notch is cov-

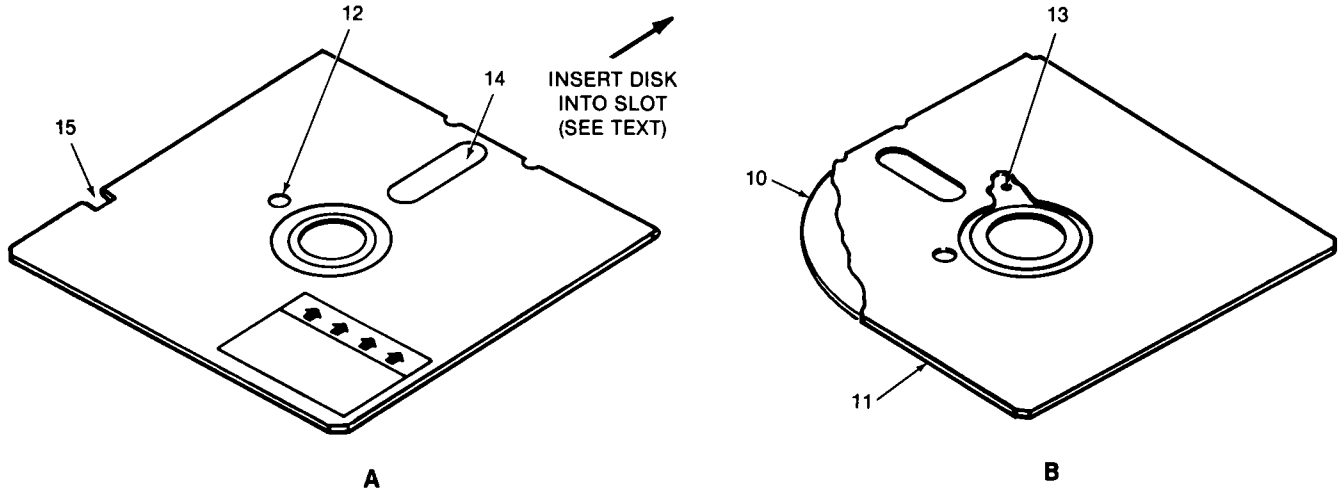


Fig. 1-5. Typical floppy disk.

ered with opaque tape, writing is disabled. Note the proper way to insert the disk (see Fig. 1-5A).

1.3 INSIDE THE VIC-1541

This section describes the insides of the VIC-1541 and basic maintenance consisting of disassembly, changing device numbers, and reassembly.

1.3.1 Disassembly and Identification of Subassemblies

WARNING

Before attempting to disassemble this disk drive, remove the ac line cord and any serial bus cables. Failure to do so could result in damage to the disk drive or personal, possibly fatal injury.

The subassemblies that make up the 1540, 1541, and 1542 may be seen in Figs. 1-6, 1-7, and 1-8, respectively. Table 1-3 identifies these subassemblies and parts. Refer to the table and the applicable illustration for the model you are disassembling. Below is a procedure to dismantle the disk drive completely. In practice, disassemble the disk drive only as far as is necessary to accomplish the maintenance you wish to perform.

To remove the top cover (Item 16) from the bottom cover (Item 17), turn the disk drive upside down and remove four screws (Item 18) using a Phillips screwdriver. Then gently lift the disk drive out of the top cover.

To remove the RFI shield (Item 19), remove two screws (Item 20) and two lockwashers (Item 21). (**Note:** In some units, the screws (Items 20, 30, and 32) and lockwashers (Items 21, 31, and 33) are all one piece.)

Lift the left-hand side of the RFI shield slightly to allow the dimples on the right-hand side to clear their mating holes. Before lifting the RFI shield clear of the disk drive, check to see if the wiring is threaded through the square hole on the right-hand side of the RFI shield; if so, disconnect the connector (Item 22) and lift the RFI shield clear of the disk drive.

Table 1-3. Subassemblies of the VIC-1541

ITEM	FIGURE	DESCRIPTION
16	1-6, 1-7, 1-8	Top Cover
17	1-6, 1-7, 1-8	Bottom Cover
18	1-6, 1-7, 1-8	Screws
19	1-6, 1-7, 1-8	RFI Shield
20	1-6, 1-7, 1-8	Screws
21	1-6, 1-7, 1-8	Lockwashers
22	1-6, 1-7, 1-8	Connector (female)
23	1-6, 1-7, 1-8	Screws
24	1-6, 1-7, 1-8	Disk Controller PC Board
25	1-6, 1-7, 1-8	Connector (female), Data
26	1-6, 1-7, 1-8	Connector (female), AC
27	1-6, 1-7, 1-8	Connector (female)
28	1-6, 1-7, 1-8	Connector (female)
29	1-6, 1-7, 1-8	Connector (female)
30	1-6, 1-7, 1-8	Screws
31	1-6, 1-7, 1-8	Lockwashers
32	1-6, 1-7, 1-8	Screws
33	1-6, 1-7, 1-8	Lockwashers
34	1-6, 1-7, 1-8	Frame
35	1-6, 1-7, 1-8	Drive Unit
36	1-6, 1-7, 1-8	Screws

To remove the bottom cover (Item 17), disconnect the connector (Item 22), then remove six screws (Item 23). Lift the disk drive assembly out of the bottom cover. To remove the disk controller PC board (Item 24), disconnect five connectors (Items 25 through 29) and remove five screws (Item 30) and five lockwashers (Item 31) from the top of the disk controller PC board. Remove two screws (Item 32) and two lockwashers (Item 33) from the right-hand side of the frame (Item 34). Carefully lift the disk controller PC board off of the frame.

To remove the drive unit (Item 35), remove two screws (Item 36) from the right-hand side of the frame, and two screws (Item 36) from the left-hand side of the frame. Carefully lift the drive unit up and forward to clear mounting tabs on the frame.

1.3.2 Changing Device Numbers

The device number is used to address a peripheral. Just as a piece of mail is sent to a specific house identified by an address, data is sent to a specific peripheral identified by an address or device number. The VIC-1541 is factory configured for device #8. If more than one VIC-1541 is to be connected to the serial bus, the additional drive(s) will require different device number(s).

Fig. 1-9 illustrates a system with two VIC-1541s on line at the same time. VIC-1541(A)

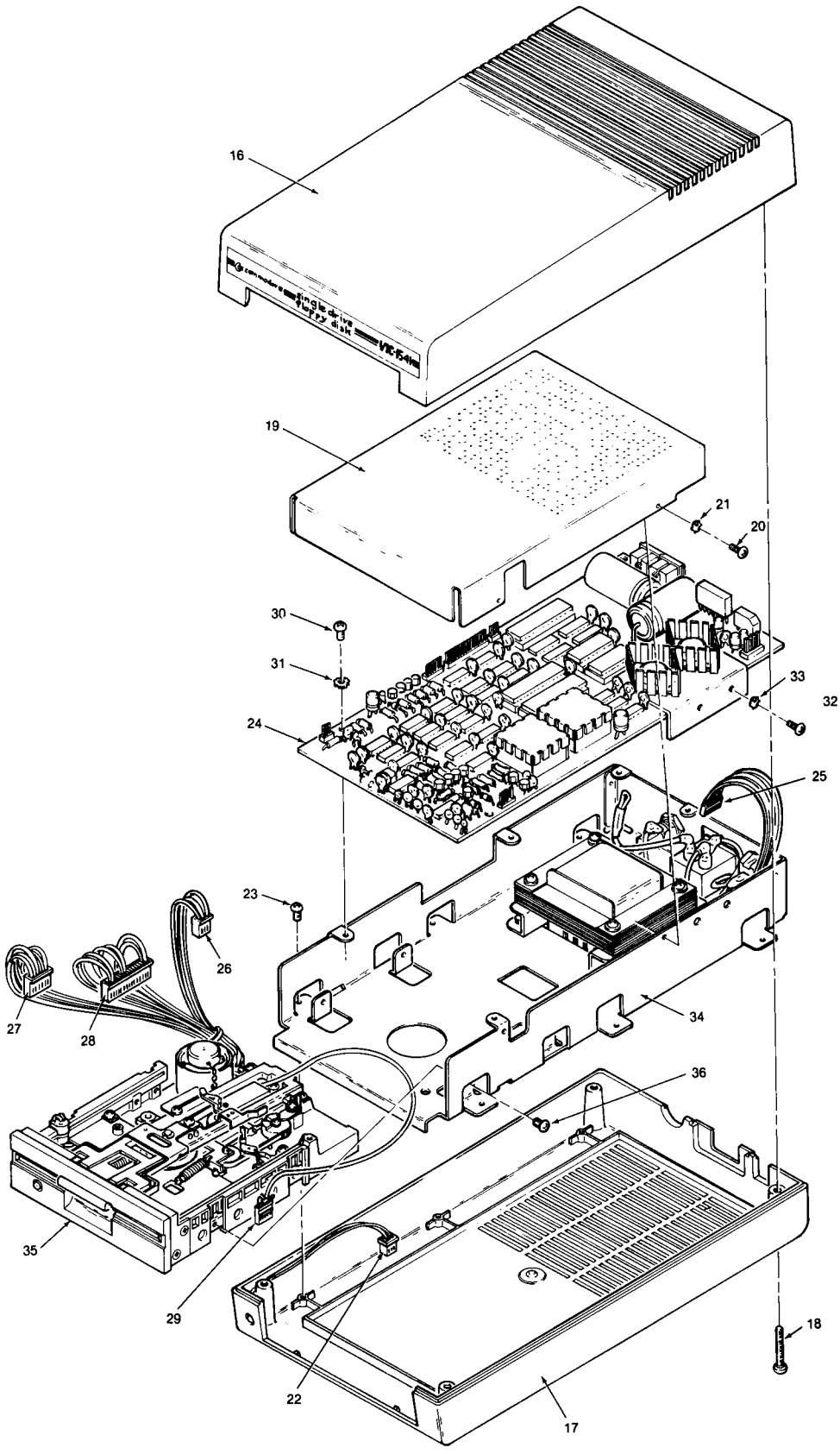


Fig. 1-6. Exploded view of Model 1540.

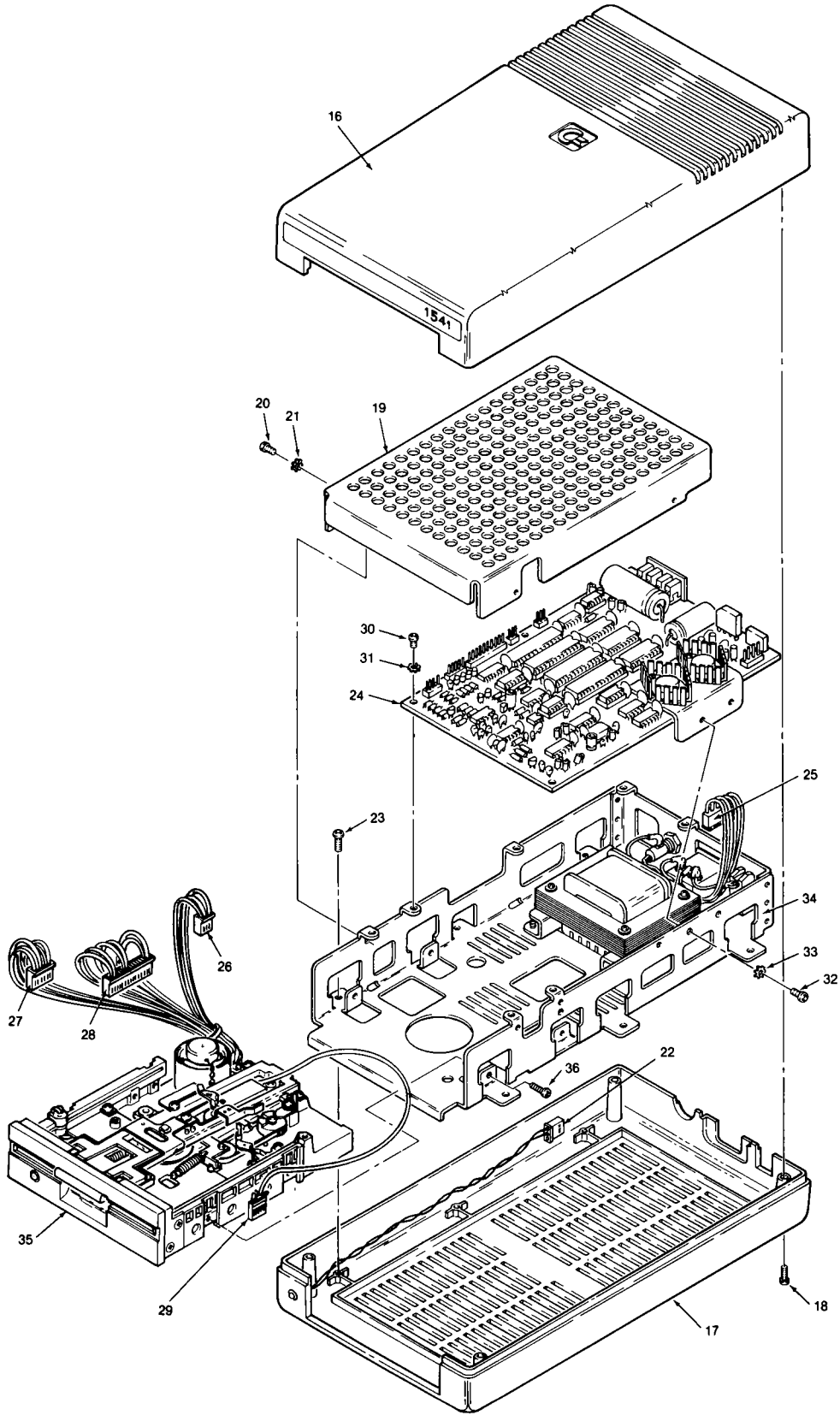


Fig. 1-7. Exploded view of Model 1541.

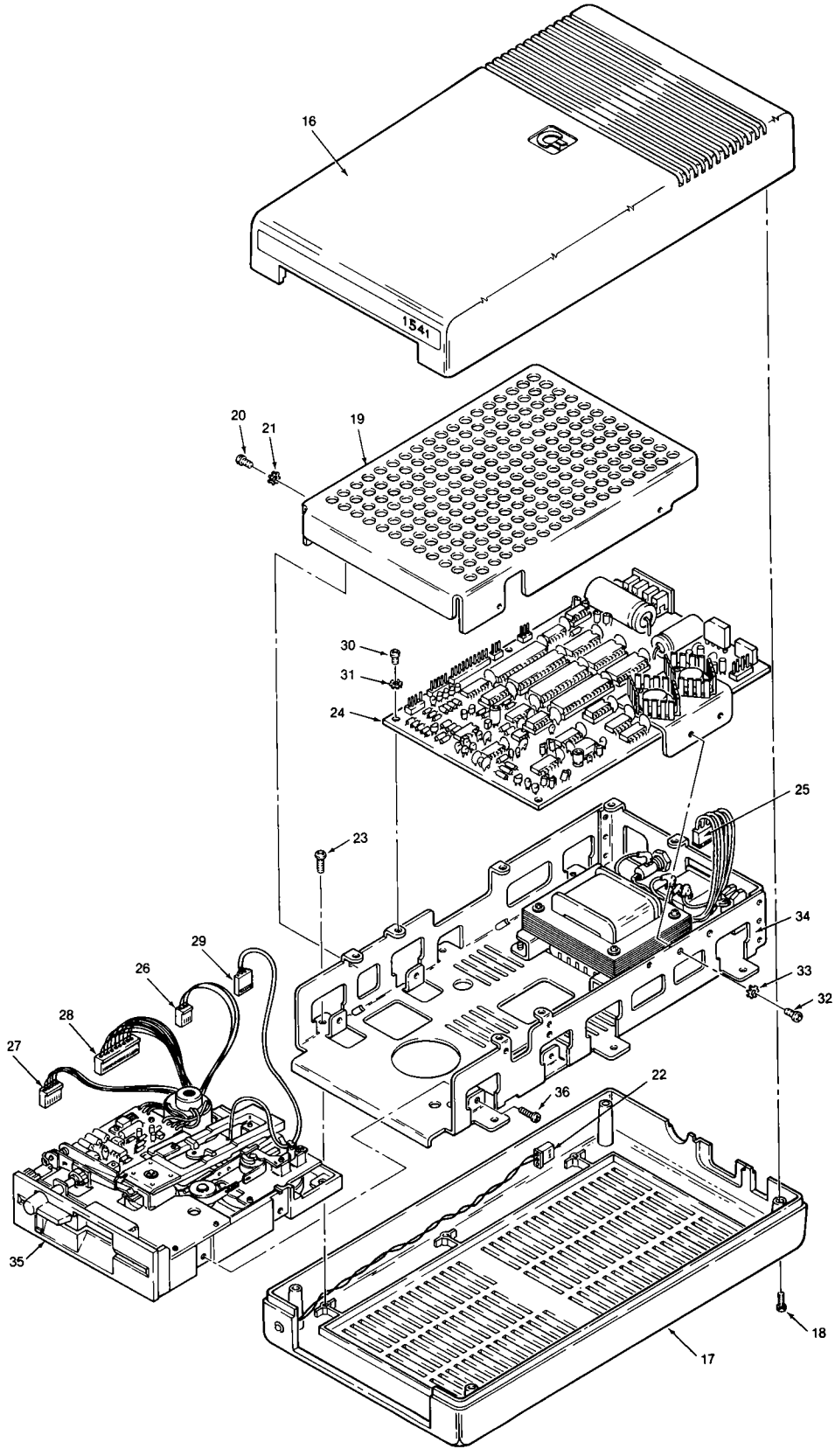


Fig. 1-8. Exploded view of Model 1542.

is configured for device #8 and VIC-1541(B) is configured for device #9. This configuration is called "daisy chaining." The data goes into a peripheral on one serial bus connector, then out the other serial bus connector to the next peripheral, and so on. The peripheral that is being addressed acts upon the data. Peripherals that are not addressed simply pass the data on to the next peripheral.

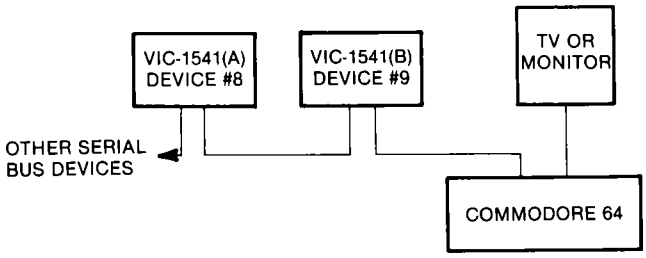


Fig. 1-9. Multiple disk drive configuration.

To illustrate the difference in commands required for two or more disk drives, assume that VIC-1541(A) and VIC-1541(B) each contain a blank floppy disk that is to be formatted. To format the floppy disk in drive (A) the command shown in Fig. 1-10 could be used.

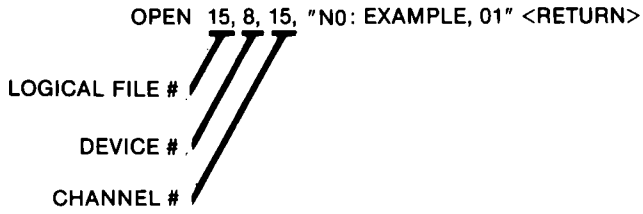


Fig. 1-10. Format command, drive A.

To format the floppy disk in drive (B), the command shown in Fig. 1-11 could be used.

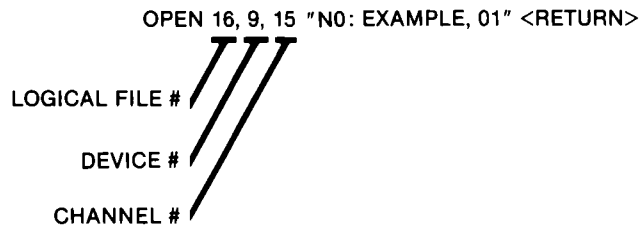


Fig. 1-11. Format command, drive B.

Notice that the device number and the logical file number change. The device number in Fig. 1-11 changes to 9 in order to address VIC-1541(B). The logical file number in this figure has also changed because logical file #15 is already opened and assigned to device #8 in Fig. 1-10. If logical file #15 were closed between Figs. 1-10 and 1-11, then the command in Fig. 1-11 could have used logical file #15 instead of logical file #16.

The VIC-1541 may be configured as either device #8, #9, #10, or #11. At least one VIC-1541 should be configured as device #8, because most prepackaged software assumes that configuration. To change the device number, proceed as follows:

1. Remove the top cover and the RFI shield from the VIC-1541. (Refer to Section 1.3.1, "Disassembly and Identification of Subassemblies.")
2. Locate the low-order programming pad (Item 37) and the high-order programming pad (Item 38). These programming pads may be located using Fig. 1-12 for the 1540, Fig. 1-13 for the 1541, and Fig. 1-14 for the 1542.
3. Item 37 and/or Item 38 may be cut to change the device number. Use Table 1-4 to determine which pads to cut for the device number desired. Use a sharp knife and cut the silver-colored conductor only enough to break continuity. Use care to avoid cutting the adjacent pathwork. (**Note:** If you wish to repair a path cut previously, solder a short bare wire between the pads, as shown in Fig. 1-15.)
4. Reassemble the VIC-1541 as described in Section 1.3.3.

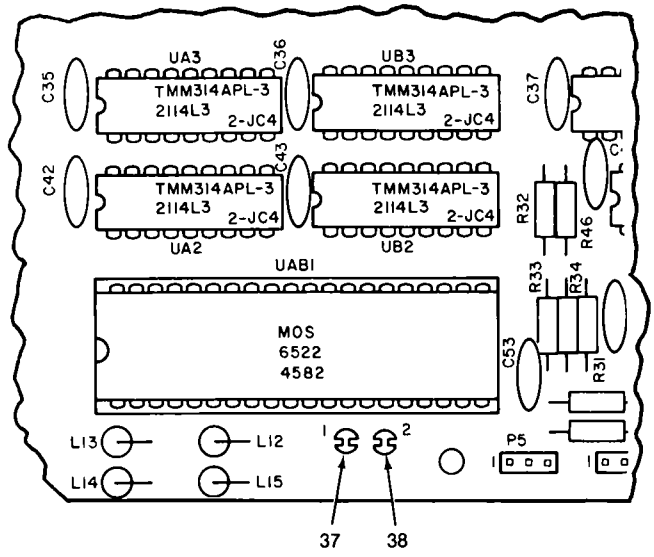


Fig. 1-12. Location of programming pads, Model 1540.

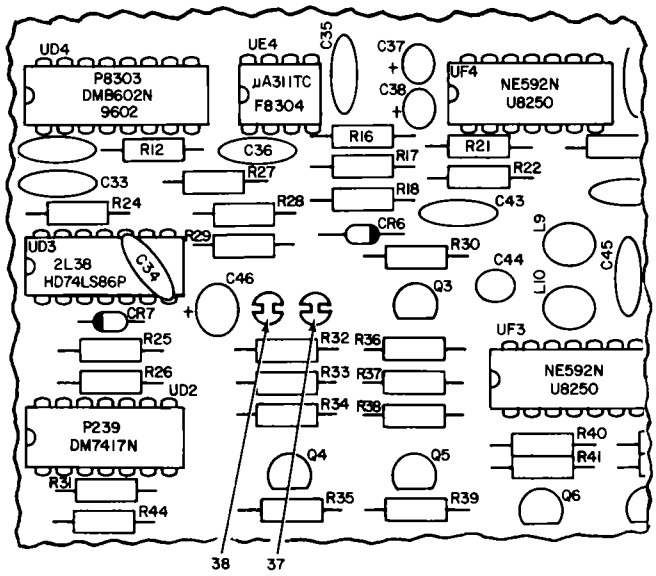


Fig. 1-13. Location of programming pads, Model 1541.

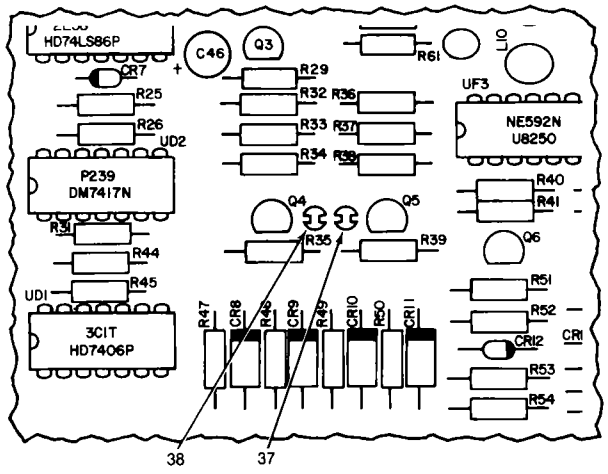


Fig. 1-14. Location of programming pads, Model 1542.

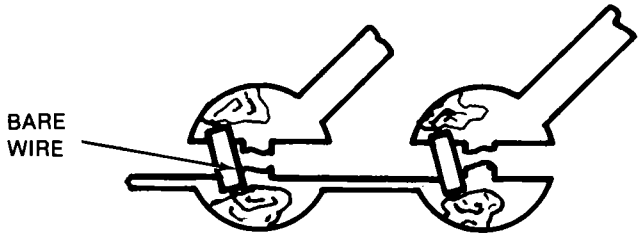


Fig. 1-15. Repairing cut programming pads.

1.3.3 Reassembly

The following procedure to reassemble the VIC-1541 assumes that the disk drive is completely disassembled down to the subassembly level. Reassemble as is necessary for the maintenance you performed. Refer to Fig. 1-16 to reassemble the 1540, Fig. 1-17 to reassemble the 1541, and Fig. 1-18 to reassemble the 1542. Refer to Table 1-5 for definitions of item numbers.

Table 1-4. Selecting Device Number

DEVICE NO.	PROGRAMMING PADS	
	LOW ORDER (ITEM 37)	HIGH ORDER (ITEM 38)
8	Not Cut	Not Cut
9	Cut	Not Cut
10	Not Cut	Cut
11	Cut	Cut

Table 1-5. Reassembly of the VIC-1541

ITEM	FIGURE	DESCRIPTION
16	1-16, 1-17, 1-18	Top Cover
17	1-16, 1-17, 1-18	Bottom Cover
18	1-16, 1-17, 1-18	Screws (4)
19	1-16, 1-17, 1-18	RFI Shield
20	1-16, 1-17, 1-18	Screws (2)
21	1-16, 1-17, 1-18	Lockwashers
22	1-16, 1-17, 1-18	Connector (female), LED
23	1-16, 1-17, 1-18	Screws (6)
24	1-16, 1-17, 1-18	Disk Controller PC Board
25	1-16, 1-17, 1-18	Connector (female), Data
26	1-16, 1-17, 1-18	Connector (female), AC
27	1-16, 1-17, 1-18	Connector (female)
28	1-16, 1-17, 1-18	Connector (female)
29	1-16, 1-17, 1-18	Connector (female)
30	1-16, 1-17, 1-18	Screws (5)
31	1-16, 1-17, 1-18	Lockwashers
32	1-16, 1-17, 1-18	Screws (2)
33	1-16, 1-17, 1-18	Lockwashers
34	1-16, 1-17, 1-18	Frame
35	1-16, 1-17, 1-18	Drive Unit
36	1-16, 1-17, 1-18	Screws
39	1-16, 1-17, 1-18	Connector (male), Data
40	1-16, 1-17, 1-18	Connector (male), AC
41	1-16, 1-17, 1-18	Connector (male)
42	1-16, 1-17, 1-18	Connector (male)
43	1-16, 1-17, 1-18	Connector (male)
44	1-16, 1-17, 1-18	Connector (male), LED

To mount the drive unit (Item 35) to the frame (Item 34), slide the drive unit into the front of the frame over the mounting tabs. When the drive is pushed back to its seating position, slide the drive unit down, guiding the mounting tabs into the recessed areas on the sides of the drive. Use great care to prevent damage to the fragile parts of the drive unit, such as the drive belt or the metal head-positioning band. Before securing the drive unit, be sure that no wires are pinched between the drive

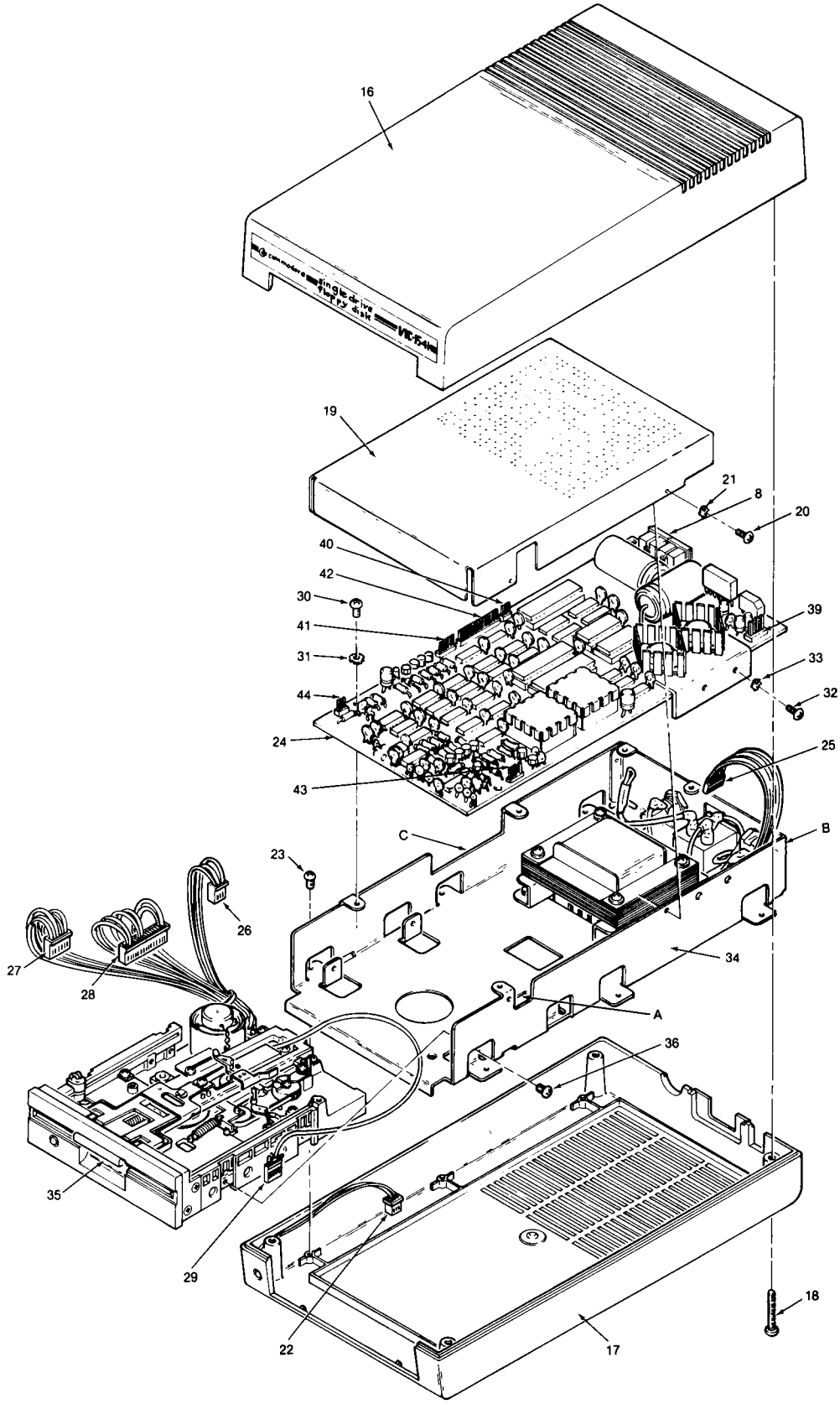


Fig. 1-16. Reassembly of Model 1540.

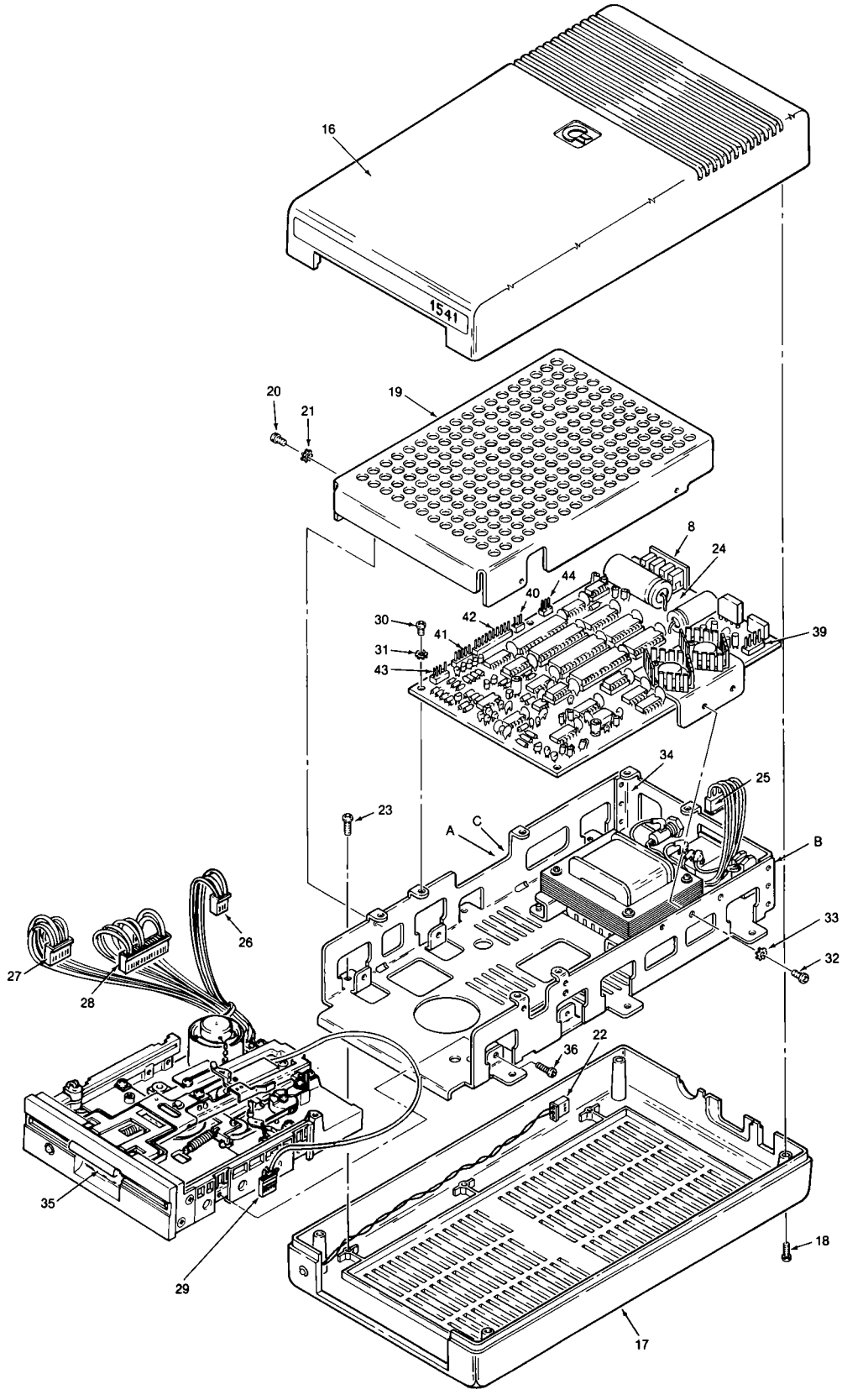


Fig. 1-17. Reassembly of Model 1541.

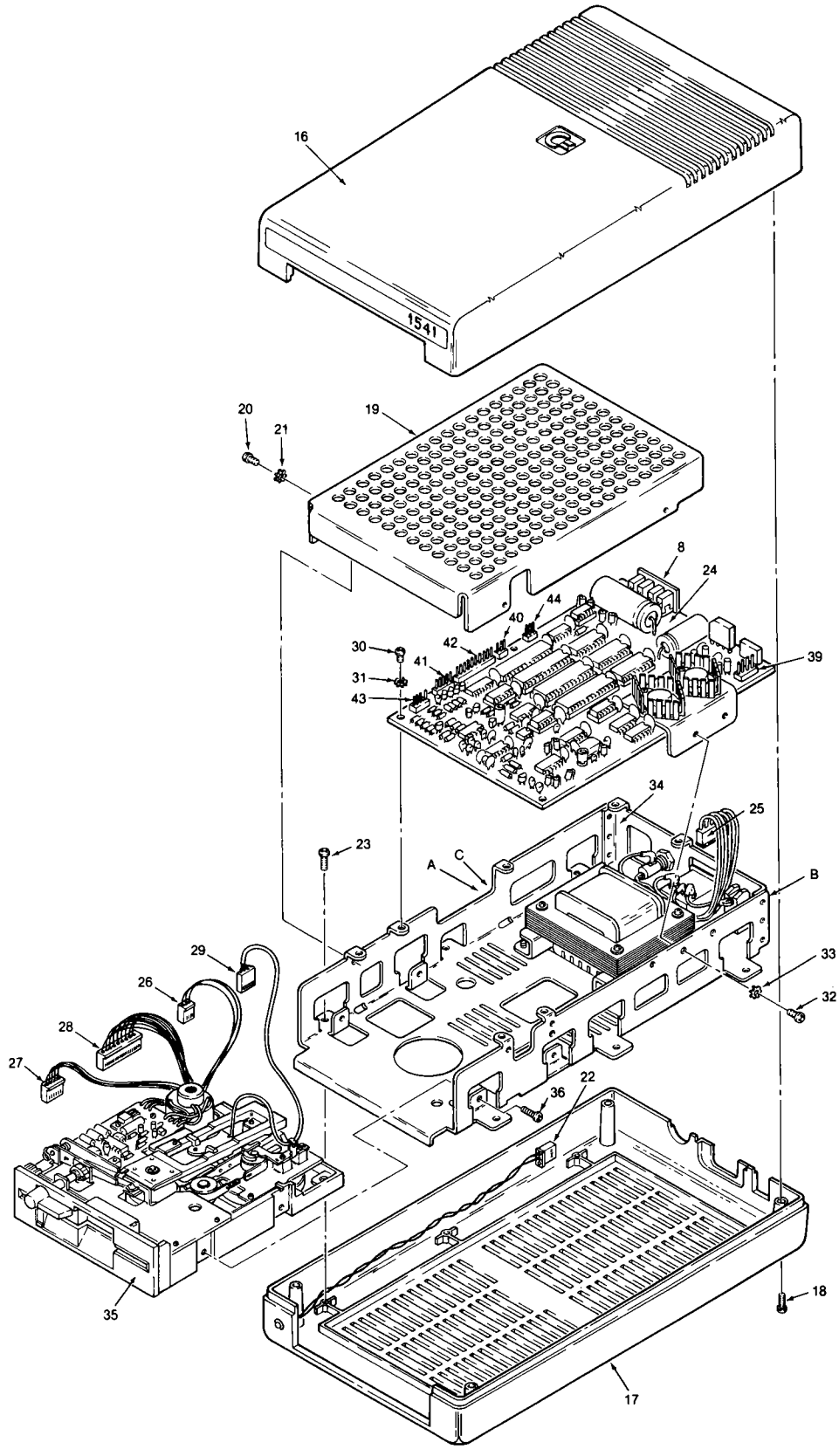


Fig. 1-18. Reassembly of Model 1542.

unit and the frame. Secure the drive unit using two screws (Item 36) on the right-hand side of the drive unit, and two screws (Item 36) on the left-hand side of the drive unit.

To install the disk controller PC board (Item 24), proceed as follows: Drape the cable bearing the connector (Item 29) into rectangular slot "A" so that the connector is outside of the frame. Drape the wire bundle bearing the connector (Item 25) over the corner of the frame marked "B" so that the connector is outside of the frame. Drape the remaining wires bearing three connectors (Items 27, 28, and 29) into the slot marked "C" so that the connectors are outside of the frame.

Note: Be sure to follow the order described here for securing the screws. To tighten in the reverse order might damage the PC board. Also, do not overtighten the screws.

Position the PC board as shown in the appropriate figure; secure it with two screws (Item 32) and two lockwashers (Item 33) through the holes in the right-hand side of the frame. Be careful to avoid pinching the wires between the frame (Item 34) and the heat sink on the PC board. Secure the PC board with five screws (Item 30) and five lockwashers (Item 31). Be careful to avoid pinching the wires between the frame and the PC board.

Connect the five female connectors (Items 25 through 29) to their mating male connectors (Items 39 through 43, respectively). On Models 1540 and 1542, these connectors are oriented so that the slotted side should face the center of the PC board. On Model 1541 only, the slots of one connector (Item 29) face away from the PC board (see Fig. 1-19).

To install the bottom cover (Item 17), place the frame (Item 34) into the bottom cover (Item 17); secure it with six screws (Item 23). Do not overtighten the screws, or the holes in the bottom cover may become stripped. Use care to ensure that the wires are not pinched between the frame and the bottom cover.

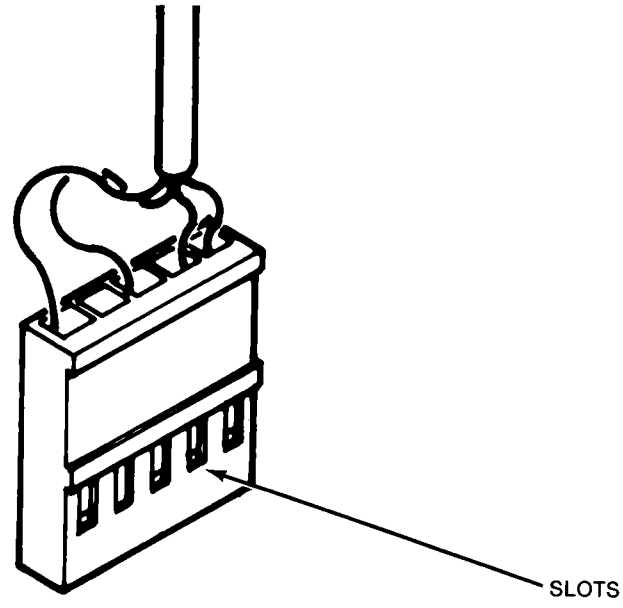


Fig. 1-19. Slotted side of connector.

To install the RFI shield (Item 19), first connect the female connector (Item 22) to its mating male connector (Item 44).

Note: On Model 1540, thread the connector (Item 22) through the square hole in the left-hand side of the RFI shield (Item 19).

Position the dimples in the RFI shield into their mating holes on the right-hand side of the frame (Item 34); position the holes on the left-hand side of the RFI shield over the threaded holes in the left-hand side of the frame, and secure with two screws (Item 20) and two lockwashers (Item 21). Take care that no wires are pinched between the RFI shield and the frame.

To install the top cover (Item 16), position the top cover over the disk drive and the bottom cover (Item 17). Turn the disk drive and the top cover upside down and secure with four screws (Item 18). Be careful to avoid pinching the wires between the top cover and the bottom cover.

CHAPTER 2

Theory of Operation

In this chapter, we will look at the theory of operation of the VIC-1541 on three different levels. As with peeling successive layers from an onion, each level of theory reveals more information about the VIC-1541 than the level before it.

2.1 OVERALL THEORY OF OPERATION, ALL MODELS

We start our discussion with Section 2.1.1, "Oversimplified Theory of Operation." This section is the most accessible, but it is also the least detailed. Section 2.1.2 "Simplified Theory of Operation," contains more detailed theory. The third level of theory of operation is presented in Sections 2.2, 2.3, and 2.4. A fourth, and the most detailed, level of theory of operation is presented in Chapter 7, "Advanced Theory of Operation." This level is based on the schematic of the VIC-1541.

2.1.1 Oversimplified Theory of Operation

The VIC-1541 can be thought of as having three basic parts—the power supply, the disk controller, and the drive unit. All three parts are required to write to or read from a floppy disk. Refer to Fig. 2-1 for the following discussion.

The power supply converts the ac line voltage into a usable, regulated, and filtered dc voltage that is used to power the disk controller. The disk controller decodes commands and performs other data transfers over the serial bus. The disk controller also operates the mechanical drive unit and performs housekeeping, such as maintaining the

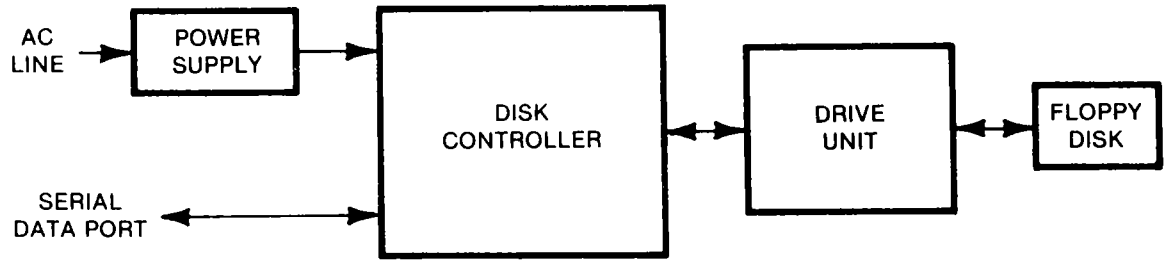


Fig. 2-1. Oversimplified block diagram of the VIC-1541.

floppy disk's directory and block availability map (BAM). The drive unit is predominantly a mechanical assembly that rotates the floppy disk and performs the actual recording and reading of the floppy disk. The drive unit is to a floppy disk as a tape deck is to a cassette tape.

2.1.2 Simplified Theory of Operation

Refer to Fig. 2-2 for a block diagram illuminating the following discussion. The power supply consists of a section of rectifiers that convert the ac line voltage to +9 volts dc and +16 volts dc. The outputs of the rectifiers are applied to the voltage regulators. The voltage regulators, in turn, produce output voltages of +5 volts and +12 volts. The voltage regulators also produce a switched output of +11 volts, which is turned off during power up and power down operations in order to prevent inadvertent writing on the disk.

The disk controller can be subdivided into eight functional circuits—computer, timing, optics, track select, drive motor servo circuit, encoder/decoder, read, and write. The *computer circuit* manages the rest of the disk drive, using a program in firmware referred to as the disk operating system (DOS). The DOS program contains routines to control the drive unit and the serial bus, as well as routines to perform the housekeeping for the floppy disk. The serial bus circuits contain line drivers, line receivers, and other logic that interfaces the computer circuit with the serial bus. The serial bus circuits also generate the reset signal for the computer circuit.

The *timing circuit* produces the microprocessor clock and the encoder/decoder clock. The microprocessor clock is a fixed 1-MHz square wave, which is the time standard for the computer. The encoder/decoder clock is a variable frequency clock that determines the data transfer rate between the disk controller and the drive unit. The frequency of the encoder/decoder clock is selected by the computer circuit.

The *optics circuit* drives the access/error LED and a photoemitter in the drive unit. The photoemitter passes light through the write protect notch in the floppy disk onto a photodetector. A signal from the photodetector is applied to the optics circuit in the disk controller. The optics circuit converts this signal to a level that is compatible with the computer circuit.

The *track select circuit* decodes position information from the computer circuit and buffers this information before applying it to the four-phase head positioning motor. Additionally, an output from the track select circuit is applied to the drive motor servo circuit. This digital signal is used to turn the drive motor on or off.

The *drive motor servo circuit* regulates the rotational speed of the floppy disk. The drive motor has a built-in tachometer which provides a feedback signal to the drive motor servo circuit. The drive motor servo circuit uses this signal to measure the speed of the disk and, in turn, adjusts the motor current accordingly until the feedback indicates that the disk is operating at the correct speed.

The *encoder/decoder circuit* is used for both read and write operations. In the write mode, the encoder/decoder converts an 8-bit byte from the computer circuit into a serial stream of precisely spaced transitions. The spacing between transitions determines whether the bit is a "1" or a "0." The encoder/decoder only cares about the transition spacing, not the direction of the transitions. In the read mode, the encoder/decoder converts the stream of transitions into an 8-bit byte and applies this byte to the computer. The parallel data which is transferred to and from the computer circuit is further encoded. The DOS must perform additional encoding and decoding to generate or recover the actual data being stored.

The transitions out of the encoder/decoder are applied to the *write circuit* which provides the necessary drive current for the recording process. This current is applied to the read/write head in the drive unit. In turn, the read/write head records these transitions on the floppy disk.

In the read mode, the read/write head senses the transitions on the surface of the floppy disk and applies these transitions to the read circuit. The *read circuit* amplifies these low-level currents to a level suitable for the encoder/decoder circuit. The output of the read circuit is applied to the encoder/decoder circuit and subsequently to the computer circuit.

2.2 MECHANICAL THEORY, MODELS 1540 AND 1541

This mechanical theory covers the theory of operation for the Alps drive unit which is used in

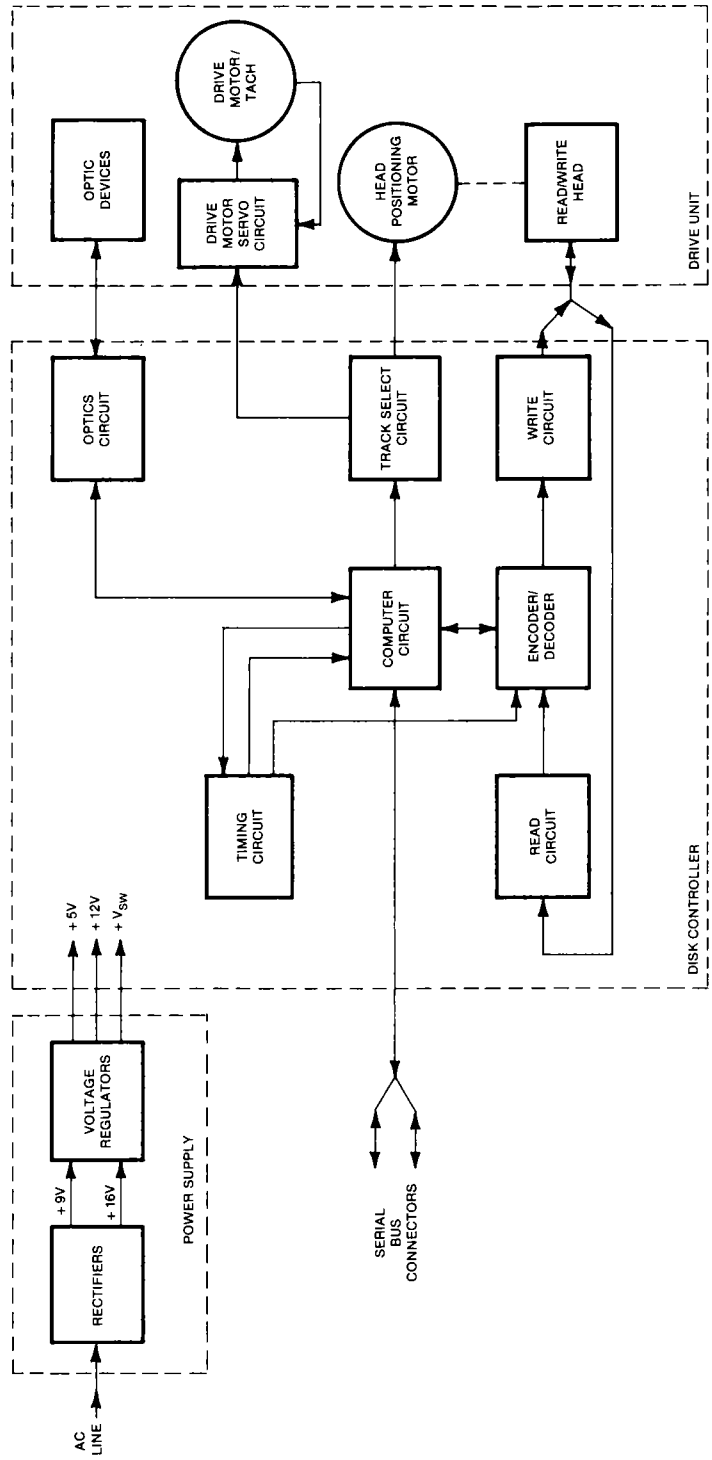


Fig. 2-2. Simplified block diagram of the VIC-1541.

the 1540 and 1541. If you have a 1542, which is equipped with a Newtronics drive unit, see Section 2.3, "Mechanical Theory, Model 1542."

2.2.1 Loading and Unloading

Refer to Table 2-1 and Fig. 2-3 for an illustration of the Alps drive unit. Every time a floppy disk is inserted into the Alps drive unit, four things happen:

1. The disk ejector is locked.
2. Read/write pressure is applied.
3. Disk tension is set.
4. The floppy disk is held firmly against the drive hub.

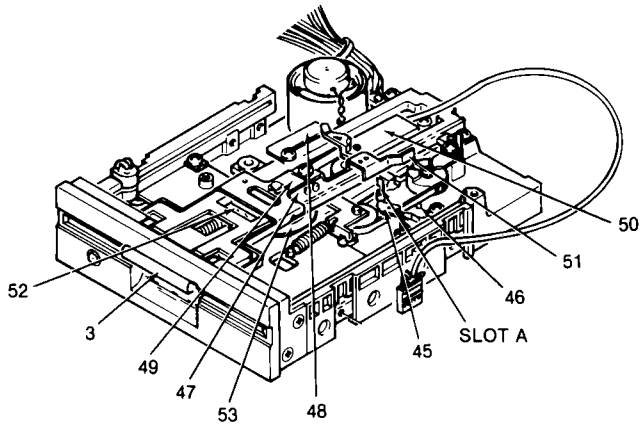


Fig. 2-3. Alps drive unit, loading and unloading.

Table 2-1. Alps Drive Unit, Loading and Unloading

ITEM	FIGURE	DESCRIPTION
3	2-3	Latch
45	2-3	Disk Ejector Arm
46	2-3	Ejector Arm Pin
47	2-3	Idler Hub Mount
48	2-3	Disk Tension Pad
49	2-3	Unloading Actuator
50	2-3	Pressure Pad Mount
51	2-3	Disk Ejector Trigger
52	2-3	Idler Hub
53	2-3	Drive Hub

When a floppy disk is inserted into the drive unit, the floppy disk will push back on the disk ejector arm (Item 45) until it reaches the ejector arm pin (Item 46), which holds the disk ejector arm into the locked position. After the disk is inserted, the operator presses down on the latch (Item 3), which lowers the idler hub mount (Item 47). As the idler hub mount is lowered, several other actions occur. The disk tension pad (Item 48) is moved into place, setting the disk tension. The unloading actuator (Item 49) is lowered, allowing the pressure pad mount (Item 50) to be lowered onto the floppy disk, setting the read/write head pressure. As the idler hub mount nears its seated position, the disk ejector trigger (Item 51) on the unloading actuator falls into slot "A" of the disk ejector arm. When the idler hub mount is fully seated, the latch (Item 3) retains the idler hub mount in its seated position. In this position, the idler hub (Item 52) sandwiches the media between it and the drive hub (Item 53). The floppy disk is then ready to be accessed.

To unload the floppy disk, the latch is pressed, causing the idler hub mount to pop up. As the idler hub mount moves upward, the disk tension pad is raised, removing the disk tension. The unloading actuator is also raised, lifting the pressure pad mount and tripping the disk ejector arm. The ejector arm then moves up over the ejector arm pin and snaps forward, kicking the floppy disk approximately 1 to 2 inches out the front of the drive unit.

2.2.2 Track Selection

Refer to Table 2-2 and Figs. 2-4 and 2-5 for illustration of the following discussion. The mechanical track selection system allows the inward/outward position of the read/write head to be selected. The read/write head mount (Item 54) can move front to back on the head mount slide rails (Item 55). The read/write head mount is attached to the track select band (Item 56). The track select band is secured to the stepping motor drive wheel (Item 57) and wrapped around the track position idler pulley (Item 58). The tension of both the track position idler pulley and of the track select band are set by a spring (Item 59). The stepping motor (Item 60) rotates in 1.8° increments. The stepping motor shaft is connected to the stepping motor drive wheel; as the stepping motor shaft rotates, so does the stepping motor drive wheel. As the drive wheel rotates, the track select band also rotates, causing the read/write head mount to move inward or outward. Overrunning the outermost track is prevented by the track No. 1 stop (Item 61).

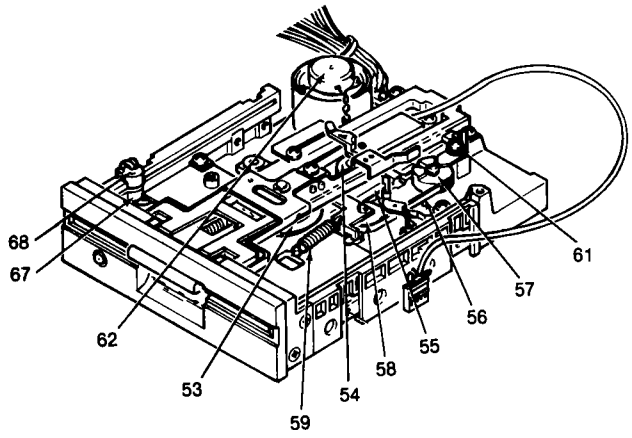


Fig. 2-4. Alps drive unit, top view.

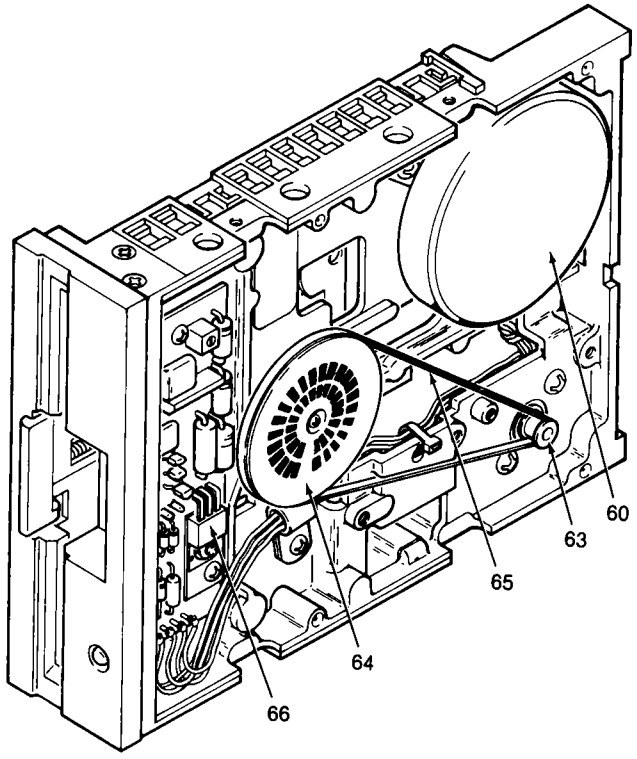


Fig. 2-5. Alps drive unit, bottom view.

Table 2-2. Alps Drive Unit, Track Selection

ITEM	FIGURE	DESCRIPTION
54	2-4	Read/Write Head Mount
55	2-4	Head Mount Slide Rails
56	2-4	Track Select Band
57	2-4	Stepping Motor Drive Wheel
58	2-4	Track Position Idler Pulley
59	2-4	Spring
60	2-5	Stepping Motor
61	2-4	Track No. 1 Stop

2.2.3 Drive System

Refer to Table 2-3 and Figs. 2-4 and 2-5 for illustration of the following discussion. The mechanical drive system rotates the drive hub (Item 53) and, therefore, the floppy disk itself.

The drive motor/tachometer (Item 62) contains a motor and a tachometer on a common shaft. The tachometer section is used to generate speed information for feedback purposes. The motor section drives the tachometer and the drive pulley (Item 63), which turns the flywheel (Item 64) via the drive belt (Item 65). The flywheel smooths out the motion of the drive hub (Item 53). The flywheel may also contain a timing disk for the purpose of disk speed calibration. Disk speed is regulated by the drive motor servo circuit (Item 66).

Table 2-3. Alps Drive Unit, Drive System

ITEM	FIGURE	DESCRIPTION
53	2-4	Drive Hub
62	2-4	Drive Motor/Tachometer
63	2-5	Drive Pulley
64	2-5	Flywheel
65	2-5	Drive Belt
66	2-5	Drive Motor Servo Circuit

2.2.4 Write Protect System

Refer to Table 2-4 and Fig. 2-4 for illustration of the following discussion. The write protect system consists of an LED (Item 67) and a phototransistor (Item 68). When a floppy disk is inserted with the write protect notch uncovered, the LED transmits light to the phototransistor, activating the phototransistor. The phototransistor then informs the disk controller that writing to the floppy disk is permitted. If, however, the write protect notch is covered, the light beam is interrupted and the disk controller will not permit writing to the floppy disk.

Table 2-4. Alps Drive Unit, Write Protect System

ITEM	FIGURE	DESCRIPTION
67	2-4	LED
68	2-4	Phototransistor

2.3 MECHANICAL THEORY, MODEL 1542

This mechanical theory covers the theory of operation for the Newtronics drive unit, which is

used in the 1542. If you have a 1540 or a 1541, which is equipped with an Alps drive unit, see Section 2.2, "Mechanical Theory, Models 1540 and 1541."

2.3.1 Loading and Unloading

Refer to Table 2-5 and Fig. 2-6 for illustration of the following discussion. Every time a floppy disk is inserted into the Newtronics drive unit, three things happen:

1. Read/write pressure is applied.
2. Disk tension is set.
3. The floppy disk is held firmly against the drive hub.

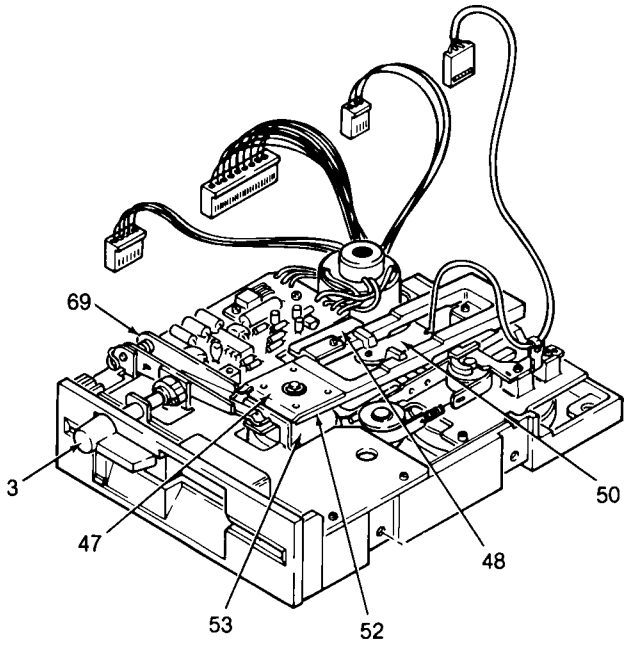


Fig. 2-6. Newtronics drive unit, loading and unloading.

Table 2-5. Newtronics Drive Unit, Loading and Unloading

ITEM	FIGURE	DESCRIPTION
3	2-6	Latch
47	2-6	Idler Hub Mount
48	2-6	Disk Tension Pad
50	2-6	Pressure Pad Mount
52	2-6	Idler Hub
53	2-6	Drive Hub
69	2-6	Loading Actuator

After you insert the disk, rotate the latch (Item 3) clockwise, which causes the loading actuator (Item 69) to press down the idler hub mount (Item 47). As the idler hub mount is depressed, the disk tension pad (Item 48) is moved into place, setting the disk tension. Also, the pressure pad mount (Item 50) is lowered onto the floppy disk, setting the read/write head pressure. Finally, the idler hub (Item 52) sandwiches the media between it and the drive hub (Item 53). The floppy disk is then ready to be accessed.

To unload the disk, rotate the latch counterclockwise, causing the loading actuator to release the idler hub mount. When the idler hub mount is released, the disk tension is removed, the pressure pad mount is lifted from the floppy disk, and the idler hub releases the disk. The floppy disk may then be removed.

2.3.2 Track Selection

Refer to Table 2-6 and Figs. 2-7 and 2-8 for illustration of the following discussion. The mechanical track selection system allows the inward/outward position of the read/write head to be selected. The read/write head mount (Item 54) can move front to back on the head mount slide rails (Item 55). The read/write head mount is attached to the track select band (Item 56). The track select band is secured to the stepping motor drive wheel (Item 57) and wrapped around the track position idler pulley (Item 58). The tension of both the track position idler pulley and of the track select band are set by a spring (Item 59). The stepping motor (Item 60) rotates in 1.8° increments. The stepping motor shaft is connected to the stepping motor drive wheel; as the stepping motor shaft rotates, so does the drive wheel. As the drive wheel rotates, the track select band also rotates, causing the read/write head mount to move inward or outward. Overrunning the outermost track is prevented by the track No. 1 stop (Item 61).

Table 2-6. Newtronics Drive Unit, Track Selection

ITEM	FIGURE	DESCRIPTION
54	2-7	Read/Write Head Mount
55	2-7	Head Mount Slide Rails
56	2-7	Track Select Band
57	2-7	Stepping Motor Drive Wheel
58	2-7	Track Position Idler Pulley
59	2-7	Spring
60	2-8	Stepping Motor
61	2-7	Track No. 1 Stop

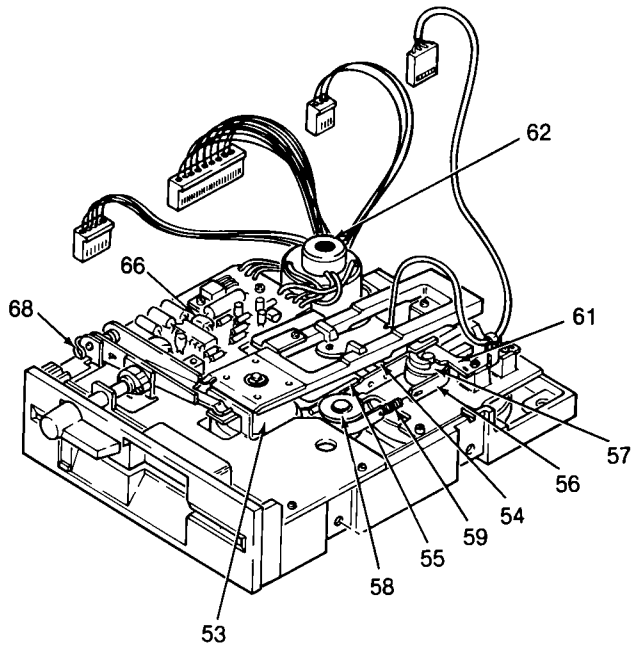


Fig. 2-7. Newtronics drive unit, top view.

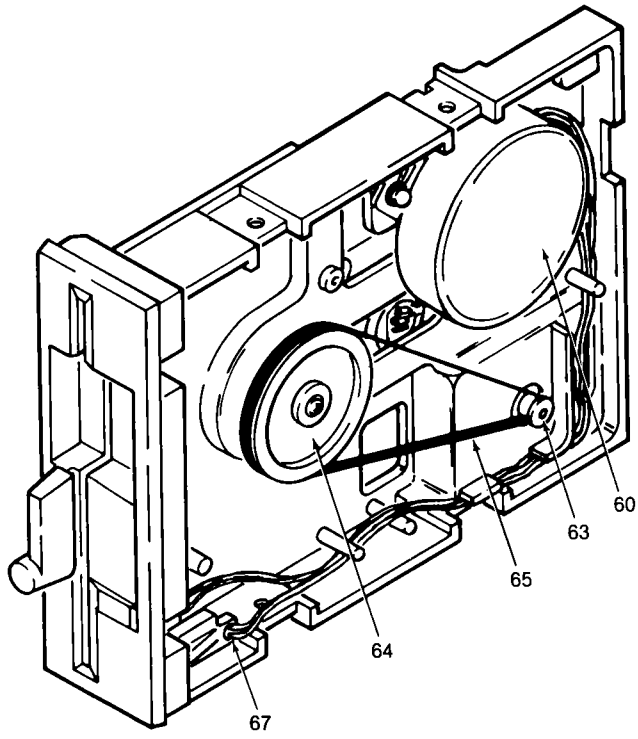


Fig. 2-8. Newtronics drive unit, bottom view.

2.3.3 Drive System

Refer to Table 2-7 and Figs. 2-7 and 2-8 for illustration of the following discussion. The mechanical drive system rotates the drive hub (Item 53) and, therefore, the floppy disk itself.

The drive motor/tachometer (Item 62) contains a motor and a tachometer on a common shaft. The tachometer section is used to generate speed information for feedback purposes. The motor section drives the tachometer and the drive pulley (Item 63), which turns the flywheel (Item 64) via the drive belt (Item 65). The flywheel smooths out the motion of the drive hub (Item 53). The flywheel may also contain a timing disk for the purpose of disk speed calibration. Disk speed is regulated by the drive motor servo circuit (Item 66).

Table 2-7. Newtronics Drive Unit, Drive System

ITEM	FIGURE	DESCRIPTION
53	2-7	Drive Hub
62	2-7	Drive Motor/Tachometer
63	2-8	Drive Pulley
64	2-8	Flywheel
65	2-8	Drive Belt
66	2-7	Drive Motor Servo Circuit

2.3.4 Write Protect System

Refer to Table 2-8 and Figs. 2-7 and 2-8 for illustration of the following discussion. The write protect system consists of an LED (Item 67) and a phototransistor (Item 68). When a floppy disk is inserted with the write protect notch uncovered, the LED transmits light to the phototransistor, activating the phototransistor. The phototransistor then informs the disk controller that writing to the floppy disk is permitted. If, however, the write protect notch is covered, the light beam is interrupted and the disk controller will not permit writing to the floppy disk.

Table 2-8. Newtronics Drive Unit, Write Protect System

ITEM	FIGURE	DESCRIPTION
67	2-8	LED
68	2-7	Phototransistor

2.4 ELECTRONIC THEORY, ALL MODELS

The following theory of operation applies to all models. The discussion is based on the use of a detailed block diagram. For component level theory discussed on the basis of the schematic, see Chapter 7, "Advanced Theory of Operation."

2.4.1 Power Supply

Refer to Fig. 2-9 for illustration pertaining to the following discussion. The power supply converts the ac line voltage to regulated dc voltages of +5 volts and +12 volts. The power supply also provides a switched supply which drives the read and write circuits.

The ac line current enters the power switch at the rear of the frame assembly. The output of the power switch is applied to the fuse, which provides overload protection, then to the transformer. The transformer provides two lower ac voltages of 9 volts and 16 volts ac. The 9 volts ac from the transformer is applied to the +5-volt rectifier, which is a full-wave rectifier. The dc voltage out of the +5-volt rectifier is filtered by the +5-volt filter, then applied to the +5-volt regulator. The +5-volt regulator regulates the voltage to +5 volts ±0.25 volt.

The 16 volts ac from the transformer passes through the +12-volt rectifier, +12-volt filter, and +12-volt regulator, which operates similarly to the +5-volt leg of the power supply. Outputs of both the +5-volt and +12-volt regulators are applied to the reliability switch. The reliability switch filters the +12-volt supply, and it turns this filtered supply on or off depending on the status of the +5-volt line. If the +5-volt line is less than +4 volts dc, then the output of the reliability switch ($+V_{SW}$) is turned off. If the +5-volt line is greater than +4 volts, the output of the reliability switch is turned on. Since the output of the reliability switch drives the read and write circuits, this feature prevents accidental writing or erasure of data at power-up, power-down or, whenever the +5-volt logic supply is unreliable.

2.4.2 Computer Circuit

Refer to Fig. 2-10 for illustration pertaining to the following discussion. The computer circuit consists of a 6502 central processing unit (CPU), 2K bytes of random-access memory (RAM), 16K bytes of read-only memory (ROM), serial bus interface, disk controller versatile interface adapter (VIA), write logic, and address decoder. The address decoder enables communications between the CPU and the device or memory whose address appears on the address bus. (See Table 2-9 for device addresses.) The 16K ROM contains the DOS firmware, which is actually a list of instructions that the CPU executes in a logical order. The 2K of RAM is used by the CPU to store temporary data such as read or write data, commands, stack information, and so on. The write logic places the RAM into the write mode when instructed to do so by the CPU.

Table 2-9. Device Addresses

DEVICE	ADDRESS (HEX)
RAM	0000-07FF
Serial Bus VIA	1800-180F
Disk Controller VIA	1C00-1C0F
ROM	C000-FFFF

The serial bus interface consists of line drivers, line receivers, a VIA, and other logic that is necessary to interface the CPU with the serial bus. The serial bus interface also generates the reset signal for the CPU. The disk controller VIA interfaces the CPU with the encoder/decoder, track select, optics, and timing circuits.

The computer circuit coordinates the activities of each of the individual circuits within the VIC-1541. Other functions of the computer circuit include decoding and responding to serial bus commands, error reporting, and housekeeping of the floppy disk directory and BAM.

2.4.3 Timing Circuit

Refer to Fig. 2-11 for illustration pertaining to the following discussion. The timing circuit gener-

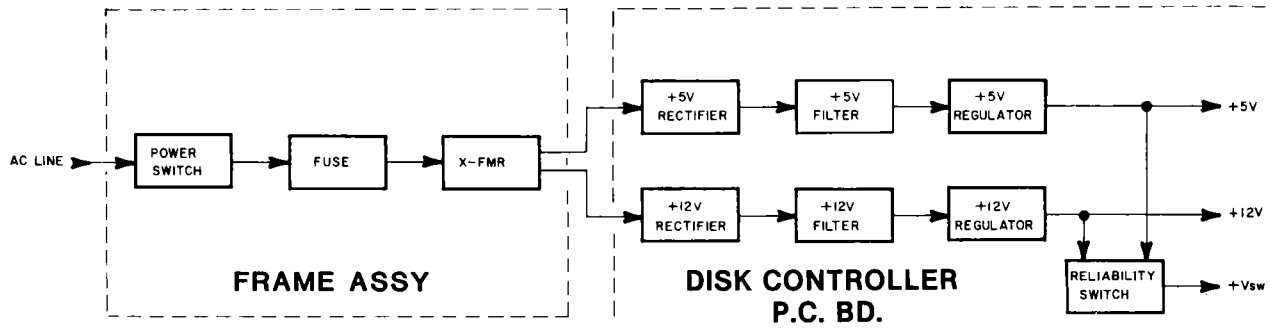


Fig. 2-9. Block diagram of the power supply.

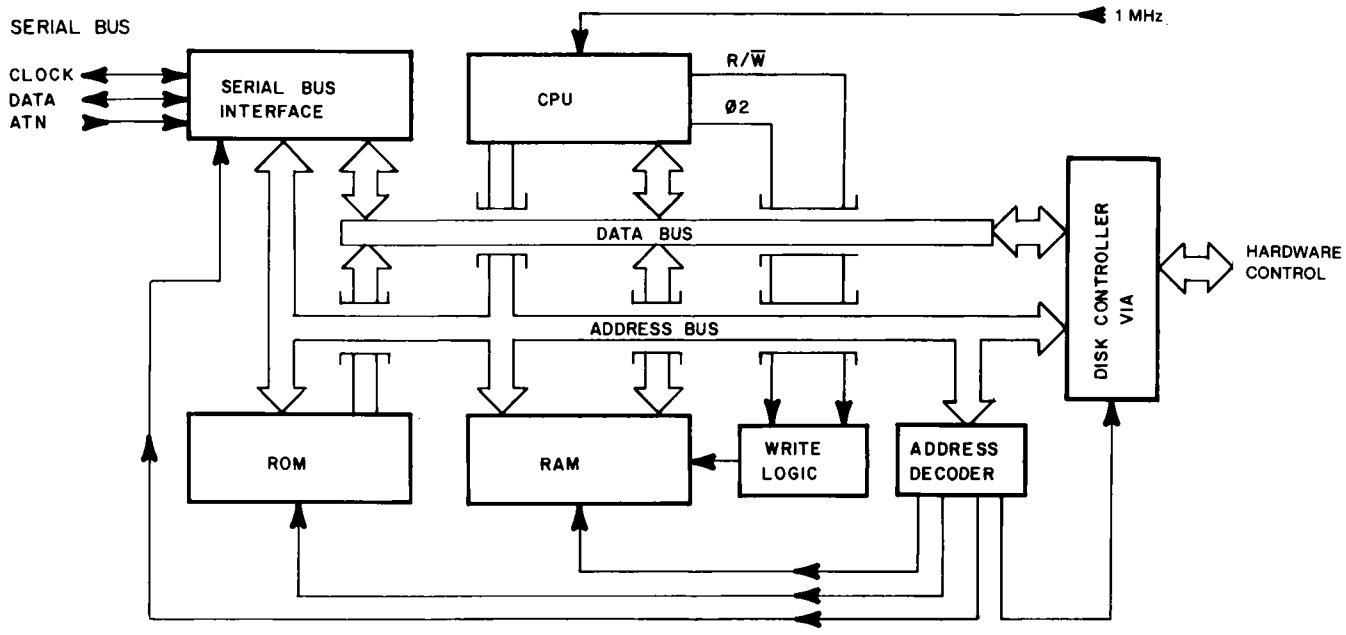


Fig. 2-10. Block diagram of the computer circuit.

ates a 1-MHz clock for the CPU and a variable (1.0 MHz to 1.2307 MHz) clock for the encoder/decoder circuit. The heart of the timing circuit is the 16-MHz oscillator. The 16-MHz square-wave output of the 16-MHz oscillator is applied to the ÷16 frequency divider and the ÷n frequency divider. The ÷16 frequency divider divides the 16-MHz square wave by 16, yielding 1 MHz which is applied to the CPU. The ÷n frequency divider, or programmable frequency divider, provides the clock for the encoder/decoder circuit and may be reset to allow the phase of the encoder/decoder clock to be controlled. Floppy disks have fewer sectors per track on the innermost track (track No. 35) than on the outermost track (track No. 1). This variation in number of sectors per track keeps the bit density relatively constant throughout the writing surface of the disk. Each disk is divided into four zones, with each zone containing a unique number of sectors per track. The programmable divider has four possible output frequencies, with each frequency corresponding to one of the four zones on the floppy disk. In order to maintain fairly even bit densities, the encoder/decoder must be clocked at a faster rate when writing on the outer tracks than when writing on the inner tracks. This is because the outer surface of the disk is passing over the head more rapidly than the inner surface. Thus it is the encoder/decoder clock which determines how many sectors will fit on any given track.

The division factor of the programmable divider is controlled by the CLOCK SEL A and CLOCK SEL B lines from the computer circuit's disk controller VIA. Table 2-10 defines specific parameters for each line. The BIT SYNC input is used to maintain the phase relationship between read data and the encoder/decoder clock to within 62 nanoseconds.

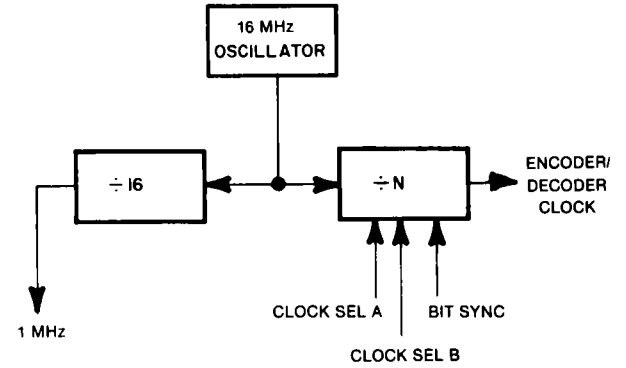


Fig. 2-11. Block diagram of the timing circuit.

Table 2-10. Timing Circuit Parameters

	ZONE 1	ZONE 2	ZONE 3	ZONE 4
CLOCK SEL A	1	0	1	0
CLOCK SEL B	1	1	0	0
Division Factor	13	14	15	16
Encoder/Decoder Clock Freq. (MHz)	1.2307	1.1428	1.0666	1.00
Sectors per Track	21	20	18	17
Track Numbers	1-17	18-24	25-30	31-35

2.4.4 Track Select Circuit

Refer to Fig. 2-12 for illustration pertaining to the following discussion. The desired track is physically selected by positioning the read/write head using the four-phase stepping motor, which rotates 1.8° per step. To move the read/write head one track, the stepping motor must rotate 3.6°, or two steps. In order to step the read/write head inward, each of the four ϕ(N) lines must be energized in ascending order (i.e., ϕ1, ϕ2, ϕ3, ϕ4, ϕ1, ϕ2 . . . etc.). To step the read/write head outward, each of the four ϕ(N) lines must be energized in descending order (i.e., ϕ4, ϕ3, ϕ2, ϕ1, ϕ4, ϕ3 . . . etc.). The phase decoder of Fig. 2-12 is a two- to four-line decoder which decodes the binary phase number from the computer circuit that is present on lines PHASE SEL A and PHASE SEL B. The decoded output is applied to the appropriate buffer (i.e., ϕ1 buffer, ϕ2 buffer, ϕ3 buffer, or ϕ4 buffer). The 2-bit binary numbers on the phase select lines are incremented to step the head in and decremented to step the head out.

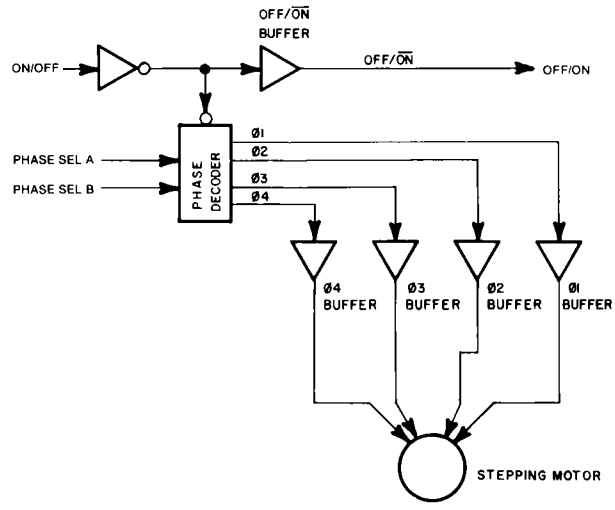


Fig. 2-12. Block diagram of the track select circuit.

Notice that the on/off signal from the computer circuit is inverted before being applied to the active-low enable input of the phase decoder. To enable the phase decoder and subsequently the stepping motor, the on/off line from the computer circuit must be high. If this line is low, then the stepping motor is allowed to rotate freely. The output of the inverter is applied to a buffer and, in turn, the output of the buffer is applied to the drive motor speed circuit. Only one line from the computer circuit controls the on or off status of both the stepping motor and the drive motor. Both motors are turned on or off at the same time; they may not operate independently.

2.4.5 Drive Motor Servo Circuit, Models 1540 and 1541

Refer to Fig. 2-13 for illustration pertaining to the following discussion. The drive motor servo circuit for the Alps drive controls the rotational speed of the floppy disk. The off/on signal from the track select circuit is applied to gate the motor driver in the drive motor servo circuit. When this line is low, the motor driver buffers the signal from the speed controller and applies this buffered signal to the drive motor/tachometer. When the off/on line is high, the motor is turned off.

As the motor turns, so does the tachometer, which is housed on the back of the motor case. The tachometer behaves like an alternator, providing an ac signal whose output frequency and voltage are proportional to the rotational speed of the motor/tachometer. The output of the tachometer is applied to the signal rectifier in the drive motor servo circuit. The output of the signal rectifier is a full-wave rectified signal that is applied to the speed controller IC. This IC monitors the output of the signal rectifier and adjusts the motor current as needed to maintain proper disk rpm. Because some floppy disks exhibit more drag than others, this circuit ensures proper disk speed from one disk to another.

2.4.6 Drive Motor Servo Circuit, Model 1542

Refer to Fig. 2-14 for illustration pertaining to the following discussion. The drive motor servo circuit for the Newtronics drive unit regulates the rotational speed of the floppy disk. The off/on line from the track select circuit is applied to the governor IC. When this line is high, the governor turns off the drive motor. When this line is low, the governor applies current to the drive motor/tachometer via the motor driver.

As the motor turns, so does the tachometer, which is housed on the back of the motor case. The tachometer behaves like an alternator, providing an ac signal whose output frequency and voltage are proportional to the rotational speed of the motor/tachometer. The output of the tachometer is ap-

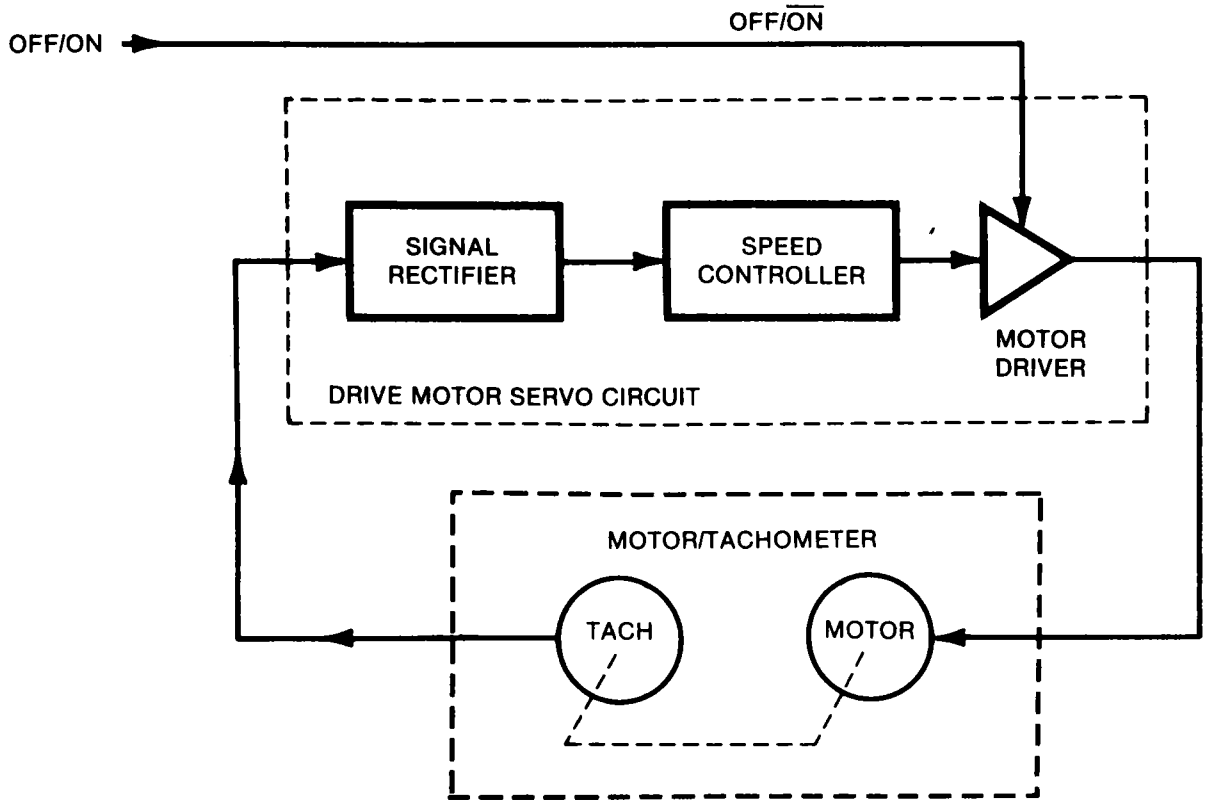


Fig. 2-13. Block diagram of the drive motor servo circuit, Models 1540 and 1541.

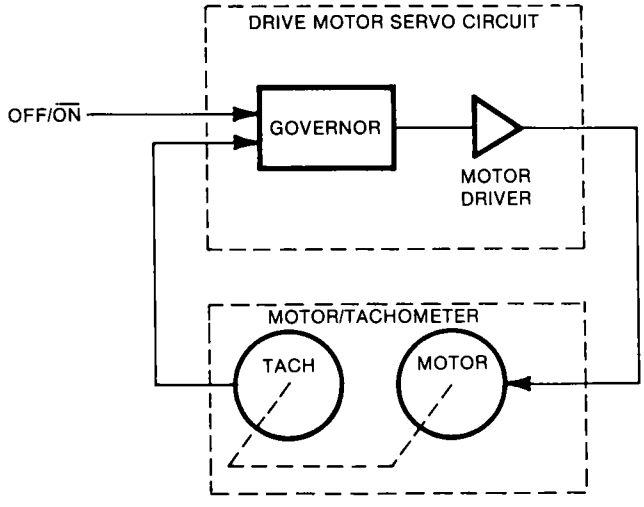


Fig. 2-14. Block diagram of the drive motor servo circuit, Model 1542.

plied to the governor in the drive motor servo circuit. The governor monitors the signal from the tachometer and adjusts the motor current as needed to maintain proper disk rpm. Because some floppy disks exhibit more drag than others, this circuit ensures proper disk speed from one disk to another.

2.4.7 Read Circuit

Refer to Fig. 2-15 for illustration pertaining to the following discussion. The read circuit senses and screens data before it is applied to the encoder/decoder. The data on the surface of the floppy disk is sensed by the read/write head and applied to the first video amplifier via a diode switch. The state of the diode switch is determined by the write circuit. When the write circuit is disabled, the diode switch gates data from the read/write head to the first video amplifier. When the write mode is enabled, the diode switch allows data to pass from the write circuit to the read/write head without affecting the read circuits. The data from the read/write head is approximately a scant 7 millivolts. After amplification by the first video amplifier, this signal is increased to 350 millivolts. The 350-millivolt signal out of the first video amplifier is applied to the second video amplifier, which has a voltage gain of approximately 10. The 3.5-volt dif-

ferential signal out of the second video amplifier is applied to a comparator, which converts the received data to a transistor-transistor logic (TTL) signal. This TTL signal is applied to the valid pulse detector. The valid pulse detector is disabled in the write mode. The valid pulse detector only passes pulses that are at least 2.5 microseconds in duration. Any pulses less than 2.5 microseconds are suppressed; this effectively rejects any noise above 400 kHz. The output of the valid pulse detector is applied to the edge detector. In turn, the edge detector produces a narrow pulse on low-to-high and high-to-low transitions of the received data. These narrow pulses marking the transitions of the data on the disk are applied both to the timing circuit as bit sync in order to synchronize the encoder/decoder clock with the transitions, and to the encoder/decoder as data for decoding.

2.4.8 Encoder/Decoder Circuit

Refer to Fig. 2-16 for illustration pertaining to the following discussion. The encoder/decoder circuit converts the serial stream of transitions into eight parallel bits of data for the computer circuit and vice versa. First we will discuss the decoding operation. Assume that the read/write line from the computer circuit is high (read mode). The decoder converts the serial stream of transitions into a serial data stream as well as generating a shift clock. Each bit cell out of the decoder is four encoder/decoder clock pulses long. If a transition (or input pulse on the data line from the read circuit) occurs at the beginning of a bit cell, then that bit cell is a logic 1. If no transition (or input pulse on the data line from the read circuit) occurs, then that bit cell is a logic 0. Both the serial data and shift clock out of the decoder are applied to a 10-bit serial-to-parallel converter (or "shift register"). Additionally, the shift clock is applied to the bit counter. When enabled by the computer circuit, the bit counter signals the computer circuit that eight bits have been shifted and the data in the serial-to-parallel converter is ready to be transferred to the computer circuit. The first eight bits of the 10-bit serial-to-parallel converter are gated by the 8-bit buffer to port A on the disk controller VIA. All 10 bits out of the 10-bit serial-to-parallel converter are applied to the sync detector. At least 10 "ones" in succession are recognized as a block sync. The block sync resets or, "synchronizes," the bit counter and also informs the computer that the start of a header or data block has been detected.

This scheme has certain limitations to it. One such limitation is that in order to reduce data bandwidth, not more than two "zeros" may occur in succession. As stated earlier, a zero is a bit cell with no transition at the start of it. To read 256 consecutive bytes of $00 would require 2048 bit cells in which no data occurred. Another limitation is the fact that data such as #$FF followed by $C0 would be detected as a sync mark. To overcome these limitations, group code recovery (GCR) is used. With GCR, five bits of recorded data are required to make one 4-bit nibble of intelligence (see Table 2-11). Using GCR coding, there will never be more than two zeros in succession. Notice that $FF is

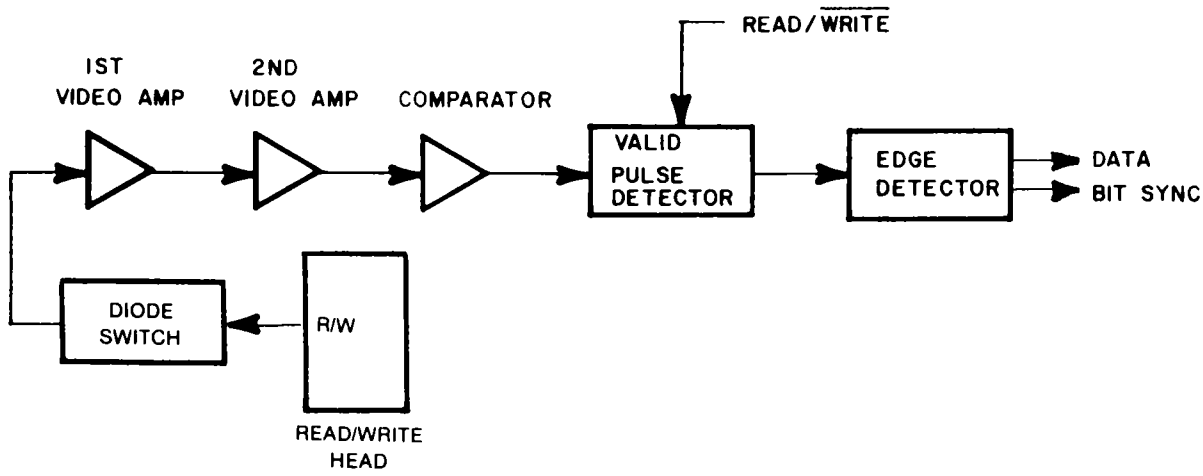


Fig. 2-15. Block diagram of the read circuit.

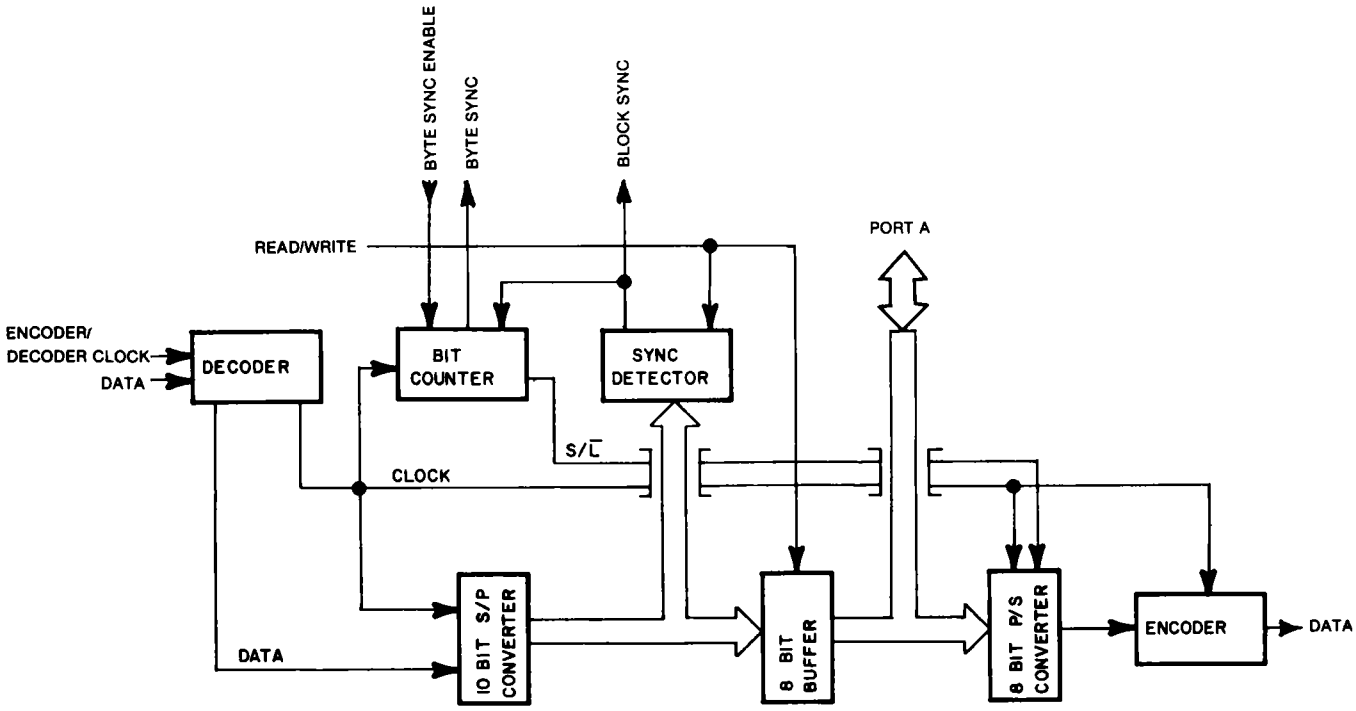


Fig. 2-16. Block diagram of the encoder/decoder circuit.

written as 1010110101, and $C0 is written as 0110101010; this does not conflict with a sync mark of 10 "ones" in succession. Encoding and decoding GCR is performed in the computer circuit's RAM, not by the encoder/decoder. The encoder/decoder performs the encoding and decoding of the transitions to GCR-coded data, and vice versa.

Table 2-11. GCR Coding

NIBBLE (HEX)	GCR
0	01010
1	01011
2	10010
3	10011
4	01110
5	01111
6	10110
7	10111
8	01001
9	11001
A	11010
B	11011
C	01101
D	11101
E	11110
F	10101

Now we will discuss the encoding operation. For encoding, the read/write line from the computer circuit is low (write mode). With the read/write line low, the read circuit is disabled, so there are no pulses (or data) from the read circuit to the decoder. However, the decoder does produce a shift clock at one-fourth the encoder/decoder clock rate.

Additionally, with the read/write line low, both the sync detector and 8-bit buffer are disabled. Data to be written is applied from port A of the disk controller VIA to the 8-bit parallel-to-serial converter (shift register). The shift clock is applied to the 8-bit parallel-to-serial converter and the bit counter. After eight serial bits are shifted out of the parallel-to-serial converter, the bit counter loads the next eight parallel bits into the parallel-to-serial converter using the S/L line. Additionally, the bit counter informs the computer circuit to get the next byte ready for the following cycle. Both the shift clock and the serial data out of the serial-to-parallel converter are applied to the encoder. The encoder generates a transition when a serial "one" is coincident with a shift clock. No transition is generated for a serial "one." The data from the encoder is applied to the write circuit.

2.4.9 Write Circuit

Refer to Fig. 2-17 for illustration pertaining to the following discussion. The write circuit supplies

the read/write head with proper bias currents to record data onto the floppy disk. Assume that the read/write line is low (write mode). The read/write line from the computer circuit and the write protect signal from the photodetector in the drive unit are applied to the write logic. If the floppy disk is not write protected and the read/write line is low, then the write protect output to the computer circuit will indicate that writing to the floppy disk is permitted. Additionally, the write logic will turn on the bias switches which provide bias to the read/write head and also biases the diode switch into the write mode via the read/write head.

The write logic also turns on the amp enable switch. In turn, the amp enable switch supplies power to the differential write amp. Data from the encoder/decoder is applied to the differential write amp, which generates the recording current. The output of the differential write amp is applied to the read/write head via the diode switch. These recording currents magnetically polarize the coating on the surface of the floppy disk. This recording process can be thought of as providing tiny magnets on the surface of the disk; these tiny magnets are later detected during the read or playback process.

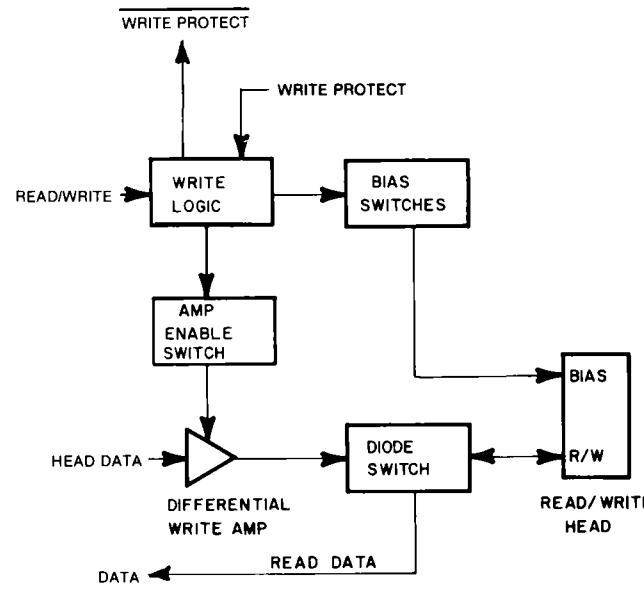


Fig. 2-17. Block diagram of the write circuit.

CHAPTER 3

Alignment

This chapter contains alignment procedures which apply to all models of the VIC-1541. Section 3.1 introduces a utility program that may be used to exercise the electromechanical functions of the drive unit. This program may be used for troubleshooting or for alignment setup. Section 3.2 is devoted to disk speed calibration. Section 3.3 contains two read/write head alignment procedures. The first procedure is a shop-quality alignment using an oscilloscope and a cat's eye alignment disk. The second procedure is not a shop-quality alignment, but, in a pinch, will get your disk drive working with a minimum of test equipment or it will enable you to recover data from a floppy disk which has been written during an out-of-alignment condition. Section 3.4 is the procedure to adjust the track No. 1 stop.

3.1 EXERCISING THE DRIVE UNIT

The program shown in Fig. 3-1 is a utility program that allows you to exercise the electromechanical functions of the disk drive. By user command, this program will step the head in, step the head out, turn the drive motor on, turn the drive motor off, and perform a bump (step out to track No. 1 stop). Store this program on cassette tape and/or disk. If your system has a cassette tape, store the program on tape because your disk drive may not be working when you need the program. If you do not have a second disk drive or cassette tape, you may have to reenter the program manually in order to troubleshoot your disk drive.

A few things should be noted about this program before attempting to enter it. A common mistake made by the novice is to use the invalid abbreviation **?#** in lieu of **PRINT#**. This condition generates a syntax error that is not easy to locate. The proper abbreviation for **PRINT#** is **P <SHIFT> R**. The instruction **PRINT #15** is abbreviated **P <SHIFT> R15**. Another source of confusion is the graphics characters in lines 60 through 110 and line 8000. In line 60, the graphics character after the first quote is obtained by pressing the f1 function key. This graphics character appears again in line 60 in the remark instruction. The remark instruction need not be typed in; it is there only for your benefit. Each of the lines that have graphics characters also have a remark instruction that defines the graphics characters. In line 60, the remark instruction indicates to press the f1 key to get the graphics character. In line 70, press f3 to get the graphics character; in line 80, press f5; and in line 90, press f7. To get the graphics character in line 100, press f2 (f2 is **<SHIFT>**

f1), and to get the graphics character in line 110, press f4 (f4 is **<SHIFT> f3**).

Line 8000 has two consecutive graphics characters. To get the first character, press CLR (CLR is **<SHIFT> CLR/HOME**). To get the next graphics character, press the cursor down key.

Refer to Table 3-1 for a description of the exerciser commands. This program may be used with formatted disks, alignment disks, or blank disks. Because it does not need the headers, the program will even work with no disk at all. The exerciser program keeps a record of the track number by adding or subtracting one-half track for each step-in or step-out command. It is important to note that if an adjustment is made or if the read/write head is physically moved by some means other than the stepping motor, the track displayed on the screen may not agree with the actual head position. To avoid any discrepancy, perform a bump (f2), which will bring the read/write head back to the track No. 1 stop and set the screen display to track No. 1. This program may be used for aligning, cleaning, testing, and troubleshooting the drive unit.

Table 3-1. Exerciser Commands

COMMAND	FUNCTION KEY
Step in 1 step (step up ½ track)	f1
Step out 1 step (step down ½ track)	f3
Turn drive motor on	f5
Turn drive motor off	f7
Perform bump	f2
Exit program	f4

3.2 CALIBRATING DISK RPM

The following procedure is used to calibrate the floppy disk rpm on all models of the VIC-1541. Before starting this step-by-step procedure, a few words about an alignment reference. Models 1540 and 1541, equipped with an Alps drive, have a timing disk adhered to the flywheel (see Fig. 3-2, Item 64). Under a fluorescent light, the timing marks on the timing disk appear to stop when the disk is rotating at the correct speed. A battery-operated fluorescent lamp will not work as a reference because the lamp must be powered by the ac line. If a fluorescent lamp is not available in your work area, you may use your TV or monitor. To use the TV/monitor as a reference, change the screen color to white using the following command:

```
POKE 53280,1:POKE 53281,1 <RETURN>
```

Then perform the adjustment in the light of the TV or monitor screen. There are a substantial number of Model 1542s, equipped with a Newtronics

```
10 OPEN15,8,15,"U+":T=1:M=0:GOSUB7000:GOSUB8000
15 B$="M-E"+CHR$(5)+CHR$(2)+CHR$(238)+CHR$(0)+CHR$(28)+"L"+CHR$(130)+CHR$(249)
16 C$="M-E"+CHR$(5)+CHR$(2)+CHR$(206)+CHR$(0)+CHR$(28)+"L"+CHR$(130)+CHR$(249)
40 A$="":FORX=631TO640:POKEX,0:NEXTX
50 GETA$:IFA$=""THEN50
60 IFA$="■"THEN130:REM"■"=F1
70 IF A$="■"THEN140:REM"■"=F3
80 IF A$="■"THENGOSUB150:GOTO40:REM"■"=F5
90 IF A$="■"THENGOSUB6000:GOTO40:REM"■"=F7
100 IF A$="■"THENGOSUB7000:GOSUB8000:GOTO40:REM"■"=F2
110 IF A$="■"THENGOSUB7000:GOSUB6000:END:REM"■"=F4
120 GOTO40
130 PRINT#15,B$:T=T+.5:M=1:GOSUB8000:GOTO40
140 PRINT#15,C$:T=T-.5:M=1:GOSUB8000:GOTO40
150 PRINT#15,"M-E"+CHR$(130)+CHR$(249):M=1:GOSUB8000:RETURN
6000 PRINT#15,"M-E"+CHR$(232)+CHR$(249):M=0:GOSUB8000:RETURN
7000 PRINT#15,"M-W"+CHR$(0)+CHR$(0)+CHR$(1)+CHR$(192):T=1
7010 FORX=1TO4000:NEXTX:IFM=1THENGOSUB150:RETURN
7020 IF M=0THENGOSUB8000:RETURN
8000 PRINT"■■STATUS:":PRINT"TRACK ";T:REM"■"=SHIFT CLR/HOME  "■"=CURSOR DOWN
8010 PRINT"MOTOR  ";:IFM=0THENPRINT"OFF":RETURN
8020 PRINT"ON":RETURN

READY.
```

Fig. 3-1. Exerciser program listing.

drive, that do not have timing disks (see Fig. 3-3, Item 64). Two procedures will remedy this. One option is to photocopy or trace Fig. 3-4, cut out the copy, and adhere the illustration to the flywheel, using rubber cement or two-sided tape only. Do not allow either the adhesive or the tape to interfere with the drive belt. The other option is to use a frequency counter as a reference. To do this, connect the frequency counter to pin 2 of the governor IC (see Fig. 3-3, Item 70). The disk is rotating at its proper speed when the frequency counter displays 367 Hz.

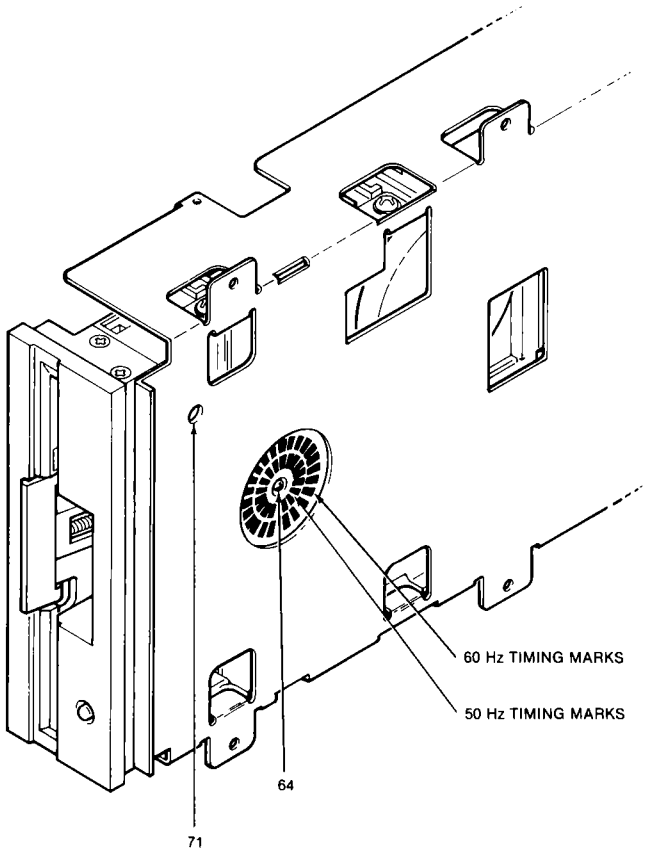


Fig. 3-2. Disk speed adjustment, Models 1540 and 1541.

To calibrate disk speed, perform the following procedure:

1. Remove all cables from the VIC-1541, especially the ac line cord.
2. Remove the top and bottom covers and the RFI shield in accordance with Section 1.3.1.
3. Prop the disk drive on its left-hand side as shown in Fig. 3-2. The left-hand edge may be propped up with a book or magazine.
4. Prepare the reference as described earlier in the text.
5. Connect the serial bus cable between the disk drive and the Commodore 64/VIC 20.
6. Connect the ac line cord between the disk drive and an ac outlet.

WARNING

Use extreme care to avoid contact with frame components. High ac voltage potentials are present during this procedure. These voltages may cause fatal injury.

7. Turn on the disk drive, the monitor, and any other peripherals.
8. Turn on the computer.
9. If you are using a VIC 20, enter the following command:

```
OPEN 15,8,15, "U:":CLOSE 15 <RETURN>
```

10. Load, or enter and then run the exerciser program of Section 3.1. Execute the drive motor on command by pressing function key f5. Alternatively, the drive motor may be turned on with the following command:

```
OPEN 15,8,15:PRINT#15, "M-E" +CHR$(130)
+CHR$(249) <RETURN>
```

Note: If a computer is not available to issue this command, the drive motor can be turned on by shorting pin 3 to pin 1 on P5.

11. Adjust VR1 (Item 71, see Fig. 3-2 for Models 1540 and 1541 or Fig. 3-3 for Model 1542) until the timing marks stop or the frequency counter displays 367 Hz, whichever reference is applicable.
12. Turn off the disk drive, computer, and all peripherals.
13. Remove all cables from the VIC-1541.
14. If further alignment needs to be performed, proceed with Section 3.3. If not, reassemble in accordance with Section 1.3.3.

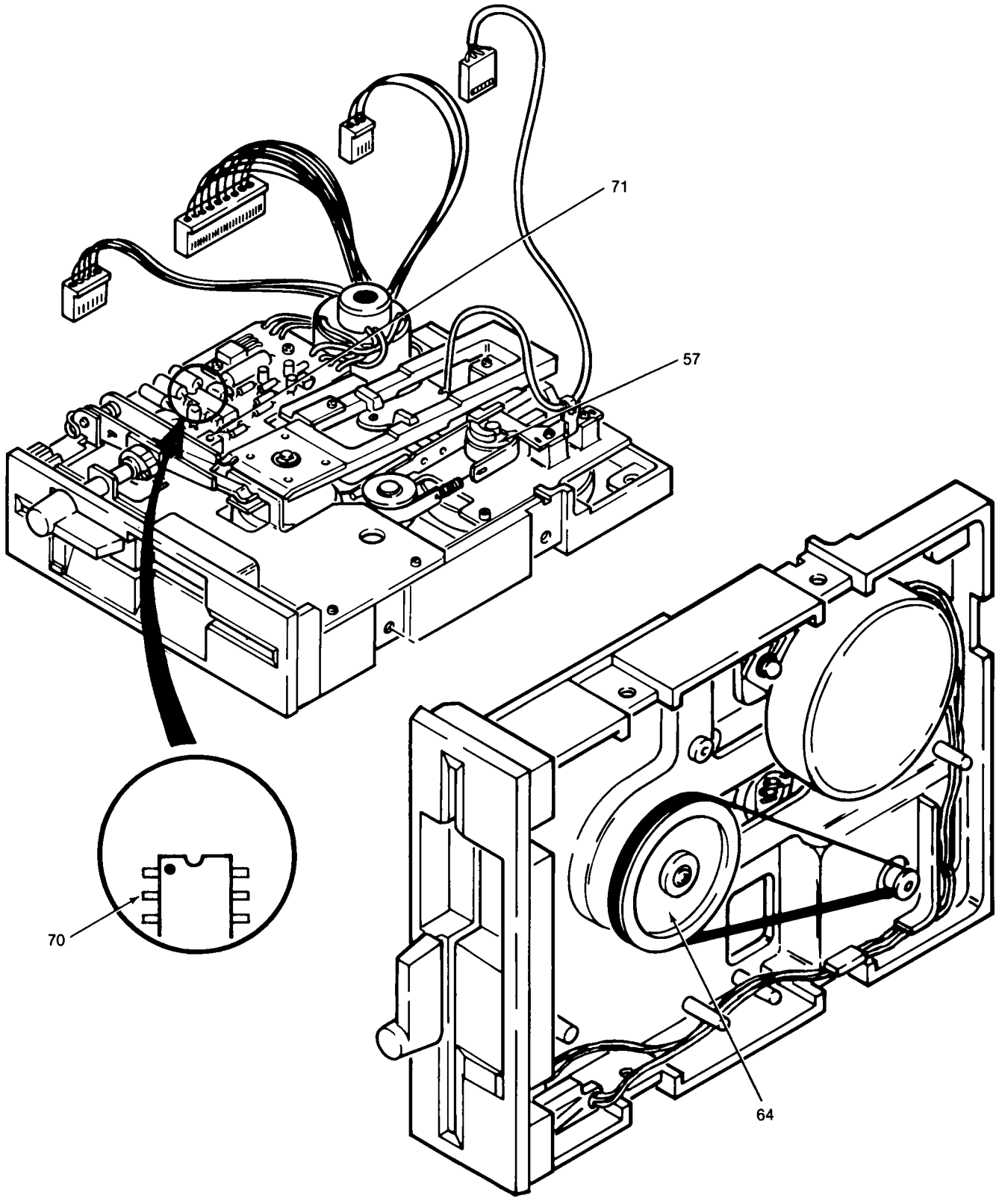


Fig. 3-3. Disk speed adjustment, Model 1542.

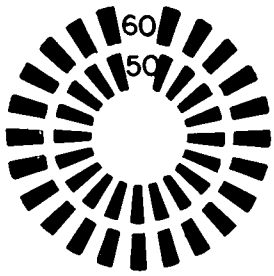


Fig. 3-4. Timing disk (actual size).

3.3 READ/WRITE HEAD ALIGNMENT

We now discuss two read/write head alignment procedures. The first (Section 3.3.1) is a step-by-step procedure, shop-quality alignment and is preferred over the second procedure, which is an emergency or makeshift alignment (Section 3.3.2).

The shop-quality alignment requires a dual-trace oscilloscope and an alignment reference disk (Dysan Analog Alignment Diskette 224/2A). If this equipment is not available, follow the second alignment procedure using a voltmeter, video detector (see Appendix B), and a formatted disk you know to be in proper alignment. This procedure is also useful for recovering data from a diskette that was recorded on a disk drive that was out of alignment.

The VIC-1541 disk drive frequently goes out of alignment because of the track select mechanism. The stepping motor drive wheel (Fig. 3-3, Item 57) is aluminum and is press-fit onto a stainless steel shaft. As the VIC-1541 heats up, the aluminum pulley expands faster than the shaft, causing the pulley to loosen slightly. When the pulley is loose and hits the track No. 1 stop (Item 61), it slips on the shaft. The result is a misaligned read/write head. At first glance, the track No. 1 stop appears to have moved because the gap between the pulley and stop increases, but this is seldom the case. Out of over 80 malfunctioning VIC-1541 disk drives I have repaired, fewer than 10 were due to problems other than the pulley slipping on the shaft.

3.3.1 Shop-Quality Alignment

This procedure requires a dual-trace oscilloscope, Dysan Analog Alignment Diskette 224/2A or equivalent, and a Phillips screwdriver.

1. Remove all cables from the VIC-1541, especially the ac line cord.
2. Disassemble the VIC-1541 in accordance with Section 1.3.1.
3. Connect five female connectors (Items 25 through 29) to their mating connectors (Items 39 through 43, respectively). (See Fig. 3-5 for the 1540, Fig. 3-6 for the 1541, and Fig. 3-7 for the 1542.) See Section 1.3.3 for proper connector orientation. Place these subassemblies in such a fashion as to allow access to the bottom of the drive unit while not allowing the PC board components to contact any metal parts.
4. Connect the serial bus cable between the serial bus connector (Item 8) and the Commodore 64/VIC 20.
5. Connect the ac line cord between the ac line cord connector (Item 6) and an ac outlet.

WARNING

Use extreme care to avoid contact with frame components. High ac voltage potentials are present during this procedure. These voltages may cause fatal injury.

6. Connect channel A of the dual-trace oscilloscope to pin 7 of the second video amp, and connect channel B to pin 8 of the second video amp. (See Fig. 3-8 for Model 1540 or Fig. 3-9 for Models 1541 and 1542.) Connect channel A at 73 and channel B at 74. Invert channel B and place the scope into A + B mode. Set the vertical sensitivity to 2V/cm and sweep time to 20 ms.
7. Turn on the disk drive, any peripherals, and the oscilloscope.
8. Turn on the Commodore 64/VIC 20.
9. Load, or enter and then run the exerciser program of Section 3.1.
10. Insert the alignment disk (Dysan Analog Alignment Diskette 224/2A or equivalent) into the drive unit.
11. Depress function key f1 as many times as necessary until the display indicates track No. 17.

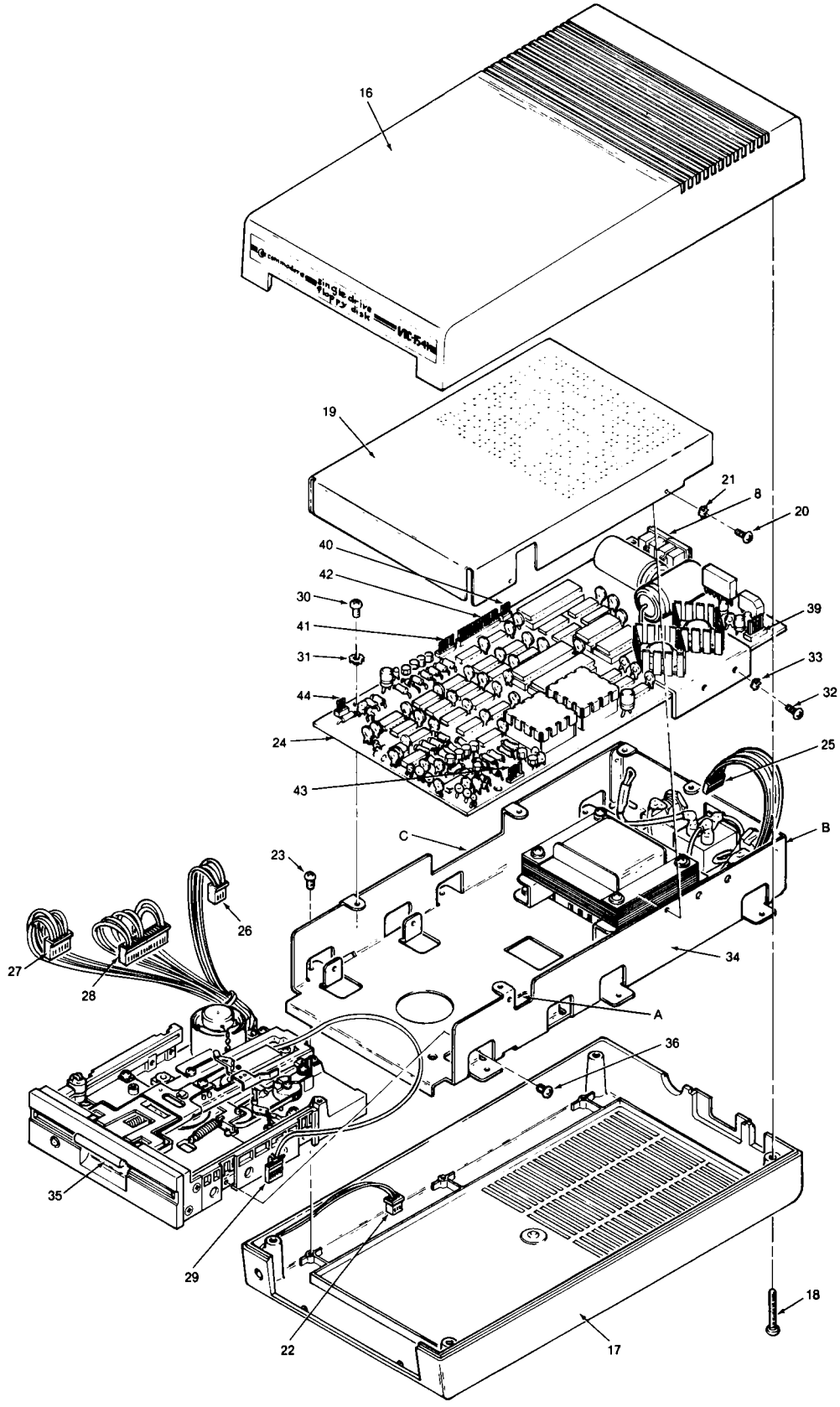


Fig. 3-5. Alignment setup, Model 1540.

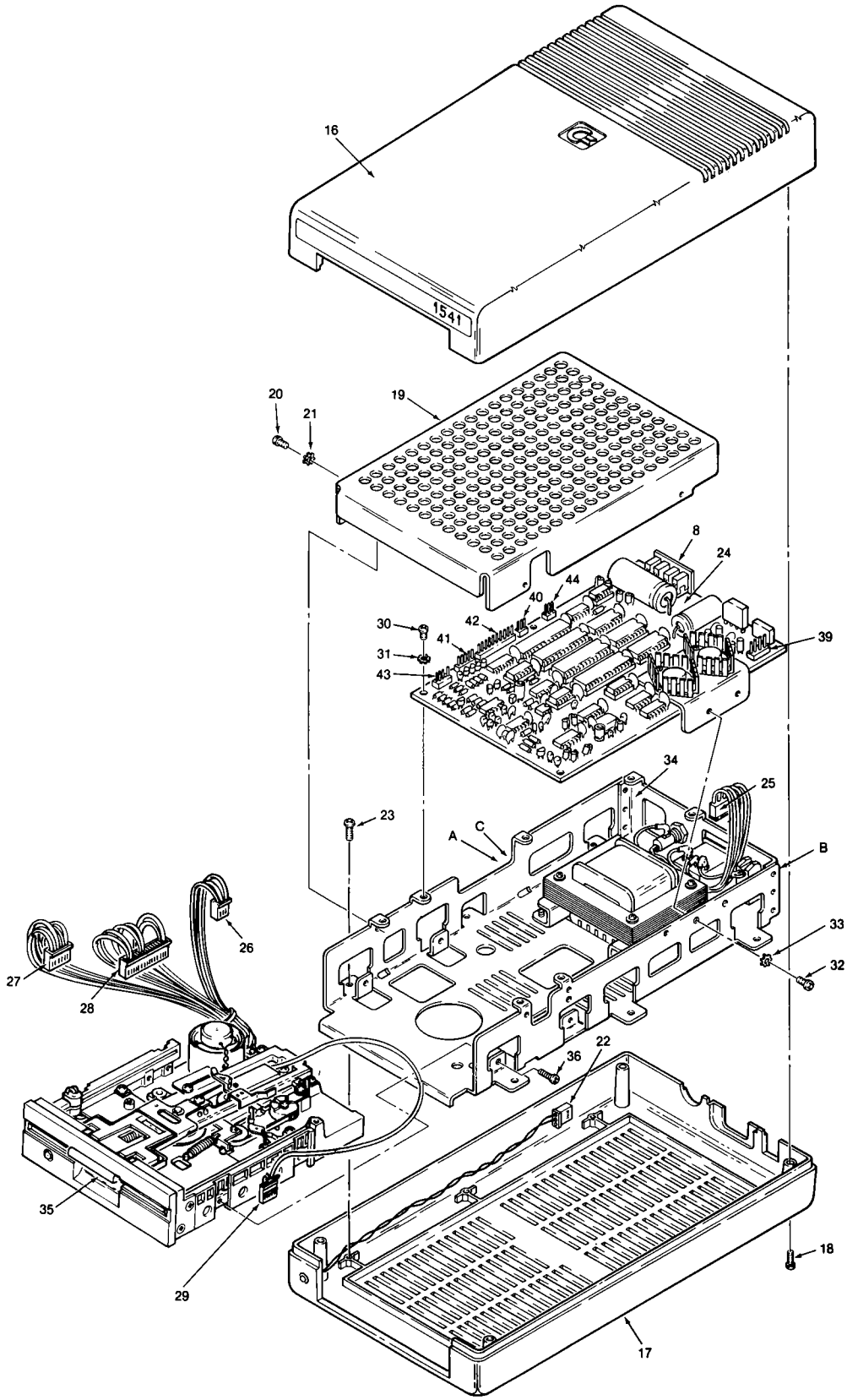


Fig. 3-6. Alignment setup, Model 1541.

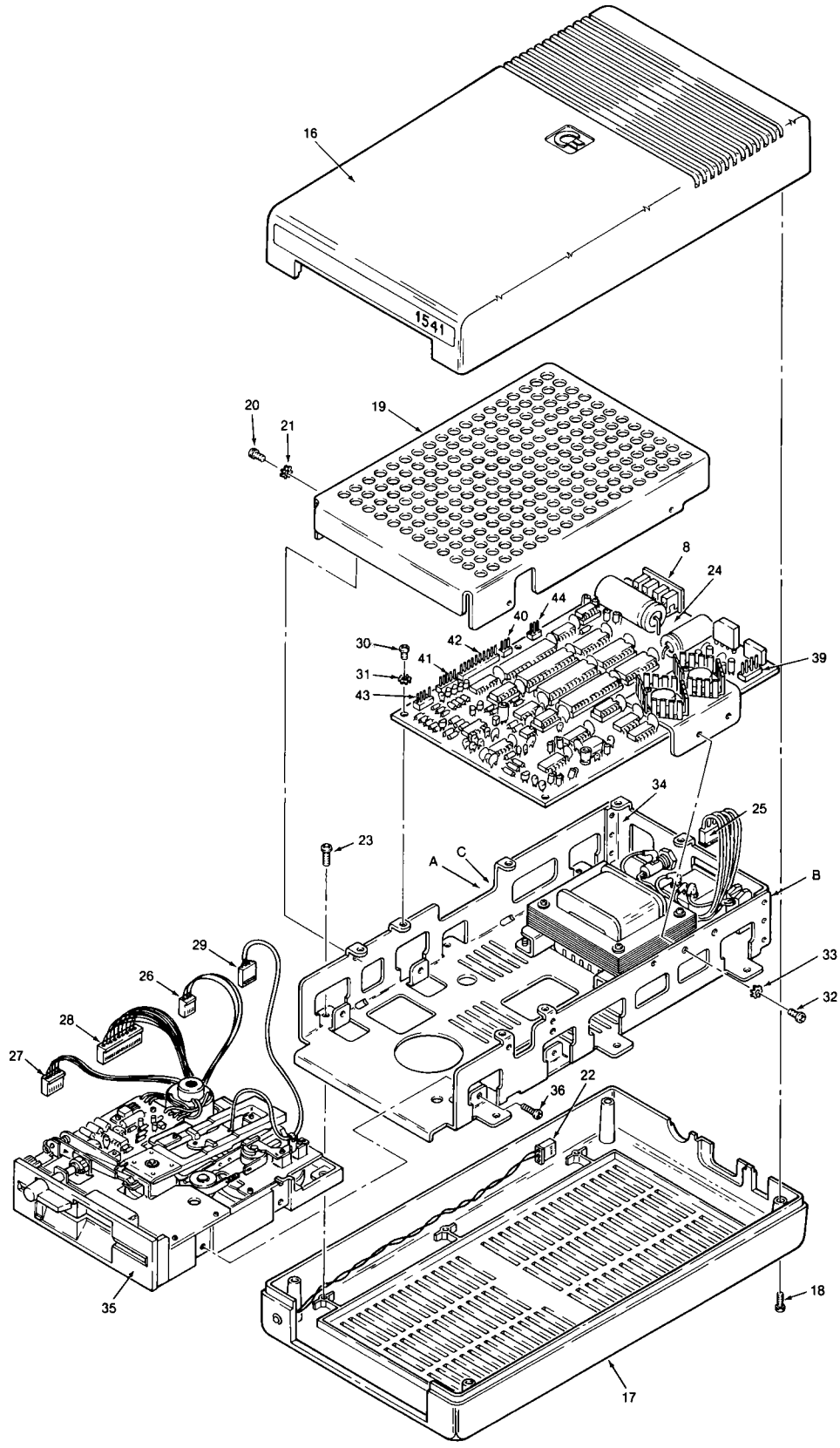


Fig. 3-7. Alignment setup, Model 1542.

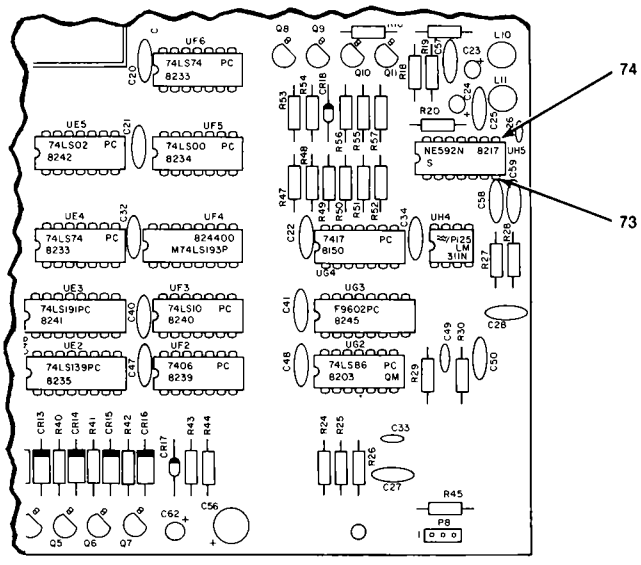


Fig. 3-8. Location of second video amplifier output pins, Model 1540.

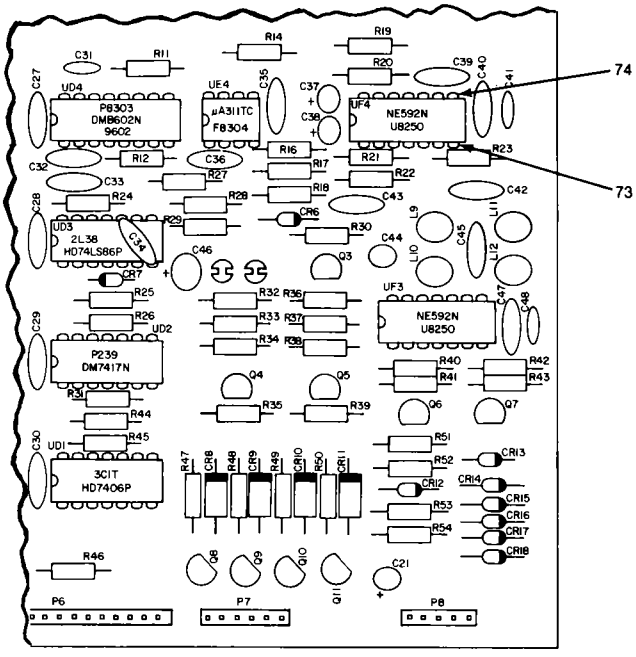


Fig. 3-9. Location of second video amplifier output pins, Models 1541 and 1542.

12. Loosen but do not remove the two screws that secure the stepping motor (Item 72). (See Fig. 3-10 for Models 1540 and 1541 or Fig. 3-11 for Model 1542.)
13. Rotate the stepping motor housing while observing the oscilloscope display (see Fig. 3-12). The correct setting for the stepping motor produces lobes of equal amplitudes. At the very least, the lobes must be within 90% of each other. Tighten the two screws which secure the stepping motor housing.

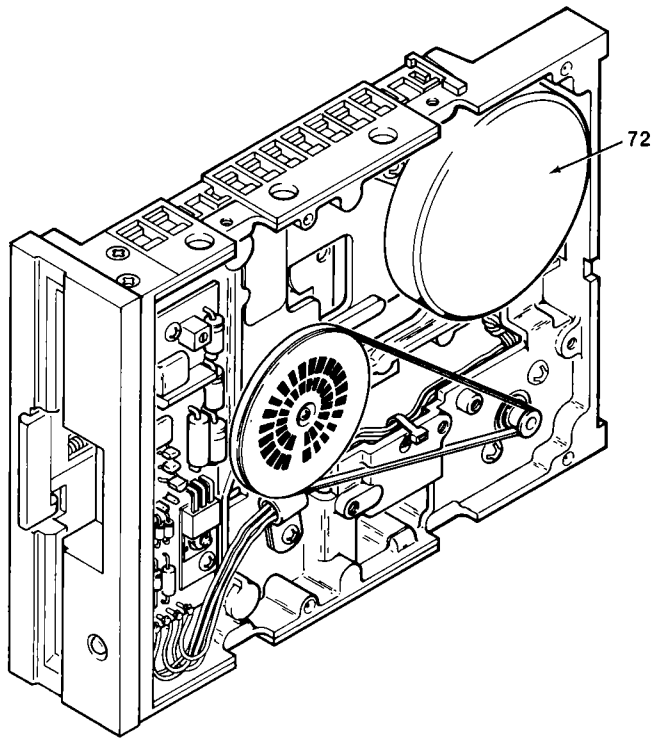


Fig. 3-10. Head alignment, Models 1540 and 1541.

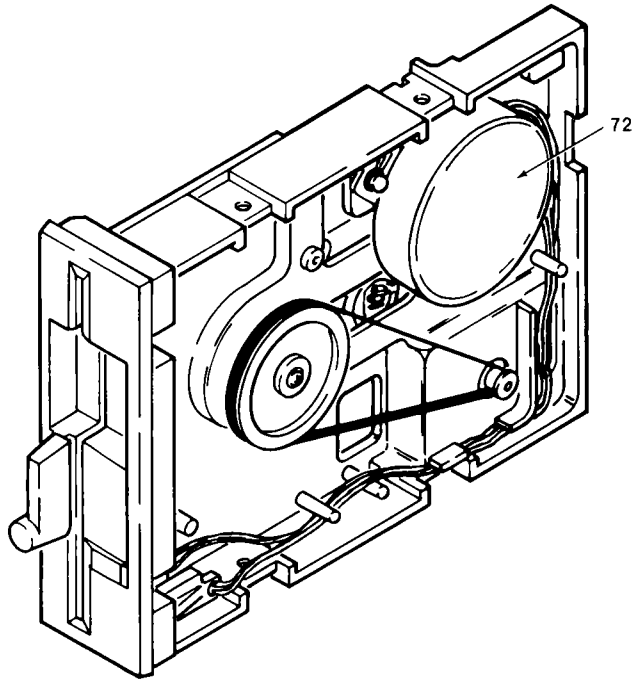


Fig. 3-11. Head alignment, Model 1542.

14. Depress function key f1 as many times as necessary until the screen displays track No. 34. Then depress function key f3 until the screen displays track No. 17. Verify that the

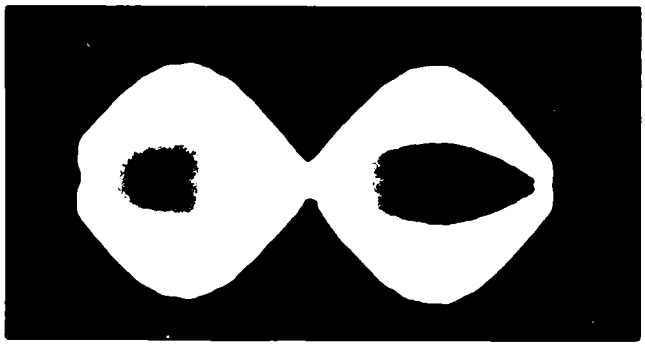


Fig. 3-12. Cat's eye pattern.

lobes on the oscilloscope display are within 90% of each other.

15. Perform a bump by depressing function key f2 (<SHIFT> f1). Then depress function key f1 until the screen displays track No. 17. Verify that the lobes on the oscilloscope display are within 90% of each other.
16. Exit the program by depressing function key f4 (<SHIFT> f3).
17. Adjust track No. 1 stop by performing the procedure in Section 3.4, "Track No. 1 Stop Adjustment," starting with step 1.

3.3.2 Emergency or Makeshift Alignment

The procedure described here allows you to align the read/write head using only a voltmeter, video detector (see Appendix B), Phillips screwdriver, and a formatted floppy disk. Before you use this procedure, it is important to understand both its advantages and its limitations.

One important advantage that this alignment has over the shop-quality alignment is that a dual-trace oscilloscope is not needed; a voltmeter and the video detector are used instead. This procedure can be performed at locations where test equipment and an alignment disk may not be available. Another advantage of this procedure is that the disk drive may be aligned to any formatted floppy disk. This means that you can temporarily align your drive to a floppy disk that has been recorded out of alignment in order to recover data from it. In this case, true alignment should be restored after recovery and backup of data.

The disadvantage of this method is the alignment reference selected. This procedure will yield an alignment as accurate as the disk chosen to act as the alignment disk or alignment reference. If the disk you choose is off, the alignment will be too. While most factory prerecorded disks are amazingly accurate, some can be off significantly. It is best to use a disk that has never been written to since the factory recording. Even if the disk you choose is off slightly, it will still allow you to "fix" a disk drive that is not working because of misalignment.

1. Remove all cables from the VIC-1541, especially the ac line cord.
2. Disassemble the VIC-1541 in accordance with Section 1.3.1.
3. Connect five female connectors (Items 25 through 29) to their mating male connectors (Items 39 through 43, respectively). (See Fig. 3-5 for the 1540, Fig. 3-6 for the 1541, and Fig. 3-7 for the 1542.) See Section 1.3.3 for proper connector orientation. Place these subassemblies in such a fashion as to allow access to the bottom of the drive unit while not allowing the PC board components to contact any metal parts.
4. Connect the serial bus cable between the serial bus connector (Item 8) and the Commodore 64/VIC 20.
5. Connect the ac line cord between the ac line cord connector (Item 6) and an ac outlet.

WARNING

Use extreme care to avoid contact with frame components. High ac voltage potentials are present during this procedure. These voltages may cause fatal injury.

6. Connect the video detector (see Appendix B) to the second video amp. (See Fig. 3-13 for the 1540 or Fig. 3-14 for the 1541 and 1542.) Connect the black lead to pin 7 (Item 73) and the red lead to pin 8 (Item 74). Connect the other end of the video detector to the voltmeter.
7. Turn on the disk drive, any peripherals, and the voltmeter.
8. Turn on the Commodore 64/VIC 20.
9. Load, or enter and then run the exerciser program of Section 3.1.

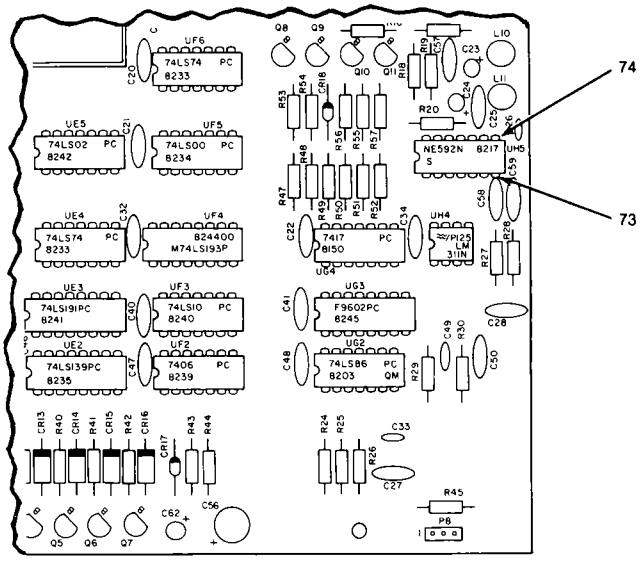


Fig. 3-13. Location of second video amplifier output pins, Model 1540.

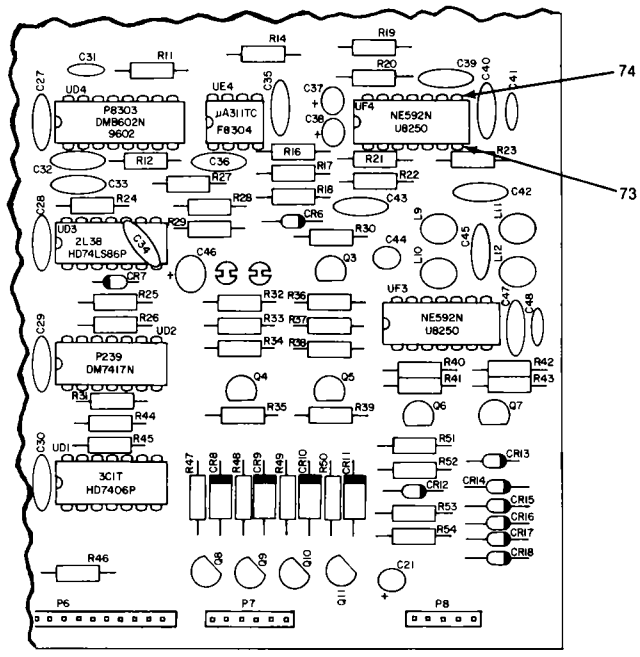


Fig. 3-14. Location of second video amplifier output pins, Models 1541 and 1542.

10. Insert the formatted disk that is to be used as a reference.
11. Depress function key f1 as many times as necessary until the display indicates track No. 6.
12. Loosen but do not remove the two screws that secure the stepping motor (Item 72). (See Fig. 3-15 for Models 1540 and 1541 or Fig. 3-16 for Model 1542.)
13. Slowly rotate the stepping motor counterclockwise (as viewed from the bottom, or drive belt, side of the drive unit) while

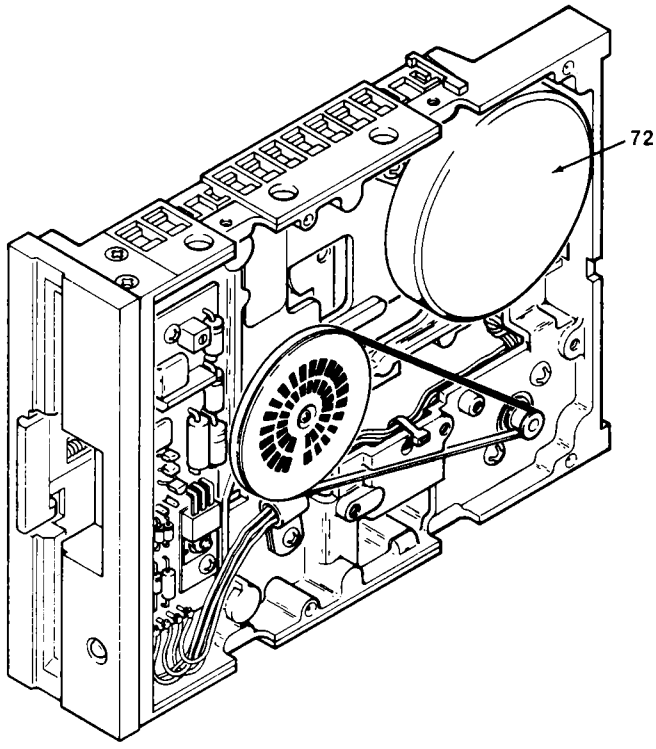


Fig. 3-15. Head alignment, Models 1540 and 1541.

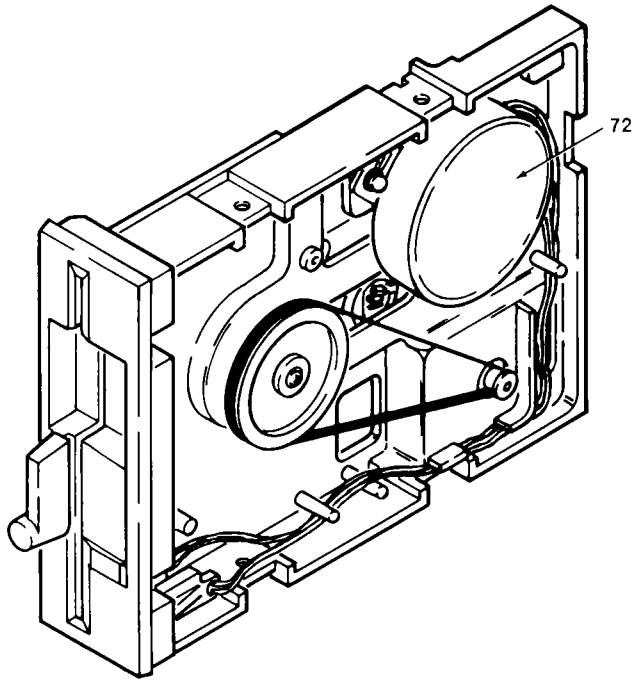


Fig. 3-16. Head alignment, Model 1542.

observing the voltmeter. You will notice that the voltage increases, peaks, then decreases. The correct setting for the stepping motor is at the peak. Tighten the two screws that secure the stepping motor housing.

14. Depress function key f2 (<SHIFT> f1) to bring the head to track No. 1 stop.
15. Depress function key f1 once and the screen should display track No. 1.5. Inspect track No. 1 stop. If the stepping motor drive pulley is not touching the track No. 1 stop, omit steps 16 through 18 and proceed directly to step 19.
16. Depress function key f1 as many times as necessary until the screen displays track No. 16.
17. Loosen but do not remove the two screws that secure the stepping motor (Item 72).
18. Slowly rotate the stepping motor clockwise while observing the voltmeter. The voltmeter display will decrease, then increase, peak, then decrease again. The correct setting for the stepping motor is at the peak. This *must not be* the same peak you observed in step 13. Tighten the two screws that secure the stepping motor housing.
19. Depress function key f2 (<SHIFT> f1) to bring the read/write head to track No. 1 stop.
20. Note the voltmeter display at track No. 1, then depress function key f1 once and verify that the voltmeter display at track No. 1.5 is no greater than 30% of that noted for track No. 1.
21. Repeat the step 20 check for tracks 2 through 35.
22. Depress function key f2 (<SHIFT> f1) to bring the read/write head back to track No. 1.
23. Adjust the track No. 1 stop by performing the procedure in Section 3.4, "Track No. 1 Stop Adjustment," starting with step 4.

3.4 TRACK NO. 1 STOP ADJUSTMENT

Never perform this procedure without first performing one of the procedures from Section 3.3. The following procedure does not include setup information. Setup is performed in procedure 3.3.1 or 3.3.2. The above procedures also indicate which step to begin with below.

1. Loosen the track No. 1 stop screw(s) (Fig. 3-17, Item 75). Loosen the track No. 1 stop so that it moves freely under the screw(s).

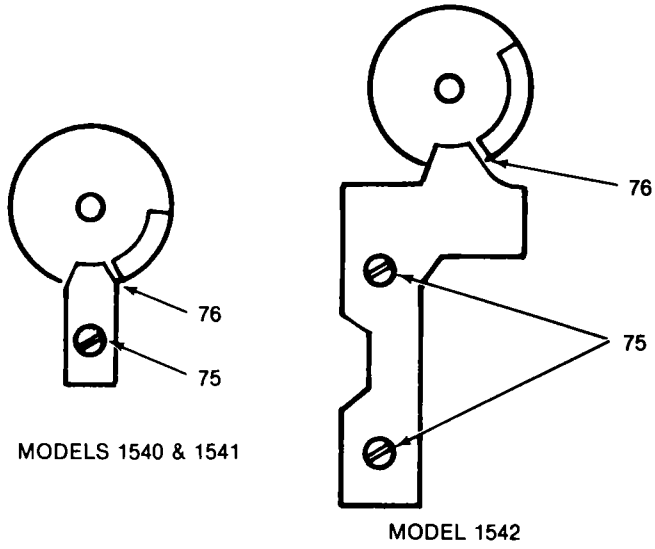


Fig. 3-17. Track No. 1 stop adjustment.

2. Verify that the oscilloscope displays the 125-Hz waveform shown in Fig. 3-18. This waveform is at track No. 1. If this waveform is not present, depress function key f1 or f3 as necessary until the oscilloscope displays the 125-Hz waveform.
3. Omit steps 4 through 6 and proceed directly to step 7.
4. Depress function key f4 to exit the exerciser program.
5. Loosen the track No. 1 stop screw(s) (Fig. 3-17, Item 75). Loosen the track No. 1 stop so that it moves freely under the screw(s).
6. Enter the following command to seek track No. 1:

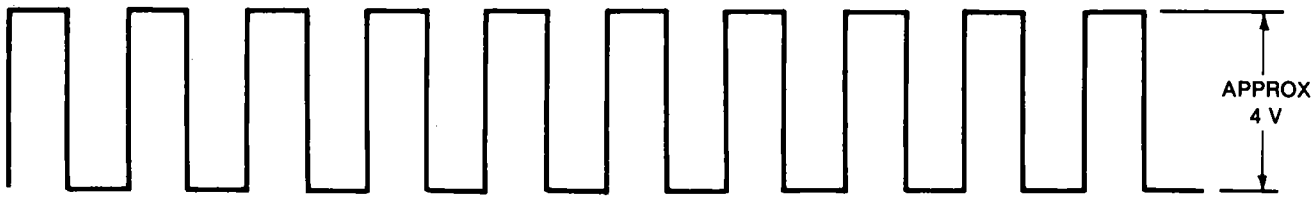


Fig. 3-18. Track No. 1 pattern.

```
OPEN 15,8,15,"I":OPEN 8,8,8,"#":PRINT#15,
"U1:"8;0;1;1
```

7. Slide a 0.006-inch feeler gauge into the gap (Fig.3-17, Item 76), gently push track No. 1 stop against the feeler gauge, and tighten the screw(s).
8. Verify the gap by sliding the feeler gauge into the gap. The feeler gauge should not bind, nor be loose.
9. Turn off the Commodore 64/VIC 20.
10. Turn off the disk drive and peripherals.
11. Disconnect all test equipment from the VIC-1541.
12. Disconnect all cables from the VIC-1541.
13. Reassemble the VIC-1541 in accordance with Section 1.3.3.

CHAPTER 4

Preventive Maintenance

This chapter provides instructions for day-to-day do's and don'ts for prolonging the life and integrity of the VIC-1541 disk drive and 5¼-inch floppy disks. Also included is information pertaining to cleaning the head and removing dust.

4.1 EXTENDING THE LIFE OF THE VIC-1541

The VIC-1541 disk drive does not require a lot of attention in order to keep it running. Other than requiring some consideration of heat buildup and contaminants, the VIC-1541 needs no special care.

The VIC-1541 typically heats up after approximately 30 minutes of operation. The 1540 gets hotter than the 1541 or 1542. There are a number of VIC-1541 add-on products which employ a fan to assist in cooling the VIC-1541. These fans are effective in cooling the disk drive, but be advised of their potential adverse side effects. If a fan is used, the case of the VIC-1541 must be either pressurized or depressurized. If the case is pressurized (fan in intake mode), the heat is blown out across the floppy disk, thereby heating the floppy disk. If the case is depressurized (fan in exhaust mode), then dust and/or other contaminants are drawn in across the floppy disk. This dust can degrade the performance of the VIC-1541, and it might cause permanent damage.

The VIC-1541 is cooled by passive airflow over its internal parts. The internal parts transfer their heat to the air inside the case of the VIC-1541. The hot air, in turn, rises out of the top vents. The hot air is replaced by cold air entering into the case through the lower cooling vents. The airflow through the VIC-1541 is subtle and should not be impeded.

To prevent overheating of your VIC-1541 disk drive, follow these precautions:

1. Do not stack VIC-1541s because the heat rising up out of the lower VIC-1541 will flow up into the upper VIC-1541. This will add to the heat generated by the upper VIC-1541, and the upper VIC-1541 may have a tendency to overheat. Additionally, the upper VIC-1541 obstructs the cooling vents on the lower VIC-1541.
2. Do not place anything on the cooling vents of the VIC-1541. Obstructing the cooling vents restricts airflow through the case of the VIC-1541, contributing to overheating.
3. Allow three inches between the VIC-1541 and any other objects. This practice allows air to

flow more freely into the bottom cooling vents of the VIC-1541.

4. When practical, do not operate the VIC-1541 in an environment above 25°C (78°F).
5. Turn off the VIC-1541 when the Commodore 64 or VIC 20 is not in use.

The VIC-1541 must also be kept free of contaminants. Dust and dirt can cause overheating and unnecessary wear. Contaminants on the read/write head or on the floppy disk can cause permanent head damage or scratch the floppy disk. If the floppy disk gets scratched, then data may be lost. The oxide coating at the edges of the scratch can be chipped off by the read/write head and cause oxide deposits on the read/write head.

Dust in the drive unit can cause wear of moving parts. Also, dust on electronic parts can promote overheating by insulating the components and inhibiting their ability to dissipate heat.

Once every 12 months, you should remove dust from the inside of the VIC-1541. To do this, disassemble the VIC-1541 using the instructions in Section 1.3.1, "Disassembly and Identification of Subassemblies." Use a soft brush to brush the dust from the internal parts. If you have compressed air available, use no more than 15 psi of pressure to blow the dust off.

Observe the following precautions when removing dust from the VIC-1541:

1. Do not bend component leads. Bending a component lead weakens it and causes it to become more brittle. If bent a few times in the same place, the lead will break.
2. Be careful when handling the drive unit. The drive unit is vulnerable when removed from the protection of the VIC-1541's case. Be especially careful to avoid wrinkling the thin metal track select band.
3. Do not touch the read/write head. Oil from your finger gets on the head and collects dirt.
4. Do not use strong solvents; if a solvent is necessary, use denatured alcohol.

Inspect the drive belt on the drive unit for signs of wear. Also, inspect all the disk drive's internal subassemblies for signs of corrosion. If corrosion is present, use denatured alcohol to clean off the corrosion. Also clean the read/write head following the instructions in Section 4.3, "Cleaning the Read/Write Head." Reassemble the VIC-1541 according to the instructions in Section 1.3.3, "Reassembly."

4.2 EXTENDING THE LIFE OF THE FLOPPY DISK

Use special care when handling floppy disks in order to prevent loss of data or even damage to the read/write head. When a floppy disk that has dust or dirt on it is inserted into the VIC-1541, the contaminants can be deposited on the read/write head. Once these deposits are on the read/write head they can scratch any floppy disk inserted into the drive, even a clean one. Occasionally inspect your disks for dirt, scratches, or warp. Don't forget the bottom surface of the disk. This is the side on which the data is written.

Follow these guidelines for prolonging the life of a floppy disk:

1. Always keep the floppy disk in its paper envelope whenever it is not in the disk drive. The envelope offers protection for the exposed areas of the media and also helps keep the disk clean.
2. Store disks in the vertical position. If disks are stacked horizontally the disk media can sometimes stick inside the jacket. When stored vertically, dirt may fall off the disk.
3. Do not store floppy disks in direct sunlight. Direct sunlight can warp the disk and crack the oxide coating.
4. Do not install a defective disk into the disk drive. This can cause head problems which promote premature disk failure.
5. Do not place disks near transformers, motors, monitors, or other sources of strong magnetic fields. Magnetic fields can alter or erase data on the disk.
6. Do not fold or bend floppy disks.
7. Don't touch the exposed surface of the disk. Fingerprints collect dirt which contaminates the read/write head.
8. Do not put disks through security X-ray machines. Instead, have the disks checked by hand.

9. When labeling floppy disks, always write on the label before applying it to the disk. Do not write on the disk jacket because pencils and pens indent the disk surface, thereby degrading disk performance.

4.3 CLEANING THE READ/WRITE HEAD

It is important to keep the read/write head clean because deposits on the head can cause disk damage and read/write errors. There are two methods you may use to remove deposits from the read/write head. One method requires a cleaning disk (see Section 4.3.1). The second method is to disassemble the disk drive and clean the read/write head with a lint-free cloth and solvent (see Section 4.3.2). Each method has its advantages and disadvantages.

The advantage of using a cleaning disk is that it is easy to use. On a cleaning disk, the media is replaced by a cloth or chamois disk wet with solvent. Insert this disk in the disk drive and rotate for approximately 30 seconds. The rotating disk rubs against the head and removes the deposits. The disadvantage of this method is that the cleaning disk can pick up abrasive deposits from the head, which then pass over the read/write head approximately 300 times a minute. These deposits could have an adverse effect on the read/write head.

The above effect does not occur if you disassemble the disk drive and clean the head manually. Additionally, this method allows you to see if all the deposits have been removed or if more cleaning is needed. Unfortunately, manually cleaning the head involves a lot more work than using a cleaning disk.

A combination of these methods is best. Typically, a cleaning disk should be used every month with a thorough manual head cleaning performed every six months. If your disk drive gets very heavy use, clean the head more often. Perform the manual cleaning if the deposits on the head are causing scratching or data loss problems. A cleaning disk should only be used for periodic cleaning. If a dirty head is causing problems, use the manual head cleaning method.

4.3.1 Using Head Cleaning Disks

To clean the read/write head with a cleaning disk, follow this procedure:

1. Connect the VIC-1541 to the Commodore 64 or VIC 20 serial bus.
2. Connect the ac line cord between its connector and an ac outlet.
3. Turn on the VIC-1541.
4. Turn on the Commodore 64 or VIC 20.
5. Load or enter the utility program of Fig. 3-1 into the Commodore 64 or VIC 20.
6. Prepare the cleaning disk in accordance with the manufacturer's instructions.
7. Insert the cleaning disk into the disk drive.
8. Run the utility program you entered in step 5.
9. Depress function key f5 to start rotating the disk.
10. Repeatedly depress function key f1 at the approximate rate of two keystrokes per second. This keeps moving the read/write head to a fresh surface of the cleaning disk, reducing the chance of abrasion from dirt already removed from the disk.
11. After approximately 30 seconds, stop the cleaning disk by depressing function key f7.
12. Remove the cleaning disk.
13. Exit the utility program by depressing function key f4 (<SHIFT> f3).
14. Allow plenty of time for solvents to evaporate before inserting a floppy disk into the VIC-1541.

4.3.2 Manual Head Cleaning

To clean the read/write head manually you will need the following materials: lint-free cloth or piece of foam rubber, cleaning solvent such as denatured alcohol or trichloroethylene, a Phillips screwdriver. Proceed as follows:

1. Remove the ac line cord from the VIC-1541.
2. Follow the instructions in Section 1.3.1 to remove the top cover, RFI shield, and disk controller PC board from the disk drive.
3. To access the read/write head, gently lift up the pressure pad mount as illustrated in Fig. 4-1.
4. Wet the lint-free cloth or foam rubber with solvent.
5. Gently rub the read/write head and pressure pad until deposits are no longer visible.

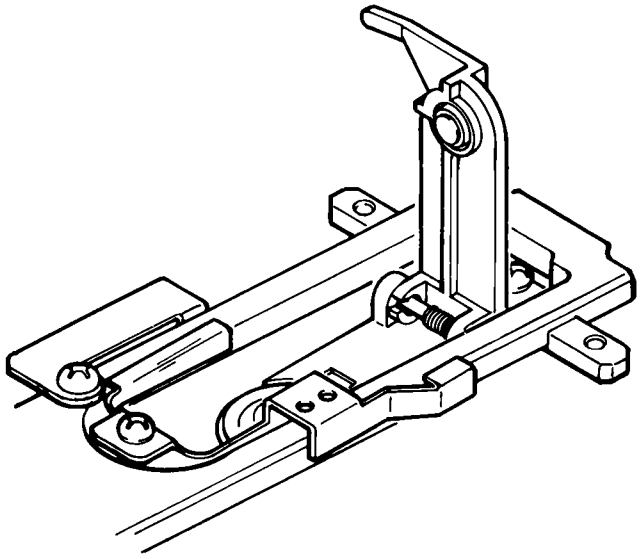


Fig. 4-1. Accessing the read/write head.

6. Allow all of the solvent to evaporate before proceeding.
7. Release the pressure pad mount.
8. Reassemble the VIC-1541 using the instructions in Section 1.3.3, "Reassembly."

CHAPTER 5

Basic Troubleshooting and Repair

This chapter covers most of the common failures of the VIC-1541 on a symptomatic basis. This means we will start troubleshooting by identifying a specific problem. Then we will look for malfunctions which can cause those specific problems. Some malfunctions can be as obvious as burned parts, a shorted conductor, or broken wires. Other malfunctions are invisible to the naked eye, such as a faulty integrated circuit (IC) or a bad transistor. In any event, you must first identify the problem in order to restore the disk drive to operation. Troubleshooting is this process of finding the problem.

5.1 INTRODUCTION TO TROUBLESHOOTING

When troubleshooting, there are some relatively safe assumptions that you can make. These assumptions are proven to be fact in approximately 95% of the malfunctions that occur in the VIC-1541. These assumptions are:

1. Assume only one problem exists. An example of this is the symptom of the drive motor and the stepping motor not turning. If you assume only one problem exists, then you know it must be a circuit of common use by both. You also know that it is not the drive motor *and* the stepping motor. It is not likely that both motors would fail at the same time. The only exceptions to this assumption are in the case of physical damage, such as could be caused by dropping the VIC-1541 or of lightning striking the power lines. In both cases, many internal parts could be permanently damaged.
2. When there is a choice between an active or passive part causing a problem, assume the active part is bad. Active parts are ICs, transistors, and diodes. Passive parts are capacitors, resistors, and inductors. With today's "low current" technology, passive parts are under no strain and very seldom fail. However, as in finding two independent malfunctions, it is still possible for these parts to fail.

Before troubleshooting, it is important to observe the malfunction carefully. Become familiar with the problem in as much detail as you can. If necessary, write down some data to compare with later, such as error numbers, track, and sector on which a malfunction occurs, commands that do not work, and so on.

While troubleshooting, always observe the disk

drive's reaction during a test and after any repair action is attempted. Compare these observations with the data that you recorded earlier. If the disk drive exhibits any change in behavior, it could be an important clue to finding the bad part.

Troubleshooting can be a long and tedious process. The purpose is to find the bad parts. In this quest it is sometimes easy to overlook the good parts. If the part is good, then this is not the part we are looking for. If you cannot find the bad part, then look for the good parts. Usually when a person troubleshoots a piece of electronic equipment, he or she starts out with two mental lists of parts. One list comprises "parts that could be bad." The other list comprises "parts that are good." Unless given a clue by the nature of the malfunctions, most troubleshooting starts with all the parts in the "parts that could be bad" list. Gradually, the troubleshooter finds circuits that work or determines that parts are good. These parts in the circuit are moved from the "parts that could be bad" list and placed on the "parts that are good" list. When the "parts that could be bad" list has one part left on it, that is the bad part. Usually, when the "parts that could be bad" list gets down to a few items, the bad part is obvious. Even if you have not yet found the bad part, as long as you are identifying good parts, you are making progress.

Except for read/write head alignment, our troubleshooting in Chapter 5 will narrow the problem down to a group of parts without the use of test equipment. This chapter assumes that you know how to solder, identify parts, and replace parts. If this is a new experience for you and you would like more information concerning these skills, read the following book:

Electronic Prototype Construction, by Stephen D. Kasten. Howard W. Sams & Co., 1983. (Cat. No. 21895)

The troubleshooting instructions in Section 5.3, "Basic Troubleshooting Flowchart," will either correct the malfunction or narrow down the list of "parts that might be bad." In addition to a parts list, Section 5.3 gives you several options on how to find the bad part. One of the options given is to follow specified instructions in Chapter 6, "Advanced Troubleshooting and Repair." Although Section 5.3 directs you to a specific section in Chapter 6, please read Section 6.1, "Introduction to Advanced Troubleshooting," before proceeding with the flowchart in Section 6.2.

5.2 IDENTIFYING A PROBLEM

This troubleshooting procedure can be used to locate and repair most common VIC-1541 malfunctions. For rare problems that require in-depth testing, see Chapter 6, "Advanced Troubleshooting and Repair."

Before you start the troubleshooting process, perform the following troubleshooting setup procedure:

1. Turn off VIC-1541 and Commodore 64 or VIC 20.
2. Remove ac line cord from the VIC-1541.
3. Remove any serial bus cables from the VIC-1541.
4. Remove top cover and RFI shield following the instructions in Section 1.3.1.
5. Connect the serial bus cable(s), which were removed in step 3, back to their respective receptacles.
6. Install ac line cord between its connector and an ac outlet.

After this setup has been performed, follow the flowchart in Section 5.3 to localize or isolate a problem. If the problem is not isolated, the flowchart will localize the malfunction to a particular circuit or group of circuits. The VIC-1541 may be repaired by replacing these parts. It may not be necessary to replace all of these parts. If you replace only one part at a time, then check to see if the problem is solved after each replacement; you might get lucky and replace the bad part on the first attempt. Of course there is always the possibility of replacing the bad part on the very last attempt. In any event, you are no worse off than replacing all the parts in question.

It is easiest to replace socketed ICs first. If you have spare ICs (6502, 6522, 6116, etc.), now is the time to make good use of them. If you know that these spares are in working order, you can substitute each of the spares for their socketed counterparts. Check to see if the malfunction still exists. If the problem has gone away, the last IC

you changed was the faulty one. If you wish to troubleshoot the problem further, see the applicable section in Chapter 6. The flowchart in Section 5.3 indicates the specific section to see. Each group of circuits is identified in a table and/or a figure specified in the flowchart. Tables have three columns labeled 1540, 1541, and 1542; the parts in question are listed under the applicable column for the model you are troubleshooting. Figures specified in the flowchart are three-part figures. Part A is for the 1540, part B is for the 1541, and part C is for the 1542. Faulty PC board parts are indicated on these figures. Use the part of the figure which is applicable to the model you are troubleshooting. Before attempting troubleshooting, inspect the read/write head for deposits and clean the head if necessary. See Section 4.3, "Cleaning the Read/Write Head."

5.3 BASIC TROUBLESHOOTING FLOWCHART

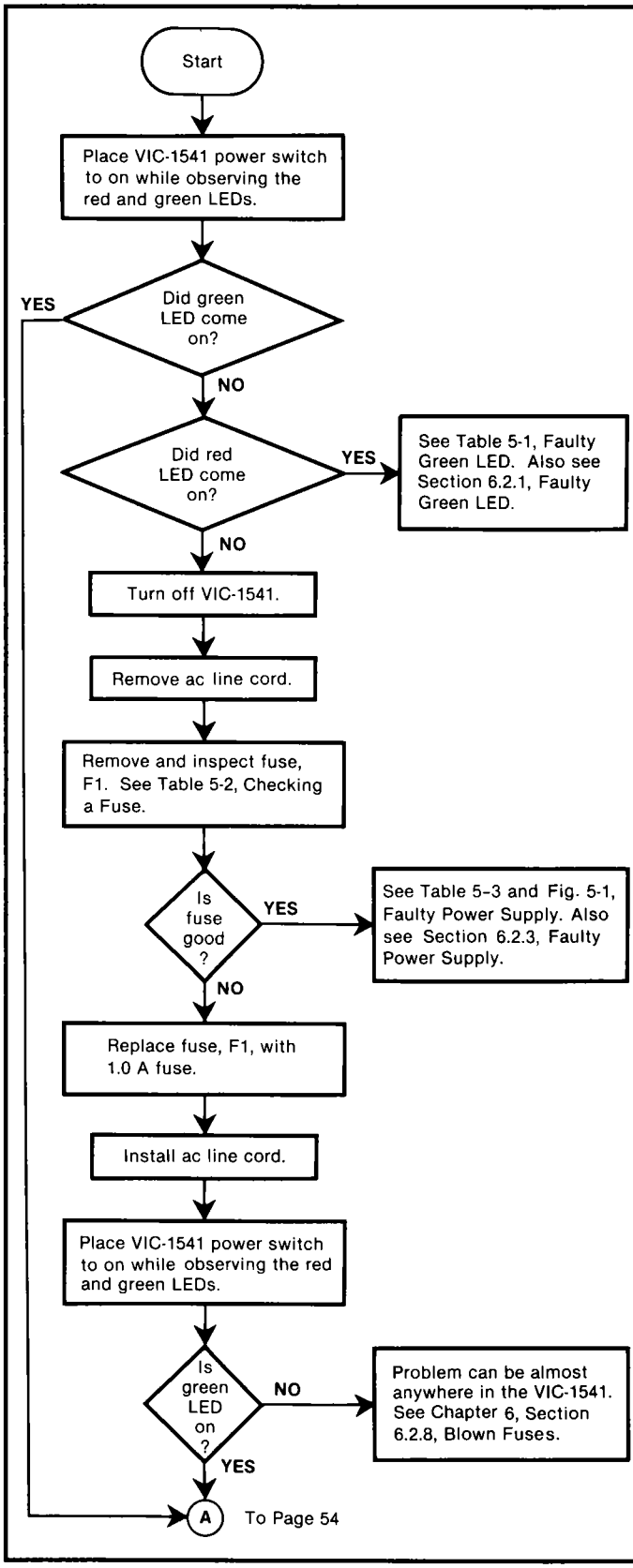
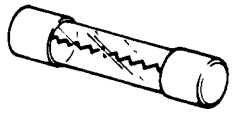


Table 5-1. Faulty Green LED

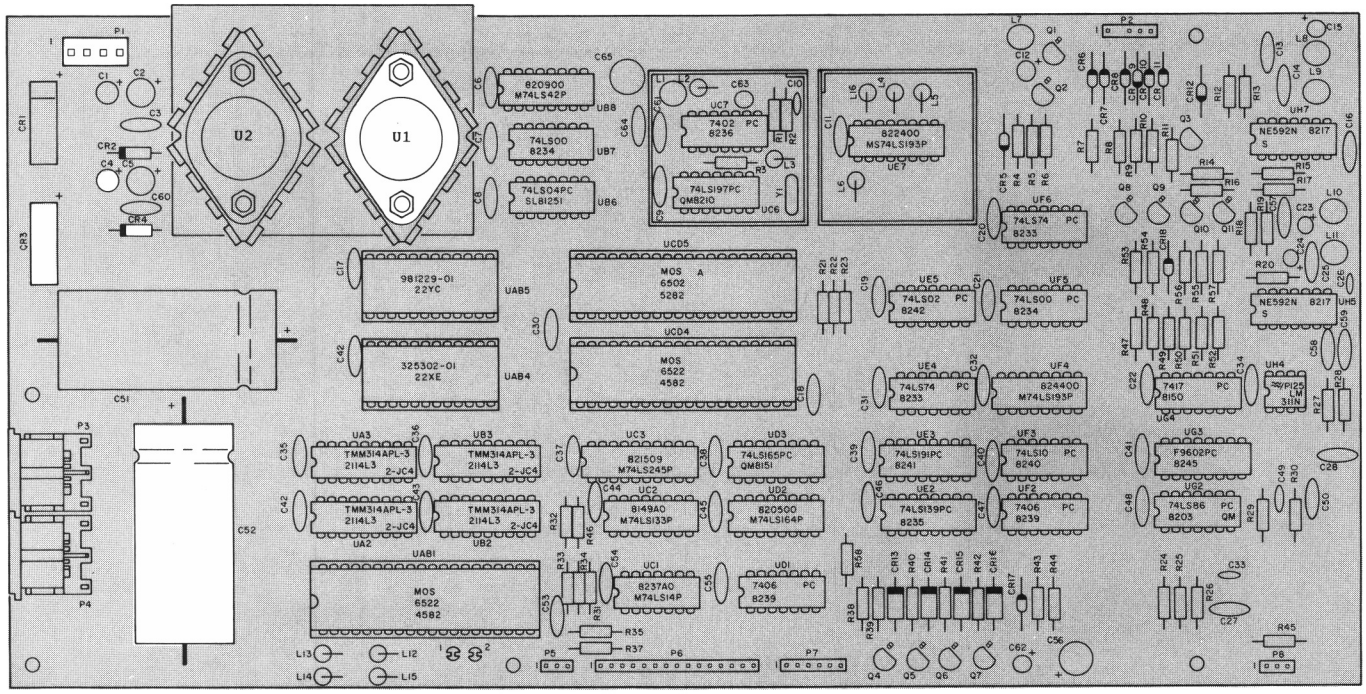
FAULTY PART IS ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
Green LED	Green LED	Green LED
Resistor, R45	Resistor, R55	Resistor, R55
Connector, P8	Connector, P4	Connector, P4
Connector, J8	Connector, J4	Connector, J4

Table 5-2. Checking a Fuse

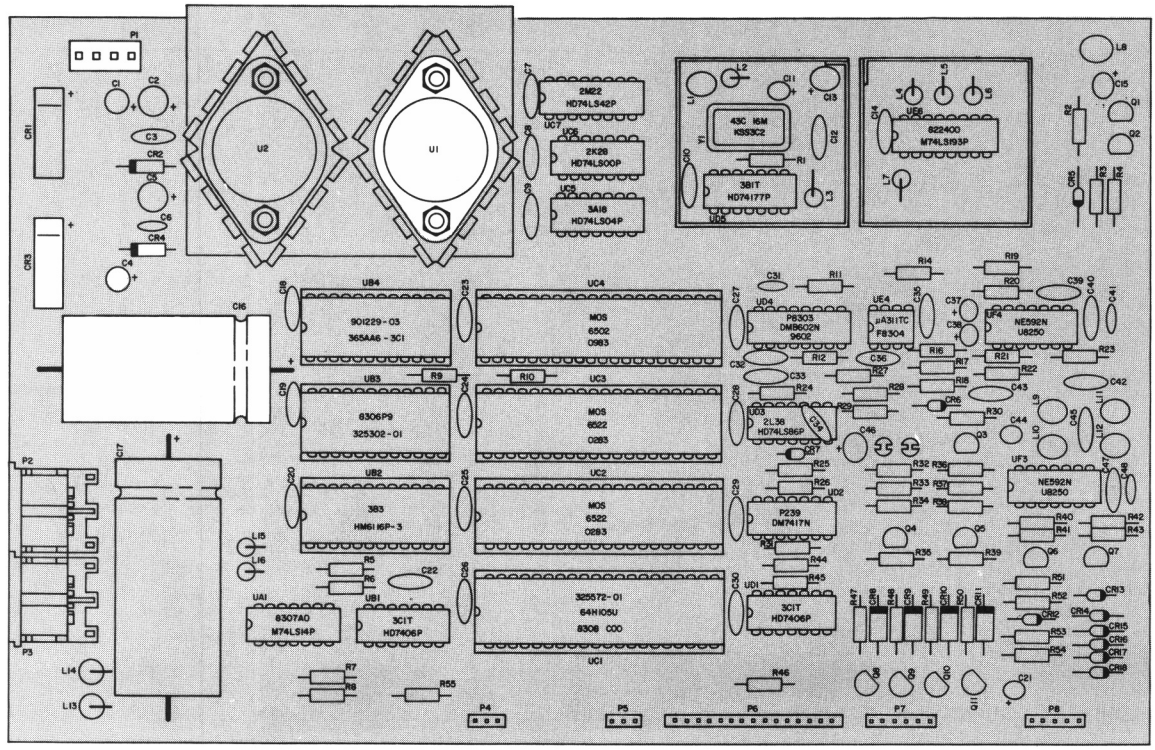
GOOD	BAD
	
Good Fuse Resistance = <2 Ω	Bad Fuse Resistance = Infinity

5-3. Faulty Power Supply

FAULTY PART IS ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
Connector, J9	Connector, J9	Connector, J9
Switch, S1	Switch, S1	Switch, S1
Fuse Holder, XF1	Fuse Holder, XF1	Fuse Holder, XF1
Transformer, T1	Transformer, T1	Transformer, T1
Connector, J1	Connector, J1	Connector, J1
Bridge, CR3	Bridge, CR3	Bridge, CR3
Diode, CR4	Diode, CR4	Diode, CR4
Capacitor, C4	Capacitor, C4	Capacitor, C4
Capacitor, C52	Capacitor, C16	Capacitor, C16
Regulator, U1	Regulator, U1	Regulator, U1
Connector, P1	Connector, P1	Connector, P1

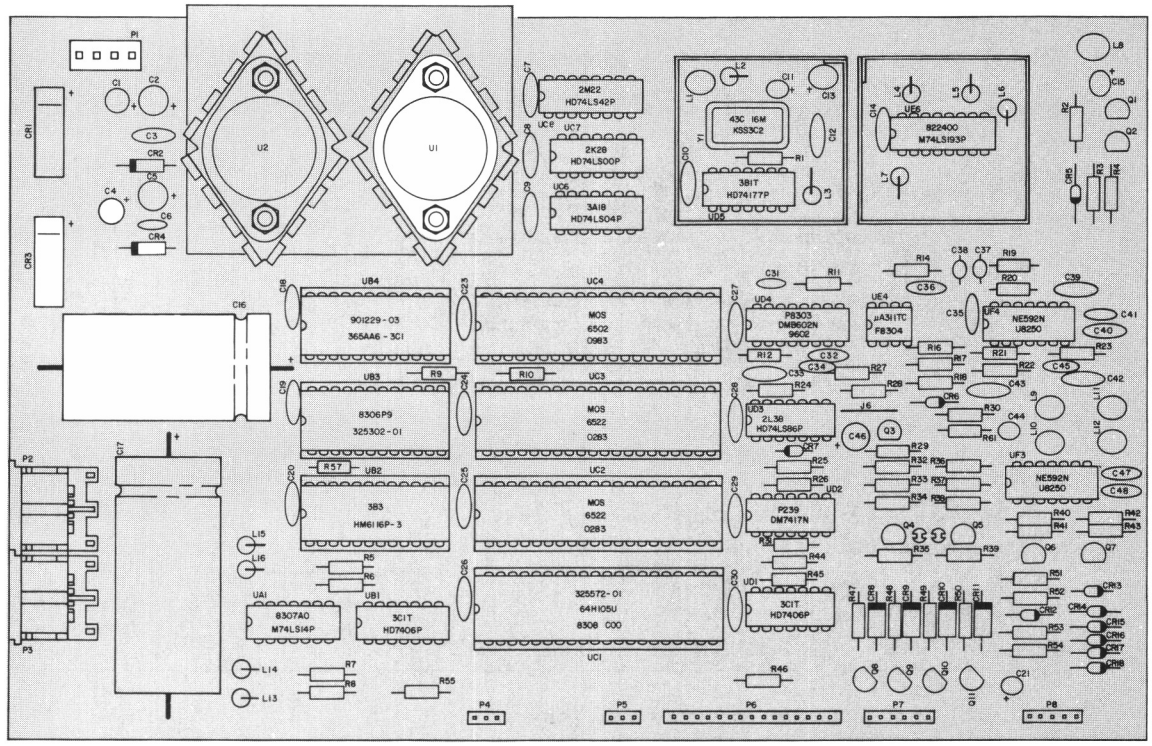


(A) 1540.



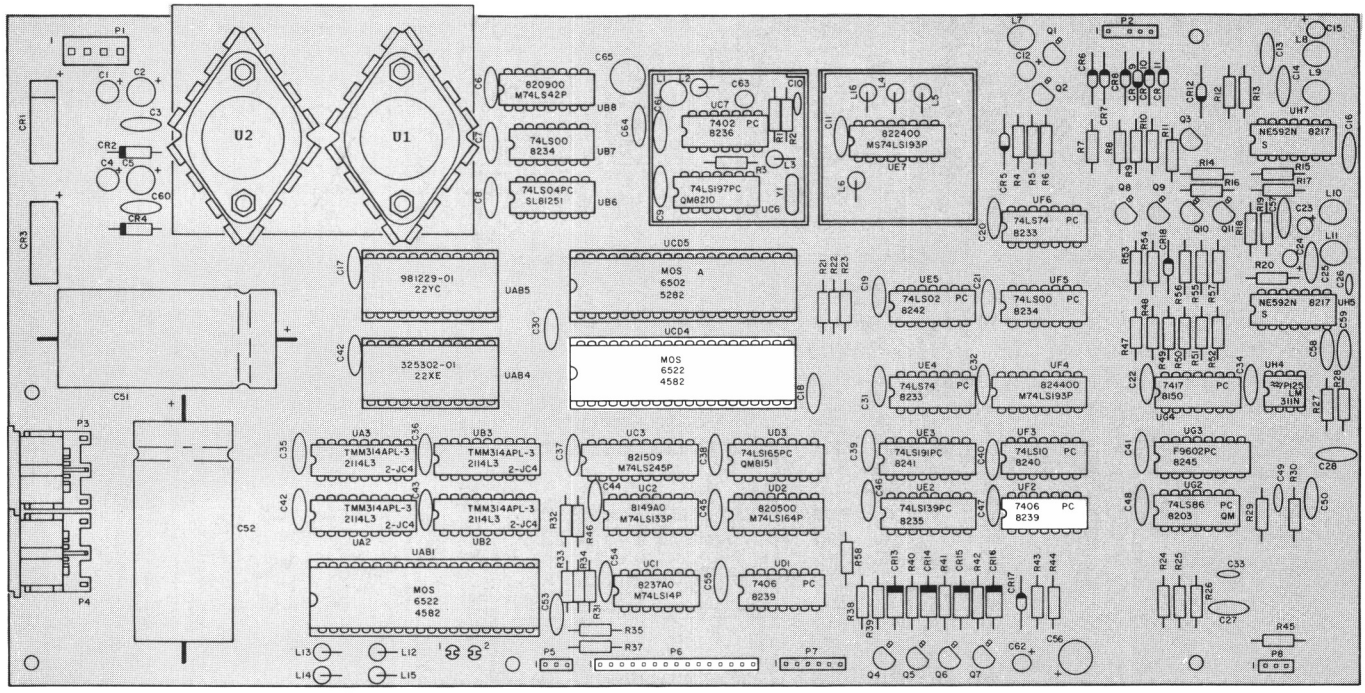
(B) 1541.

Fig. 5-1. Faulty power supply.



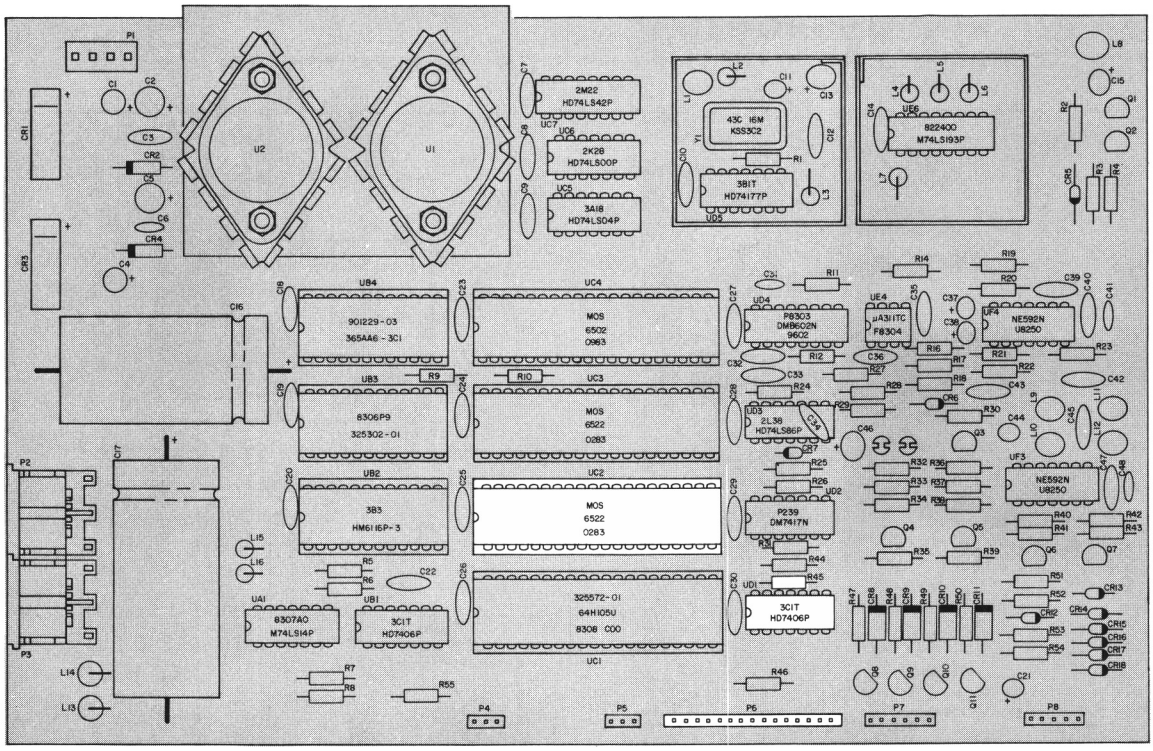
(C) 1542.

Fig. 5-1. Faulty power supply (cont.).

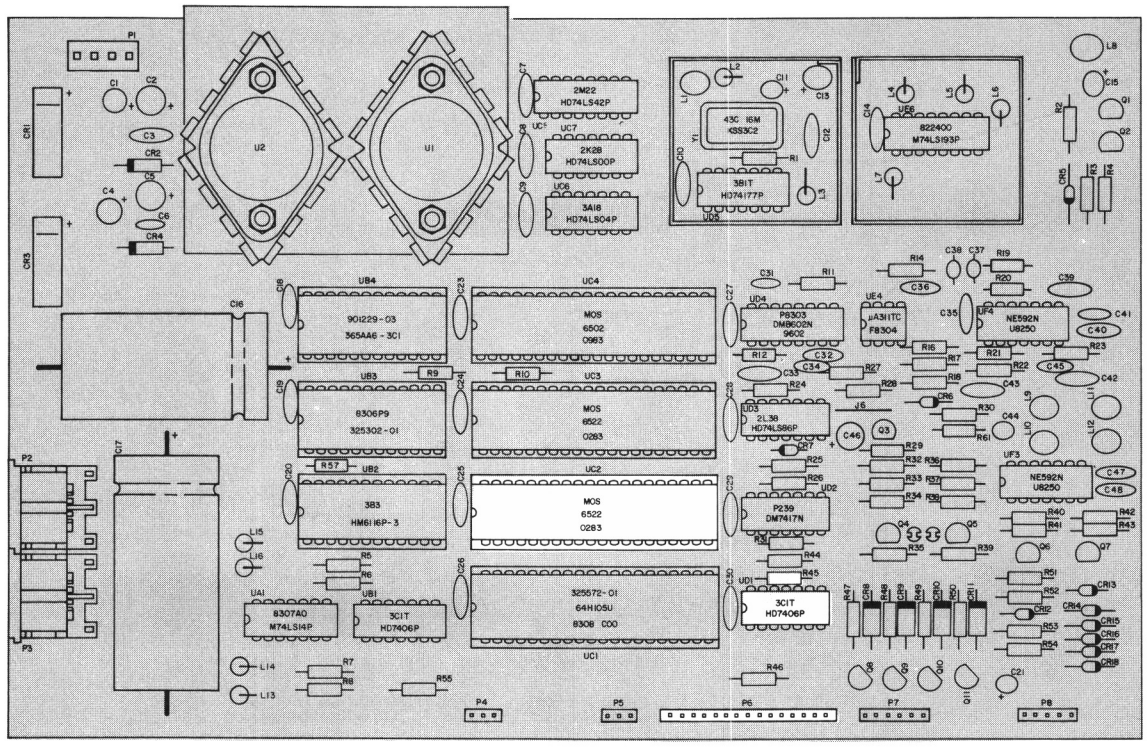


(A) 1540.

Fig. 5-2. Faulty red LED.



(B) 1541.



(C) 1542.

Fig. 5-2. Faulty red LED (cont.).

5.3 BASIC TROUBLESHOOTING FLOWCHART (cont.)

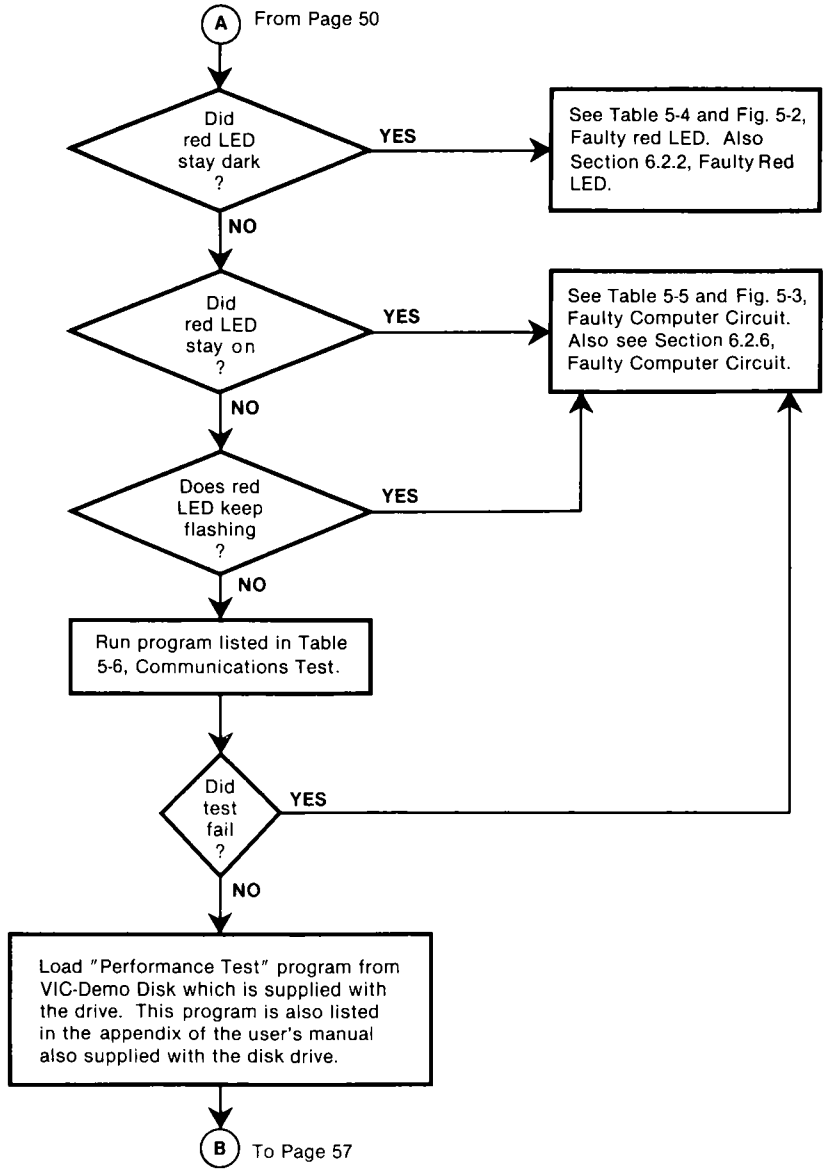
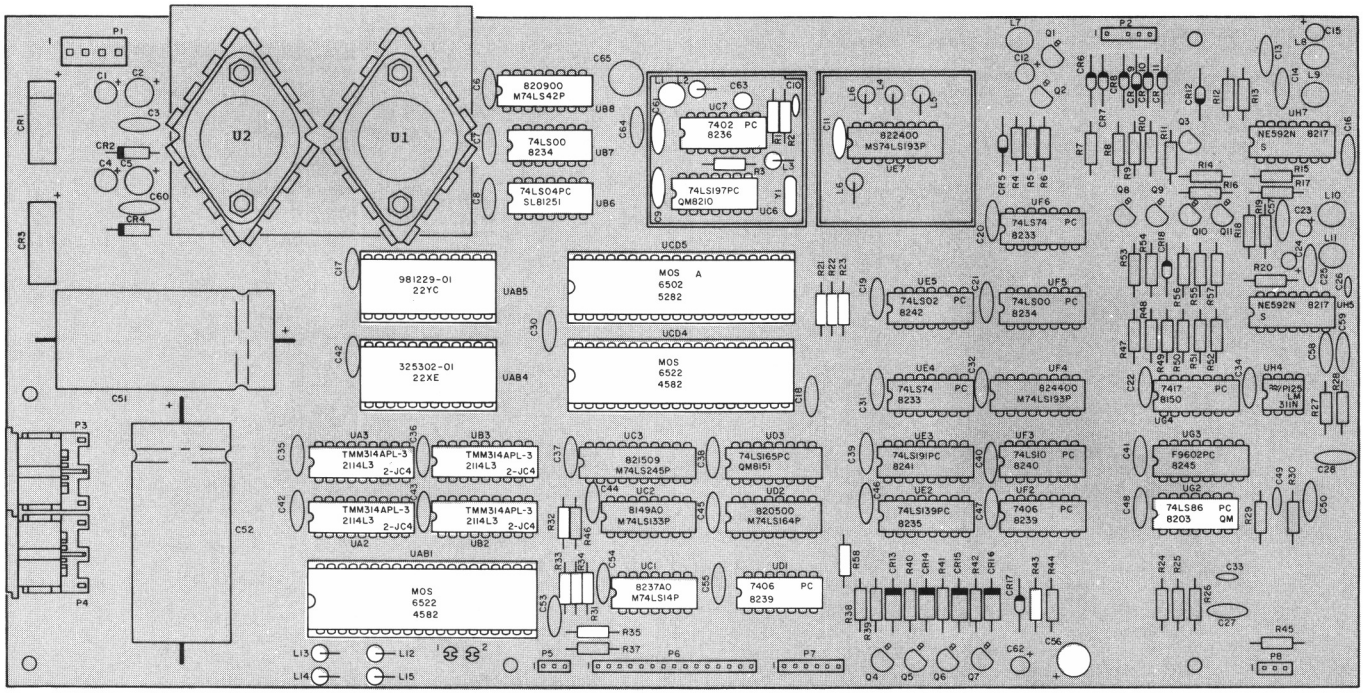
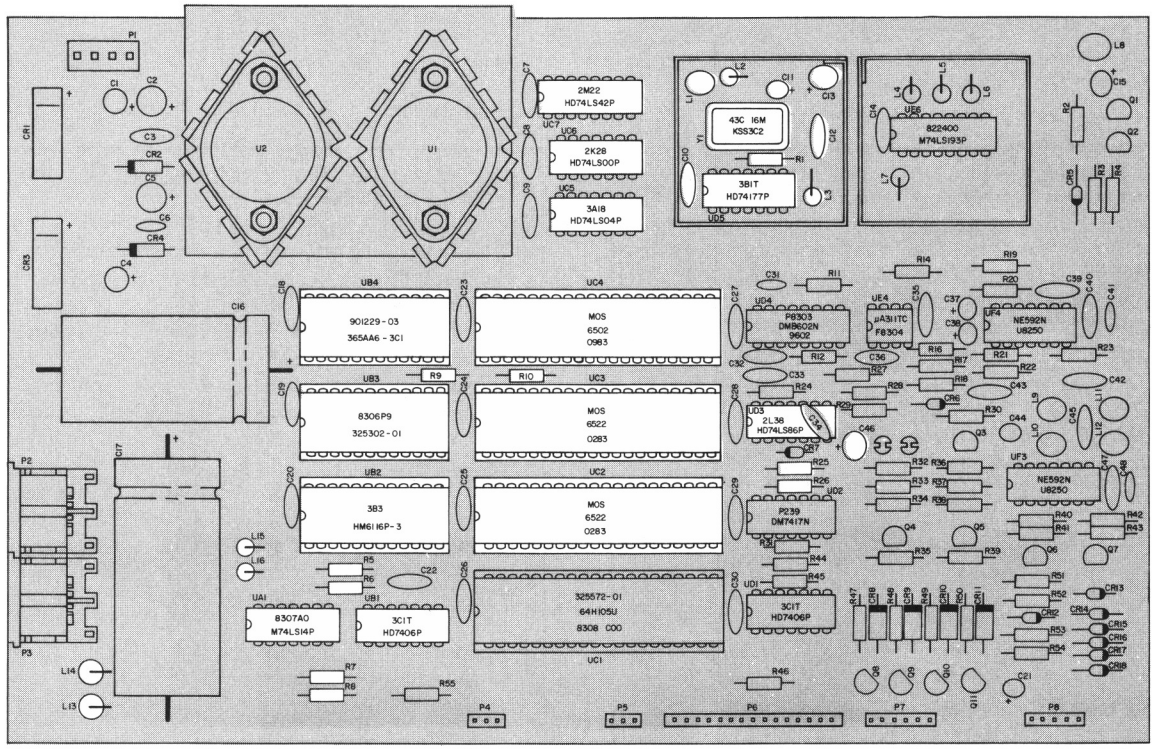


Table 5-4. Faulty Red LED

FAULTY PART IS ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
IC, UF2	IC, UD1	IC, UD1
IC, UCD4	IC, UC2	IC, UC2
Resistor, R36	Resistor R45	Resistor R45
Red LED	Red LED	Red LED
Connector, P6	Connector, P6	Connector, P6
Connector, J6	Connector, J6	Connector, J6

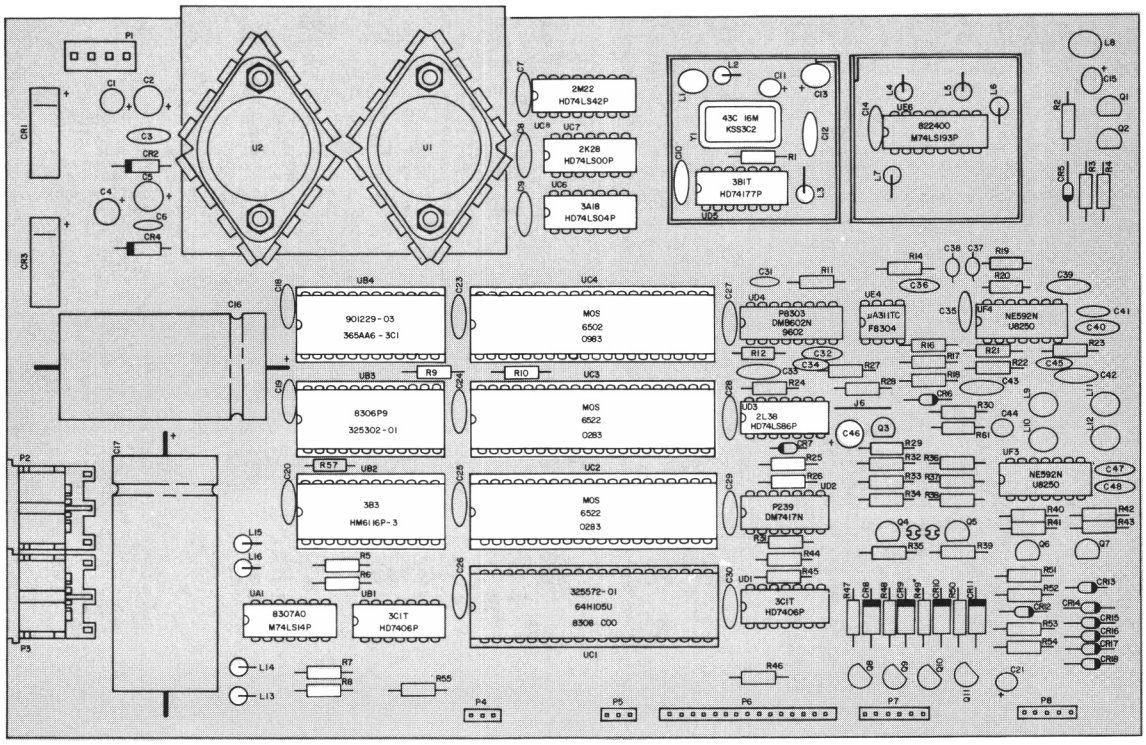


(A) 1540.



(B) 1541.

Fig. 5-3. Faulty computer circuit.



(C) 1542.

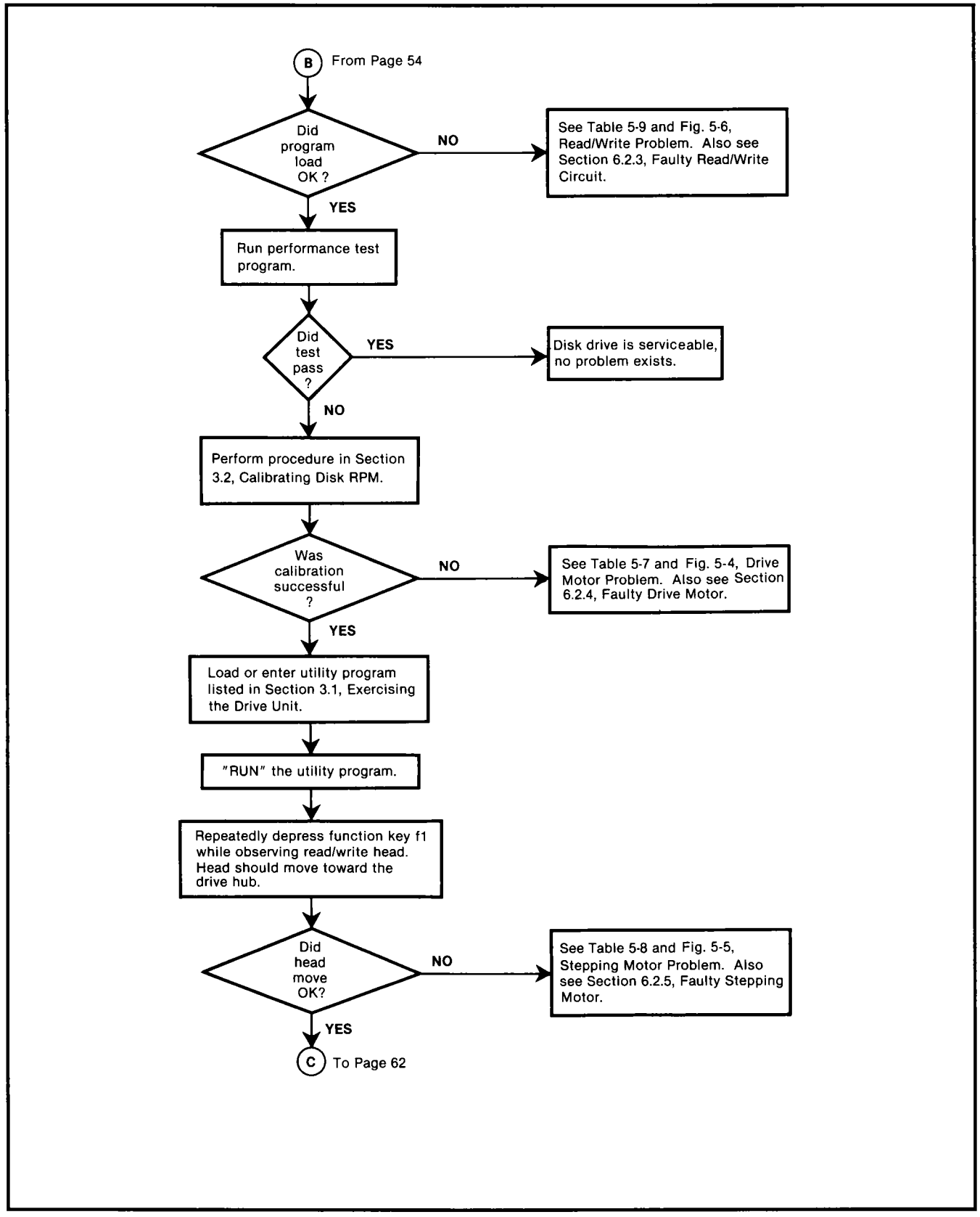
Fig. 5-3. Faulty computer circuit (cont.).

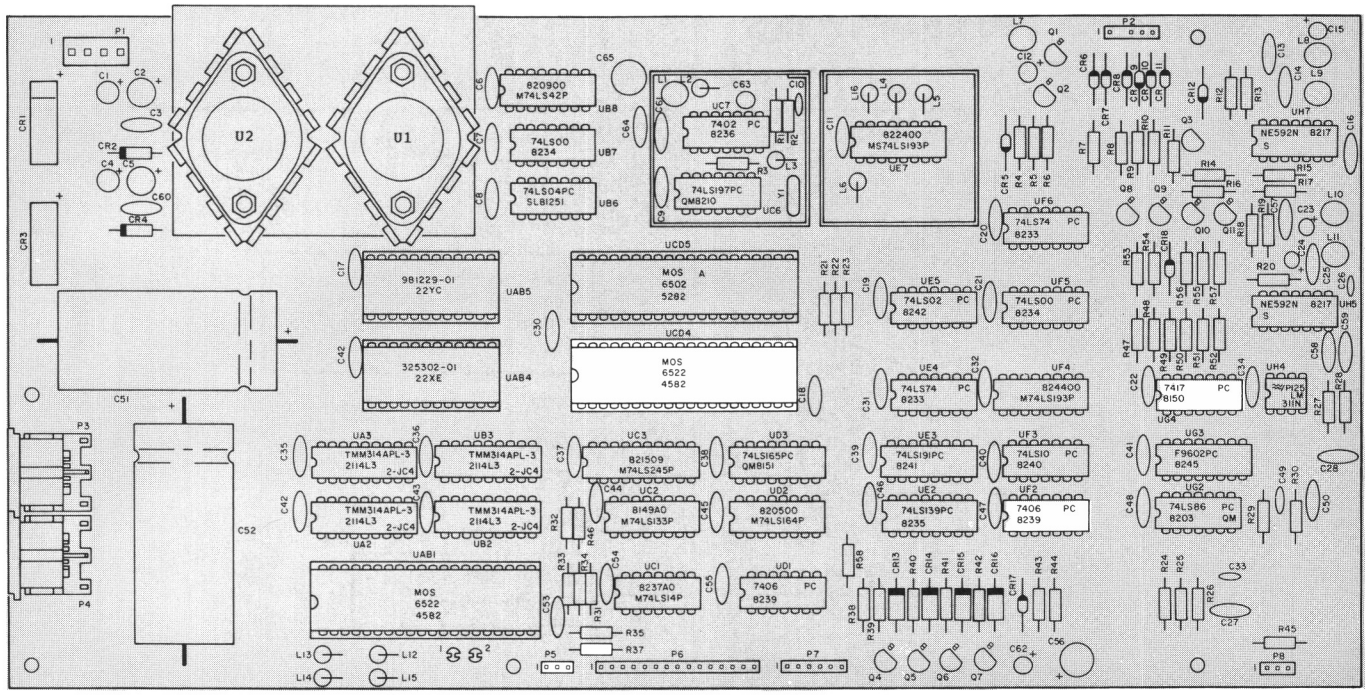
Table 5-5. Faulty Computer Circuit

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
MPU, UCD5	MPU, UC4	MPU, UC4
VIA, UAB1	VIA, UC3	VIA, UC3
VIA, UCD4	VIA, UC2	VIA, UC2
ROM, UAB5	ROM, UB4	ROM, UB4
ROM, UAB4	ROM, UB3	ROM, UB3
RAM, UB3	RAM, UB2	RAM, UB2
RAM, UA3	IC, UC7	IC, UC8
RAM, UB2	IC, UC6	IC, UC7
RAM, UA2	IC, UC5	IC, UC6
IC, UB8	IC, UA1	IC, UA1
IC, UB6	IC, UB1	IC, UB1
IC, UB7	IC, UD3	IC, UD3
IC, UC1	IC, UD5	IC, UD5
IC, UD1	Oscillator, Y1	Oscillator, Y1
IC, UG2	Resistor, R5	Resistor, R5
IC, UC6	Resistor, R6	Resistor, R6
IC, UC7	Resistor, R7	Resistor, R7
Crystal, Y1	Resistor, R8	Resistor, R8
Resistor, R1	Resistor, R9	Resistor, R9
Resistor, R2	Resistor, R10	Resistor, R10
Resistor, R3	Resistor, R25	Resistor, R25
Resistor, R21	Resistor, R26	Resistor, R26

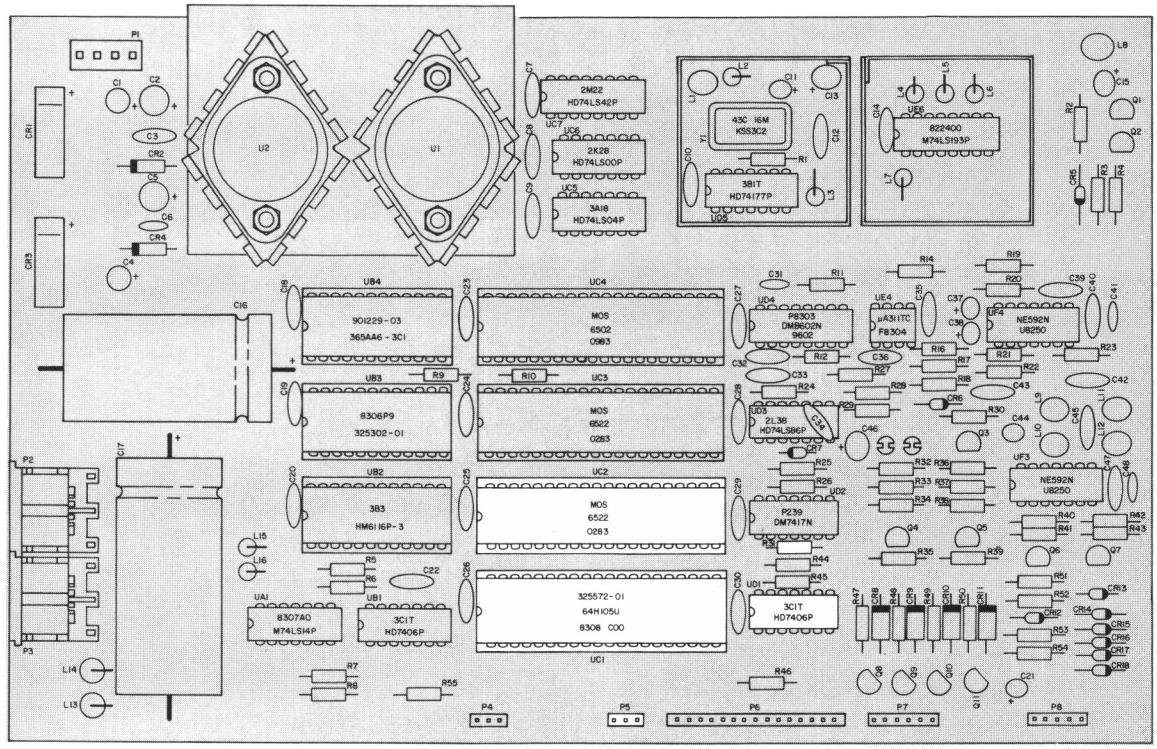
THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
Resistor, R22	Resistor, R1	Resistor, R1
Resistor, R23	Inductor, L1	Inductor, L1
Resistor, R31	Inductor, L2	Inductor, L2
Resistor, R32	Inductor, L3	Inductor, L3
Resistor, R33	Inductor, L13	Inductor, L13
Resistor, R34	Inductor, L14	Inductor, L14
Resistor, R35	Inductor, L15	Inductor, L15
Resistor, R43	Inductor, L16	Inductor, L16
Resistor, R58	Capacitor, C46	Capacitor, C46
Inductor, L1	Capacitor, C10	Capacitor, C10
Inductor, L2	Capacitor, C11	Capacitor, C11
Inductor, L3	Capacitor, C12	Capacitor, C12
Inductor, L12	Capacitor, C13	Capacitor, C13
Inductor, L13		
Inductor, L14		
Inductor, L15		
Capacitor, C56		
Capacitor, C9		
Capacitor, C10		
Capacitor, C61		
Capacitor, C63		
Capacitor, C11		

5.3 BASIC TROUBLESHOOTING FLOWCHART (cont.)



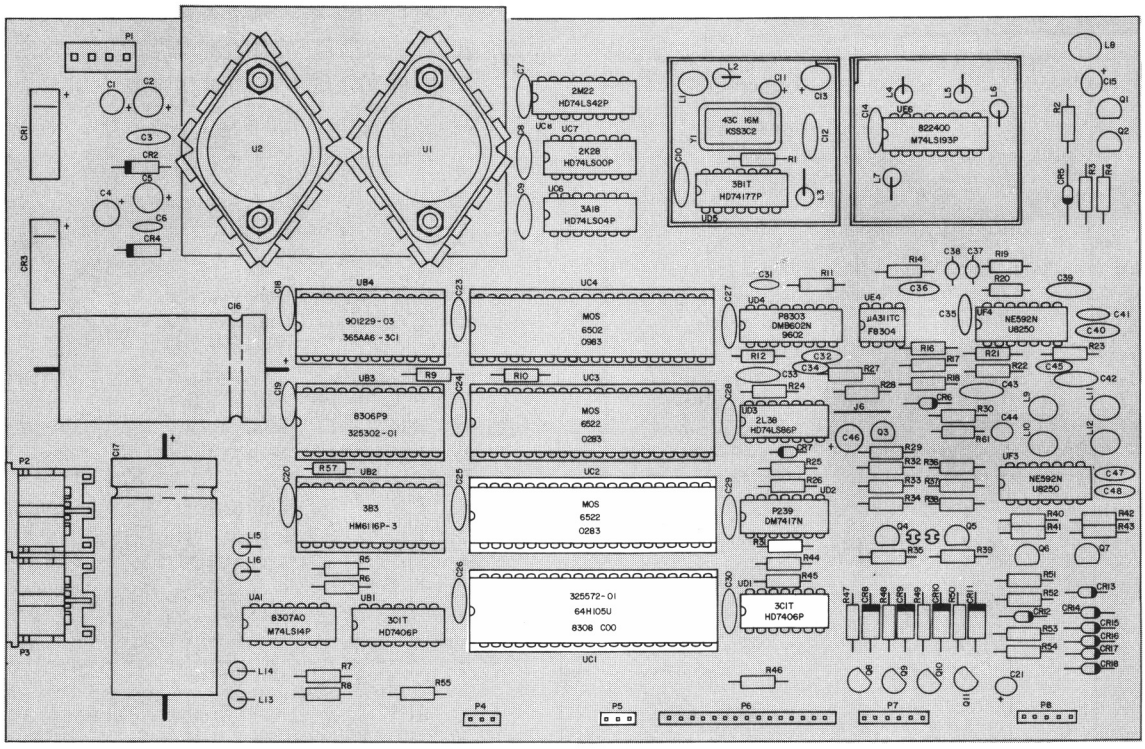


(A) 1540.



(B) 1541.

Fig. 5-4. Drive motor problem.



(C) 1542.

Fig. 5-4. Drive motor problem (cont.).

Table 5-6. Communications Test

TYPE THE FOLLOWING ONTO THE SCREEN:	
You Type This	`1 OPEN15,8,15:INPUT#15,A,A$,B,C:?A;A$;B;C <RETURN KEY>` `RUN <RETURN KEY>`
Correct Results, Test Passes	`00OK00` `READY.`
	Note: If computer responds with the following:

Test Fails	`DEVICE NOT PRESENT ERROR IN LINE 1`
	`READY.`
	Check for proper device number. If the VIC-1541 is not device No. 8, then change the "8" in line 1 to 9, 10, or 11, as applicable. Then "RUN" the program again. If device numbers are correct, then the VIC-1541 computer circuits are at fault. If the device number is unknown, see Section 1.3.2, "Changing Device Numbers."

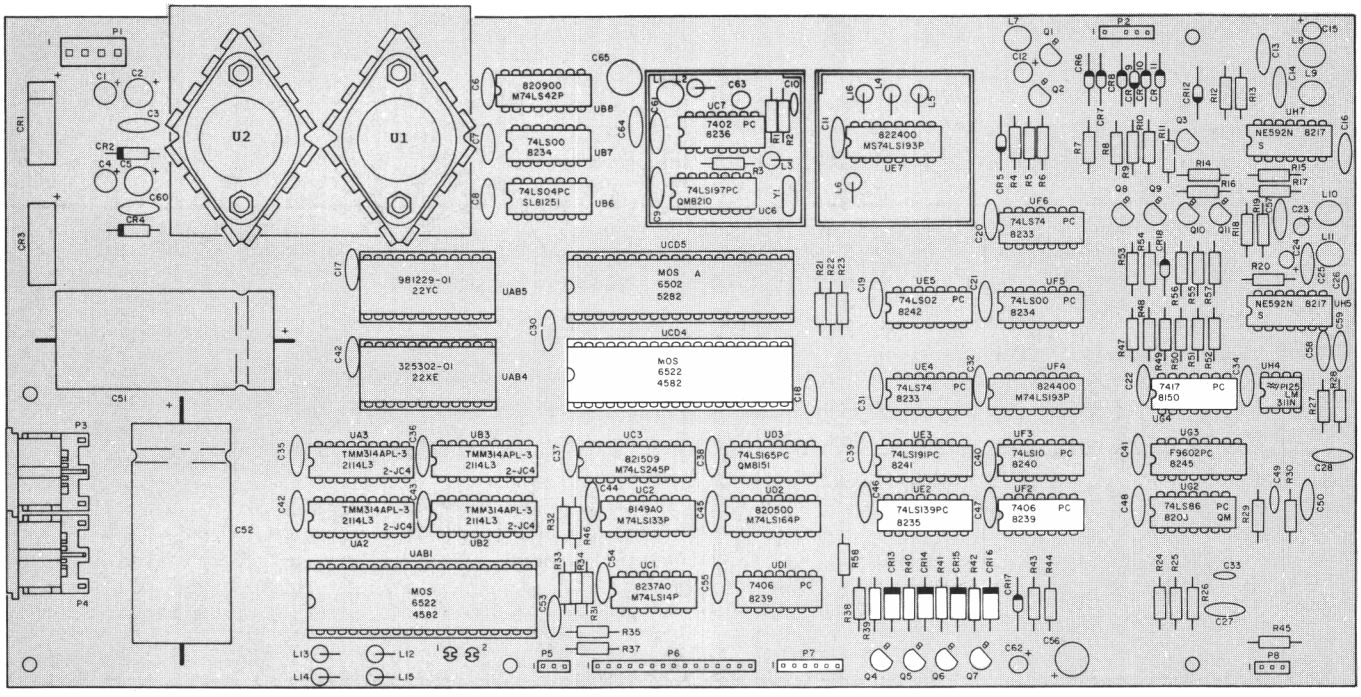
Test Fails	No response, cursor does not return.

Table 5-7. Drive Motor Problem

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
VIA, UCD4	VIA, UC2	VIA, UC2
IC, UF2	IC, UC1	IC, UC1
IC, UG4	IC, UD1	IC, UD1
Drive Motor, B1	Drive Motor, B1	Drive Motor, B1
Drive Motor Servo Circuit	Drive Motor Servo Circuit	Drive Motor Servo Circuit
Connector, P5	Connector, P5	Connector, P5
Resistor, R37	Resistor, R31	Resistor, R31
Drive Unit Moving Parts	Drive Unit Moving Parts	Drive Unit Moving Parts
Connector, J5	Connector, J5	Connector, J5

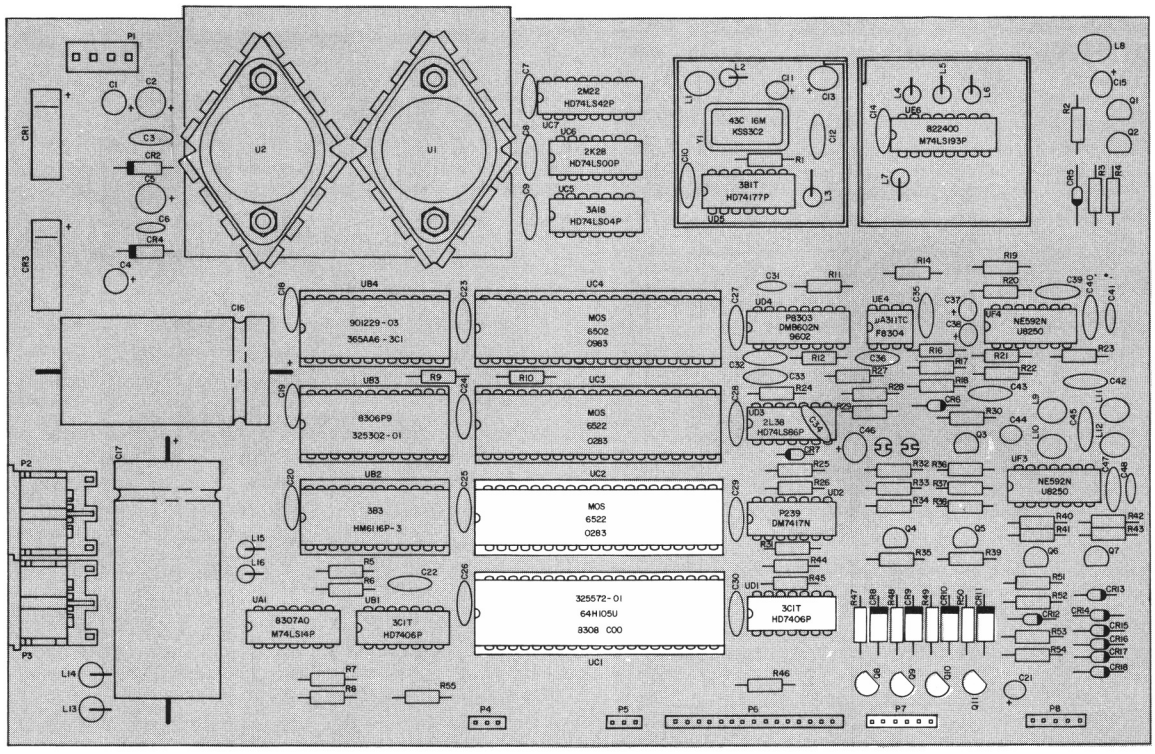
Table 5-8. Stepping Motor Problem

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
VIA, UCD4	VIA, UC2	VIA, UC2
IC, UF2	IC, UC1	IC, UC1
IC, UG4	IC, UD1	IC, UD1
IC, UE2	-	-
Transistor, Q4	Transistor, Q8	Transistor, Q8
Transistor, Q5	Transistor, Q9	Transistor, Q9
Transistor, Q6	Transistor, Q10	Transistor, Q10
Transistor, Q7	Transistor, Q11	Transistor, Q11
Diode, CR13	Diode, CR8	Diode, CR8
Diode, CR14	Diode, CR9	Diode, CR9
Diode, CR15	Diode, CR10	Diode, CR10
Diode, CR16	Diode, CR11	Diode, CR11
Resistor, R39	Resistor, R47	Resistor, R47
Resistor, R40	Resistor, R48	Resistor, R48
Resistor, R41	Resistor, R49	Resistor, R49
Resistor, R42	Resistor, R50	Resistor, R50
Connector, P7	Connector, P7	Connector, P7
Connector, J7	Connector, J7	Connector, J7

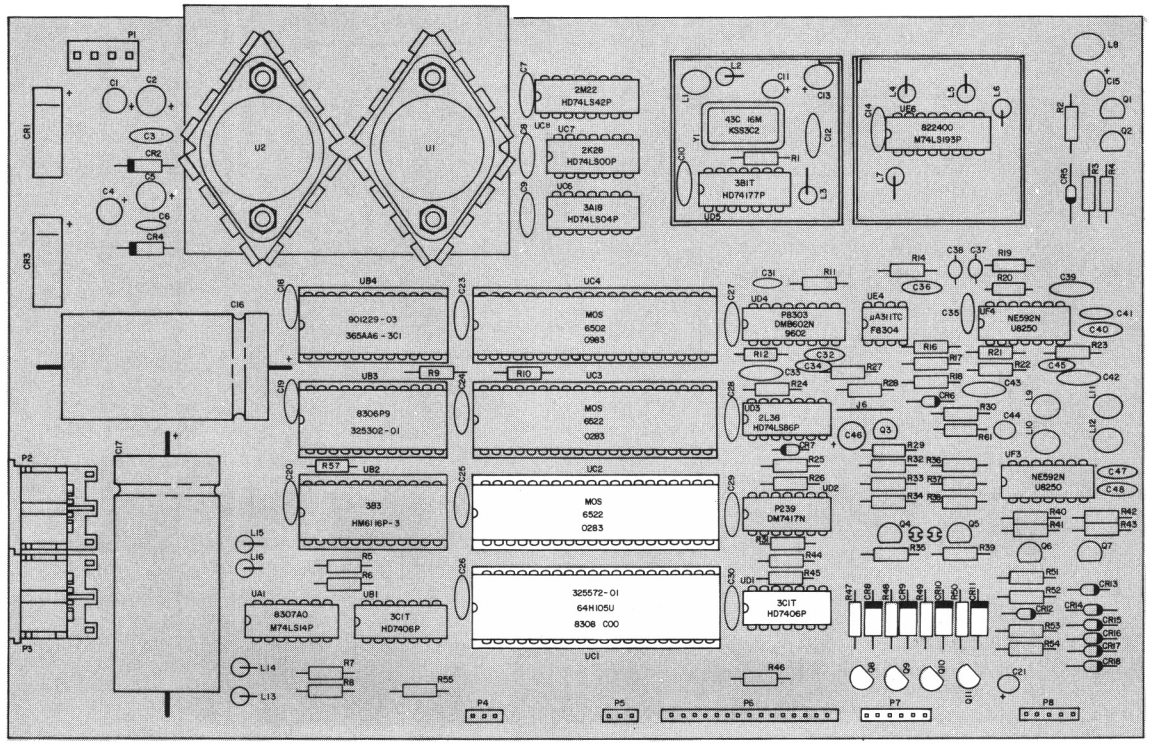


(A) 1540.

Fig. 5-5. Stepping motor problem.



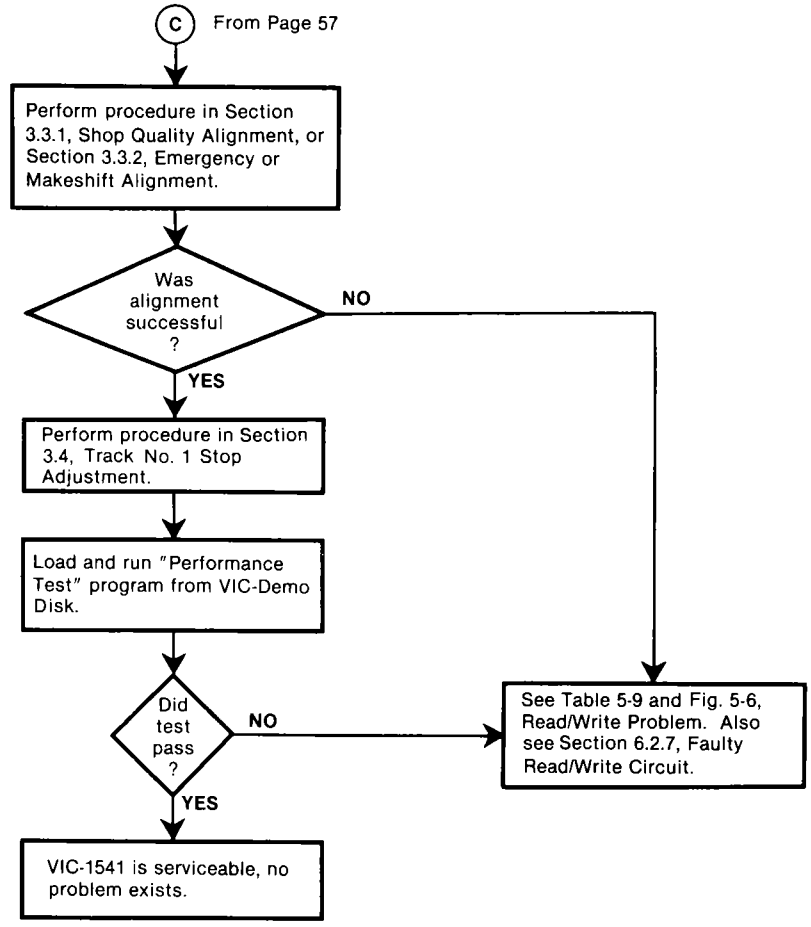
(B) 1541.

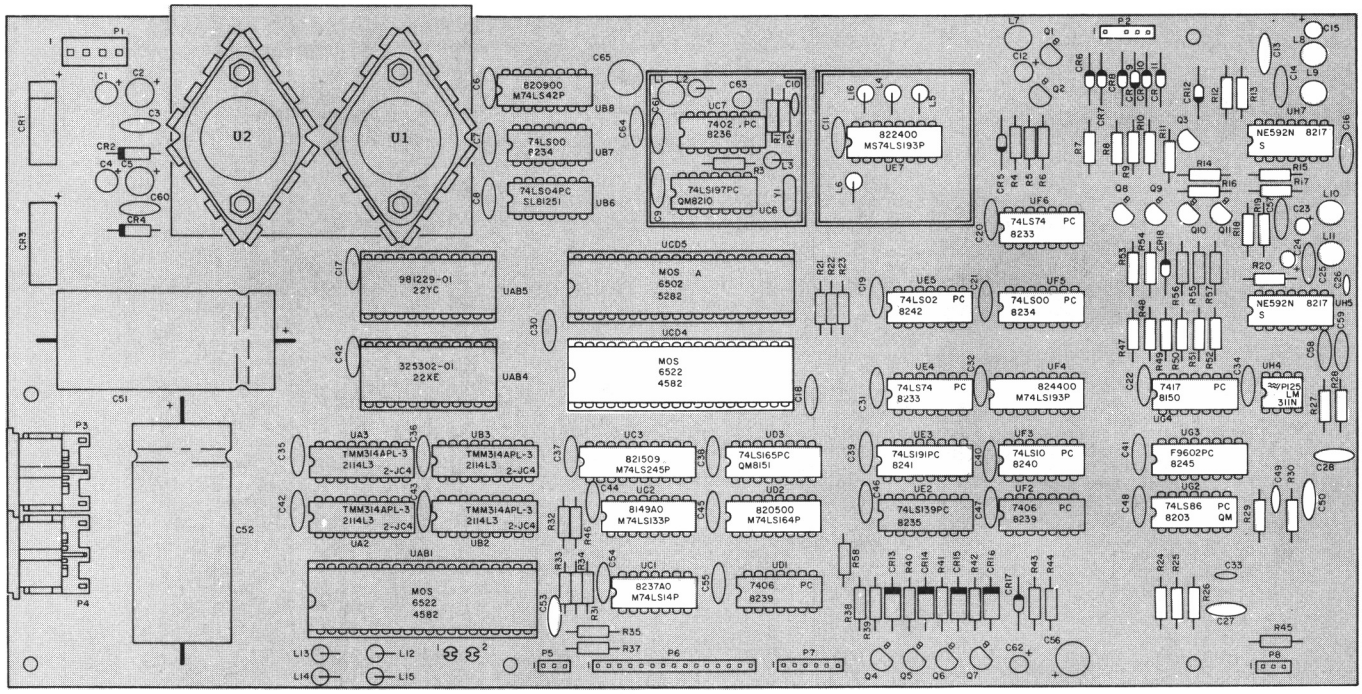


(C) 1542.

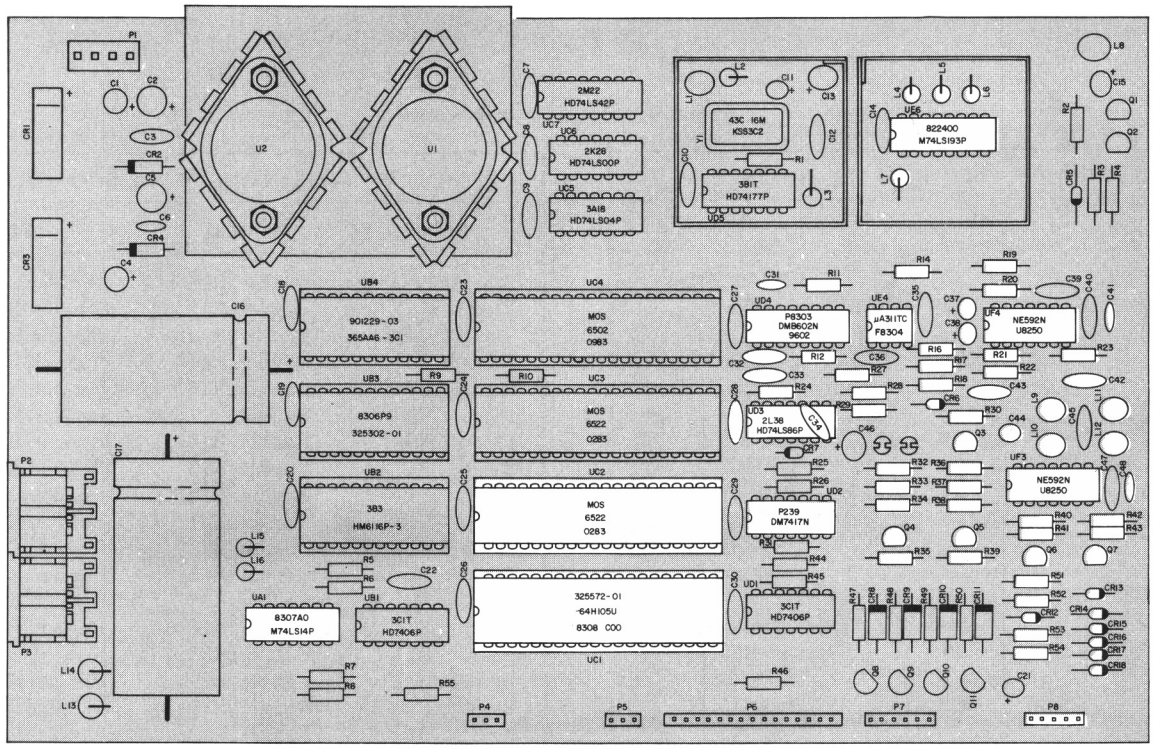
Fig. 5-5. Stepping motor problem (cont.).

5.3 BASIC TROUBLESHOOTING FLOWCHART (cont.)



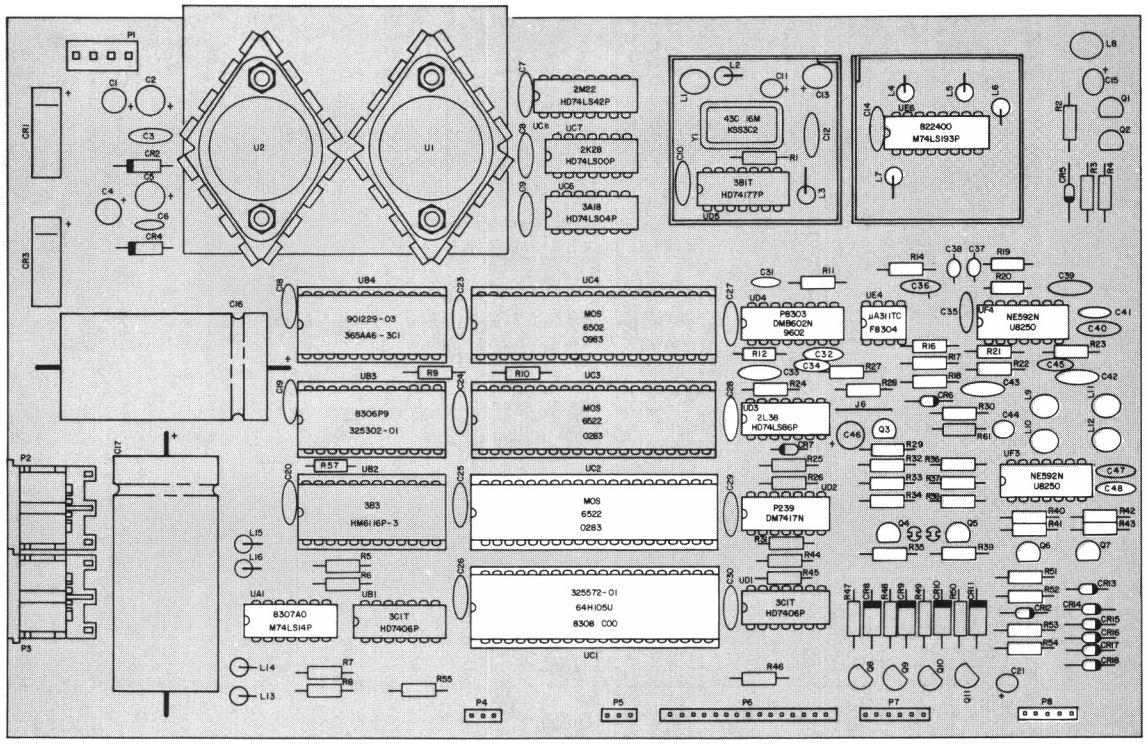


(A) 1540.



(B) 1541.

Fig. 5-6. Read/write problem.



(C) 1542.

Fig. 5-6. Read/write problem (cont.).

Table 5-9. Read/Write Problem

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
VIA, UCD4	VIA, UC2	VIA, UC2
IC, UE7	IC, UE6	IC, UE6
IC, UE5	IC, UC1	IC, UC1
IC, UF4	IC, UD2	IC, UD2
IC, UE3	IC, UF3	IC, UF3
IC, UF3	IC, UF4	IC, UF4
IC, UC1	IC, UE4	IC, UE4
IC, UD2	IC, UD3	IC, UD3
IC, UC2	IC, UD4	IC, UD4
IC, UC3	IC, UA1	IC, UA1
IC, UD3	Transistor, Q3	Transistor, Q3
IC, UE4	Transistor, Q4	Transistor, Q4
IC, UF5	Transistor, Q5	Transistor, Q5
IC, UG2	Transistor, Q6	Transistor, Q6
IC, UG4	Transistor, Q7	Transistor, Q7
IC, UF6	Diode, CR6	Diode, CR6
IC, UH7	Diode, CR12	Diode, CR12
IC, UH5	Diode, CR13	Diode, CR13
IC, UH4	Diode, CR14	Diode, CR14
IC, UG3	Diode, CR15	Diode, CR15
Transistor, Q3	Diode, CR16	Diode, CR16
Transistor, Q8	Diode, CR17	Diode, CR17

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
Transistor, Q9	Diode, CR18	Diode, CR18
Transistor, Q10	Resistor, R11	Resistor, R11
Transistor, Q11	Resistor, R12	Resistor, R12
Diode, CR6	Resistor, R14	Resistor, R14
Diode, CR7	Resistor, R16	Resistor, R16
Diode, CR8	Resistor, R17	Resistor, R17
Diode, CR9	Resistor, R18	Resistor, R18
Diode, CR10	Resistor, R19	Resistor, R19
Diode, CR11	Resistor, R20	Resistor, R20
Diode, CR12	Resistor, R21	Resistor, R21
Diode, CR18	Resistor, R22	Resistor, R22
Resistor, R8	Resistor, R23	Resistor, R23
Resistor, R9	Resistor, R24	Resistor, R24
Resistor, R10	Resistor, R27	Resistor, R27
Resistor, R11	Resistor, R28	Resistor, R28
Resistor, R12	Resistor, R29	Resistor, R29
Resistor, R13	Resistor, R30	Resistor, R30
Resistor, R14	Resistor, R32	Resistor, R32
Resistor, R15	Resistor, R33	Resistor, R33
Resistor, R16	Resistor, R34	Resistor, R34
Resistor, R17	Resistor, R35	Resistor, R35
Resistor, R18	Resistor, R36	Resistor, R36

Table 5-9. Read/Write Problem (cont.)

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
Resistor, R19	Resistor, R37	Resistor, R37
Resistor, R20	Resistor, R38	Resistor, R38
Resistor, R24	Resistor, R39	Resistor, R39
Resistor, R25	Resistor, R40	Resistor, R40
Resistor, R26	Resistor, R41	Resistor, R41
Resistor, R27	Resistor, R42	Resistor, R42
Resistor, R28	Resistor, R43	Resistor, R43
Resistor, R29	Resistor, R51	Resistor, R51
Resistor, R30	Resistor, R52	Resistor, R52
Resistor, R7	Resistor, R53	Resistor, R53
Resistor, R47	Resistor, R54	Resistor, R54
Resistor, R48	Capacitor, C28	Capacitor, C28
Resistor, R49	Capacitor, C31	Capacitor, C31
Resistor, R50	Capacitor, C32	Capacitor, C32
Resistor, R51	Capacitor, C33	Capacitor, C33
Resistor, R52	Capacitor, C34	Capacitor, C34
Resistor, R53	Capacitor, C37	Capacitor, C37
Resistor, R54	Capacitor, C38	Capacitor, C38
Capacitor, C13	Capacitor, C41	Capacitor, C41
Capacitor, C15	Capacitor, C42	Capacitor, C42

THE PROBLEM IS IN ONE OF THE FOLLOWING:		
1540	**1541**	**1542**
Capacitor, C23	Capacitor, C43	Capacitor, C43
Capacitor, C24	Capacitor, C44	Capacitor, C44
Capacitor, C26	Capacitor, C48	Capacitor, C48
Capacitor, C27	Inductor, L4	Inductor, L4
Capacitor, C28	Inductor, L5	Inductor, L5
Capacitor, C49	Inductor, L6	Inductor, L6
Capacitor, C50	Inductor, L7	Inductor, L7
Capacitor, C53	Inductor, L9	Inductor, L9
Inductor, L4	Inductor, L10	Inductor, L10
Inductor, L5	Inductor, L11	Inductor, L11
Inductor, L6	Inductor, L12	Inductor, L12
Inductor, L8	Connector, P8	Connector, P8
Inductor, L9	Connector, J8	Connector, J8
Inductor, L10	Read/Write Head	Read/Write Head
Inductor, L11		
Inductor, L16		
Connector, P2		
Connector, J2		
Read/Write Head		

CHAPTER 6

Advanced Troubleshooting and Repair

This chapter contains advanced troubleshooting instructions for your VIC-1541. If you have not attempted to troubleshoot your VIC-1541 using Chapter 5, "Basic Troubleshooting and Repair," please do so as that is prerequisite to this chapter. Most common malfunctions, such as misalignment, are corrected by Chapter 5. However, if the malfunction is caused by a faulty component, this chapter may be used to isolate it.

6.1 INTRODUCTION TO ADVANCED TROUBLESHOOTING

After troubleshooting the problem down to a group of parts using Chapter 5, use this chapter to isolate the problem. First, consult the applicable flowchart in Section 6.2. To use those flowcharts, you will need to know how to use a multimeter and, depending on the nature of the problem, you might also need to use an oscilloscope. If you are not familiar with the use of those pieces of test equipment, read the applicable books listed here:

Analog Instrumentation Fundamentals, by Vincent F. Leonard, Jr. Howard W. Sams & Co., 1981.(Cat. No. 21835)

Know Your Oscilloscope, 4th Ed., by Robert G. Middleton. Howard W. Sams & Co., 1980. (Cat. No. 21742)

Troubleshooting With the Oscilloscope, 4th Ed., by Robert G. Middleton. Howard W. Sams & Co., 1980. (Cat. No. 21738)

Another option for those with technical experience is to read Chapter 7, "Advanced Theory of Operation," then consult Appendix A, "Technical Data." Chapter 7 and Appendix A contain enough data to enable an experienced technician to analyze and trace the problem to a specific part. The following instructions are applicable to the flowcharts in Section 6.2.

When measuring voltage, the flowcharts will usually specify two points to measure between. Some examples of this are, "Measure voltage between pins 1 and 3 of P5" and "Measure voltage across R3." In the first example, you would place one of the voltmeter test leads on pin 1 and the other on pin 3. In the second example, you would place one of the voltmeter leads on one of the leads of R3 and place the other voltmeter lead on the remaining lead of R3. In some cases, the flowcharts may only give one point to measure. An example of this is "Measure voltage at pin 2 of UC2." In this

case, the measurement is taken between pin 2 of integrated circuit UC2 and the circuit ground. It is important to know that the frame of the VIC-1541 is not circuit ground. Circuit ground may be found on pin 1 of connector P5.

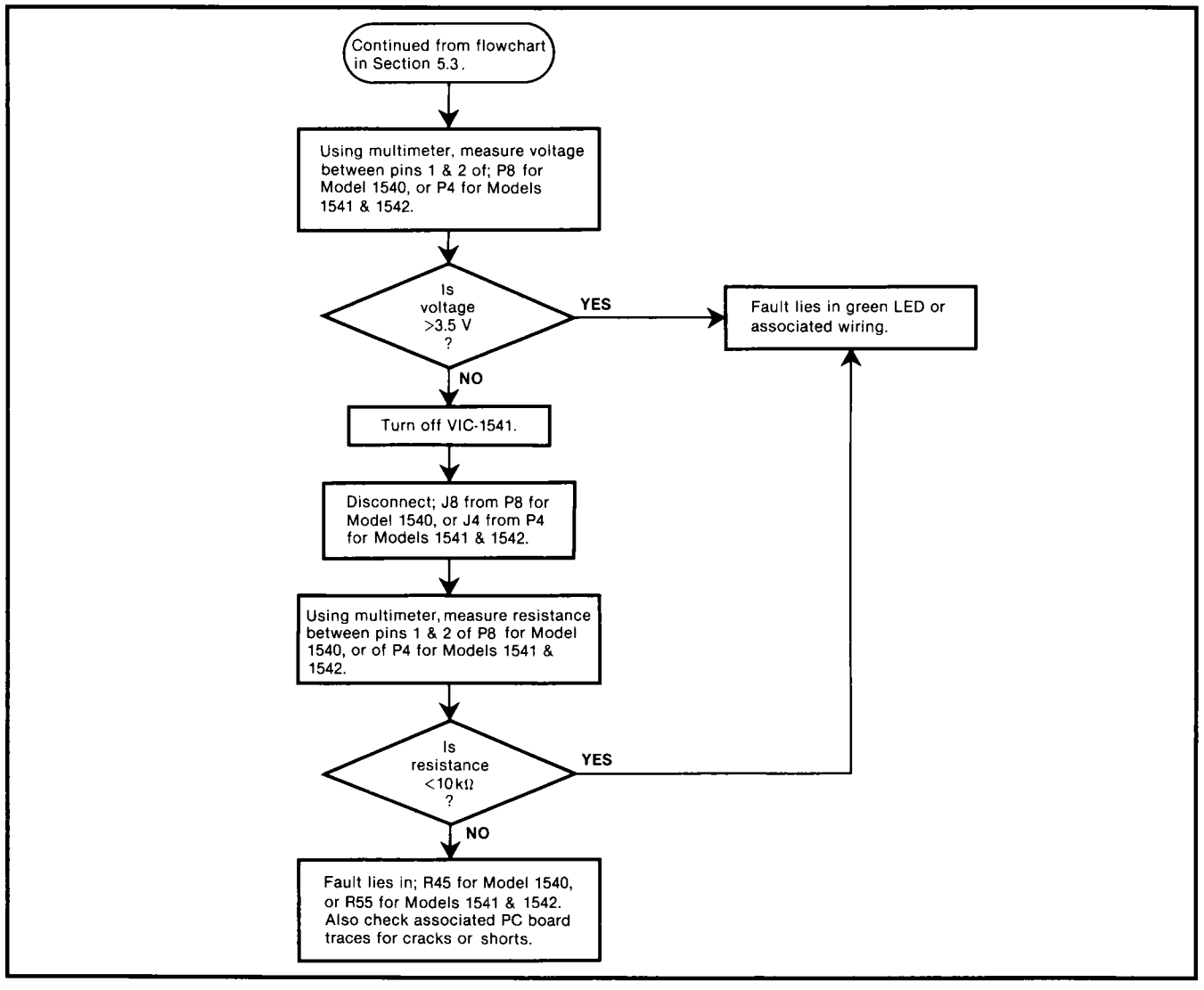
Once you are given a test point or component to measure across, you may locate this component by referring to Appendix A, Section A.4, "VIC-1541 Parts Layouts." Section A.1 has an index to help you locate the illustration pertaining to the subassembly you are troubleshooting. If you are not familiar with the pin numbering scheme of integrated circuits, consult Appendix D.

The flowcharts may list more than one set of test points. An example of this is, "Measure voltage across; R3 for Model 1540, or R4 for Models 1541 and 1542." Be sure to use the information which applies to the particular model that you are troubleshooting. If only one set of test points is listed without mention of a model number, that test point applies to all models.

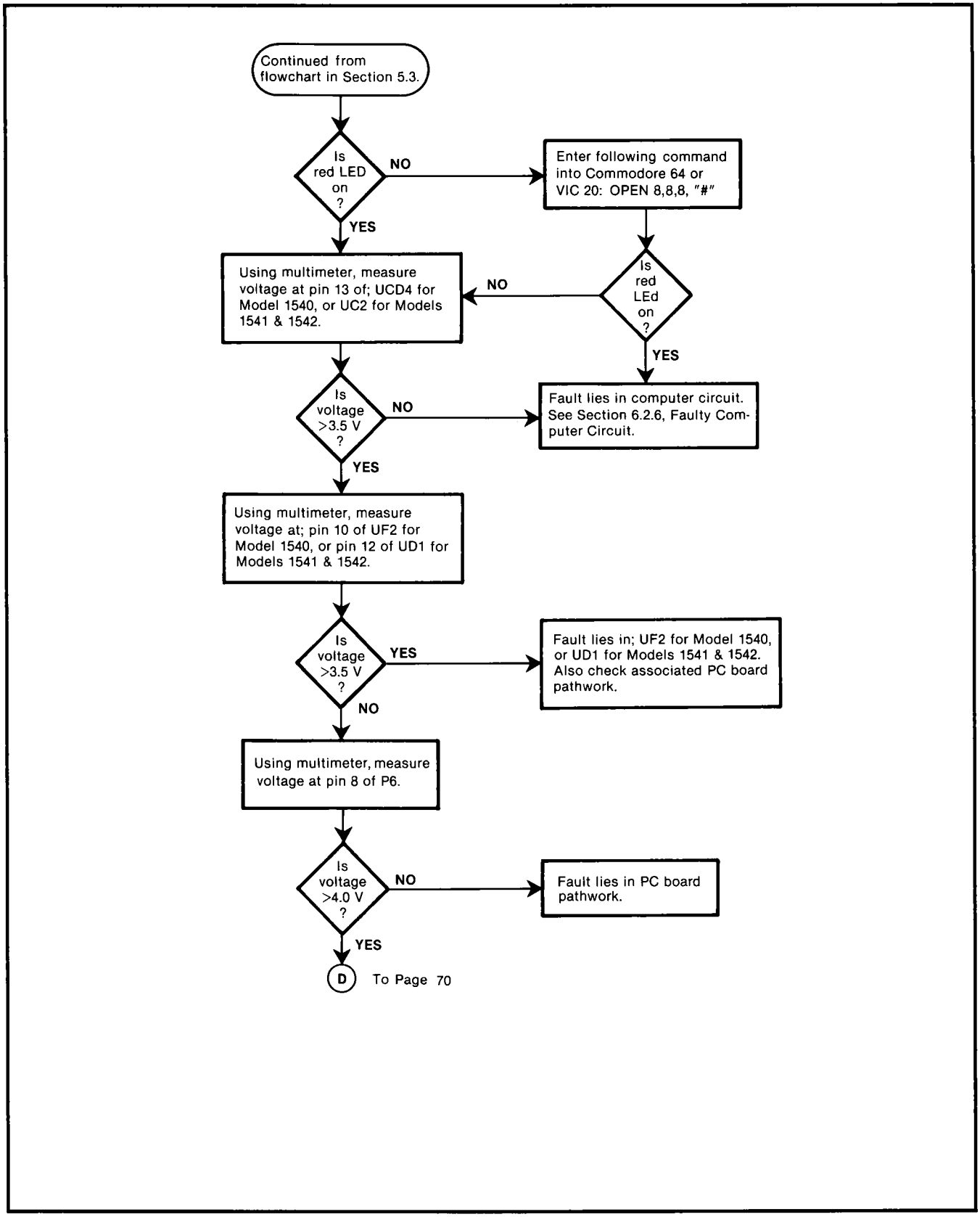
6.2 ADVANCED TROUBLESHOOTING FLOWCHARTS

This section contains advanced troubleshooting flowcharts which are essentially a continuation of the flowchart in Section 5.3. Read Sections 5.2 and 6.1 prior to performing the flowcharts which follow.

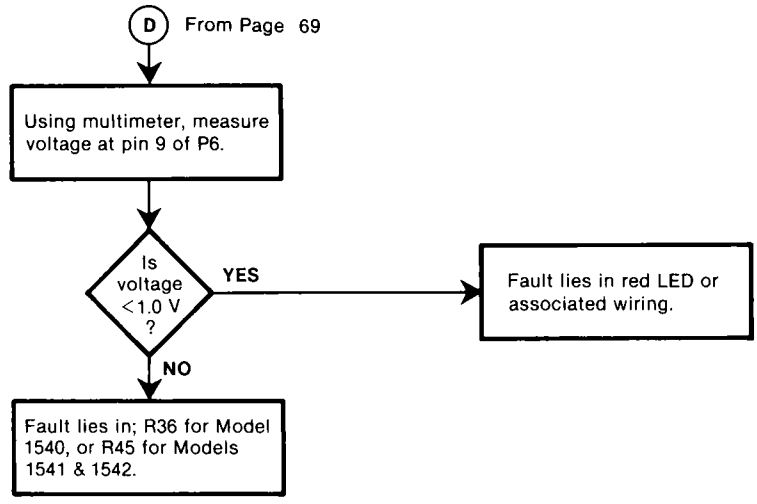
6.2.1 Faulty Green LED



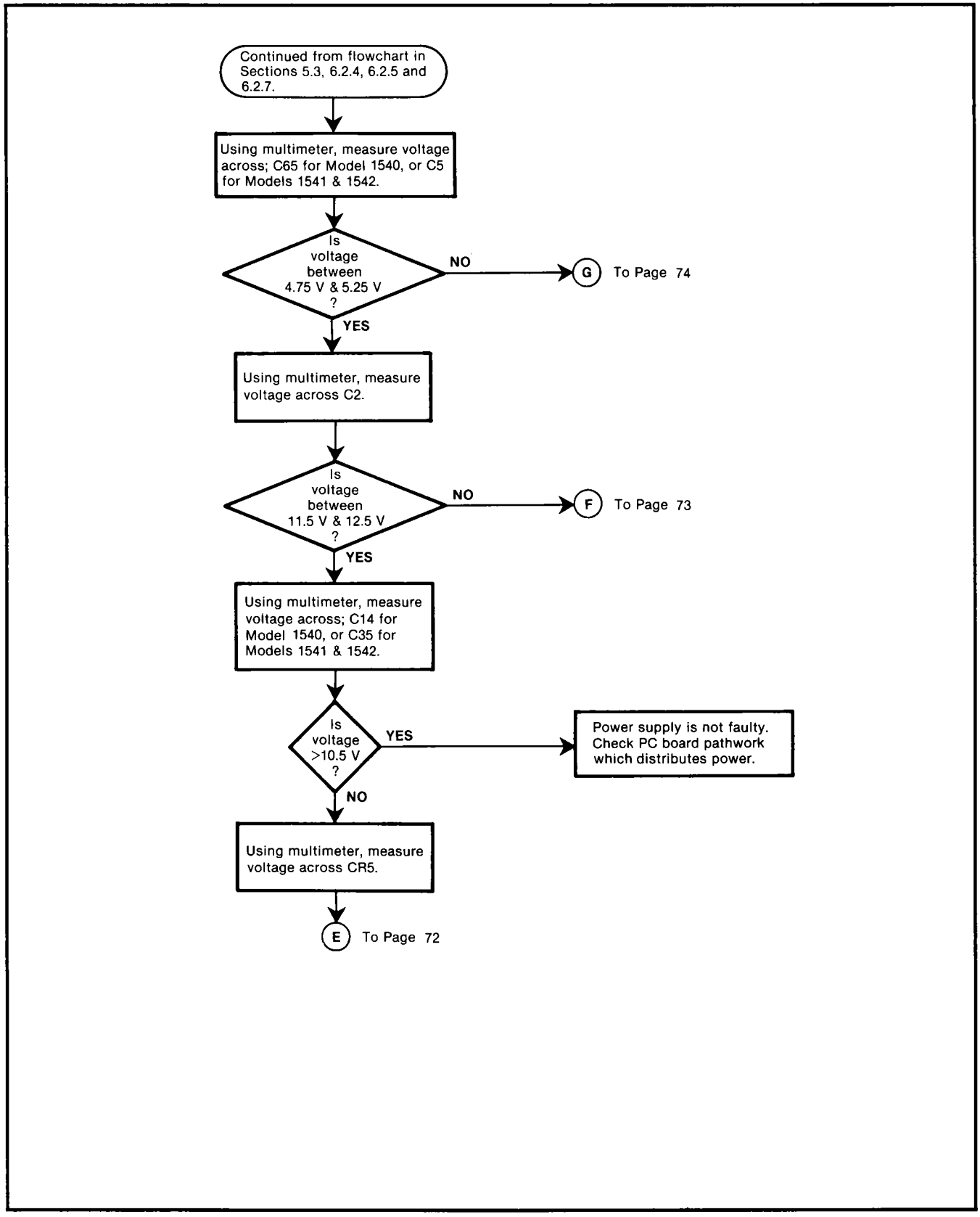
6.2.2 Faulty Red LED



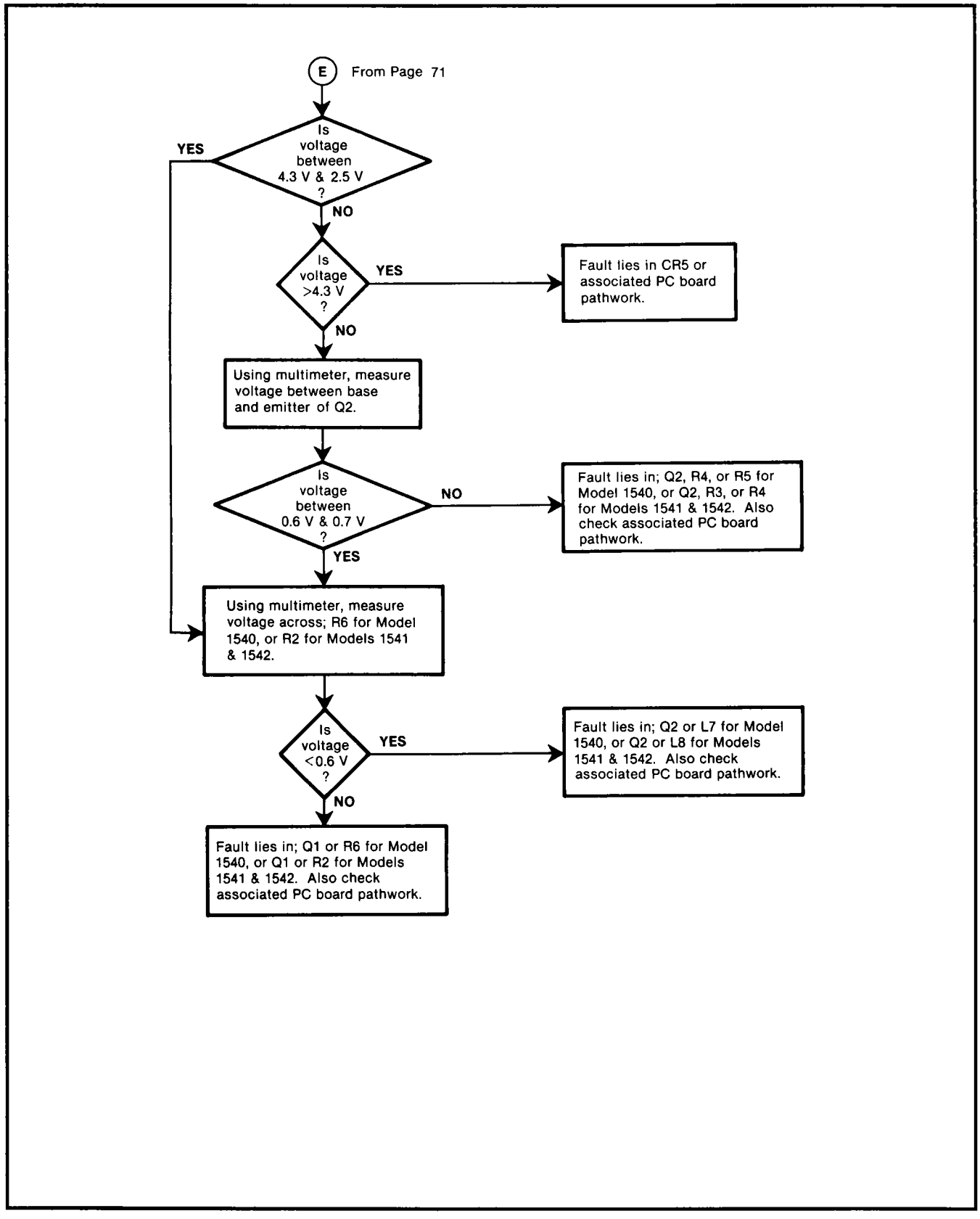
6.2.2 Faulty Red LED (cont.)



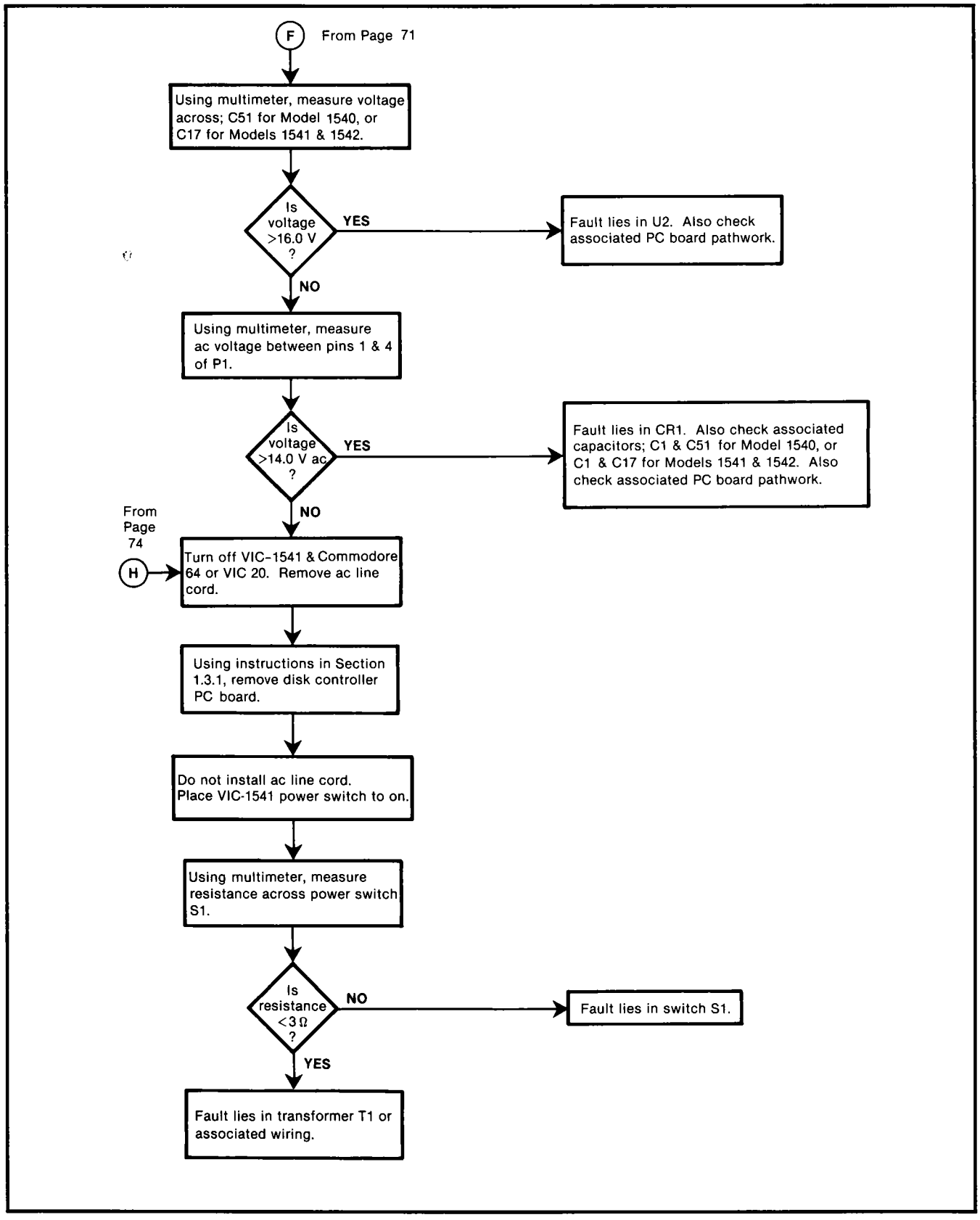
6.2.3 Faulty Power Supply



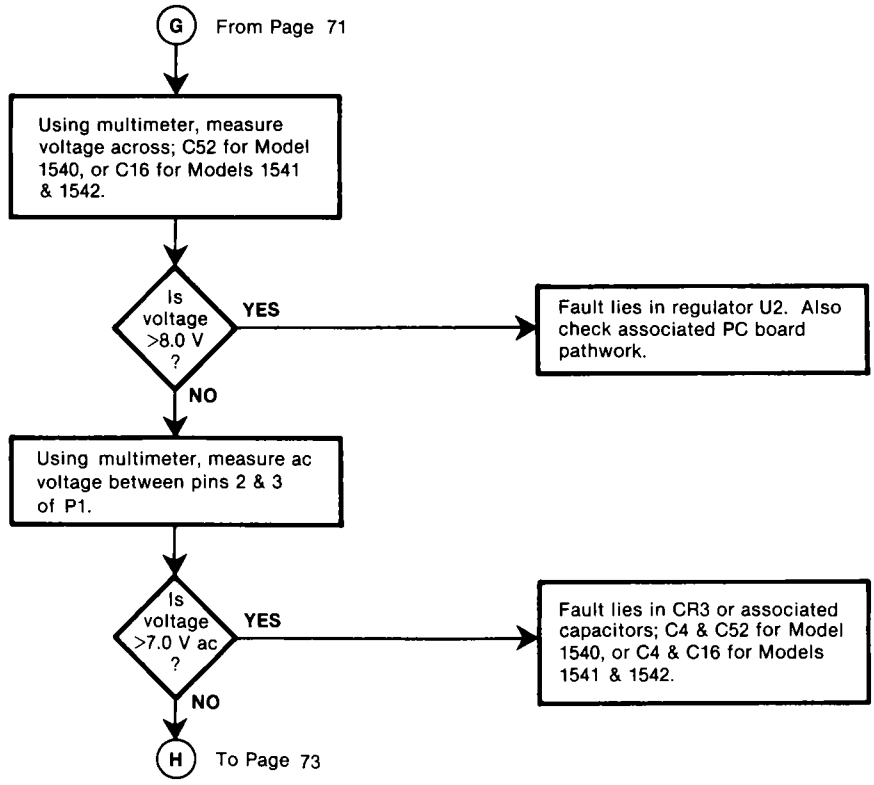
6.2.3 Faulty Power Supply (cont.)



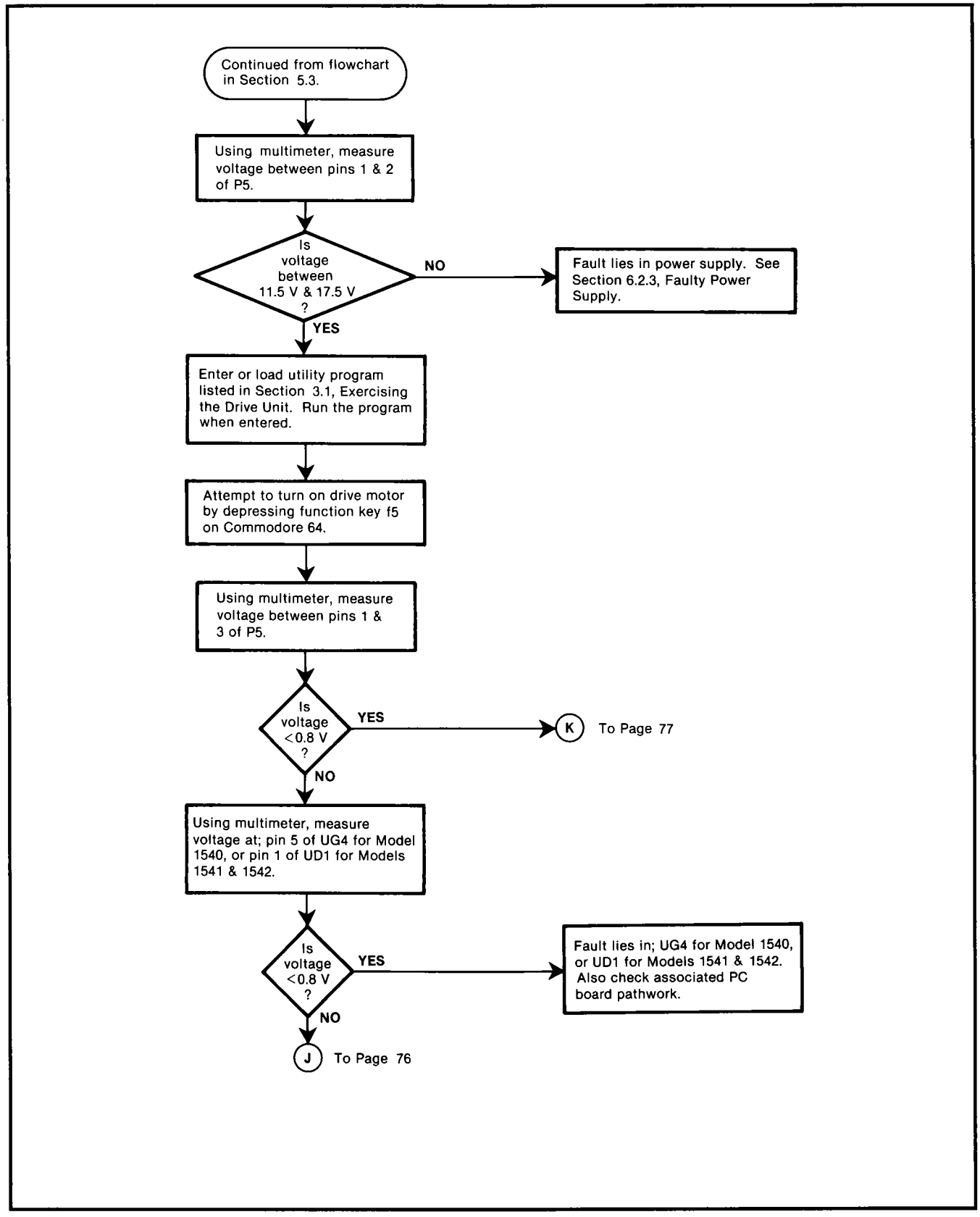
6.2.3 Faulty Power Supply (cont.)



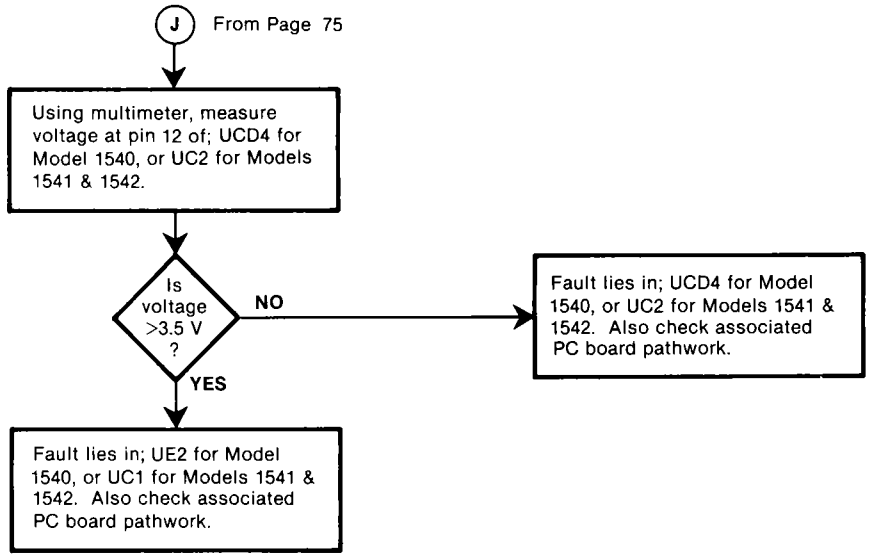
6.2.3 Faulty Power Supply (cont.)



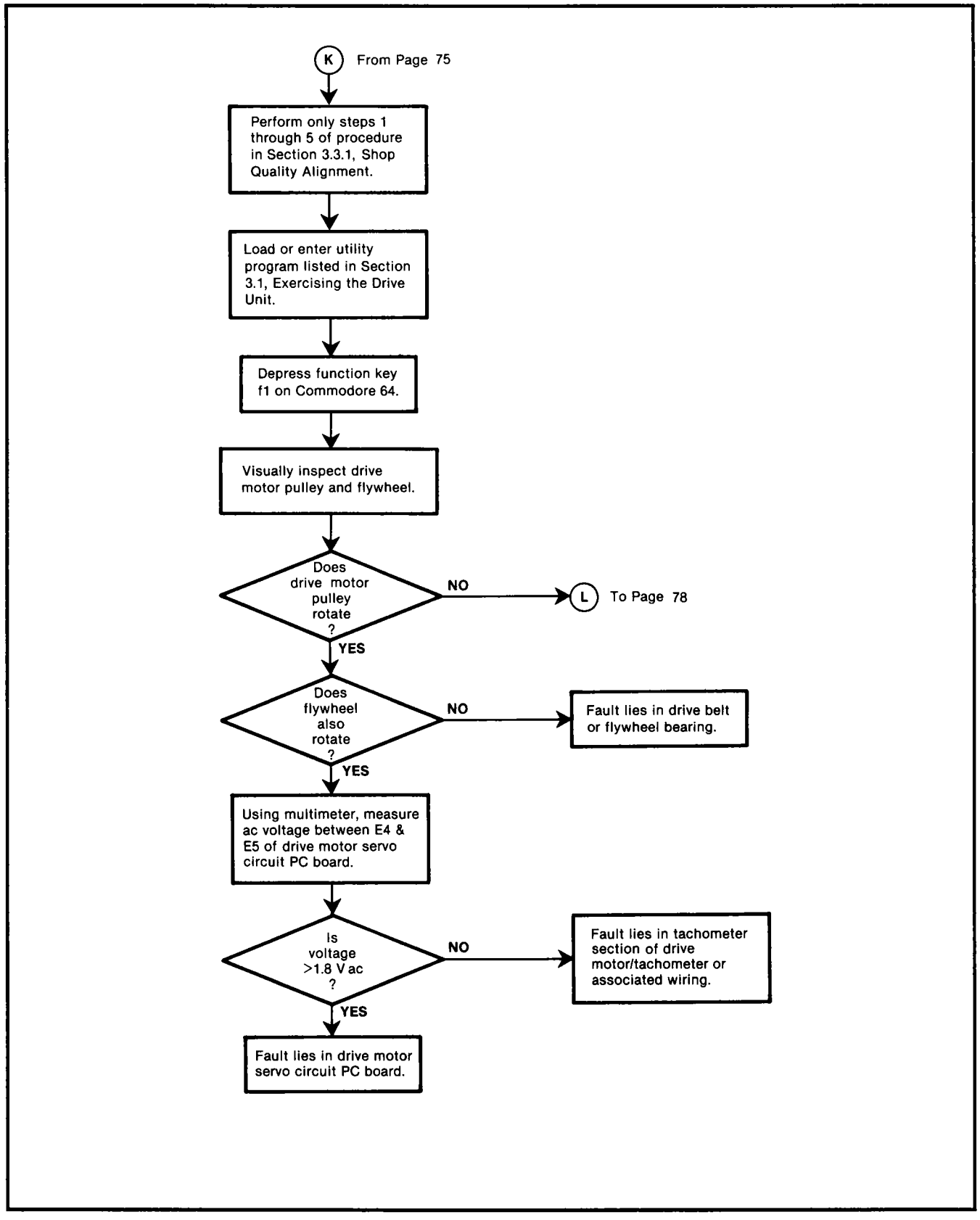
6.2.4 Faulty Drive Motor



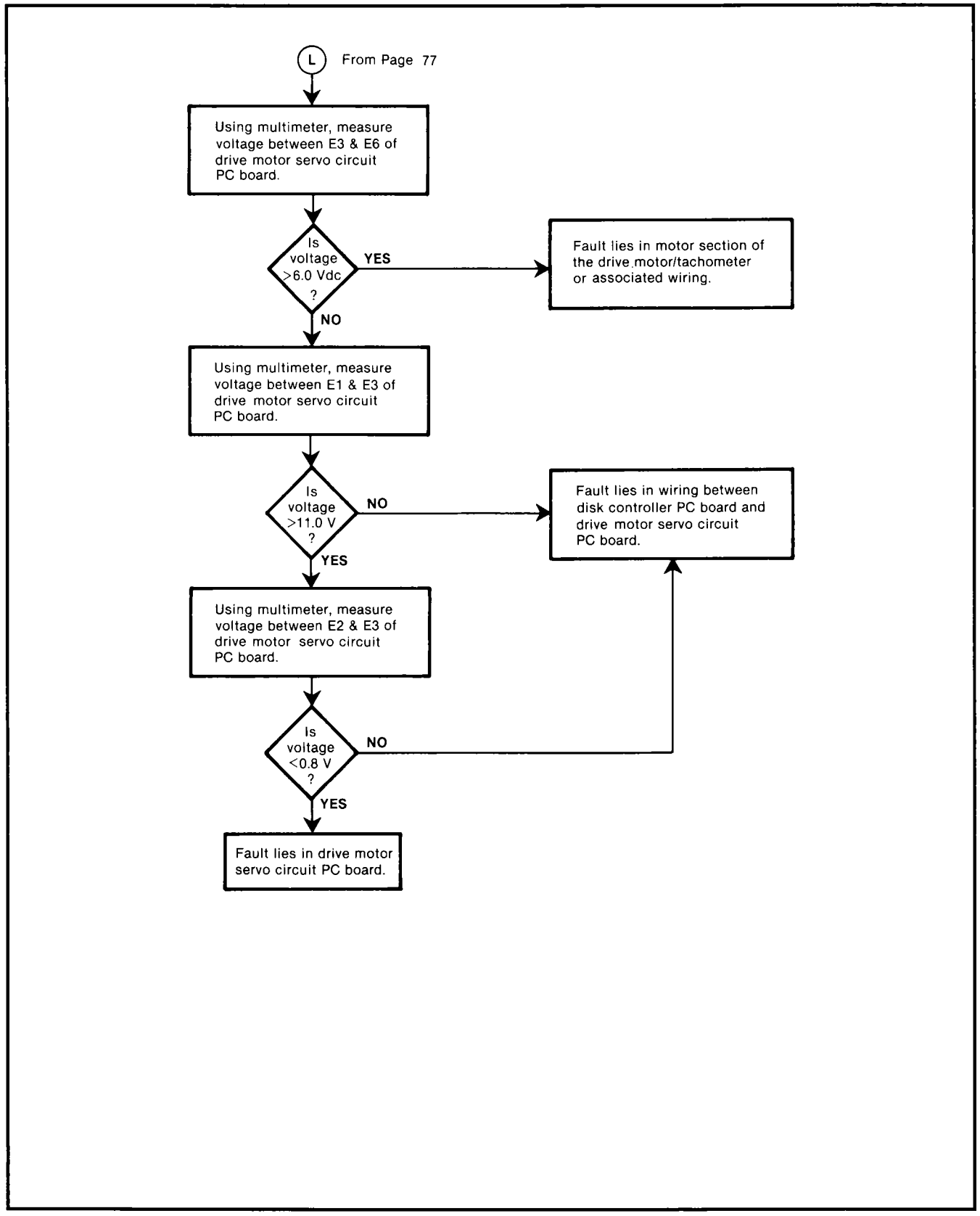
6.2.4 Faulty Drive Motor (cont.)



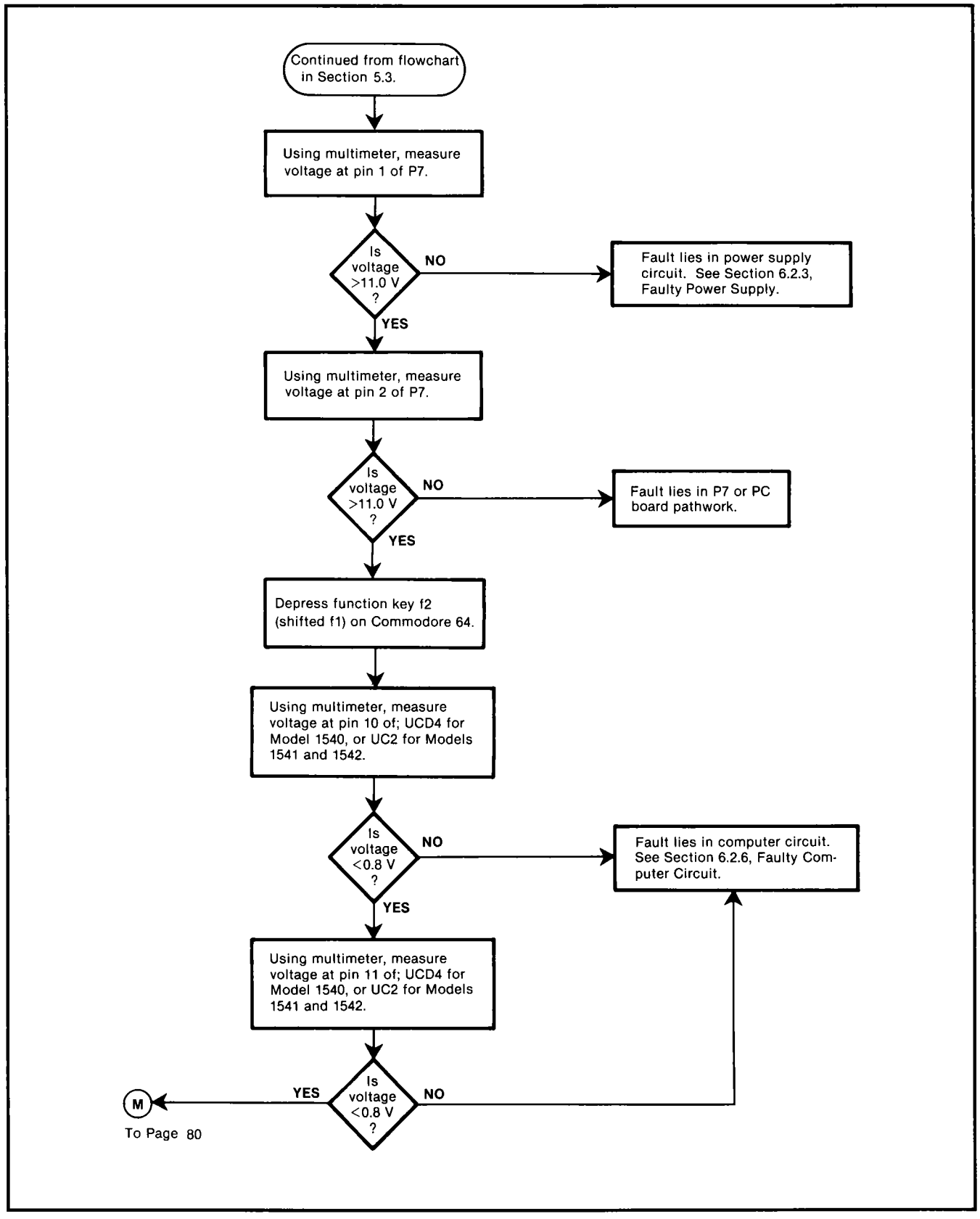
6.2.4 Faulty Drive Motor (cont.)



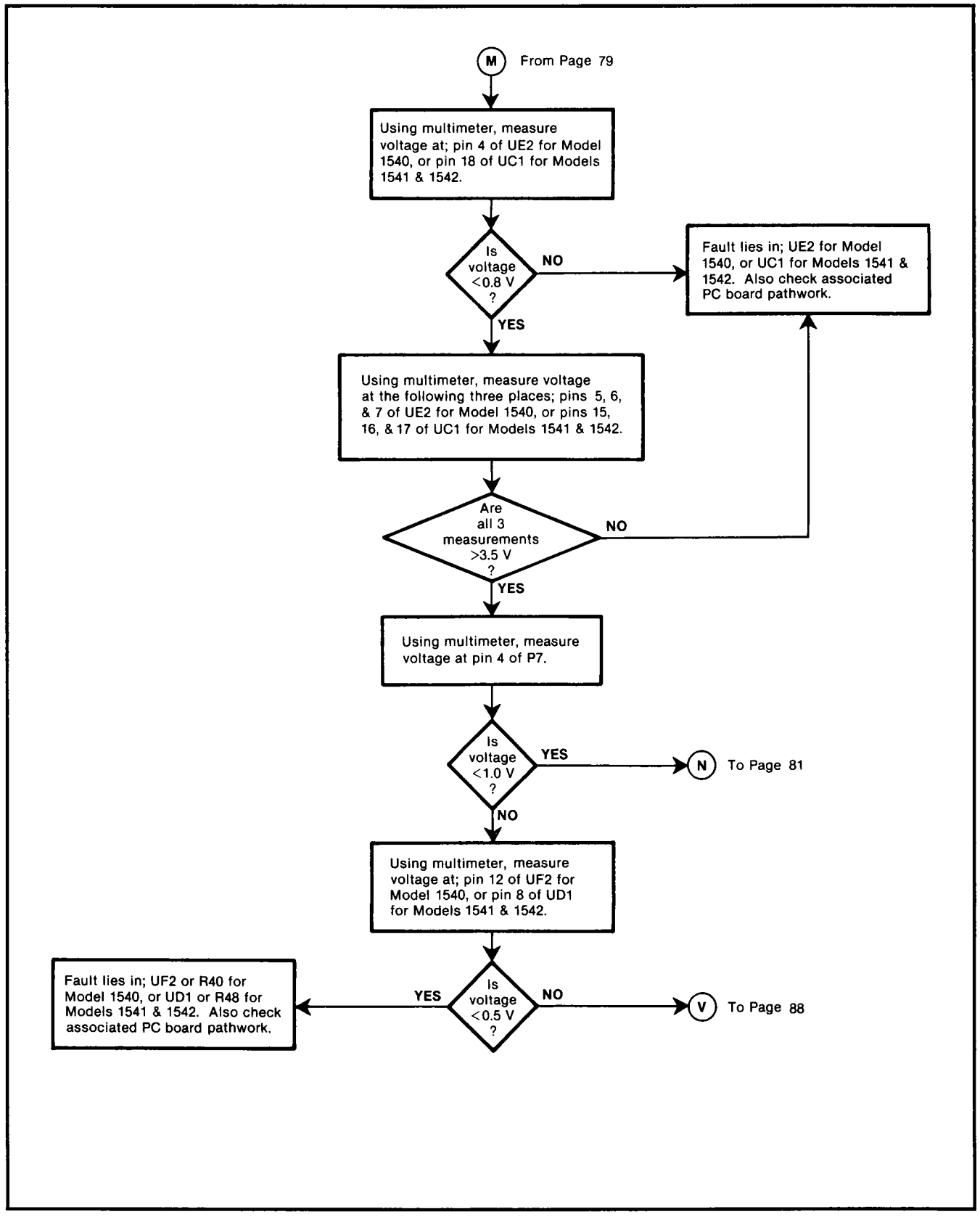
6.2.4 Faulty Drive Motor (cont.)



6.2.5 Faulty Stepping Motor



6.2.5 Faulty Stepping Motor (cont.)



6.2.5 Faulty Stepping Motor (cont.)

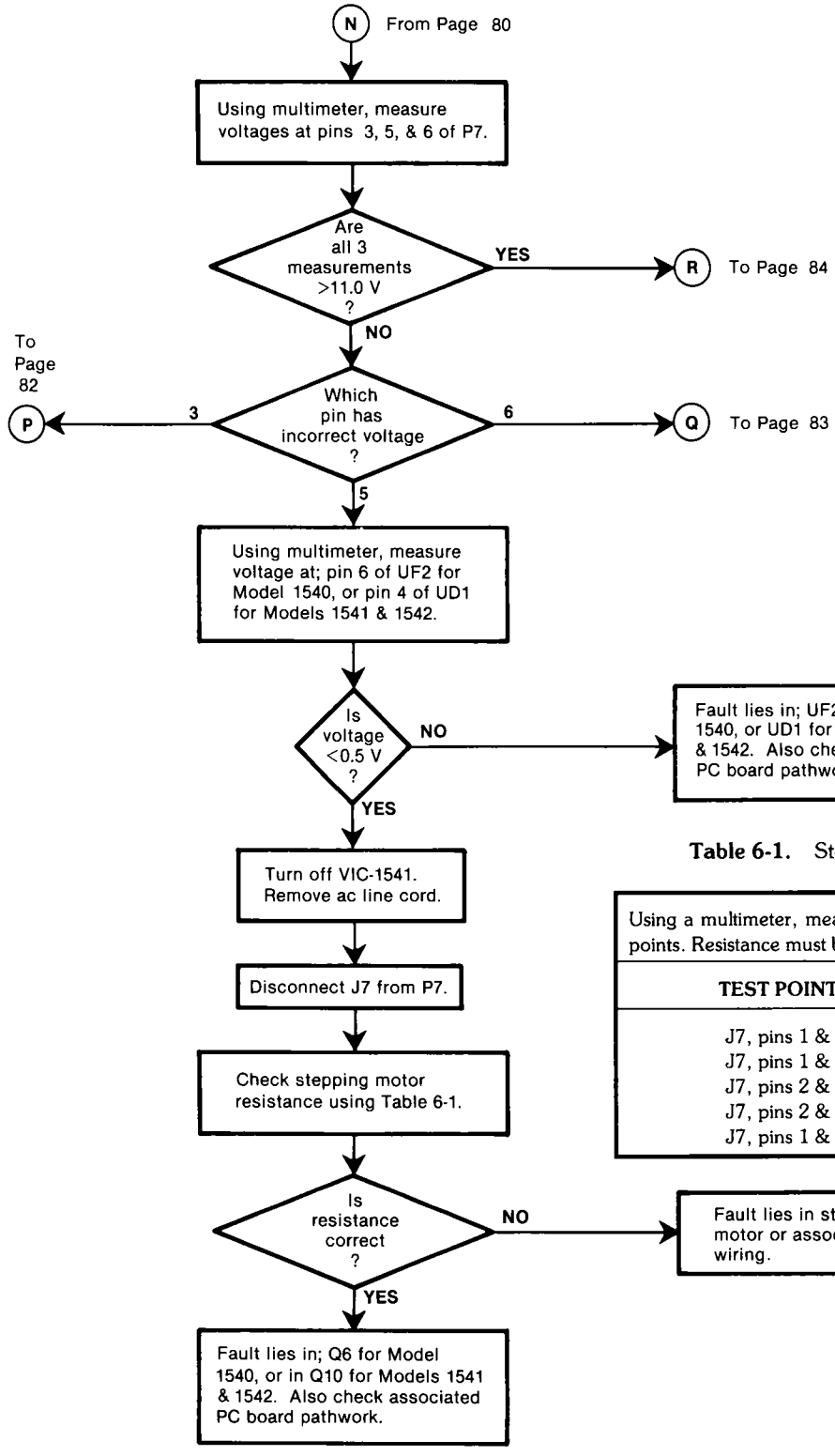
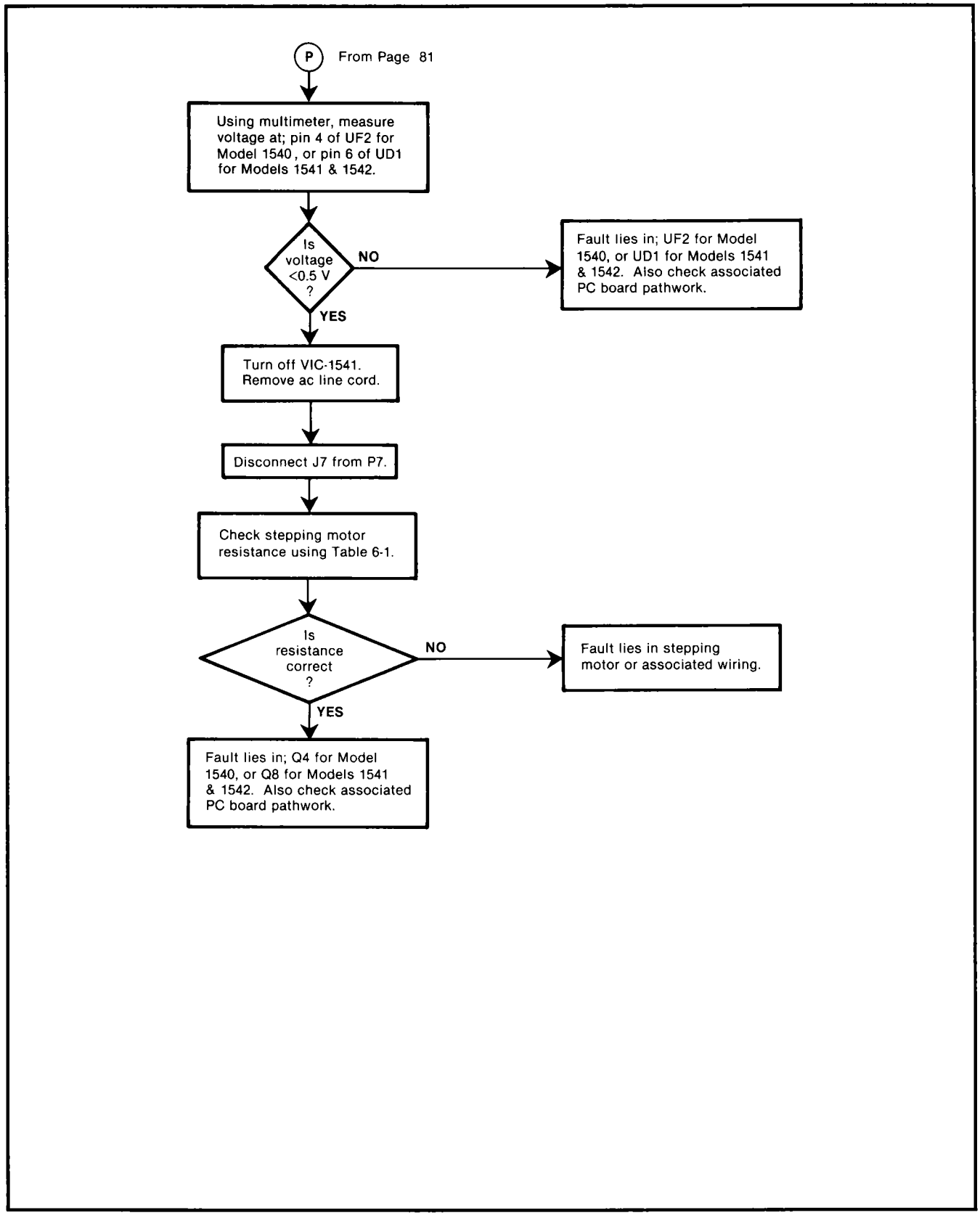


Table 6-1. Stepping Motor Resistance Check

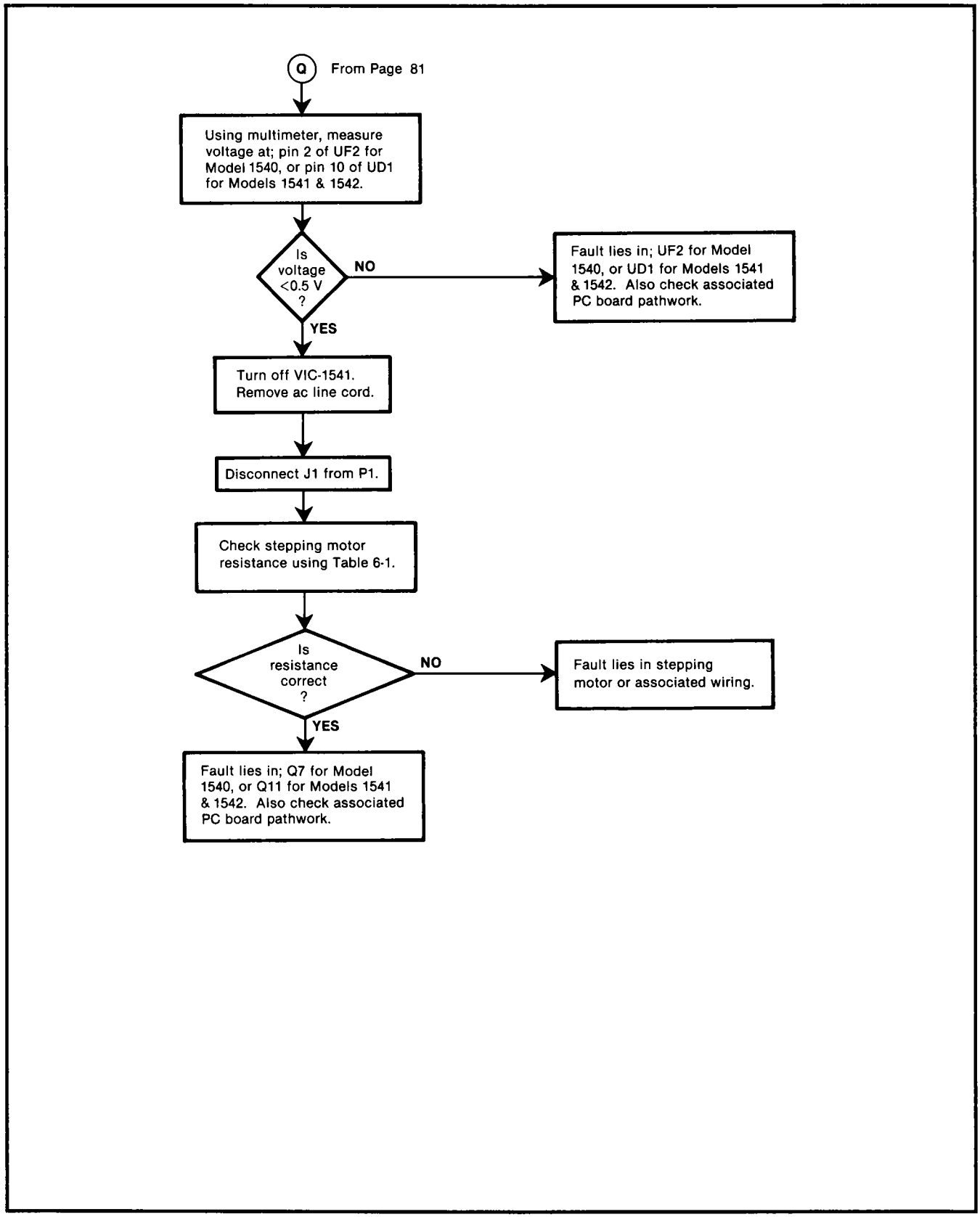
Using a multimeter, measure resistance between the following test points. Resistance must be within the limits listed.

TEST POINTS	RESISTANCE
J7, pins 1 & 3	30-36 ohms
J7, pins 1 & 4	30-36 ohms
J7, pins 2 & 5	30-36 ohms
J7, pins 2 & 6	30-36 ohms
J7, pins 1 & 2	infinity

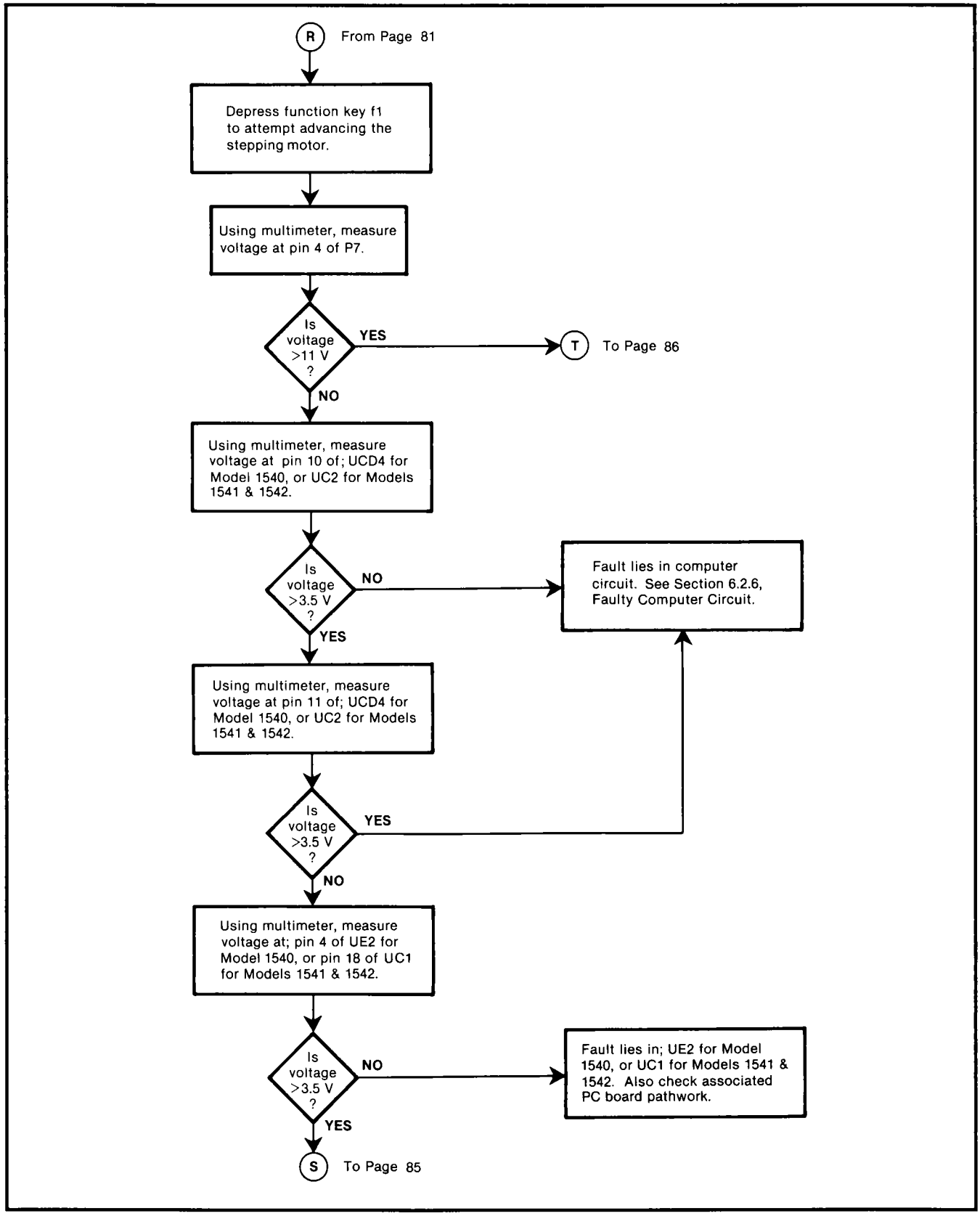
6.2.5 Faulty Stepping Motor (cont.)



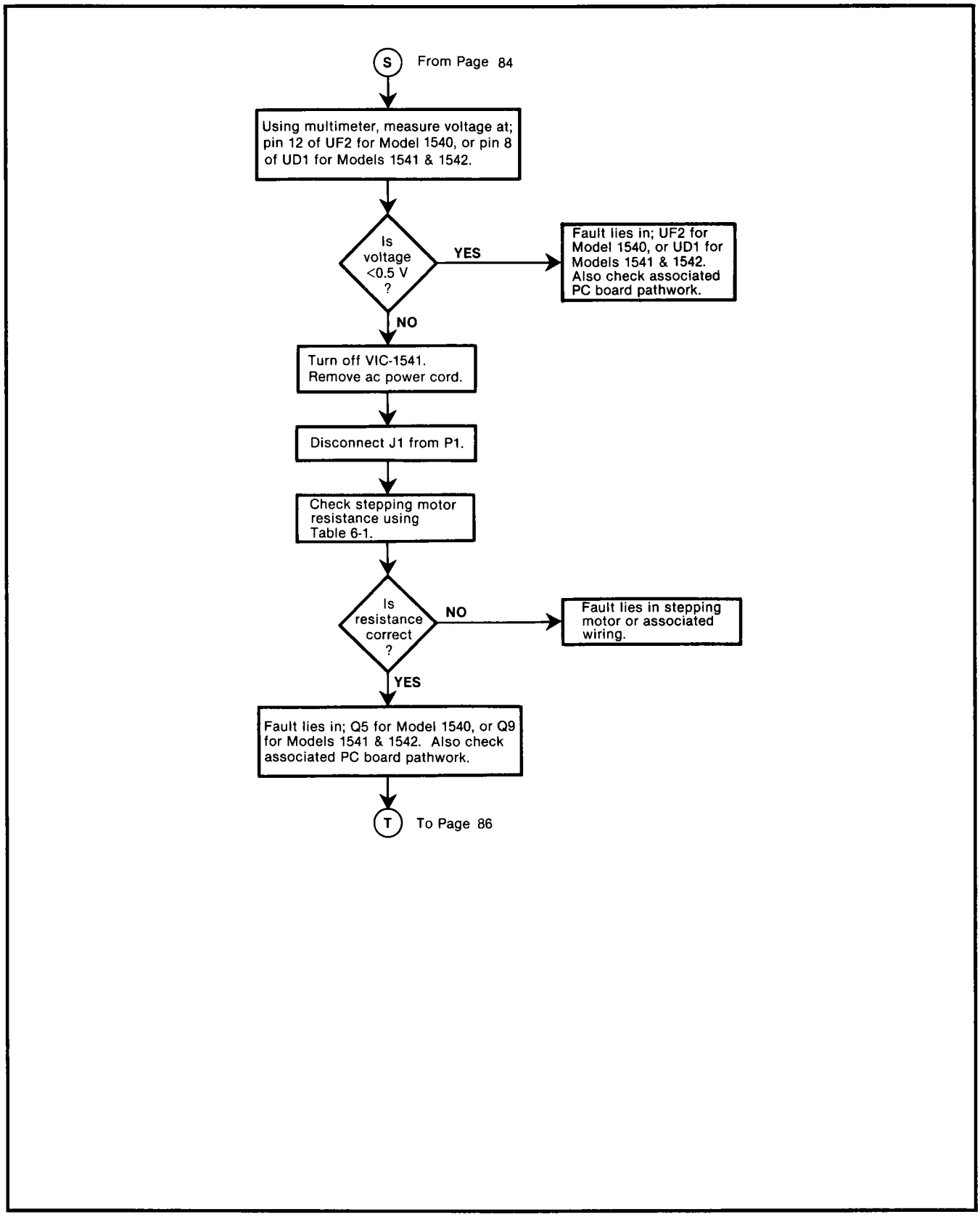
6.2.5 Faulty Stepping Motor (cont.)



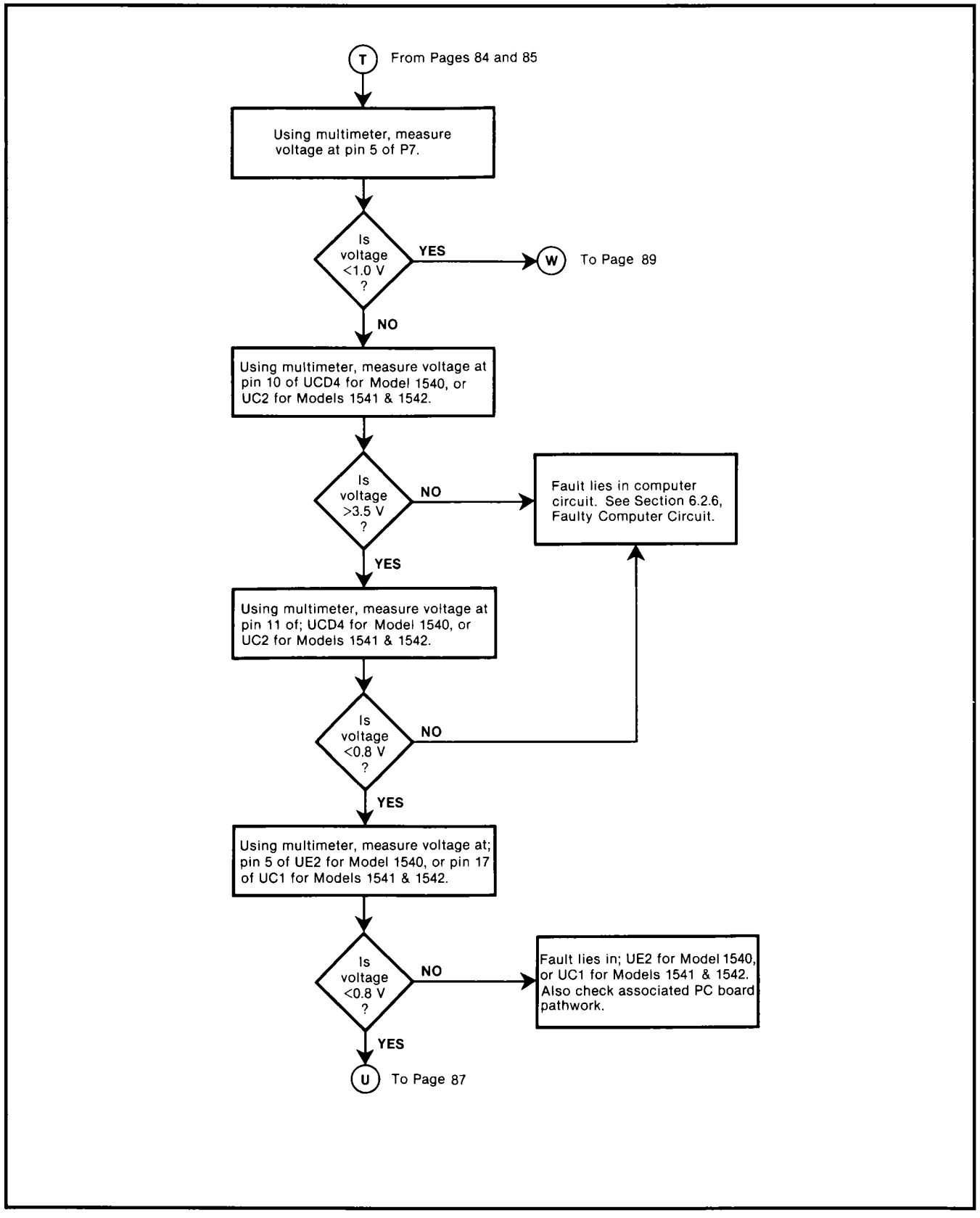
6.2.5 Faulty Stepping Motor (cont.)



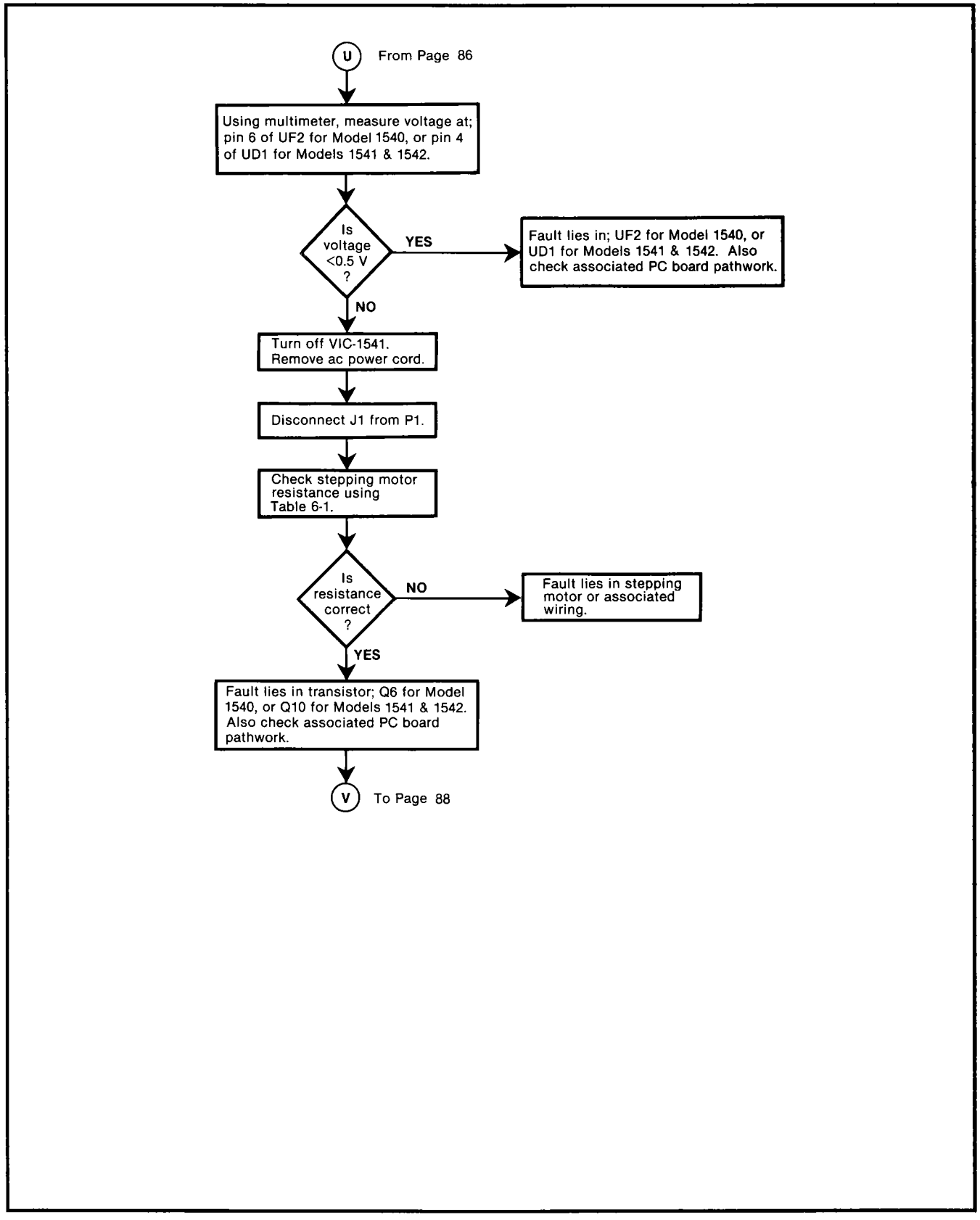
6.2.5 Faulty Stepping Motor (cont.)



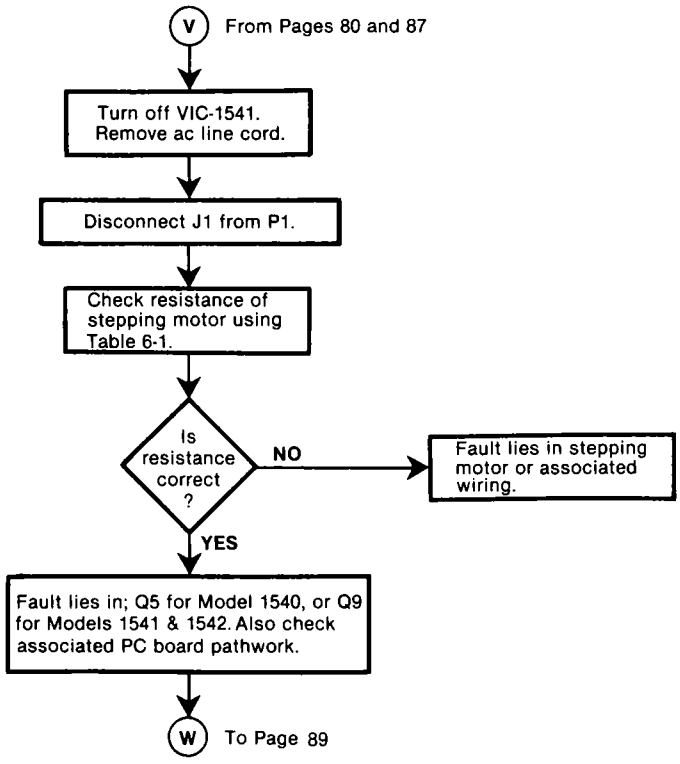
6.2.5 Faulty Stepping Motor (cont.)



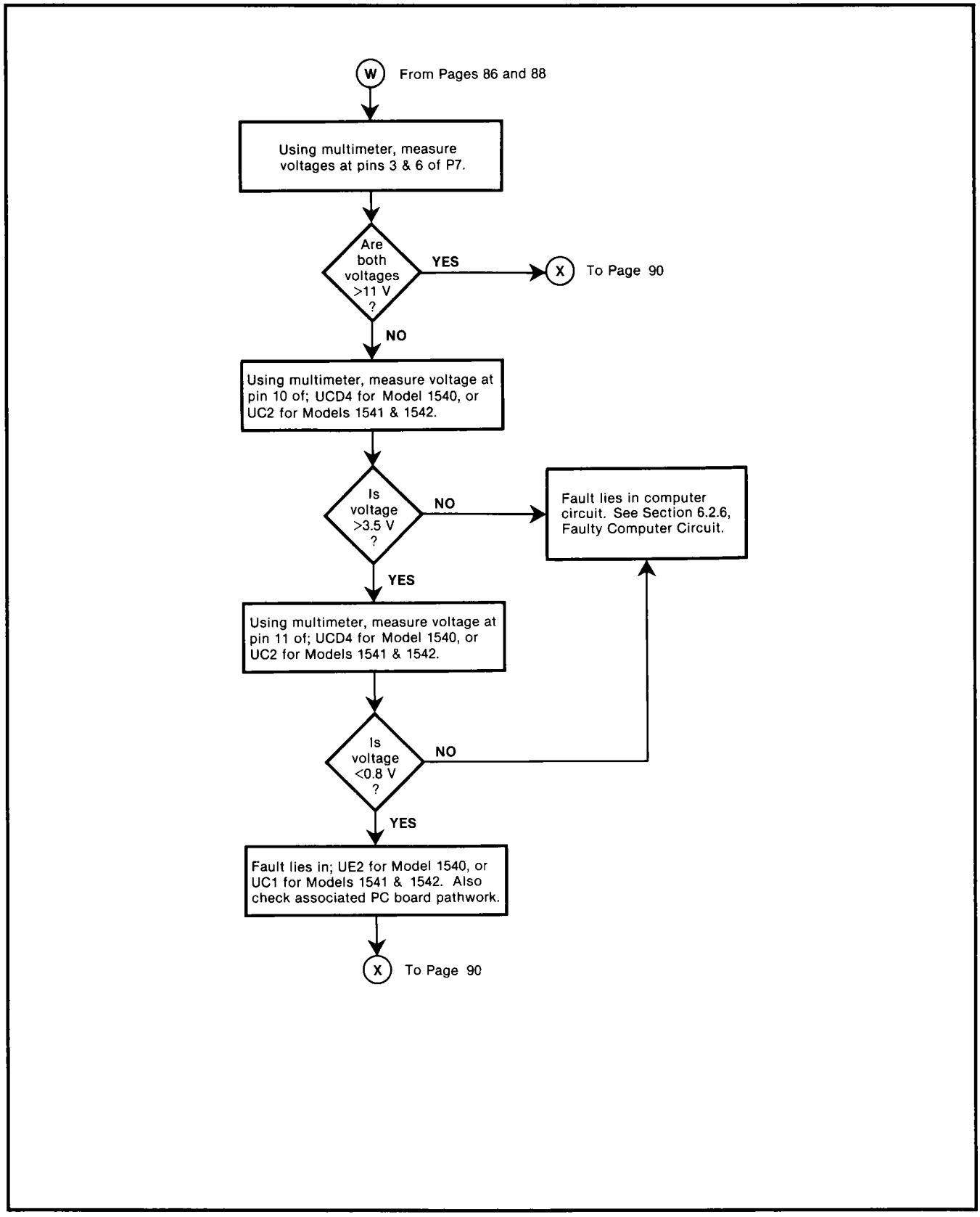
6.2.5 Faulty Stepping Motor (cont.)



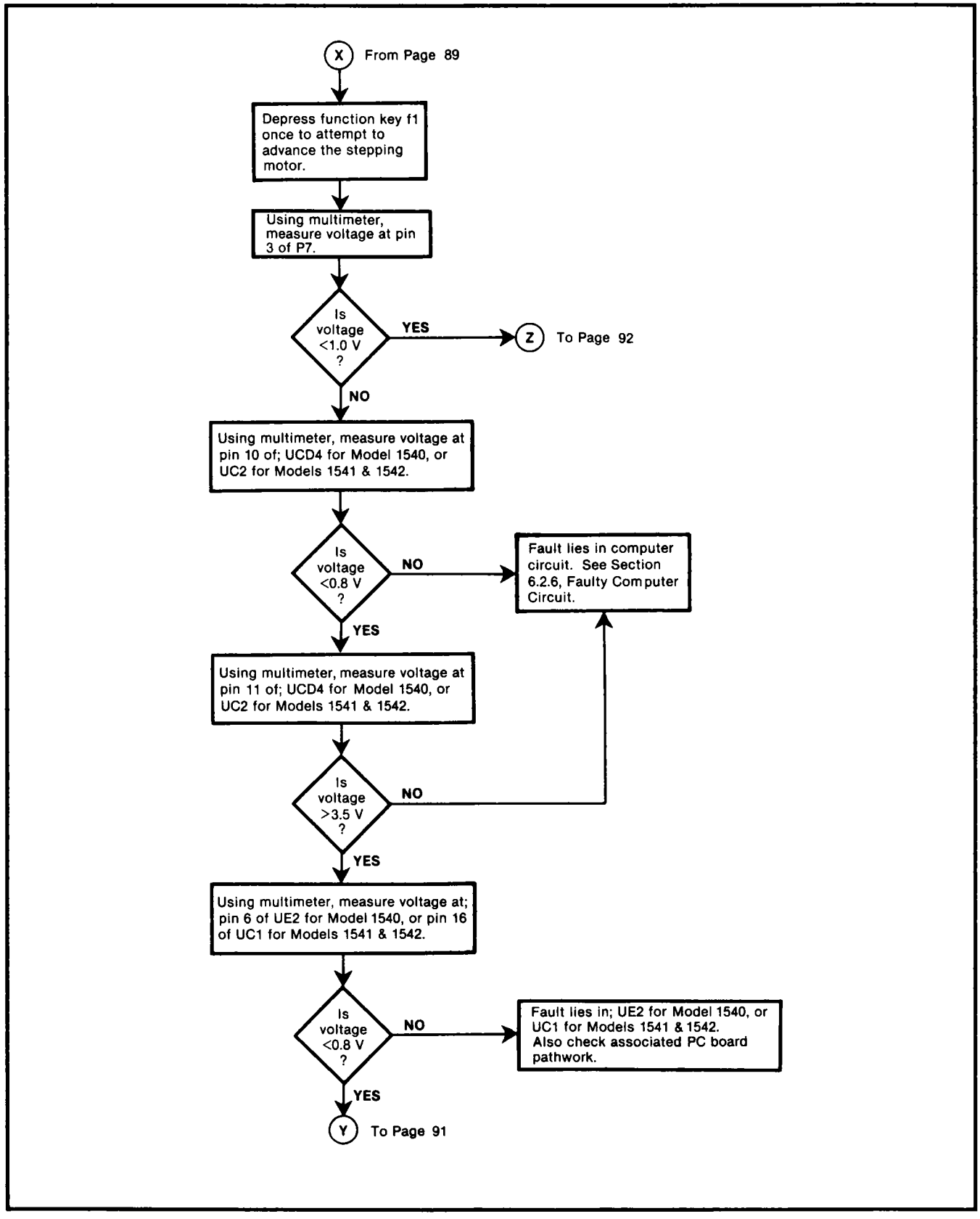
6.2.5 Faulty Stepping Motor (cont.)



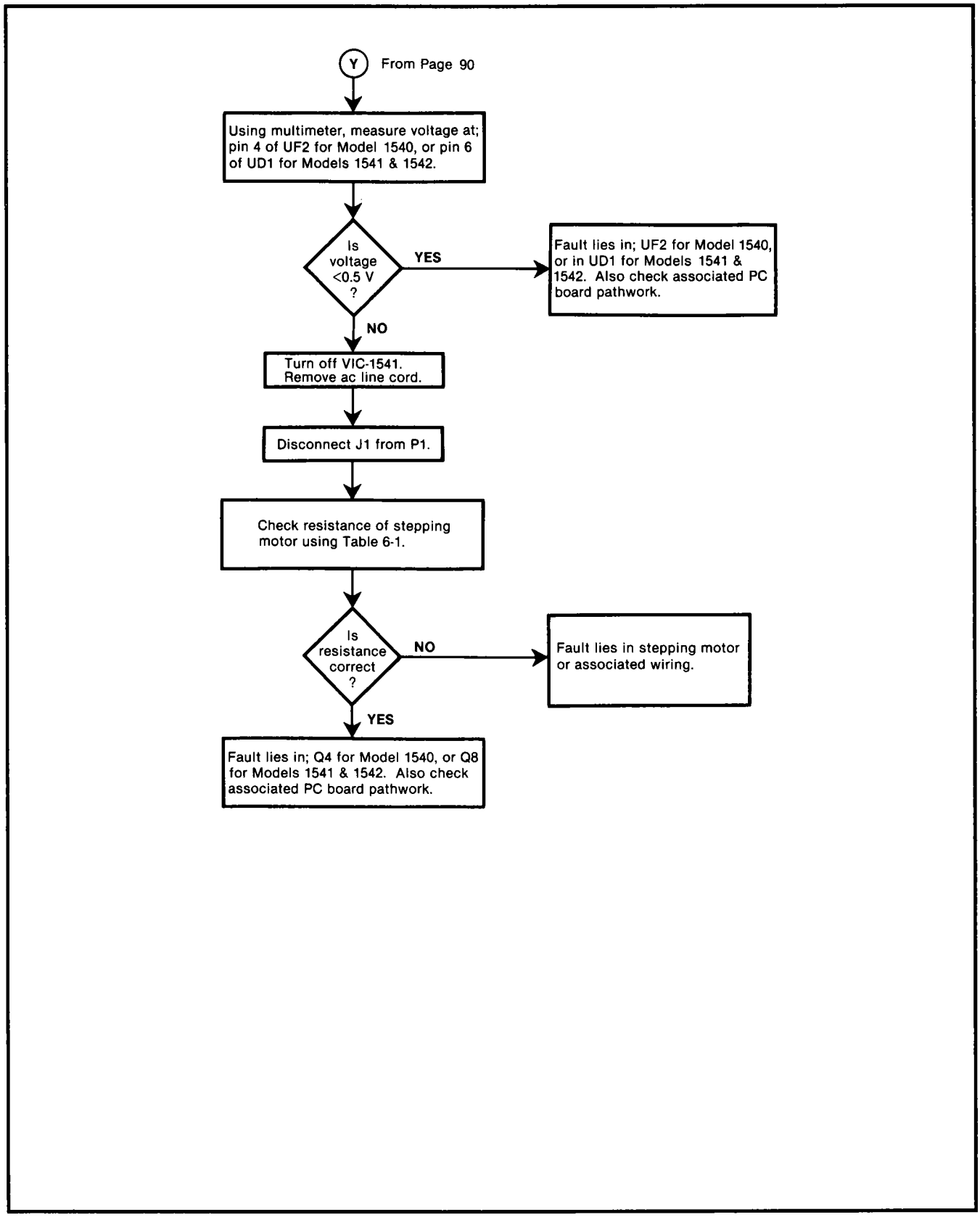
6.2.5 Faulty Stepping Motor (cont.)



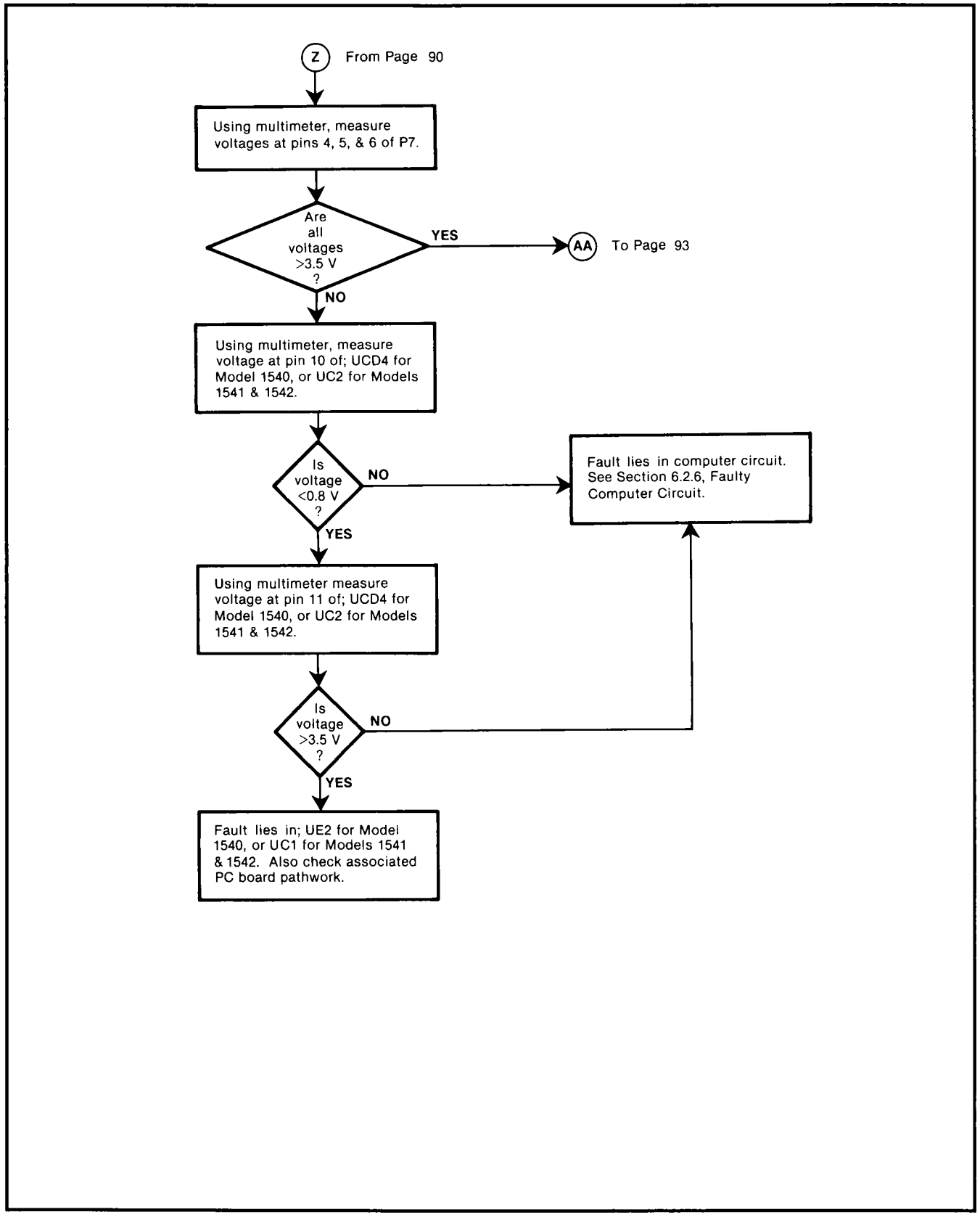
6.2.5 Faulty Stepping Motor (cont.)



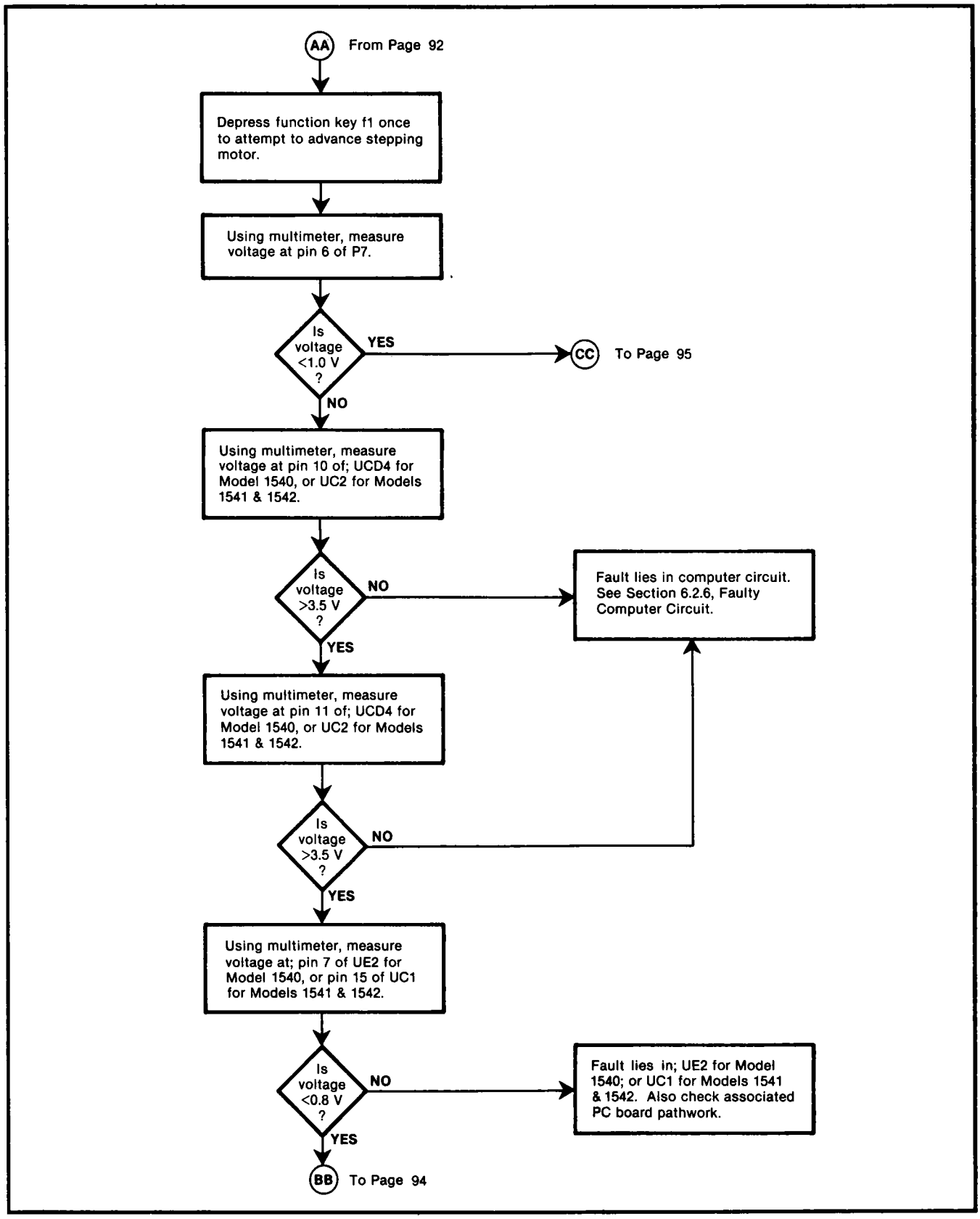
6.2.5 Faulty Stepping Motor (cont.)



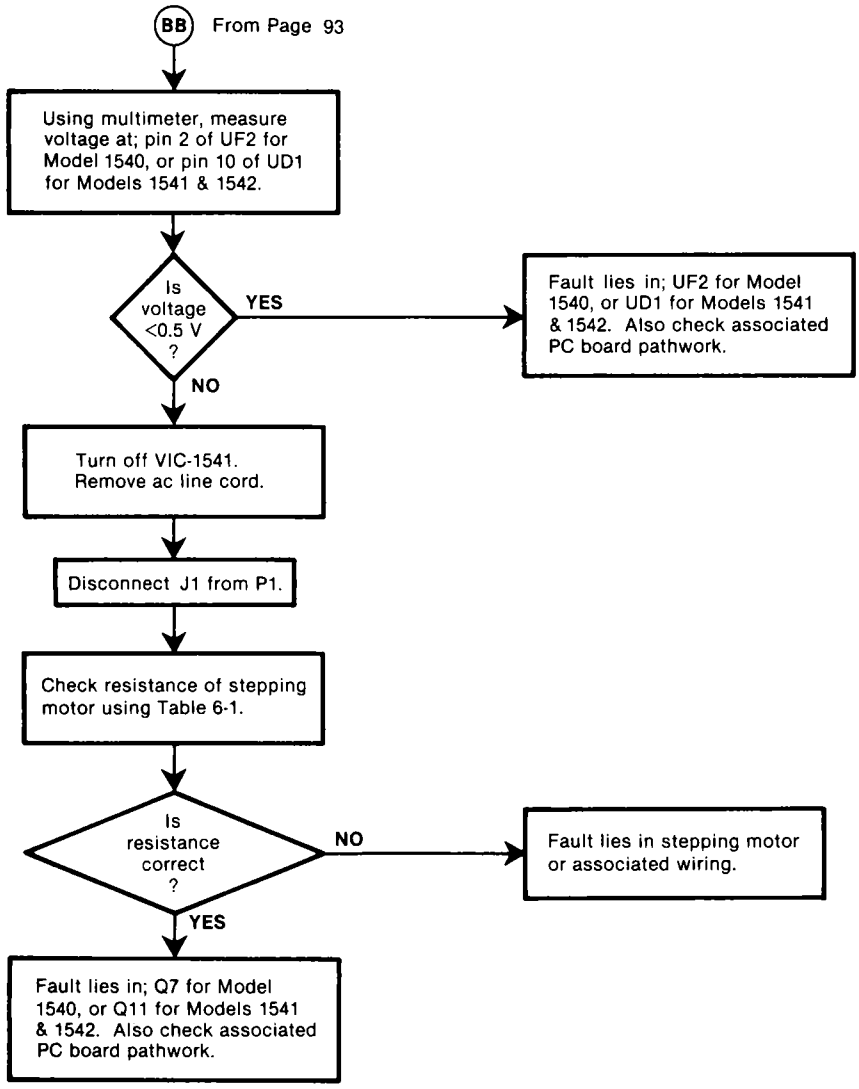
6.2.5 Faulty Stepping Motor (cont.)



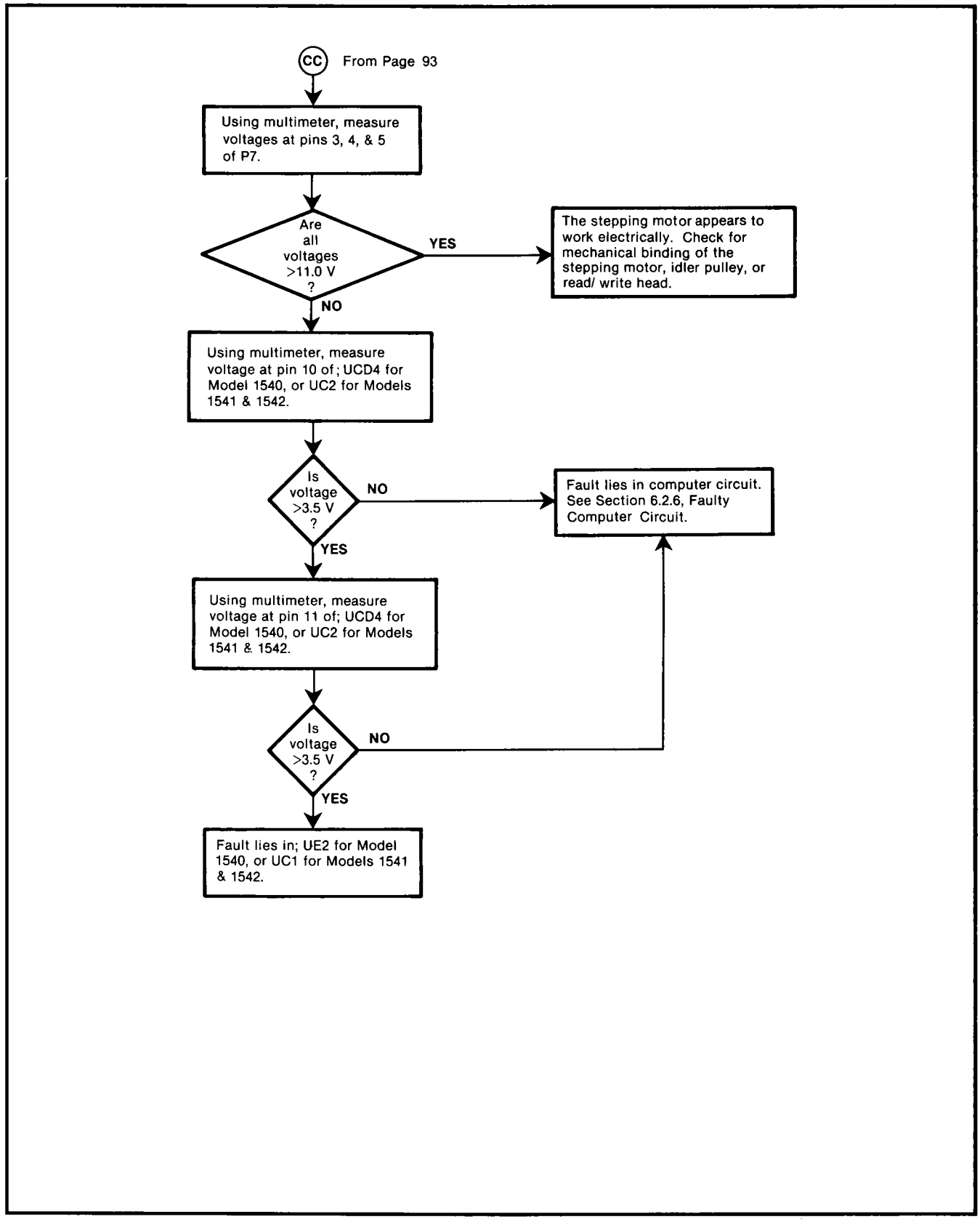
6.2.5 Faulty Stepping Motor (cont.)



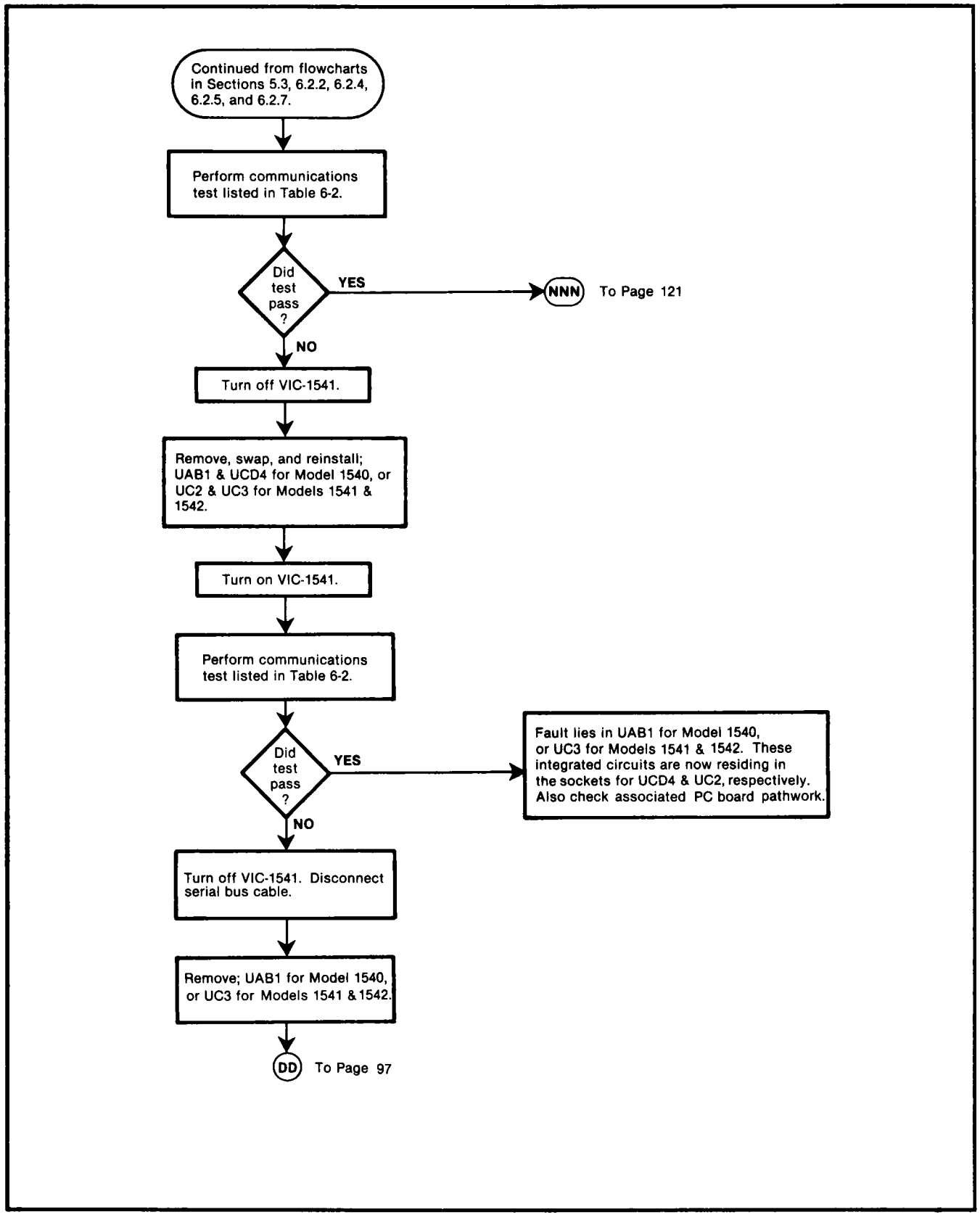
6.2.5 Faulty Stepping Motor (cont.)



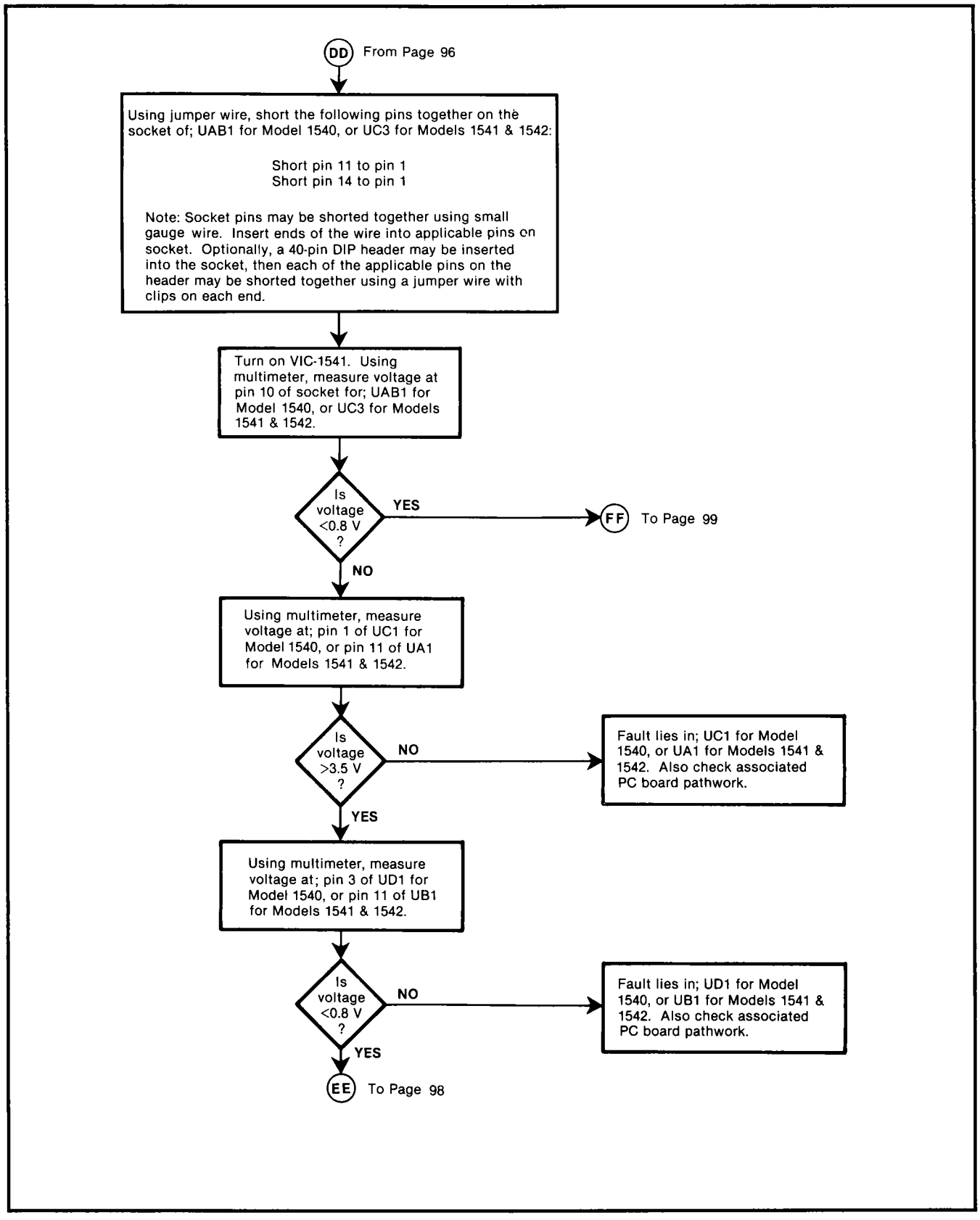
6.2.5 Faulty Stepping Motor (cont.)



6.2.6 Faulty Computer Circuit



6.2.6 Faulty Computer Circuit (cont.)



6.2.6 Faulty Computer Circuit (cont.)

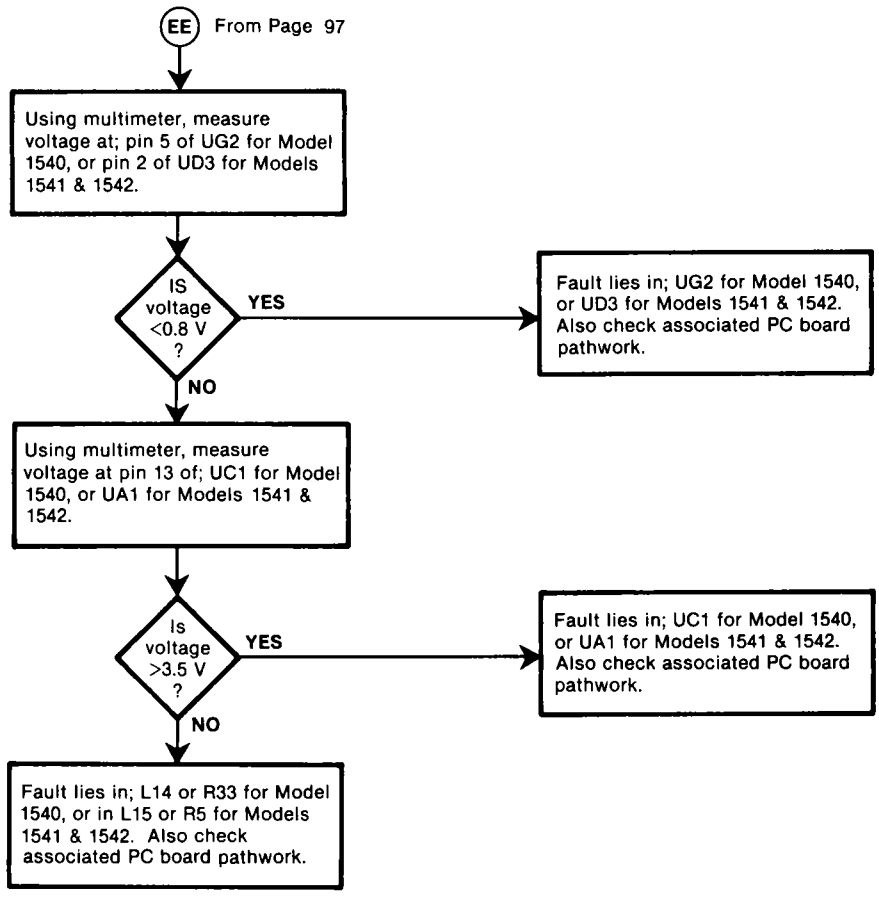


Table 6-2. Communications Test

TYPE THE FOLLOWING ONTO THE SCREEN:	
You Type This	`1 OPEN15,8,15:INPUT#15,A,A$,B,C:?A;A$;B;C <RETURN KEY>` `RUN <RETURN KEY>`
Correct Results, Test Passes	`00OK00` `READY.`
	Note: If computer responds with the following:

Test Fails	`DEVICE NOT PRESENT ERROR IN LINE 1`
	`READY.`
	
	Check for proper device number. If the VIC-1541 is not device No. 8, then change the "8" in line 1 to 9, 10, or 11, as applicable. Then "RUN" the program again. If device numbers are correct, then the VIC-1541 computer circuits are at fault. If the device number is unknown, see Section 1.3.2, "Changing Device Numbers."

Test Fails	No response, cursor does not return.

6.2.6 Faulty Computer Circuit (cont.)

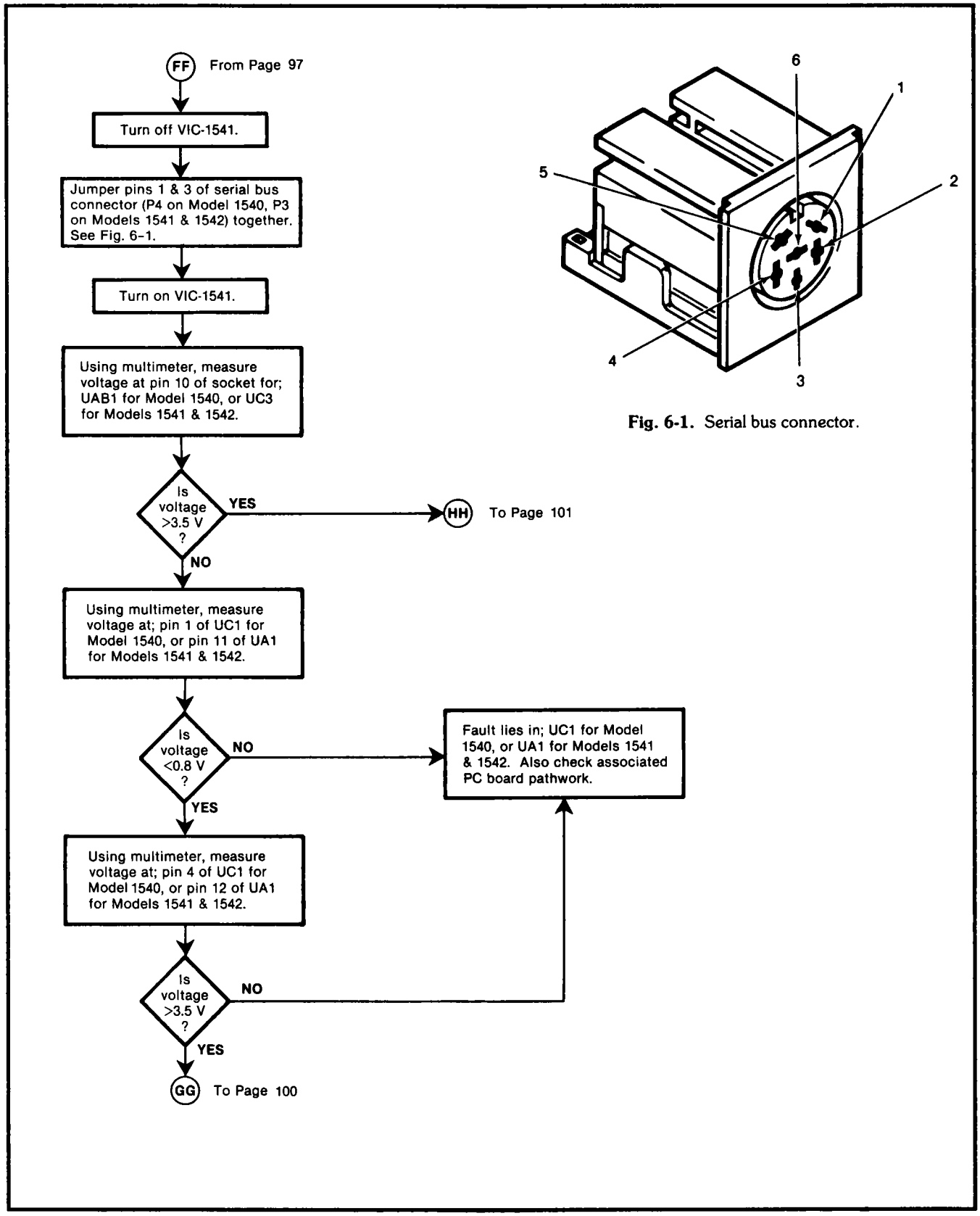
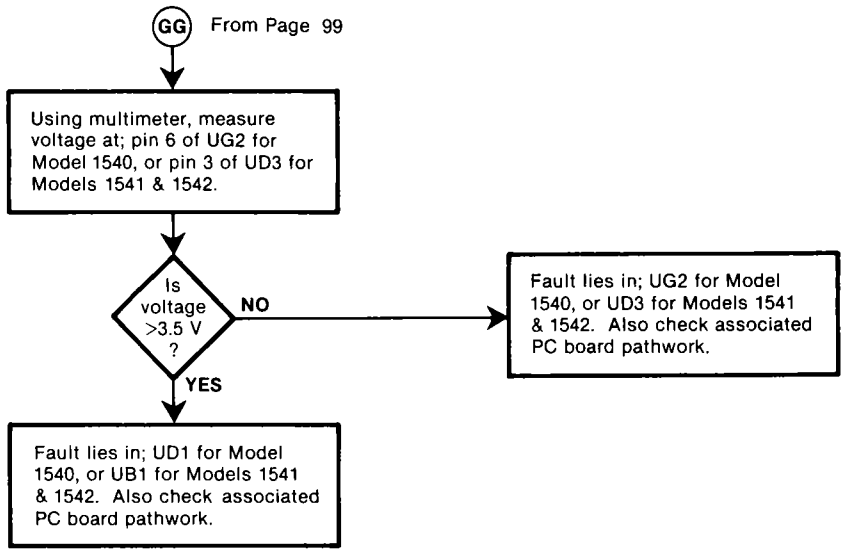
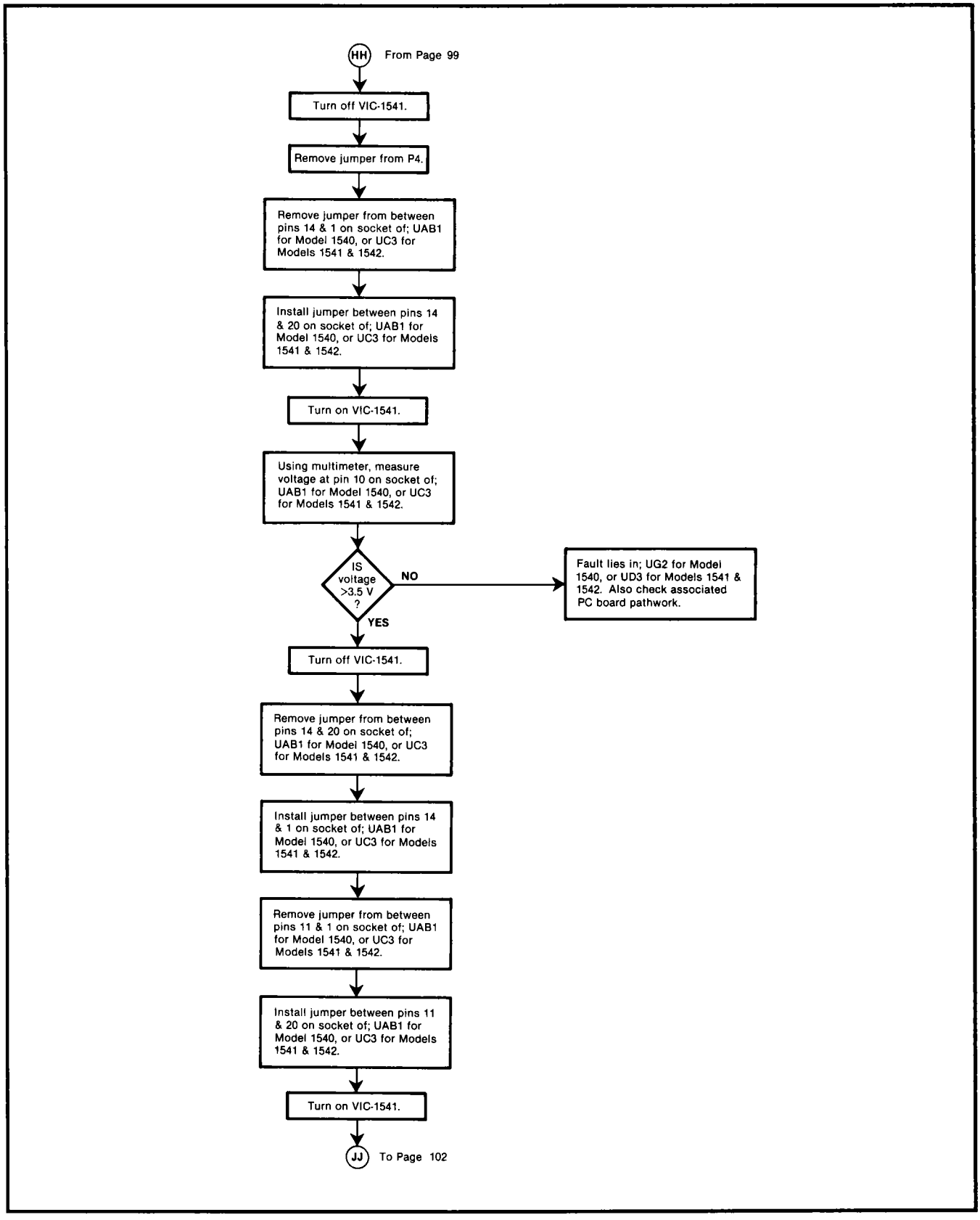


Fig. 6-1. Serial bus connector.

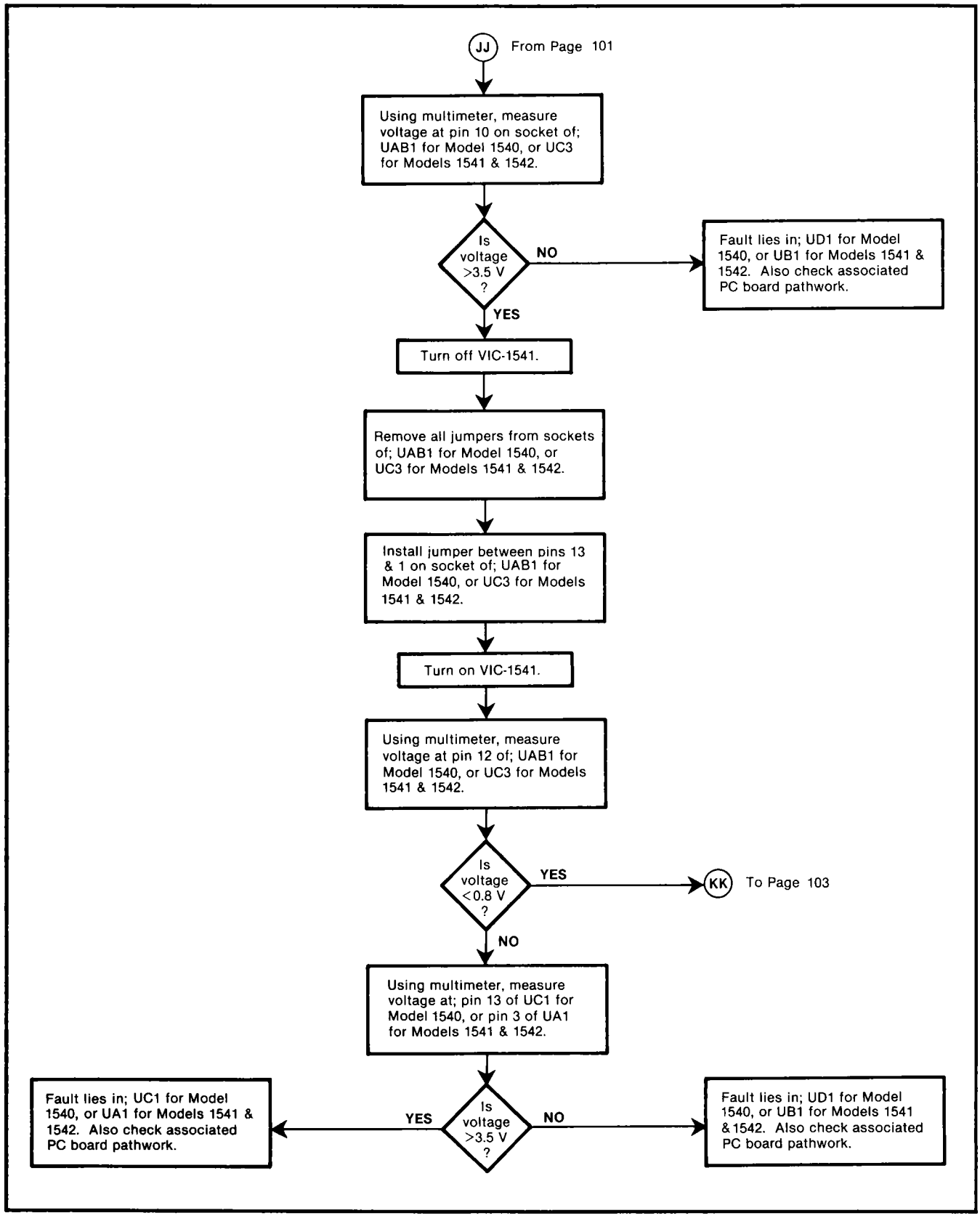
6.2.6 Faulty Computer Circuit (cont.)



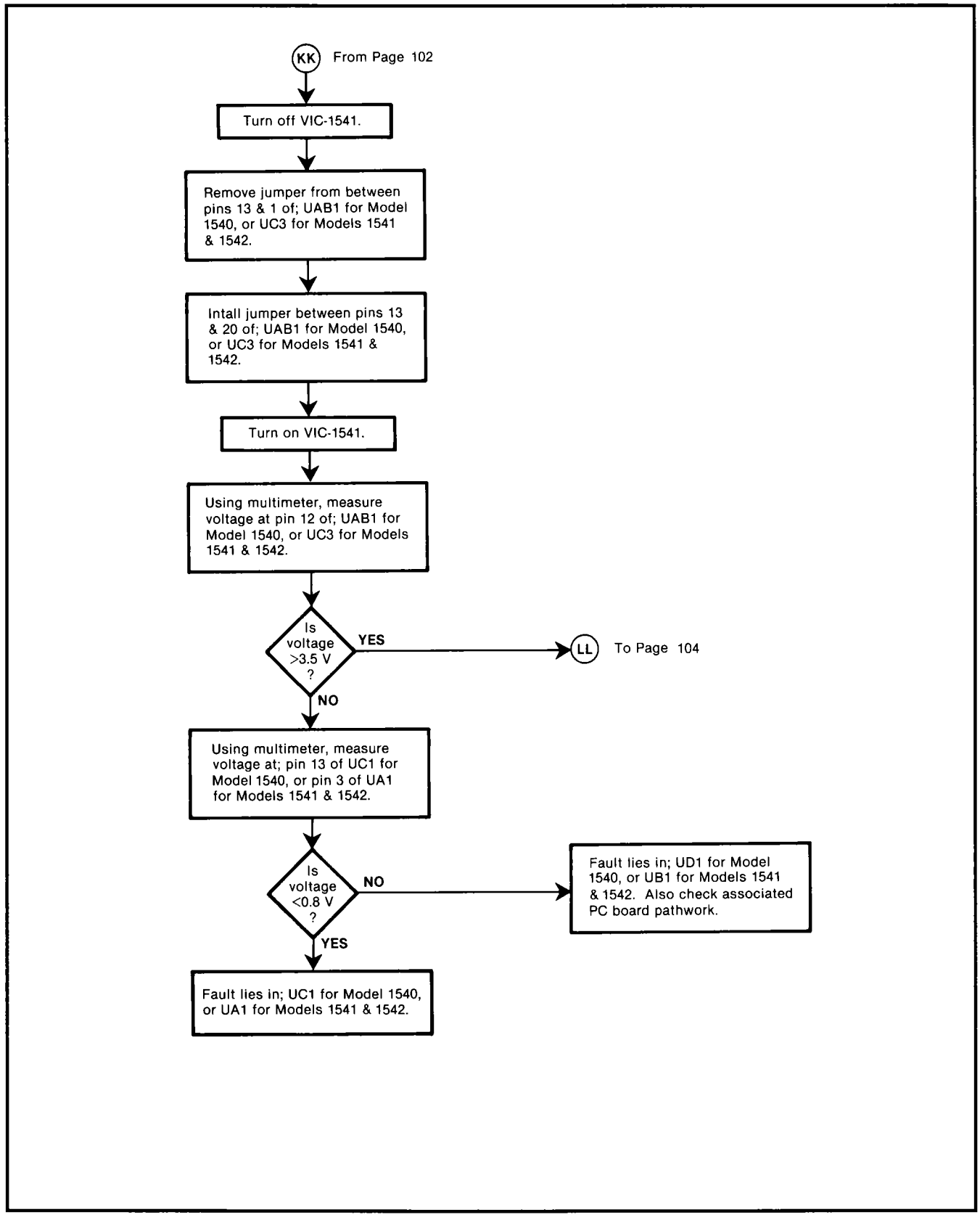
6.2.6 Faulty Computer Circuit (cont.)



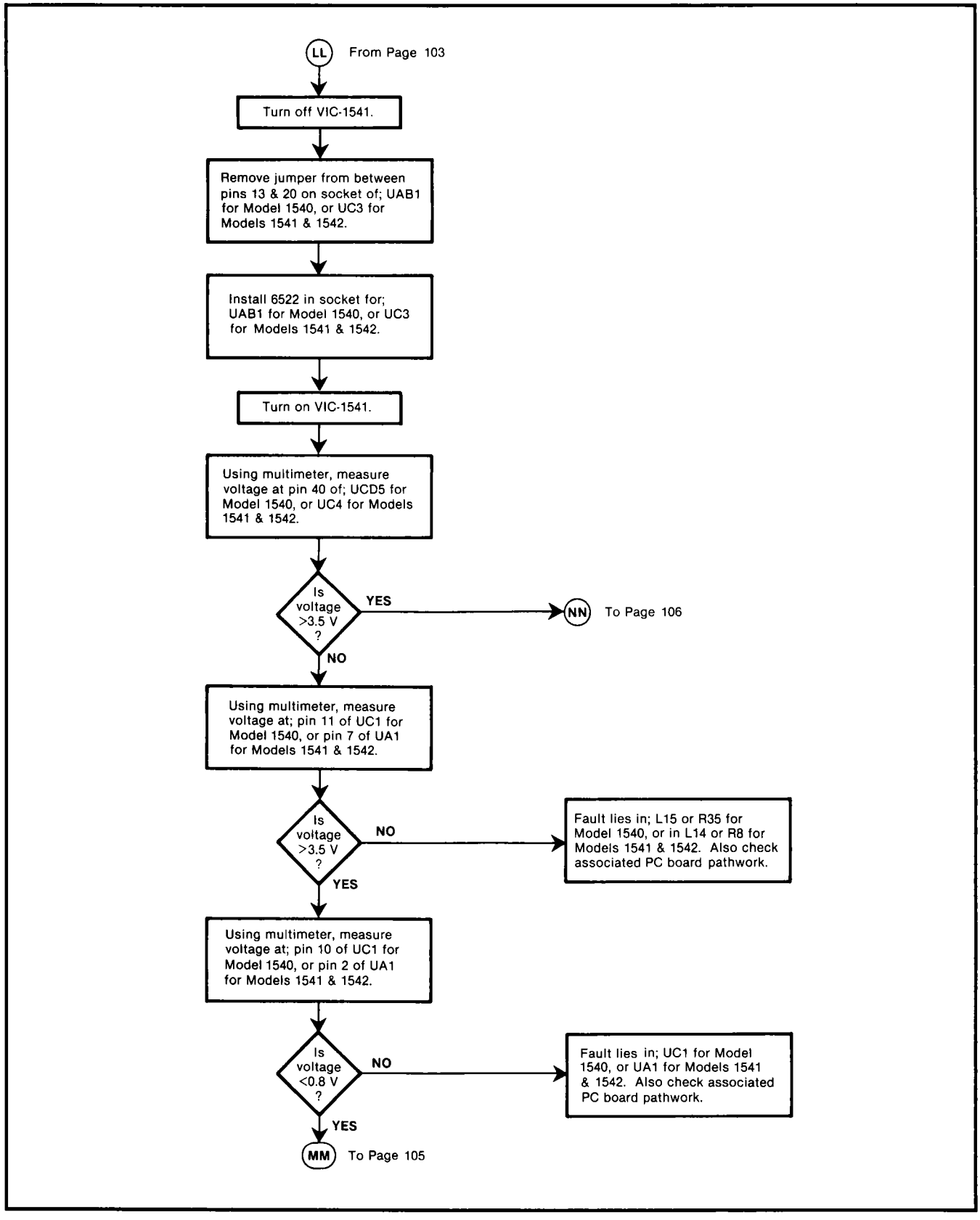
6.2.6 Faulty Computer Circuit (cont.)



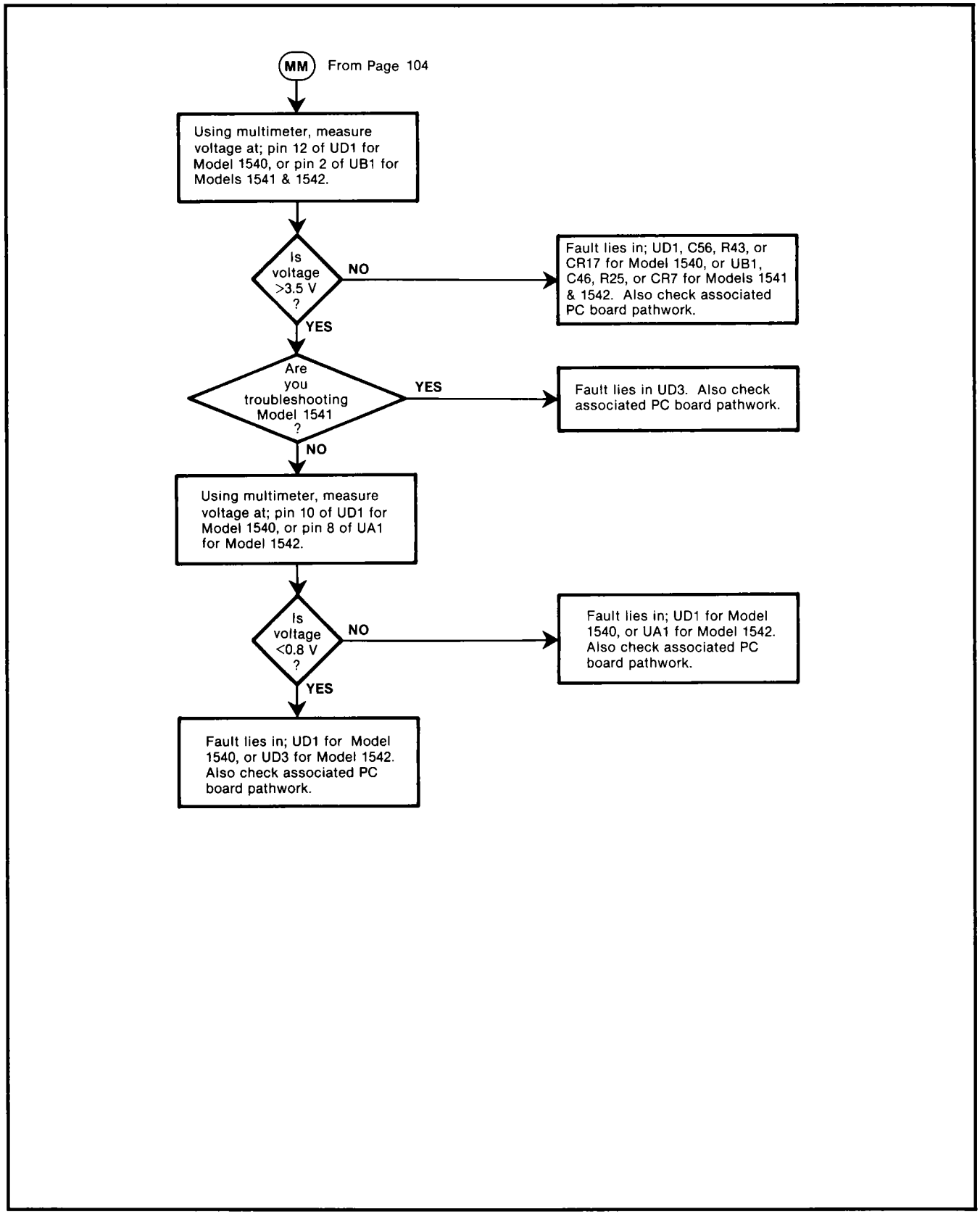
6.2.6 Faulty Computer Circuit (cont.)



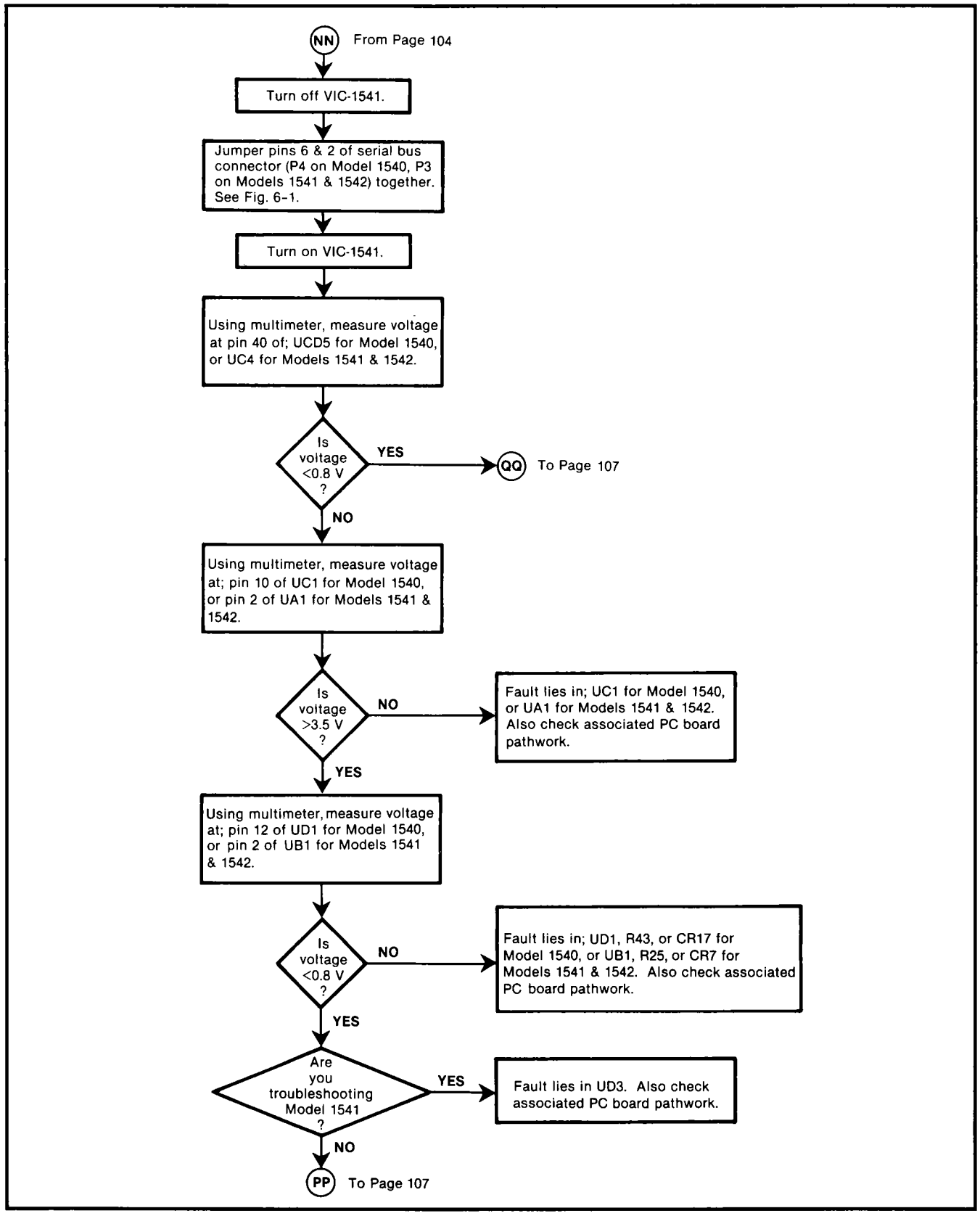
6.2.6 Faulty Computer Circuit (cont.)



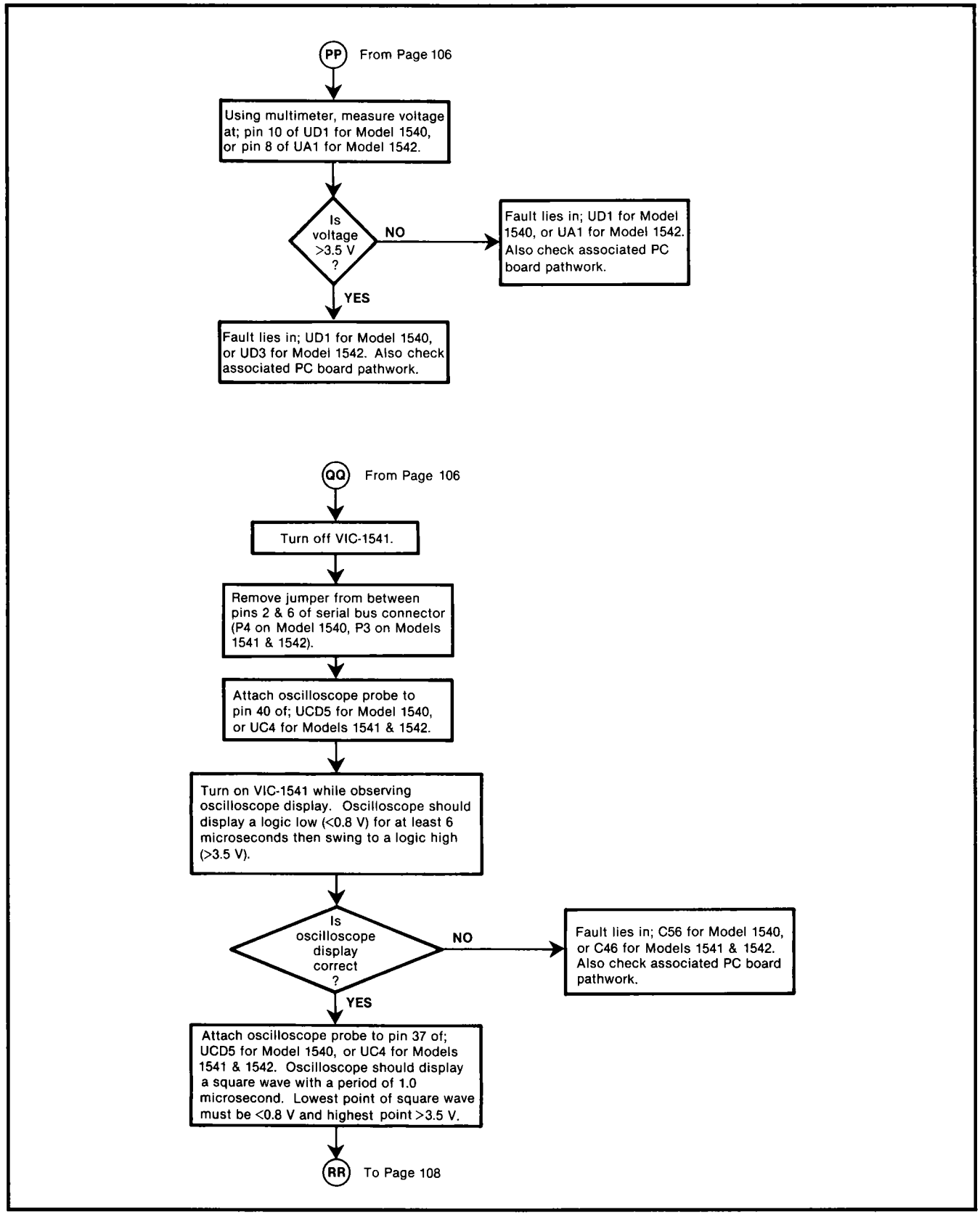
6.2.6 Faulty Computer Circuit (cont.)



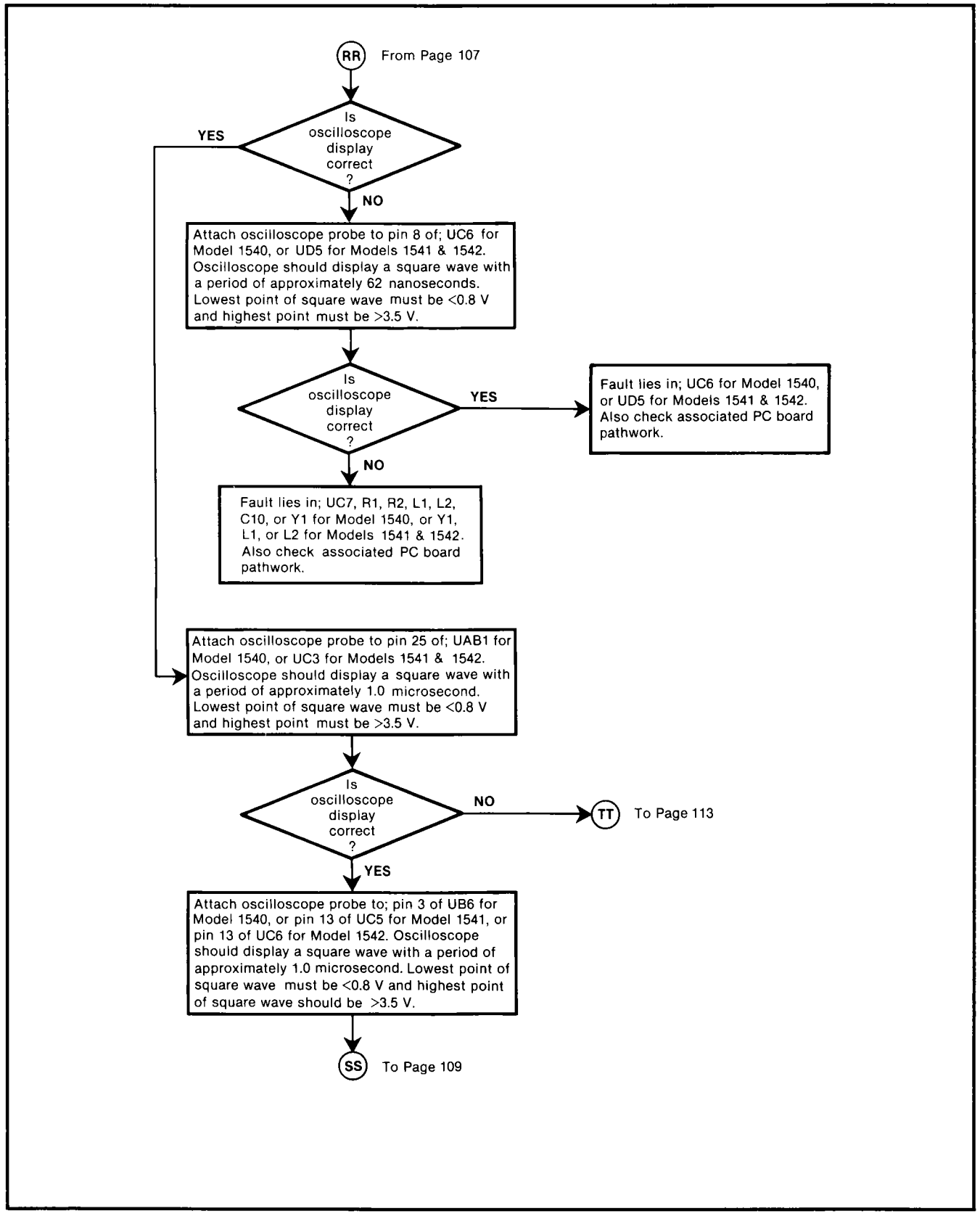
6.2.6 Faulty Computer Circuit (cont.)



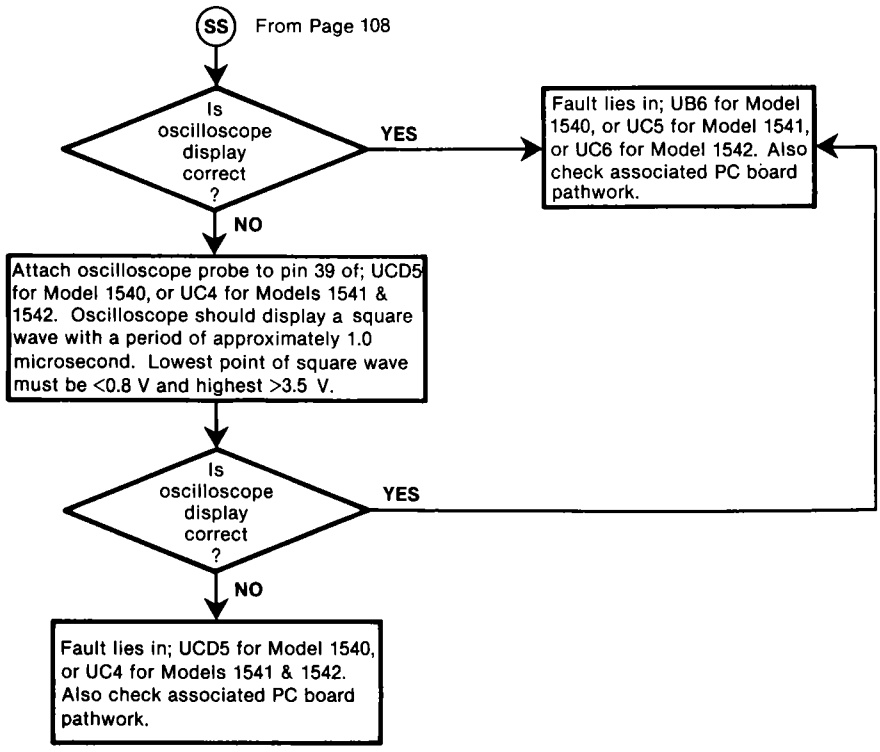
6.2.6 Faulty Computer Circuit (cont.)



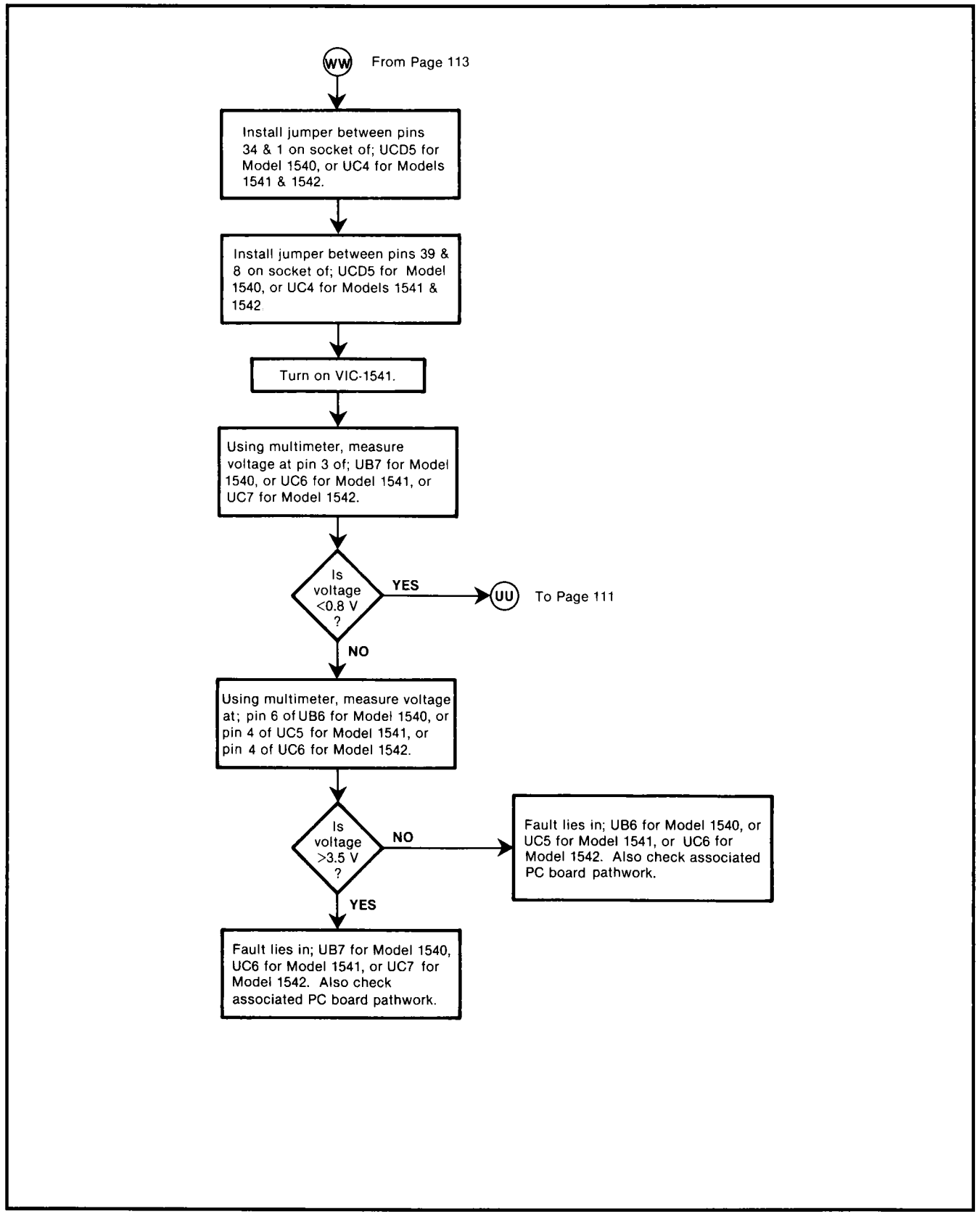
6.2.6 Faulty Computer Circuit (cont.)



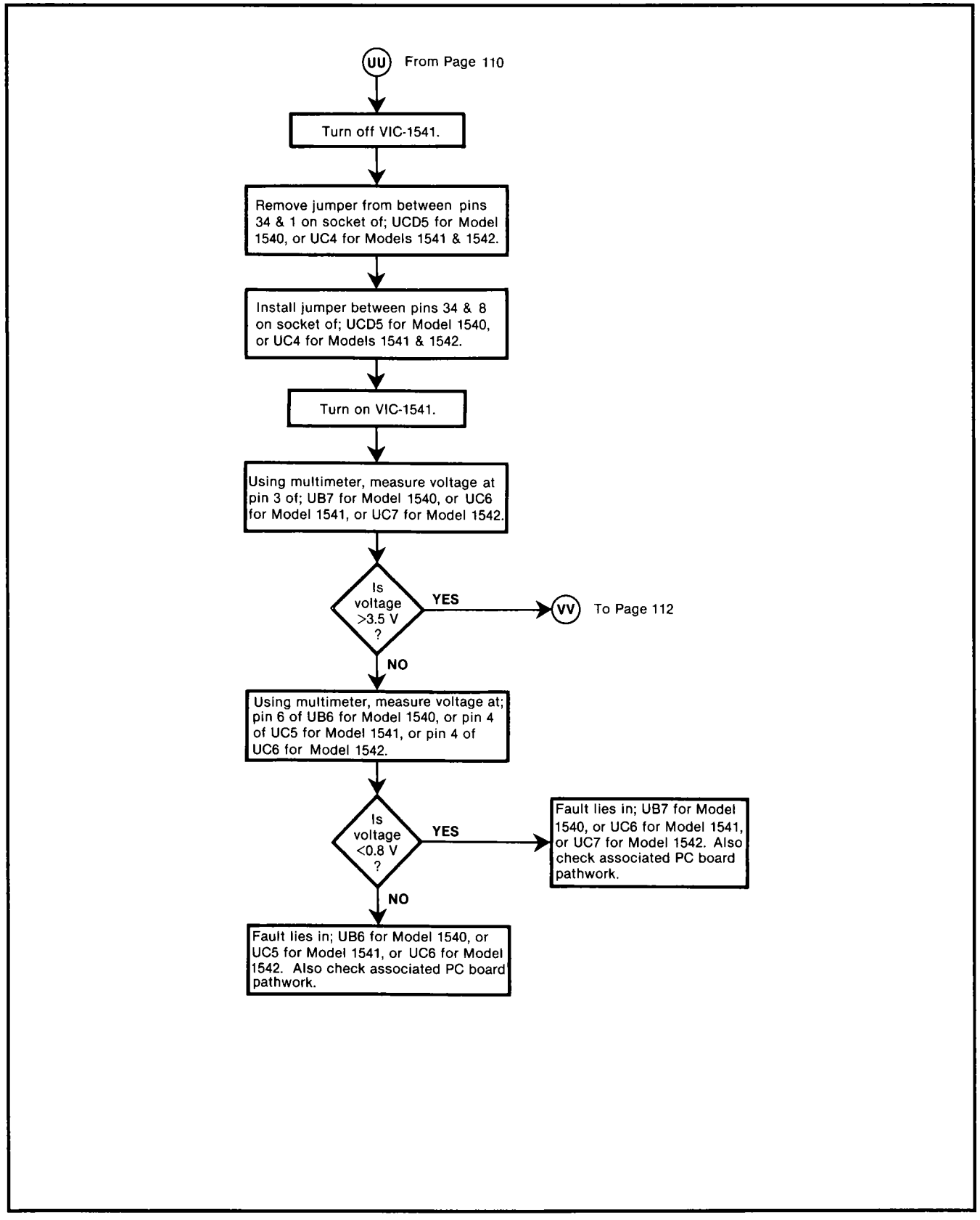
6.2.6 Faulty Computer Circuit (cont.)



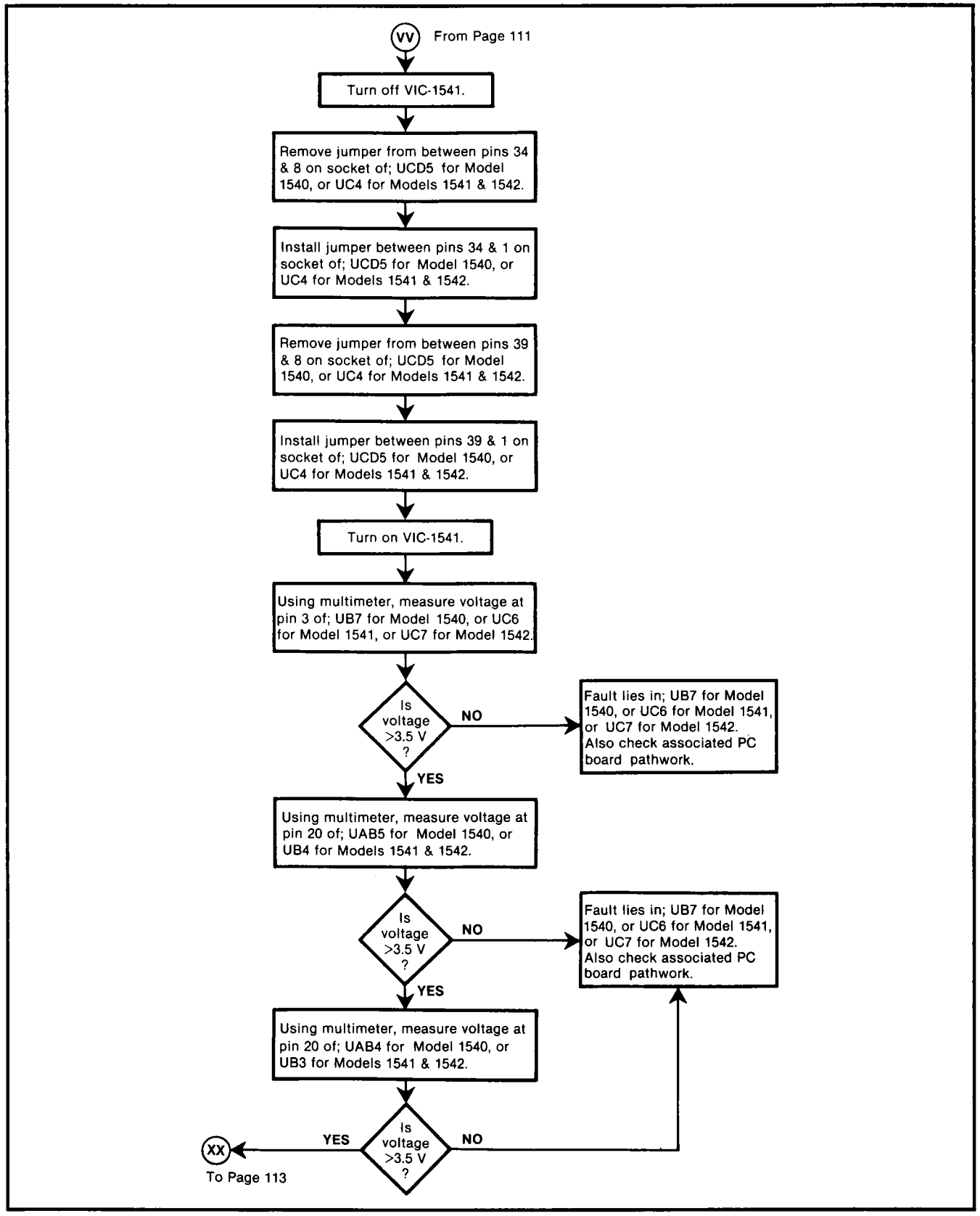
6.2.6 Faulty Computer Circuit (cont.)



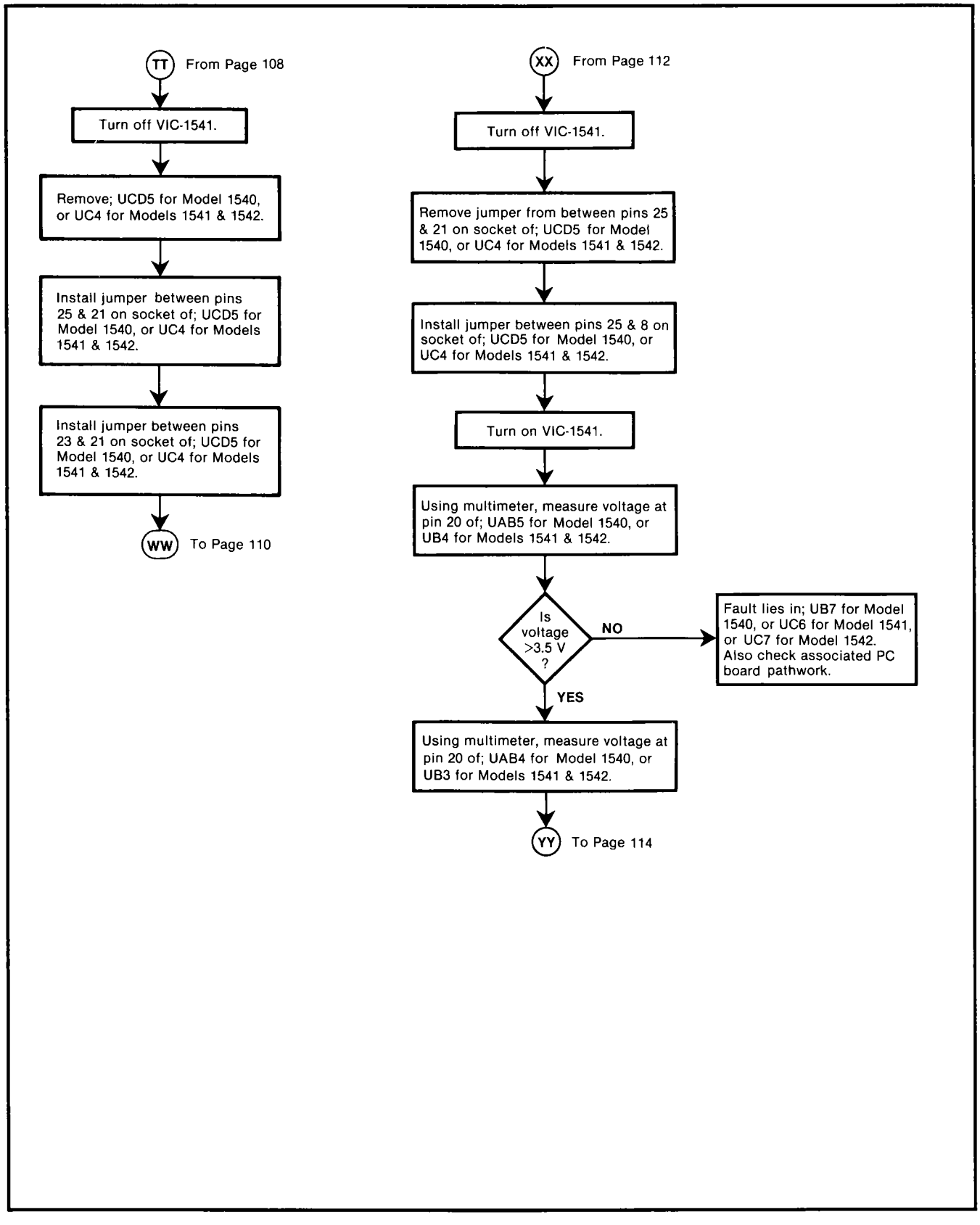
6.2.6 Faulty Computer Circuit (cont.)



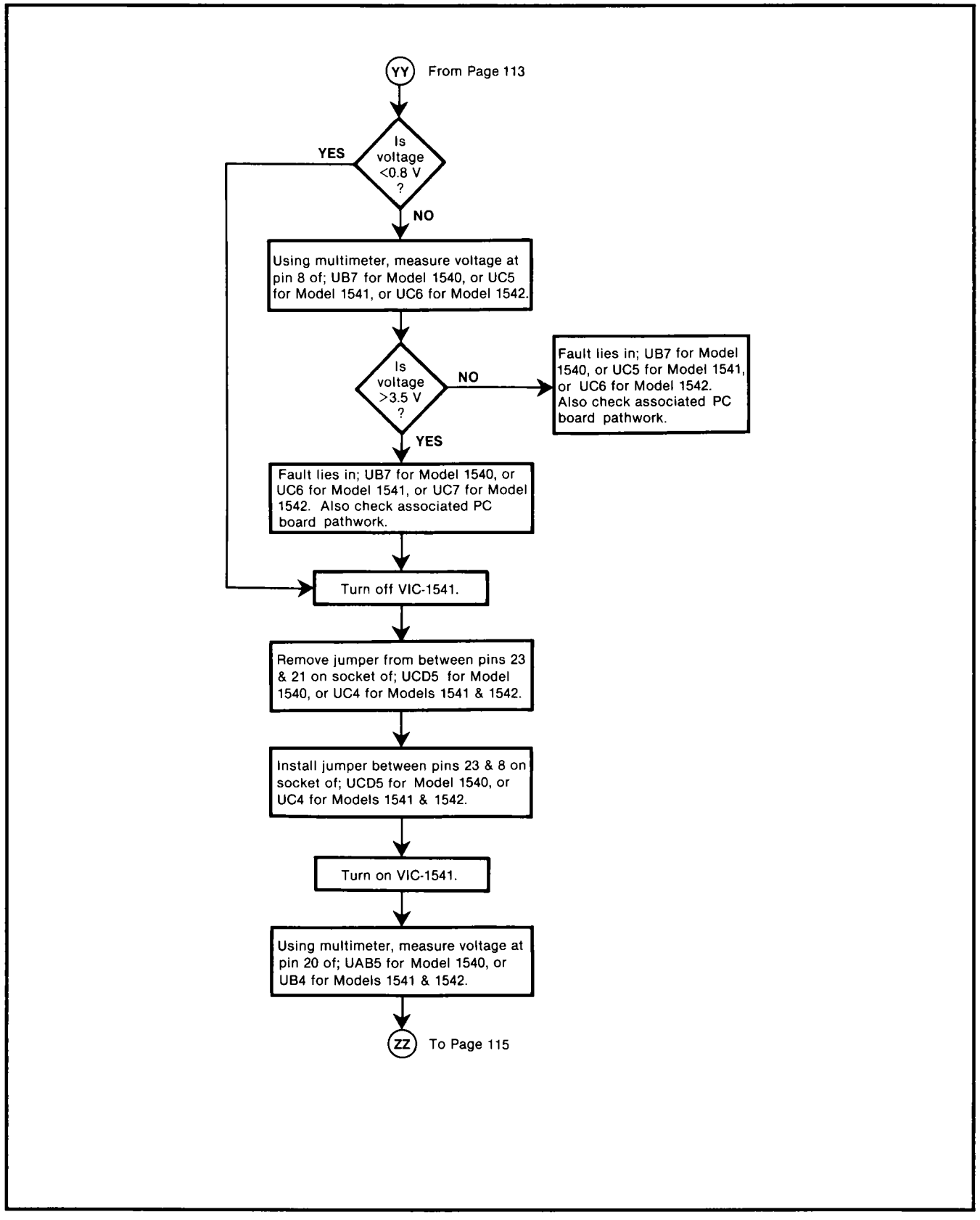
6.2.6 Faulty Computer Circuit (cont.)



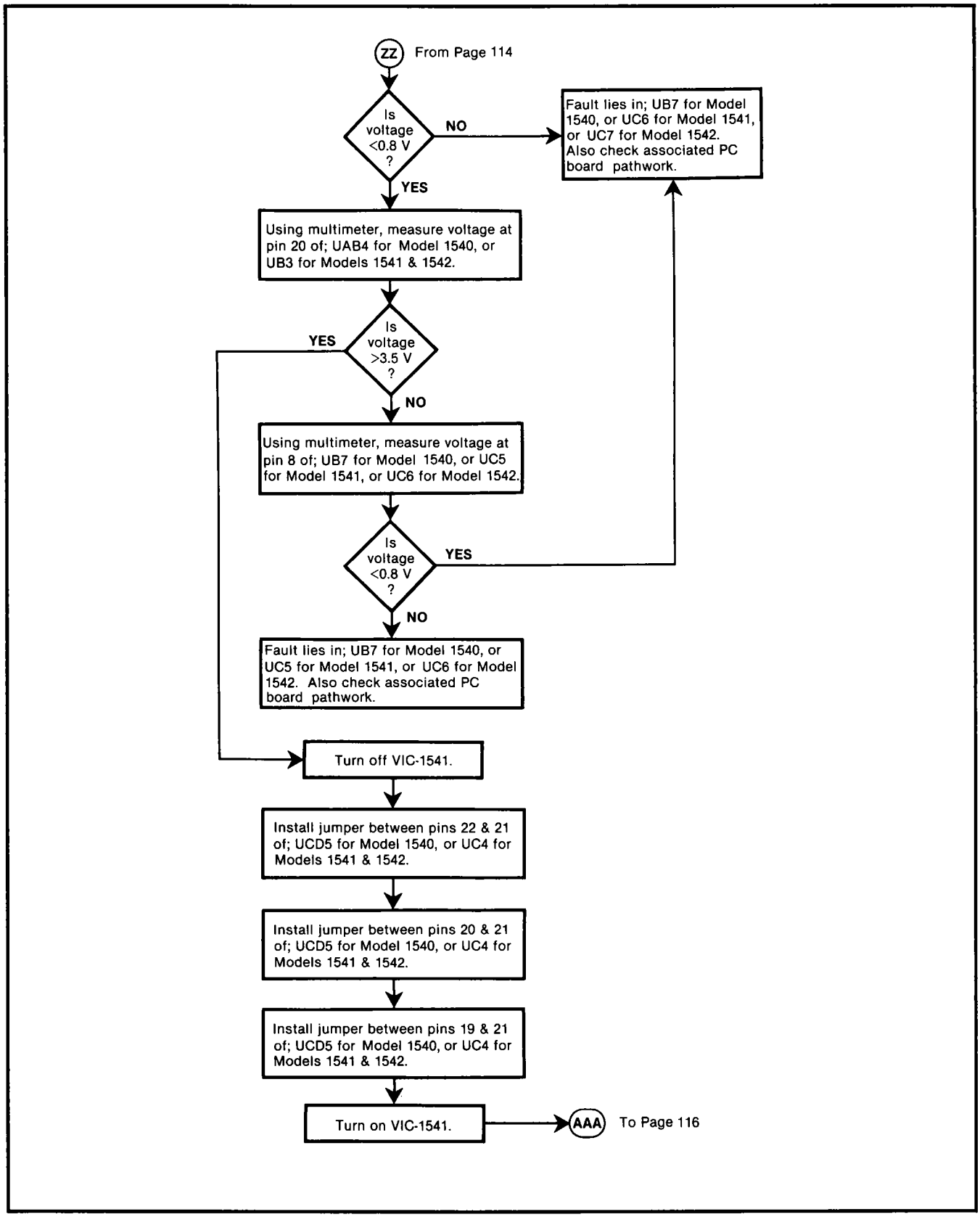
6.2.6 Faulty Computer Circuit (cont.)



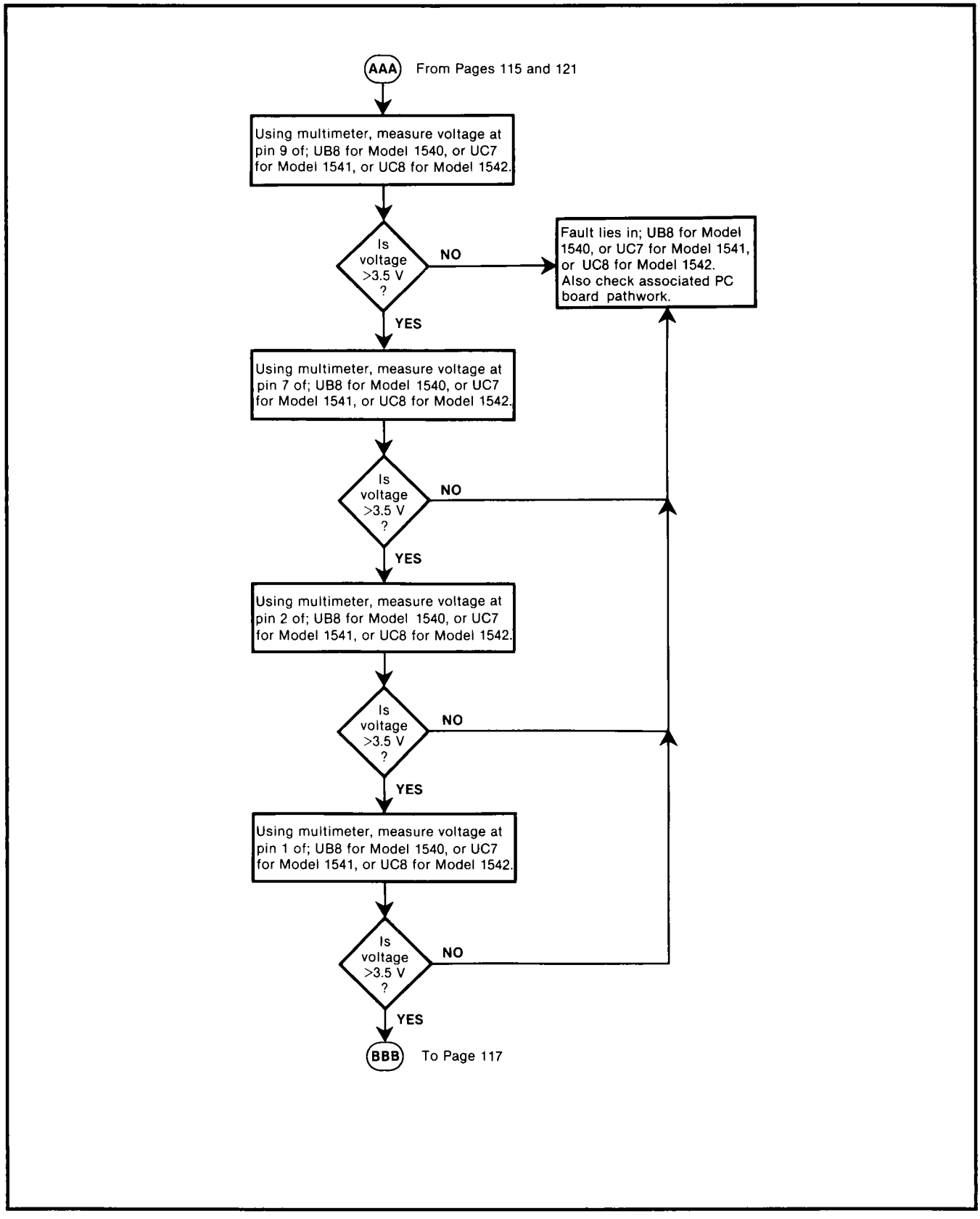
6.2.6 Faulty Computer Circuit (cont.)



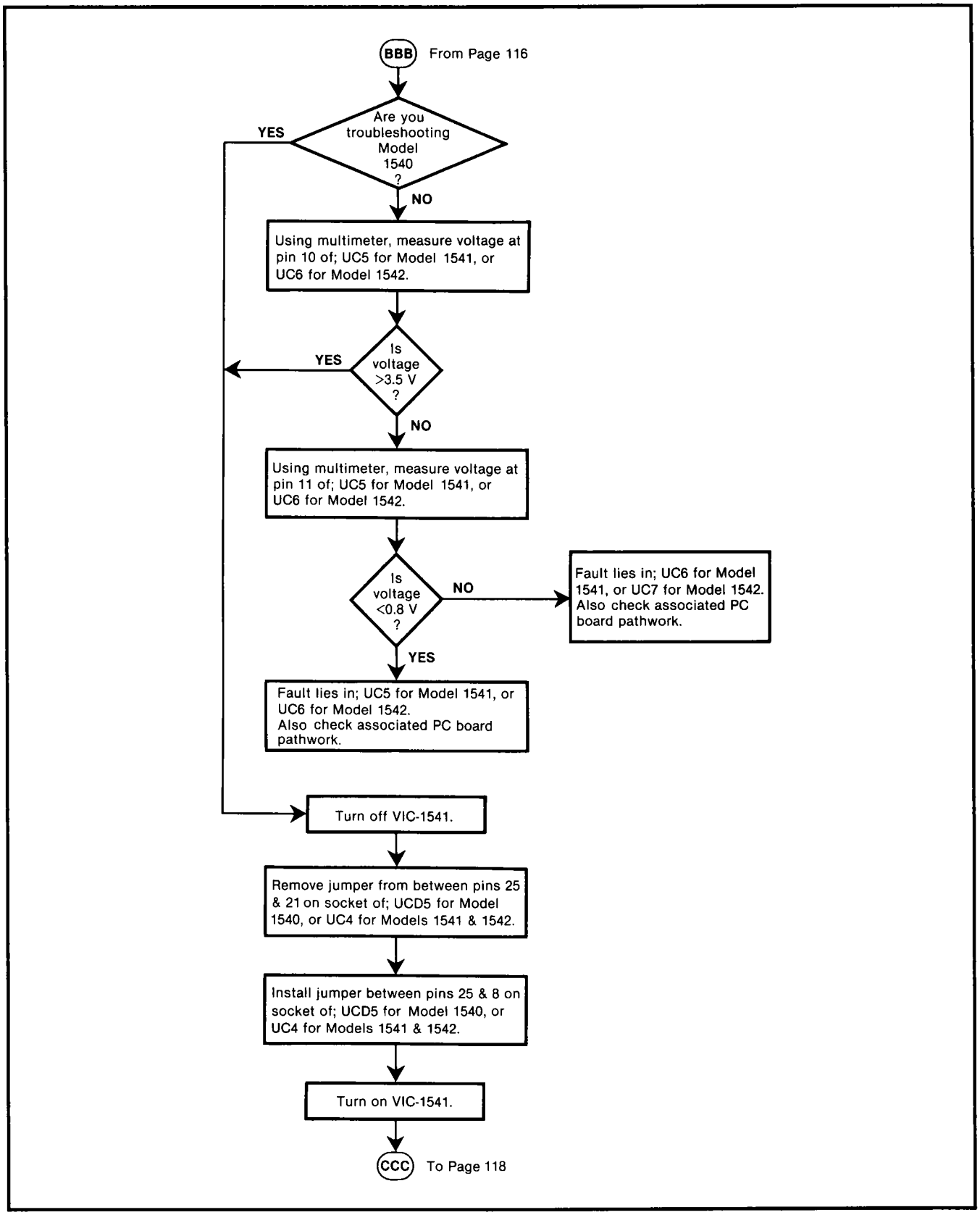
6.2.6 Faulty Computer Circuit (cont.)



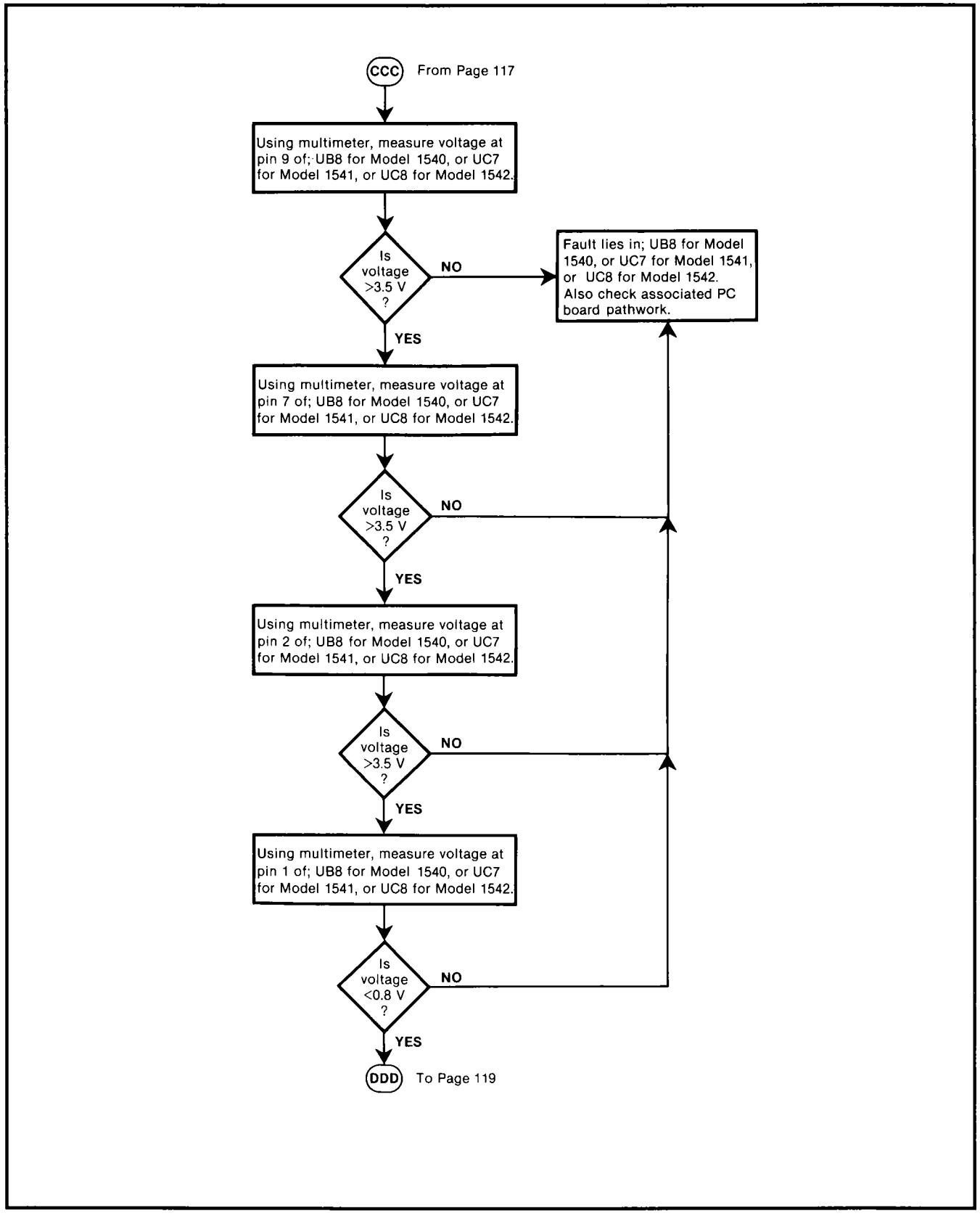
6.2.6 Faulty Computer Circuit (cont.)



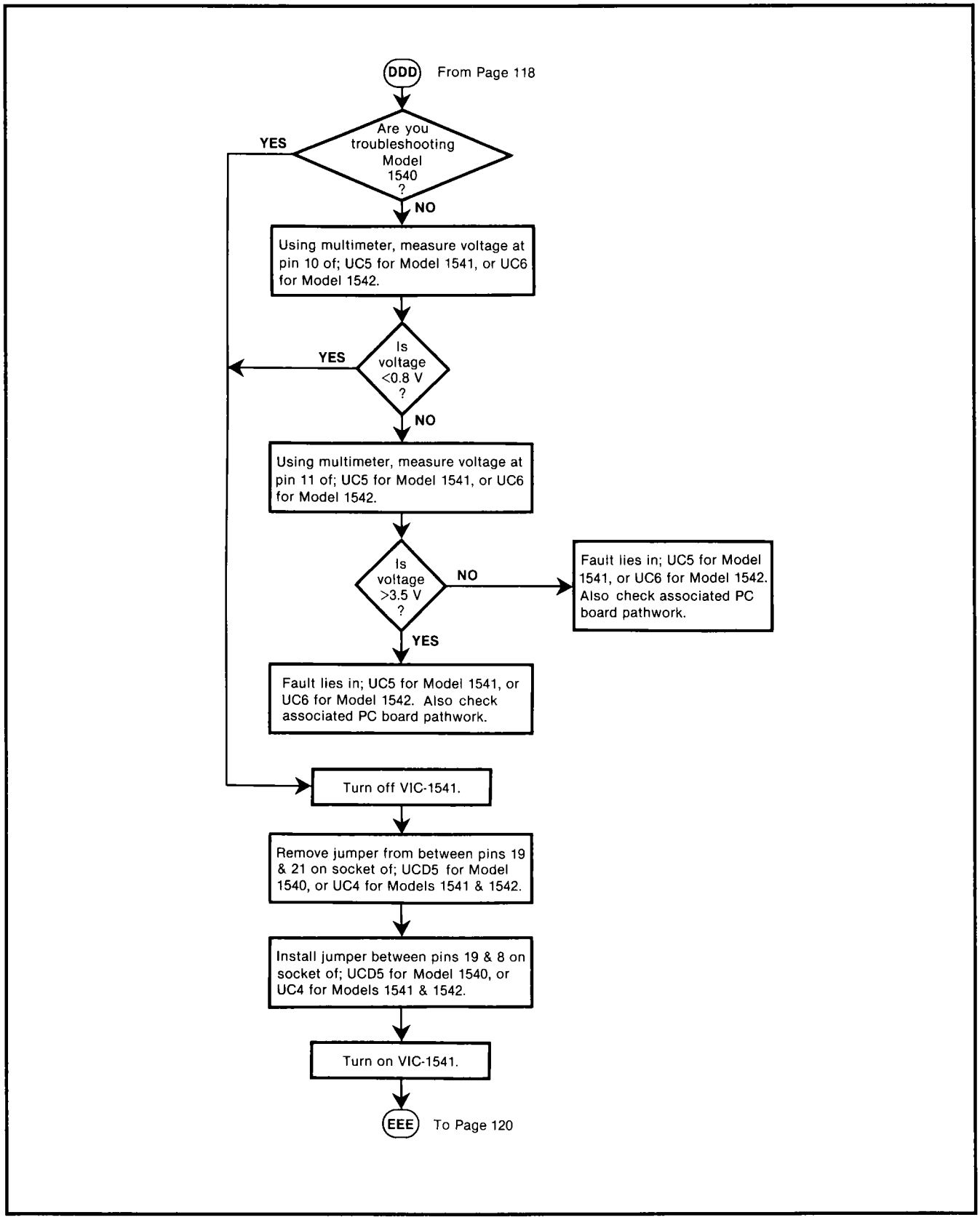
6.2.6 Faulty Computer Circuit (cont.)



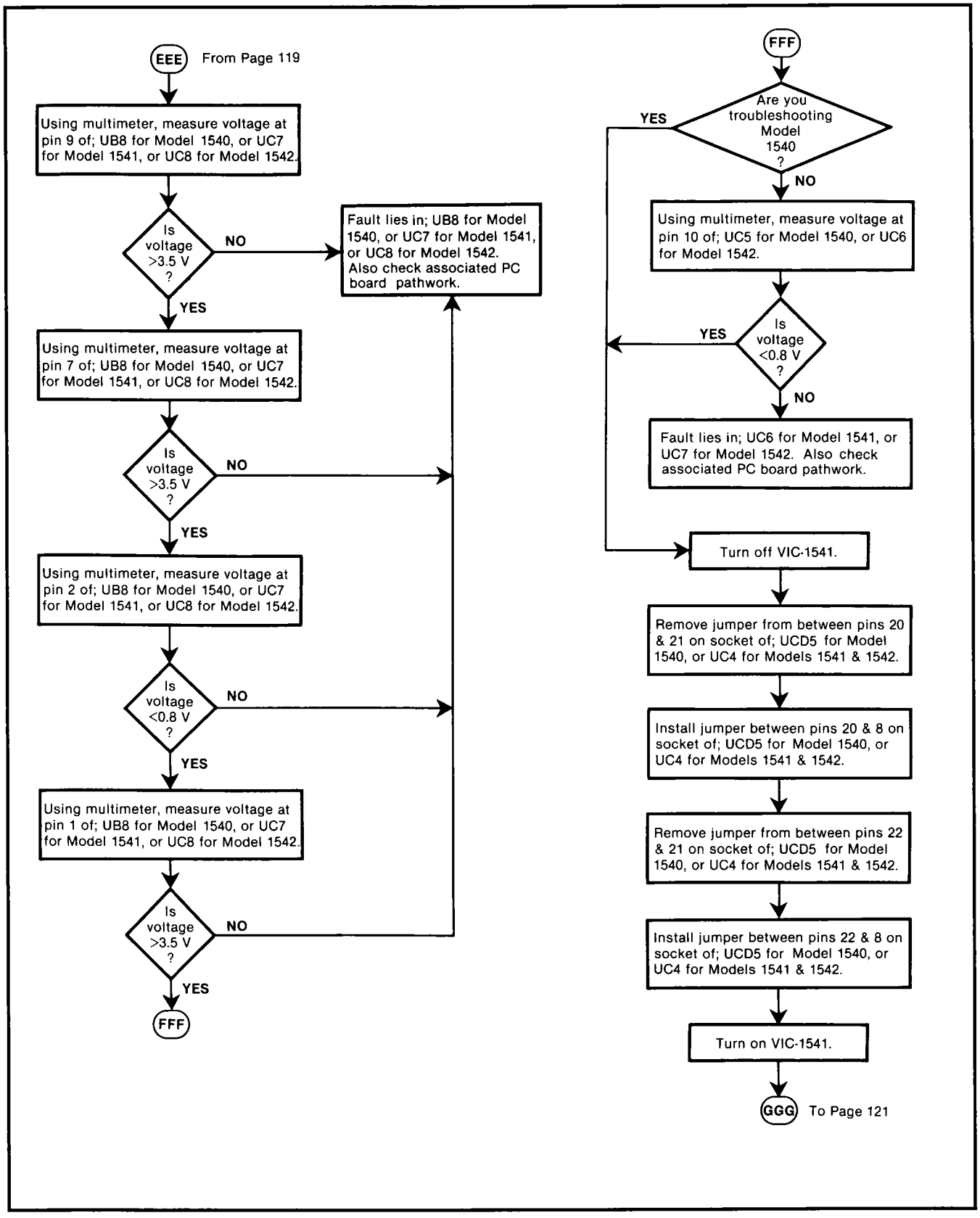
6.2.6 Faulty Computer Circuit (cont.)



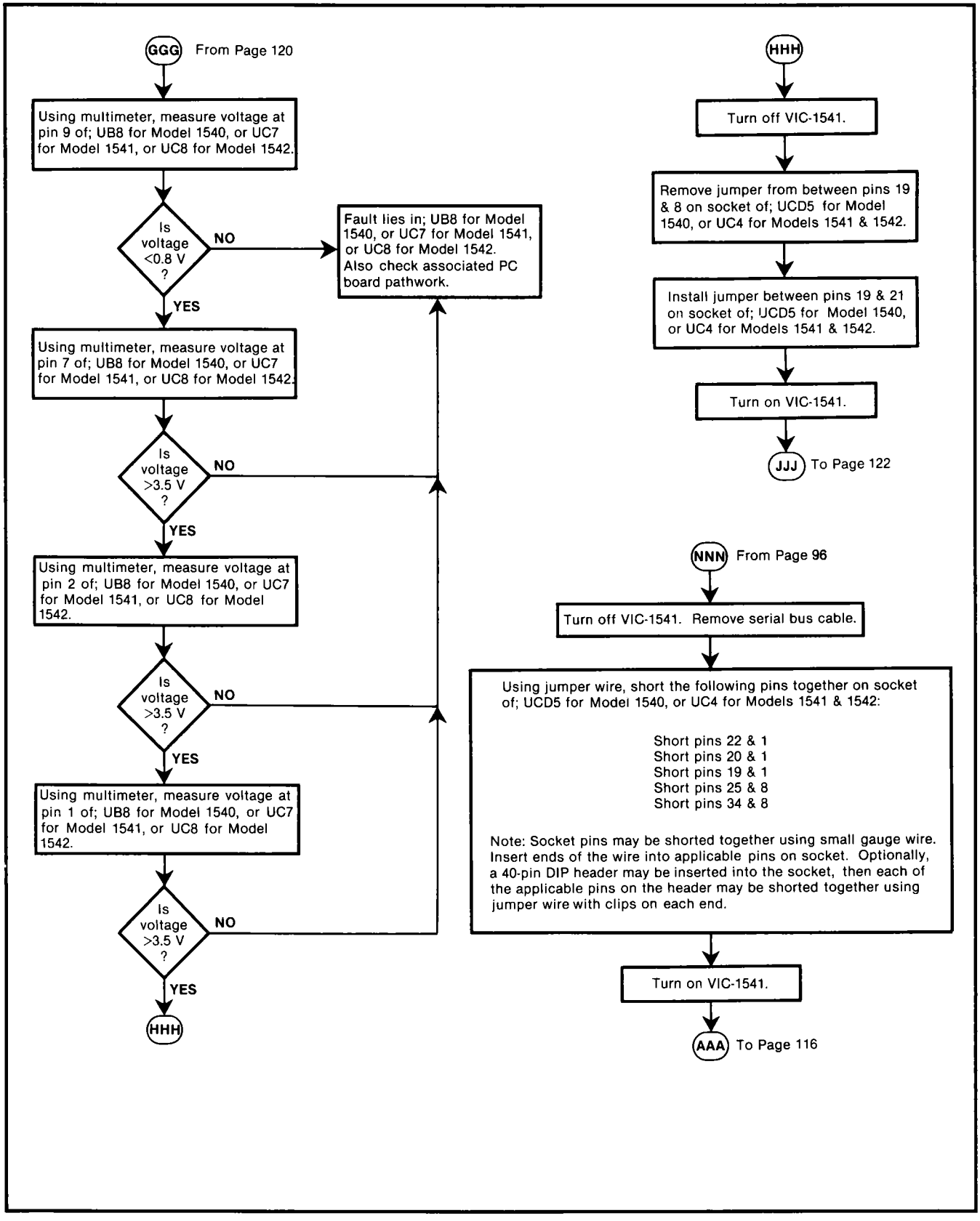
6.2.6 Faulty Computer Circuit (cont.)



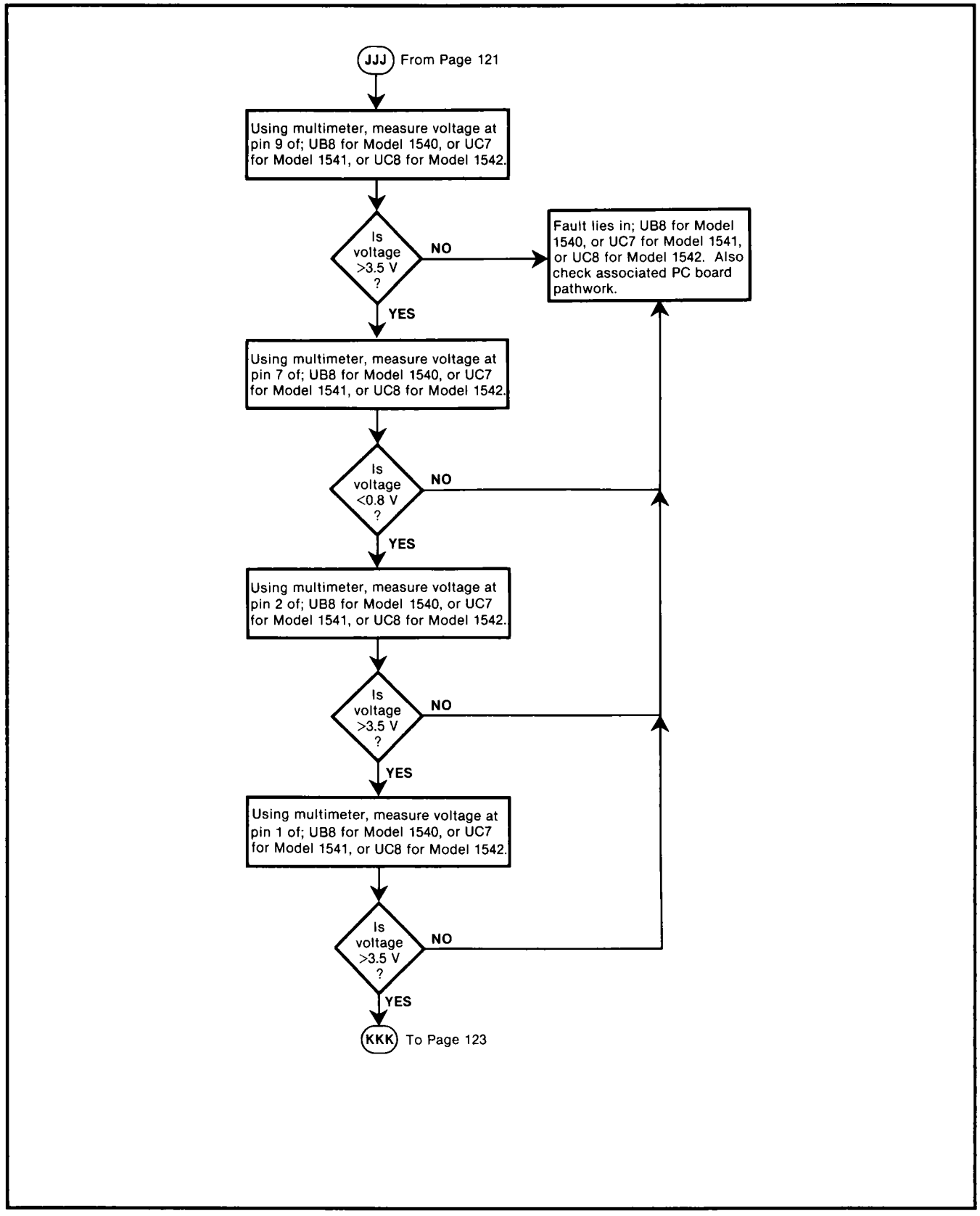
6.2.6 Faulty Computer Circuit (cont.)



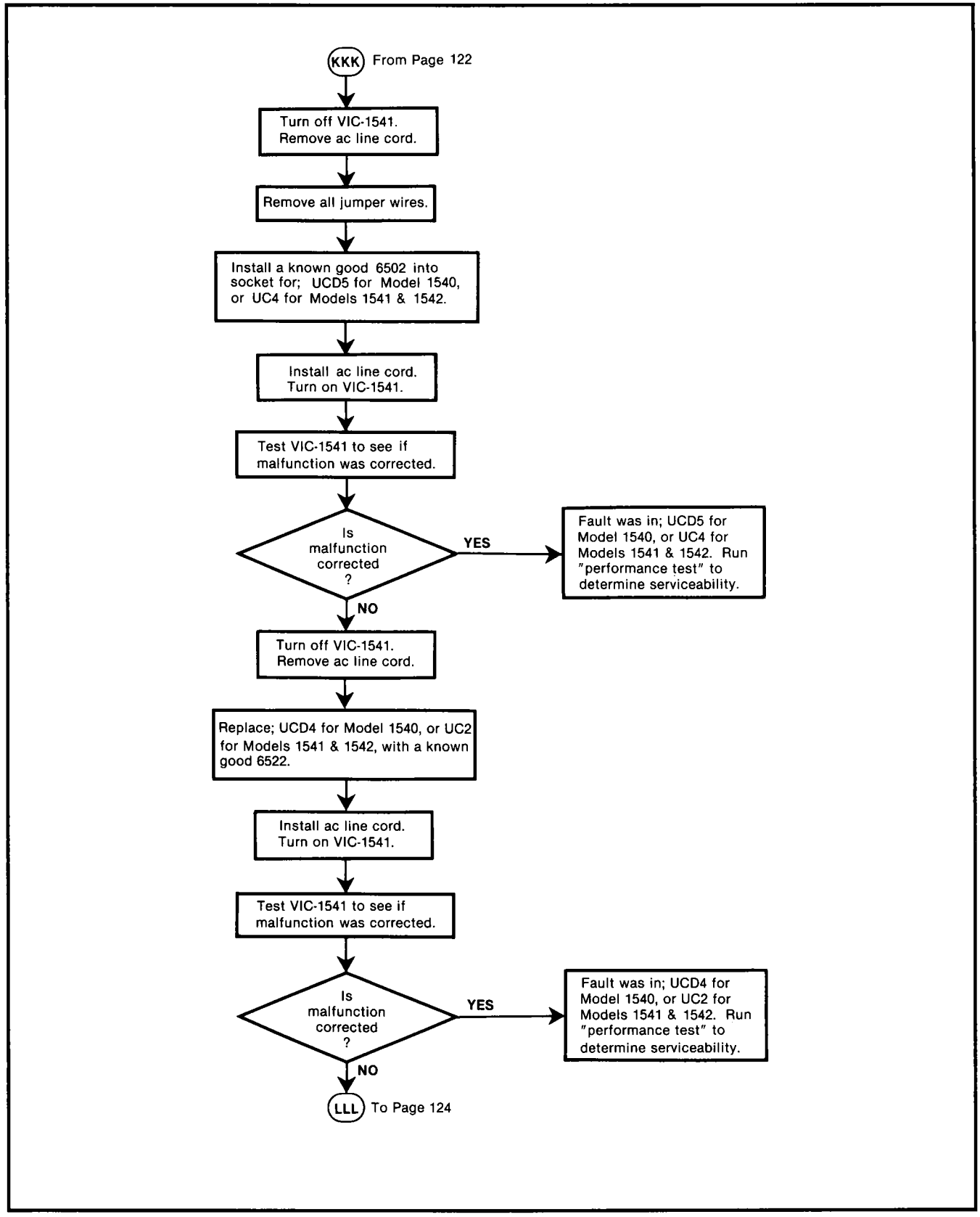
6.2.6 Faulty Computer Circuit (cont.)



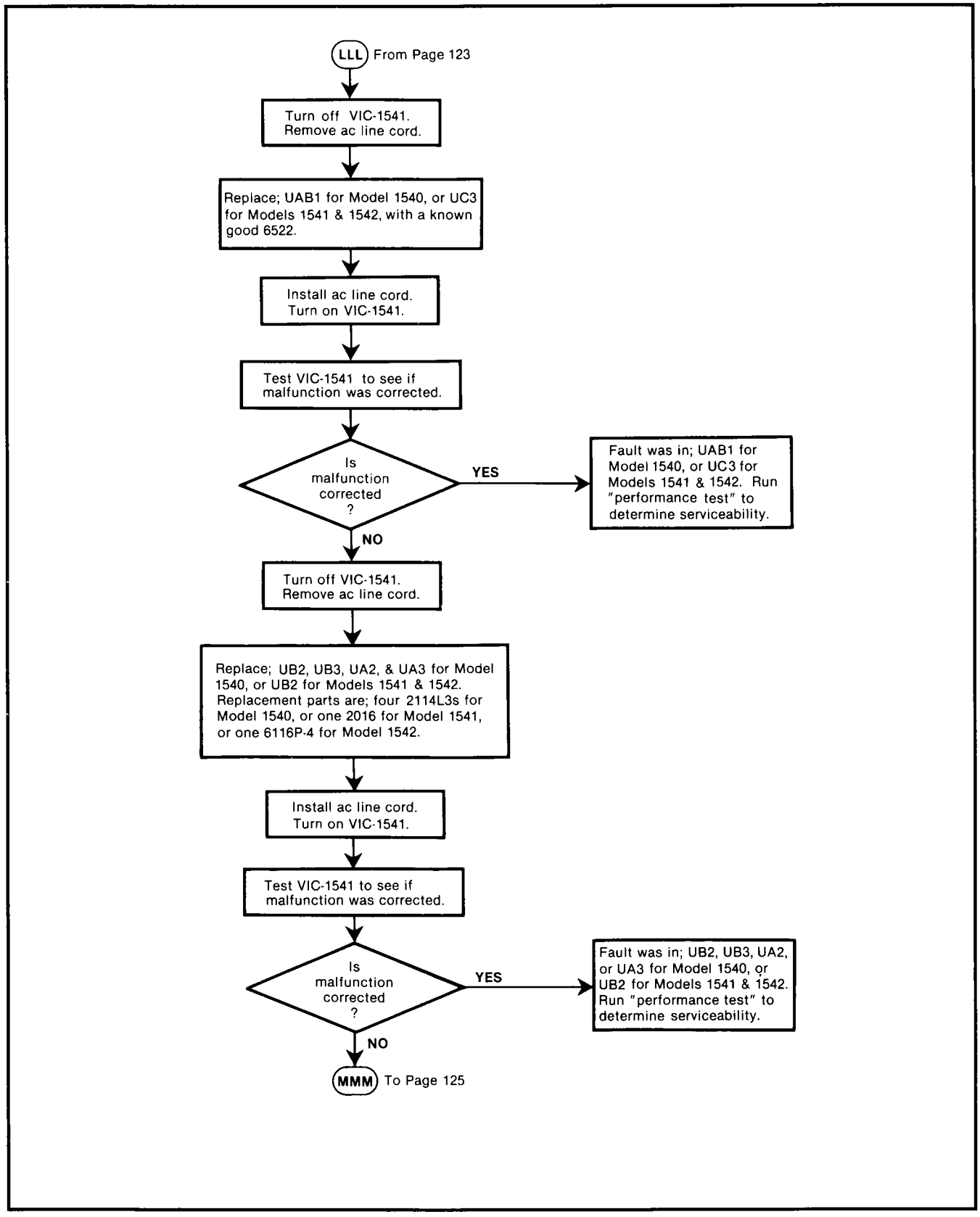
6.2.6 Faulty Computer Circuit (cont.)



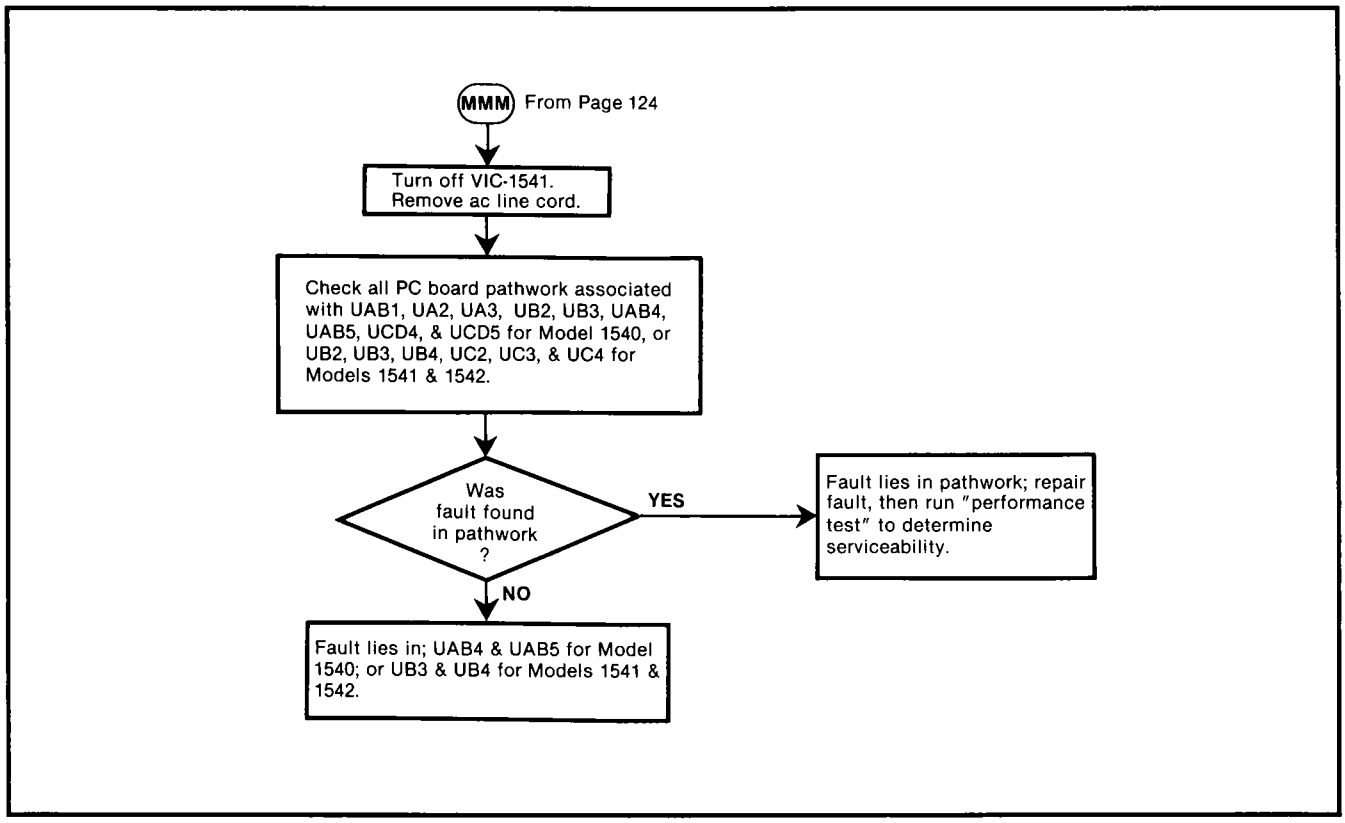
6.2.6 Faulty Computer Circuit (cont.)



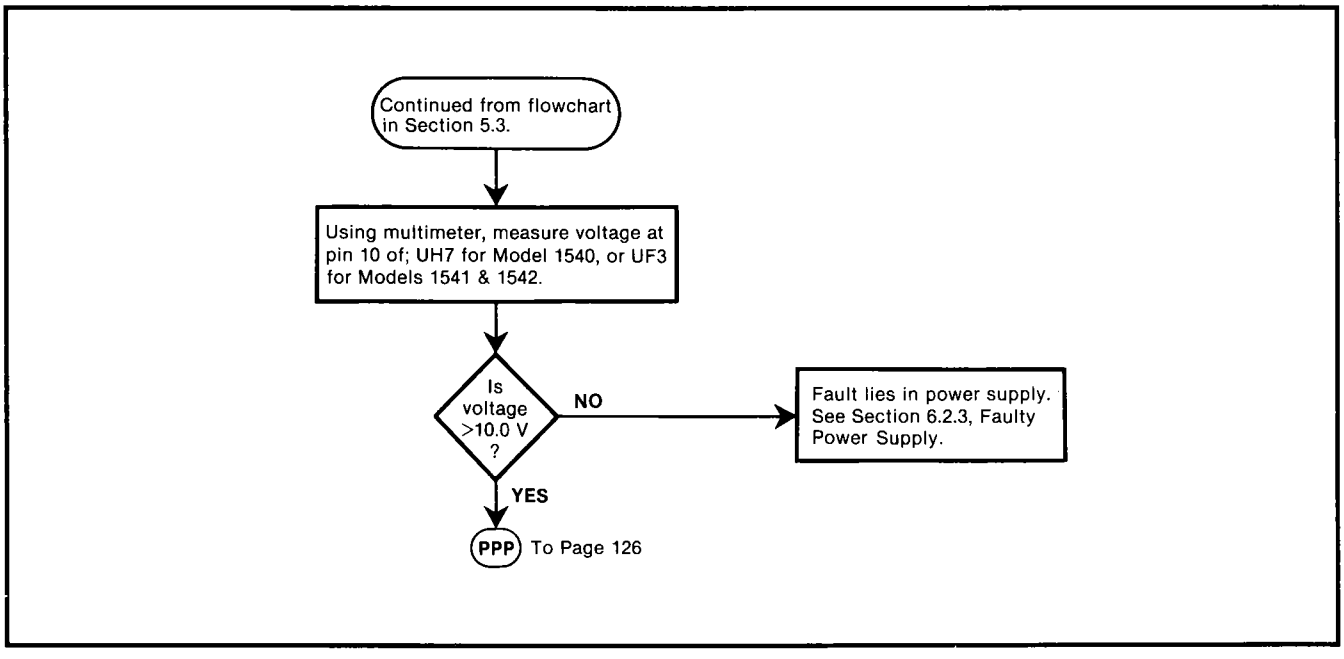
6.2.6 Faulty Computer Circuit (cont.)



6.2.6 Faulty Computer Circuit (cont.)



6.2.7 Faulty Read/Write Circuit



6.2.7 Faulty Read/Write Circuit (cont.)

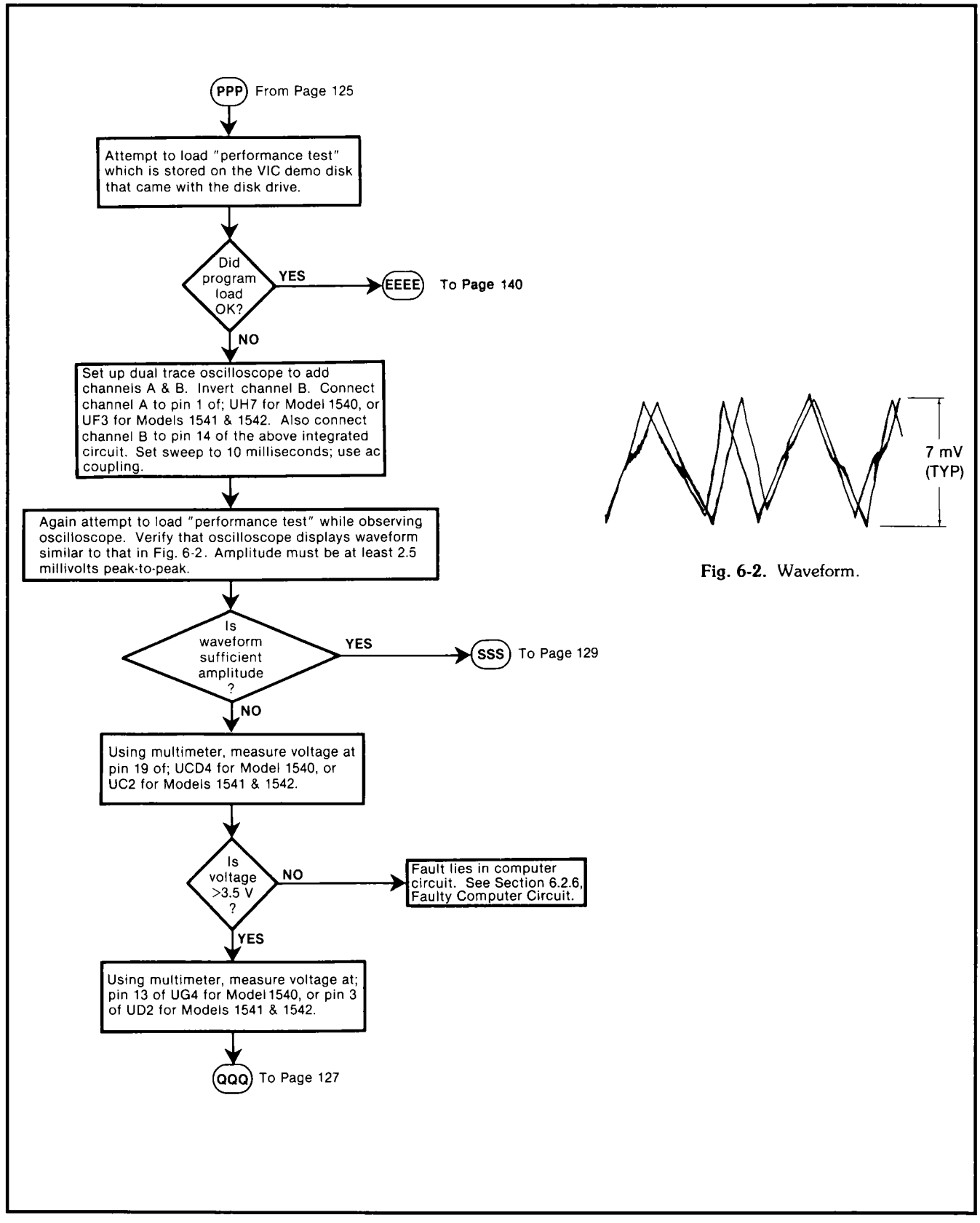
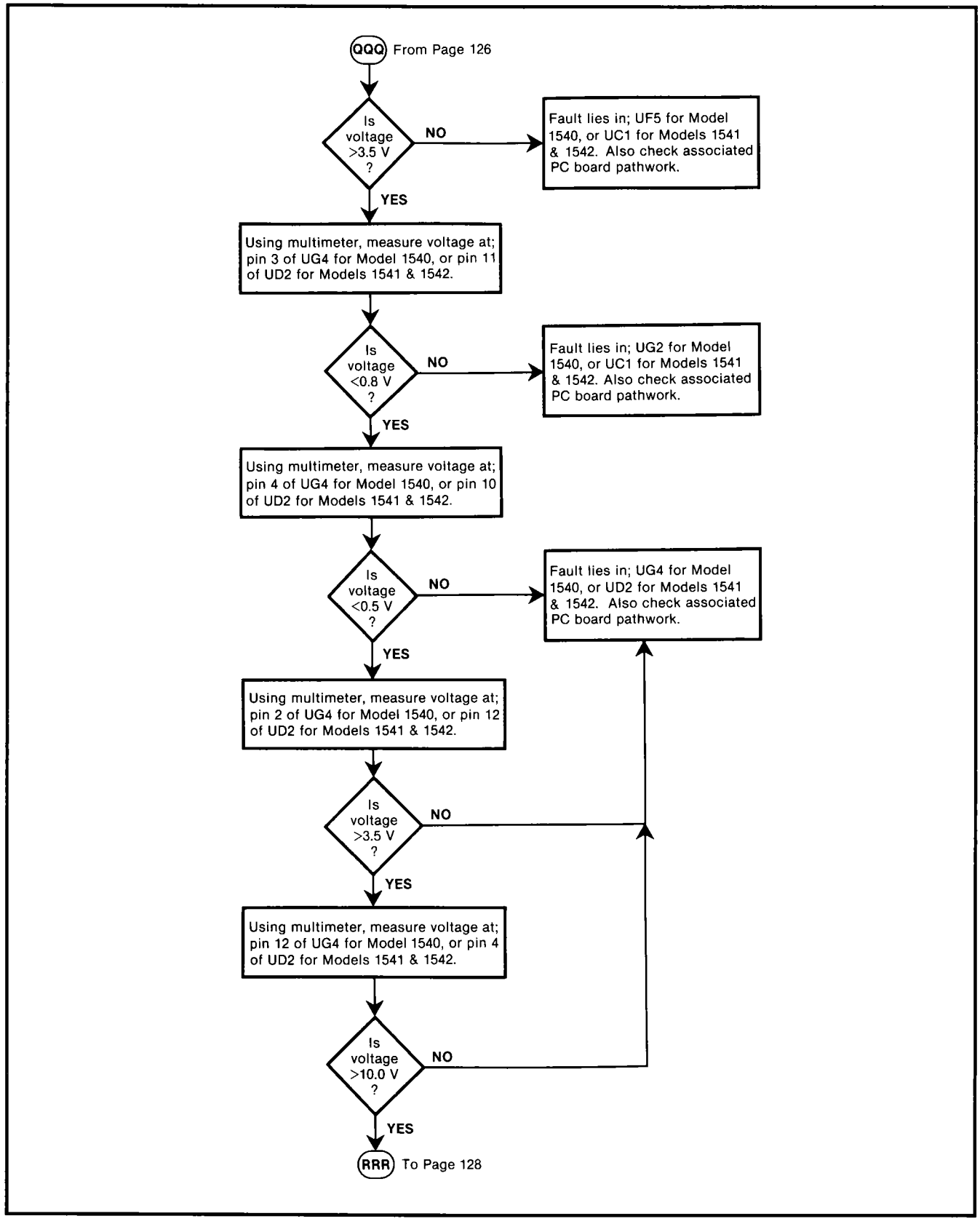
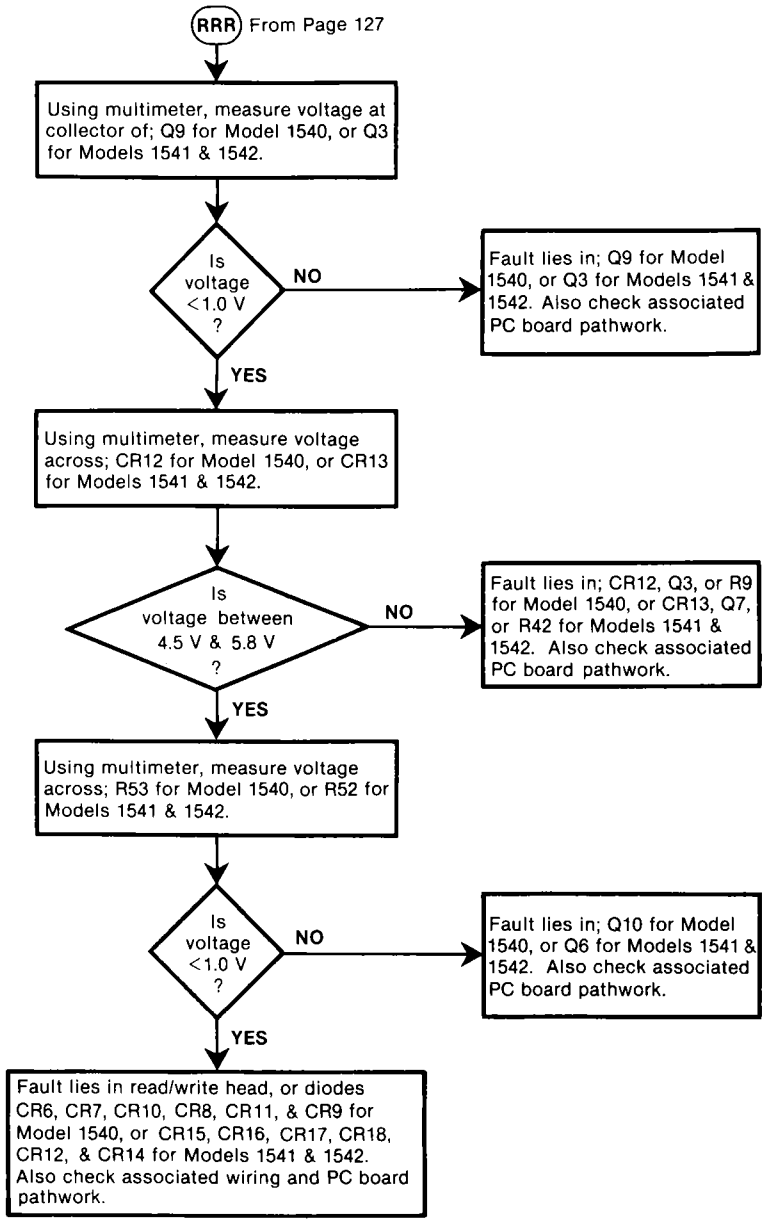


Fig. 6-2. Waveform.

6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)

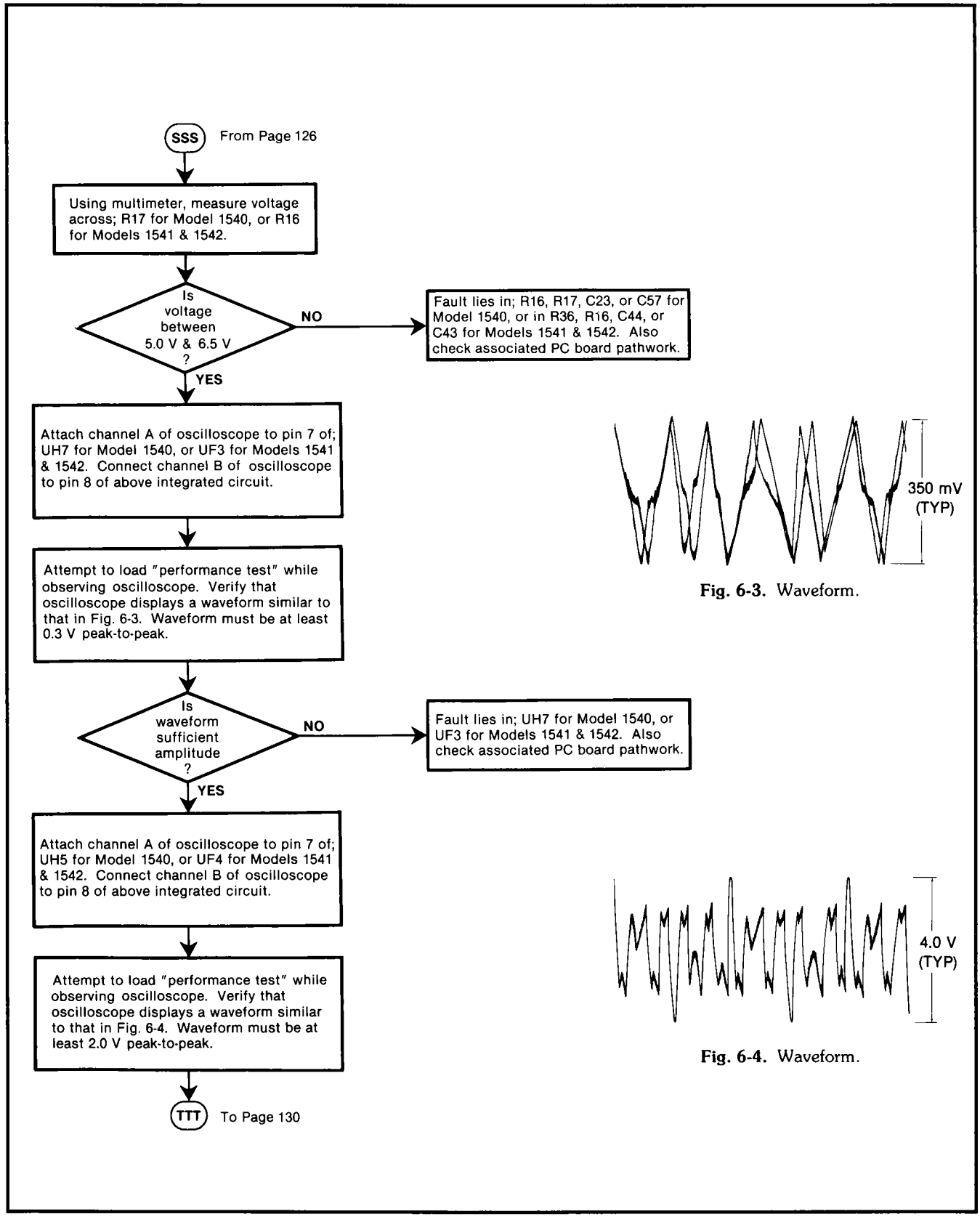
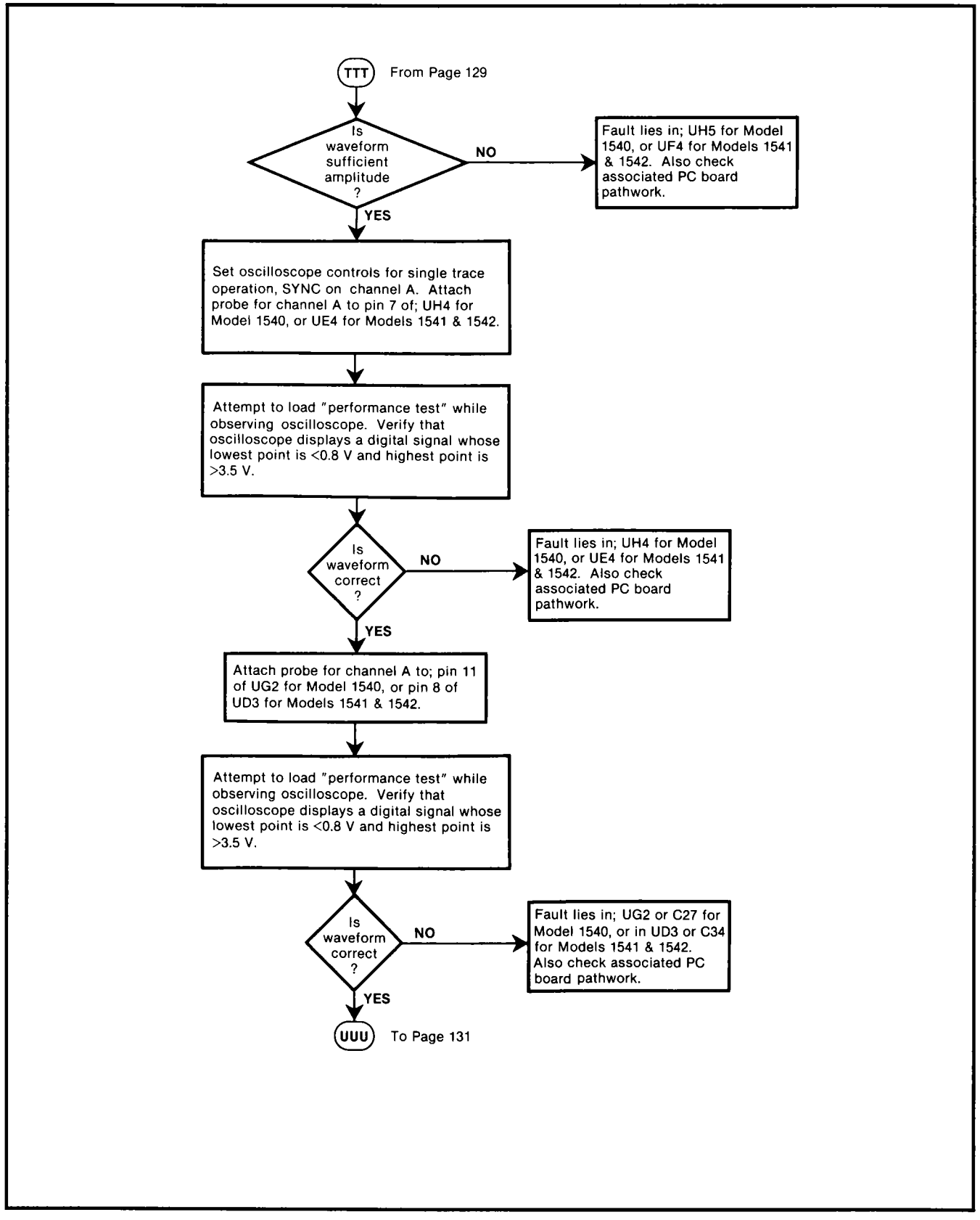


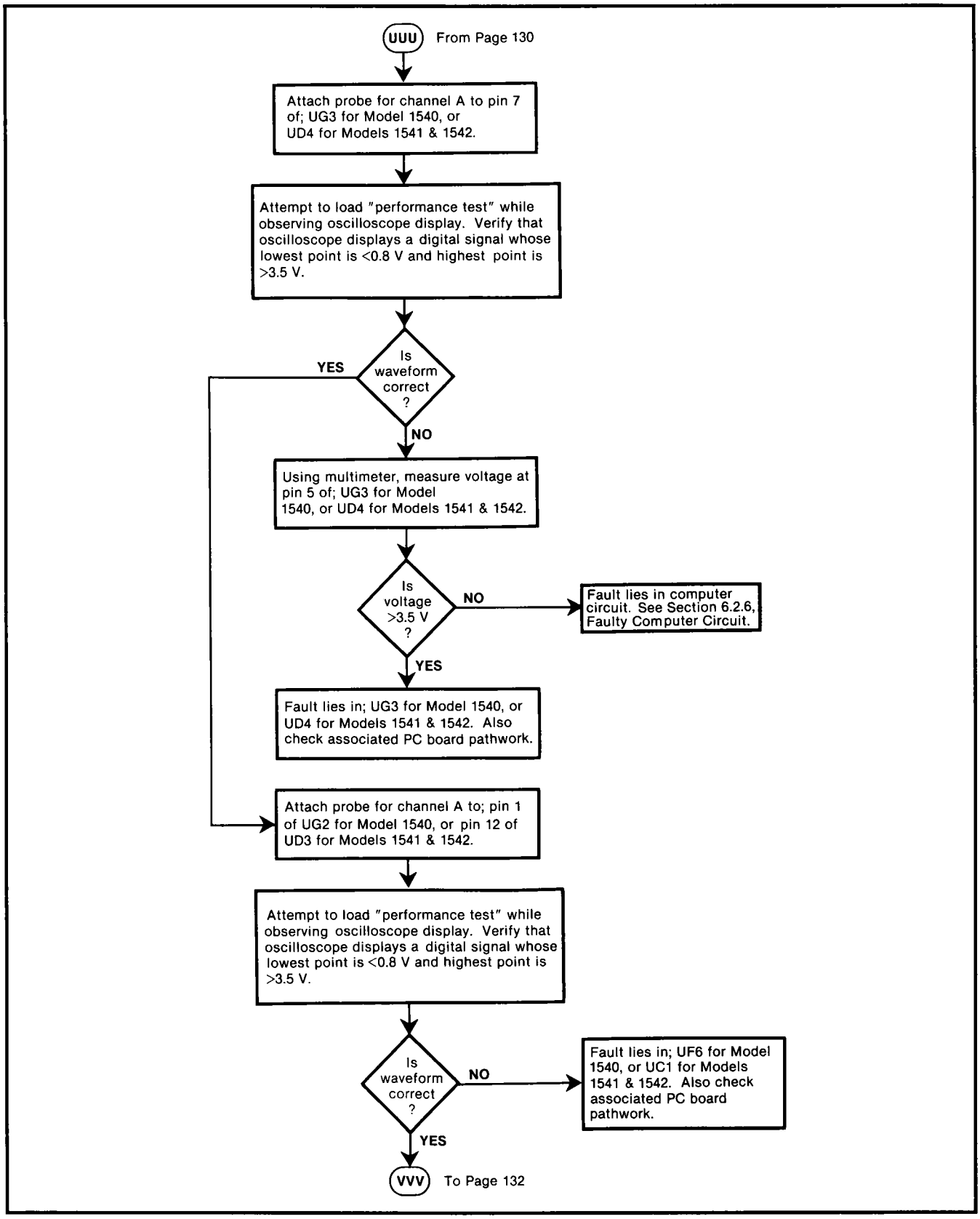
Fig. 6-3. Waveform.

Fig. 6-4. Waveform.

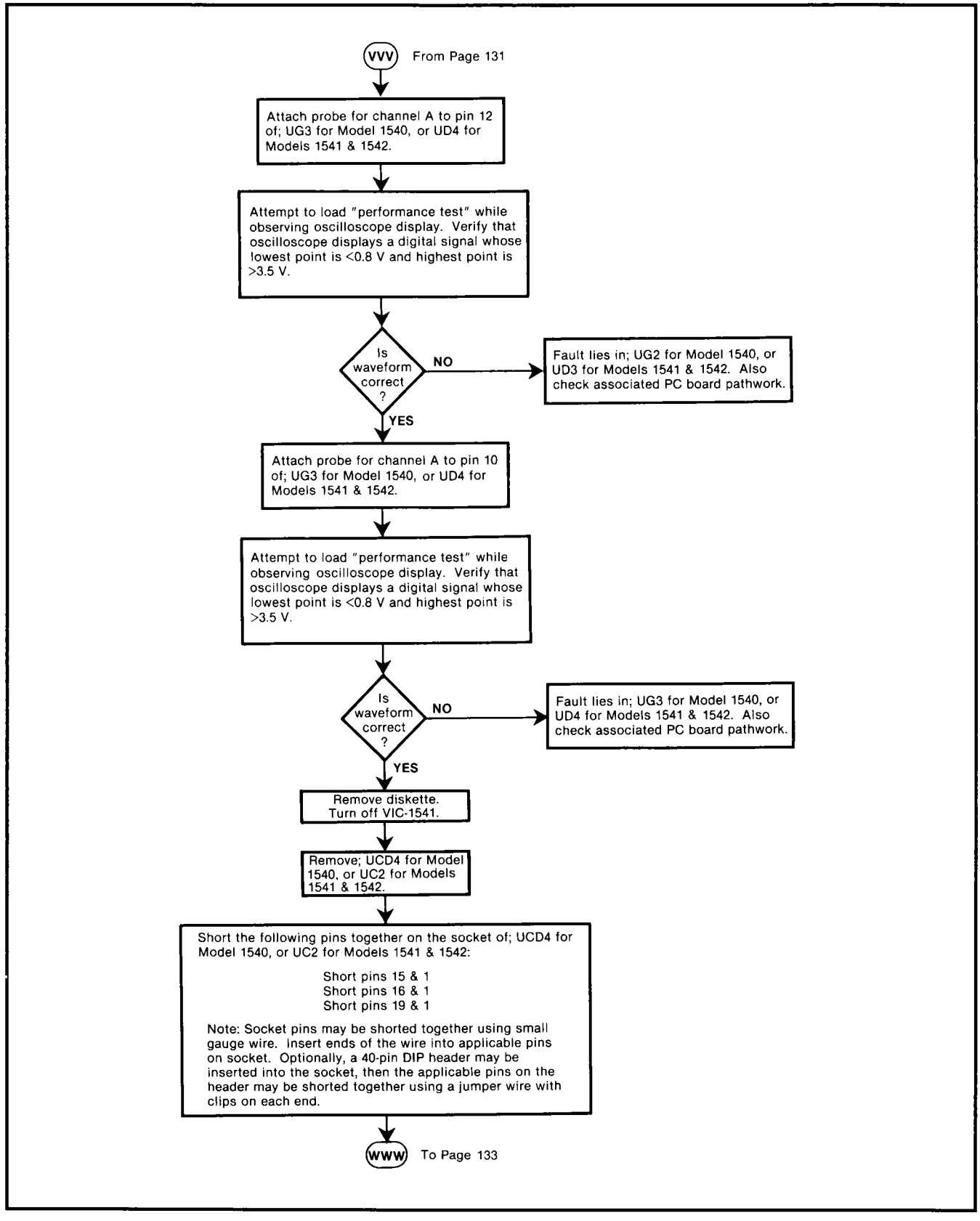
6.2.7 Faulty Read/Write Circuit (cont.)



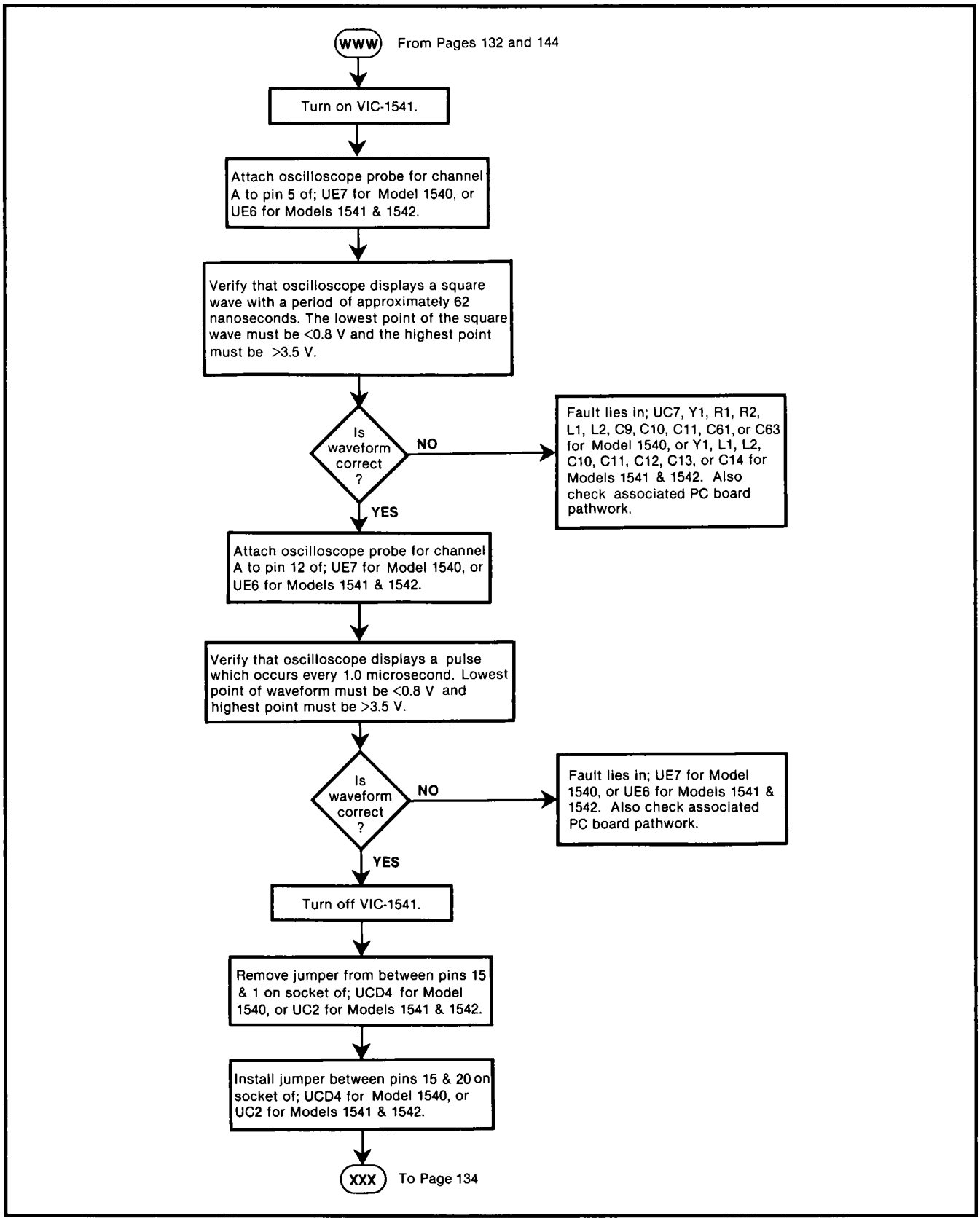
6.2.7 Faulty Read/Write Circuit (cont.)



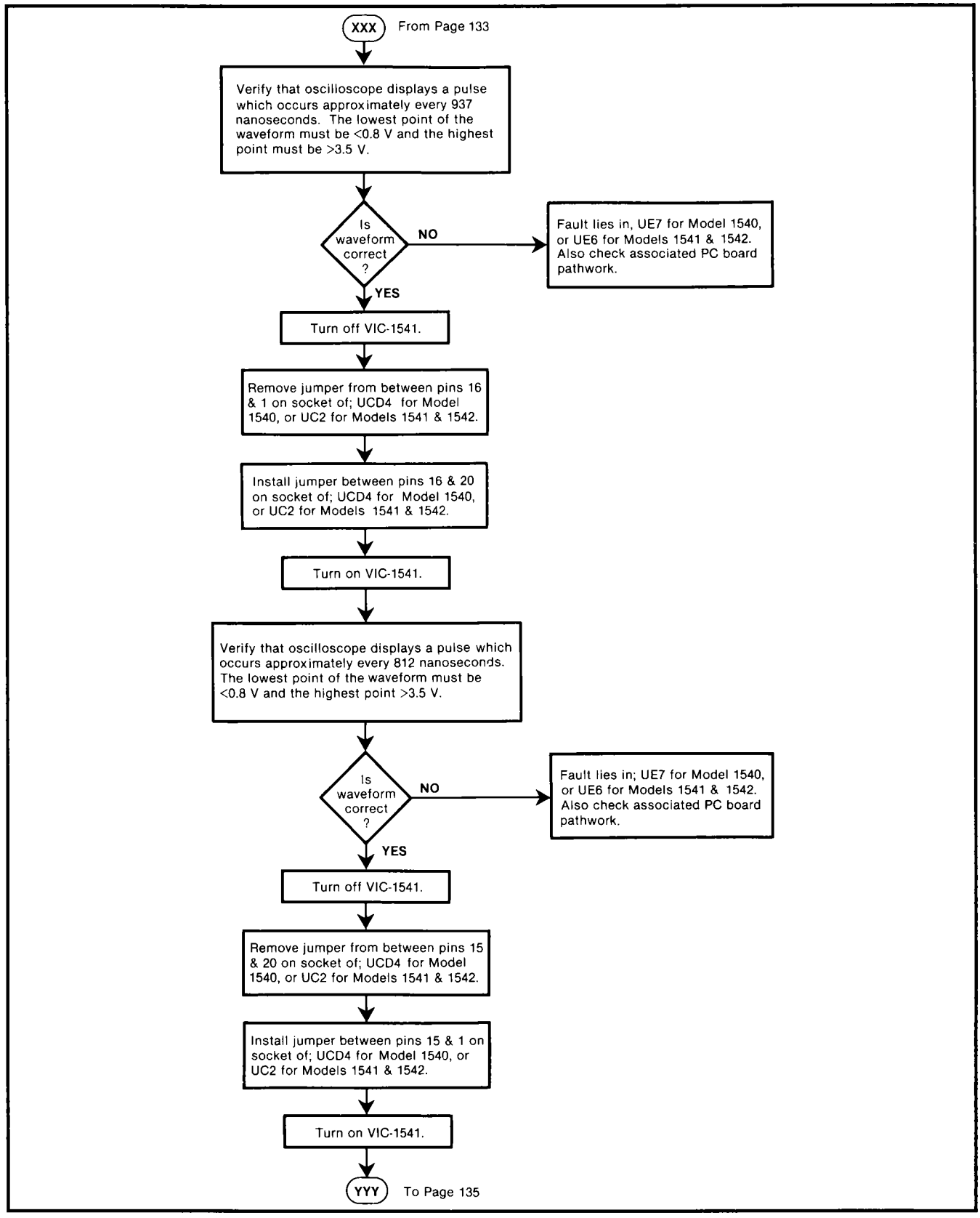
6.2.7 Faulty Read/Write Circuit (cont.)



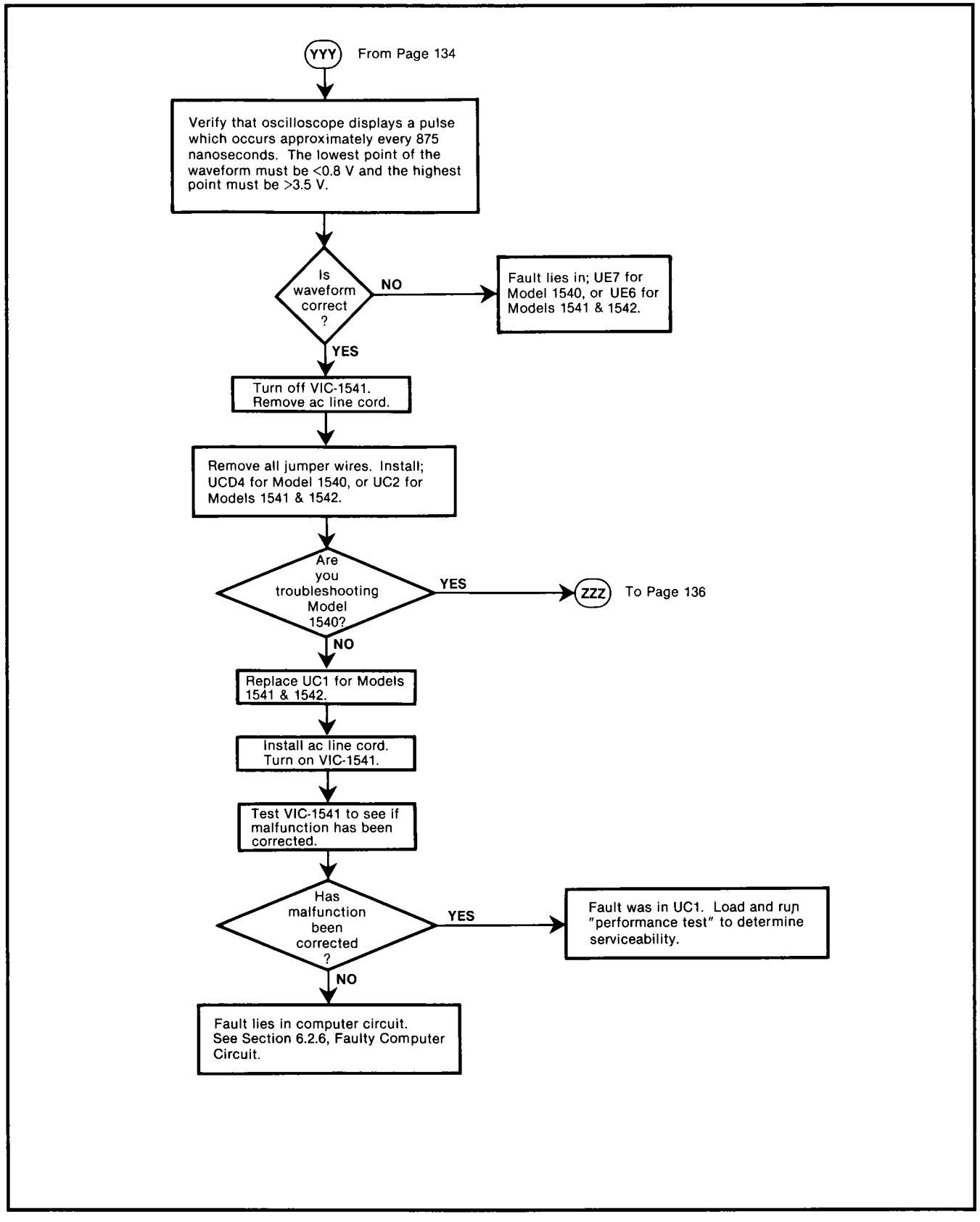
6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)



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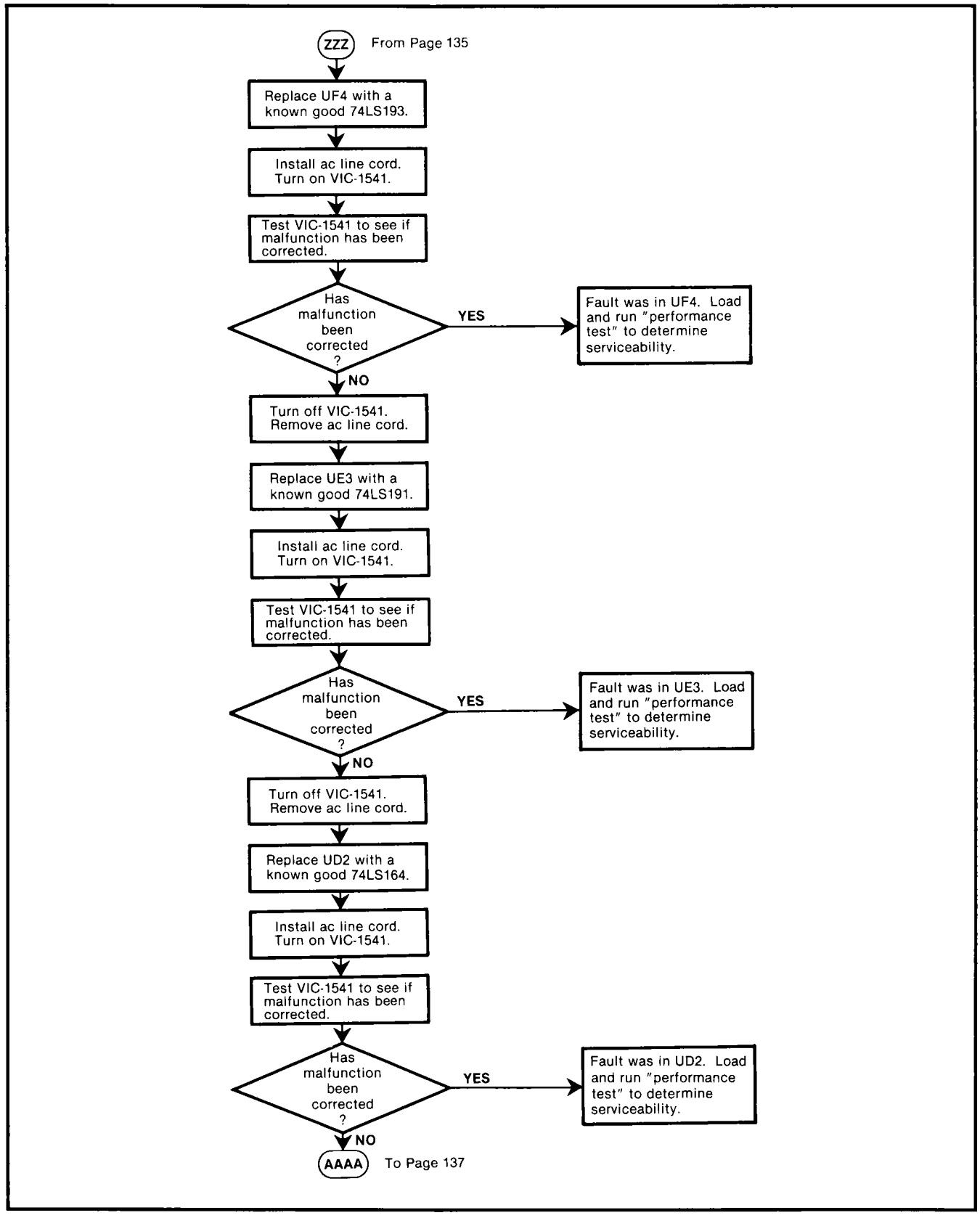
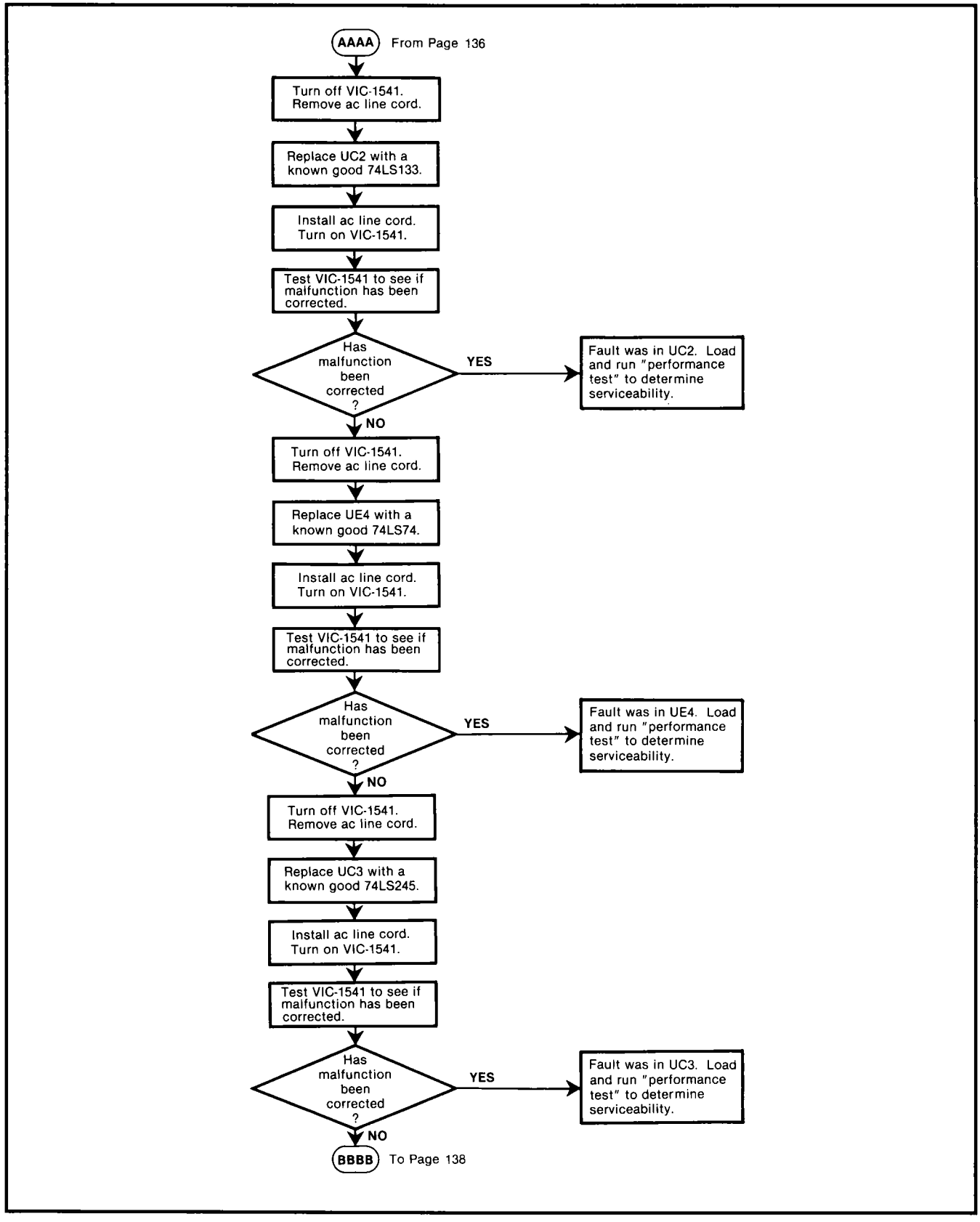
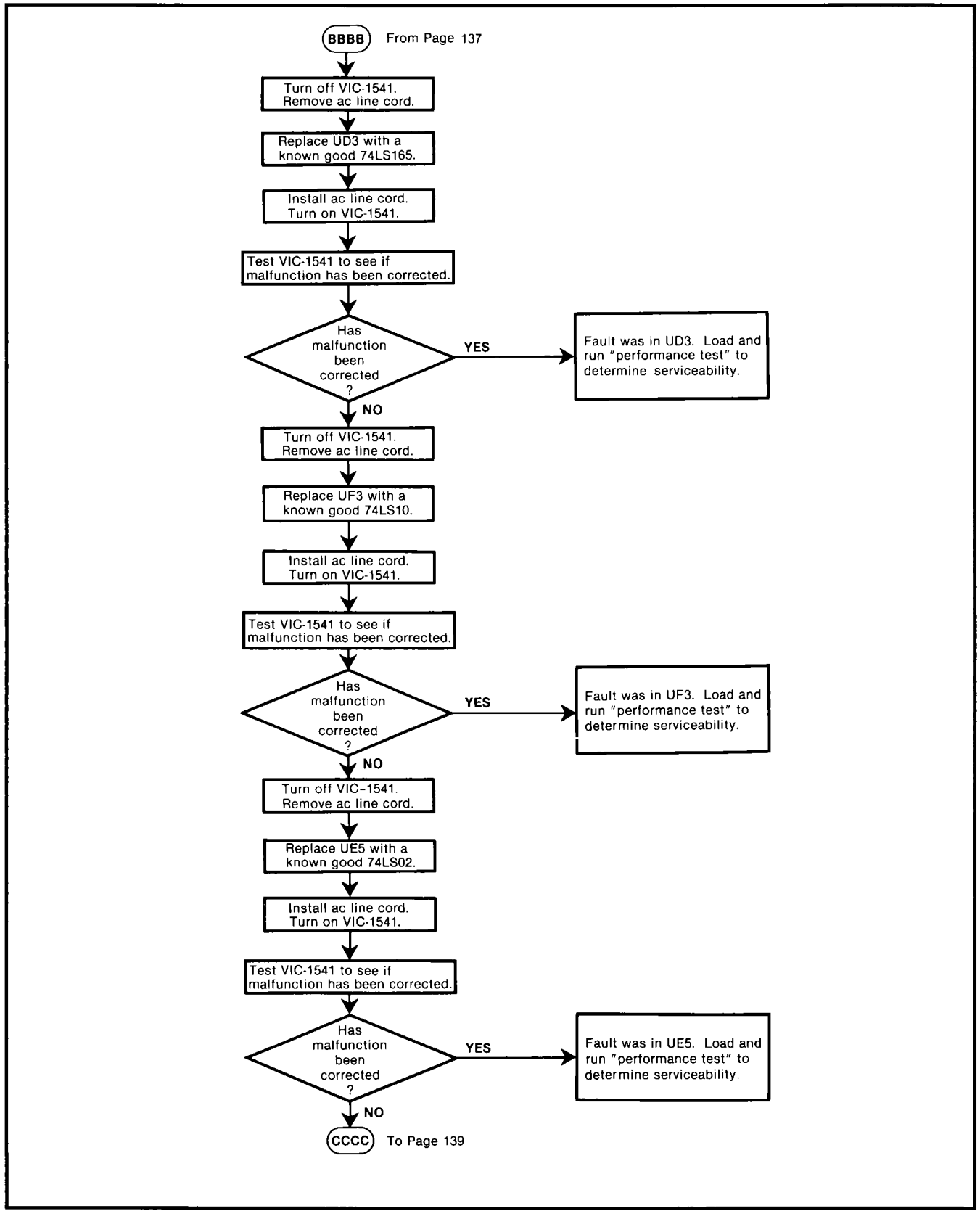


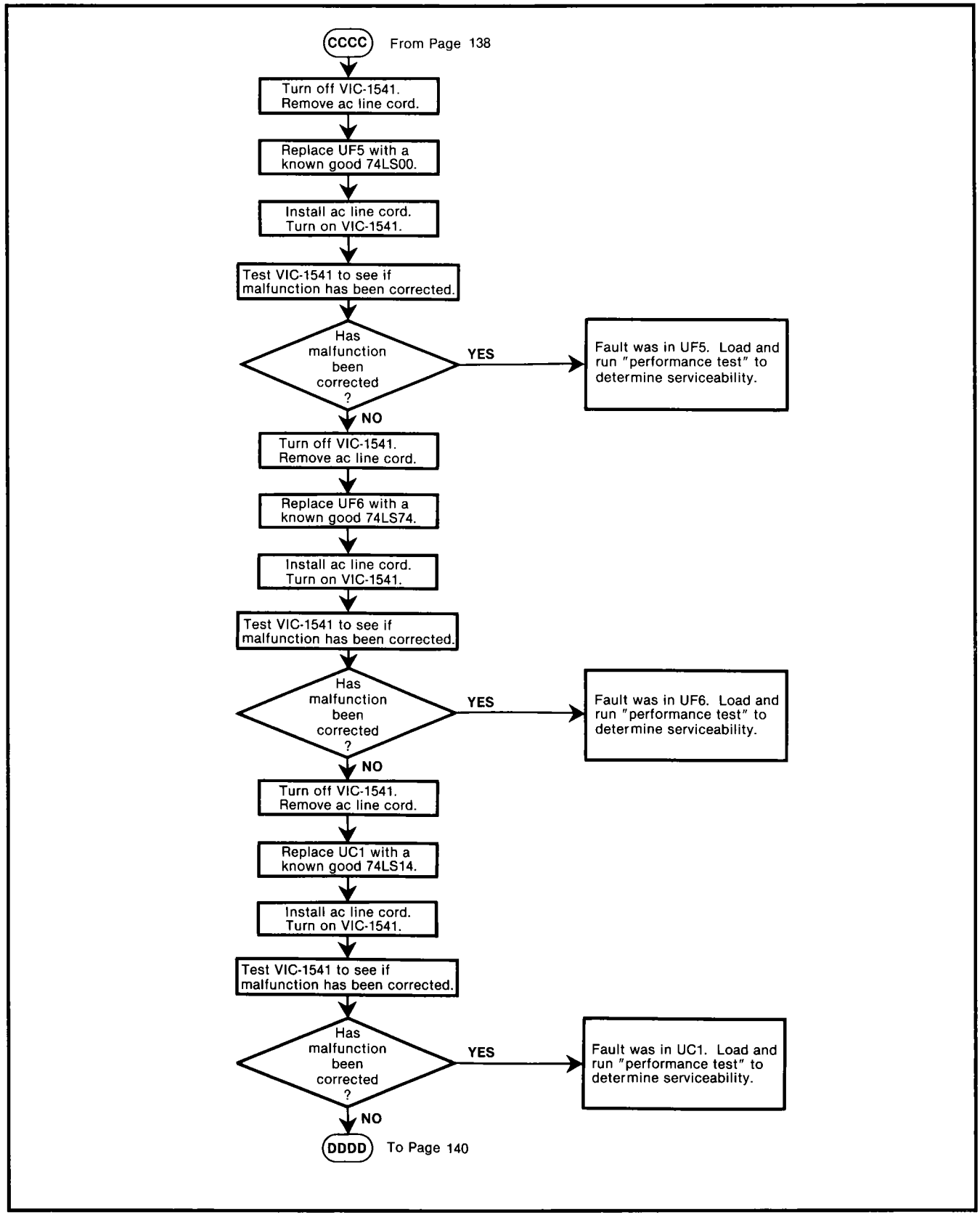
6.2.7 Faulty Read/Write Circuit (cont.)



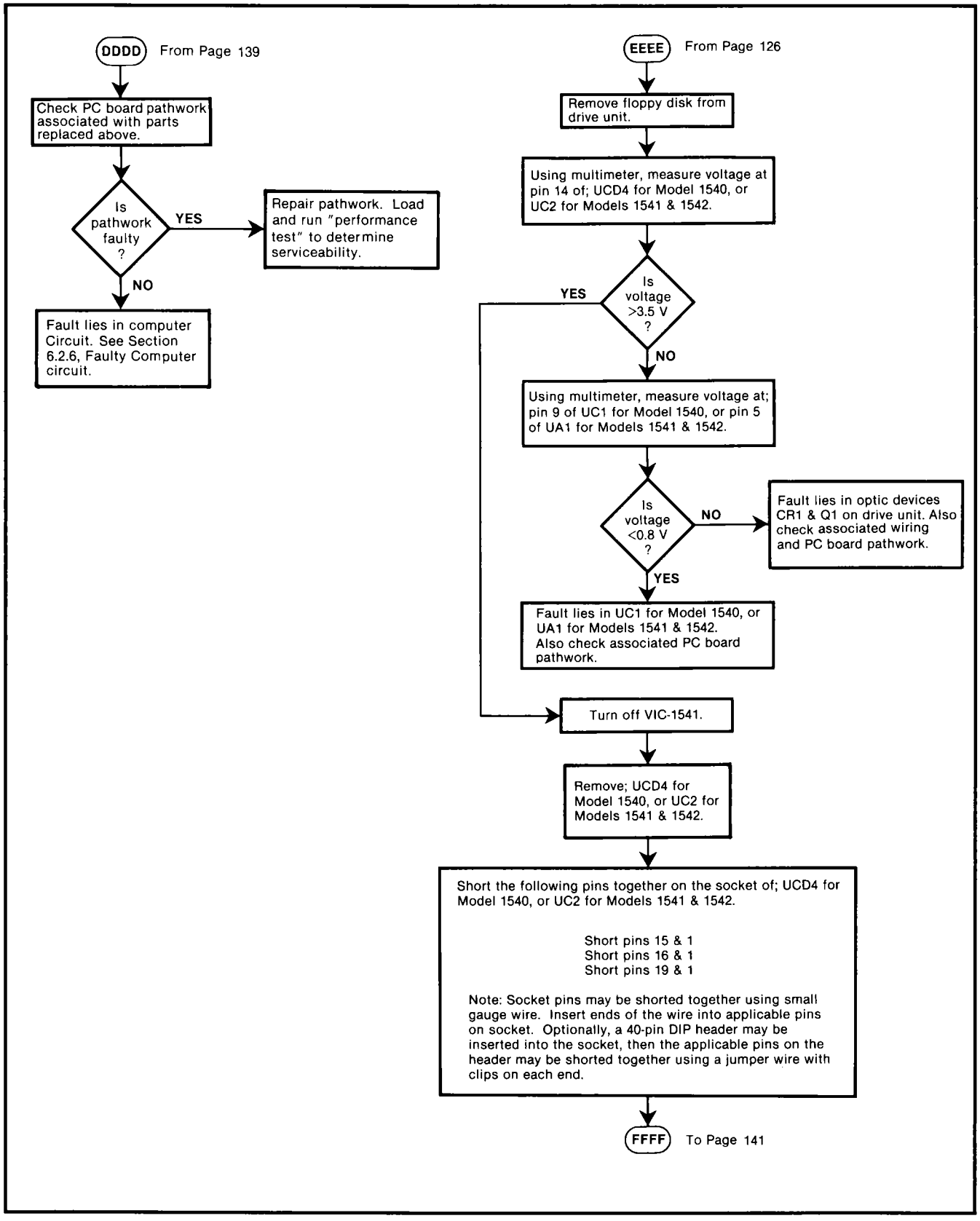
6.2.7 Faulty Read/Write Circuit (cont.)



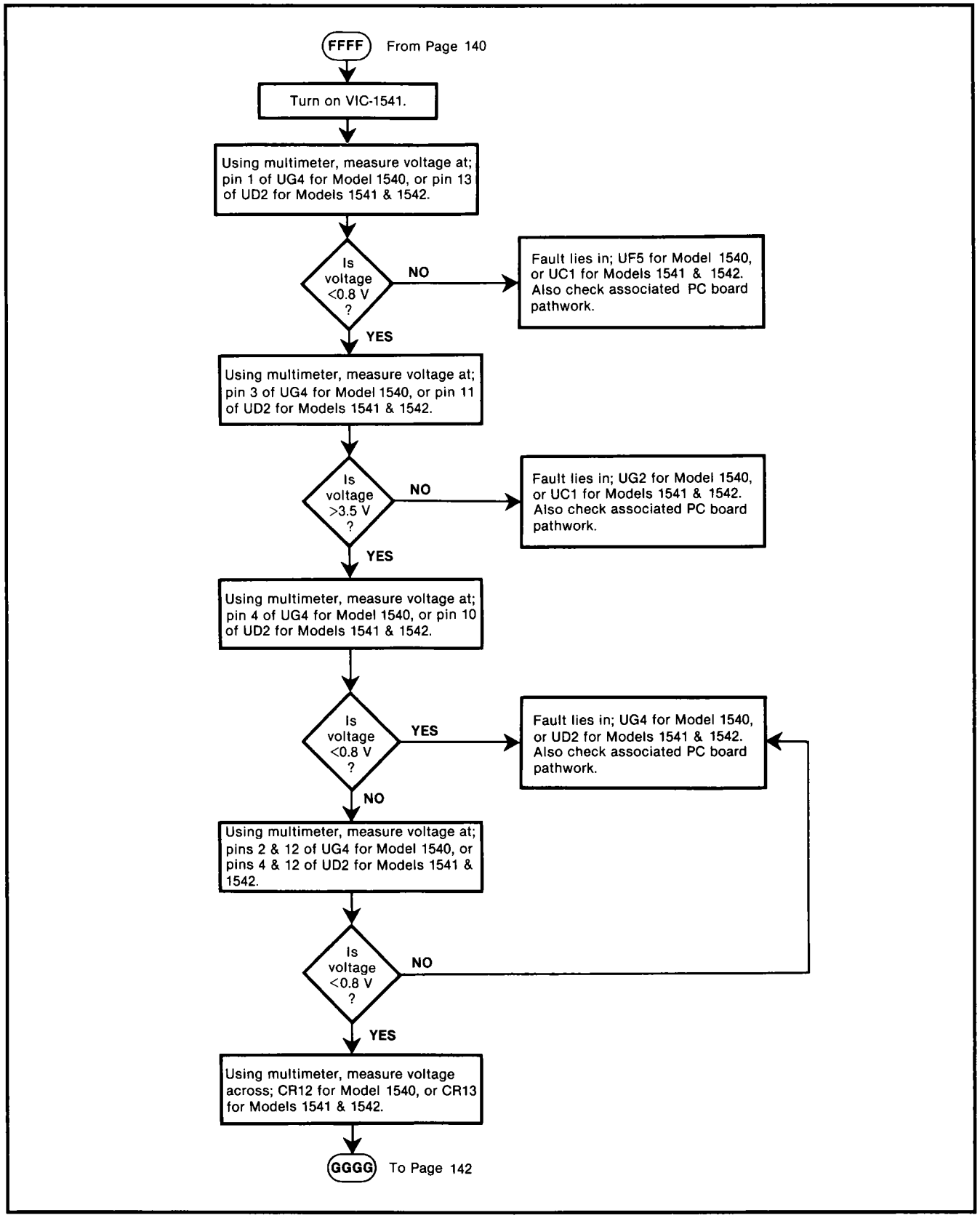
6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)

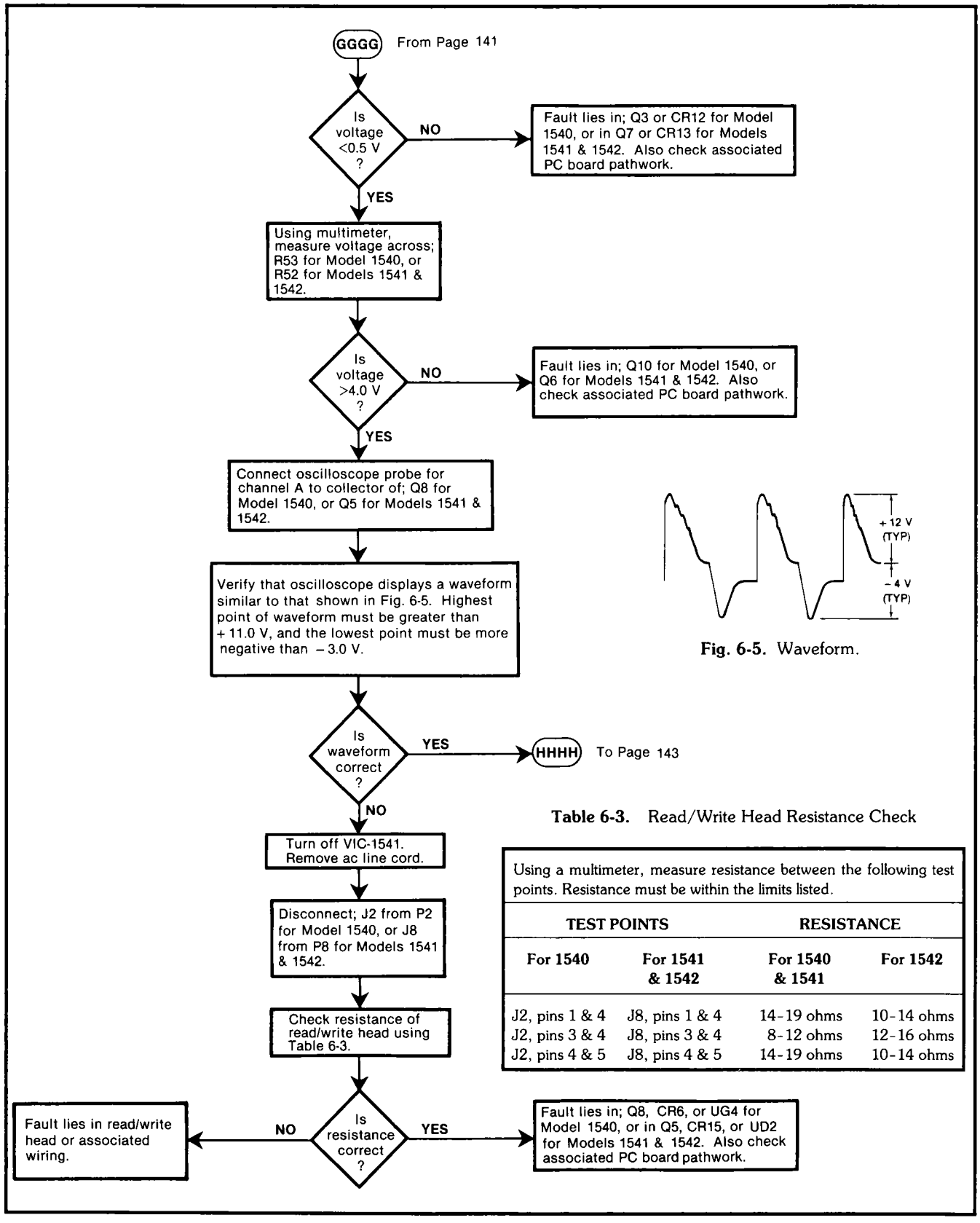


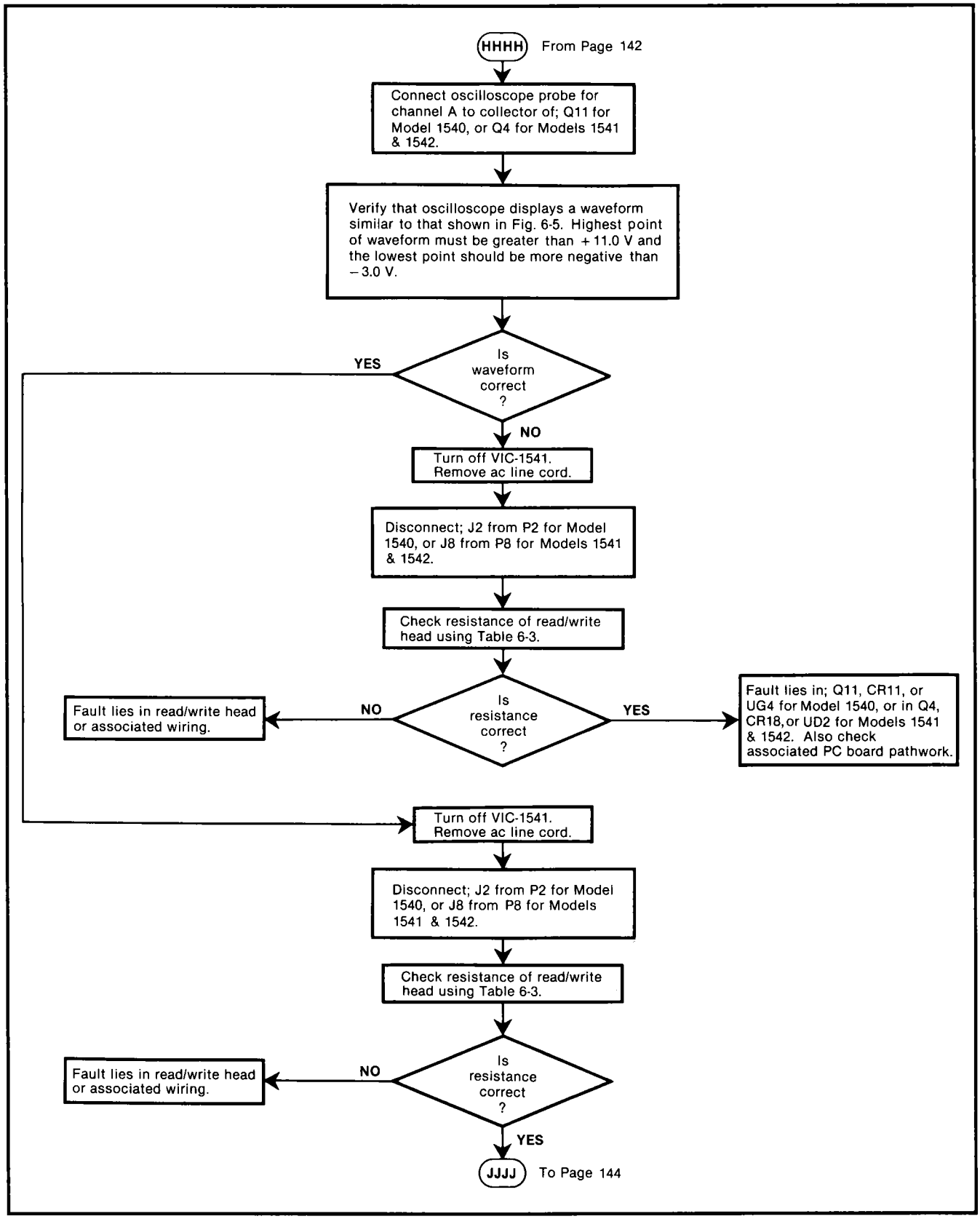
Fig. 6-5. Waveform.

Table 6-3. Read/Write Head Resistance Check

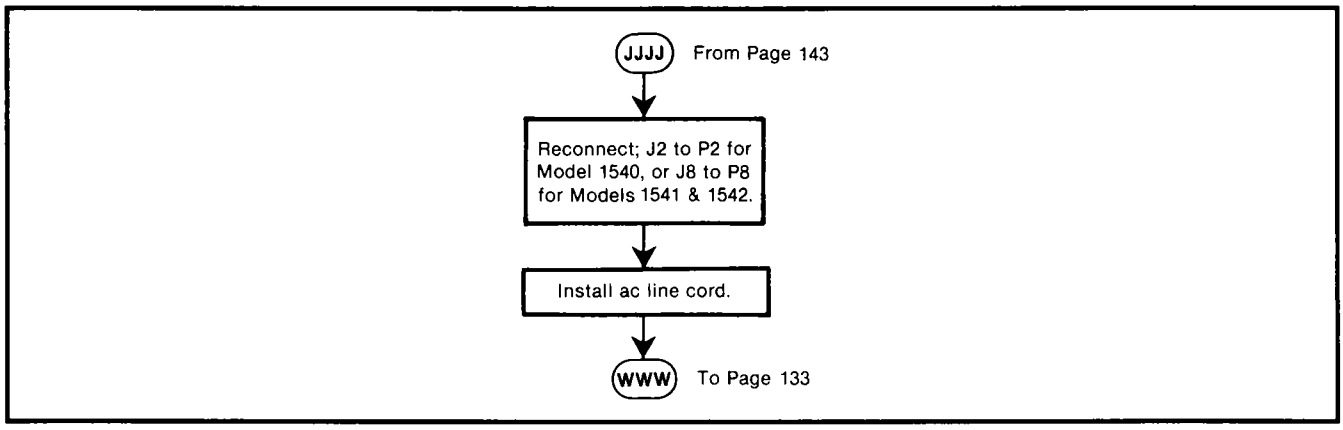
Using a multimeter, measure resistance between the following test points. Resistance must be within the limits listed.

TEST POINTS		RESISTANCE	
For 1540	For 1541 & 1542	For 1540 & 1541	For 1542
J2, pins 1 & 4	J8, pins 1 & 4	14-19 ohms	10-14 ohms
J2, pins 3 & 4	J8, pins 3 & 4	8-12 ohms	12-16 ohms
J2, pins 4 & 5	J8, pins 4 & 5	14-19 ohms	10-14 ohms

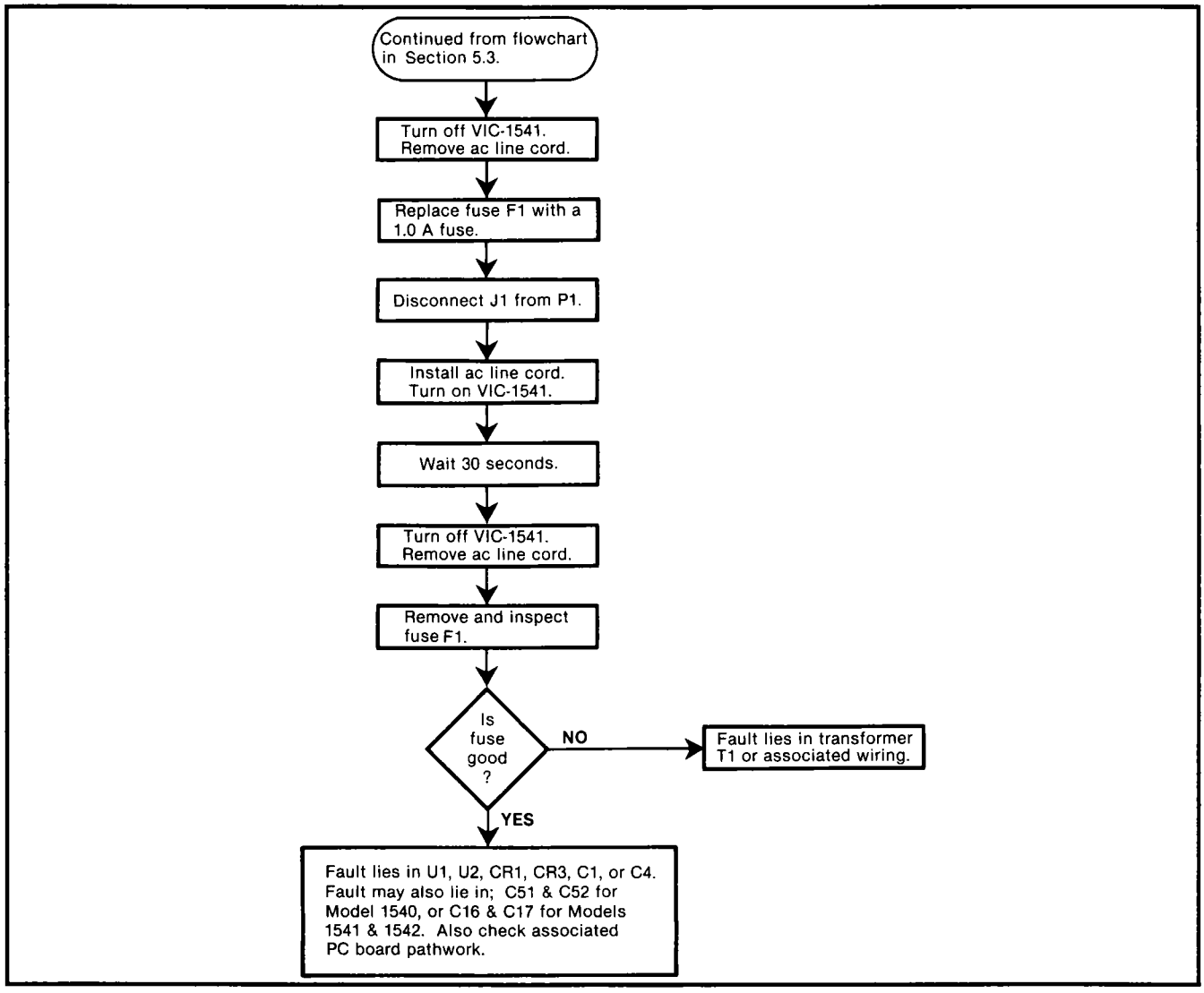
6.2.7 Faulty Read/Write Circuit (cont.)



6.2.7 Faulty Read/Write Circuit (cont.)



6.2.8 Blown Fuses



CHAPTER 7

Advanced Theory of Operation

This chapter provides the fourth level of theory of operation, discussed on the component level using the circuit schematic. Section 7.1 covers Model 1540 and Section 7.2 covers Model 1541. Because Model 1542 is so similar to Model 1541, Section 7.3 only points out the minor differences between Models 1541 and 1542. If you are troubleshooting Model 1542, read Sections 7.2 and 7.3.

7.1 ADVANCED THEORY, MODEL 1540

7.1.1 Frame Electrical Theory (Refer to Figs. 7-1 and 7-2)

The electrical function of the frame assembly is to condition and convert the ac line voltage before applying it to the power supply on the disk controller PC board.

The ac line voltage enters the disk drive at J9, which is both a connector and an RFI filter. After passing through the filter, the ac voltage is applied to the SPST power switch, S1. The output of the power switch is applied to F1, which provides overcurrent protection. F1 is a 1-ampere, 250-volt slow blow fuse. The output of F1 is fed to the transformer, T1. T1 steps down the ac line voltage into 9 volts ac and 16 volts ac. Both of these outputs have their own secondary windings and are isolated from each other.

Fig. 7-1. Block diagram of frame assembly, Model 1540.

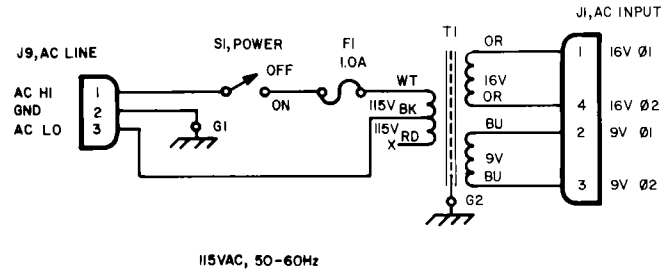


Fig. 7-2. Schematic of frame assembly, Model 1540.

7.1.2 Power Supply Electrical Theory (Refer to Figs. 7-3 and 7-4)

The VIC-1541 power supply produces two regulated voltages, +12 volts dc and +5 volts dc. These voltages are derived, respectively, from the 16 volts ac and 9 volts ac supplied by the frame assembly. The power supply, located on the disk controller PC board, has a reliability switch which removes power from the write amplifiers in the

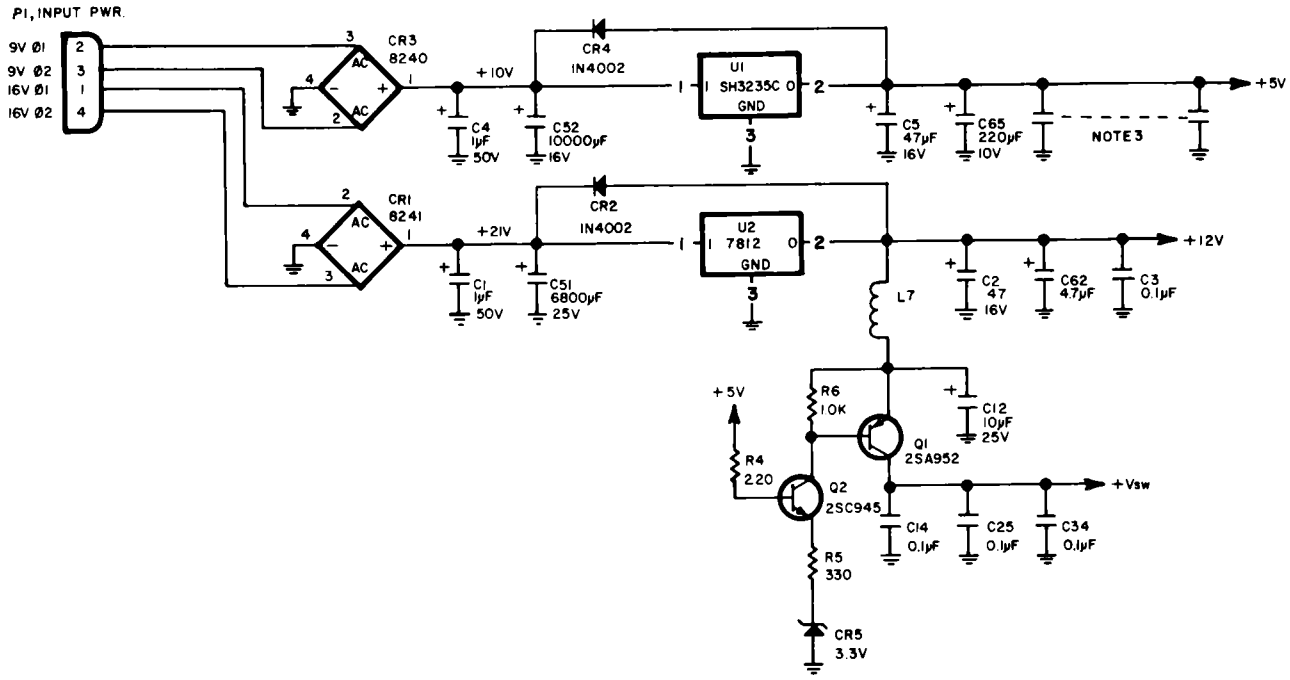


Fig. 7-3. Schematic of power supply, Model 1540.

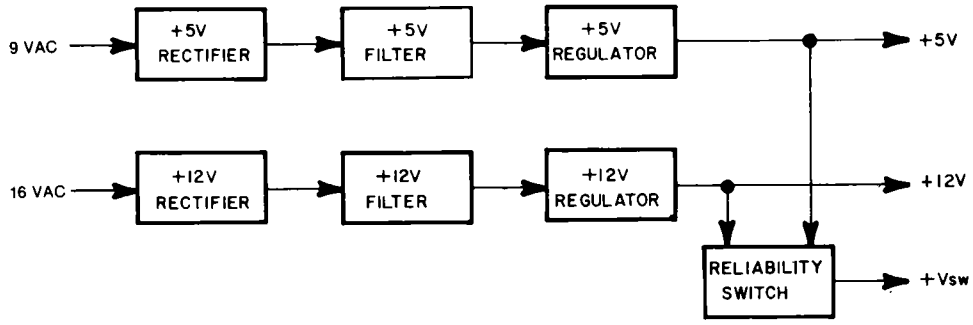


Fig. 7-4. Block diagram of power supply, Model 1540.

event of a +5-volt failure or during power up/down. Thus, the reliability switch protects the data on the floppy disk by disabling the write amplifiers whenever the +5-volt line goes below 3.9 volts.

7.1.2.1 +12 Volts DC

Sixteen volts ac is applied to the power supply via pins 1 and 4 of P1. From P1, the ac power is applied to bridge rectifier CR1. CR1 rectifies (full wave) the 16 volts ac to produce approximately +21 volts dc. The output of the rectifier is applied to a filter consisting of C1 and C51, which smooths out the pulsating dc from CR1. The output of the filter is applied to U2, a +12-volt regulator. The output of U2 is the regulated +12 volts dc output of the power supply. C2, C62, and C3 reduce line noise, and CR2 protects the regulator against negative voltage excursions during power up/down.

7.1.2.2 +5 Volts DC

The +5-volt leg of the power supply operates in the same fashion as the +12-volt leg, the only difference between them is in voltage levels. Nine volts ac is applied to the power supply via pins 2 and 3 of P1. The ac power is applied to bridge rectifier CR3. After rectification, the resulting +10 volts dc is filtered by C4 and C52 before it is applied to the +5-volt regulator, U1. The output of U1 is the regulated +5 volts dc output of the power supply. Both C5 and C65 reduce line noise and CR4 protects the regulator against negative voltage excursions during power up/down.

7.1.2.3 Reliability Switch

The reliability switch consists of Q1, Q2, CR5, and associated components. Q2 and CR5 form a comparator. When the +5-volt line exceeds +3.9

volts, base current of Q2 flows through the base-emitter junction via R4, R5, and CR5. The cutoff voltage is determined by CR5 (3.3 volts) and the base-emitter drop of Q2 (0.6 volt). As the base-emitter current increases, collector-emitter current also increases. When Q2 begins to draw collector current, it forces Q1 into conduction by causing base-emitter current to flow through Q1 via L7, Q2, R5, and CR5. When Q1 is turned on, approximately 11.6 volts is applied to the $+V_{SW}$ line to enable the write amplifiers. If the +5-volt line drops below 3.9 volts, Q2 is turned off, in turn turning off Q1. With Q1 turned off, power is removed from the $+V_{SW}$ line and the write amplifiers are disabled. R6 ensures that Q1 is properly turned off by shunting any Q2 leakage current away from Q1. L7 and C12 form a low-pass L-type filter which isolates the noise produced by the motors in the +12-volt line. C14, C25, and C34 are bypass capacitors which reduce noise in the $+V_{SW}$ line.

7.1.3 Timing Electrical Theory (Refer to Figs. 7-5 and 7-6)

The timing circuit produces the clock signals. One of the outputs is a 1-MHz square wave. This fixed 1-MHz clock signal is applied to the microprocessor, controlling the rate at which the microprocessor executes instructions. The second output is a variable frequency pulse which is used to control the encoder/decoder circuit. The timing circuit consists of a 16-MHz oscillator, a divide-by-16 frequency divider, and a programmable divider.

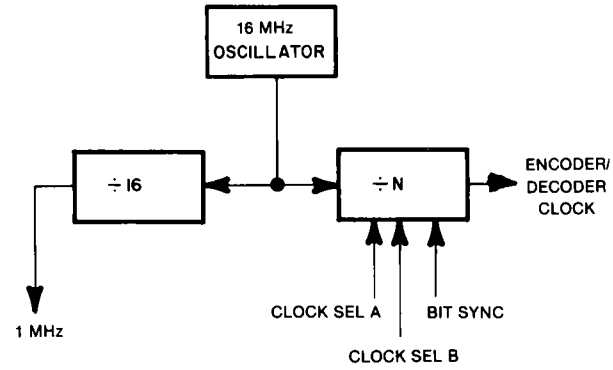


Fig. 7-5. Block diagram of timing circuit, Model 1540.

7.1.3.1 16-MHz Oscillator

The 16-MHz oscillator consists of UC7, Y1, and associated components. Y1, UC7C, UC7D, R1, R2, and C10 form a crystal-controlled square-wave oscillator. UC7B buffers and shapes the clock signal. The output of the 16-MHz oscillator (UC7B, pin 4) is applied to the divide-by-16 frequency divider and to the programmable divider.

7.1.3.2 Divide-by-16 Frequency Divider

The divide-by-16 frequency divider consists of a 4-bit binary counter, UC6. Pin 5 (the divide-by-2 output) of UC6 is applied to pin 6 of UC6 in order to clock the last three stages of the counter. The output of the divide-by-16 frequency divider is taken from pin 12 and is applied to the microprocessor via L3 and R3 which filter the clock line to reduce noise.

7.1.3.3 Programmable Divider

The programmable divider produces the clock for the encoder/decoder circuit and may be reset to allow the phase of the encoder/decoder clock to

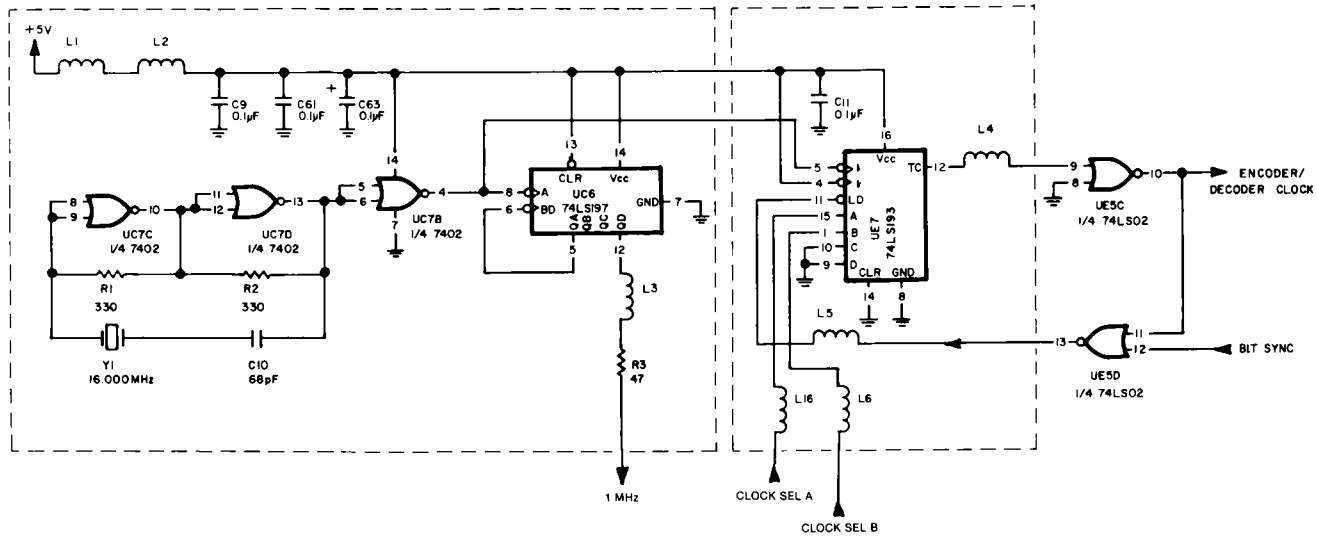


Fig. 7-6. Schematic of timing circuit, Model 1540.

be controlled. Floppy disks have fewer sectors per track on the innermost track (track No. 35) than on the outermost track (track No. 1). This variation in number of sectors per track keeps the bit density fairly constant throughout the writing surface of the disk. Each disk is further divided into four zones, with each zone containing a unique number of sectors per track. The programmable divider has four possible output frequencies, with each frequency corresponding to one of the four zones on the floppy disk. In order to maintain fairly even bit densities, the encoder/decoder must be clocked at a faster rate when writing on the outer tracks than when writing on the inner tracks. This is because the outer surface of the disk is passing over the head more quickly than the inner surface. Thus, it is the encoder/decoder clock that determines how many sectors will fit on any given track.

The division factor of the programmable divider is controlled by the CLOCK SEL A and CLOCK SEL B lines. Table 7-1 defines parameters for each zone. The programmable divider consists of UE7, UE5C, and UE5D. UE7 is configured as a presettable 4-bit binary up counter. The output of UE7 is taken off pin 12, the TC output. The TC output (active low terminal count) goes low when the counter overflows from $1111_{(2)}$ to $0000_{(2)}$. This active low pulse is inverted by UE5C, producing a positive pulse. The output of UE5C is applied to UE5D and to the encoder/decoder circuit. The output of UE5D is an active low pulse that is applied to the load input of the presettable counter. When the load input goes low, the counter is preset to the values present on the A, B, C, and D lines. The C and D lines are strapped low and therefore each line is set to 0. If the A and B lines are both low (zone 4 condition), the counter is preset to $0000_{(2)}$. Sixteen counts later the load line will reset the counter to $0000_{(2)}$. If the A line only is a logic 1 (zone 3 condition), the counter is preset to $0001_{(2)}$ and 15 counts later the load line will again preset the counter to $0001_{(2)}$. Note that only 15 counts were required, since the counter had a head start of one count. If the B line only is a logic 1 (zone 2 condition), the counter is preset to $0010_{(2)}$. The counter now has a head start of two counts and will require only 14 counts before it is preset again. If both the A and B lines are at logic 1 (zone 1 condition), the counter is preset to $0011_{(2)}$. The counter now has a head start of three counts and will require only 13 counts before it is preset again.

Table 7-1. Timing Circuit Parameters

	ZONE 1	ZONE 2	ZONE 3	ZONE 4
CLOCK SEL A	1	0	1	0
CLOCK SEL B	1	1	0	0
Division Factor	13	14	15	16
Encoder/Decoder Clock Freq (MHz)	1.2307	1.1428	1.0666	1.00
Sectors per Track	21	20	18	17
Track Numbers	1-17	18-24	25-30	31-35

L16 and L4 through L6 filter the signal lines to reduce noise. L1, L2, C9, C61, C63, and C11 form a low-pass L-type filter which prevents the coupling of noise from the timing circuit to the +5-volt line and vice versa.

Pin 12 of UE5D is the BIT SYNC input. When a positive pulse is applied to pin 12, the output of UE5D (pin 13) is applied to the load line, causing the encoder/decoder clock to terminate the current cycle early and begin a new one. A pulse from the read circuit is applied to the BIT SYNC input every time a high-to-low or a low-to-high transition occurs in the serial data on the disk. When this pulse occurs, the encoder/decoder clock is set to the beginning of its cycle and the clock is synchronized with the serial data. The timing circuit maintains the phase relationship between the serial data and the encoder/decoder clock to within 62 nanoseconds.

7.1.4 Computer Electrical Theory (Refer to Figs. 7-7 and 7-8)

The computer performs two major functions—serial bus communication and floppy disk control. Communication with the serial bus is accomplished by the serial bus interface. Interfacing with the floppy disk is accomplished by the read, write, track select, motor drive, timing, and optics circuits, along with the drive unit itself. The computer communicates with these devices through the versatile interface adapter (VIA). The computer consists of the MPU, ROM, RAM, write logic, address decoder, VIA, and the serial bus interface.

7.1.4.1 MPU

UCD5 is a 6502, 8-bit microprocessor. The microprocessor fetches an instruction from ROM or RAM and executes the instruction. The instruction, in turn, causes the microprocessor to alter data in RAM, internal registers, or registers in the VIAs. After completing each instruction, the MPU fetches the next instruction and the cycle continues. The

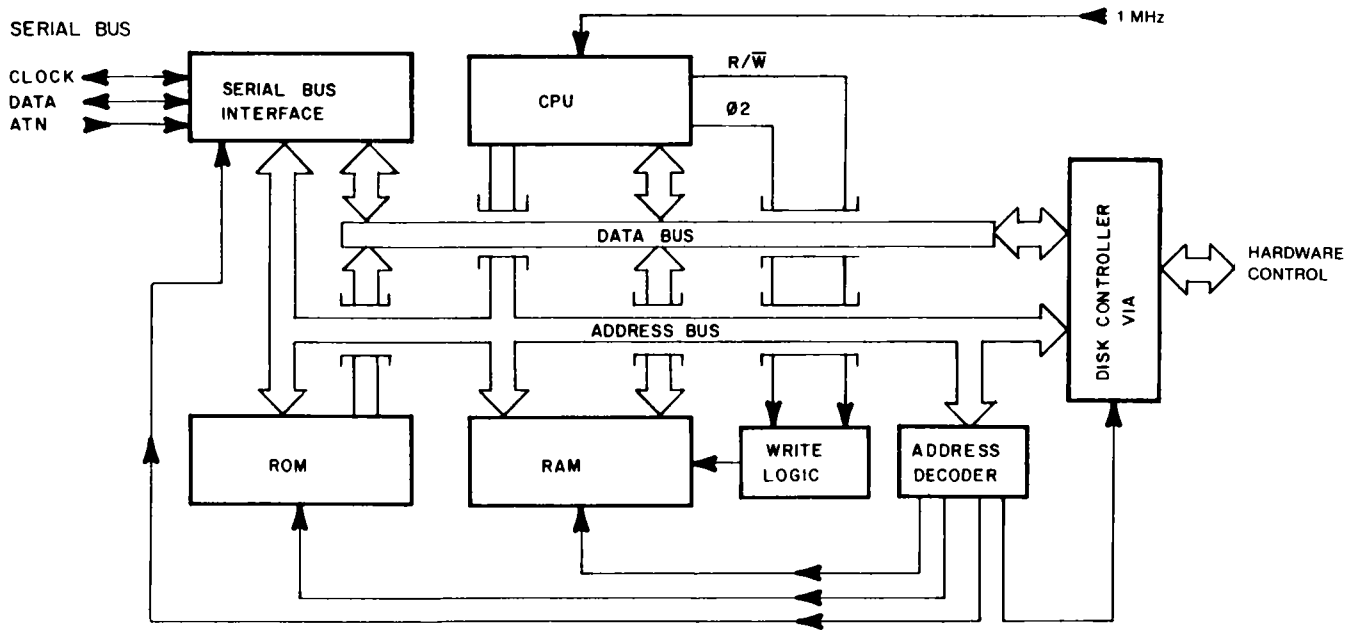


Fig. 7-7. Block diagram of computer circuit, Model 1540.

rate at which the microprocessor executes instructions is determined by the $\phi 1$ clock present at pin 37 of UCD5. The $\phi 1$ clock is produced by the timing circuits (refer to Section 7.1.3, "Timing Electrical Theory"). The microprocessor in turn produces an inverted, nonoverlapping clock signal (i.e., $\phi 2$) from the $\phi 1$ clock. The $\phi 2$ signal is present at pin 39 of UCD5. Two NOT gates, UB6A and UB6B, buffer the $\phi 2$ clock before it is sent to the VIAs (UCD4 and UAB1) and to the write logic. The $\phi 2$ signal is used to synchronize write operations; therefore, the ROM does not require the $\phi 2$ signal.

The nonmaskable interrupt (NMI, UCD5, pin 6) is disabled by R23 and is not used. The ready line (RDY, UCD5, pin 2) is held at a logic high by R22 and also is not used.

There are three lines entering the microprocessor that allow hardware devices in the VIC-1541 to change the sequence of instructions executed by UCD5. These lines are: set overflow (SO, pin 38), interrupt request (IRQ, pin 4), and reset (RST, pin 40). When the set overflow line goes high, it sets the overflow bit in the status register internal to UCD5. The sequence of instructions may be changed by testing the overflow flag using the BVC (branch if overflow clear) or BVS (branch if overflow set) instructions.

When the interrupt request line goes low, the microprocessor calls the subroutine whose starting address is stored at locations $FFFE_{(hex)}$ (low byte) and $FFFF_{(hex)}$ (high byte). $FFFE_{(hex)}$ contains $FE_{(hex)}$ and $FFFF_{(hex)}$ contains $67_{(hex)}$. These two bytes form the 16-bit address $FE67_{(hex)}$, which is the starting address of the interrupt routine. The IRQ line may be defeated or "masked" under software control.

When the RST line is pulled low, the microprocessor executes the instructions whose starting address is located at $FFFD_{(hex)}$ (high byte) and $FFFC_{(hex)}$ (low byte). The address stored in these two locations is $EAA0_{(hex)}$, which is the address of the first instruction of the reset routine. The reset routine initializes the VIC-1541.

7.1.4.2 ROM

UAB4 and UAB5 are 8K × 8 ROMs which together form a 16K ROM. The ROMs contain instructions which make up a machine language program called the DOS (disk operating system). The ROMs are located between addresses $C000_{(hex)}$ and $FFFF_{(hex)}$. Data is applied to the data bus (D0 through D7) from the ROM when the CE line (pin 20) goes low. The address inputs (A0 through A12) determine which one of the 8192 bytes in the ROM will be applied to the data bus. While the CE line is high, the data outputs are tristated and essentially disconnected from the data bus.

7.1.4.3 RAM

The RAM consists of four 1K × 4 RAM chips; UB3, UA3, UB2, and UA2. Together they form a 2K-byte RAM. The RAM is located between addresses 0 ($0000_{(hex)}$) and 2047 ($07FF_{(hex)}$). Significant locations in ROM are:

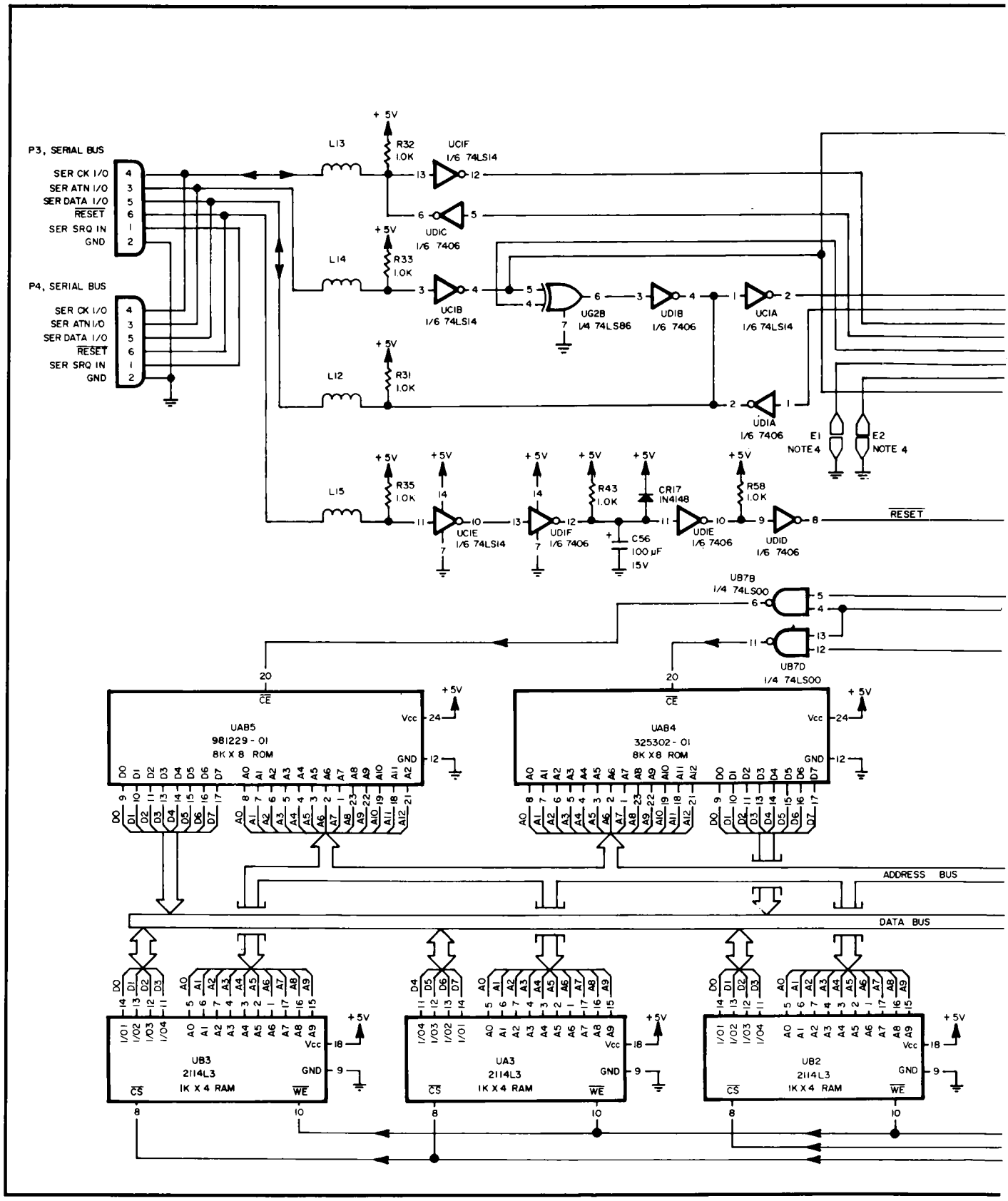
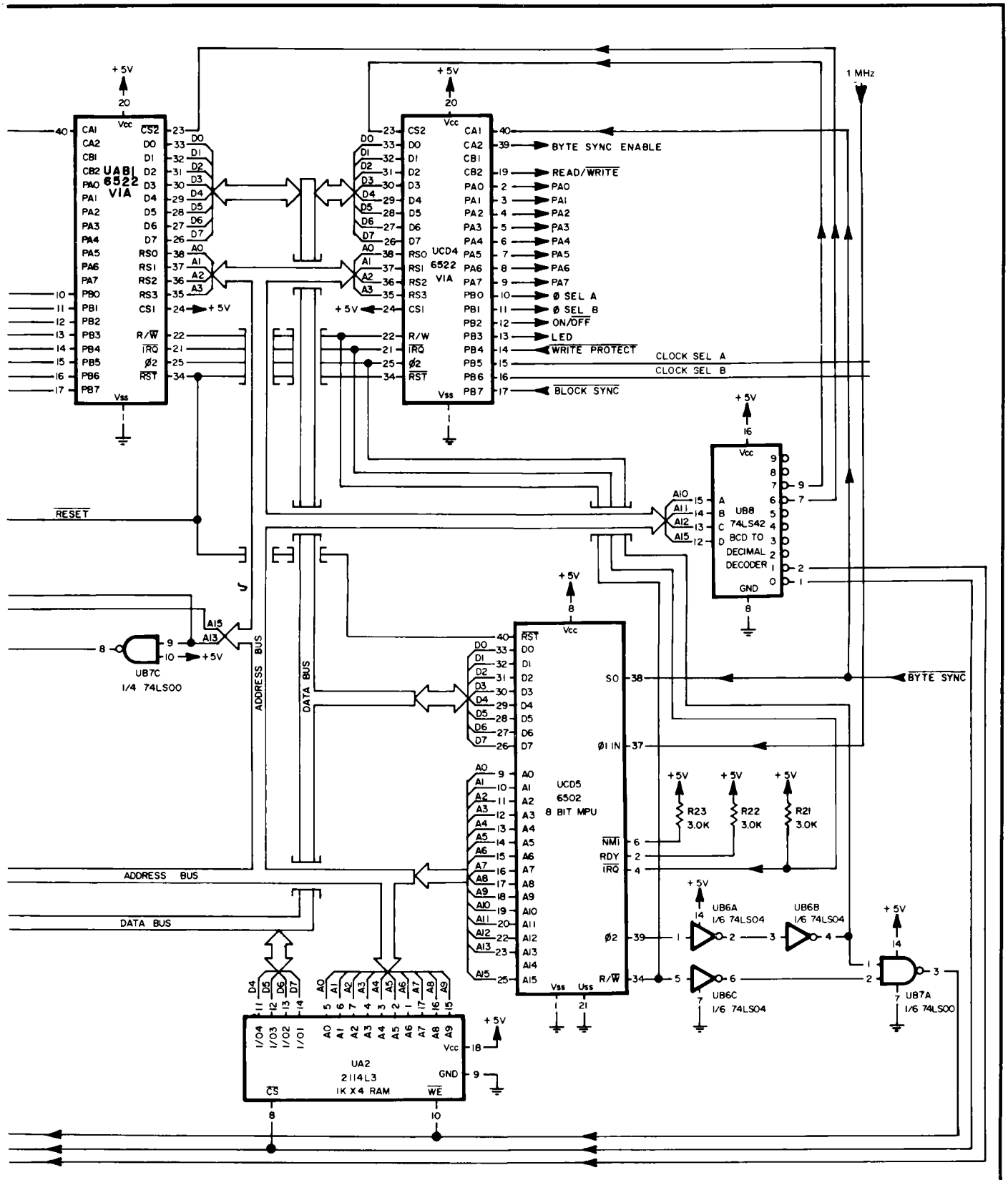


Fig. 7-8. Schematic of computer



circuit, Model 1540.

0000-00FF	Zero Page
0100-01FF	Microprocessor Stack

The zero page contains variables, pointers, and other data used by the DOS. The microprocessor stack is used for temporary storage of data.

When the MPU writes to the RAM, the data to be written is placed on the data bus (D0 through D7), the location that the data is to be written into is placed on the address bus (A0 through A15), and the WE (write enable) and CS (chip select) lines are brought low. When the MPU reads from the RAM, the location to be read is placed on the address bus (A0 through A15) and the CS line is brought low. Data is then gated from the RAM to the data bus (D0 through D7).

7.1.4.4 Address Decoder

The address decoder selects one of the devices listed in Table 7-2 when the address bus contains an address within the address range of the device. UB7B, UB7C, and UB7D decode the ROM low and ROM high addresses. UB7C is configured as a NOT gate, which inverts A13 before it is applied to UB7D. UB7D enables UAB4, the low ROM, when A15 = logic 1 and A13 = logic 1. UB7B enables UAB5, the high ROM, when A15 = logic 1 and A13 = logic 1. A0 through A12 are decoded by the selected high or low ROM. Notice that A14 is not decoded, and it therefore does not affect the operation of the decoder. The end result is two identical 16K blocks of ROM. Each of the ROM chips has two valid address ranges. One range is used with A14 = logic 1 as in Table 7-3.

Table 7-2. Address Decoder Parameters

DEVICE	ADDRESS RANGE (HEX)
RAM, Low (UB2 & UA2)	0000-03FF
RAM, High (UB3 & UA3)	0400-07FF
VIA, Serial Bus (UAB1)	1800-180F
VIA, Disk Control (UCD4)	1C00-1C0F
ROM, Low (UAB4)	C000-DFFF
ROM, High (UAB5)	E000-FFFF

Table 7-3. ROM Images

	A14 = LOGIC 0	A14 = LOGIC 1
ROM, Low (UAB4)	8000-9FFF	C000-DFFF
ROM, High (UAB5)	A000-BFFF	E000-FFFF

Data that is read from address $8000_{(hex)}$ is identical to the data read from address $C000_{(hex)}$. This must be so because both address the same location in the same ROM. The redundant 16K block between $8000_{(hex)}$ and $BFFF_{(hex)}$ is not normally used. It is just a by-product of the address decoder scheme. Notice that the read/write signals are not decoded for ROM addresses. The VIC-1541 hardware does not prevent a bus conflict between the microprocessor and the ROMs. The hardware design merely assumes any memory transfer at or above $8000_{(hex)}$ is a read operation.

> **CAUTION**
>
> Never write to memory locations at or above $8000_{(hex)}$. A bus conflict may occur, causing permanent damage to UAB4, UAB5, or UCD5.

UB8, a BCD-to-decimal decoder, decodes the RAM and VIA address ranges. Address lines A10, A11, and A12 are connected to the A, B, and C inputs, respectively, of UB8. As a result, the outputs of UB8 decode one of eight 1024-byte blocks. Address line A15 is applied to the D input of UB8. When the D input is a logic 0, one of the 0 through 7 outputs will be active (i.e., logic 0). When the D input is a logic 1, outputs 0 through 7 will be inactive, effectively disabling UB8. Any address at or below $7FFF_{(hex)}$ will enable UB8. Any address at or above $8000_{(hex)}$ will enable the ROM array.

As noted previously, UB8 can decode one of eight 1024-byte blocks of memory. Notice that UB8 does not decode A13 or A14. As in the ROM address decoder, this produces redundant images of the 8K block decoded by UB8. Since two bits are not decoded, UB8 produces four identical 8K blocks of memory as opposed to the two identical blocks produced by the ROM address decoder. The address ranges for each 8K block are as follows: $0000\text{-}1FFF_{(hex)}$, $2000\text{-}3FFF_{(hex)}$, $4000\text{-}5FFF_{(hex)}$, and $6000\text{-}7FFF_{(hex)}$. Writing to location $0000_{(hex)}$ produces the same result as writing to locations $2000_{(hex)}$, $4000_{(hex)}$, or $6000_{(hex)}$. The redundant ranges of $2000\text{-}3FFF_{(hex)}$, $4000\text{-}5FFF_{(hex)}$, and $6000\text{-}7FFF_{(hex)}$ are not normally used.

The 0 output of UB8 is used to enable the low RAM pair (UB2 and UA2), while the 1 out-

put is used to select the high RAM pair. Table 7-4 illustrates the RAM address range. The 2 through 5 outputs of UB8 are not used. With four images being produced, this leaves the following locations not addressing any devices: 0800-17FF$_{(hex)}$, 2800-37FF$_{(hex)}$, 4800-57FF$_{(hex)}$, and 6800- 77FF$_{(hex)}$.

Table 7-4. RAM Images

	A13 = 0, A14 = 0	A13 = 1, A14 = 0	A13 = 0, A14 = 1	A13 = 1, A14 = 1
RAM, Low	0000-03FF	2000-23FF	4000-43FF	6000-63FF
RAM, High	0400-07FF	2400-27FF	4400-47FF	6400-64FF

The 6 output of UB8 enables the serial bus VIA, UAB1. Notice that UAB1 decodes A0 through A3. A4 through A9 are not decoded, again producing redundant images. There are 64 images of the 16 VIA registers in the 1024-byte block enabled by UB8. There are also four images of each 1024-byte block that is selected. This gives a total of 256 images of the VIA registers. Typically, the serial bus registers are accessed at 1800-180F$_{(hex)}$ by the DOS.

The 7 output of UB8 is used to enable the disk controller VIA, UCD4. Again, this VIA has a total of 256 redundant images. Typically, the disk controller VIA is accessed at 1C00-1C0F$_{(hex)}$ by the DOS.

7.1.4.5 Write Logic

UB6C and UB7A form the write logic circuit. UB6C inverts the R/W (read/write) line from pin 34 of UCD5. The output of UB6C will be high during a write cycle and will be applied to the NAND gate UB7A together with the $\phi 2$ signal from UB6B. The output of UB7A drives the WE (write enable) lines on the RAM chips UB2, UB3, UA2, and UA3. The write logic for the VIAs is internal to the VIAs. Therefore, the R/W line and the $\phi 2$ signal are applied directly to the VIA chips.

7.1.4.6 Serial Bus

The serial bus circuits consist of UAB1, UG2B, UD1, UC1A, UC1B, UC1E, UC1F, and associated components. The serial bus circuits interface the computer with the serial bus and allow the VIC-1541 to communicate with the VIC 20/Commodore 64. The serial bus circuits also control the reset line for the VIC-1541 computer.

When power is first applied to the VIC-1541, C56 is in a discharged state, producing a logic 0 at the input of UD1E. This makes the output of UD1E a logic 1, which is applied to pin 9 of UD1D. The resulting logic 0 out of UD1D drives the reset line for UAB1, UCD4, and UCD5, causing them to assume their initialized states. After a short period of time, C56 will be charged through R43, up to the logic threshold of UD1E. This causes the output of UD1E to change states. In turn, UD1D changes states and places the reset line high, allowing the computer to start execution of the DOS. If the VIC 20/Commodore 64 is reset, the reset line on the serial bus (pin 6 of P3 and P4) will go low (logic 0). This logic 0 is inverted by UC1E and applied as a logic 1 to the input of UD1F, which discharges C56 to a logic 0. Subsequent action of the reset circuit is as described earlier. CR17 is provided to discharge C56 if power is momentarily removed from the VIC-1541. The reset circuits are active only during power-up of the VIC-1541 or the VIC 20/Commodore 64.

The VIC-1541 serial bus is similar to the IEEE-488 bus (also known as GPIB or HPIB), but it is slower and does not use some of the control signals. Like the IEEE-488 bus, the VIC-1541 bus may be interfaced with several peripherals, each having a unique address. All the peripherals are daisy-chained together. Daisy-chaining means the first peripheral is connected to the computer, the second peripheral is connected to the first, the third peripheral is connected to the second, and so on. Daisy-chaining is the reason the two serial bus connectors, P3 and P4, are wired in parallel. The users of the bus (e.g., VIC 20/Commodore 64, VIC-1541, printers) can be divided into three groups according to their activities at any given instant: controller, talker, and listener.

Only the VIC 20/Commodore 64 may be a controller, talker, and a listener. The peripherals may either be talkers or listeners. The controller dictates bus commands to the peripherals which tell the addressed device whether to talk, listen, untalk, or unlisten. These bus commands are:

Talk—Addresses a specific device and instructs the device to prepare to send data.

Untalk—Addressed device is instructed to cease transmissions.

Listen—Addressed device is instructed to prepare to receive data.

Unlisten—Addressed device is instructed to

ignore any further data transmissions. Device will wait for next command.

These bus commands are sent as an 8-bit byte. Five of the bits are used for the address and the others are used for the command definition. A total of 28 devices may be addressed by the serial bus. However, even though the address range of the serial bus is 4 through 31, it can only drive five loads at any given time.

> **CAUTION**
>
> Connecting more than five devices to the serial bus could result in permanent damage to the serial bus circuits.

Applicable bus signals used by the VIC-1541 are:

SER CK—Primarily used to indicate that data is valid on the serial data line. Also used as a ready-to-send signal.

SER DATA—Primarily used to carry data bits. Also used as cleared to send, EOI acknowledge, and handshaking signal.

SER ATN—When false, serial data contains data to be transferred. When active, it indicates that the data bus contains a command. Only the controller may drive this line.

All of these signals are active low signals. The signal lines are driven by open collector outputs, allowing all the peripherals to be write-ORable. That is, any or all of the devices may drive the bus lines at the same time. If any device pulls a bus line active (low), the result will be an active line. In order for a line to be inactive (high), all peripherals must release the line to high.

Refer to Fig. 7-9 for a typical data transmission signal. Prior to T0, the bus is in its standby state, the serial clock line is held low by the talker, and the data line is held low by the listener. The SER ATN line is high, indicating the transmission to take place is data rather than a command. At T0, the talker signals "ready to send" by releasing the clock line. At T1, the listener acknowledges the "ready to send" by signaling "clear to send." The listener signals "clear to send" by releasing the clock line to a logic high. If the listener is busy, it will not signal "clear to send." The time between T0 and T1 is undefined and is determined by the listener. Within 200 microseconds, the talker pulls the clock line low at T2. At some time between T2 and T3, the talker places the least significant bit on the SER DATA line. Since the bus lines are active low, the data appears inverted. That is, a low represents a "true" bit. At T3, the clock line is released to logic 1, indicating to the listener that the data bit on the SER DATA line is valid. The talker holds this condition until T4, where the talker releases the data line to a logic 1 and pulls the clock line low. This sequence continues until T18. After clocking in the most significant bit at T17, the talker once again pulls the clock line low and releases the data line at T18. Now the talker is waiting for the handshake signal which occurs at T19. At T19, the listener pulls the data line low. After T19, the serial bus is back in its standby condition, as it was prior to T0. Throughout the transmission of this byte, the talker keeps control of the clock line. The talker has

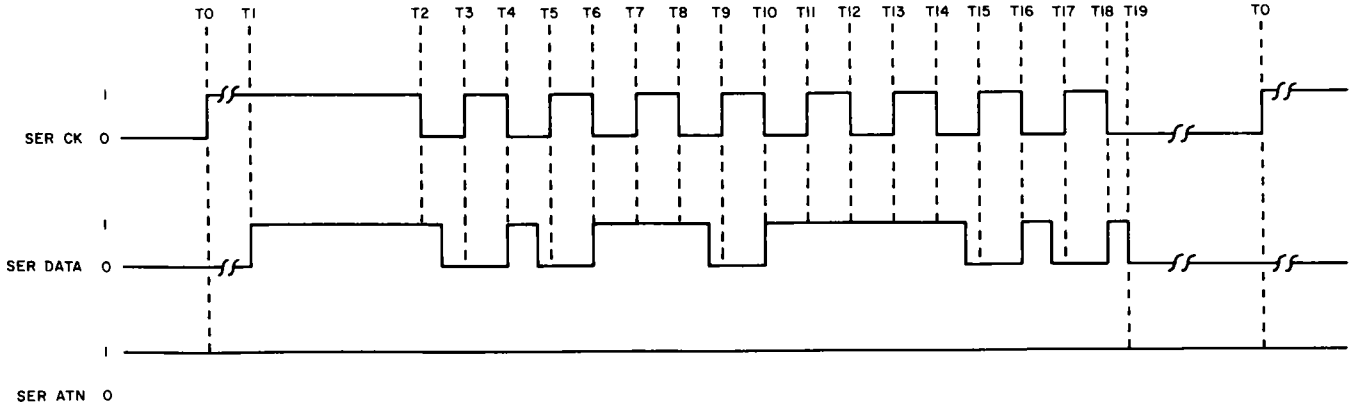


Fig. 7-9. Typical data transmission.

control of the data bus from T2 to T18 only. The rest of the time the listener uses the data line for handshaking. Data transfers continue in this fashion until the last byte to be transferred. The last byte to be transferred contains "end or identify" handshaking.

The handshaking signal for "end or identify" takes place between T1 and T2 (refer to Fig. 7-10 for "end or identify" information). The talker signals "end or identify" by not pulling the clock line low for at least 200 microseconds. After approximately 200 microseconds, the listener acknowledges the "end or identify" at T1A by pulling the serial data line low. At T1B, the listener releases the SER DATA line to logic 1, informing the talker to transmit the last byte. At T2, the talker pulls the clock line low and the byte is transmitted. At some time after T19, the talker and the listener release the clock and data lines, respectively. These actions occur at T20.

A bus command is transmitted in the same manner as bus data, except that the SER ATN line is pulled low during the transmission. When a bus command is being transferred, the VIC 20/Commodore 64 is the bus controller and all the peripherals on the line become listeners. After the bus command, a secondary address may also appear. The secondary address is optional and is used to control and specify a subchannel. After the bus command is issued, the addressed device assumes the role issued by the bus command. Usually, the VIC 20/Commodore 64 assumes the opposite role. For example, if a talk command is issued, the computer assumes the role of the listener. All the devices in the bus that are not involved with the transfer of data release control of the bus lines and await the next command (i.e., SER ATN pulled low). It is possible for the controller to issue a listen command to one peripheral and a talk command to another peripheral, causing data to be transferred between two peripherals while the VIC 20/Commodore 64 is free to perform other tasks. Such a possibility is difficult to accomplish, but the VIC-1541 bus is capable of doing so.

UC1F is the line receiver for the serial clock line. The output of UC1F is entered into the serial bus VIA, UAB1. When the VIC-1541 is a talker, it takes control of the serial clock line using port B, bit 3 (pin 13, UAB1) of the serial bus VIA. When pin 13 of UAB1 goes high, UD1C pulls the clock line active. UD1 has open collector outputs.

UC1A is the line receiver for the SER DATA line. The data is inverted and applied to the serial bus VIA. The SER DATA line is driven in the write mode by UD1A. The serial-to-parallel and parallel-to-serial conversions are performed by the software.

UC1B is the line receiver for the SER ATN line. The output of UC1B is applied to pin 40 of UAB1, generating an interrupt to the computer. The output is also applied to pin 17 to allow the computer to sample the state of the SER ATN line. When the SER ATN line is active, the SER DATA line is pulled low by UG2B and UD1B. The VIC-1541 releases the data line by using the other input (pin 4) of the Exclusive OR gate, UG2B.

E1 and E2 set the address of the VIC-1541. Refer to Chapter 1 for instructions on configuring E1 and E2.

UAB1 is a versatile interface adapter (VIA) containing two parallel ports, interrupt logic, and two 16-bit counters, all of which are accessible to the computer through the data bus.

7.1.4.7 Disk Controller VIA

UCD4, the disk controller VIA, has two 8-bit ports which are used to interface with the timing,

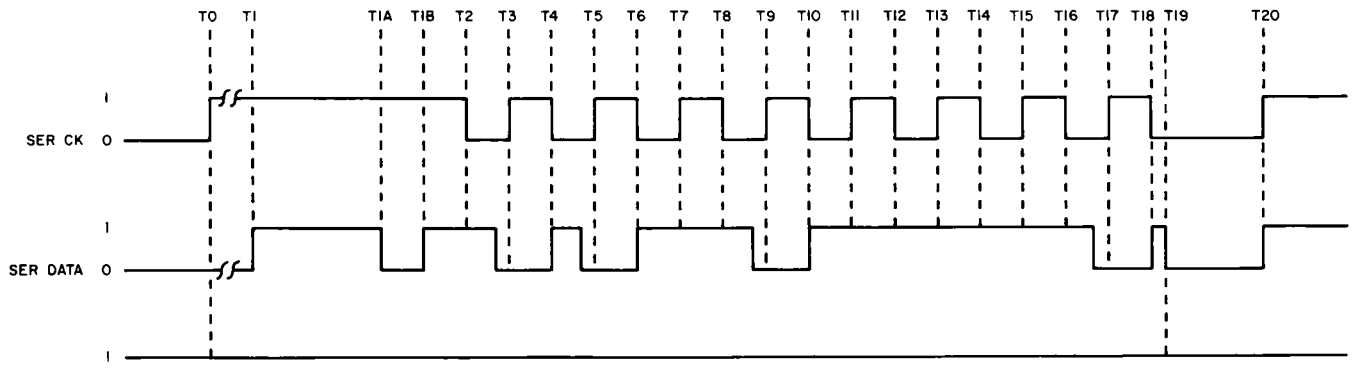


Fig. 7-10. End or identify.

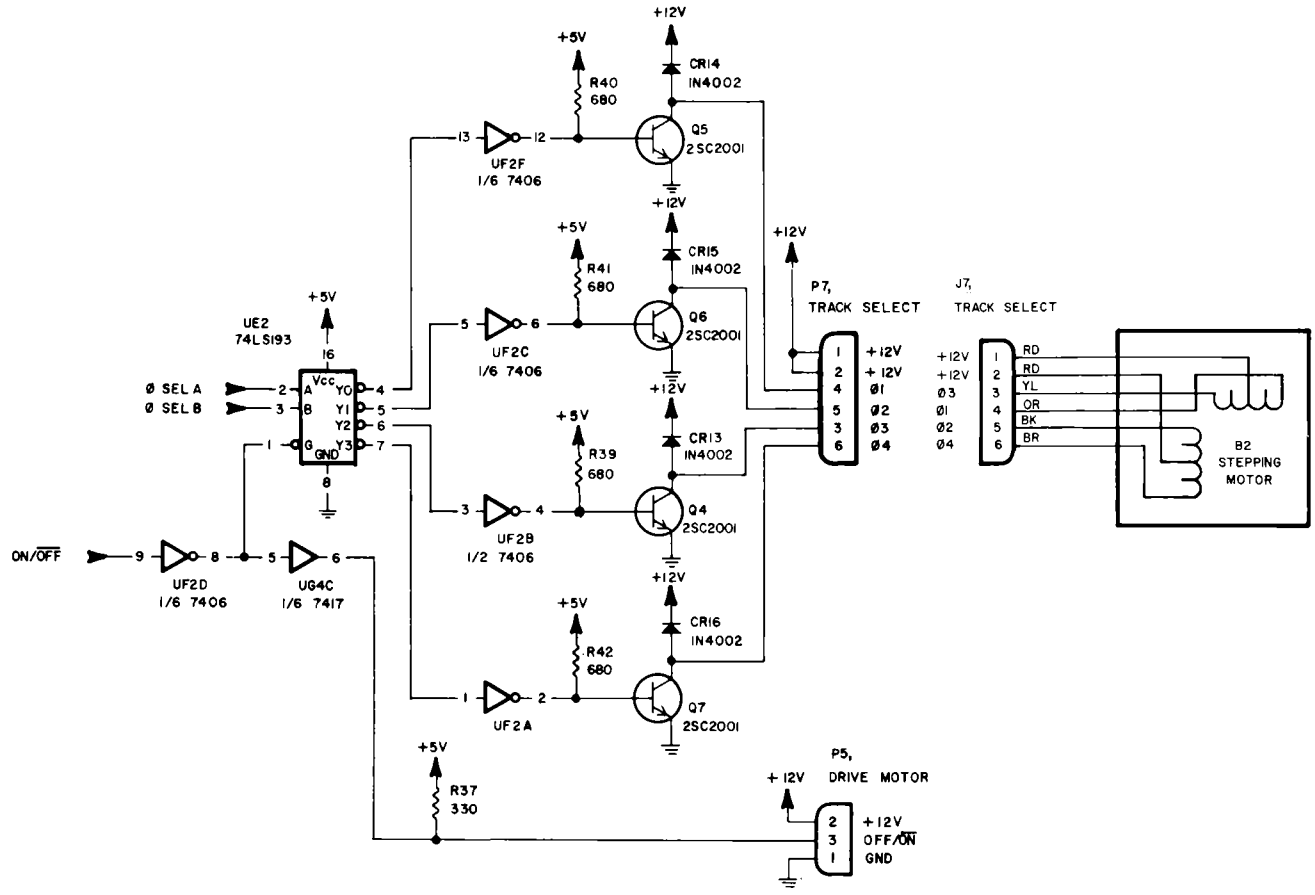


Fig. 7-11. Schematic of track select circuit, Model 1540.

Table 7-5. Track Select Truth Table

ON/OFF	ϕ SEL A	ϕ SEL B	ϕ1	ϕ2	ϕ3	ϕ4	OFF/ON
0 V	X	X	+12 V	+12 V	+12 V	+12 V	+5 V
+5 V	0 V	0 V	0 V	+12 V	+12 V	+12 V	0 V
+5 V	+5 V	0 V	+12 V		+12 V	+12 V	0 V
+5 V	0 V	+5 V	+12 V	+12 V	0 V	+12 V	0 V
+5 V	+5 V	+12 V	+12 V	+12 V	0 V	0 V	

read, write, encoder/decoder, track select, and optics circuits. UCD4 also contains interrupt logic and two 16-bit counters that may be accessed by the computer.

7.1.5 Track Select Electrical Theory (Refer to Figs. 7-11 and 7-12)

The track select circuit consists of UE2, UF2A, UF2B, UF2C, UF2D, UF2F, UG4C, and Q4 through Q7. UE2, the phase decoder, pulls the selected ϕ(N) output low. To step inward (increasing track number), the four ϕ(N) lines must be clocked in ascending order (i.e., ϕ1, ϕ2, ϕ3, ϕ4, ϕ1, ϕ2 . . .). To step outward, the ϕ(N) lines must be clocked in descending order (i.e., ϕ4, ϕ3, ϕ2, ϕ1, ϕ4, ϕ3 . . .). Each of the ϕ(N) outputs is buffered by a NOT gate (UF2A, UF2B, UF2C, UF2F) and a transistor (Q4-Q7) configured as a common-emitter buffer. The windings of B2 (the stepping motor) form the collector loads for Q4-Q7. CR13-CR16 clip any overshoot produced by the inductive characteristics of the windings of B2.

When a logic 1 is applied to pin 9 of UF2D (ON/OFF line), the output of UE2 is enabled. When a logic 0 is applied to pin 9 of UF2D, the output of UE2 is disabled and none of the ϕ(N) lines are driven.

UG4C buffers the enable signal for UE2 and

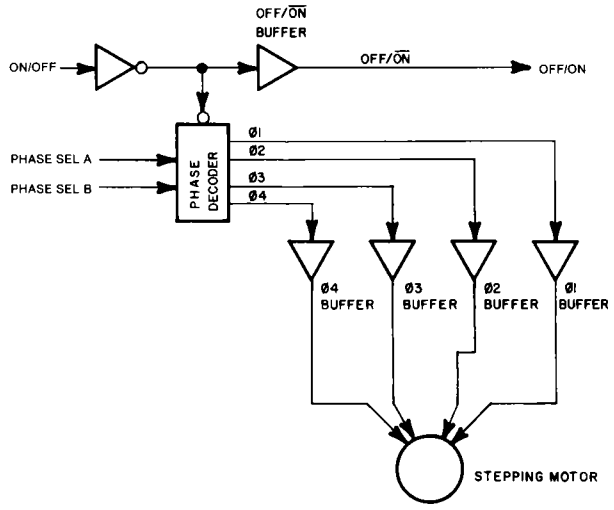


Fig. 7-12. Block diagram of track select circuit, Model 1540.

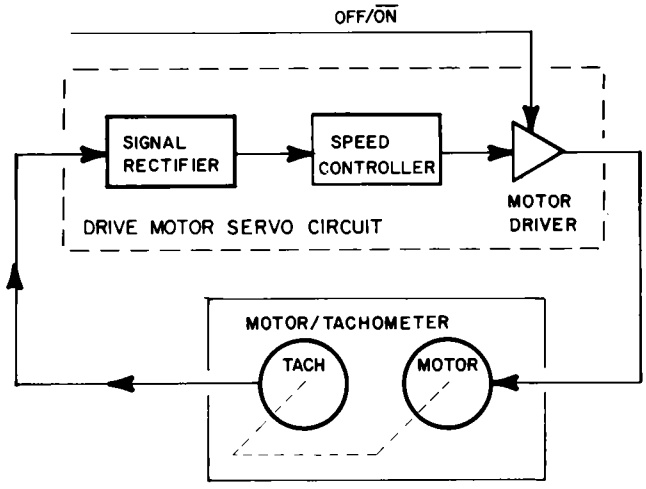


Fig. 7-13. Block diagram of drive motor system, Model 1540.

applies this signal to the motor driver servo circuit. Since the motor enable and step enable controls are both accomplished with the same line, tracks can only be changed while the drive motor (B1) is running. Table 7-5 illustrates the relationship between the ON/OFF, ϕ SEL A, and ϕ SEL B lines and the $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, and OFF/ON lines.

7.1.6 Drive Motor System Electrical Theory (Refer to Figs. 7-13 and 7-14)

The purpose of the drive motor system is to maintain the disk at a constant speed. The drive motor system consists of the drive motor servo circuit and the drive motor tachometer.

7.1.6.1 Drive Motor/Tachometer

The drive motor/tachometer contains a dc permanent magnet motor and a tachometer on a common shaft. The tachometer acts as a low-power ac generator. The voltage output of the tachometer increases with increasing drive speed and provides feedback to the drive motor servo circuit. This feedback contains motor speed information that the drive motor servo circuit uses to determine how hard to drive the motor. The drive motor servo circuit adjusts the motor current as necessary to maintain a constant speed of 300 rpm. This is necessary because each floppy disk may offer different mechanical loads to the motor, due to manufacturers' differences or age of the floppy disk.

7.1.6.2 Drive Motor Servo Circuit

Tachometer information enters the drive motor circuit at E4 and E5. This information, a sine wave, is rectified by the bridge rectifier consisting of CR1 through CR4. R1 provides a load for the tachometer. The output of the rectifier is applied to pin 1 of IC1.

IC1 is the speed controller. Power is supplied through a low-pass filter (R3 and C5). C2 is also provided for filtering. R2, R10, and VR1 determine the speed of the floppy disk. VR1 is used to calibrate disk speed. C3 and C6 provide filtering. The output of IC1 (pin 5) will increase if the voltage at pin 1 is less than the threshold set by VR1. Conversely, the output at pin 5 will decrease if the voltage at pin 1 is greater than the voltage set by VR1. The circuit will settle when the feedback at pin 1 is equal to the threshold set by VR1. The output of the speed controller (IC1, pin 5) is applied to the motor driver.

The motor driver consists of Q1 through Q4, R4 through R9, C4, and C7 through C9. Q2 is an inverting dc amplifier. C4 provides filtering. R4 limits its base current. The combination of Q1, CR5, and R7 enables or disables Q2. A logic low at E2 turns off Q1, allowing Q2 to operate normally. A logic high at E2 turns on Q1, shutting off Q2 by shunting its base current to ground and thus shutting off the motor. Q4 is the final pass transistor. When its base is pulled low by Q2, through R6, it will conduct harder. As Q2 increases in conduction, Q4 will proportionately increase its own conduction. R9 and Q3 form a current limiter. As emitter current in Q4 increases, the voltage drop across R9 increases. When the drop across R9 reaches approximately 0.65 volt, Q3 will conduct. When Q3 starts conducting, it shunts some of the bias current for Q4 to

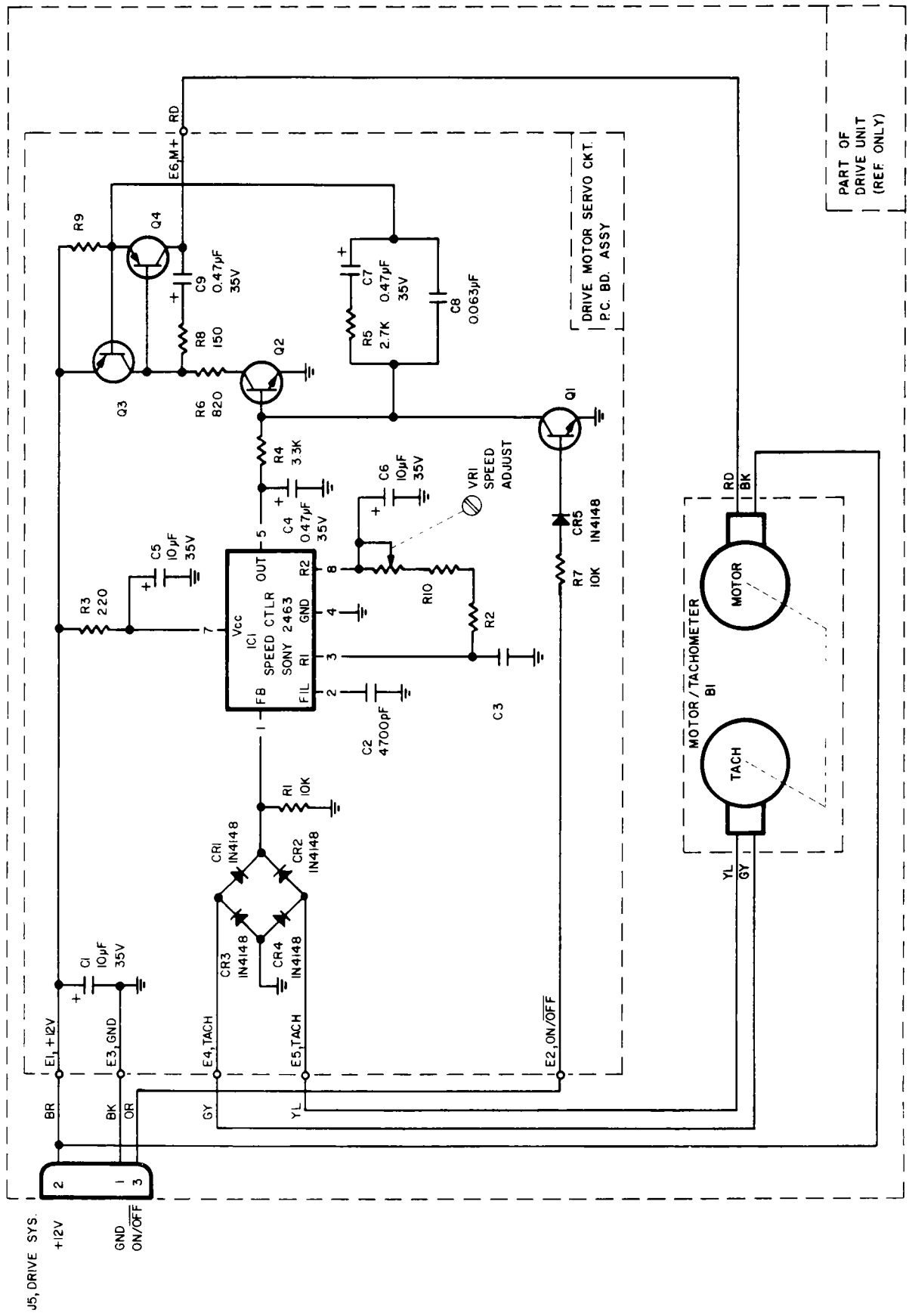


Fig. 7-14. Schematic of drive motor system, Model 1540.

the positive supply. Q3 will shunt enough bias for Q4 to maintain motor current at a safe level for B1 (the drive motor). C7 through C9, R5, and R8 control the slew rate and noise of the motor driver. The collector of Q4 is tied to the drive motor/tachometer to complete the servo loop. C1 is provided to bypass noise from the +12-volt supply.

7.1.7 Write Circuit Electrical Theory (Refer to Figs. 7-15 and 7-16)

The write circuit consists of the following major blocks: write logic, bias switch, amp enable switch, differential write amp, and the diode switch.

7.1.7.1 Write Logic

The write logic consists of UF5D, UF5A, UF5C, UG2C, and UC1D. UC1D inverts the write protect signal and applies this signal to UF5D and to the disk controller VIA. When the output of UC1D is high, the write protect notch is uncovered. UF5A inverts the read/write line and applies its output to UF5D. The output of UF5D is active (active low) only if the write/read and write protect lines are both high. The output of UF5D is applied to the amp disable switch, one of the bias switches, to UF5C (a NAND gate configured as an inverter), and to UG2C (an Exclusive OR gate also configured as an inverter). The output of UF5C (which is high when writing) is applied to pins 13 and 10 of UF6B which, in turn, enables the flip-flop. The output of UG2C is applied to the bias switch.

7.1.7.2 Bias Switch

During a write operation, the bias switch applies current through the bias winding (U1L2) in the read/write head. One side of the bias switch, Q10, drives the positive side of the bias winding. Q10 is gated into conduction by the input of UG4A, which is low when writing. The other side of the bias switch, Q3, drives the negative side of the bias winding. Q3 is driven into conduction by the input of UG4C, which is high when writing. Bias current flows through U1L2 via Q10, R8, Q3, CR8, and CR9 (both diodes are forward biased).

7.1.7.3 Amp Enable Switch

The amp enable switch consists of Q9 and UG4F. A low is applied to UG4F while writing, driving Q9 into conduction. When Q9 is conducting, power is applied to the differential write amp.

7.1.7.4 Differential Write Amp

The differential write amp consists of UG4D, UG4E, Q8, and Q11. UG4D and UG4E are driven by the encoder/decoder and, in turn, drive the differential transistor pair Q8 and Q11. When Q8 is conducting, Q11 is turned off. When Q11 is conducting, Q8 is turned off. The outputs of the differential write amp are applied to the read/write head via the diode switch.

7.1.7.5 Diode Switch

The diode switch consists of CR6 and CR11. When in the write mode, the center tap of the read/write winding (U1L1) is at ground potential because of bias switch Q3 and CR9. When Q3 goes into conduction, current flows through the read/write winding via either Q11, CR11, CR9, and Q3 or via Q8, CR6, CR9, and Q3, depending upon the state of the differential write data from the encoder/decoder circuit.

7.1.8 Read Circuit Electrical Theory (Refer to Figs. 7-15, 7-17, and 7-18)

The read circuit senses and amplifies data from the floppy disk. The amplified data is checked for valid pulse widths to improve noise immunity. The output of the read circuit is a narrow pulse which occurs on both the rising and falling edges of the data.

The read circuit does not care if the data is high or low. Only the positions of the transitions are significant. The data is divided into cells. If a transition occurs at the beginning of a cell, the cell is interpreted as a logic 1. If no transition occurs, the cell is interpreted as a logic 0.

The data is sensed by the read/write head and applied to the first video amplifier (UH7) via the diode switch (see Fig. 7-15). When in the read mode, Q9, Q10, and Q3 are not conducting. CR7 and CR10 are forward biased via R12, R13, U1L1, CR9 (which is also forward biased), and CR12 (a 5.2-volt zener diode). The cathodes of CR7 and CR10 are at approximately +6 volts, causing the data to be applied to the first video amplifier (UH7). The +6-volt bias is applied to the cathodes of CR11 and CR6.

Since Q9 is not conducting, R10 and R7 pull the anodes of CR11 and CR6 to ground, causing CR11 and CR6 to be reverse biased and isolating the write circuit from the read circuit. CR8 is also reverse biased, since the +6-volt bias on the cathodes of CR7 and CR11 is applied to the cathode of

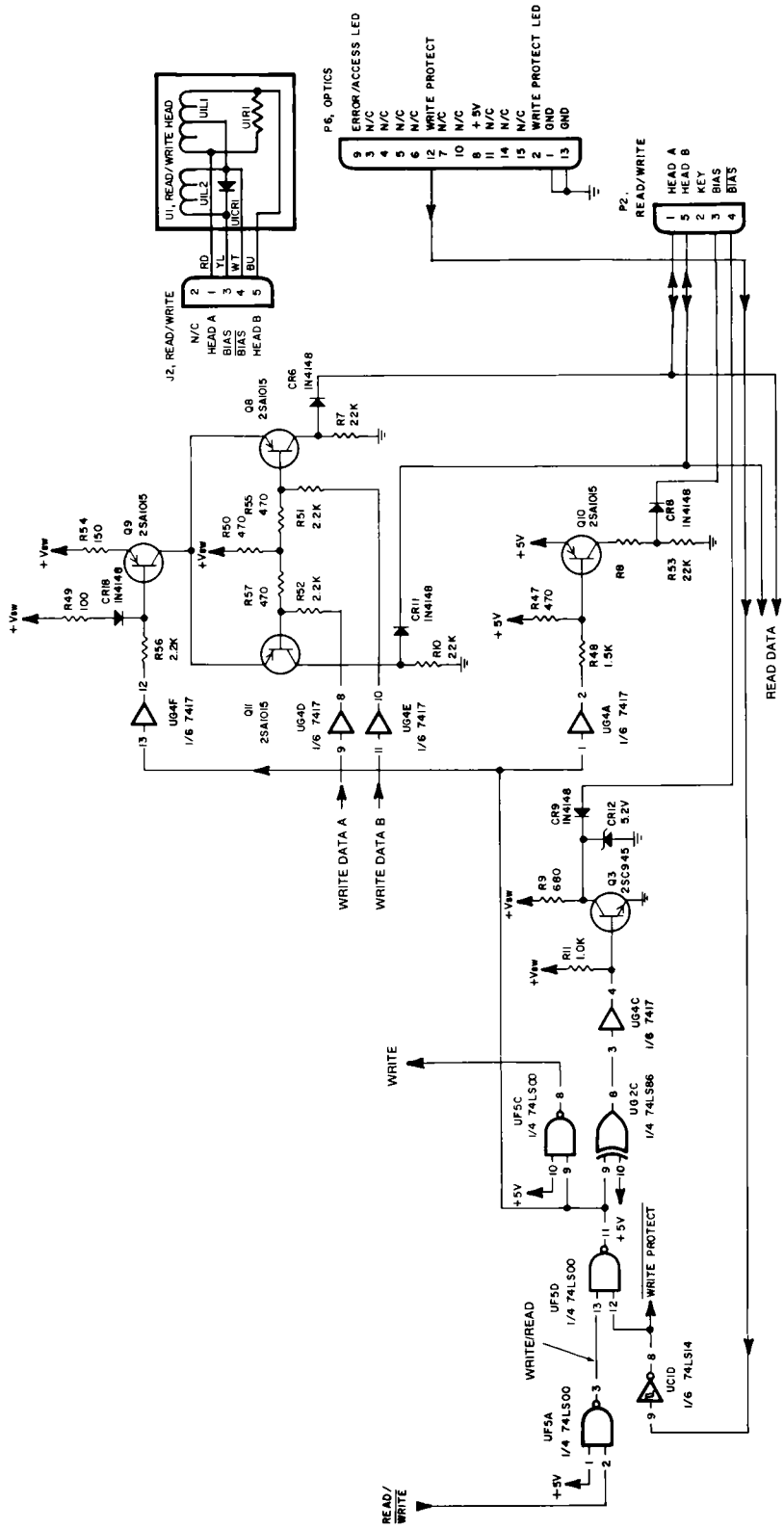


Fig. 7-15. Schematic of write circuit, Model 1540.

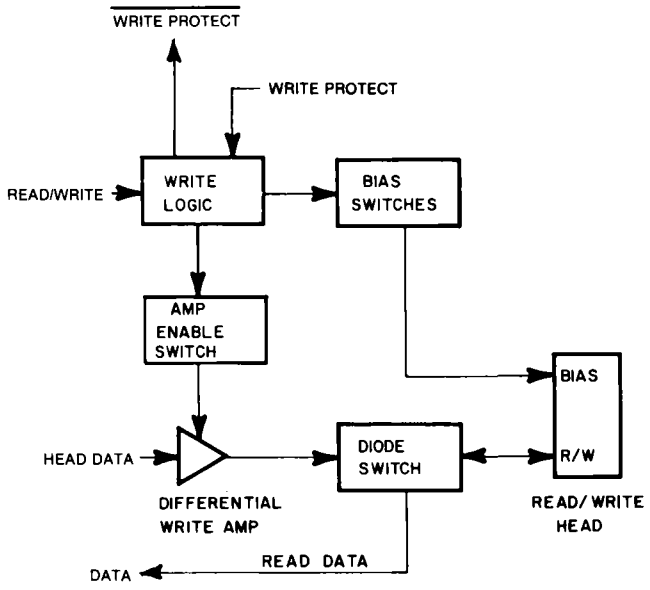


Fig. 7-16. Block diagram of write circuit, Model 1540.

CR8 via the read/write winding (U1L1) and the bias winding (U1L2).

The output of UH7, the first video amplifier (see Fig. 7-18), is applied to a low-pass filter formed by L8 through L11 and C16. C15 and C24 block the dc offset out of the UH7 to prevent the offset from disturbing the input bias to UH5. R16 and R17 set a bias voltage of +6 volts which is filtered by C23 and C57 and applied to the input signal of UH5 via R18 and R19. The output of UH5 is applied to the comparator via C58, C59, R27, and R28. C58 and C59 block the dc offset out of UH5 to prevent the offset from affecting the bias on the input of the comparator, UH4. A +6-volt bias is applied to the input signal of the comparator from R16 and R17 via R14 and R15.

The output of the comparator is applied to the valid pulse detector (UG2D, UG3A, and UF6A). UG2D, along with C27, R24, and R25, forms an edge detector. Pin 11 of UG2D will produce a 500-nanosecond active high pulse on rising edges of the comparator's output and will produce a 150-nanosecond high pulse on falling edges of the comparator's output. The pulse out of UG2D is applied to UG3A, a single-shot multivibrator. UG3A produces an active low pulse which is approximately 2.5 microseconds wide. Flip-flop UF6A is clocked on the trailing edge of the output pulse of UG3A. The output of the comparator must be maintained for at least 2.5 microseconds in order to be latched into the flip-flop. If a narrow noise pulse triggers this circuit, the output of the flip-flop will not change since the noise pulse will terminate before UG3A triggers UF6A. The output of the flip-flop (UF6A) will reflect the data delayed by approximately 2.5 microseconds.

The valid data out of the valid pulse detector is applied to an edge detector consisting of UG2A and UG3B. UG2A operates the same as UG2D above. The pulses out of UG2A trigger UG3B, a single-shot multivibrator. UG3B produces a narrow pulse, which represents transitions of the data. This output is applied to the timing circuit to synchronize the encoder/decoder clock, and to the encoder/decoder, which will detect the data and perform a serial-to-parallel conversion. Notice that pin 5 of UG3A is connected to the read/write line, causing

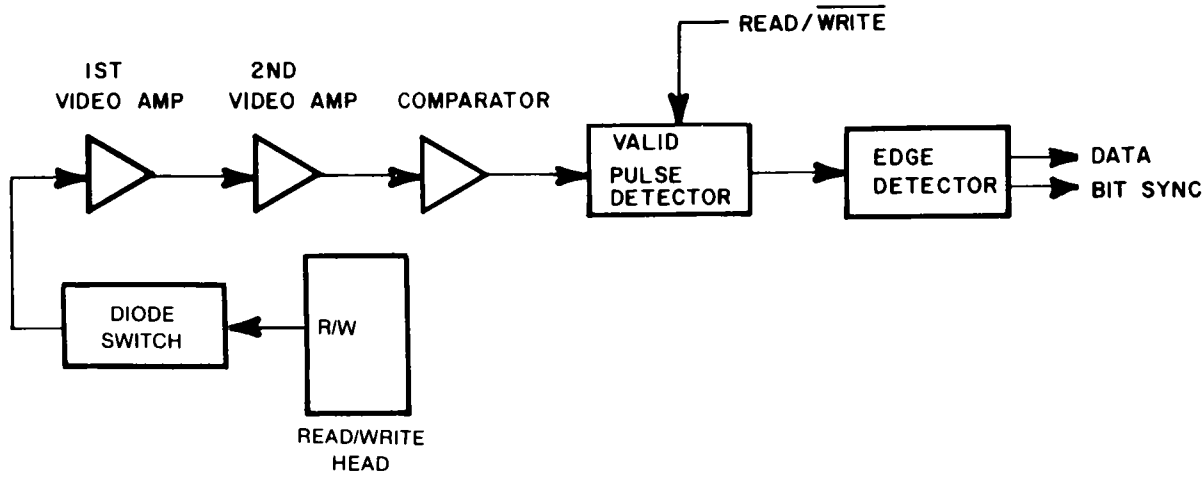


Fig. 7-17. Block diagram of read circuit, Model 1540.

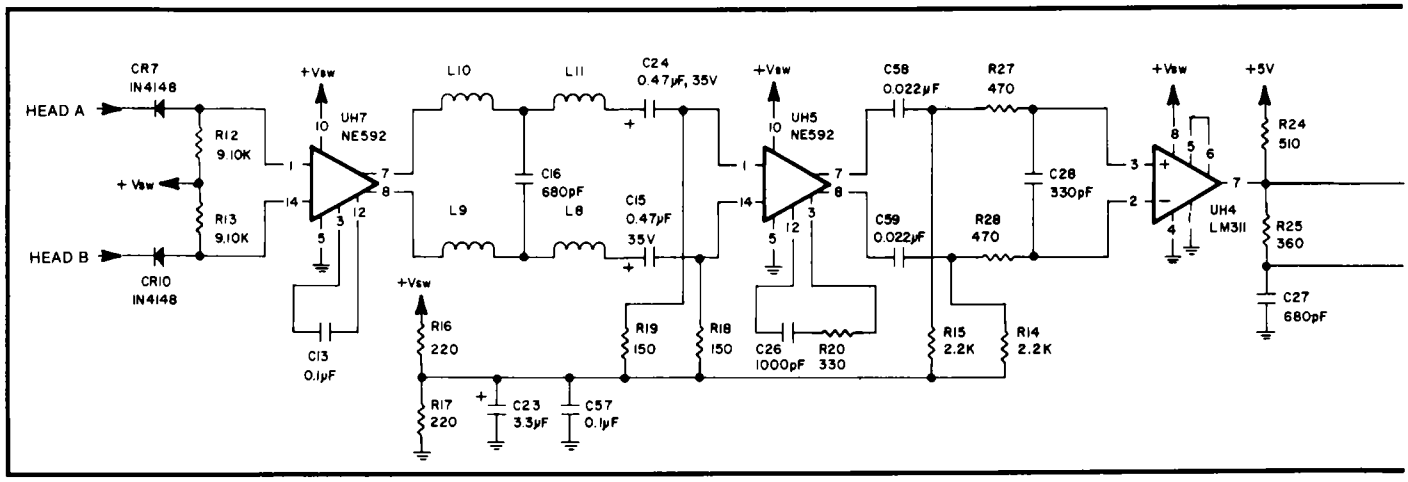


Fig. 7-18. Schematic of read

the valid pulse detector to be disabled during a write operation.

The video amplifiers will often oscillate with no data in, but these oscillations are high enough in frequency that they seldom get past the valid pulse detector.

7.1.9 Encoder/Decoder Electrical Theory (Refer to Figs. 7-19 and 7-20)

The encoder/decoder circuit encodes and decodes the transition positions which are written to, or read from, the disk. The encoder/decoder circuit also performs the serial-to-parallel and parallel-to-serial conversions necessary to move the data between the computer and the floppy disk.

7.1.9.1 Decoder

The decoder consists of UF4 and UE5A. The decoder has two outputs. Pin 1 of UE5A is the serial data output and pin 2 of UF4 is the serial clock output. The serial data output contains a clock bit between data bits. The serial clock output is high whenever the clock or data bits are valid on the serial data line.

A cell is four encoder/decoder clock pulses wide. As mentioned in read circuit theory, if a transition (or pulse into the decoder) occurs at the beginning of a cell, that cell is a logic 1. If no transition occurs, the cell is a logic 0. When a transition does occur, UF4 (a binary counter) is cleared and the timing circuit is reset to start the encoder/decoder clock at the beginning of its cycle. Pins 6 and 7 of UF4 are at logic lows, causing the output of UE5A, the serial data line, to go to a logic 1.

Two encoder/decoder clock pulses later, the serial clock (pin 2 of UF4) goes high. When the serial clock line is high, the serial data line is valid. The serial clock line remains high for two clock cycles.

A bit cell is now complete. At this time, pins 2 and 3 of UF4 will again be a logic 0 and pin 6 will be a logic 1. The logic 1 on pin 6 of UF4 causes the serial data line (pin 1 of UE5A) to be a logic 0. If no transition occurs at the beginning of the next cell, the serial data line will remain at a logic 0 when the serial clock line goes high, two encoder/decoder clock cycles into the cell.

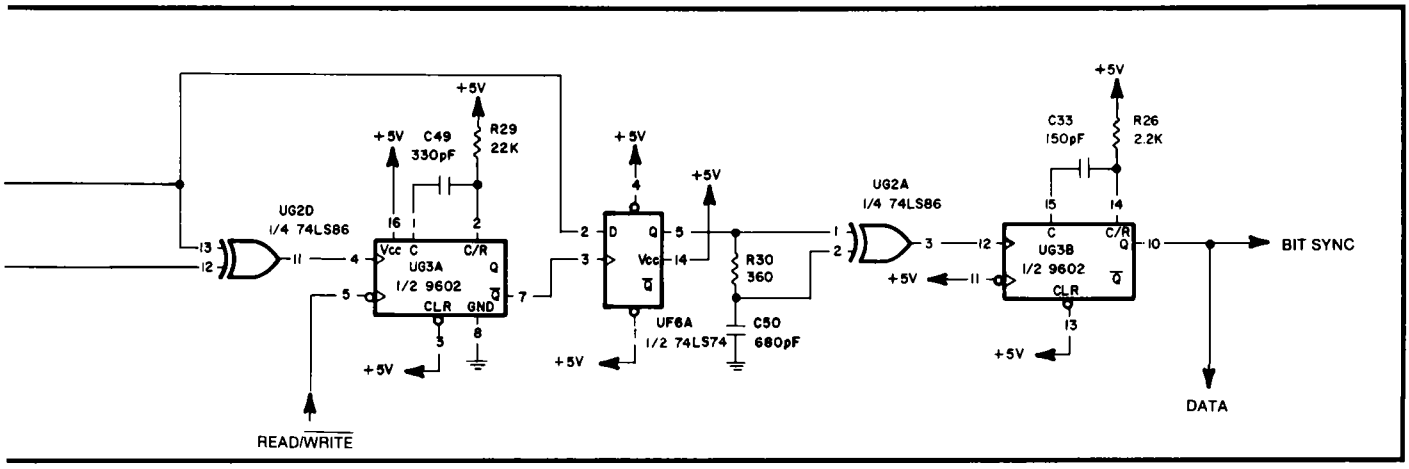
7.1.9.2 Bit Counter

The bit counter produces the byte sync signal to the microprocessor and the shift/load signal for the parallel-to-serial converter. UE3, UF3, and UC1B form the bit counter. UE3 is a 4-bit binary counter that is clocked by the serial clock. Every eight serial clock pulses, when the outputs of QA, QB, and QC go to logic 1, the output of UF3A goes low. The logic 0 from UF3A causes the output of UC1B to go high. The high output of UC1B is then applied to UF3B and UF3C. UF3C NANDs the output of UC1B with the byte sync enable line from the disk controller VIA and with the inverted serial clock from UE5B. The output of UF3C informs the microprocessor that a byte is ready to be read into the computer. When in the write mode, the output of UF3C is used to indicate that the next byte to be written should be loaded.

UF3B NANDs the output of UC1B with the serial clock and with the QA output of UF4. The output of UF3B, when low, causes the next byte to be transmitted to be loaded into the parallel-to-serial converter.

7.1.9.3 Serial-to-Parallel Converter

The serial-to-parallel converter consists of UD2 and UE4. UD2 produces eight bits in parallel, which may be entered into the computer. UE4 adds an additional two bits, which are used to de-



circuit, Model 1540.

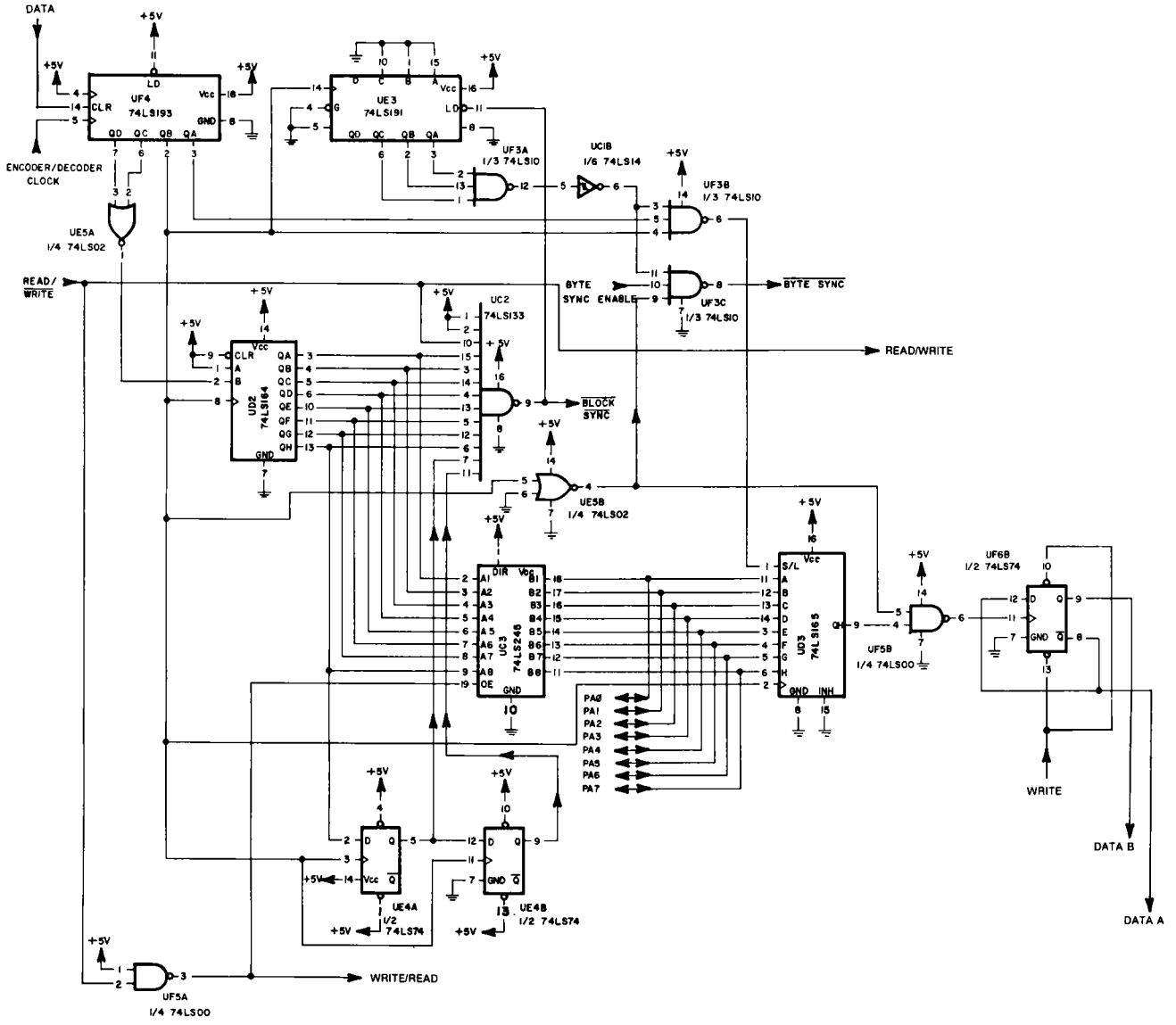


Fig. 7-19. Schematic of encoder/decoder circuit, Model 1540.

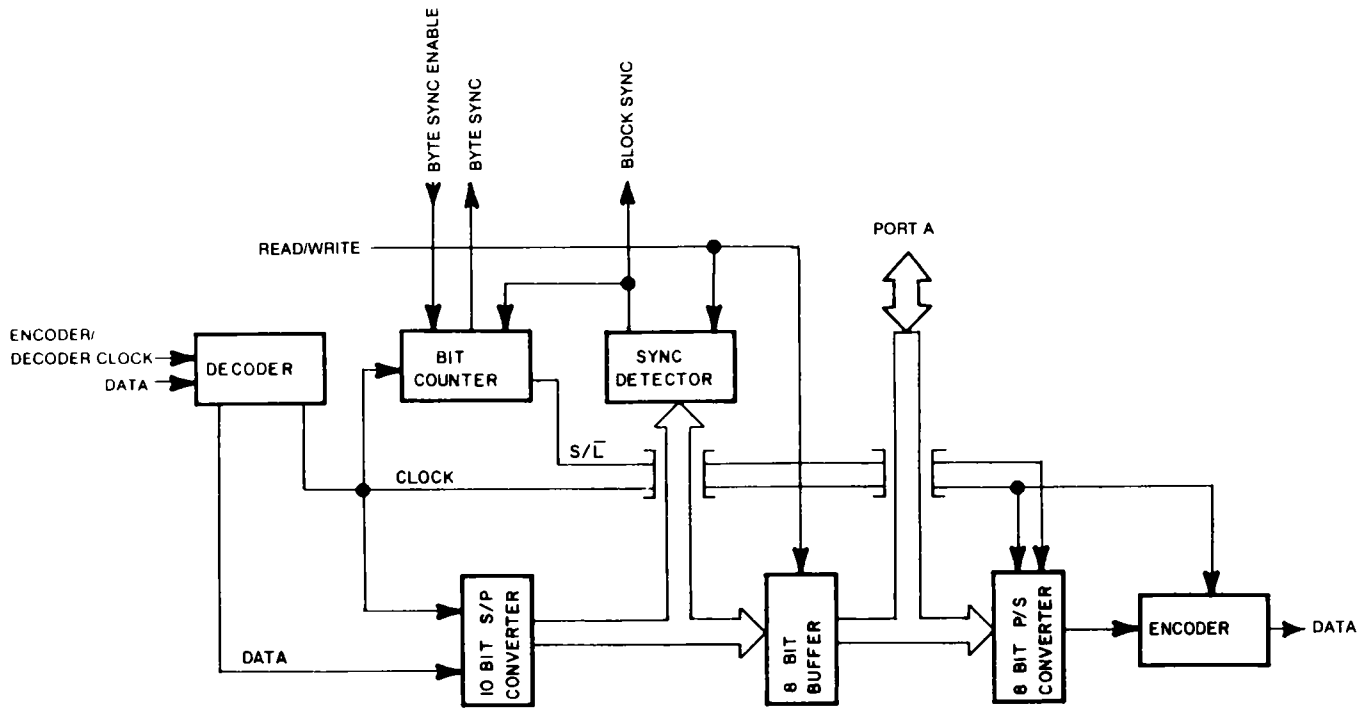


Fig. 7-20. Block diagram of encoder/decoder circuit, Model 1540.

tect block sync signals. Serial data is presented to the input of UD2 (pin 2). The serial clock, which is applied to the clock input of UD2 (pin 8), shifts the contents of the serial-to-parallel converter on its rising edge. Data on the disk is encoded using 10-bit group code recovery (GCR). The computer encodes and decodes the GCR code. GCR coding prevents more than two zeros from appearing together. Because GCR coding uses 10 bits to define a decoded 8-bit byte, the encoder/decoder must deliver five bytes of encoded data to the computer in order for the computer to decode four bytes of data.

7.1.9.4 Buffer

The buffer, UC3, gates data onto port A of UCD4 when in the read mode. When in the write mode, the buffer is tristated, allowing data from port A of UCD4 to be applied to the parallel-to-serial converter without conflict from UD2.

7.1.9.5 Sync Detector

A block sync signal consists of at least 16 logic 1s (clock and data bits set to logic 1). During a read operation, the output of UC2 goes low when 10 consecutive logic 1s are detected by the serial-to-parallel converter. The block sync signal is available on pin 9 of UC2. The leading edge of the block sync signal interrupts the computer, which then monitors the signal until its falling edge. After the falling edge occurs, the computer enables the byte sync and waits for the byte sync to become active. When the byte sync becomes active, the received byte is loaded into the computer. All received data is synchronized in this manner.

7.1.9.6 Parallel-to-Serial Converter

In the write mode, data from port A of UCD4 is applied to the parallel-to-serial converter, UD3. When the output of UF3B becomes active, the byte to be written is loaded into the serial-to-parallel converter. The inverted clock signal is used to shift bits out of the parallel-to-serial converter. UF3C informs the computer to load the next byte to be written.

7.1.9.7 Encoder

The encoder consists of UF5B and UF6B. The encoder must produce a transition for each high bit presented to it and must not produce a transition for a low bit. UF5B gates the inverted clock signal to the flip-flop (UF6B) when a high is applied to UF5B from UD3. When a low from UD3 is applied to UF5B, no clock pulse is gated to UF6B. UF6B will change states whenever a clock pulse is applied to pin 11. The result is a transition for every high bit

out of UD3. UF6B may be disabled by applying a logic low to pins 13 and 12 of UF6B. The complementary outputs of UF6B are available on pins 8 and 9 and are applied to the write circuit.

7.1.10 Optics Circuit Electrical Theory (Refer to Figs. 7-21 and 7-22)

The optics circuits consist of DS1 on the case assembly; DS1, CR1, and Q1 on the drive unit; and UF2E, R35, R36, R44, and R45 on the disk controller PC board.

R45 provides current limiting for the power LED, DS1 on the case assembly. R35 provides current limiting for CR1, the optical transmitter, on the drive unit. Both CR1 on the drive unit and DS1 on the case assembly turn on as soon as the +5-volt line becomes active (power on). The optical receiver, Q1 on the drive unit, is positioned under CR1 in such a manner that the write protect notch is directly between them when the floppy disk is seated. Q1 on the drive unit conducts (produces a logic 0) when the write protect notch is left uncovered (writing permitted). When the write protect notch is covered, Q1 on the drive unit does not conduct (logic 1). The write protect output of the optical receiver is available on pin 12 of P6 and is applied to the write circuit. UF2E drives the access/error LED. A high on the LED line causes DS1 on the drive unit to illuminate. R36 limits the current through DS1.

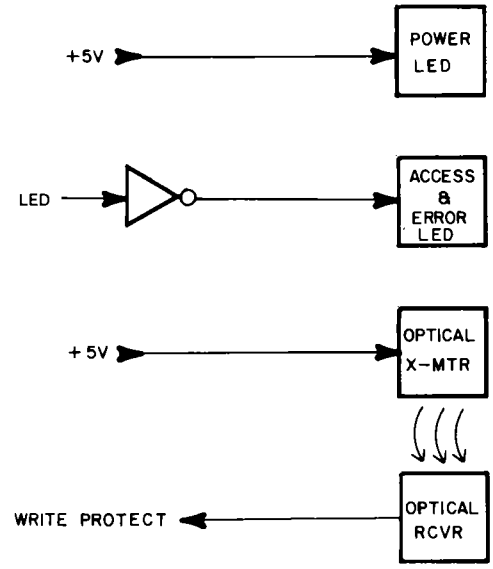


Fig. 7-22. Block diagram of optics circuit, Model 1540.

7.2 ADVANCED THEORY, MODEL 1541

7.2.1 Frame Electrical Theory (Refer to Figs. 7-23 and 7-24)

The electrical function of the frame assembly is to condition and convert the ac line voltage before applying it to the power supply on the disk controller PC board.

The ac line voltage enters the disk drive at J9, which is both a connector and an RFI filter. After

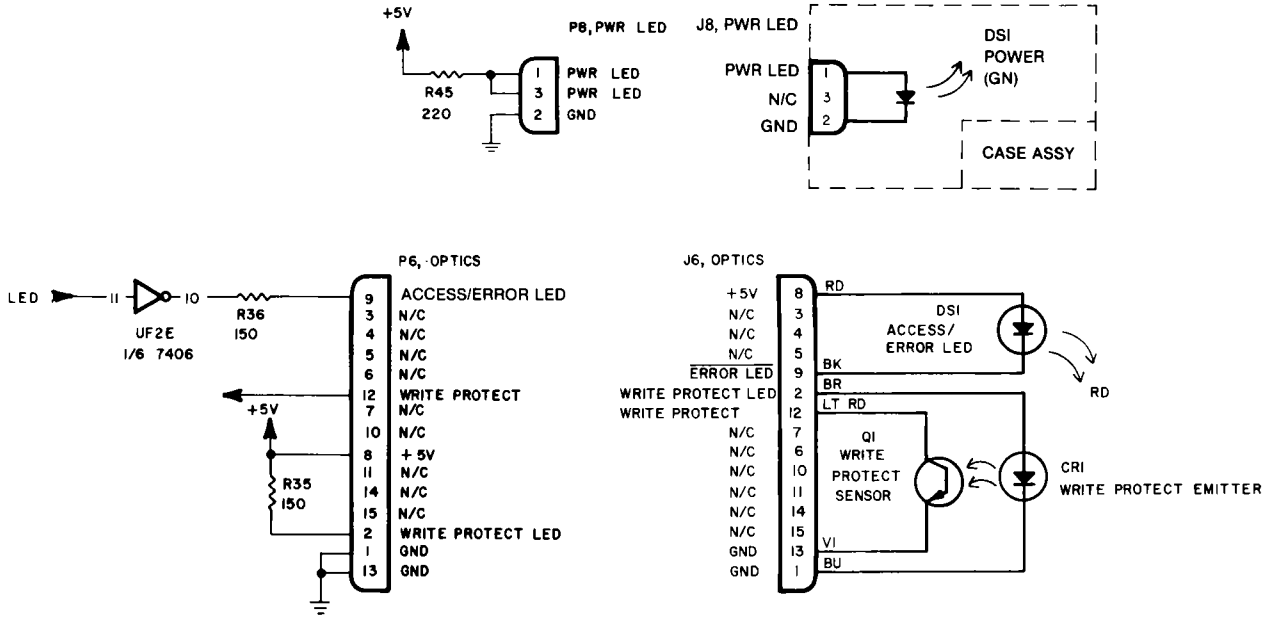


Fig. 7-21. Schematic of optics circuit, Model 1540.

Fig. 7-23. Block diagram of frame assembly, Model 1541.

passing through the filter, the ac voltage is applied to the SPST power switch, S1. The output of the power switch is applied to F1, which provides overcurrent protection. F1 is a 1-ampere, 250-volt slow blow fuse. The output of F1 is fed to the transformer, T1. T1 steps down the ac line voltage into 9 volts ac and 16 volts ac. Both of these outputs have their own secondary windings and are isolated from each other.

7.2.2 Power Supply Electrical Theory (Refer to Figs. 7-25 and 7-26)

The VIC-1541 power supply produces two regulated voltages, +12 volts dc, and +5 volts dc. These voltages are derived, respectively, from the 16 volts ac and 9 volts ac supplied by the frame assembly. The power supply, located on the disk controller PC board, has a reliability switch which removes power from the write amplifiers in the event of a +5-volt failure or during power up/down. Thus, the reliability switch protects the data on the floppy disk by disabling the write amplifiers whenever the +5-volt line goes below 3.9 volts.

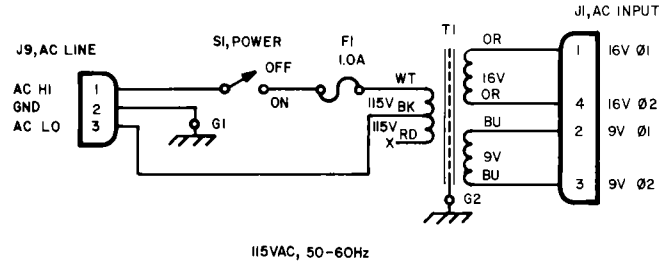


Fig. 7-24. Schematic of frame assembly, Model 1541.

7.2.2.1 +12 Volts DC

Sixteen volts ac is applied to the power supply via pins 1 and 4 of P1. From P1, the ac power is applied to bridge rectifier CR1. CR1 rectifies (full wave) the 16 volts ac to produce approximately +21 volts dc. The output of the rectifier is applied to a filter consisting of C1 and C17, which smooths out the pulsating dc from CR1. The output of the filter is applied to U2, a +12-volt regulator. The output of U2 is the regulated +12 volts dc output of the power supply. C2, C21, and C3 reduce line noise, and CR2 protects the regulator against negative voltage excursions during power up/down.

7.2.2.2 +5 Volts DC

The +5-volt leg of the power supply operates in the same fashion as the +12-volt leg, the only difference between them is in voltage levels. Nine

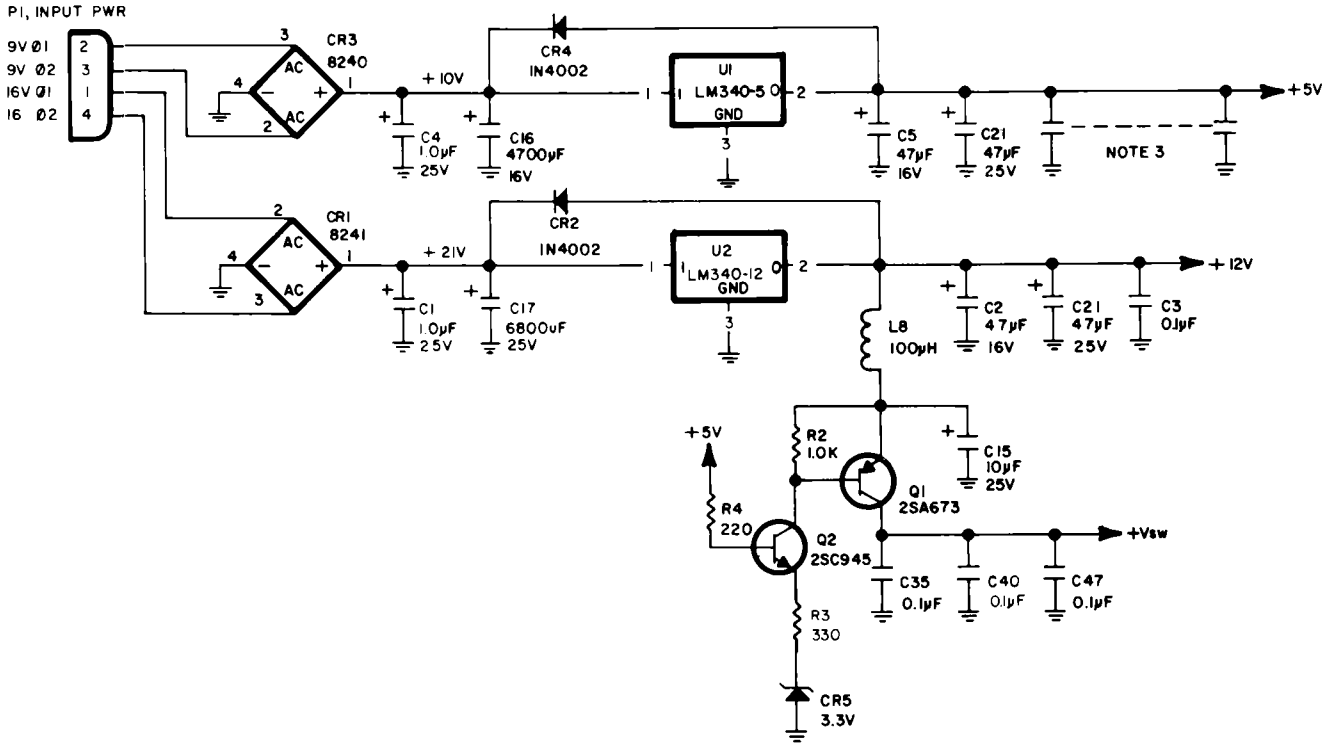


Fig. 7-25. Schematic of power supply, Model 1541.

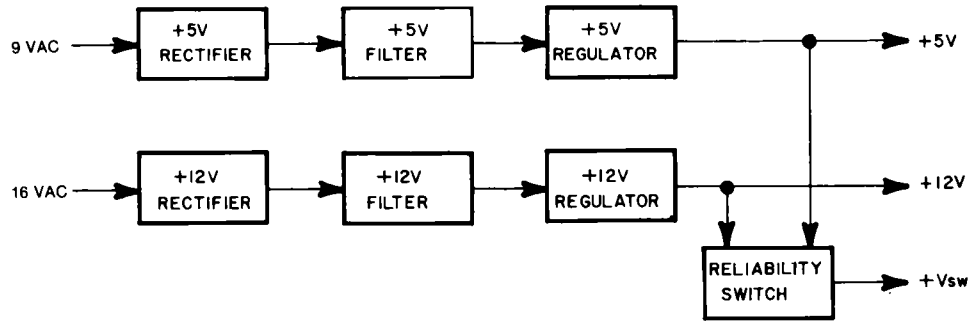


Fig. 7-26. Block diagram of power supply, Model 1541.

volts ac is applied to the power supply via pins 2 and 3 of P1. The ac power is applied to bridge rectifier CR3. After rectification, the resulting +10 volts dc is filtered by C4 and C16 before it is applied to the +5-volt regulator, U1. The output of U1 is the regulated +5-volts dc output of the power supply. C5 reduces line noise and CR4 protects the regulator against negative voltage excursions during power up/down.

7.2.2.3 Reliability Switch

The reliability switch consists of Q1, Q2, CR5, and associated components. Q2 and CR5 form a comparator. When the +5-volt line exceeds +3.9 volts, base current of Q2 flows through the base-emitter junction via R4, R3, and CR5. The cutoff voltage is determined by CR5 (3.3 volts) and the base-emitter drop of Q2 (0.6 volt). As the base-emitter current increases, collector-emitter current also increases. When Q2 begins to draw collector current, it forces Q1 into conduction by causing base-emitter current to flow through Q1 via L8, Q2, R3, and CR5. When Q1 is turned on, approximately 11.6 volts is applied to the $+V_{SW}$ line to enable the write amplifiers. If the +5-volt line drops below 3.9 volts, Q2 is turned off, in turn turning off Q1. With Q1 turned off, power is removed from the $+V_{SW}$ line and the write amplifiers are disabled. R2 ensures that Q1 is properly turned off by shunting any Q2 leakage current away from Q1. L8 and C15 form a low-pass L-type filter which isolates the noise produced by the motors in the +12-volt line. C35, C40, and C47 are bypass capacitors which reduce noise in the $+V_{SW}$ line.

7.2.3 Timing Electrical Theory (Refer to Figs. 7-27 and 7-28)

The timing circuit produces the clock signals. One of the outputs is a 1-MHz square wave. This fixed 1-MHz clock signal is applied to the microprocessor, controlling the rate at which the microprocessor executes instructions. The second output is a variable frequency pulse which is used to control the encoder/decoder circuit. The timing circuit consists of a 16-MHz oscillator, a divide-by-16 frequency divider, and a programmable divider.

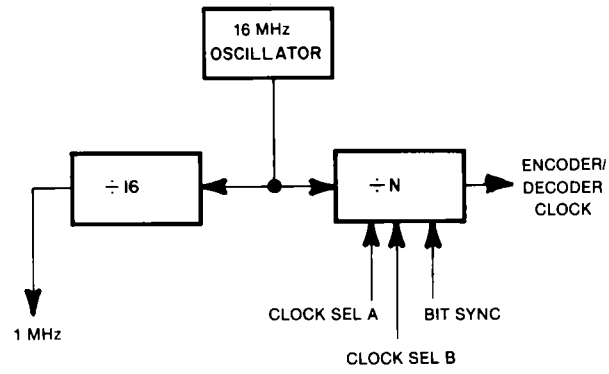


Fig. 7-27. Block diagram of timing circuit, Model 1541.

7.2.3.1 16-MHz Oscillator

The 16-MHz oscillator is Y1, a crystal-controlled square-wave oscillator. The output of the 16-MHz oscillator is applied to the divide-by-16 frequency divider and to the programmable divider.

7.2.3.2 Divide-by-16 Frequency Divider

The divide-by-16 frequency divider consists of a 4-bit binary counter, UD5. Pin 5 (the divide-by-2 output) of UD5 is applied to pin 6 of UD5 in order to clock the last three stages of the counter. The output of the divide-by-16 frequency divider is taken from pin 12 and is applied to the microprocessor via L3 and R1, which filter the clock line to reduce noise.

7.2.3.3 Programmable Divider

The programmable divider produces the clock for the encoder/decoder circuit and may be reset to

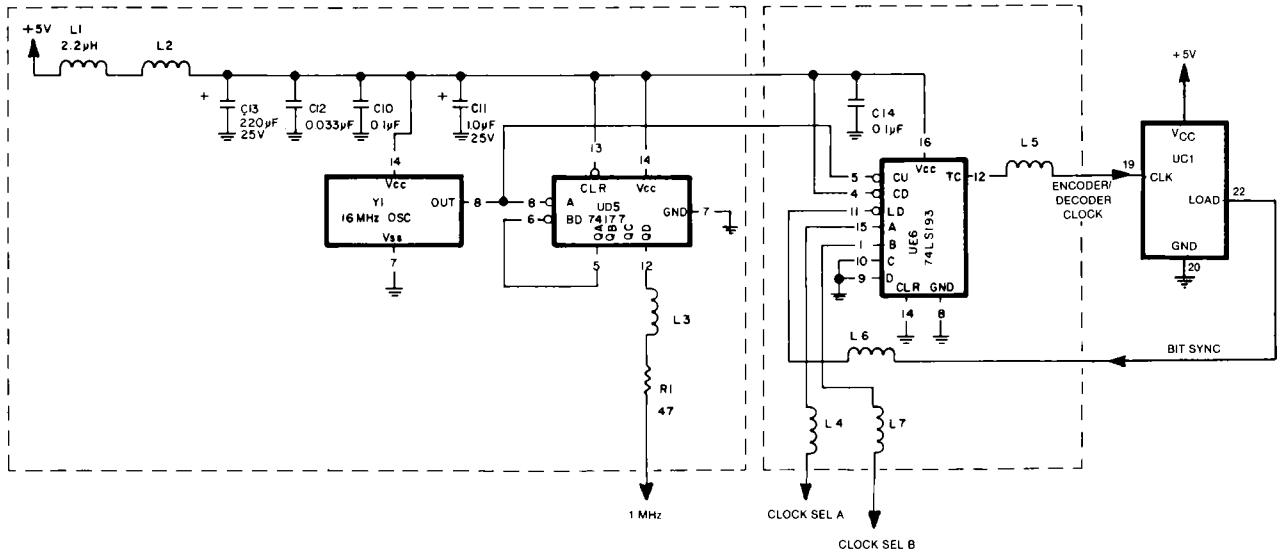


Fig. 7-28. Schematic of timing circuit, Model 1541.

allow the phase of the encoder/decoder clock to be controlled. Floppy disks have fewer sectors per track on the innermost track (track No. 35) than on the outermost track (track No. 1). This variation in number of sectors per track keeps the bit density fairly constant throughout the writing surface of the disk. Each disk is further divided into four zones, with each zone containing a unique number of sectors per track. The programmable divider has four possible output frequencies, with each frequency corresponding to one of the four zones on the floppy disk. In order to maintain fairly even bit densities, the encoder/decoder must be clocked at a faster rate when writing on the outer tracks than when writing on the inner tracks. This is because the outer surface of the disk is passing over the head more quickly than the inner surface. Thus, it is the encoder/decoder clock that determines how many sectors will fit on any given track.

The division factor of the programmable divider is controlled by the CLOCK SEL A and CLOCK SEL B lines. Table 7-6 defines parameters for each zone. The programmable divider consists of UE6 and UC1. UE6 is configured as a presettable 4-bit binary up counter. The output of UE6 is taken off pin 12, the TC output. The TC output (active low terminal count) goes low when the counter overflows from $1111_{(2)}$ to $0000_{(2)}$. This active low pulse is applied to UC1, the encoder/decoder circuit. An output of UC1, (pin 22), is an active low pulse that is applied to the load input of the presettable counter. When the load goes low, the counter is preset to the values present on the A, B, C, and D lines. The C and D lines are strapped low and therefore each line is set to 0. If the A and B lines are both low (zone 4 condition), the counter is preset to $0000_{(2)}$. Sixteen counts later the load line will reset the counter to $0000_{(2)}$. If the A line only is a logic 1 (zone 3 condition), the counter is preset to $0001_{(2)}$ and 15 counts later the load line will again preset the counter to $0001_{(2)}$. Note that only 15 counts were required, since the counter had a head start of one count. If the B line only is a logic 1 (zone 2 condition), the counter is preset to $0010_{(2)}$. The counter now has a head start of two counts and will require only 14 counts before it is preset again. If both the A and B lines are at logic 1 (zone 1 condition), the counter is preset to $0011_{(2)}$. The counter now has a head start of three counts and will require only 13 counts before it is preset again.

Table 7-6. Timing Circuit Parameters

	ZONE 1	ZONE 2	ZONE 3	ZONE 4
CLOCK SEL A	1	0	1	0
CLOCK SEL B	1	1	0	0
Division Factor	13	14	15	16
Encoder/Decoder Clock Freq (MHz)	1.2307	1.1428	1.0666	1.00
Sectors per Track	21	20	18	17
Track Numbers	1-17	18-24	25-30	31-35

L4 through L7 filter the signal lines to reduce noise. L1, L2, L7, and C10 through C14 form a

low-pass L-type filter which prevents the coupling of noise from the timing circuit to the +5-volt line and vice versa.

Pin 22 of UC1 is the BIT SYNC output. The BIT SYNC output produces a pulse whenever the programmable counter, UE6, overflows or whenever a high-to-low or a low-to-high transition occurs in the serial data on the disk. When this pulse occurs, the encoder/decoder clock is set to the beginning of its cycle and the clock is synchronized with the serial data. UC1 maintains the phase relationship between the serial data and the encoder/decoder clock to within 62 nanoseconds.

7.2.4 Computer Electrical Theory (Refer to Figs. 7-29 and 7-30)

The computer performs two major functions—serial bus communications and floppy disk control. Communication with the serial bus is accomplished by the serial bus interface. Interfacing with the floppy disk is accomplished by the read, write, track select, motor drive, timing, and optics circuits along with the drive unit itself. The computer communicates with these devices through the versatile interface adapter (VIA). The computer consists of the MPU, ROM, RAM, write logic, address decoder, VIA, and the serial bus interface.

7.2.4.1 MPU

UC4 is a 6502, 8-bit microprocessor. The microprocessor fetches an instruction from ROM or RAM and executes the instruction. The instruction, in turn, causes the microprocessor to alter data in RAM, internal registers, or registers in the VIAs. After completing each instruction, the MPU fetches the next instruction and the cycle continues. The rate at which the microprocessor executes instructions is determined by the $\phi 1$ clock present at pin 37 of UC4. The $\phi 1$ clock is produced by the timing circuits (refer to Section 7.2.3 "Timing Electrical Theory"). The microprocessor, in turn, produces an inverted, nonoverlapping clock signal (i.e., $\phi 2$) from the $\phi 1$ clock. The $\phi 2$ signal is present at pin 39 of UC4. Two NOT gates, UC5A and UC5F, buffer the $\phi 2$ clock before it is sent to the VIAs (UC2 and UC3) and to the write logic. The $\phi 2$ signal is used to synchronize write operations; therefore, the ROM does not require the $\phi 2$ signal.

The nonmaskable interrupt (NMI, UC4, pin 6) is disabled by R10 and is not used. The ready line (RDY, UC4, pin 2) is held at a logic high by R9 and also is not used.

There are three lines entering the microprocessor that allow hardware devices in the VIC-1541 to change the sequence of instructions executed by UC4. These lines are: set overflow (SO, pin 38), interrupt request (IRQ, pin 4), and reset (RST, in 40). When the set overflow line goes high, it sets the overflow bit in the status register internal to UC4. The sequence of instructions may be changed by testing the overflow flag using the BVC (branch if overflow clear) or BVS (branch if overflow set) instructions.

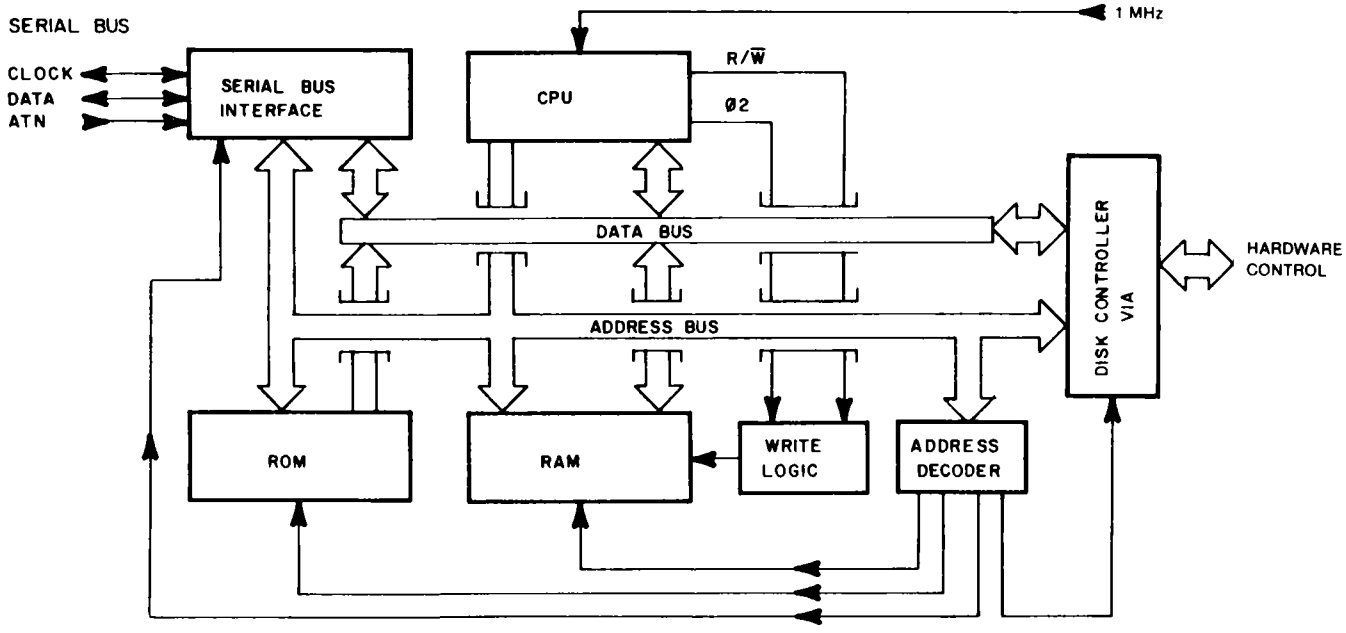


Fig. 7-29. Block diagram of computer circuit, Model 1541.

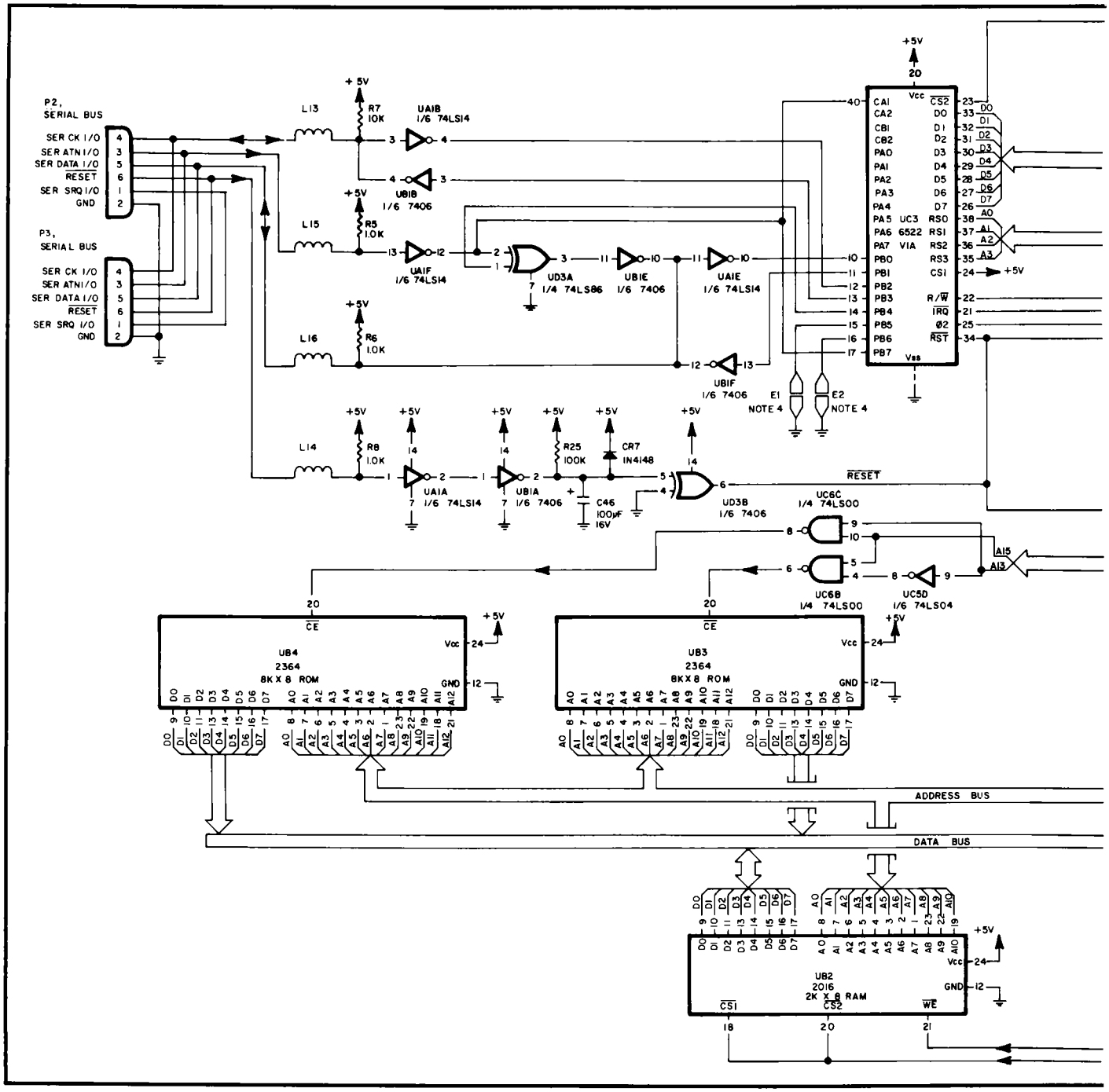


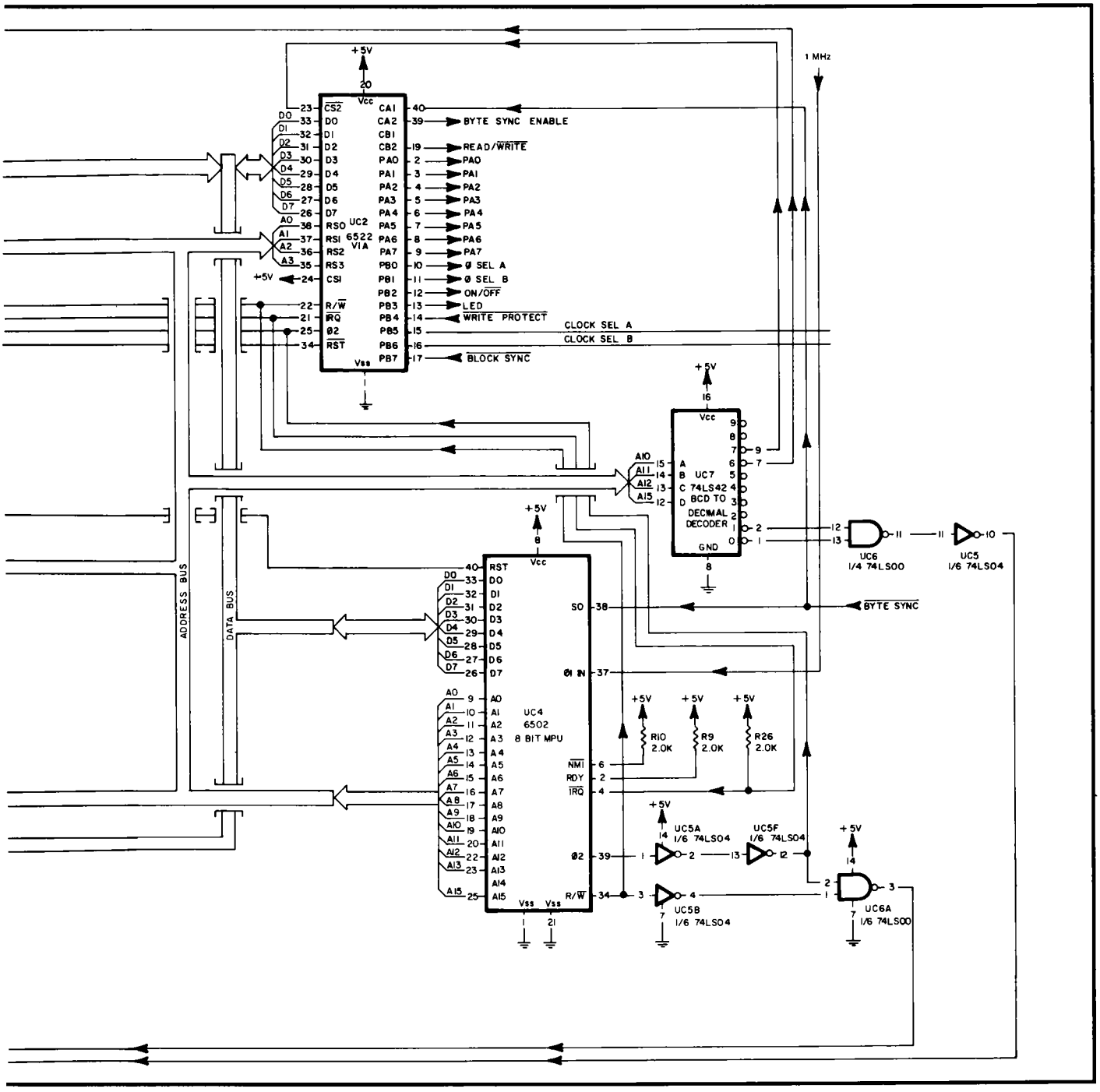
Fig. 7-30. Schematic of computer

When the interrupt request line goes low, the microprocessor calls the subroutine whose starting address is stored at locations $FFFE_{(hex)}$ (low byte) and $FFFF_{(hex)}$ (high byte). $FFFE_{(hex)}$ contains $FE_{(hex)}$ and $FFFF_{(hex)}$ contains $67_{(hex)}$. These two bytes form the 16-bit address $FE67_{(hex)}$, which is the starting address of the interrupt routine. The IRQ line may be defeated or "masked" under software control.

When the RST line is pulled low, the microprocessor executes the instructions whose starting address is located at $FFFD_{(hex)}$ (high byte) and $FFFC_{(hex)}$ (low byte). The address stored in these two locations is $EAA0_{(hex)}$, which is the address of the first instruction of the reset routine. The reset routine initializes the VIC-1541.

7.2.4.2 ROM

UB4 and UB3 are 8K × 8 ROMs which together form a 16K ROM. The ROMs contain in-



circuit, Model 1541.

structions which make up a machine language program called the DOS (disk operating system). The ROMs are located between addresses $C000_{(hex)}$ and $FFFF_{(hex)}$. Data is applied to the data bus (D0 through D7) from the ROM when the CE line (pin 20) goes low. The address inputs (A0 through A12) determine which one of the 8192 bytes in the ROM will be applied to the data bus. While the CE line is high, the data outputs are tristated and essentially disconnected from the data bus.

7.2.4.3 RAM

The RAM is UB2, a 2K-byte RAM. The RAM is located between addresses 0 ($0000_{(hex)}$) and 2047 ($07FF_{(hex)}$). Significant locations in RAM are:

0000-00FF	Zero Page
0100-01FF	Microprocessor Stack

The zero page contains variables, pointers, and other data used by the DOS. The microprocessor stack is used for temporary storage of data.

When the MPU writes to the RAM, the data to be written is placed on the data bus (D0 through D7), the location that the data is to be written into is placed on the address bus (A0 through A15), and the WE (write enable) and CS (chip select) lines are brought low. When the MPU reads from the RAM, the location to be read is placed on the address bus (A0 through A15) and the CS line is brought low. Data is then gated from the RAM to the data bus (D0 through D7).

7.2.4.4 Address Decoder

The address decoder selects one of the devices listed in Table 7-7 when the address bus contains an address within the address range of the device.

Table 7-7. Address Decoder Parameters

DEVICE	ADDRESS RANGE (HEX)
RAM, (UB2)	0000-07FF
VIA, Serial Bus (UC3)	1800-180F
VIA, Disk Control (UC2)	1C00-1C0F
ROM, Low (UB3)	C000-DFFF
ROM, High (UB4)	E000-FFFF

UC6B and UC6C decode the ROM low and ROM high addresses. UC5D is a NOT gate, which inverts A13 before it is applied to UC6B. UC6B enables UB3, the low ROM, when A15 = logic 1 and A13 = logic 0. UC6C enables UB4, the high ROM, when A15 = logic 1 and A13 = logic 1. A0 through A12 are decoded by the selected high or low ROM. Notice that A14 is not decoded, and it therefore does not affect the operation of the decoder. The end result is two identical 16K blocks of ROM. Each of the ROM chips has two valid address ranges. One range is used with A14 = logic 0 and the other range is used with A14 = logic 1 as in Table 7-8.

Table 7-8. ROM Images

	A14 = LOGIC 0	A14 = LOGIC 1
ROM, Low (UB3)	8000-9FFF	C000-DFFF
ROM, High (UB4)	A000-BFFF	E000-FFFF

Data that is read from address $8000_{(hex)}$ is identical to the data read from address $C000_{(hex)}$. This must be so because both address the same location in the same ROM. The redundant 16K block between $8000_{(hex)}$ and $BFFF_{(hex)}$ is not normally used. It is just a by-product of the address decoder scheme. Notice that the read/write signals are not decoded for ROM addresses. The VIC-1541 hardware does not prevent a bus conflict between the microprocessor and the ROMs. The hardware design merely assumes any memory transfer at or above $8000_{(hex)}$ is a read operation.

CAUTION

Never write to memory locations at or above $8000_{(hex)}$. A bus conflict may occur, causing permanent damage to UB3, UB4, or UC4.

UC7, a BCD-to-decimal decoder, decodes the RAM and VIA address ranges. Address lines A10, A11, and A12 are connected to the A, B, and C inputs, respectively, of UC7. As a result, the outputs of UC7 decode one of eight 1024-byte blocks. Address line A15 is applied to the D input of UC7. When the D input is a logic 0, one of the 0 through 7 outputs will be active (i.e., logic 0). When the D input is a logic 1, outputs 0 through 7 will be inactive, effectively disabling UC7. Any address at or below $7FFF_{(hex)}$ will enable UC7. Any address at or above $8000_{(hex)}$ will enable the ROM array.

As noted previously, UC7 can decode one of eight 1024-byte blocks of memory. Notice that UC7 does not decode A13 or A14. As in the ROM address decoder, this produces redundant images of the 8K block decoded by UC7. Since two bits are not decoded, UC7 produces four identical 8K blocks of memory as opposed to the two identical blocks produced by the ROM address decoder. The address ranges for each 8K block are as follows: $0000\text{-}1FFF_{(hex)}$, $2000\text{-}3FFF_{(hex)}$, $4000\text{-}5FFF_{(hex)}$, and $6000\text{-}7FFF_{(hex)}$. Writing to location $0000_{(hex)}$ produces the same result as writing to locations $2000_{(hex)}$, $4000_{(hex)}$, or $6000_{(hex)}$. The redundant ranges of $2000\text{-}3FFF_{(hex)}$, $4000\text{-}5FFF_{(hex)}$, and $6000\text{-}7FFF_{(hex)}$ are not normally used. UC6 and UC5 combine the 0 and 1 outputs of UC7 to select the 2K RAM, UB2. Table 7-9 illustrates the RAM address range. The 2 through 5 outputs of UC7 are not used. With four images being produced, this leaves the following locations not addressing any devices: $0800\text{-}17FF_{(hex)}$, $2800\text{-}37FF_{(hex)}$, $4800\text{-}57FF_{(hex)}$, and $6800\text{-}77FF_{(hex)}$.

Table 7-9. RAM Images

	A13 = 0, A14 = 0	A13 = 1, A14 = 0	A13 = 0, A14 = 1	A13 = 1, A14 = 1
RAM (UB2)	0000-03FF	2000-23FF	4000-43FF	6000-63FF

The 6 output of UC7 enables the serial bus VIA, UC3. Notice that UC3 decodes A0 through A3. A4 through A9 are not decoded, again producing redundant images. There are 64 images of the 16 VIA registers in the 1024-byte block enabled by UC7. There are also four images of each 1024-byte block that is selected. This gives a total of 256 images of the VIA registers. Typically, the serial bus registers are accessed at $1800\text{-}180F_{(hex)}$ by the DOS.

The 7 output of UC7 is used to enable the disk controller VIA, UC2. Again, this VIA has a total of 256 redundant images. Typically, the disk controller VIA is accessed at $1C00\text{-}120F_{(hex)}$ by the DOS.

7.2.4.5 Write Logic

UC5B and UC6A form the write logic circuit. UC5B inverts the R/W (read/write) line from pin 34 of UC4. The output of UC5B will be high during a write cycle and will be applied to NAND gate UC6A, together with the $\phi 2$ signal from UC5F. The output of UC6A drives the WE (write/enable) line on the RAM chip UB2. The write logic for the VIAs is internal to the VIAs. Therefore, the R/W line and the $\phi 2$ signal are applied directly to the VIA chips.

7.2.4.6 Serial Bus

The serial bus circuits consist of UC3, UD3A, UA1A, UA1B, UA1E, UA1F, UB1A, UB1B, UB1E, UB1F, UD3B, and associated components. The serial bus circuits interface the computer with the serial bus and allow the VIC-1541 to communicate with the VIC 20/Commodore 64. The serial bus circuits also control the reset line for the VIC-1541 computer.

When power is first applied to the VIC-1541, C46 is in a discharged state producing a logic 0 at the input of UD3B. The resulting logic 0 out of UD3B drives the reset line for UC2 and UC4, causing them to assume their initialized states. After a short period of time, C46 will be charged through R25, up to the logic threshold of UD3B. This causes the output of UD3B to change states, placing the reset line high, allowing the computer to start execution of the DOS. If the VIC 20/Commodore 64 is reset, the reset line on the serial bus (pin 6 of P3 and P2) will go low (logic 0). This logic 0 is inverted by UA1A and applied as a logic 1 to the input of UB1A, which discharges C46 to a logic 0. Subsequent action of the reset circuit is as described earlier. CR7 is provided to discharge C46 if power is momentarily removed from the VIC-1541. The reset circuits are active only during power-up of the VIC-1541 or the VIC 20/Commodore 64.

The VIC-1541 serial bus is similar to the IEEE-488 bus (also known as GPIB or HPIB), but it is slower and does not use some of the control signals. Like the IEEE-488 bus, the VIC-1541 bus may be interfaced with several peripherals, each having a unique address. All the peripherals are daisy-chained together. Daisy-chaining means the first peripheral is connected to the computer, the second peripheral is connected to the first, the third peripheral is connected to the second, and so on. Daisy-chaining is the reason the two serial bus connectors, P3 and P2, are wired in parallel. The users of the bus (e.g., VIC 20/Commodore 64, VIC-1541, printers) can be divided into three groups according to their activities at any given instant: controller, talker, and listener.

Only the VIC 20/Commodore 64 may be a controller, talker, and a listener. The peripherals may be either talkers or listeners. The controller dictates bus commands to the peripherals which tell the addressed device whether to talk, listen, untalk, or unlisten. These bus commands are:

Talk—Addresses a specific device and instructs the device to prepare to send data.

Untalk—Addressed device is instructed to cease transmissions.

Listen—Addressed device is instructed to prepare to receive data.

Unlisten—Addressed device is instructed to ignore any further data transmissions. Device will wait for next command.

These bus commands are sent as an 8-bit byte. Five of the bits are used for the address and the others are used for the command definition. A total of 28 devices may be addressed by the serial bus. However, even though the address range of the serial bus is 4 through 31, it can only drive five loads at any given time.

CAUTION

Connecting more than five devices to the serial bus could result in permanent damage to the serial bus circuits.

Applicable bus signals used by the VIC-1541 are:

SER CK—Primarily used to indicate that data is valid on the serial data line. Also used as a ready to send signal.

SER DATA—Primarily used to carry data bits. Also used as cleared to send, EOI acknowledge, and handshaking signal.

SER ATN—When false, serial data contains data to be transferred. When active, it indicates that the data bus contains a command. Only the controller may drive this line.

All of these signals are active low signals. The signal lines are driven by open collector outputs, allowing all the peripherals to be write-ORable. That is, any or all of the devices may drive the bus lines at the same time. If any device pulls a bus line active (low), the result will be an active line. In order for a line to be inactive (high), all peripherals must release the line to high.

Refer to Fig. 7-31 for a typical data transmission signal. Prior to T0, the bus is in its standby state, the serial clock line is held low by the talker, and the data line is held low by the listener. The SER ATN line is high, indicating the transmission to take place is data rather than a command. At T0, the talker signals "ready to send" by releasing the clock line. At T1, the listener acknowledges the "ready to send" by signaling "clear to send." The listener signals "clear to send" by releasing the clock line to a logic high. If the listener is busy, it will not signal "clear to send." The time between T0 and T1 is undefined and is determined by the listener. Within 200 microseconds, the talker pulls the clock line low at T2. At some time between T2 and T3, the talker places the least significant bit on the SER DATA line. Since the bus lines are active low, the data appears inverted. That is, a low represents a "true" bit. At T3, the clock line is released to logic 1, indicating to the listener that the data bit on the SER DATA line is valid. The talker holds this condition until T4, where the talker releases the data line to a logic 1 and pulls the clock line low. This sequence continues until T18. After clocking in the most significant bit at T17, the talker once again pulls the clock line low and releases the data line at T18. Now the talker is waiting for the handshake signal which occurs at T19. At T19, the listener pulls the data line low. After T19, the serial bus is back in its standby condition, as it was prior to T0. Throughout the transmission of this byte, the talker keeps control of the clock line. The talker has control of the data bus from T2 to T18 only. The rest of the time the listener uses the data line for handshaking. Data transfers continue in this fashion until the last byte to be transferred. The last byte to be transferred contains "end or identify" handshaking.

The handshaking signal for "end or identify" takes place between T1 and T2 (refer to Fig. 7-32 for "end or identify" information). The talker signals

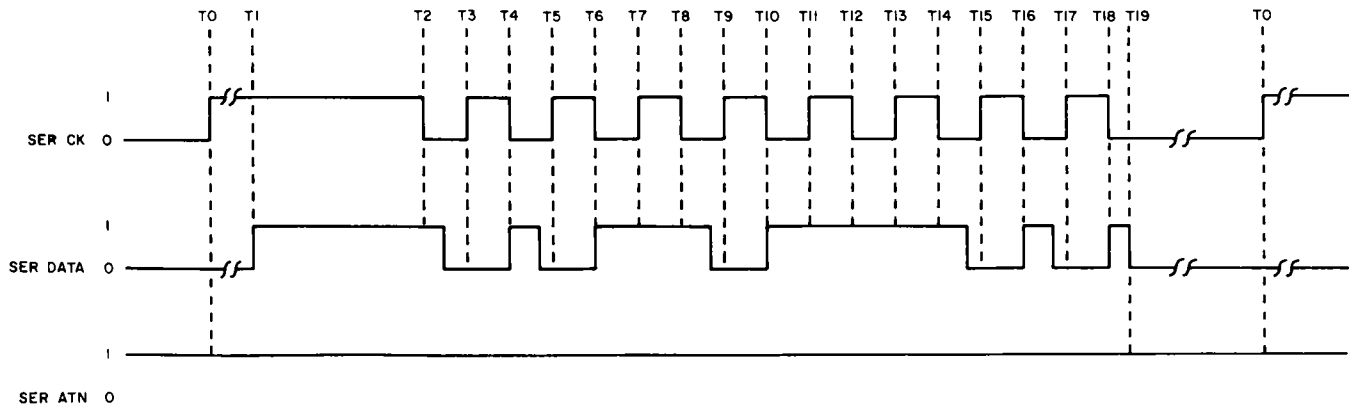


Fig. 7-31. Typical data transmission.

"end or identify" by not pulling the clock line low for at least 200 microseconds. After approximately 200 microseconds, the listener acknowledges the "end or identify" at T1A by pulling the serial data line low. At T1B, the listener releases the SER DATA line to logic 1, informing the talker to transmit the last byte. At T2, the talker pulls the clock line low and the byte is transmitted. At some time after T19, the talker and the listener release the clock and data lines, respectively. These actions occur at T20.

A bus command is transmitted in the same manner as bus data, except that the SER ATN line is pulled low during the transmission. When a bus command is being transferred, the VIC 20/Commodore 64 is the bus controller and all the peripherals on the line become listeners. After the bus command, a secondary address may also appear. The secondary address is optional and is used to control and specify a subchannel. After the bus command is issued, the addressed device assumes the role issued by the bus command. Usually, the VIC 20/Commodore 64 assumes the opposite role. For example, if a talk command is issued the computer assumes the role of the listener. All the devices on the bus that are not involved with the transfer of data release control of the bus lines and await the next command (i.e., SER ATN pulled low). It is possible for the controller to issue a listen command to one peripheral and a talk command to another peripheral, causing data to be transferred between two peripherals while the VIC 20/Commodore 64 is free to perform other tasks. Such a possibility is difficult to accomplish, but the VIC-1541 bus is capable of doing so.

UA1B is the line receiver for the serial clock line. The output of UA1B is entered into the serial bus VIA, UC3. When the VIC-1541 is a talker, it takes control of the serial clock line using port B, bit 3 (pin 13, UC3) of the serial bus VIA. When pin 13 of UC3 goes high, UB1E pulls the clock line active. UB1 has open collector outputs.

UA1E is the line receiver for the SER DATA line. The data is inverted and applied to the serial bus VIA. The SER DATA line is driven in the write mode by UB1F. The serial-to-parallel and parallel-to-serial conversions are performed by the software.

UA1F is the line receiver for the SER ATN line. The output of UA1F is applied to pin 40 of UC3, generating an interrupt to the computer. The output is also applied to pin 17 to allow the computer to sample the state of the SER ATN line. When the SER ATN line is active, the SER DATA line is pulled low by UD3A and UB1E. The VIC-1541 releases the data line by using the other input (pin 1) of the Exclusive OR gate, UD3A.

E1 and E2 set the address of the VIC-1541. Refer to Chapter 1 for instructions on configuring E1 and E2.

UC3 is a versatile interface adapter (VIA) containing two parallel ports, interrupt logic, and two 16-bit counters, all of which are accessible to the computer through the data bus.

7.2.4.7 Disk Controller VIA

UC2, the disk controller VIA, has two 8-bit ports which are used to interface with the timing, read, write, encoder/decoder, track select, and optics circuits. UC2 also contains interrupt logic and two 16-bit counters that may be accessed by the computer.

7.2.5 Track Select Electrical Theory (Refer to Figs. 7-33 and 7-34)

The track select circuit consists of UC1, UD1B, UD1C, UD1D, UD1E, and Q8 through Q11. UC1

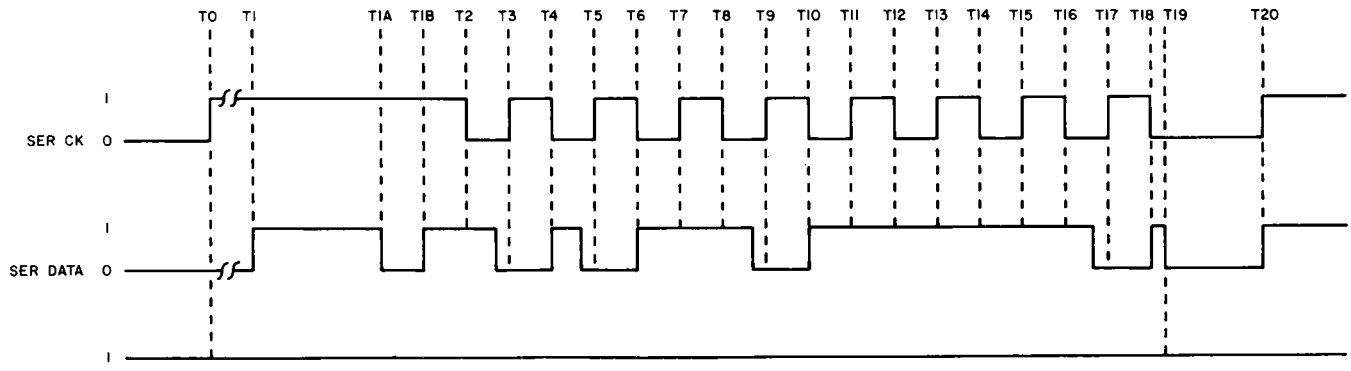


Fig. 7-32. End or identify.

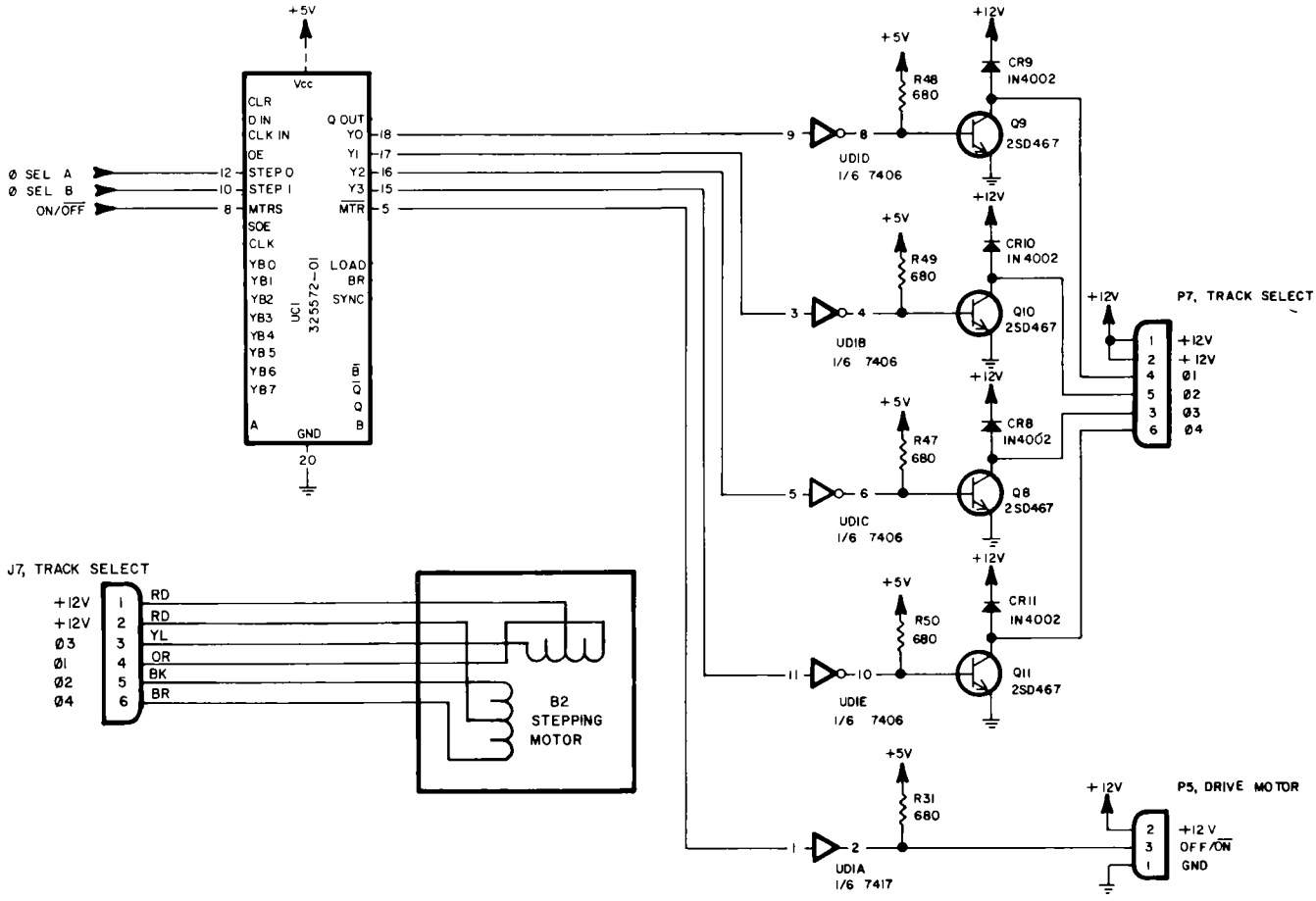


Fig. 7-33. Schematic of track select circuit, Model 1541.

pulls the selected Y(N) output low. To step inward (increasing track number), the four Y(N) lines must be clocked in ascending order (i.e., 1, 2, 3, 4, 1, 2 . . .). To step outward, the Y(N) lines must be clocked in descending order (i.e., 4, 3, 2, 1, 4, 3 . . .). Each of the Y(N) outputs is buffered by a NOT gate (UD1B through UD1E) and a transistor (Q8-Q11) configured as a common-emitter buffer. The windings of B2 (the stepping motor) form the collector loads for Q8-Q11. CR8-CR11 clip any overshoot produced by the inductive characteristics of the windings of B2.

When a logic 1 is applied to pin 8 of UC1 (ON/OFF line), the Y0 through Y3 outputs of UC1 are enabled. When a logic 0 is applied to pin 8 of UC1, the outputs are disabled and none of the Y(N) lines are driven.

Internally, UC1 buffers the enable signal for UD1A and applies this signal to the motor driver servo circuit. Since the motor enable and step enable controls are both accomplished with the same line, tracks can only be changed while the drive motor (B1) is running. Table 7-10 illustrates the relationship between the ON/OFF, ϕ SEL A, and ϕ SEL B lines and the ϕ1, ϕ2, ϕ3, ϕ4, and OFF/ON lines.

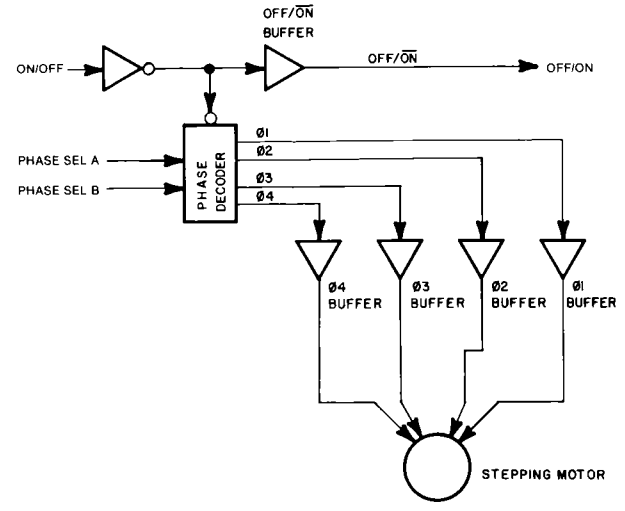


Fig. 7-34. Block diagram of track select circuit, Model 1541.

Table 7-5. Track Select Truth Table

ON/OFF	ϕ SEL A	ϕ SEL B	ϕ1	ϕ2	ϕ3	ϕ4	OFF/ON
0 V	X	X	+12 V	+12 V	+12 V	+12 V	+5 V
+5 V	0 V	0 V	0 V	+12 V	+12 V	+12 V	0 V
+5 V	+5 V	0 V	+12 V		+12 V	+12 V	0 V
+5 V	0 V	+5 V	+12 V	+12 V	0 V	+12 V	0 V
+5 V	+5 V	+5 V	+12 V	+12 V	+12 V	0 V	0 V

To get a more comprehensive understanding of the internal operation of UC1, see Section 7.1, "Advanced Theory, Model 1540." UC1 is essentially a custom IC that contains the discrete ICs used in the 1540. Also see Appendix E.

7.2.6 Drive Motor System Electrical Theory (Refer to Figs. 7-35 and 7-36)

The purpose of the drive motor system is to maintain the disk at a constant speed. The drive motor system consists of the drive motor servo circuit and the drive motor/tachometer.

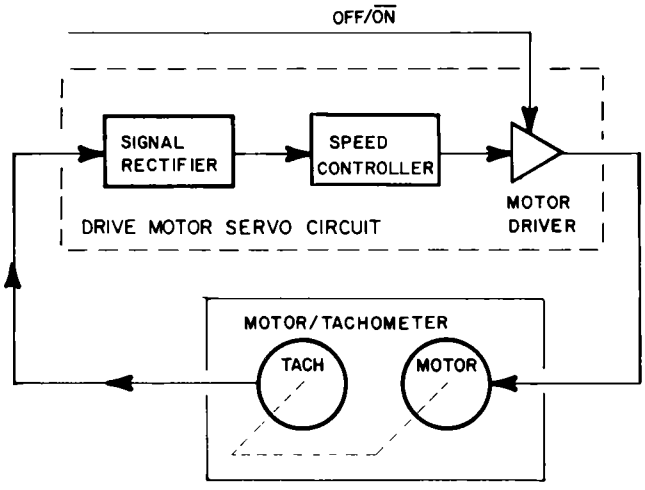


Fig. 7-35. Block diagram of drive motor system, Model 1541.

7.2.6.1 Drive Motor/Tachometer

The drive motor/tachometer contains a dc permanent magnet motor and a tachometer on a common shaft. The tachometer acts as a low-power ac generator. The voltage output of the tachometer increases with increasing drive speed and provides feedback to the drive motor servo circuit. This feedback contains motor speed information that the drive motor servo circuit uses to determine how hard to drive the motor. The drive motor servo circuit adjusts the motor current as necessary to maintain a constant speed of 300 rpm. This is necessary because each floppy disk may offer different mechanical loads to the motor, due to manufacturers' differences or age of the disk.

7.2.6.2 Drive Motor Servo Circuit

Tachometer information enters the drive motor circuit at E4 and E5. This information, a sine wave, is rectified by the bridge rectifier consisting of CR1 through CR4. R1 provides a load for the tachometer. The output of the rectifier is applied to pin 1 of IC1.

IC1 is the speed controller. Power is supplied through a low-pass filter (R3 and C5). C2 is also provided for filtering. R2, R10, and VR1 determine the speed of the floppy disk. VR1 is used to calibrate disk speed. C3 and C6 provide filtering. The output of IC1 (pin 5) will increase if the voltage at pin 1 is less than the threshold set by VR1. Conversely, the output at pin 5 will decrease if the voltage at pin 1 is greater than the voltage set by VR1. The circuit will settle when the feedback at pin 1 is equal to the threshold set by VR1. The output of the speed controller (IC1, pin 5) is applied to the motor driver.

The motor driver consists of Q1 through Q4, R4 through R9, C4, and C7 through C9. Q2 is an inverting dc amplifier. C4 provides filtering. R4 limits base current. The combination of Q1, CR5, and R7 enables or disables Q2. A logic low at E2 turns off Q1, allowing Q2 to operate normally. A logic high at E2 turns on Q1, shutting off Q2 by shunting its base current to ground and thus shutting off the motor. Q4 is the final pass transistor. When its base is pulled low by Q2, through R6, it will conduct harder. As Q2 increases in conduction, Q4 will proportionately increase its own conduction. R9 and Q3 form a current limiter. As emitter current in Q4 increases, the voltage drop across R9 increases. When the drop across R9 reaches approximately 0.65 volt, Q3 will conduct. When Q3 starts conducting, it shunts some of the bias current for Q4 to the positive supply. Q3 will shunt enough bias for

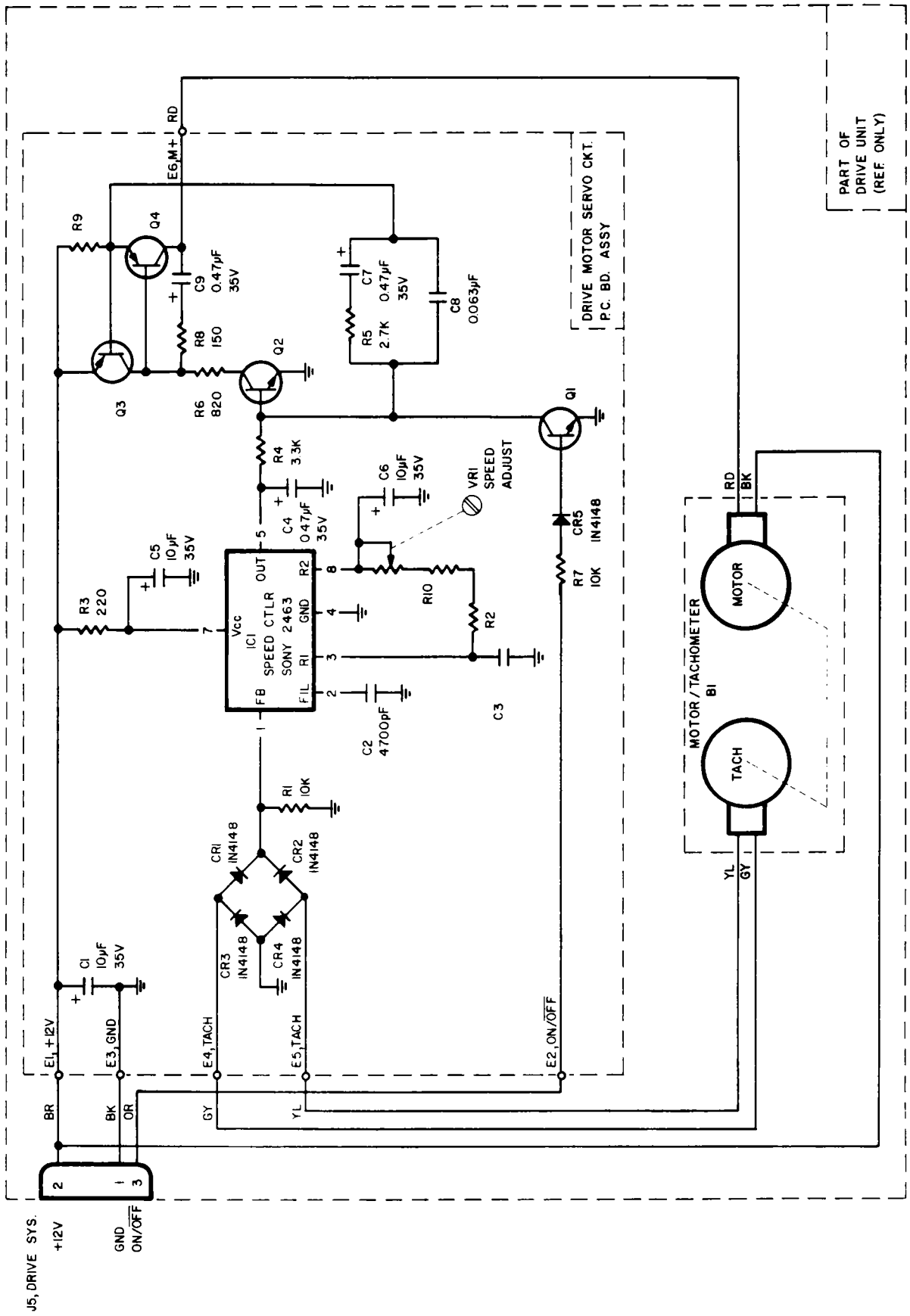


Fig. 7-36. Schematic of drive motor system, Model 1541.

Q4 to maintain motor current at a safe level for B1 (the drive motor). C7 through C9, R5, and R8 control the slew rate and noise of the motor driver. The collector of Q4 is tied to the drive motor/tachometer to complete the servo loop. C1 is provided to bypass noise from the +12-volt supply.

7.2.7 Write Circuit Electrical Theory (Refer to Figs. 7-37 and 7-38)

The write circuit consists of the following major blocks: write logic, bias switch, amp enable switch, differential write amp, and the diode switch.

7.2.7.1 Write Logic

The write logic consists of UA1C and UC1. UA1C inverts the write protect signal and applies this signal to UC1 and to the disk controller VIA. When the output of UA1C is high, the write protect notch is uncovered. UC1 gates the read/write line only when the write protect input (pin 6) is high. When gated, the B output of UC1, pin 2, is low. This line turns on the amp enable switch. Additionally, when writing is enabled, the B output of UC1, pin 40, is high; this is applied to the bias switch. For more information concerning UC1, see Appendix E.

7.2.7.2 Bias Switch

During a write operation, the bias switch applies current through the bias winding (U1L2) in the read/write head. One side of the bias switch, Q6, drives the positive side of the bias winding. Q6 is gated into conduction by the input of UD2F, which is low when writing. The other side of the bias switch, Q7, drives the negative side of the bias winding. Q7 is driven into conduction by the input of UD2E, which is high when writing. Bias current flows through U1L2 via Q6, R51, Q7, CR12, and CR14 (both diodes are forward biased).

7.2.7.3 Amp Enable Switch

The amp enable switch consists of Q3 and UD2B. A low is applied to UD2B while writing, driving Q3 into conduction. When Q3 is conducting, power is applied to the differential write amp.

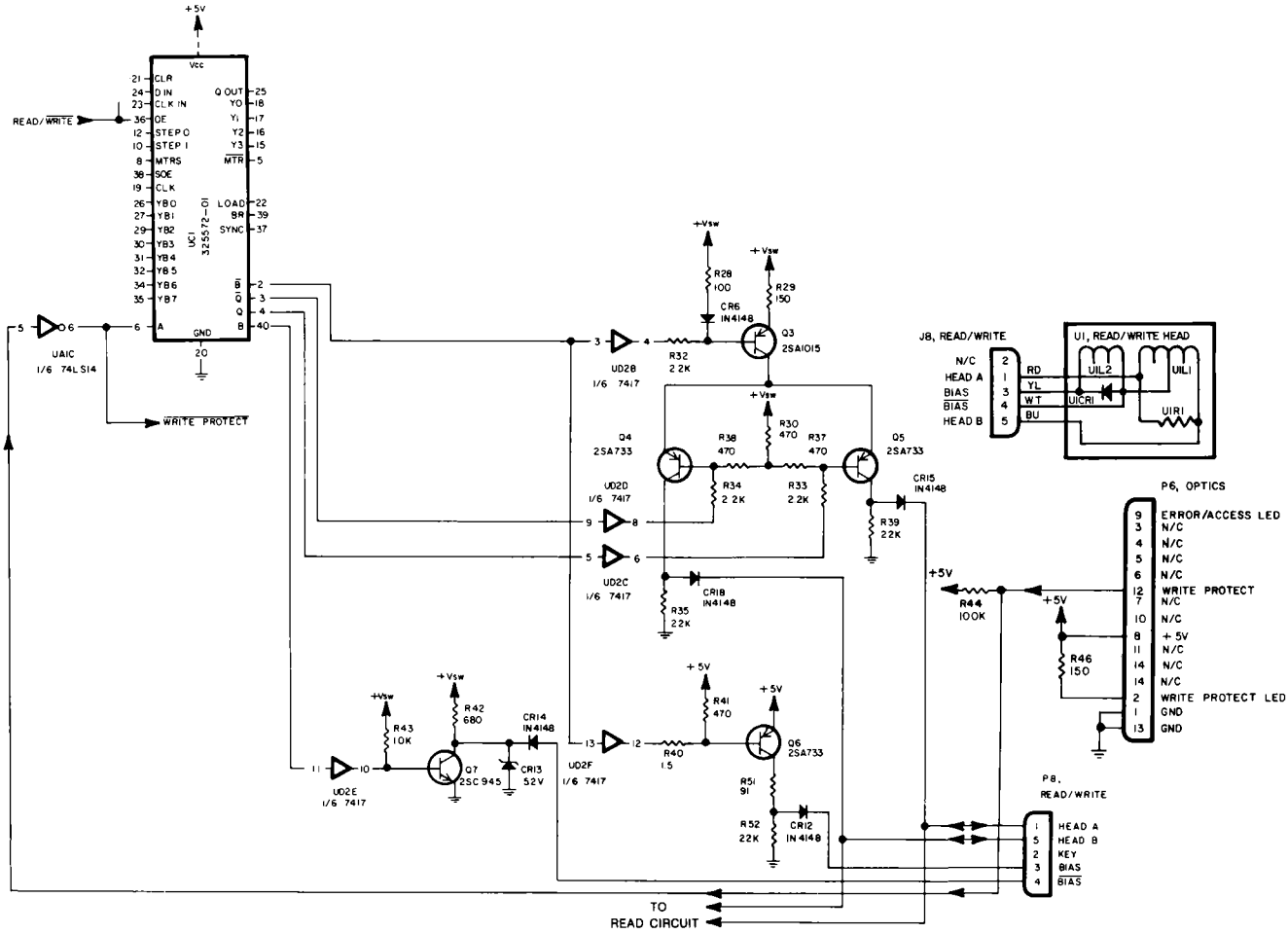


Fig. 7-37. Schematic of write circuit, Model 1541.

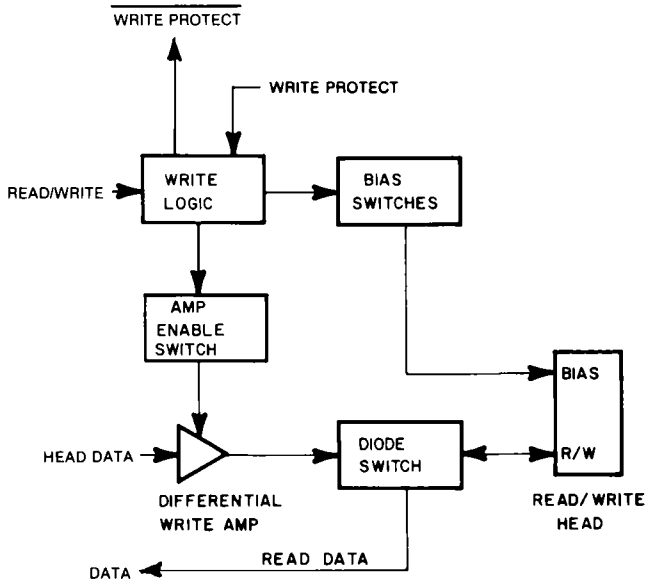


Fig. 7-38. Block diagram of write circuit, Model 1541.

7.2.7.4 Differential Write Amp

The differential write amp consists of UD2C, UD2D, Q4, and Q5. UD2C and UD2D are driven by the encoder/decoder and, in turn, drive the differential transistor pair, Q4 and Q5. When Q5 is conducting, Q4 is turned off. When Q4 is conducting, Q5 is turned off. The outputs of the differential write amp are applied to the read/write head via the diode switch.

7.2.7.5 Diode Switch

The diode switch consists of CR15 and CR18. When in the write mode, the center tap of the read/write winding (U1L1) is at ground potential because of bias switch Q7 and CR14. When Q7 goes into conduction, current flows through the read/write winding via either Q4, CR18, CR14, and Q7 or via Q5, CR15, CR14, and Q7, depending upon the state of the differential write data from the encoder/decoder circuit.

7.2.8 Read Circuit Electrical Theory (Refer to Figs. 7-37, 7-39, and 7-40)

The read circuit senses and amplifies data from the floppy disk. The amplified data is checked for valid pulse widths to improve noise immunity. The output of the read circuit is a narrow pulse which occurs on both the rising and falling edges of the data.

The read circuit does not care if the data is high or low. Only the positions of the transitions are significant. The data is divided into cells. If a transition occurs at the beginning of a cell, the cell is interpreted as a logic 1. If no transition occurs, the cell is interpreted as a logic 0.

The data is sensed by the read/write head and applied to the first video amplifier (UF3) via the diode switch (see Fig. 7-37). When in the read mode, Q3, Q6, and Q7 are not conducting. CR16 and CR17 are forward biased via the read/write winding (U1L1), CR14 (which is also forward biased), and CR13 (a 5.2-volt zener diode). The cathodes of CR16 and CR17 are at approximately +6 volts, causing the data to be applied to the first video amplifier (UF3). The +6-volt bias is applied to the cathodes of CR18 and CR15.

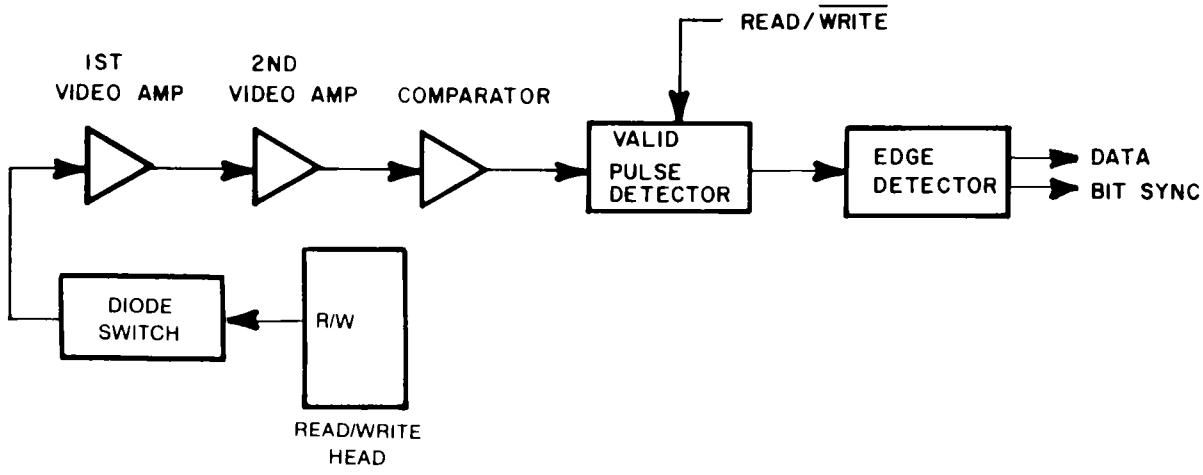


Fig. 7-39. Block diagram of read circuit, Model 1541.

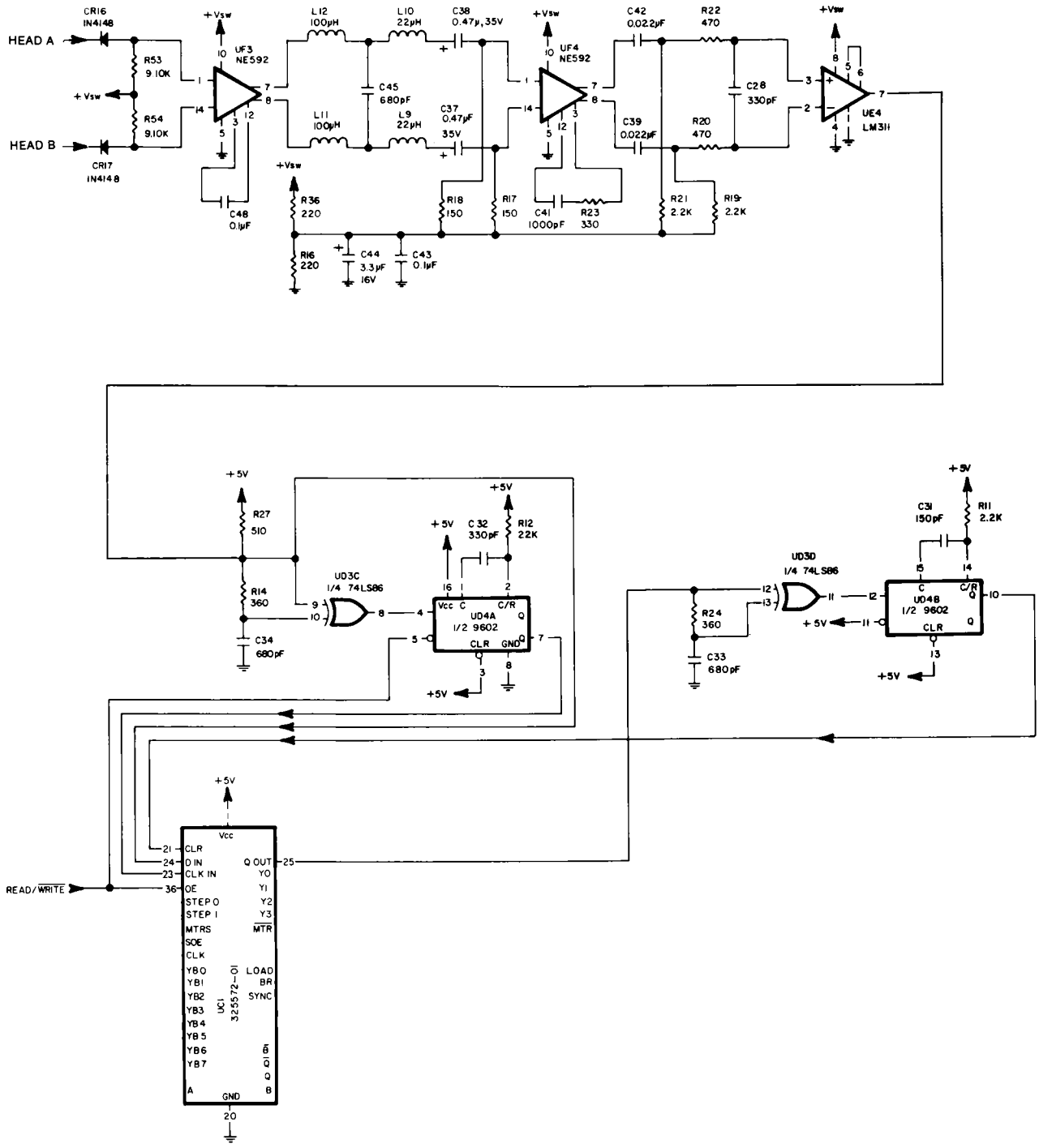


Fig. 7-40. Schematic of read circuit, Model 1541.

Since Q3 is not conducting, R35 and R39 pull the anodes of CR18 and CR15 to ground, causing CR18 and CR15 to be reverse biased and isolating the write circuit from the read circuit. CR12 is also reverse biased, since the +6-volt bias on the cathodes of CR16 and CR17 is applied to the cathode of CR12 via the read/write winding (U1L1) and the bias winding (U1L2).

The output of UF3, the first video amplifier (see Fig. 7-40), is applied to a low-pass filter formed by L9 through L12 and C45. C37 and C38 block the dc offset out of UF3 to prevent the offset from disturbing the input bias to UF4. R16 and R36 set a bias voltage of +6 volts, which is filtered by C43 and C44 and applied to the input signal of UF4 via R18 and R17. The output of UF4 is ap-

plied to the comparator via C42, C39, R20, and R22. C42 and C39 block the dc offset out of UF4 to prevent the offset from affecting the bias on the input signal of the comparator, UE4. A +6-volt bias is applied to the input signal of the comparator from R16 and R36 via R19 and R21.

The output of the comparator is applied to the valid pulse detector (UD3C, UD4A, and UC1). UD4A, along with C34, R14, and R27, forms an edge detector. Pin 8 of UD3C will produce a 500-nanosecond active high pulse on rising edges of the comparator's output and will produce a 150-nanosecond active high pulse on falling edges of the comparator's output. The pulse out of UD3C is applied to UD4A, a single-shot multivibrator. UD4A produces an active low pulse which is approximately 2.5 microseconds wide. A flip-flop in UC1 is clocked on the trailing edge of the output pulse of UD4A. The output of the comparator must be maintained for at least 2.5 microseconds in order to be latched into the flip-flop. If a narrow noise pulse triggers this circuit, the output of the flip-flop will not change since the noise pulse will terminate before UD4A triggers the flip-flop in UC1. The output of UC1, pin 25, will reflect the data delayed by approximately 2.5 microseconds.

The valid data out of the valid pulse detector part of UC1 is applied to an edge detector consisting of UD3D and UD4B. UD3D operates the same as UD3C above. The pulses out of UD3D trigger UD4B, a single-shot multivibrator. UD4B produces a narrow pulse which represents transitions of the data. This output is applied to the timing circuit via UC1 to synchronize the encoder/decoder clock, and to the encoder/decoder, which will detect the data and perform a serial-to-parallel conversion. Notice that pin 5 of UD4A is connected to the read/write line, causing the valid pulse detector to be disabled during a write operation.

The video amplifiers will often oscillate with no data in, but these oscillations are high enough in frequency that they seldom get past the valid pulse detector.

7.2.9 Encoder/Decoder Electrical Theory (Refer to Fig. 7-41)

The encoder/decoder is fully integrated into UC1 on Models 1541 and 1542. The encoder/decoder decodes the serial data which is applied to pin 21. Both data and sync information are separated internally. The separated data is converted to eight parallel bits which are available on pins 26, 27, 29, 30, 31, 32, 34, and 35. Three sync signals are also provided: bit sync, pin 22; byte sync, pin 39; and block sync, pin 37. In order to decode data the read/write input, pin 36, must be high.

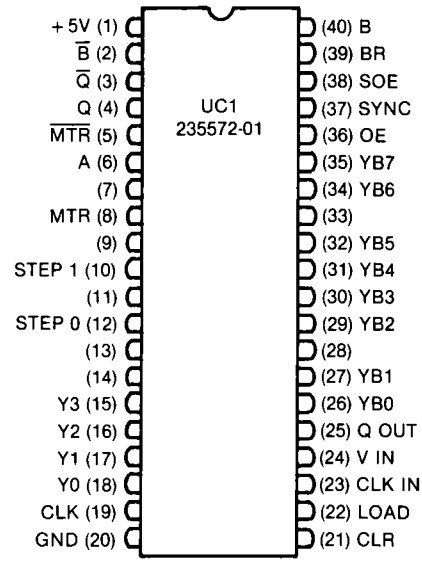


Fig. 7-41. Disk controller integrated circuit, Model 1541.

When encoding data, the read/write input, pin 36, and write protect input, pin 6, must both be high. When encoding data, eight parallel bits are applied to pins 26, 27, 29, 30, 31, 32, 34, and 35. The encoder/decoder converts this byte to serial data which is encoded into transitions. The differential encoded data is available at pins 3 and 4. The bit sync and byte sync outputs are available during encoding.

All timing for the encoder/decoder is derived from the encoder/decoder clock, pin 17. The remaining pins on UC1 are dedicated to other disk controller functions. For more information concerning UC1 see Appendix E and encoder/decoder theory for Model 1540, Section 7.1.9.

7.2.10 Optics Circuit Electrical Theory (Refer to Figs. 7-42 and 7-43)

The optics circuits consist of DS1 on the case assembly; DS1, CR1, and Q1 on the drive unit; and UD1F, R46, R45, R55, and R44 on the disk controller PC board.

R55 provides current limiting for the power LED, DS1 on the case assembly. R46 provides current limiting for CR1, the optical transmitter, on the drive unit. Both CR1 on the drive unit and DS1

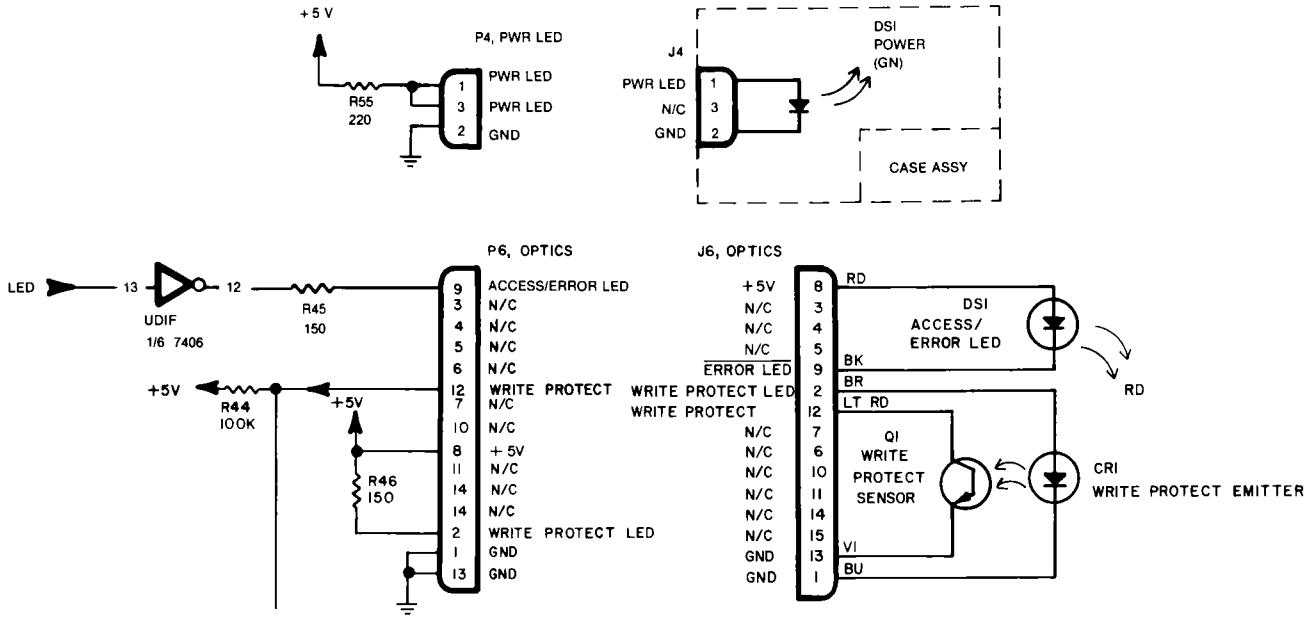


Fig. 7-42. Schematic of optics circuit, Model 1541.

on the case assembly turn on as soon as the +5-volt line becomes active (power on). The optical receiver, Q1 on the drive unit, is positioned under CR1 in such a manner that the write protect notch is directly between them when the floppy disk is seated. Q1 on the drive unit conducts (produces a logic 0) when the write protect notch is left uncovered (writing permitted). When the write protect notch is covered, Q1 on the drive unit does not conduct (logic 1). The write protect output of the optical receiver is available on pin 12 of P6 and is applied to the write circuit. UD1F drives the access/error LED. A high on the LED line causes DS1 on the drive unit to illuminate. R45 limits the current through DS1.

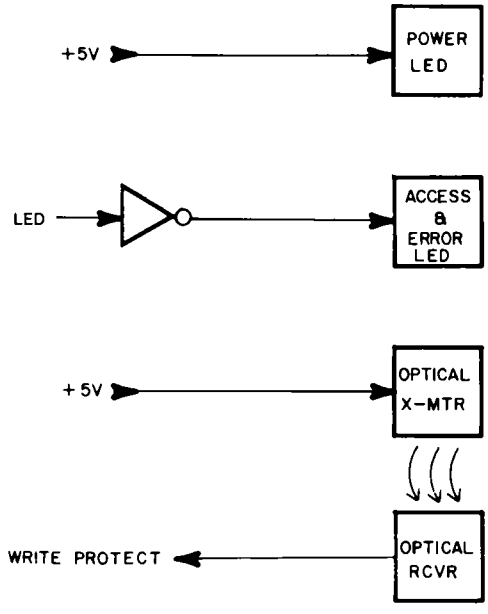


Fig. 7-43. Block diagram of optics circuit, Model 1541.

7.3 ADVANCED THEORY, MODEL 1542

Model 1542 is closely related to Model 1541. This section covers the minor differences between Models 1541 and 1542. If you are troubleshooting Model 1542, please read section 7.2, "Advanced Theory, Model 1541," before proceeding.

With only a few exceptions, the schematic for Model 1542 is identical to the schematic for Model 1541; even the reference designators are the same. Only the computer circuit and the drive motor servo circuit differ.

7.3.1 Computer Circuit

The computer's address decoder for the ROM, RAM, and VIAs have different reference designators in Model 1542 than they did in Model 1541. UC5 on Model 1541 has been changed to UC6 on Model 1542. UC6 on Model 1541 has been changed to UC7 on Model 1542, and UC7 on Model 1541 has been changed to UC8 on Model 1542. For these circuits, the only change is the ref-

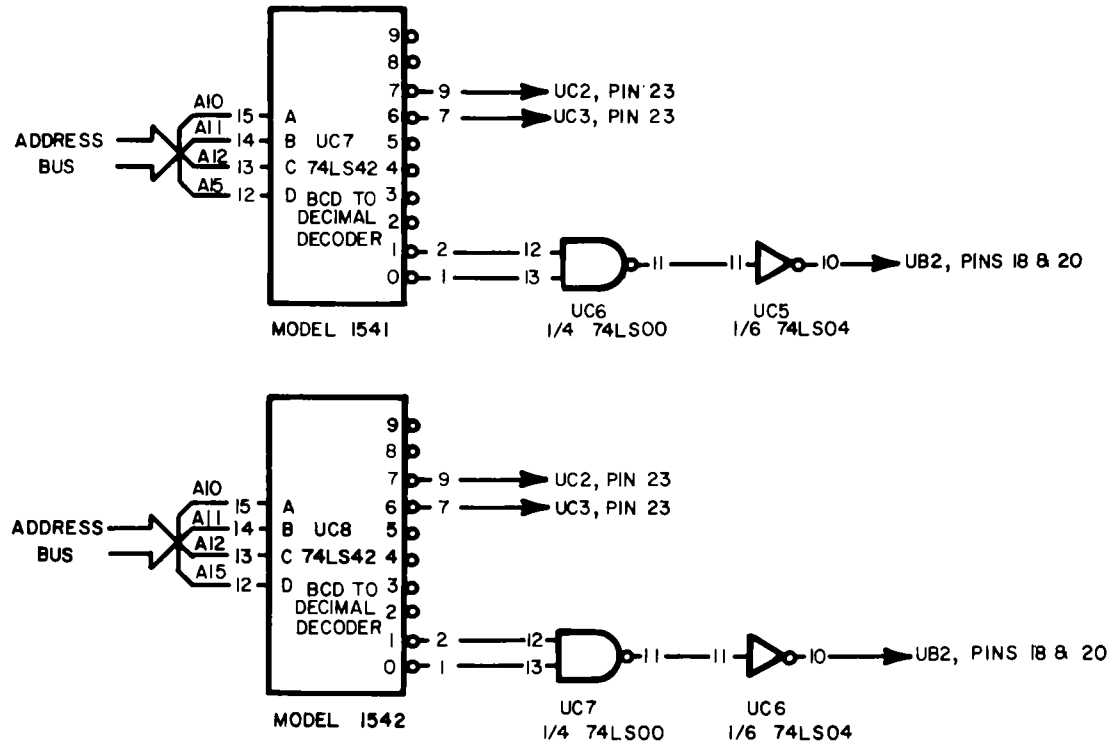


Fig. 7-44. RAM/VIA address decoder changes, Model 1542.

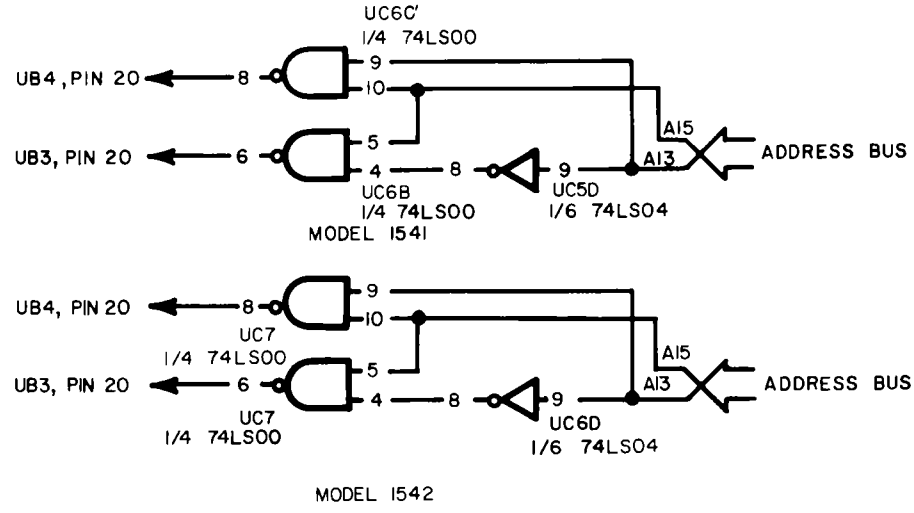


Fig. 7-45. ROM address decoder changes, Model 1542.

erence designator, as even the pin numbers remain the same. This change is illustrated in Figs. 7-44 and 7-45.

The computer's write circuit changed from Model 1541 to Model 1542 (see Fig. 7-46). In addition to the reference designator changes, pins 1 and 2 on the NAND gate (UC7, Model 1542) have been swapped. The inverted read/write line is applied to pin 2 on Model 1542 instead of pin 1 on Model 1541. Also, the $\phi 2$ signal is applied directly to the NAND gate from pin 39 of UC4 on Model 1542 instead of going through the two buffers first as it did on Model 1541. Functionally, there is no difference between Models 1541 and 1542 concerning this change.

The reset circuit on Model 1542 has been changed to provide a sharper edge to the reset signal. An inverter with a Schmitt trigger input has been added between C46 and UD3B. Also, UD3B is configured as a noninverting buffer in Model 1542 instead of being configured as an inverter in Model 1541 (see Fig. 7-47).

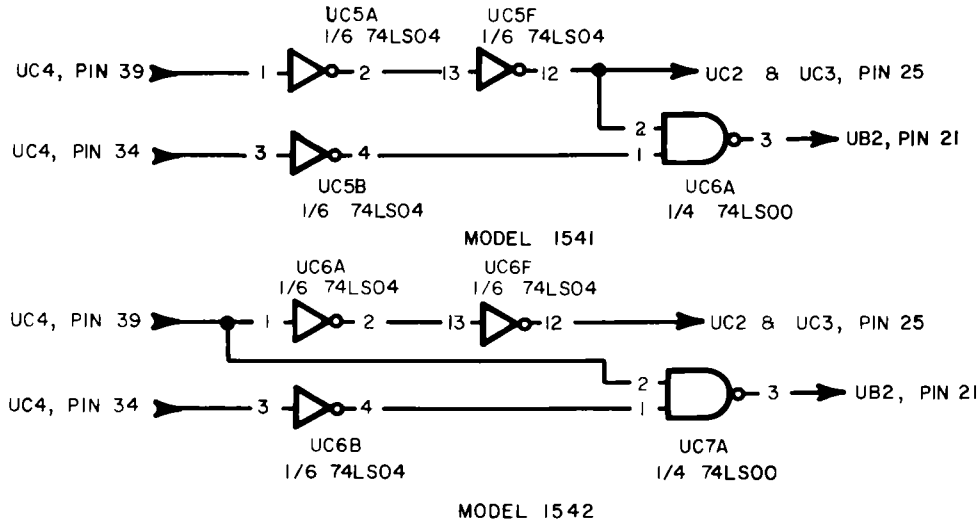


Fig. 7-46. Write logic changes, Model 1542.

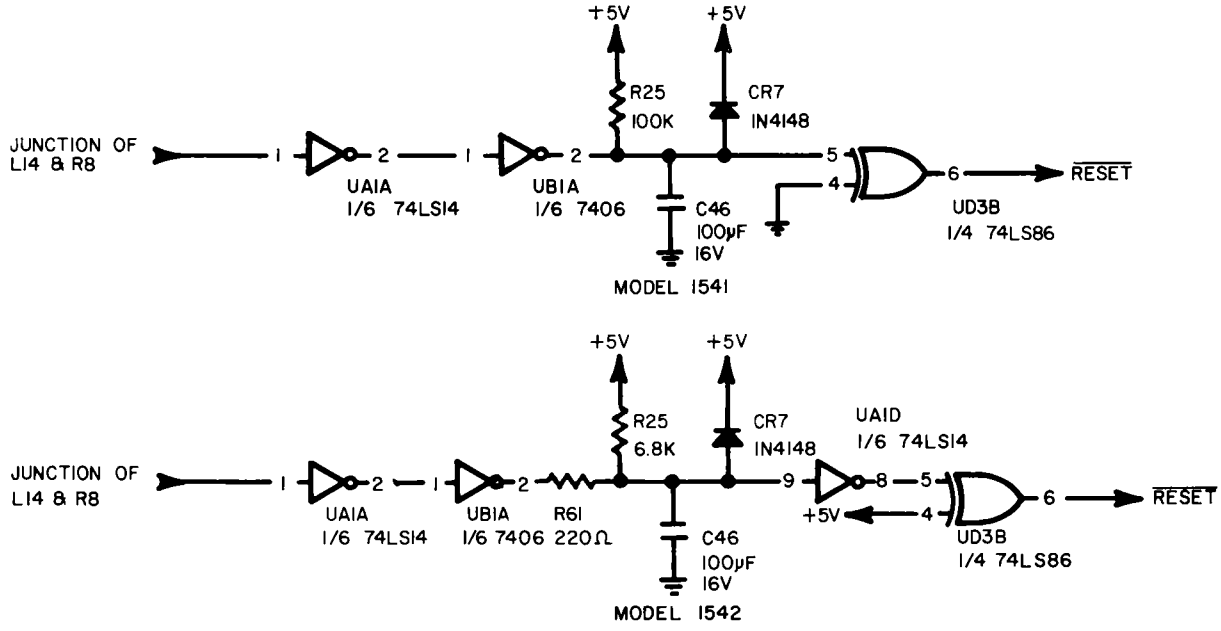


Fig. 7-47. Reset circuit changes, Model 1542.

7.3.2 Drive Motor Servo Circuit (Refer to Figs. 7-48 and 7-49)

The drive motor servo circuit in Model 1542 is drastically different from the drive motor servo circuit used in Model 1541. Although input and output signals are the same, the two drive motor servo circuits use different ICs to control motor speed. The following discussion applies to the drive motor servo circuit on Model 1542 (Newtronics drive unit).

Tachometer information from the drive motor/tachometer enters the drive motor servo circuit at E4 and E5. This information is applied to R1 and R2, which form a voltage divider as well as a load for the tachometer. From the voltage divider, the tachometer information is coupled to IC1, the governor, via coupling capacitor C1. IC1 compares this information with a speed standard set by VR1, R3, R4, C2, and C10.

The output of IC1, pin 11, drives the motor control transistor TR2 via R7. TR1 in turn drives the drive motor/tachometer. If the tachometer information indicates that the motor is turning too slow, then IC1 will drive TR2 harder. If, on the

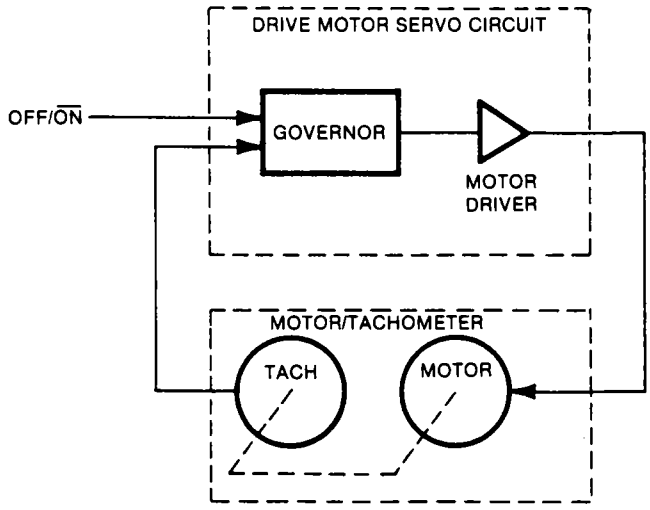


Fig. 7-48. Block diagram of drive motor servo circuit, Model 1542.

other hand, the tachometer information indicates that the motor is turning too fast, IC1 will reduce the drive current to TR2. TR1 and R10 provide current limiting for the drive motor. When approximately 1 ampere is being drawn by the motor through R10 and TR2, TR1 will turn on, causing the drive current for TR2 to be shunted around the base-emitter junction of TR2 via TR1. The governor is disabled (motor turned off) when pin 8 of IC1 is high. When pin 8 of IC1 is low, the governor is enabled (motor turned on). C3, C5, and R5 filter the +12-volt supply line to IC1. R6, R8, C4, C6, and C7 sample motor current changes and provide this information to pins 10 and 12 of IC1.

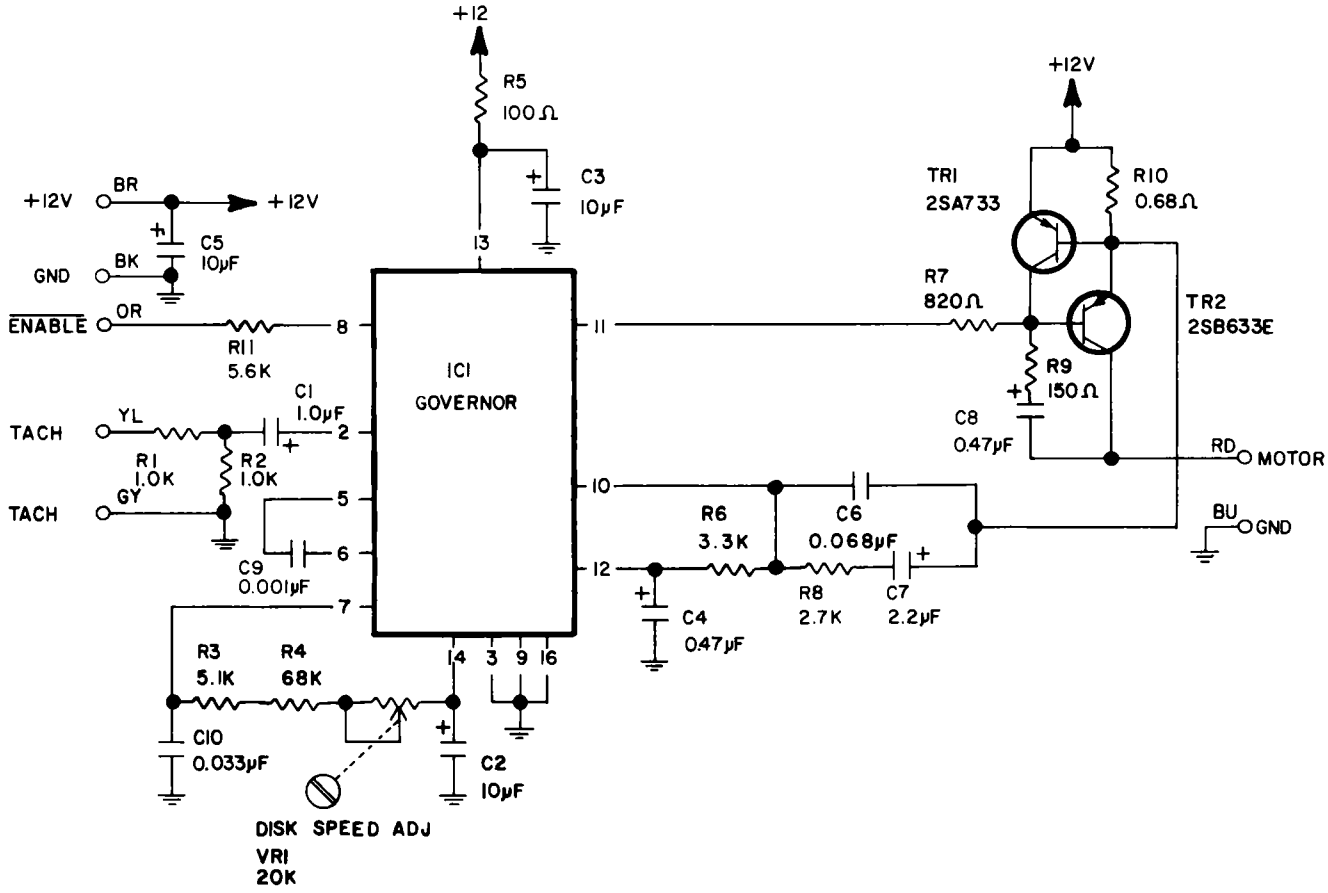


Fig. 7-49. Schematic of drive motor servo circuit, Model 1542.

APPENDIX A

Technical Data

This appendix provides technical data for the VIC-1541. Included in this appendix are an index, interconnect diagrams, schematics, parts layouts, and parts lists.

The interconnect diagrams illustrate how the various connectors are arranged in the VIC-1541. When tracing a signal to a connector, the interconnect diagram illustrates which subassembly is plugged into that connector. Once the subassembly is identified on the interconnect diagram, the schematic for that subassembly may be consulted. The signal-tracing process may then continue to the next schematic. The interconnect diagram is a means of linking the individual schematics together.

The block diagram is a composite simplified explanation of how the individual circuits are logically arranged.

The schematic diagrams illustrate how all of the components are electrically connected. Reading a schematic diagram can be an art in itself. Some people might not be able to get much information from a schematic, while those with a lot of experience could get enough information from a schematic to almost make the rest of the information in this book redundant. If you are interested in learning more about reading schematics, the following book is recommended:

How to Read Schematics, 4th Ed., by Donald E. Herrington. Howard W. Sams & Co., 1986. (Cat. No. 22457)

The parts layouts are simply maps that can be used to locate a part in question. Although most parts are labeled on the PC board, these labels may become illegible due to dirt, wear, or age. If a reference designator is illegible or a part is not labeled (such as motors or LEDs), consult the appropriate parts layout.

Like the parts layouts, the parts lists are provided in the event that a part number or color code becomes illegible due to burns, dirt, or wear. If you cannot read a part number, consult the appropriate parts list.

Section A.1 provides an index to individual figures and lists contained in this appendix.

A.1 INDEX TO TECHNICAL DATA

Interconnect Diagrams

Schematics

Parts Layouts

Parts Lists

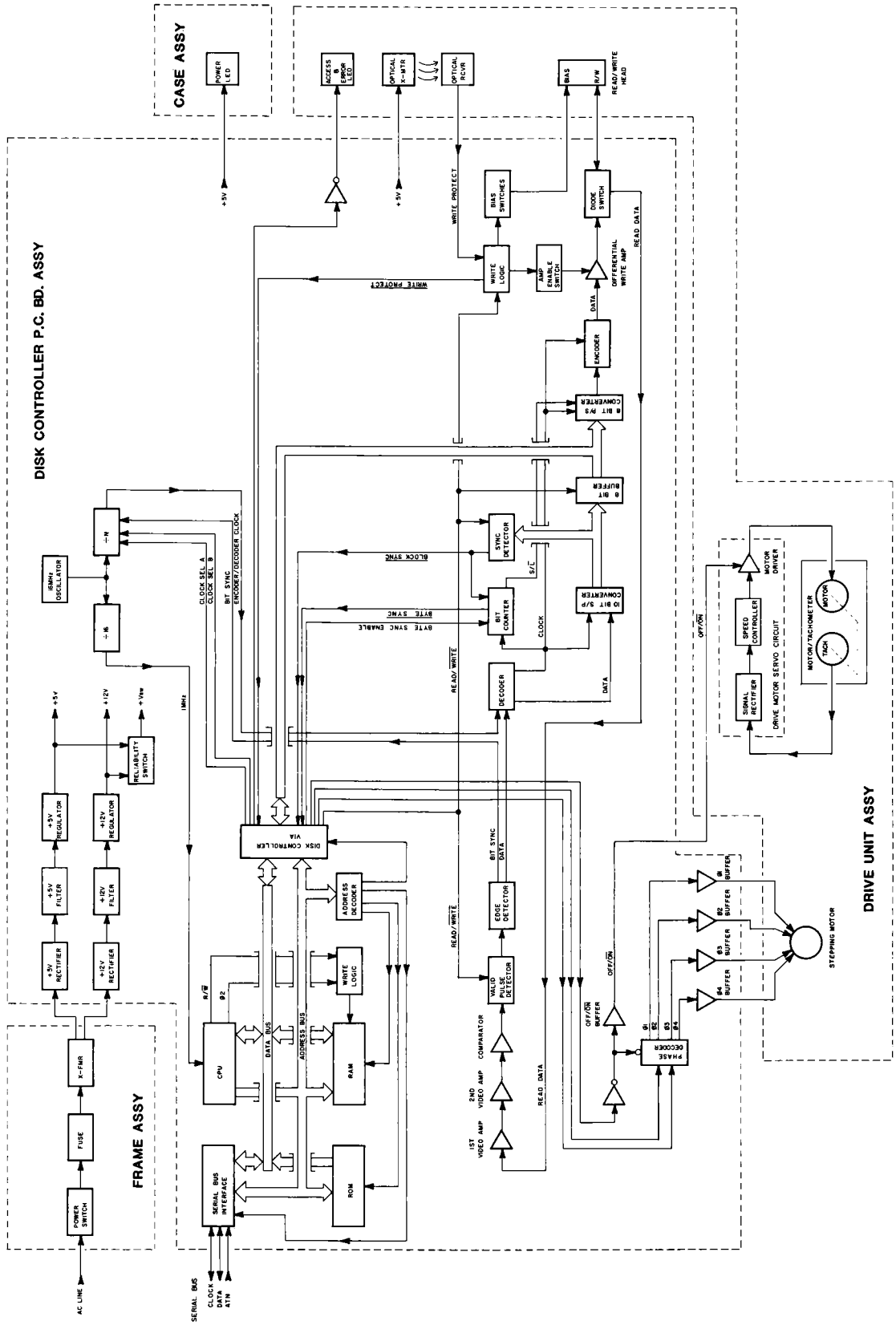


Fig. A-1. Block diagram, all models.

A.2 VIC-1541 INTERCONNECT DIAGRAMS

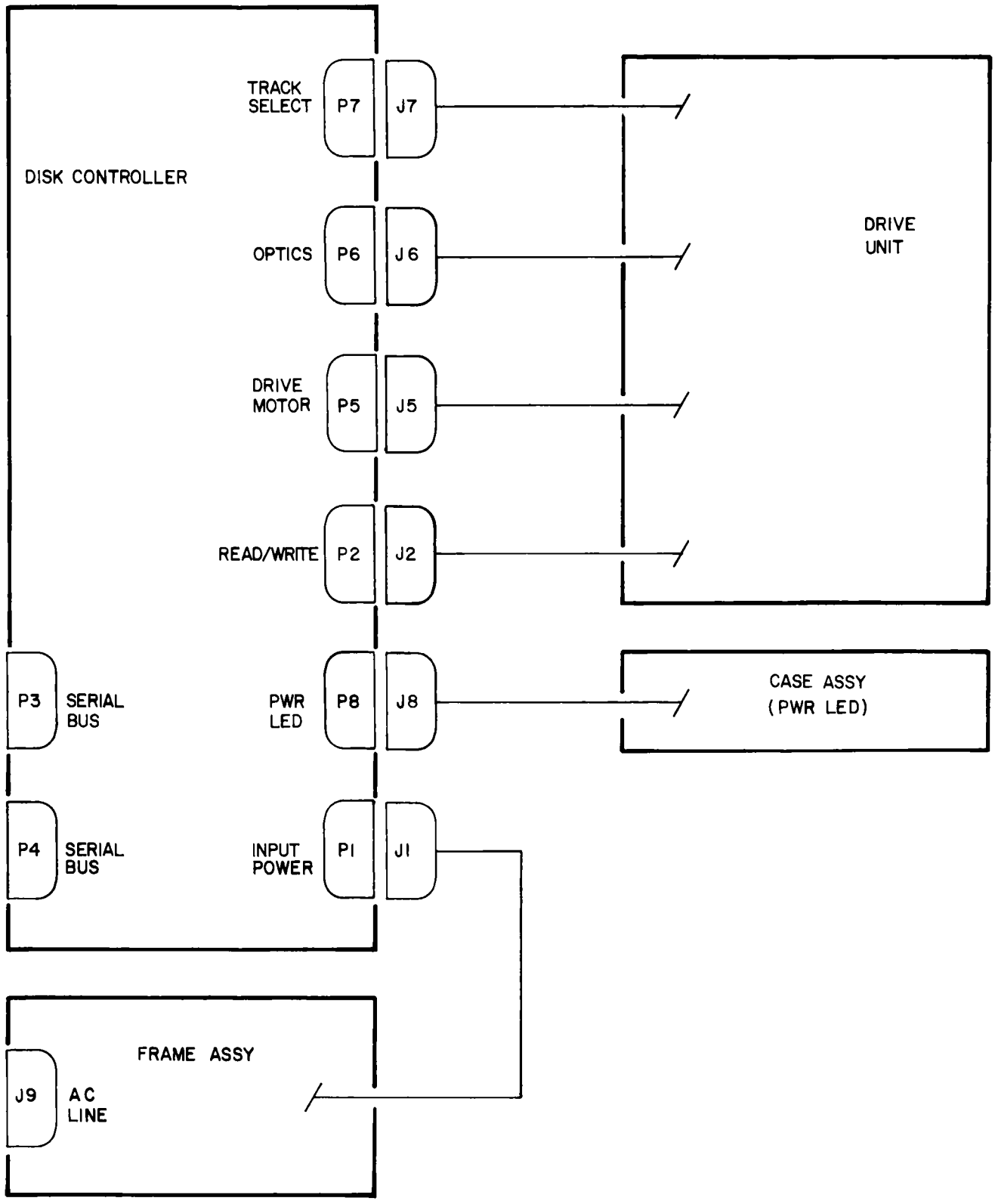


Fig. A-2. Interconnect diagram, Model 1540.

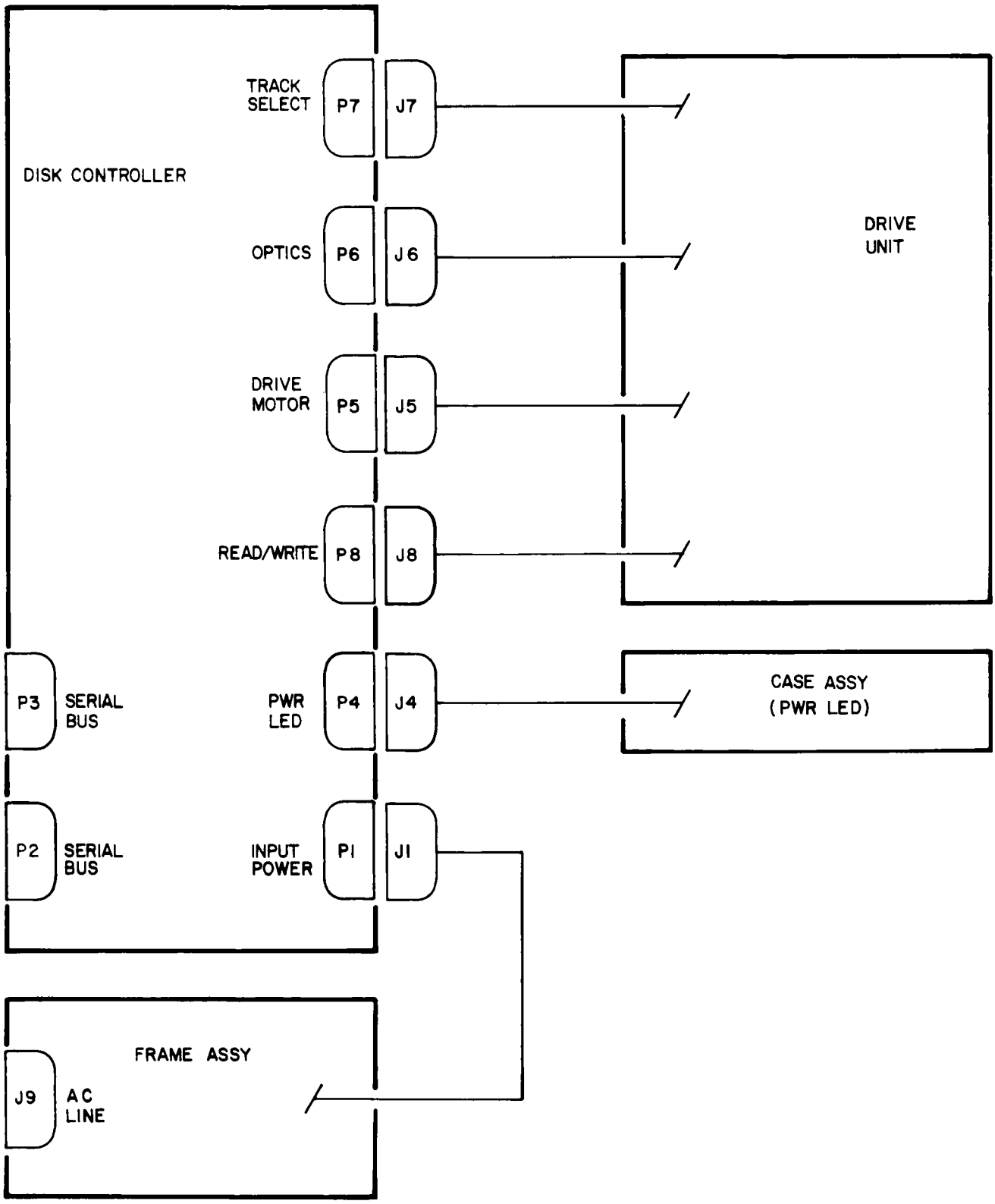


Fig. A-3. Interconnect diagram, Models 1541 and 1542.

A.3 VIC-1541 SCHEMATICS

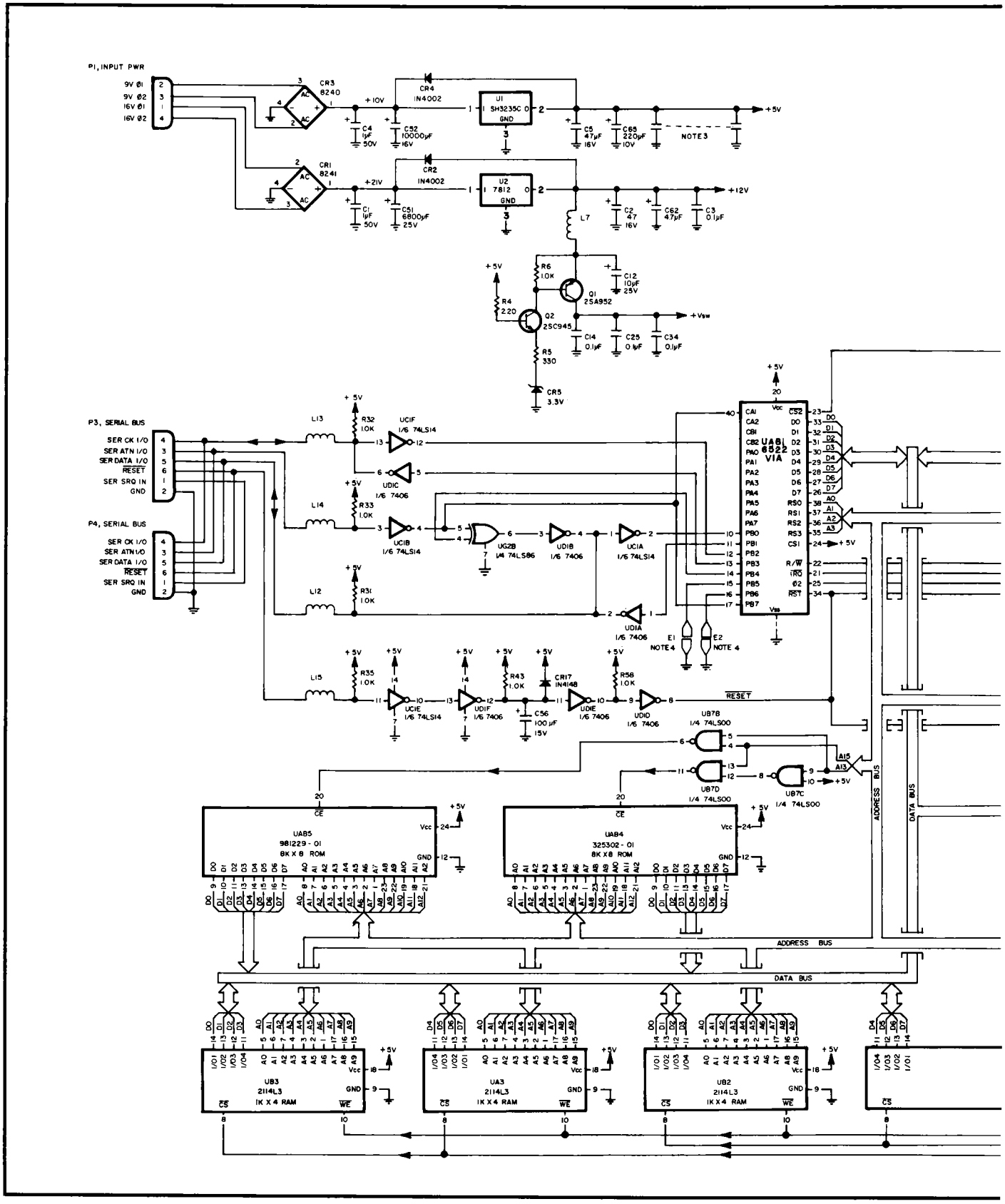
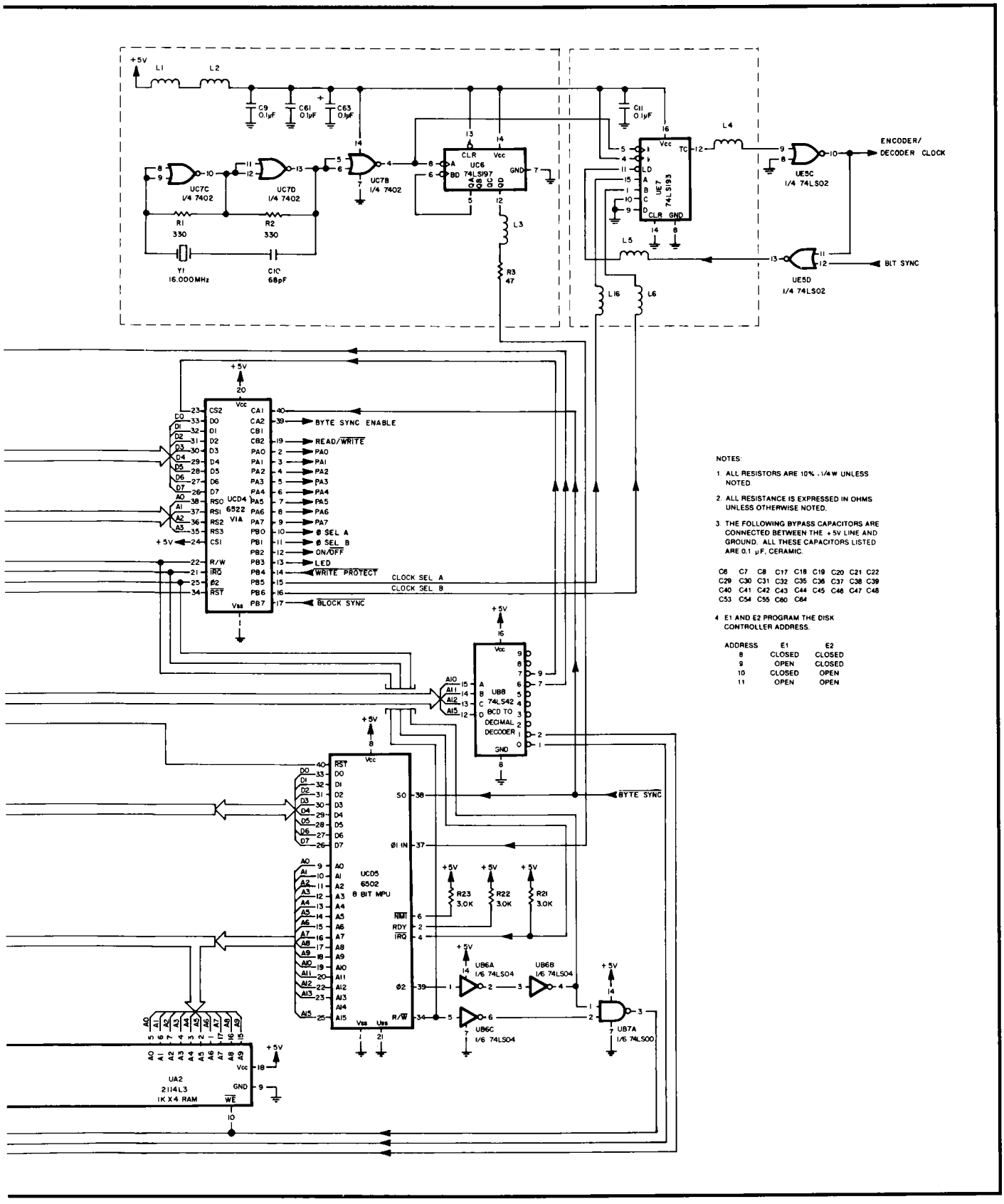


Fig. A-4. Disk controller



NOTES:

1. ALL RESISTORS ARE 10% , 1/4W UNLESS NOTED.
2. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
3. THE FOLLOWING BYPASS CAPACITORS ARE CONNECTED BETWEEN THE +5V LINE AND GROUND. ALL THESE CAPACITORS LISTED ARE 0.1 μF, CERAMIC.

C6	C7	C8	C17	C18	C19	C20	C21	C22
C29	C30	C31	C32	C35	C36	C37	C38	C39
C40	C41	C42	C43	C44	C45	C46	C47	C48
C53	C54	C55	C60	C64				

4. E1 AND E2 PROGRAM THE DISK CONTROLLER ADDRESS.

ADDRESS	E1	E2
8	CLOSED	CLOSED
9	OPEN	CLOSED
10	CLOSED	OPEN
11	OPEN	OPEN

schematic, Model 1540.

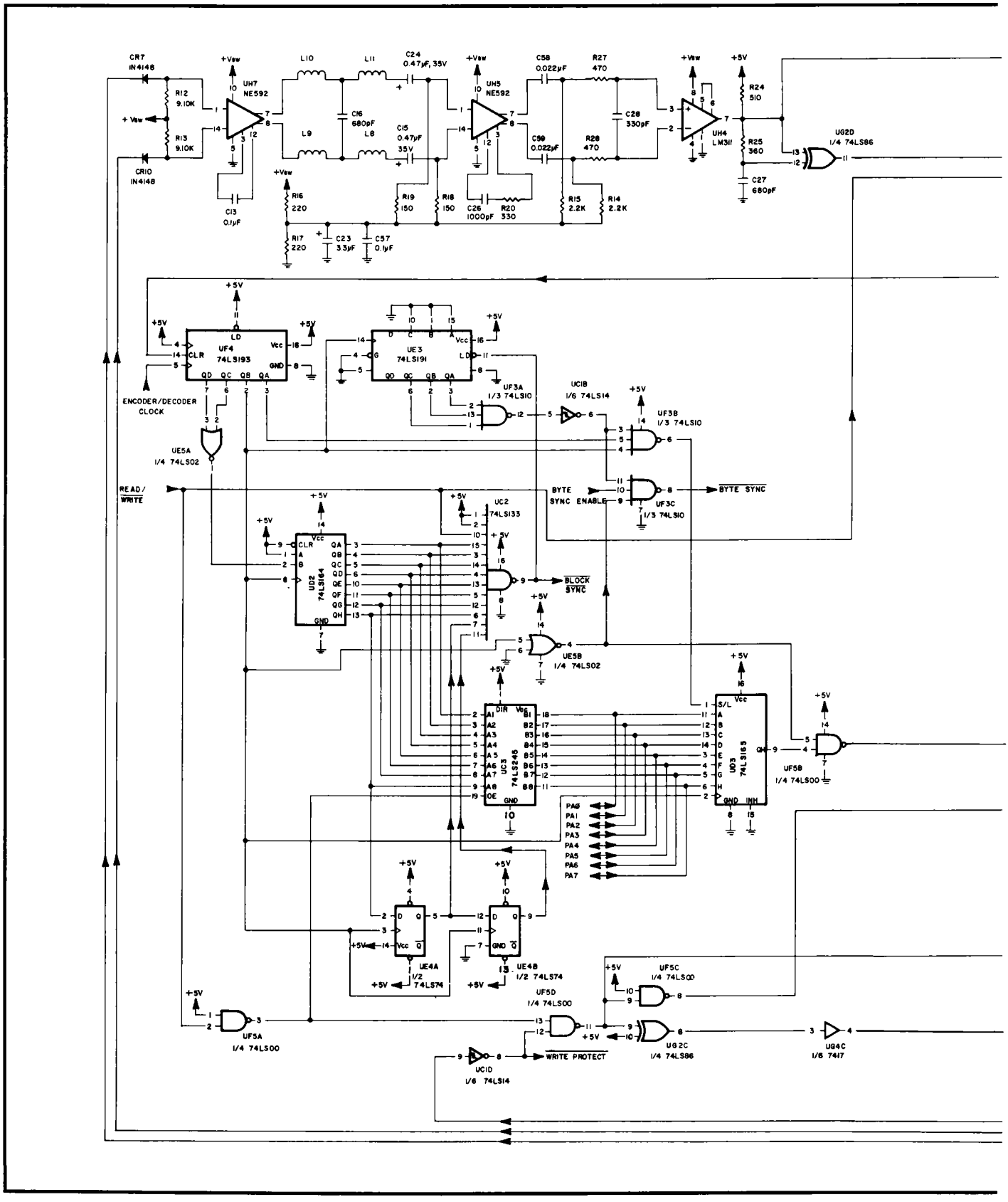
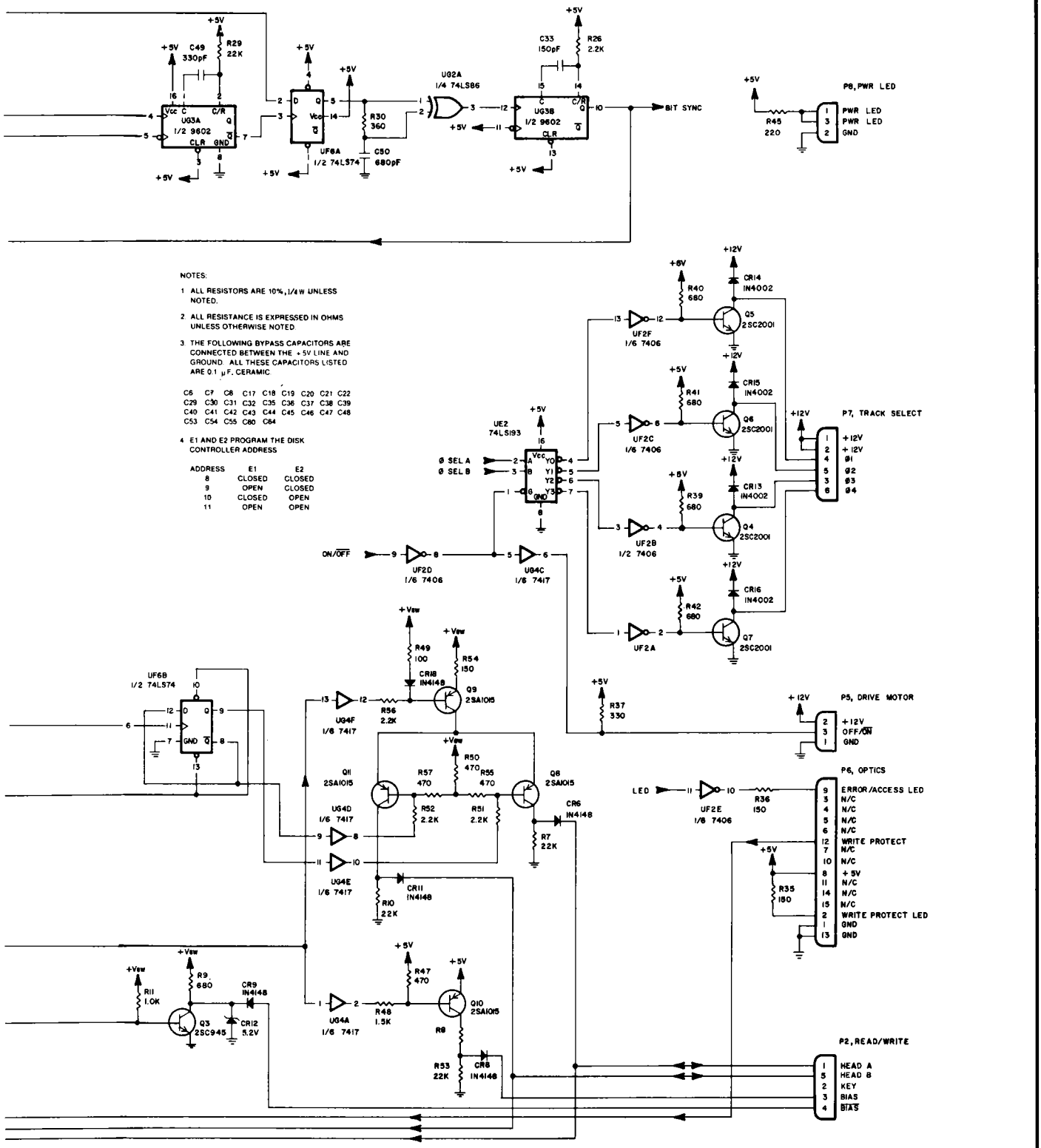


Fig. A-4. Disk controller



schematic, Model 1540 (cont.)

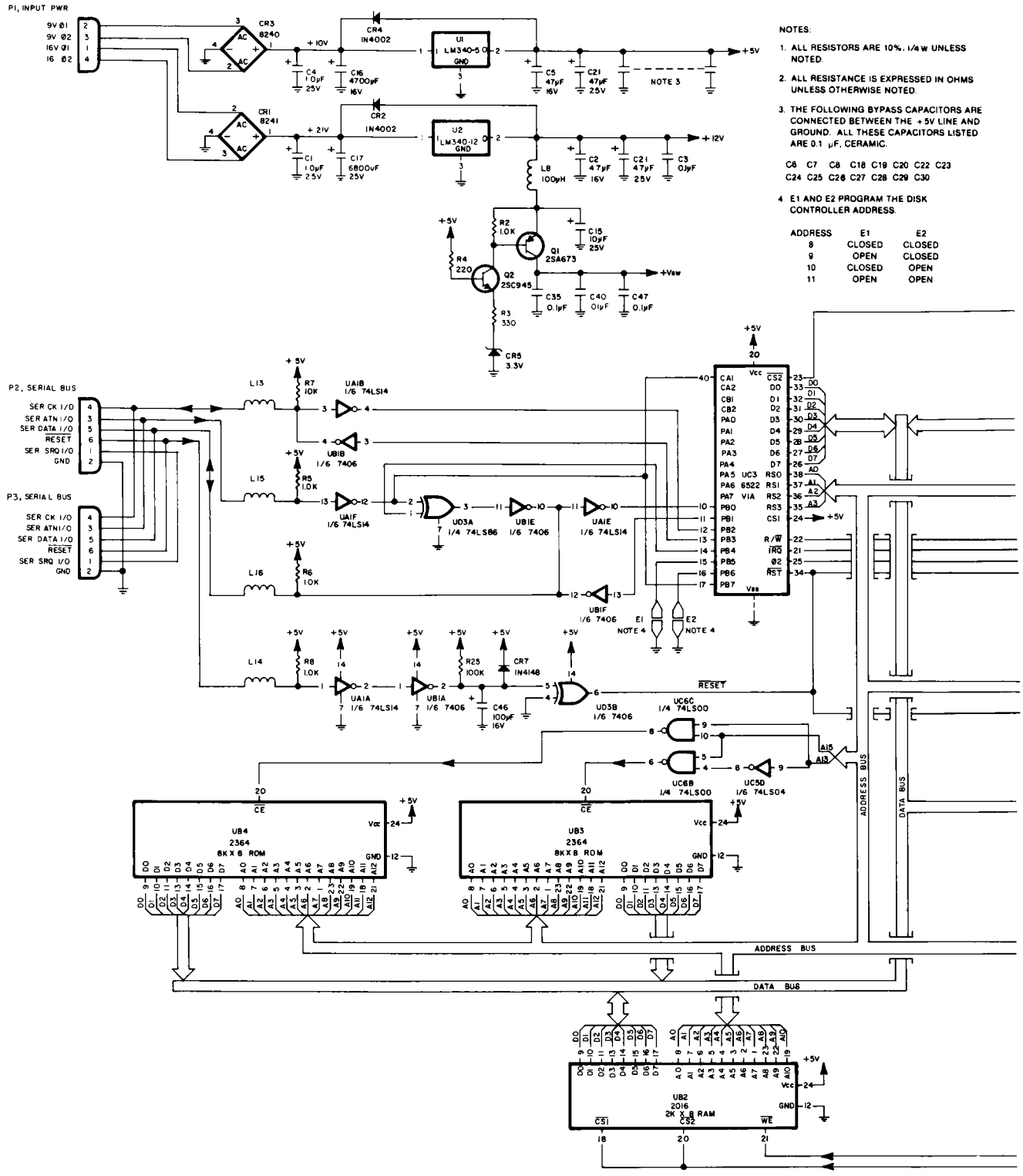
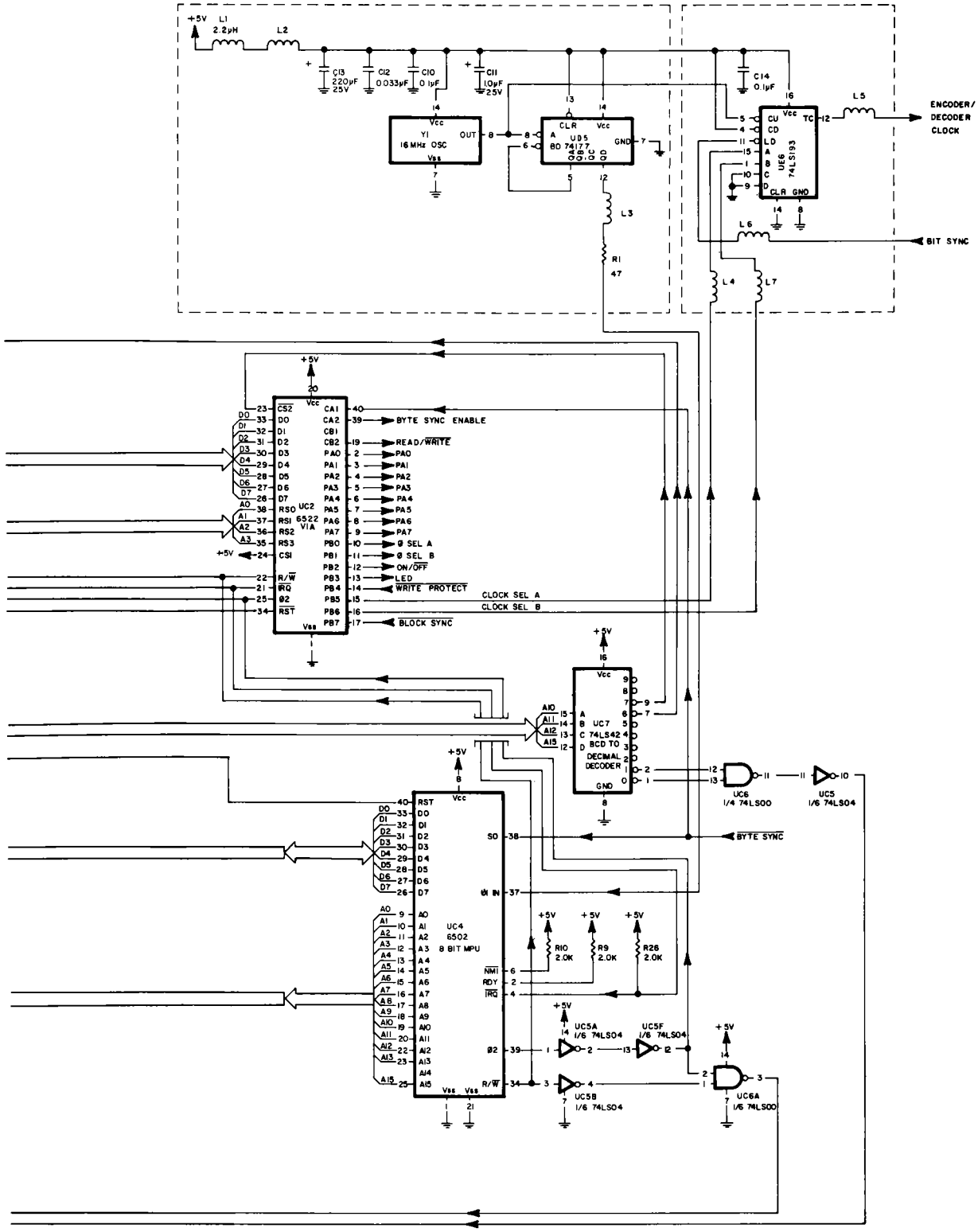
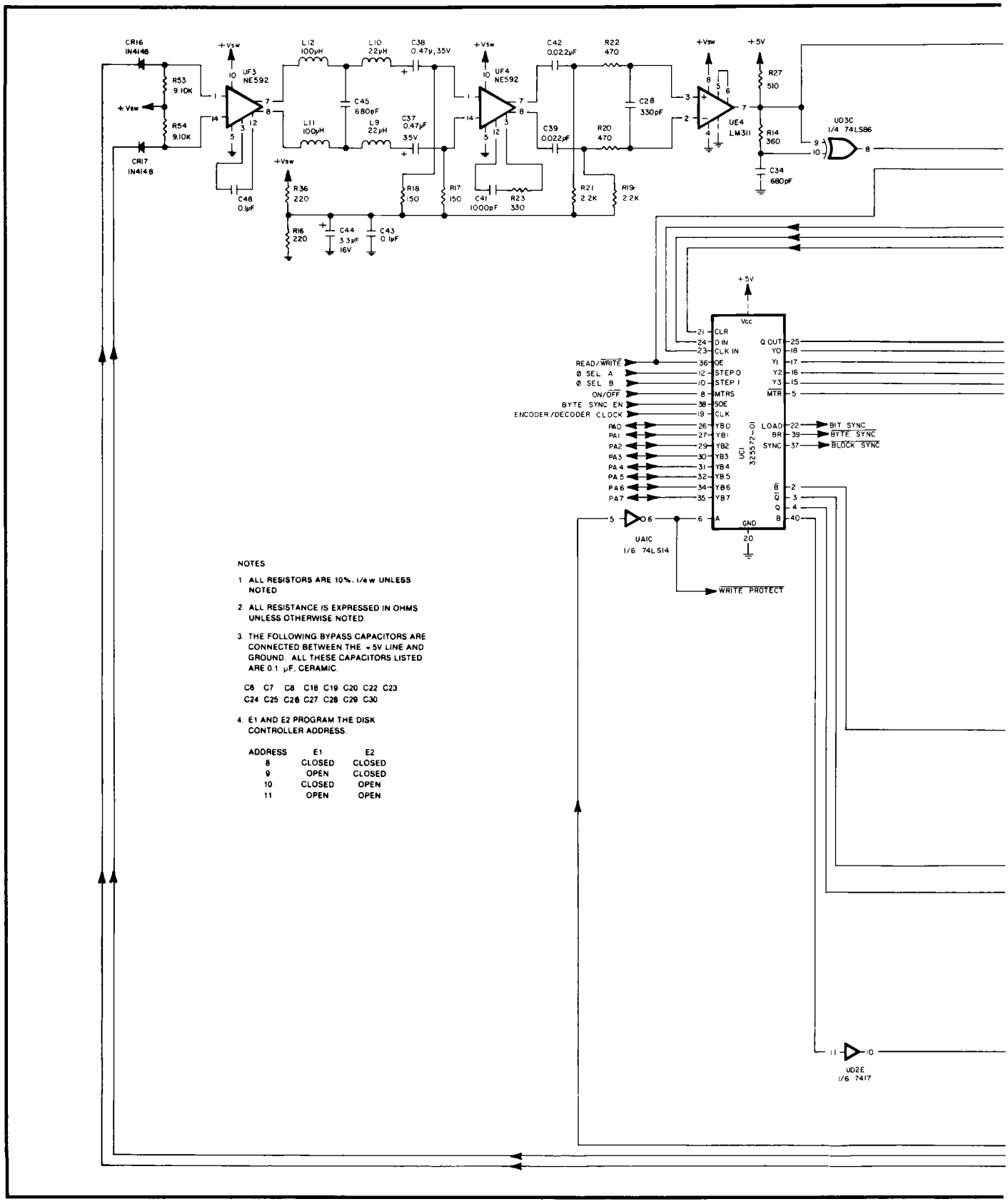


Fig. A-5. Disk controller



schematic, Model 1541.



NOTES

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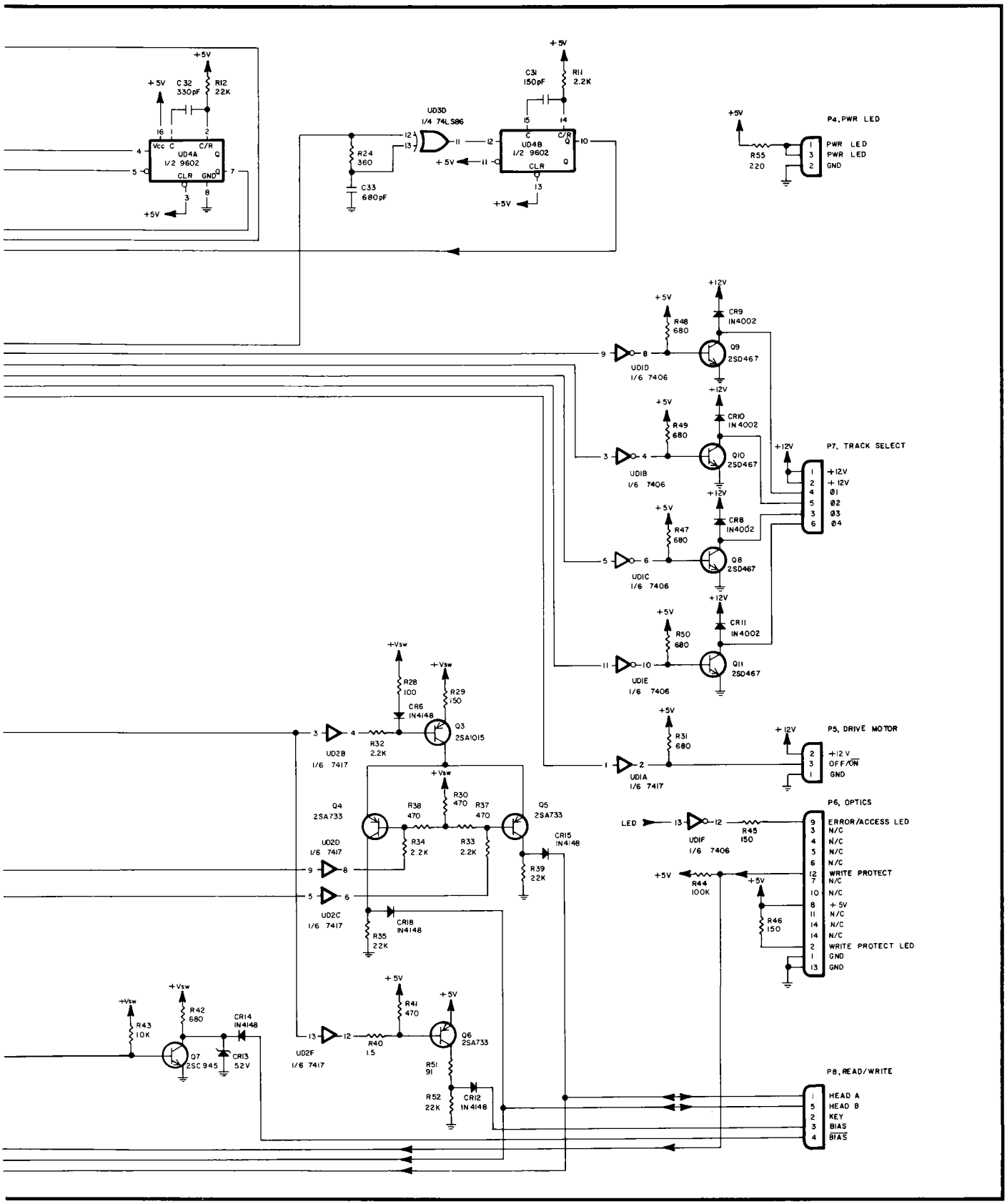
3. THE FOLLOWING BYPASS CAPACITORS ARE CONNECTED BETWEEN THE +5V LINE AND GROUND. ALL THESE CAPACITORS LISTED ARE 0.1 μF, CERAMIC.

   C6 C7 C8 C18 C19 C20 C22 C23
   C24 C25 C26 C27 C28 C29 C30

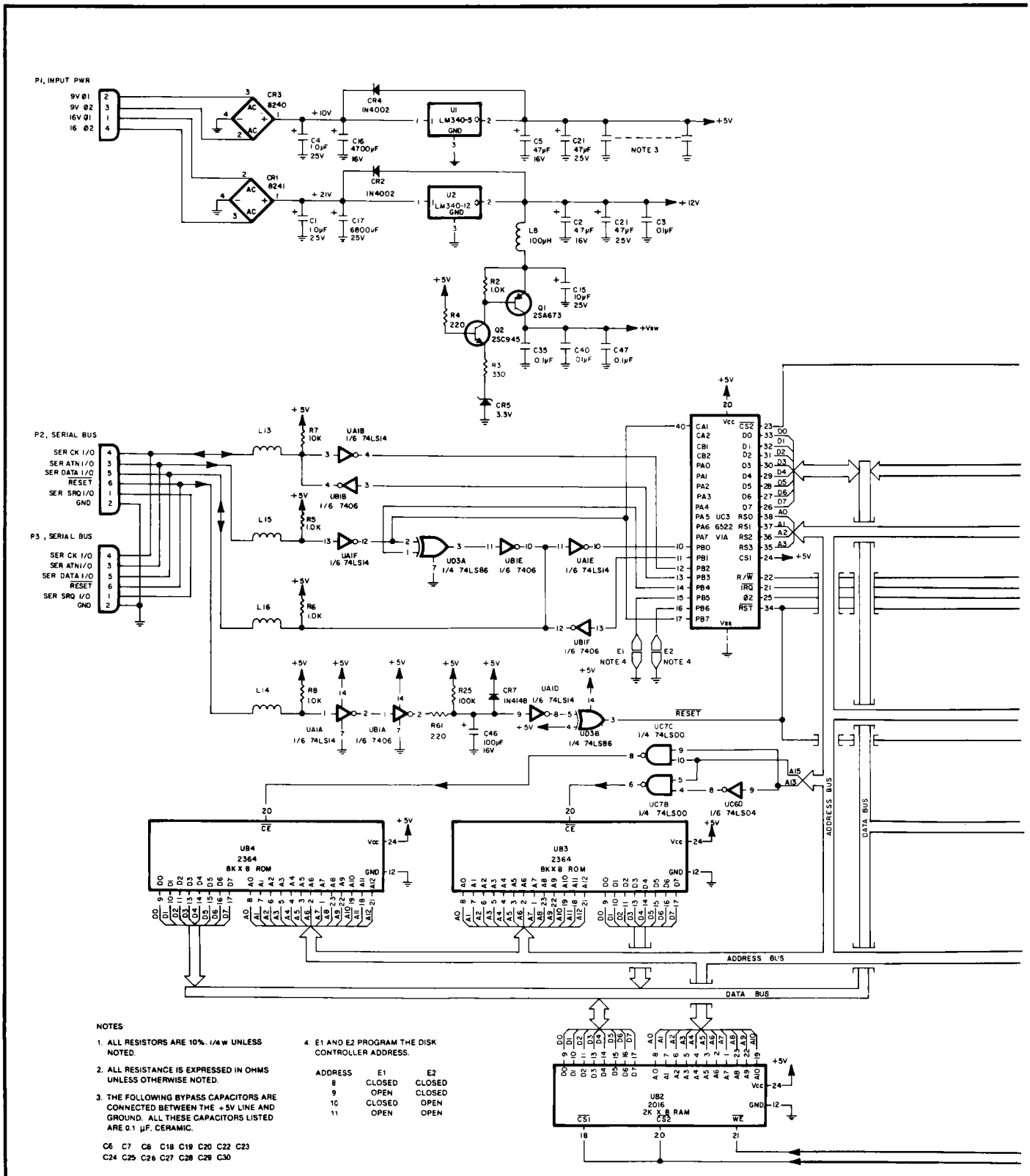
4. E1 AND E2 PROGRAM THE DISK CONTROLLER ADDRESS.

ADDRESS	E1	E2
8	CLOSED	CLOSED
9	OPEN	CLOSED
10	CLOSED	OPEN
11	OPEN	OPEN

Fig. A-5. Disk controller



schematic, Model 1541 (cont.)



NOTES

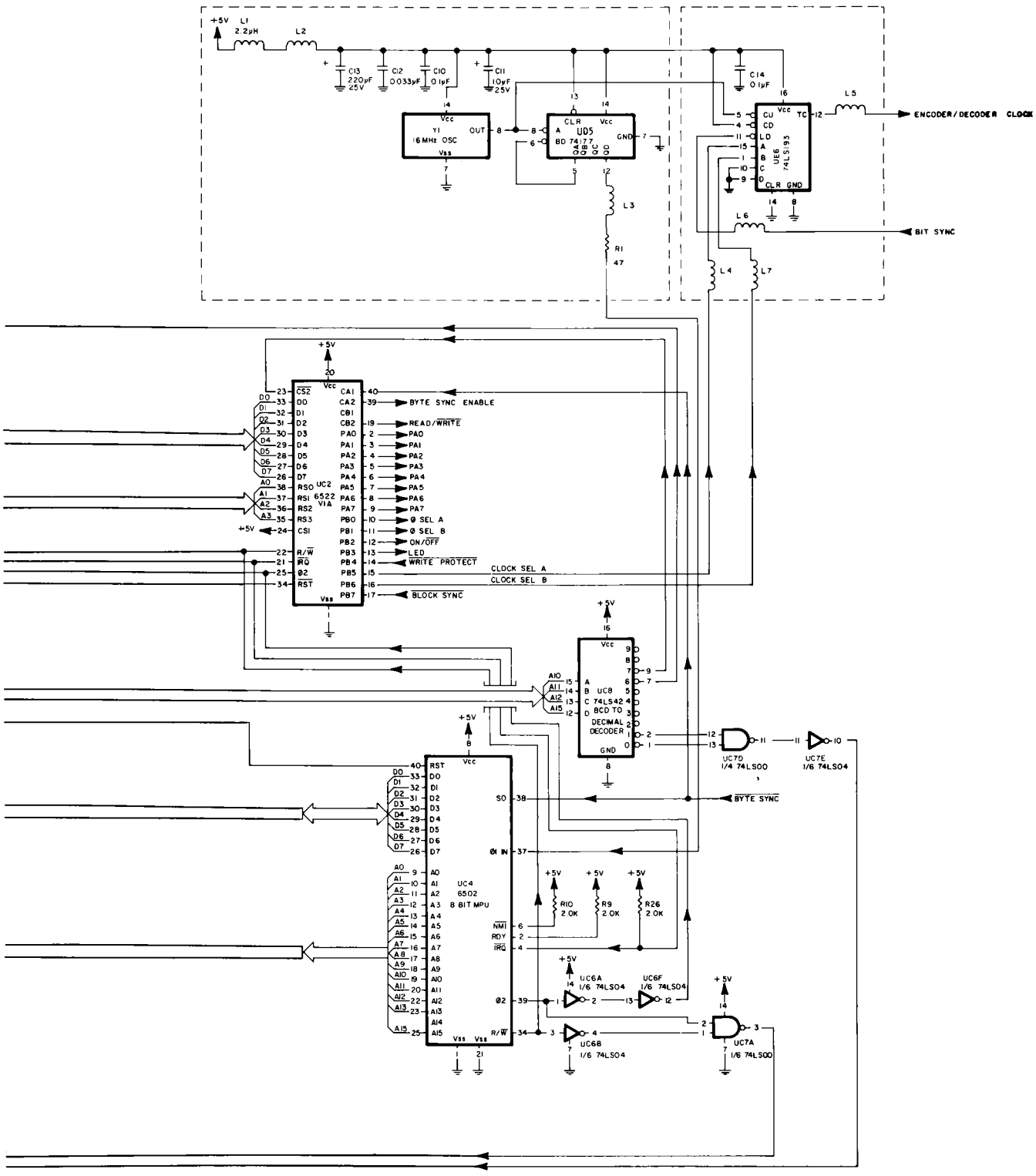
1. ALL RESISTORS ARE 10%, 1/4 W UNLESS NOTED.
2. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
3. THE FOLLOWING BYPASS CAPACITORS ARE CONNECTED BETWEEN THE +5V LINE AND GROUND. ALL THESE CAPACITORS LISTED ARE 0.1 µF. CERAMIC.

C6 C7 C8 C18 C19 C20 C22 C23
C24 C25 C26 C27 C28 C29 C30

4. E1 AND E2 PROGRAM THE DISK CONTROLLER ADDRESS.

ADDRESS	E1	E2
8	CLOSED	CLOSED
9	OPEN	CLOSED
10	CLOSED	OPEN
11	OPEN	OPEN

Fig. A-6. Disk controller



schematic, Model 1542.

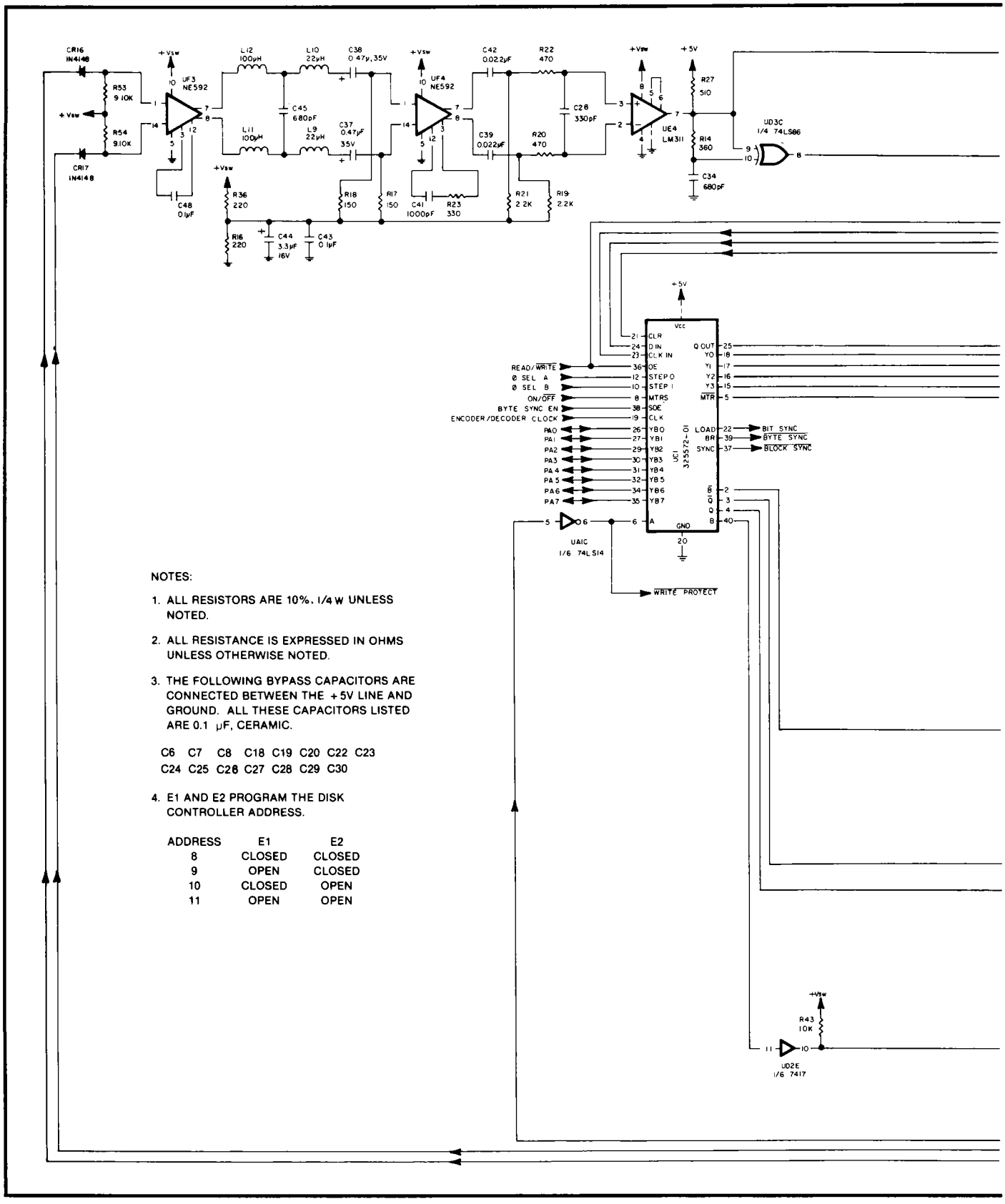
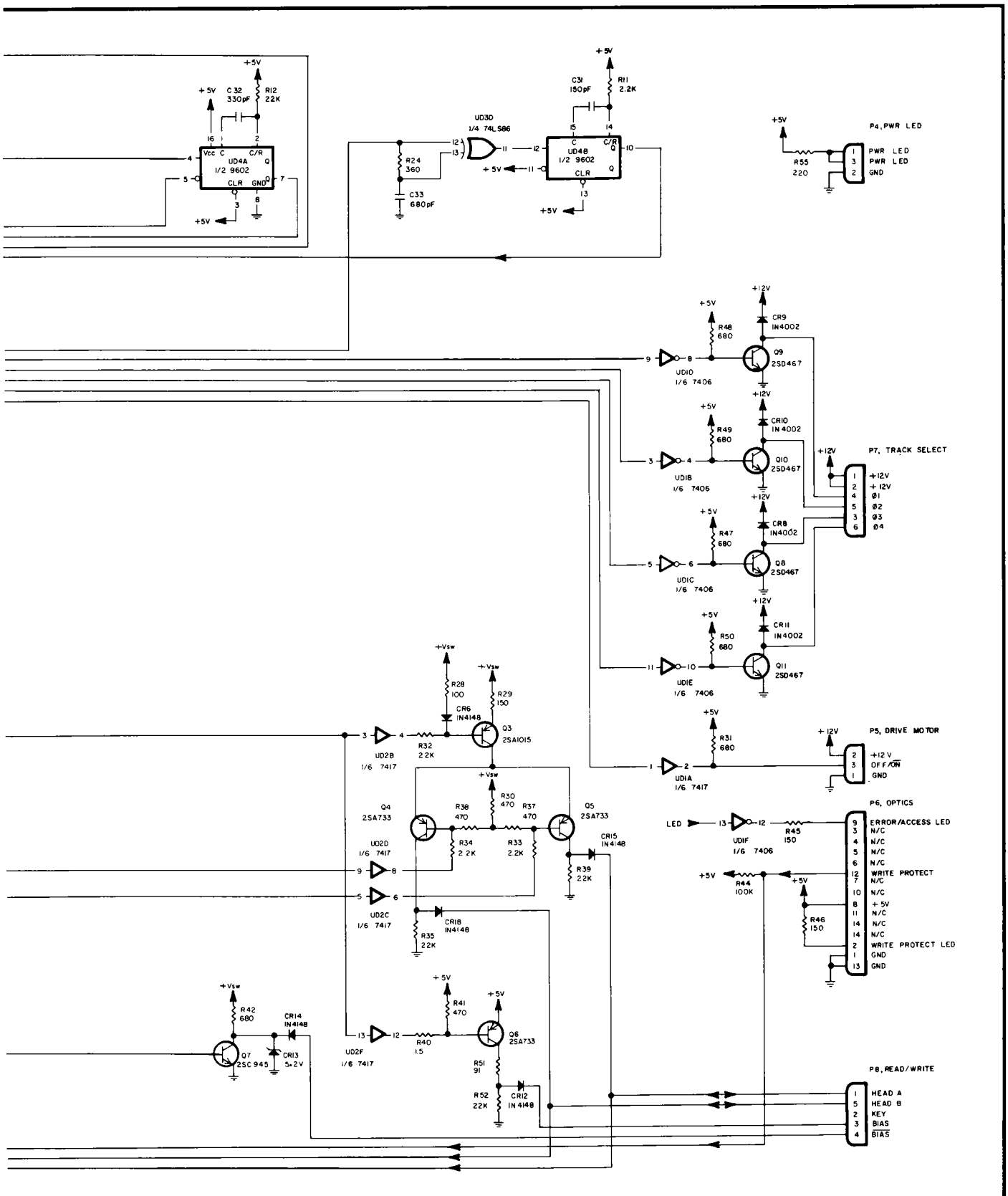


Fig. A-6. Disk controller



schematic, Model 1542 (cont.)

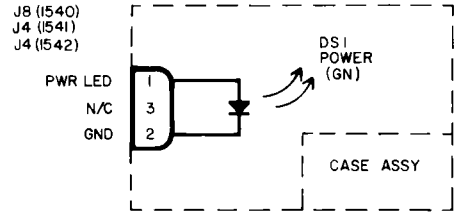


Fig. A-7. Case assembly, all models.

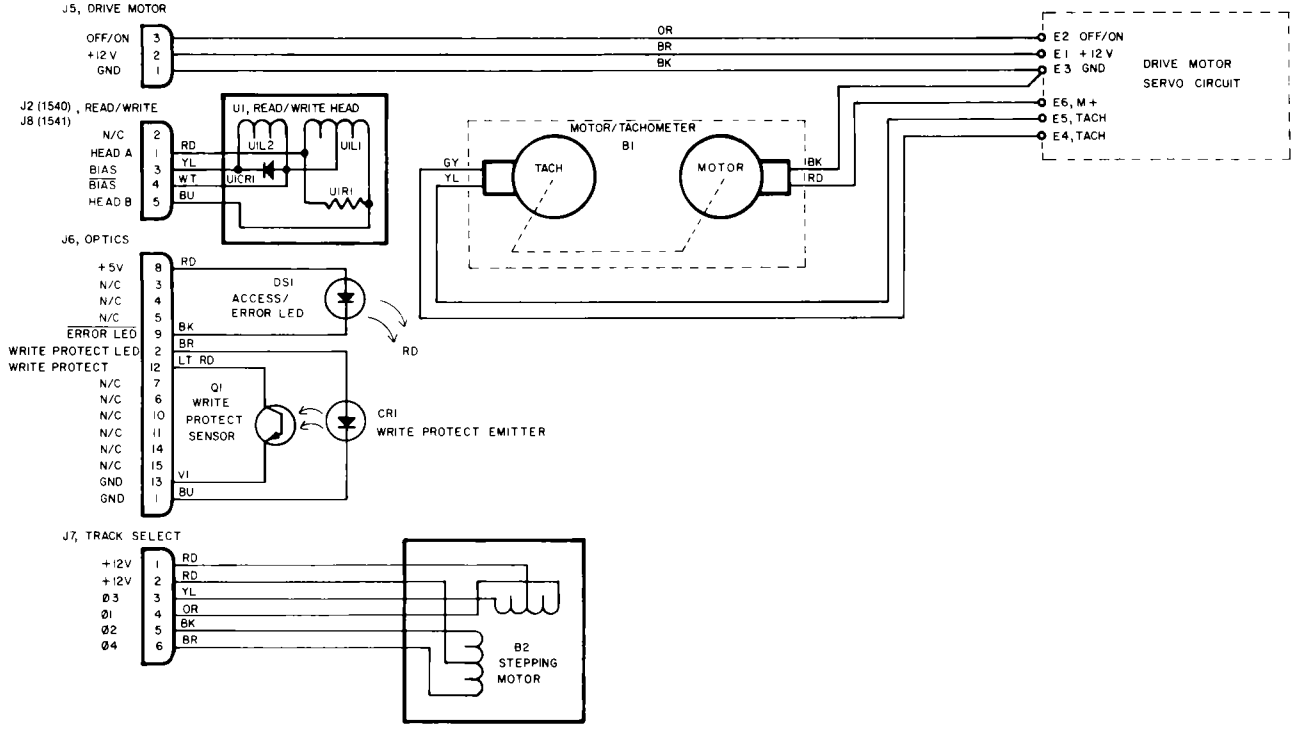


Fig. A-8. Drive unit schematic, Models 1540 and 1541.

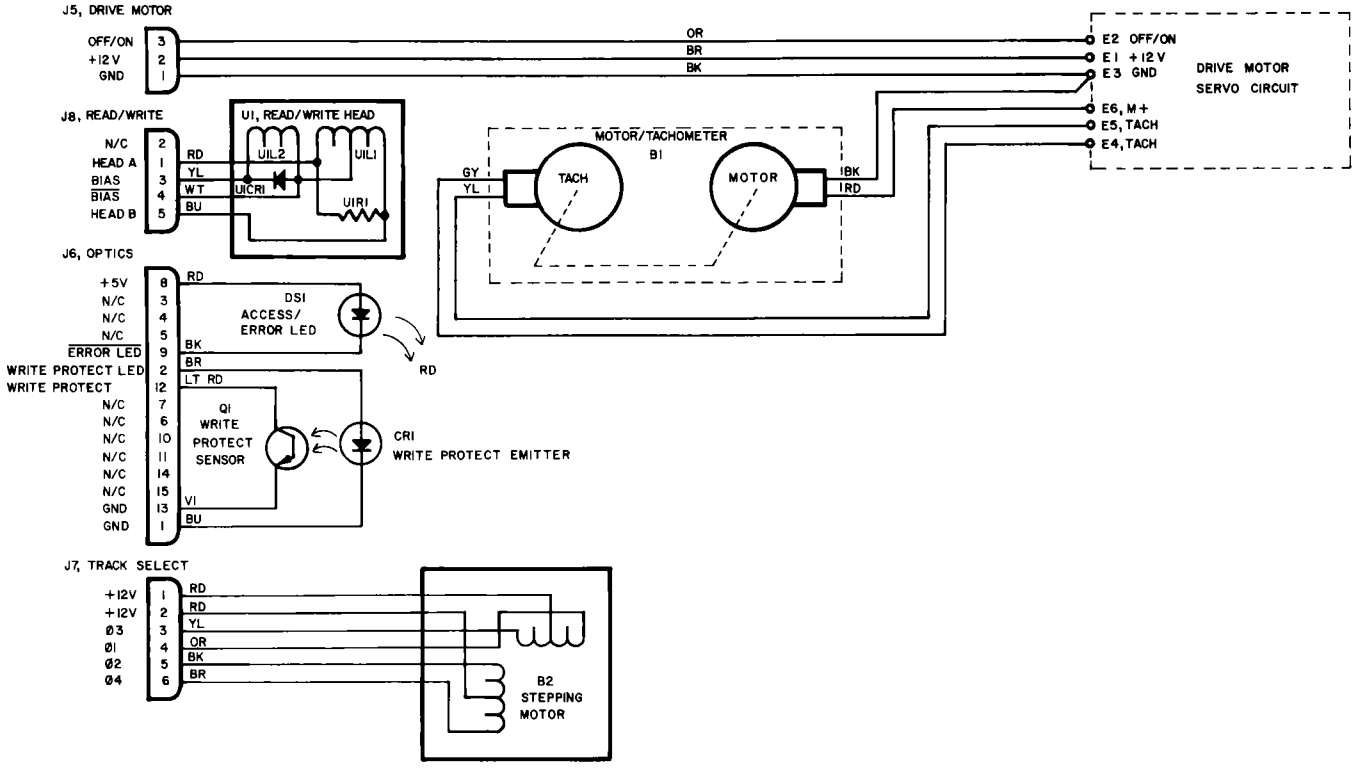


Fig. A-9. Drive unit schematic, Model 1542.

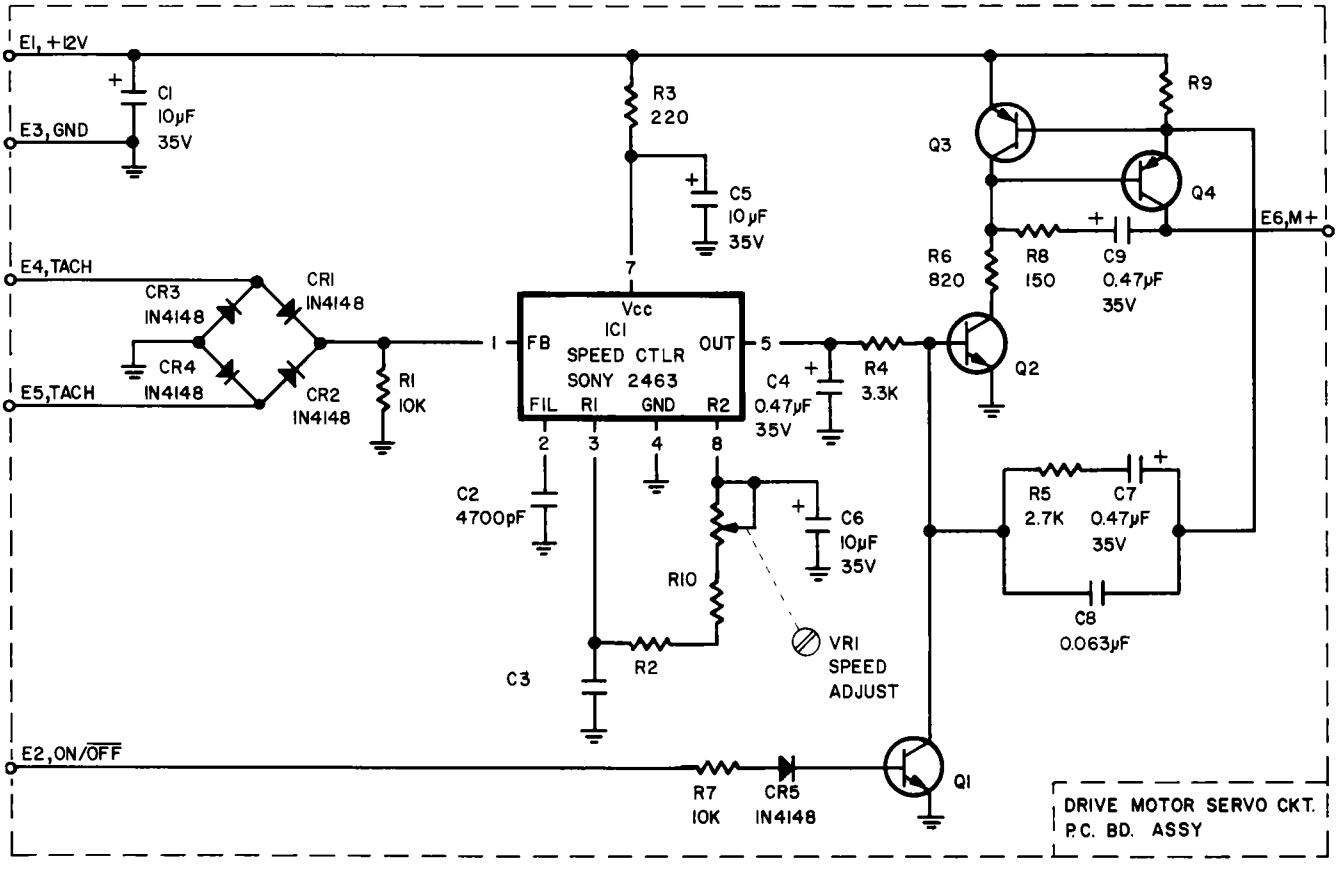


Fig. A-10. Drive motor servo circuit, Models 1540 and 1541.

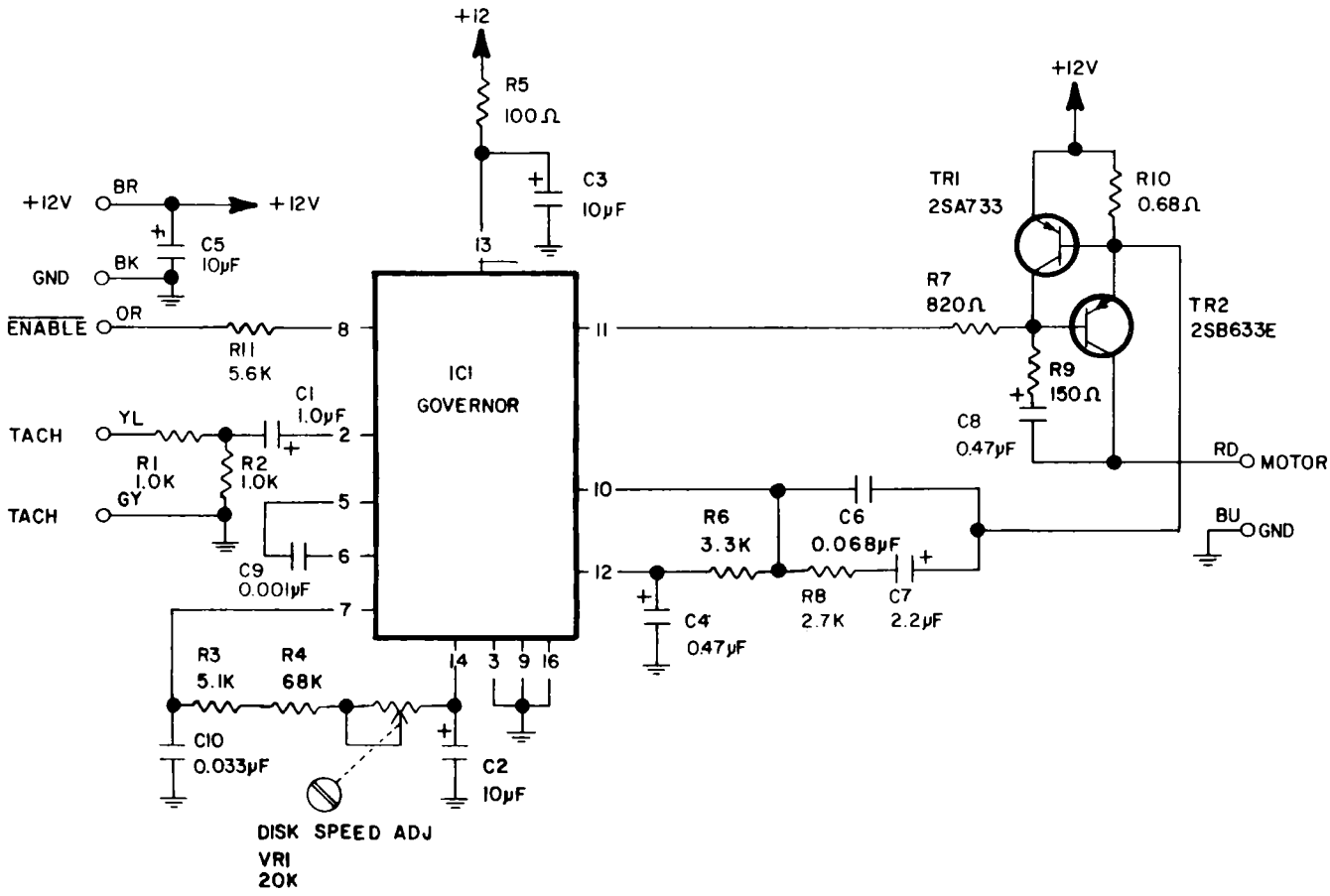


Fig. A-11. Drive motor servo circuit, Model 1542.

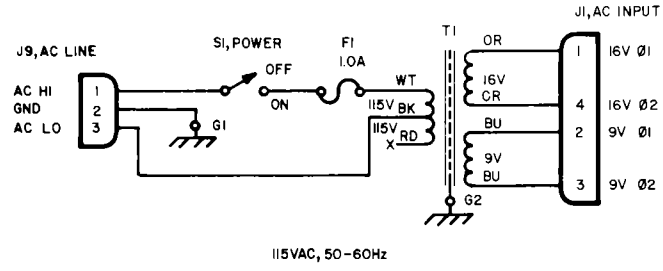


Fig. A-12. Frame assembly, all models.

A.4 VIC-1541 PARTS LAYOUTS

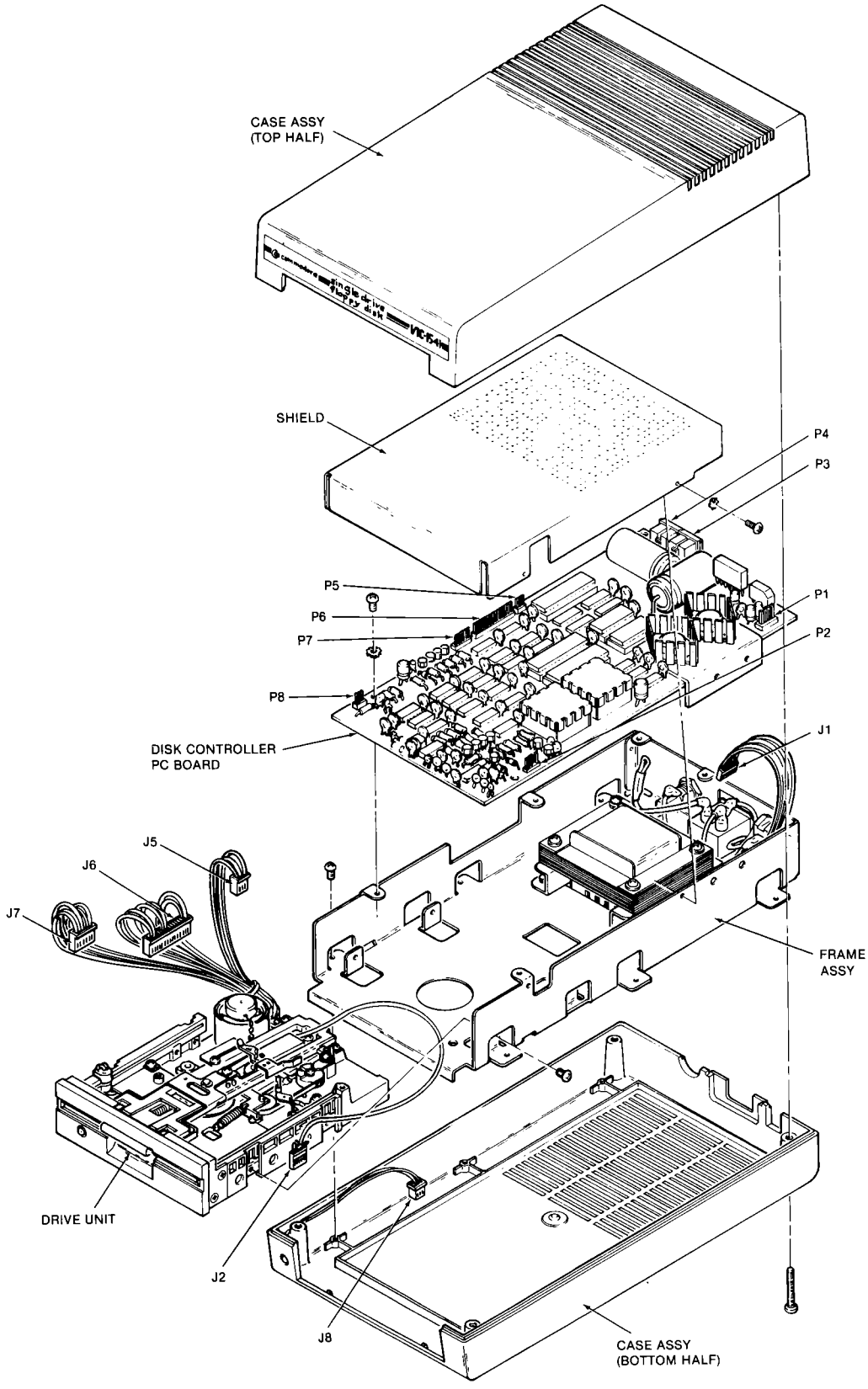


Fig. A-13. Subassembly identification, Model 1540.

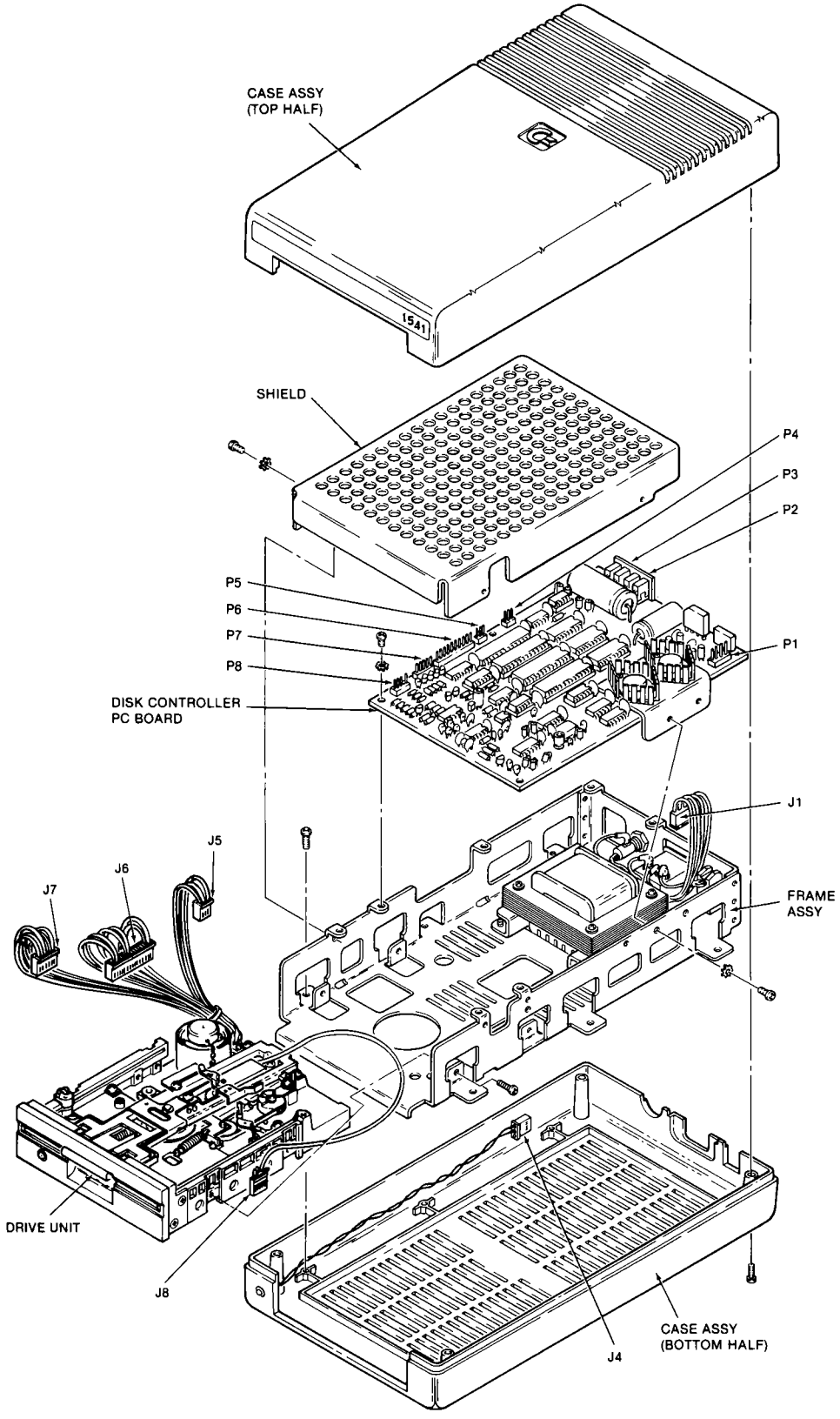


Fig. A-14. Subassembly identification, Model 1541.

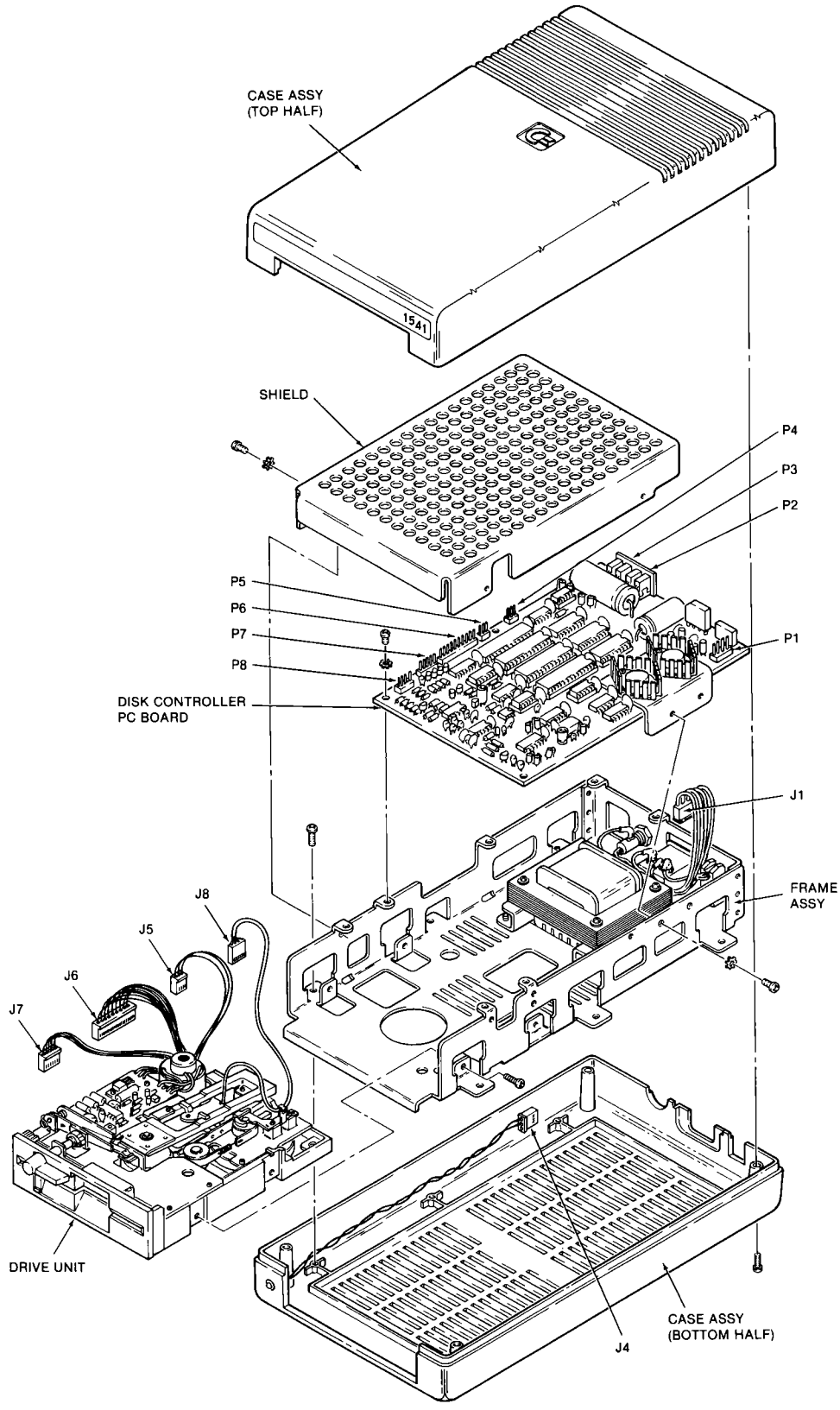


Fig. A-15. Subassembly identification, Model 1542.

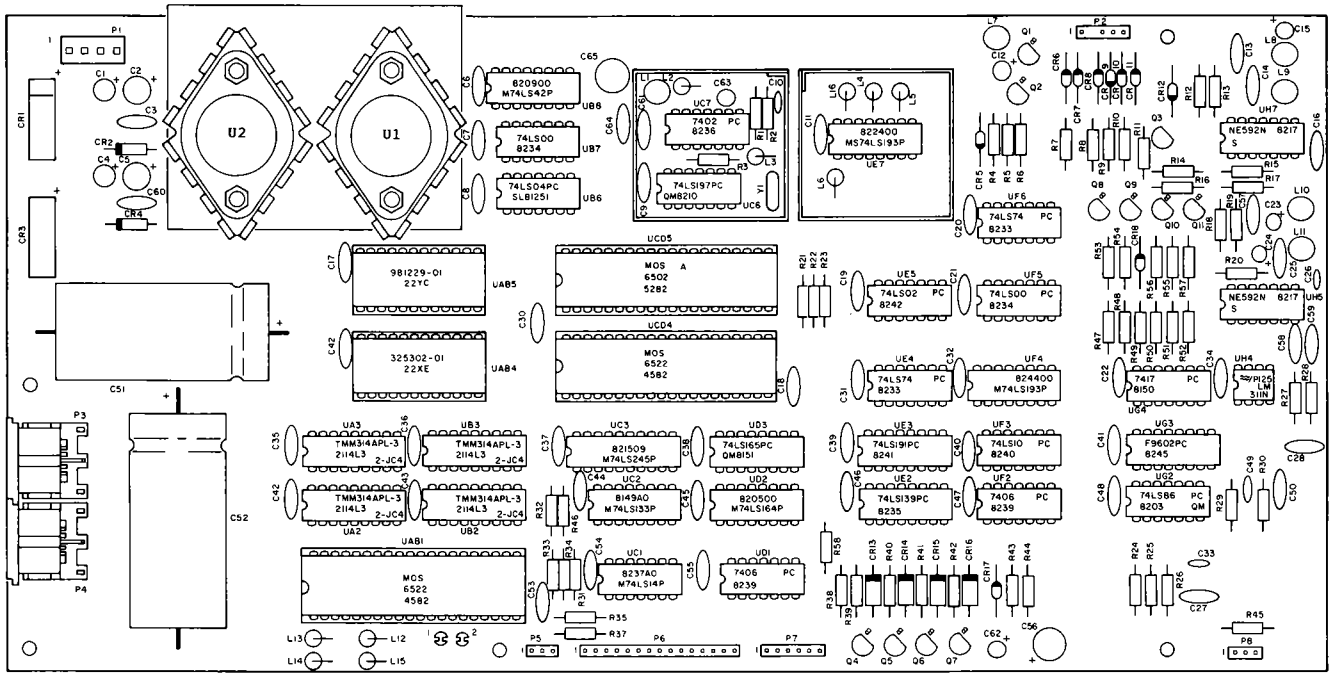


Fig. A-16. Disk controller parts layout, Model 1540.

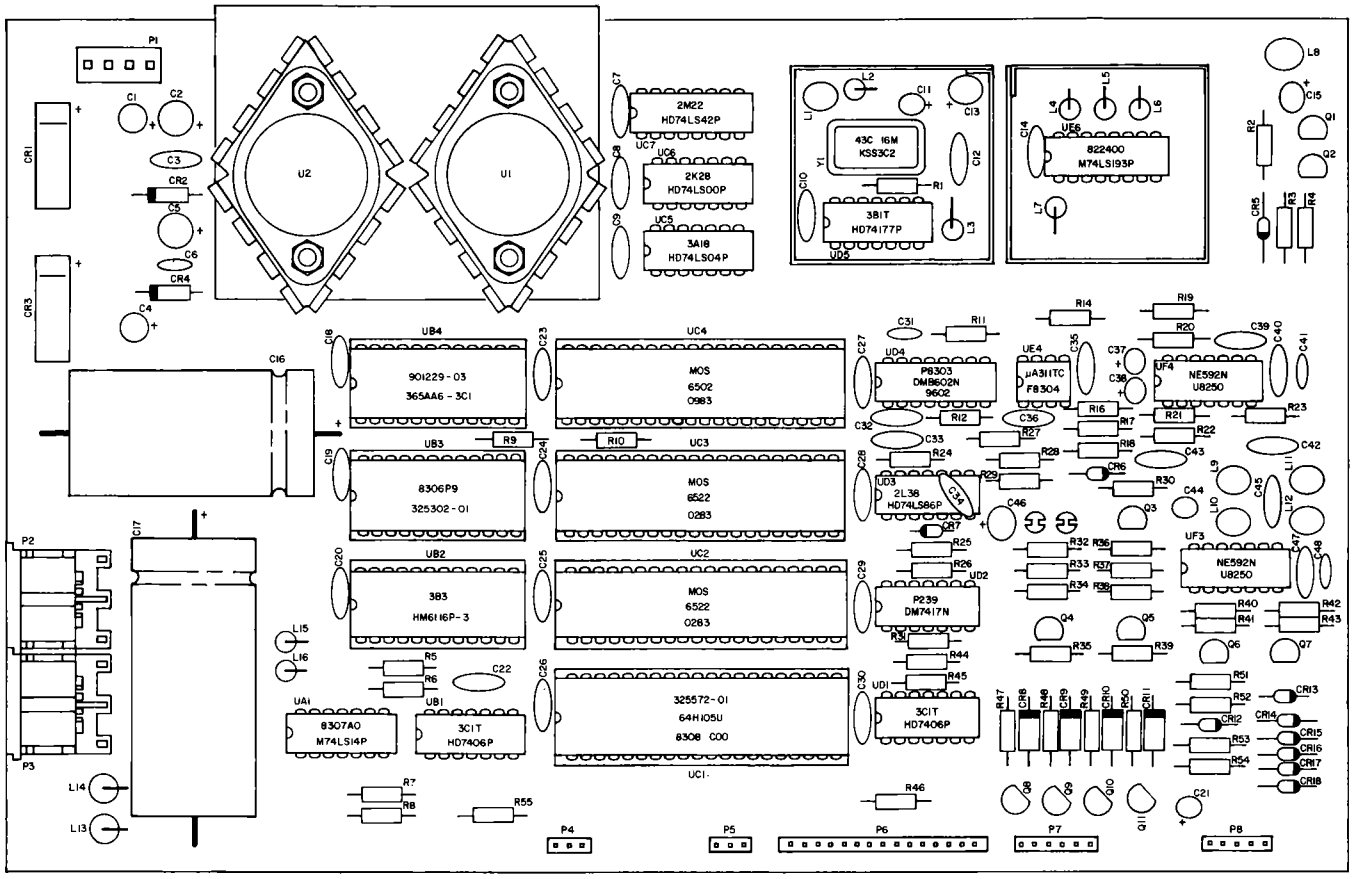


Fig. A-17. Disk controller parts layout, Model 1541.

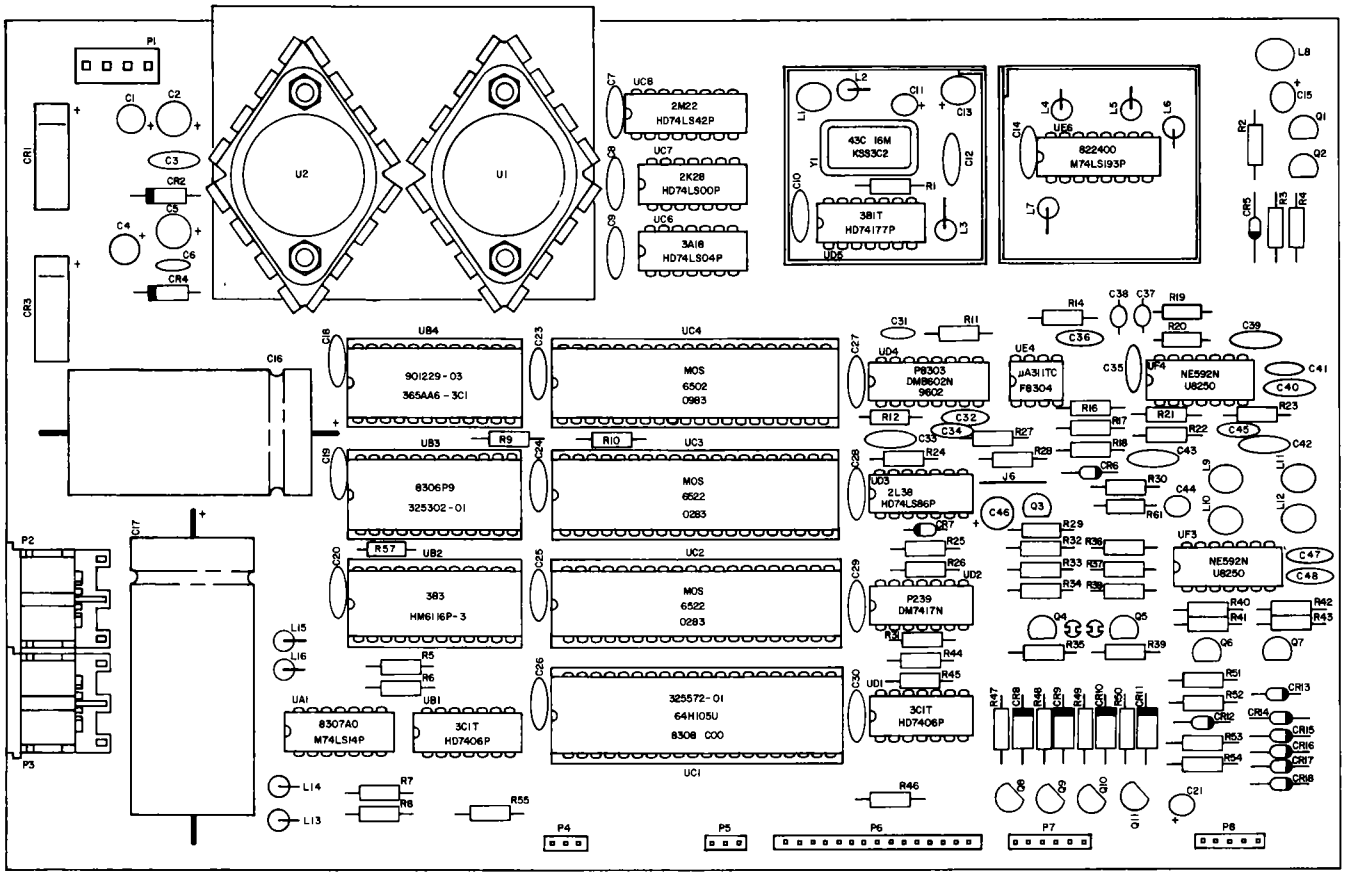


Fig. A-18. Disk controller parts layout, Model 1542.

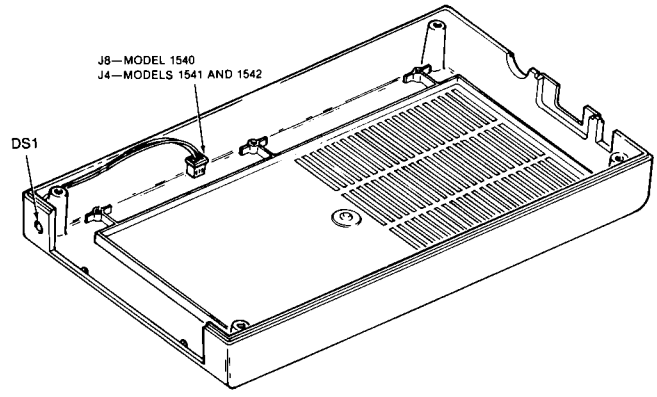


Fig. A-19. Case assembly parts layout, all models.

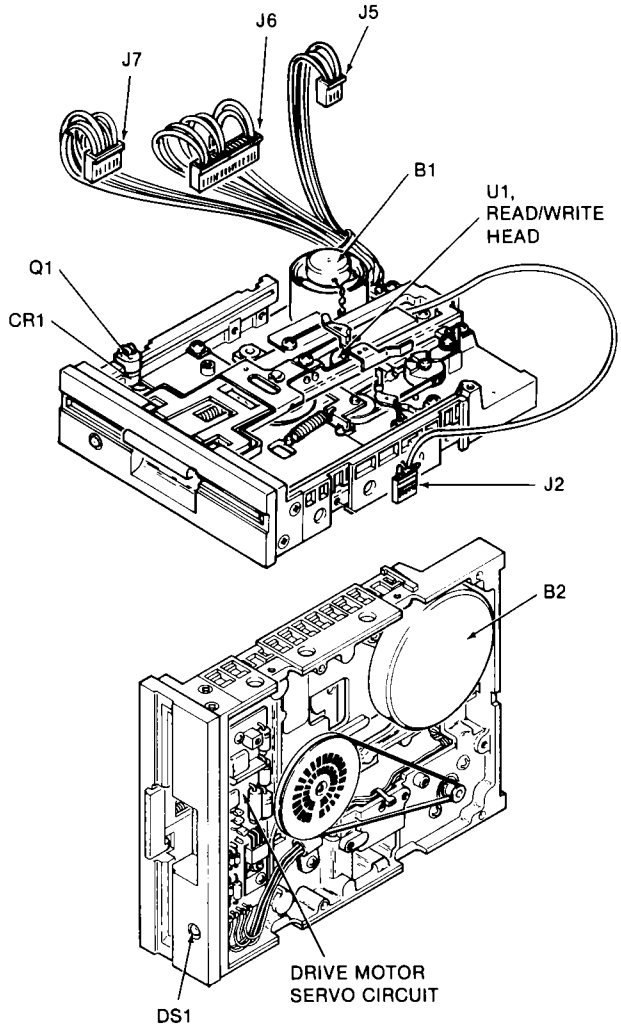


Fig. A-20. Drive unit parts layout, Model 1540.

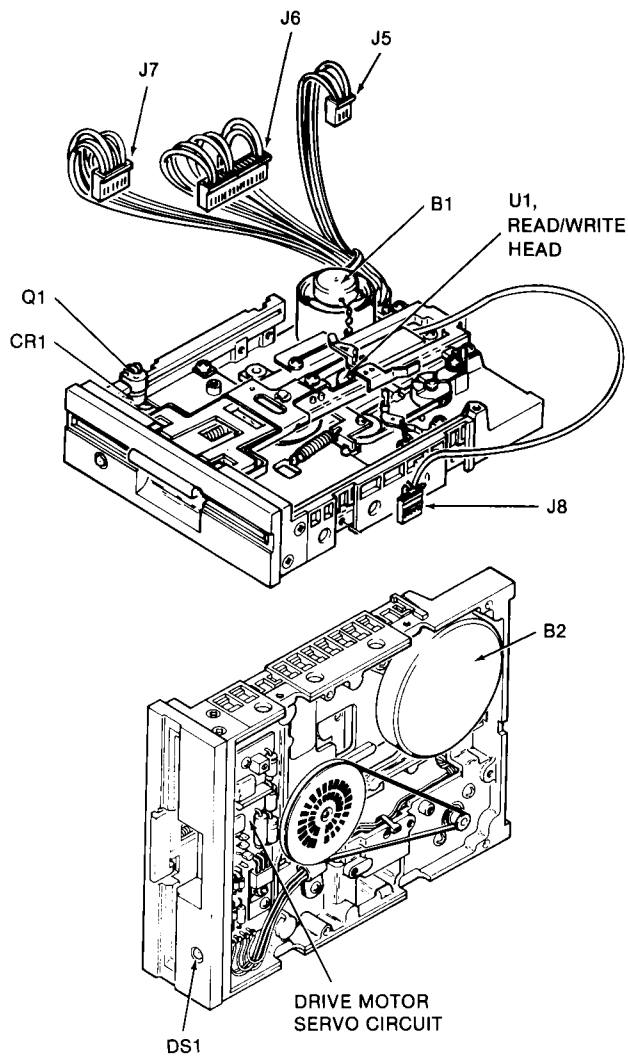


Fig. A-21. Drive unit parts layout, Model 1541.

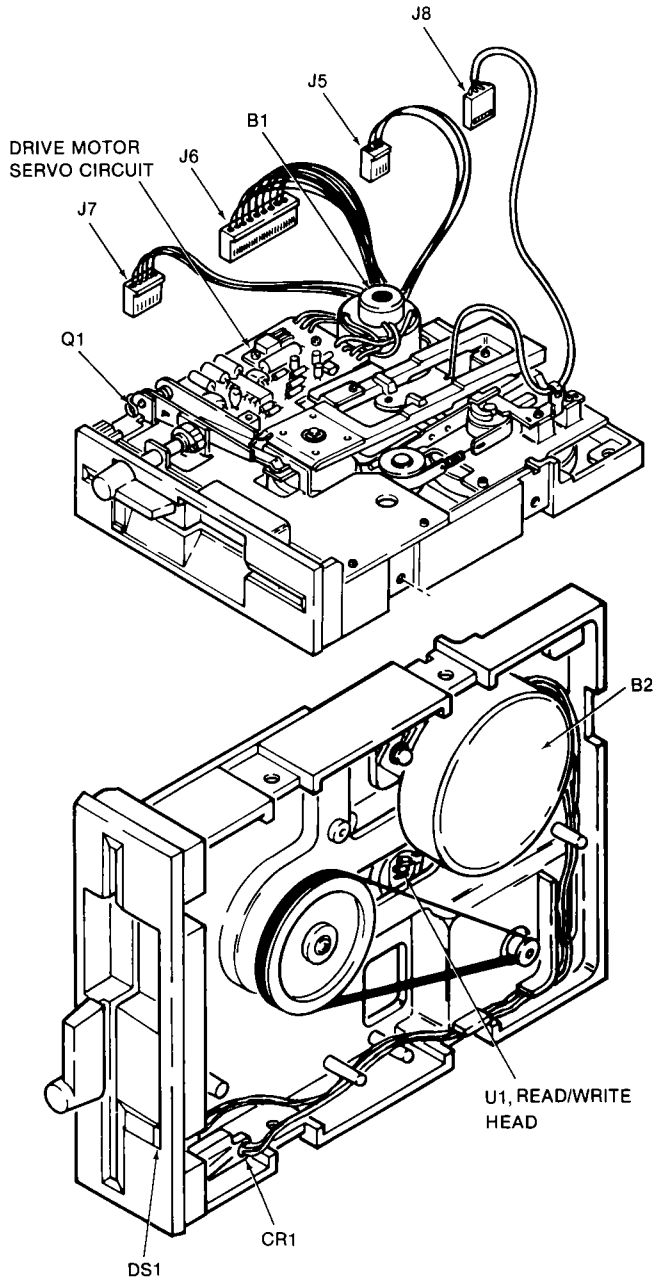


Fig. A-22. Drive unit parts layout, Model 1542.

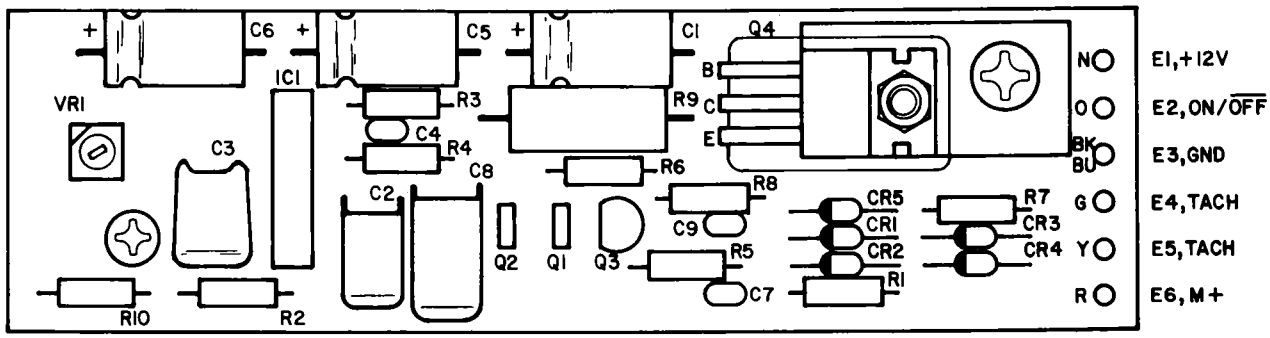


Fig. A-23. Drive motor servo circuit parts layout, Models 1540 and 1541.

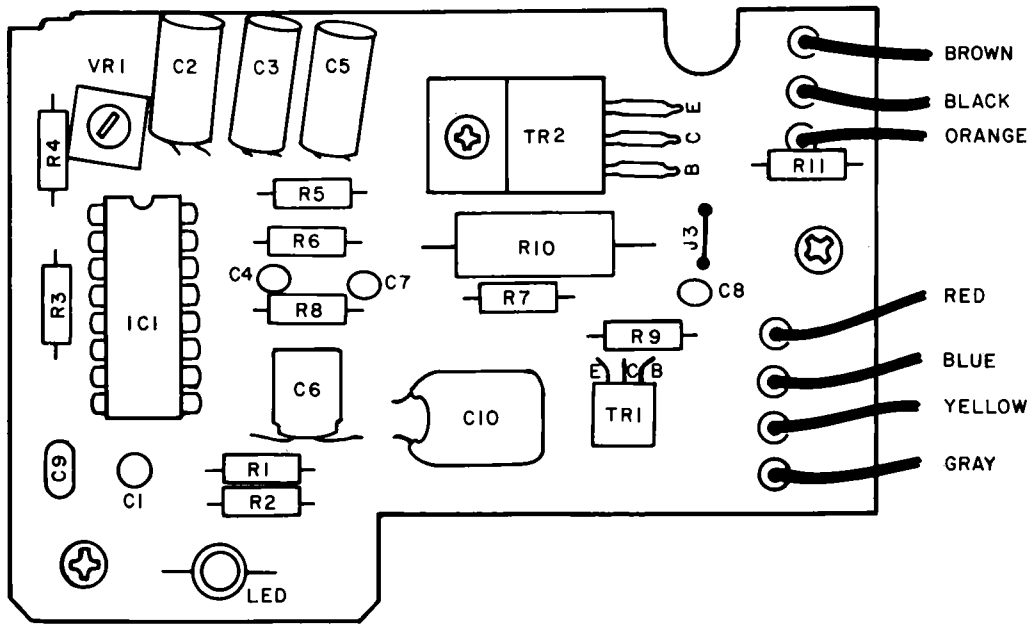


Fig. A-24. Drive motor servo circuit parts layout, Model 1542.

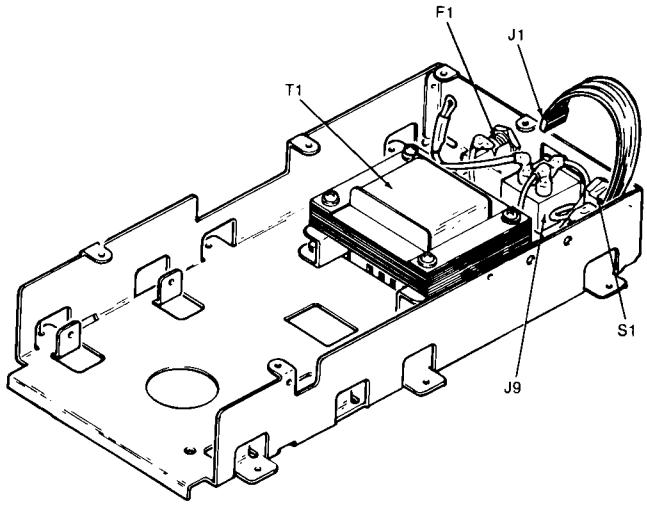


Fig. A-25. Frame assembly parts layout, Model 1540.

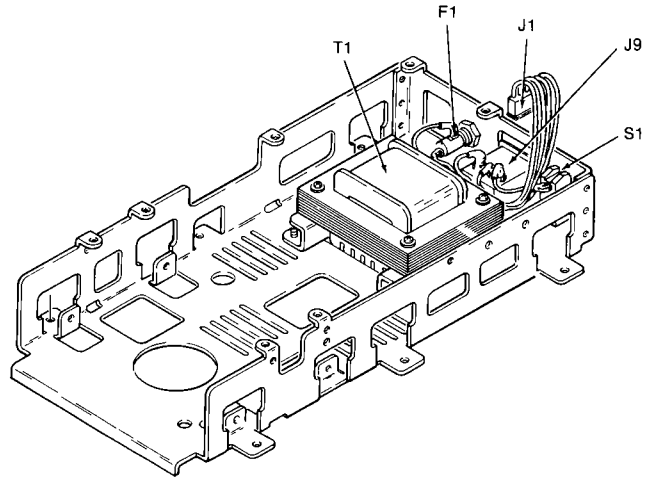


Fig. A-26. Frame assembly parts layout, Models 1541 and 1542.

A.5 MODEL 1540 PARTS LIST

A.5.1 Disk Controller PC Board

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C1	Capacitor	1.0 μF, 50 V
C2	Capacitor	47 μF, 16 V
C3	Capacitor	0.1 μF
C4	Capacitor	1.0 μF, 50 V
C5	Capacitor	47 μF, 16 V
C6	Capacitor	0.1 μF
C7	Capacitor	0.1 μF
C8	Capacitor	0.1 μF
C9	Capacitor	0.1 μF
C10	Capacitor	68 pF
C11	Capacitor	0.1 μF
C12	Capacitor	10 μF, 25 V
C13	Capacitor	0.1 μF
C14	Capacitor	0.1 μF
C15	Capacitor	0.47 μF, 35 V
C16	Capacitor	680 pF
C17	Capacitor	0.1 μF
C18	Capacitor	0.1 μF
C19	Capacitor	0.1 μF
C20	Capacitor	0.1 μF
C21	Capacitor	0.1 μF
C22	Capacitor	0.1 μF
C23	Capacitor	3.3 μF, 25 V
C24	Capacitor	0.47 μF, 35 V
C25	Capacitor	0.1 μF
C26	Capacitor	1000 pF
C27	Capacitor	680 pF
C28	Capacitor	330 pF
C29	Capacitor	0.1 μF
C30	Capacitor	0.1 μF
C31	Capacitor	0.1 μF
C32	Capacitor	0.1 μF
C33	Capacitor	150 pF
C34	Capacitor	0.1 μF
C35	Capacitor	0.1 μF
C36	Capacitor	0.1 μF
C37	Capacitor	0.1 μF
C38	Capacitor	0.1 μF
C39	Capacitor	0.1 μF
C40	Capacitor	0.1 μF
C41	Capacitor	0.1 μF
C42	Capacitor	0.1 μF
C43	Capacitor	0.1 μF
C44	Capacitor	0.1 μF
C45	Capacitor	0.1 μF
C46	Capacitor	0.1 μF
C47	Capacitor	0.1 μF
C48	Capacitor	0.1 μF
C49	Capacitor	330 pF
C50	Capacitor	680 pF
C51	Capacitor	6800 μF, 25 V
C52	Capacitor	10,000 μF, 16 V
C53	Capacitor	0.1 μF
C54	Capacitor	0.1 μF
C55	Capacitor	0.1 μF
C56	Capacitor	100 μF, 15 V
C57	Capacitor	0.1 μF

A.5.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C58	Capacitor	.022 μF
C59	Capacitor	.022 μF
C60	Capacitor	0.1 μF
C61	Capacitor	0.1 μF
C62	Capacitor	4.7 μF
C63	Capacitor	1.0 μF
C64	Capacitor	0.1 μF
C65	Capacitor	220 μF, 10 V
CR1	Bridge Rectifier	8241
CR2	Diode	1N4002
CR3	Bridge Rectifier	8240
CR4	Diode	1N4002
CR5	Zener Diode	3.3 V
CR6	Diode	1N4148
CR7	Diode	1N4148
CR8	Diode	1N4148
CR9	Diode	1N4148
CR10	Diode	1N4148
CR11	Diode	1N4148
CR12	Zener Diode	5.2 V
CR13	Diode	1N4002
CR14	Diode	1N4002
CR15	Diode	1N4002
CR16	Diode	1N4002
CR17	Diode	1N4002
F1	Fuse	3AG1A250V
L11	Inductor	*
L2	Inductor	*
L3	Inductor	*
L4	Inductor	*
L5	Inductor	*
L6	Inductor	*
L7	Inductor	*
L8	Inductor	*
L9	Inductor	*
L10	Inductor	*
L11	Inductor	*
L12	Inductor	*
L13	Inductor	*
L14	Inductor	*
L15	Inductor	*
L16	Inductor	*
Q1	Transistor	2SA952
Q2	Transistor	2SC945
Q3	Transistor	2SC945
Q4	Transistor	2SC2001
Q5	Transistor	2SC2001
Q6	Transistor	2SC2001
Q7	Transistor	2SC2001
Q8	Transistor	2SA1015
Q9	Transistor	2SA1015
Q10	Transistor	2SA1015
Q11	Transistor	2SA1015
R1	Resistor, ¼ W	330 Ω
R2	Resistor, ¼ W	330 Ω
R3	Resistor, ¼ W	47 Ω
R4	Not Used	
R5	Resistor, ¼ W	330 Ω
R6	Resistor, ¼ W	1.0 kΩ
R7	Resistor, ¼ W	22 kΩ
R8	Resistor, ¼ W	91 Ω, 1.0%

A.5.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
R9	Resistor, ¼ W	680 Ω
R10	Resistor, ¼ W	22 kΩ
R11	Resistor, ¼ W	1.10 kΩ
R12	Resistor, ¼ W	9.10 kΩ
R13	Resistor, ¼ W	9.10 kΩ
R14	Resistor, ¼ W	2.2 kΩ
R15	Resistor, ¼ W	2.2 kΩ
R16	Resistor, ¼ W	220 Ω
R17	Resistor, ¼ W	220 Ω
R18	Resistor, ¼ W	150 Ω
R19	Resistor, ¼ W	150 Ω
R20	Resistor, ¼ W	330 Ω
R21	Resistor, ¼ W	3.0 kΩ
R22	Resistor, ¼ W	3.0 kΩ
R23	Resistor, ¼ W	3.0 kΩ
R24	Resistor, ¼ W	510 Ω
R25	Resistor, ¼ W	360 Ω
R26	Resistor, ¼ W	2.2 kΩ
R27	Resistor, ¼ W	470 Ω
R28	Resistor, ¼ W	470 Ω
R29	Resistor, ¼ W	22 kΩ
R30	Resistor, ¼ W	360 Ω
R31	Resistor, ¼ W	1.0 kΩ
R32	Resistor, ¼ W	1.0 kΩ
R33	Resistor, ¼ W	1.0 kΩ
R34	Resistor, ¼ W	1.0 kΩ
R35	Resistor, ¼ W	150 Ω
R36	Resistor, ¼ W	150 Ω
R37	Resistor, ¼ W	330 Ω
R38	Not Used	
R39	Resistor, ¼ W	680 Ω
R40	Resistor, ¼ W	680 Ω
R41	Resistor, ¼ W	680 Ω
R42	Resistor, ¼ W	680 Ω
R43	Resistor, ¼ W	1.0 kΩ
R44	Resistor, ¼ W	100 kΩ
R45	Resistor, ¼ W	220 Ω
R46	Not Used	
R47	Resistor, ¼ W	470 Ω
R48	Resistor, ¼ W	1.5 kΩ
R49	Resistor, ¼ W	100 Ω
R50	Resistor, ¼ W	470 Ω
R51	Resistor, ¼ W	2.2 kΩ
R52	Resistor, ¼ W	2.2 kΩ
R53	Resistor, ¼ W	22 kΩ
R54	Resistor, ¼ W	150 Ω
R55	Resistor, ¼ W	470 Ω
R56	Resistor, ¼ W	2.2 kΩ
R57	Resistor, ¼ W	470 Ω
R58	Resistor, ¼ W	1.0 kΩ
UA2	1024 × 4-Bit Static RAM	2114L3
UA3	1024 × 4-Bit Static RAM	2114L3
UAB1	Versatile Interface Adapter	6522
UAB4	8K × 8 ROM	235302-01
UAB5	8K × 8 ROM	981229-01
UB2	1024 × 4-Bit Static RAM	2114L3
UB3	1024 × 4-Bit Static RAM	2114L3
UB6	Hex Inverter	74LS04
UB7	Quad 2-Input Pos. NAND Gate	74LS00
UB8	BCD-to-Decimal Decoder	74LS42

A.5.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
UC1	Hex Schmitt-Trigger Inverter	74LS14
UC2	13-Input Pos. NAND Gate	74LS133
UC3	Octal Bus Transceiver	74LS245
UC6	Binary Presettable Counter/ Latch	74LS197
UC7	Quad 2-Input Pos. NOR Gate	7402
UCD4	Versatile Interface Adapter	6522
UCD5	8-Bit Microprocessor	6502
UD1	Hex Inverter Buffer/Driver	7406
UD2	8-Bit Parallel Output Serial Shift Register	74LS164
UD3	Parallel Load 8-Bit Shift Register with Complementary Outputs	74LS165
UE2	Dual 2- to 4-Line Decoder/ Multiplexer	74LS139
UE3	Binary Synchronous Up/Down Counter	74LS191
UE4	Dual-D Flip-Flop	74LS74
UE5	Quad 2-Input Pos. NOR Gate	74LS02
UE7	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UF2	Hex Inverter Buffer/Driver	7406
UF3	Triple 3-Input Pos. NAND Gate	74LS10
UF4	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UF5	Quad 2-Input Pos. NAND Gate	74LS00
UF6	Dual-D Flip-Flop	74LS74
UG1	Hex Schmitt-Trigger Inverter	74LS14
UG2	Quad 2-Input Exclusive-OR Gate	74LS86
UG3	Dual Retriggerable Resettable Monostable Multivibrator	9602
UG4	Hex Buffer/Driver	7417
UH4	Comparator w/Open Collector Output	LM311
UH5	Differential Video Amplifier	NE592N
UH7	Differential Video Amplifier	NE592N
Y1	Crystal	16 MHz

* Values not available

A.5.2 Drive Motor Servo Circuit

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C1	Capacitor	10 μF, 35 V
C2	Capacitor	4700 pF
C3	Capacitor	0.033μF, 100 V
C4	Capacitor	0.47 μF, 35 V
C5	Capacitor	10 μF, 35 V
C6	Capacitor	10 μF, 35 V
C7	Capacitor	0.47 μF, 35 V
C8	Capacitor	0.013 μF, 10%
C9	Capacitor	0.47 μF, 35 V
CR1	Diode	1N4148

A.5.2 Drive Motor Servo Circuit (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
CR2	Diode	1N4148
CR3	Diode	1N4148
CR4	Diode	1N4148
CR5	Diode	1N4148
IC1	Speed Controller	Sony 2463
Q1	Transistor	25C2785
Q2	Transistor	25C2785
Q3	Transistor	25A1015
Q4	Transistor	25B569
R1	Resistor	10 kΩ
R2	Resistor	68 kΩ
R3	Resistor	220 Ω
R4	Resistor	3.3 kΩ
R5	Resistor	2.7 kΩ
R6	Resistor	820 Ω
R7	Resistor	10 kΩ
R8	Resistor	0.68 Ω, 3 W
R10	Resistor	3.32 kΩ
VR1	Variable Resistor	20 kΩ

A.6 MODEL 1541 PARTS LIST

A.6.1 Disk Controller PC Board

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C1	Capacitor	1.0 μF, 50 V
C2	Capacitor	47 μF, 16 V
C3	Capacitor	0.1 μF
C4	Capacitor	1.0 μF, 50 V
C5	Capacitor	47 μF,16 V
C6	Capacitor	0.1 μF
C7	Capacitor	0.1 μF
C8	Capacitor	0.1 μF
C9	Capacitor	0.1 μF
C10	Capacitor	0.1 μF
C11	Capacitor	1.0 μF
C12	Capacitor	0.33 μF
C13	Capacitor	220 μF, 25 V
C14	Capacitor	1.0 μF
C15	Capacitor	10 μF, 25 V
C16	Capacitor	4700 μF, 16 V
C17	Capacitor	6800 μF, 25 V
C18	Capacitor	0.1 μF
C19	Capacitor	0.1 μF
C20	Capacitor	0.1 μF
C21	Capacitor	4.7 μF
C22	Capacitor	0.1 μF
C23	Capacitor	0.1 μF
C24	Capacitor	0.1 μF
C25	Capacitor	0.1 μF
C26	Capacitor	0.1 μF
C27	Capacitor	0.1 μF
C28	Capacitor	0.1 μF
C29	Capacitor	0.1 μF
C30	Capacitor	0.1 μF

A.6.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C31	Capacitor	150 pF
C32	Capacitor	330 pF
C33	Capacitor	680 pF
C34	Capacitor	680 pF
C35	Capacitor	0.1 μF
C36	Capacitor	330 pF
C37	Capacitor	0.47 μF, 35 V
C38	Capacitor	0.47 μF, 35 V
C39	Capacitor	0.022 μF
C40	Capacitor	0.1 μF
C41	Capacitor	1000 pF
C42	Capacitor	0.022 μF
C43	Capacitor	0.1 μF
C44	Capacitor	3.3 μF, 25 V
C45	Capacitor	680 pF
C46	Capacitor	100 μF, 15 V
C47	Capacitor	0.1 μF
C48	Capacitor	0.1 μF
CR1	Bridge Rectifier	8241
CR2	Diode	1N4002
CR3	Bridge Rectifier	8240
CR4	Diode	1N4002
CR5	Zener Diode	3.3 V
CR6	Diode	1N4148
CR7	Diode	1N4002
CR8	Diode	1N4002
CR9	Diode	1N4002
CR10	Diode	1N4002
CR11	Diode	1N4002
CR12	Diode	1N4148
CR13	Zener Diode	5.2 V
CR14	Diode	1N4148
CR15	Diode	1N4148
CR16	Diode	1N4148
CR17	Diode	1N4148
CR18	Diode	1N4148
L1	Inductor	2.2 μH
L2	Inductor	*
L3	Inductor	*
L4	Inductor	*
L5	Inductor	*
L6	Inductor	*
L7	Inductor	*
L8	Inductor	100 μH
L9	Inductor	*
L10	Inductor	*
L11	Inductor	*
L12	Inductor	*
L13	Inductor	*
L14	Inductor	*
L15	Inductor	*
L16	Inductor	*
Q1	Transistor	A952
Q2	Transistor	C945
Q3	Transistor	25A1015
Q4	Transistor	25A1015
Q5	Transistor	25A1015
Q6	Transistor	25A1015
Q7	Transistor	25C945
Q8	Transistor	25C2001
Q9	Transistor	25C2001

A.6.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
Q10	Transistor	25C2001
Q11	Transistor	25C2001
R1	Resistor, ¼ W	47 Ω
R2	Resistor, ¼ W	1.0 kΩ
R3	Resistor, ¼ W	330 Ω
R4	Resistor, ¼ W	220 Ω
R5	Resistor, ¼ W	1.0 kΩ
R6	Resistor, ¼ W	1.0 kΩ
R7	Resistor, ¼ W	1.0 kΩ
R8	Resistor, ¼ W	1.0 kΩ
R9	Resistor, ¼ W	2.0 kΩ
R10	Resistor, ¼ W	2.0 kΩ
R11	Resistor, ¼ W	2.2 kΩ
R12	Resistor, ¼ W	22 kΩ
R13	Resistor, ¼ W	
R14	Resistor, ¼ W	360 Ω
R16	Resistor, ¼ W	200 Ω
R17	Resistor, ¼ W	150 Ω
R18	Resistor, ¼ W	150 Ω
R19	Resistor, ¼ W	360 Ω
R20	Resistor, ¼ W	470 Ω
R21	Resistor, ¼ W	2.2 kΩ
R22	Resistor, ¼ W	470 Ω
R23	Resistor, ¼ W	330 Ω
R24	Resistor, ¼ W	360 Ω
R25	Resistor, ¼ W	1.0 kΩ
R26	Resistor, ¼ W	2.0 kΩ
R27	Resistor, ¼ W	510 Ω
R28	Resistor, ¼ W	100 Ω
R29	Resistor, ¼ W	150 Ω
R30	Resistor, ¼ W	470 Ω
R31	Resistor, ¼ W	330 Ω
R32	Resistor, ¼ W	2.2 kΩ
R33	Resistor, ¼ W	2.2 kΩ
R34	Resistor, ¼ W	2.2 kΩ
R35	Resistor, ¼ W	22 kΩ
R36	Resistor, ¼ W	220 Ω
R37	Resistor, ¼ W	470 Ω
R38	Resistor, ¼ W	470 Ω
R39	Resistor, ¼ W	22 kΩ
R40	Resistor, ¼ W	1.5 kΩ
R41	Resistor, ¼ W	470 Ω
R42	Resistor, ¼ W	680 Ω
R43	Resistor, ¼ W	1.0 kΩ
R44	Resistor, ¼ W	100 kΩ
R45	Resistor, ¼ W	150 Ω
R46	Resistor, ¼ W	150 Ω
R47	Resistor, ¼ W	680 Ω
R48	Resistor, ¼ W	680 Ω
R49	Resistor, ¼ W	680 Ω
R50	Resistor, ¼ W	680 Ω
R51	Resistor, ¼ W	91 Ω, 1%
R52	Resistor, ¼ W	22 kΩ
R53	Resistor, ¼ W	910 kΩ
R54	Resistor, ¼ W	910 kΩ
R55	Resistor, ¼ W	220 Ω
UA1	Hex Schmitt-Trigger Inverter	74LS14
UB1	Hex Inverter Buffer/Driver	7406
UB2	2K × 8 RAM	2016
UB3	8K × 8 ROM	235302-01
UB4	8K × 8 ROM	901229-03

A.6.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
UC1	Logic Array	325572-01
UC2	Versatile Interface Adapter	6522
UC3	Versatile Interface Adapter	6522
UC4	8-Bit Microprocessor	6502
UD1	Hex Inverter Buffer/Driver	7406
UD2	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UD3	Quad 2-Input Exclusive-OR Gate	74LS86
UD4	Dual Retriggerable Resettable Monostable Multivibrator	9602
UD5	Binary Presettable Counter/ Latch	74LS197
UE4	Comparator w/Open Collector Output	LM311
UE6	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UF3	Differential Video Amplifier	NE592N
UF4	Differential Video Amplifier	NE592N
Y1	Crystal	16 MHz

*Values not available

A.6.2 Drive Motor Servo Circuit

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C1	Capacitor	10 μF, 35 V
C2	Capacitor	4700 pF
C3	Capacitor	0.033 μF, 100 V
C4	Capacitor	0.47 μF, 35 V
C5	Capacitor	10 μF, 35 V
C6	Capacitor	10 μF, 35 V
C7	Capacitor	0.47 μF, 35 V
C8	Capacitor	0.013 μF, 10%
C9	Capacitor	0.47 μF, 35 V
CR1	Diode	1N4148
CR2	Diode	1N4148
CR3	Diode	1N4148
CR4	Diode	1N4148
CR5	Diode	1N4148
IC1	Speed Controller	Sony 2463
Q1	Transistor	25C2785
Q2	Transistor	25C2785
Q3	Transistor	25A1015
Q4	Transistor	25B569
R1	Resistor	10 kΩ
R2	Resistor	68 kΩ
R3	Resistor	220 Ω
R4	Resistor	3.3 kΩ
R5	Resistor	2.7 kΩ
R6	Resistor	820 Ω
R7	Resistor	10 kΩ
R8	Resistor	0.68 Ω, 3 W
R10	Resistor	3.32 kΩ
VR1	Variable Resistor	20 kΩ

A.7 MODEL 1542 PARTS LIST

A.7.1 Disk Controller PC Board

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C1	Capacitor	1.0 μF, 50 V
C2	Capacitor	47 μF, 16 V
C3	Capacitor	0.1 μF
C4	Capacitor	1.0 μF, 50 V
C5	Capacitor	47 μF, 16 V
C6	Capacitor	0.1 μF
C7	Capacitor	0.1 μF
C8	Capacitor	0.1 μF
C9	Capacitor	0.1 μF
C10	Capacitor	0.1 μF
C11	Capacitor	1.0 μF
C12	Capacitor	0.33 μF
C13	Capacitor	220 μF, 25 V
C14	Capacitor	1.0 μF
C15	Capacitor	10 μF, 25 V
C16	Capacitor	4700 μF, 16 V
C17	Capacitor	6800 μF, 25 V
C18	Capacitor	0.1 μF
C19	Capacitor	0.1 μF
C20	Capacitor	0.1 μF
C21	Capacitor	4.7 μF
C22	Capacitor	0.1 μF
C23	Capacitor	0.1 μF
C24	Capacitor	0.1 μF
C25	Capacitor	0.1 μF
C26	Capacitor	0.1 μF
C27	Capacitor	0.1 μF
C28	Capacitor	0.1 μF
C29	Capacitor	0.1 μF
C30	Capacitor	0.1 μF
C31	Capacitor	150 pF
C32	Capacitor	330 pF
C33	Capacitor	680 pF
C34	Capacitor	680 pF
C35	Capacitor	0.1 μF
C36	Capacitor	330 pF
C37	Capacitor	0.47 μF, 35 V
C38	Capacitor	0.47 μF, 35 V
C39	Capacitor	0.022 μF
C40	Capacitor	0.1 μF
C41	Capacitor	1000 pF
C42	Capacitor	0.022 μF
C43	Capacitor	0.1 μF
C44	Capacitor	3.3 μF, 25 V
C45	Capacitor	680 μF
C46	Capacitor	100 μF, 15 V
C47	Capacitor	0.1 μF
C48	Capacitor	0.1 μF
CR1	Bridge Rectifier	8241
CR2	Diode	1N4002
CR3	Bridge Rectifier	8240
CR4	Diode	1N4002
CR5	Zener Diode	3.3 V
CR6	Diode	1N4148
CR7	Diode	1N4002
CR8	Diode	1N4002
CR9	Diode	1N4002

A.7.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
CR10	Diode	1N4002
CR11	Diode	1N4002
CR12	Diode	1N4148
CR13	Zener Diode	5.2 V
CR14	Diode	1N4148
CR15	Diode	1N4148
CR16	Diode	1N4148
CR17	Diode	1N4148
CR18	Diode	1N4148
L1	Inductor	2.2 μH
L2	Inductor	*
L3	Inductor	*
L4	Inductor	*
L5	Inductor	*
L6	Inductor	*
L7	Inductor	*
L8	Inductor	100 μH
L9	Inductor	*
L10	Inductor	*
L11	Inductor	*
L12	Inductor	*
L13	Inductor	*
L14	Inductor	*
L15	Inductor	*
L16	Inductor	*
Q1	Transistor	A952
Q2	Transistor	C945
Q3	Transistor	25A1015
Q4	Transistor	25A1015
Q5	Transistor	25A1015
Q6	Transistor	25A1015
Q7	Transistor	25C945
Q8	Transistor	25C2001
Q9	Transistor	25C2001
Q10	Transistor	25C2001
Q11	Transistor	25C2001
R1	Resistor, ¼ W	47 Ω
R2	Resistor, ¼ W	1.0 kΩ
R3	Resistor, ¼ W	330 Ω
R4	Resistor, ¼ W	220 Ω
R5	Resistor, ¼ W	1.0 kΩ
R6	Resistor, ¼ W	1.0 kΩ
R7	Resistor, ¼ W	1.0 kΩ
R8	Resistor, ¼ W	1.0 kΩ
R9	Resistor, ¼ W	2.0 kΩ
R10	Resistor, ¼ W	2.0 kΩ
R11	Resistor, ¼ W	2.2 kΩ
R12	Resistor, ¼ W	22 kΩ
R13	Resistor, ¼ W	
R14	Resistor, ¼ W	360 Ω
R16	Resistor, ¼ W	200 Ω
R17	Resistor, ¼ W	150 Ω
R18	Resistor, ¼ W	150 Ω
R19	Resistor, ¼ W	360 Ω
R20	Resistor, ¼ W	470 Ω
R21	Resistor, ¼ W	2.2 kΩ
R22	Resistor, ¼ W	470 Ω
R23	Resistor, ¼ W	330 Ω
R24	Resistor, ¼ W	360 Ω
R25	Resistor, ¼ W	1.0 kΩ
R26	Resistor, ¼ W	2.0 kΩ

A.7.1 Disk Controller PC Board (cont.)

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
R27	Resistor, ¼ W	510 Ω
R28	Resistor, ¼ W	100 Ω
R29	Resistor, ¼ W	150 Ω
R30	Resistor, ¼ W	470 Ω
R31	Resistor, ¼ W	330 Ω
R32	Resistor, ¼ W	2.2 kΩ
R33	Resistor, ¼ W	2.2 kΩ
R34	Resistor, ¼ W	2.2 kΩ
R35	Resistor, ¼ W	22 kΩ
R36	Resistor, ¼ W	220 Ω
R37	Resistor, ¼ W	470 Ω
R38	Resistor, ¼ W	470 Ω
R39	Resistor, ¼ W	22 kΩ
R40	Resistor, ¼ W	1.5 kΩ
R41	Resistor, ¼ W	470 Ω
R42	Resistor, ¼ W	680 Ω
R43	Resistor, ¼ W	1.0 kΩ
R44	Resistor, ¼ W	100 kΩ
R45	Resistor, ¼ W	150 Ω
R46	Resistor, ¼ W	150 Ω
R47	Resistor, ¼ W	680 Ω
R48	Resistor, ¼ W	680 Ω
R49	Resistor, ¼ W	680 Ω
R50	Resistor, ¼ W	680 Ω
R51	Resistor, ¼ W	91 Ω, 1%
R52	Resistor, ¼ W	22 kΩ
R53	Resistor, ¼ W	910 kΩ
R54	Resistor, ¼ W	910 kΩ
R55	Resistor, ¼ W	220 Ω
UA1	Hex Schmitt-Trigger Inverter	74LS14
UB1	Hex Inverter Buffer/Driver	7406
UB2	2K × 8 RAM	2016
UB3	8K × 8 ROM	235302-01
UB4	8K × 8 ROM	901229-05
UC1	Logic Array	325572-01
UC2	Versatile Interface Adapter	6522
UC3	Versatile Interface Adapter	6522
UC4	8-Bit Microprocessor	6502
UC6	Hex Inverter	7713
UC7	Quad 2-Input Pos. NAND Gate	74LS00
UC8	BCD-to-Decimal Decoder	74LS42
UD1	Hex Inverter Buffer/Driver	7406
UD2	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UD3	Quad 2-Input Exclusive-OR Gate	74LS86
UD4	Dual Retriggerable Resettable Monostable Multivibrator	9602
UD5	Binary Presettable Counter/ Latch	74LS197
UE4	Comparator w/Open Collector Output	LM311
UE6	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UF3	Differential Video Amplifier	NE592N
UF4	Differential Video Amplifier	NE592N
Y1	Crystal	16 MHz

* Values not available

A.7.2 Drive Motor Servo Circuit

DESIGNATOR	DESCRIPTION	VALUE/PART NUMBER
C1	Capacitor	1.0 μF, 50 V
C2	Capacitor	10 μF, 35 V
C3	Capacitor	10 μF, 35 V
C4	Capacitor	0.47 μF, 50 V
C5	Capacitor	10 μF, 35 V
C6	Capacitor	0.068 μF, 50 V, 10%
C7	Capacitor	2.2 μF, 50 V
C8	Capacitor	0.47 μF, 50 V
C9	Capacitor	100 pF, 50 V, 10%
C10	Capacitor	0.033 μF, 100 V, 10%
IC1	Governor	LAG 570
R1	Resistor	1.0 kΩ
R2	Resistor	1.0 kΩ
R3	Resistor	5.1 kΩ, 3%
R4	Resistor	68 kΩ, 1%
R5	Resistor	100 Ω
R6	Resistor	3.3 kΩ
R7	Resistor	820 Ω
R8	Resistor	2.7 kΩ
R9	Resistor	150 Ω
R10	Resistor	0.68 Ω, 3 W
R11	Resistor	5.6 kΩ
TR1	Transistor	2SB633E
TR2	Transistor	2SA733
VR1	Variable Resistor	20 kΩ

APPENDIX B

Fabrication of Video Detector

Materials Required

- One set of meter leads
- One capacitor, 0.01 μF, 50 V
- One resistor, 1.0 kΩ, 10%, $\frac{1}{4}$ W
- One diode, 1N4148 or equivalent

Equipment and Supplies

- Knife
- Soldering iron
- Wire cutters
- Needle-nose pliers
- Heat shrink tubing, $\frac{1}{2}$ inch
- Heat shrink tubing, $\frac{3}{16}$ inch
- Solder, 60/40 resin core
- Scale (ruler)
- Ohmmeter
- String or two wire ties

Preparation

1. Cut meter leads as shown in Fig. B-1:

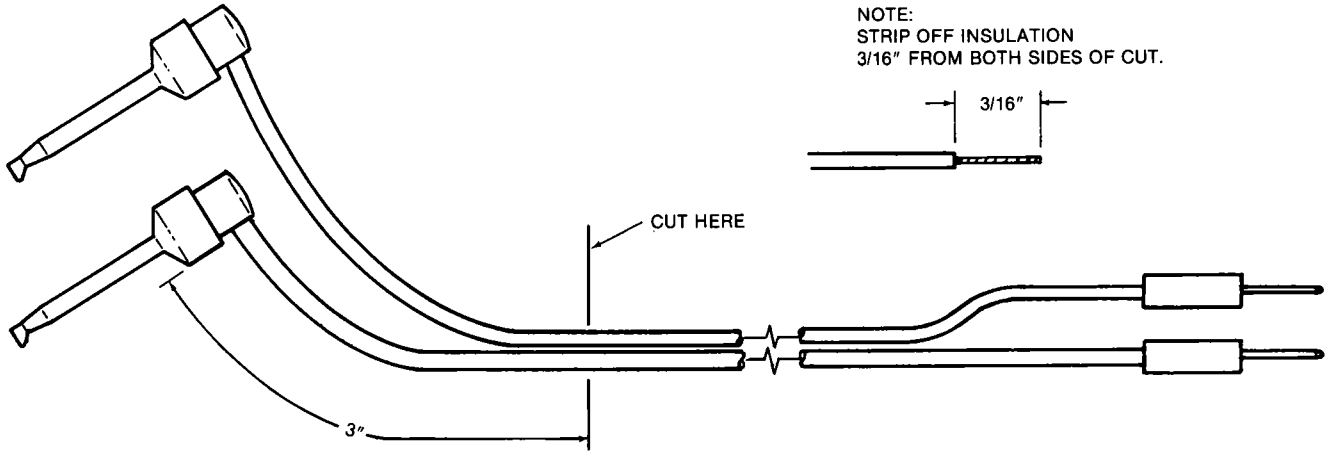


Fig. B-1. Preparation, step 1.

2. Prepare diode as shown in Fig. B-2:

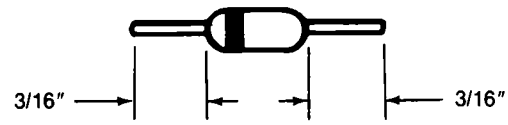


Fig. B-2. Preparation, step 2.

3. Prepare resistor as shown in Fig. B-3:

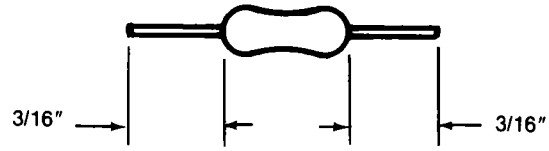


Fig. B-3. Preparation, step 3.

4. Tin all leads on resistor, diode, and meter leads.

Assembly

1. Slide 1 ½-inch length of ⅛-inch heat shrink tubing onto red meter lead as shown in Fig. B-4. Do not shrink the tubing at this time.

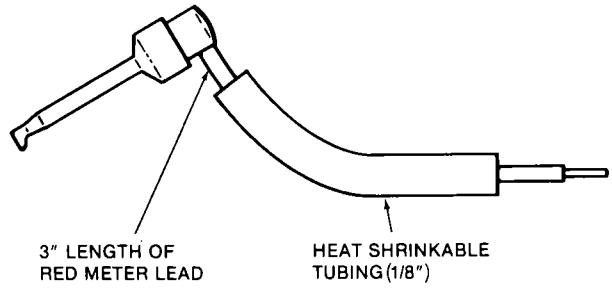


Fig. B-4. Assembly, step 1.

2. Solder diode, resistor, and remaining end of meter lead together as shown in Fig. B-5. Note proper polarity of diode.

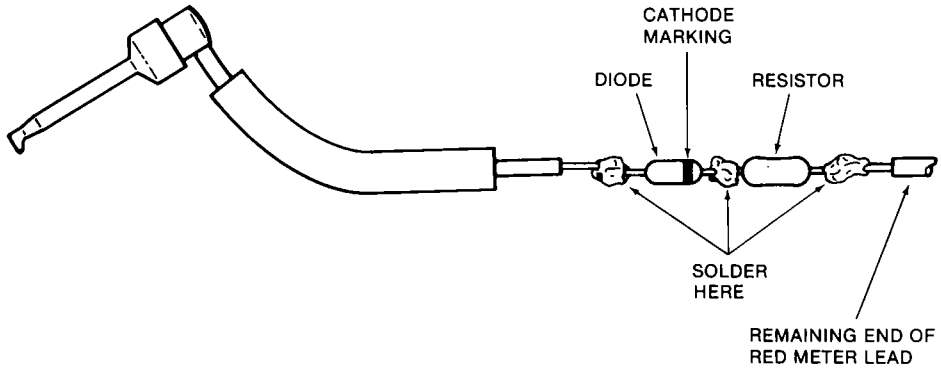


Fig. B-5. Assembly, step 2.

3. Slide heat shrink tubing over diode and resistor, leaving one lead of resistor exposed, and then shrink the tubing. See Fig. B-6.

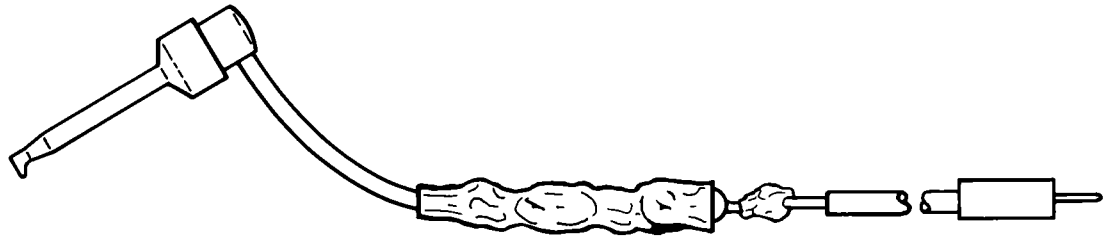


Fig. B-6. Assembly, step 3.

4. Solder capacitor and black meter leads as shown in Fig. B-7. Tie meter leads where shown.

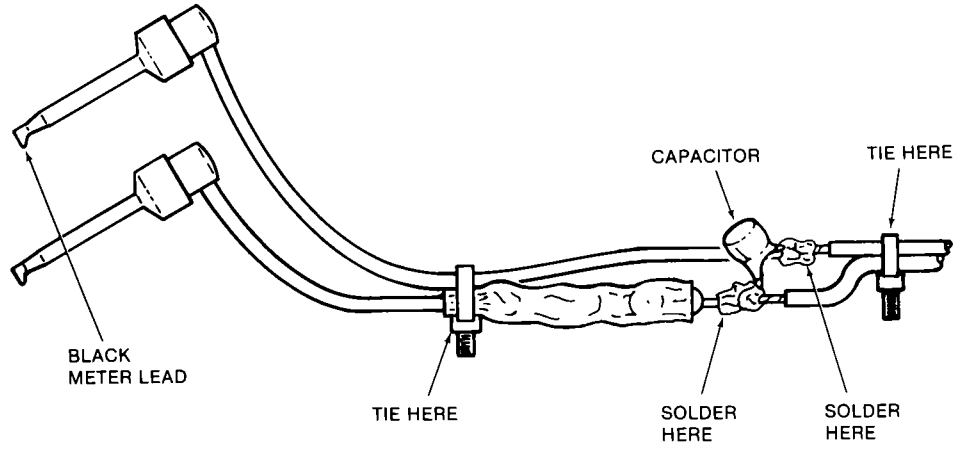


Fig. B-7. Assembly, step 4.

5. Slide a 2-inch length of ½-inch heat shrink tubing over capacitor and then shrink the tubing. See Fig. B-8.

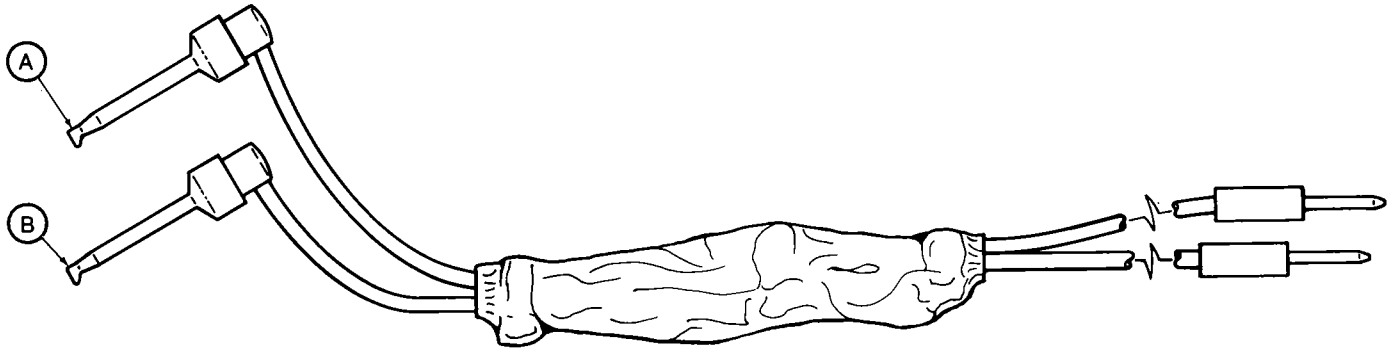


Fig. B-8. Assembly, step 5.

APPENDIX C

MOS Handling Precautions

When handling the controller board or any of the MOS ICs used in the VIC-1541, you must be aware of the possible damage to the MOS ICs from static discharge.

A static charge of only several hundred volts is enough to cause permanent damage to a MOS IC. It is not uncommon for the human body to accumulate tens of thousands of volts of static charge. The following precautions will help to reduce damage caused by static charges:

- Avoid wearing synthetic material when servicing the VIC-1541.
- Do not service the VIC-1541 in a room with carpeting on the floor.
- The use of conductive floor mats and wrist straps is advised (if possible).
- Before handling the PC board, touch a ground such as a shop ground or a cold water pipe for 30 to 60 seconds in order to discharge any static charge in your body. Also touch any tools being used or antistatic devices (i.e., conductive foam rubber or conductive packaging tubes) to the same ground.
- Avoid touching the pins of the ICs as much as possible.
- After removing a MOS IC for troubleshooting purposes, place the IC into conductive foam until it is to be reinstalled.
- When replacing MOS ICs, always ground conductive packaging to shop ground or cold water pipe before handling the IC.

APPENDIX D

Standard IC Pin Numbers

Locations of IC pin numbers are illustrated in Figs. D-1 through D-9 below. This numbering system is standard throughout the electronics industry and is not unique to the VIC-1541.

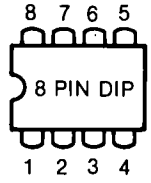


Fig. D-1. 8-pin dual in-line package.

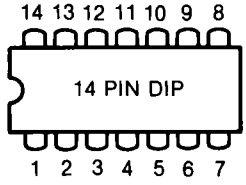


Fig. D-2. 14-pin dual in-line package.

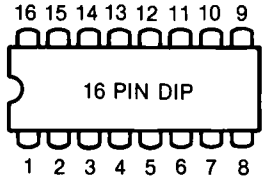


Fig. D-3. 16-pin dual in-line package.

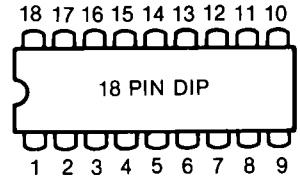


Fig. D-4. 18-pin dual in-line package.

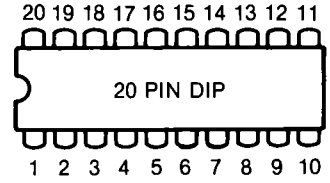


Fig. D-5. 20-pin dual in-line package.

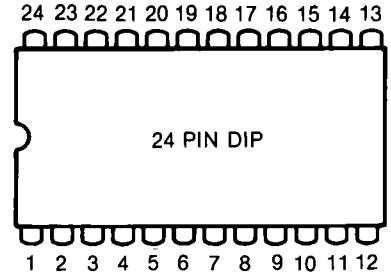


Fig. D-6. 24-pin dual in-line package.

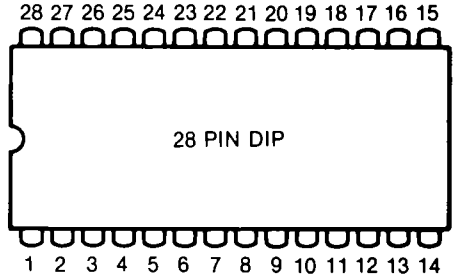


Fig. D-7. 28-pin dual in-line package.

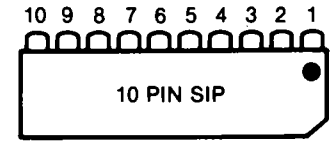


Fig. D-9. 10-pin single in-line package.

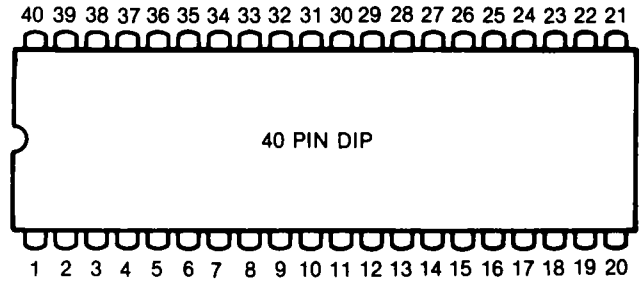


Fig. D-8. 40-pin dual in-line package.

APPENDIX E

Description of Disk Controller IC

When Commodore upgraded the VIC-1541 from Model 1540 to Model 1541, they created a custom integrated circuit. This integrated circuit (UC1, Models 1541 and 1542) reduces power consumption, heat, and production costs. The pin description of this integrated circuit is illustrated in Fig. E-1.

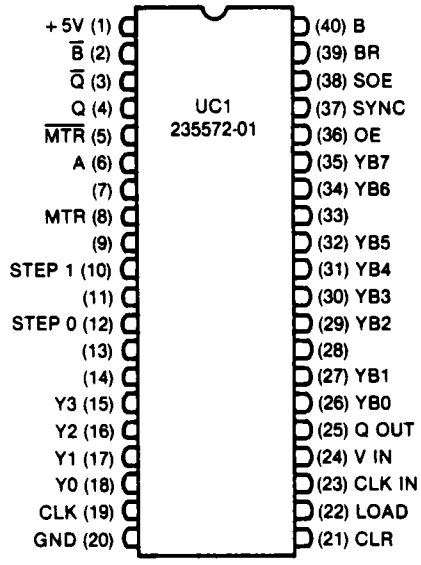


Fig. E-1. Disk controller integrated circuit, pinouts.

A block diagram of this disk controller integrated circuit is shown in Fig. E-2.

Internally, this integrated circuit contains essentially the same circuit that is used in the 1540. Table E-1 lists the parts that are integrated into the new disk controller integrated circuit. For theory of operation of these parts, refer to the theory of operation for Model 1541 (Chapter 7, Section 7.2). The encoder/decoder track select and read circuits are affected by this integrated circuit.

Table E-1. Parts Integrated into UC1

UC1B	UE5D
UC2	UF2D
UC3	UF3A
UD2	UF3B
UD3	UF3C
UE2	UF4
UE3	UF5A
UE4A	UF5B
UE4B	UF5C
UE5A	UF6A
UE5B	UF6B
UE5C	UG2C

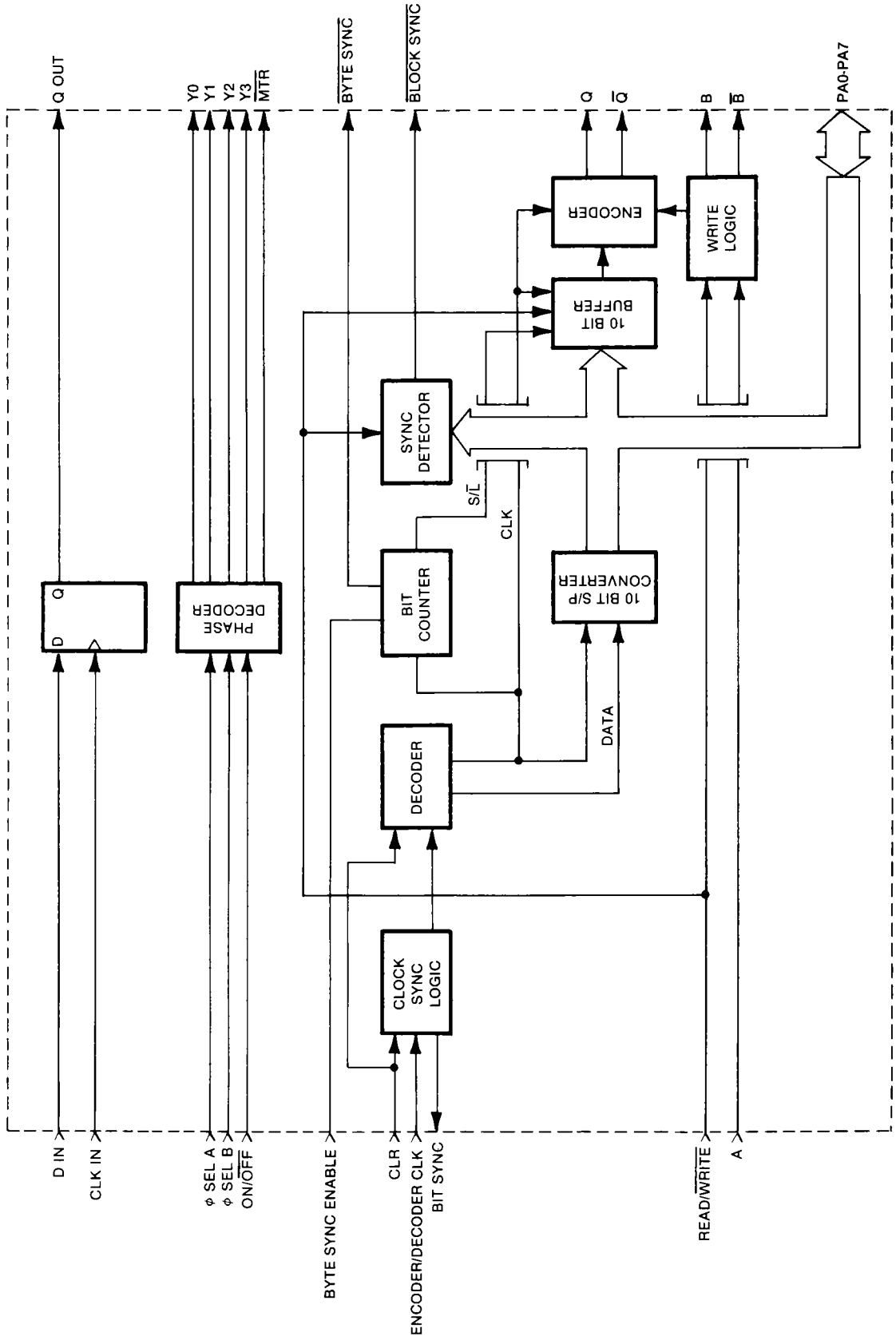


Fig. E-2. Disk controller integrated circuit, block diagram.

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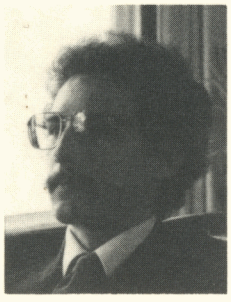

Mike Peltier is an experienced electronics technician, technical writer, inventor of electronic devices, and designer of video games, with four years' experience in electronics servicing and repair in the Air Force. Mr. Peltier has written numerous technical manuals associated with the electronics service industry.

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