YAMAHA CS-10
SERVICE MANUAL

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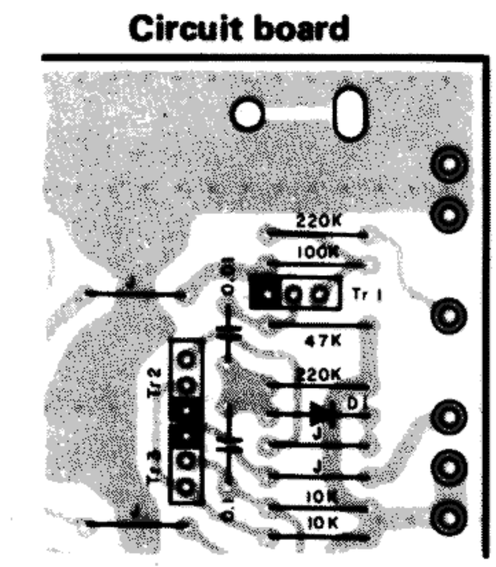
PARTS LIST (パーツリスト)

CORDING GUIDE (活用の手引)

1 CIRCUIT BOARD AND WIRING

Two (2) black wires are connected to "E" on circuit board. One goes to each "E" terminal of A and FG circuit boards. In this case, the coding system is as follows:

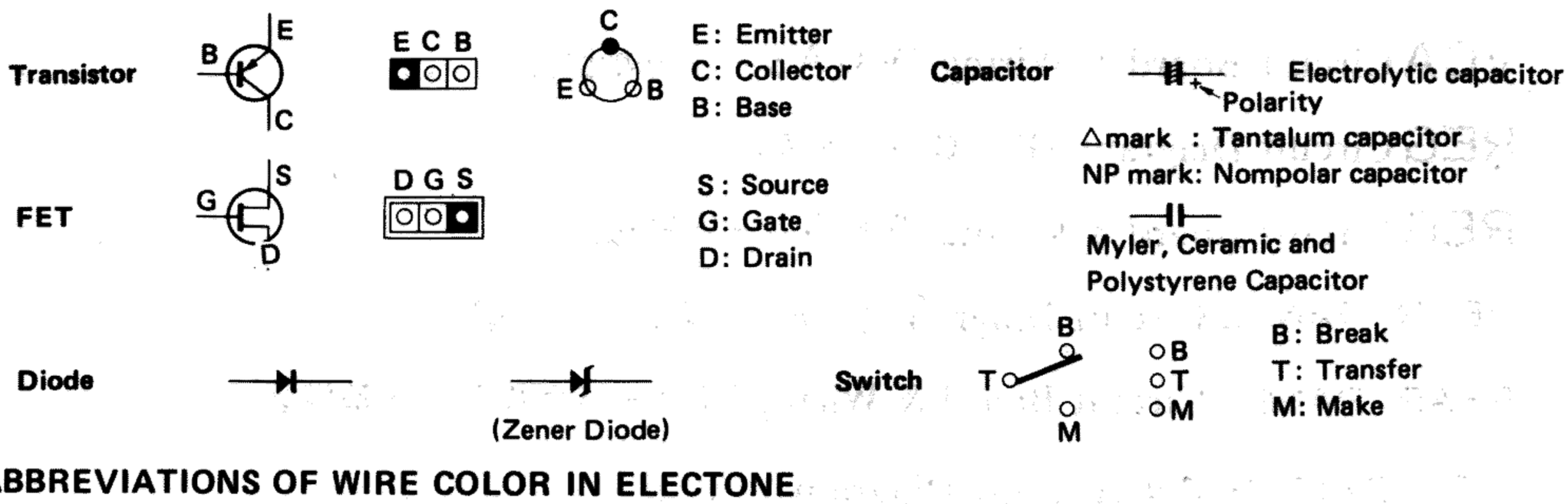


[The pattern shows the view from the side parts mounted]

(2) E BL12 x 2 RA-A-E(2) / RA-FG-E(2)

- Color of wire.
- Number of stands contained in the core. (In case of 8 cores, the number is not shown.)
- Number of wires.
- Terminal point physical eyelet space location
- Terminal reference.
- Unit (Board).
- Rack general physical location.
- Terminal point shown on the board. (Solder eyelet space number)
- Terminal E shown on the board.

2 SYMBOL DESCRIPTION



3 ABBREVIATIONS OF WIRE COLOR IN ELECTONE

BLACK	BL	BROWN	BR	RED	RE
ORANGE	OR	YELLOW	YE	GREEN	GR
BLUE	BE	VIOLET	VI	GRAY	GY
WHITE	WH	GRASS GREEN	GG	SKY BLUE	SB
PINK	PK	TRANSPAPENT	TR		

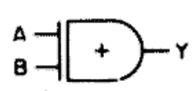
4 WIRE COLOR — Musical Note Indication

C	C#	D	D#	E	F	F#	G	G#	A	A#	B
BR	RE	OR	YE	GR	BE	VI	GY	WH	GG	SB	PK

5 LOGIC SYMBOL

	MIL	YAMAHA
NOT	A — Y	A — Y
NOR	A, B — Y	A, B — + — Y
NAND	A, B — Y	A, B — • — Y

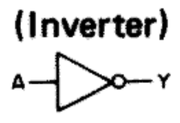
Exlusive OR



Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

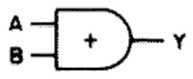
NOT (Inverter)



Truth Table

A	Y
0	1
1	0

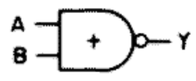
OR



Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

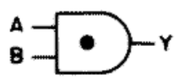
NOR



Truth Table

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

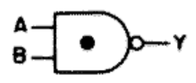
AND



Truth Table

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

NAND



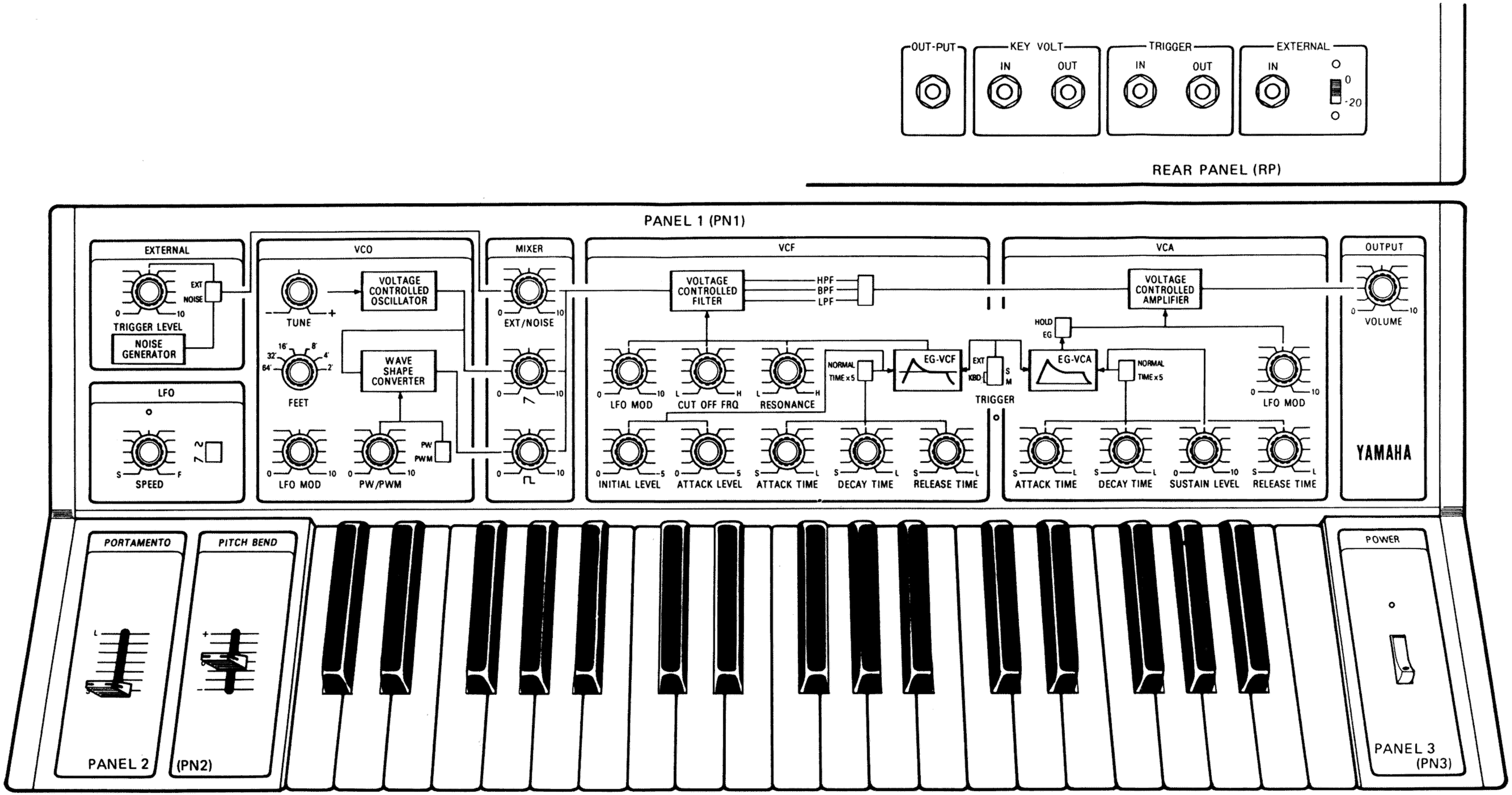
Truth Table

A	B	Y
0	0	1
1	0	1
0	1	1
0	0	0

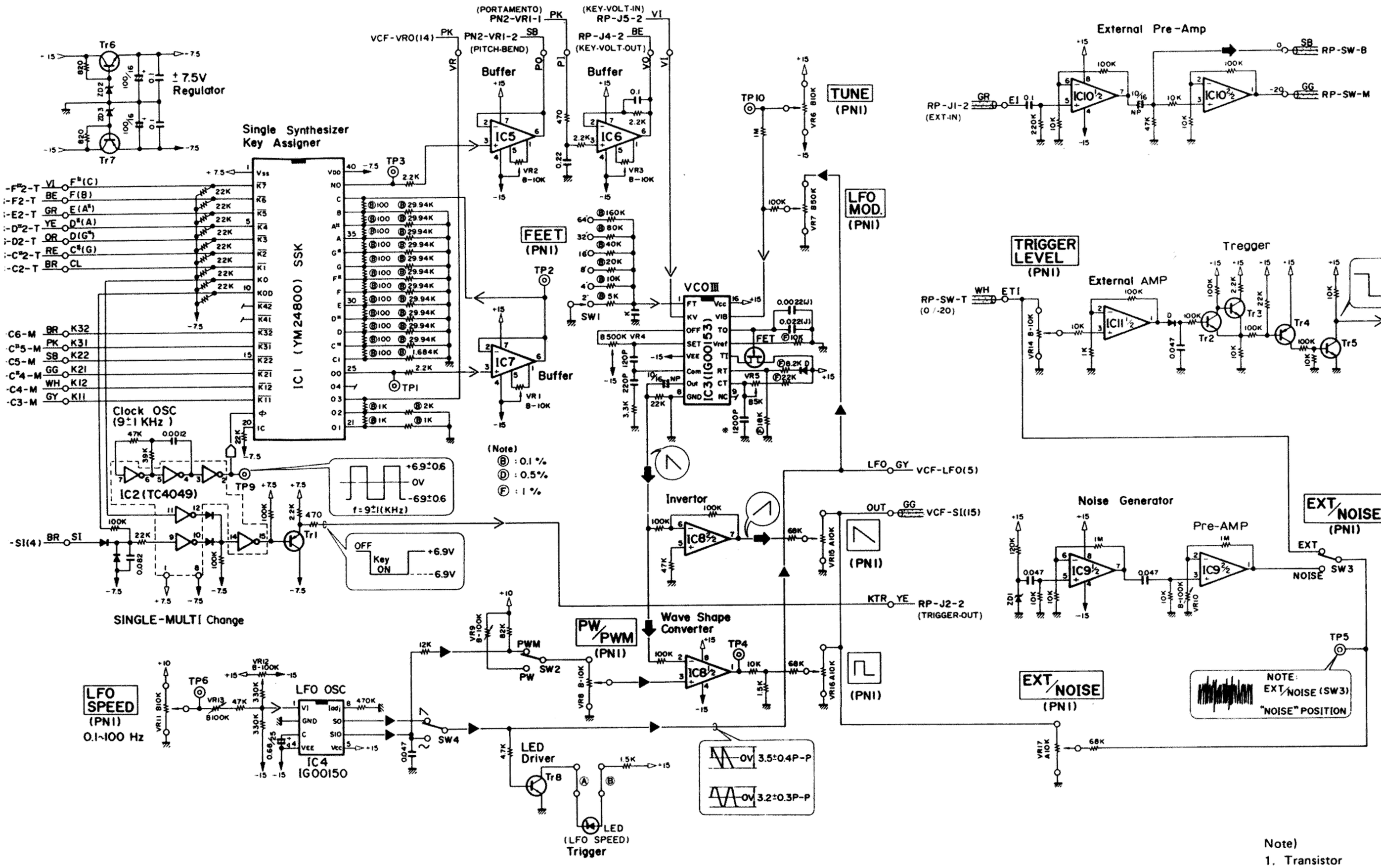
SPECIFICATIONS (総合仕様)

Keyboard	:	37 keys, C_3 ～ C_6 (3 octaves)
VCO Section	:	
1. Feet	:	2', 4', 8', 16', 32' and 64' selectable
2. Tune	:	–50 ～ +50 cent. variable
3. LFO Mod.	:	±60 cent. (Max.)
4. PW	:	50 ～ 90% variable
PWM	:	75 ± 20% (Max.) (with LFO sine wave applied to input)
5. Portamento	:	Short ～ Long (0 ～ 4 sec.)
6. Pitch Bend	:	+1 OCT ～ –1 OCT ± 20 cent.
7. Output Waveform	:	Square wave, saw-tooth wave.
VCF Section		
1. Cut Off Frequency		
2. Resonance	:	Q = 10 (Max.)
3. LFO Mod.	:	±3 OCT (Max.)
4. Envelope Generator (EG)		
Initial Level (IL)	:	0 ～ –5
Attack Level (AL)	:	0 ～ +5
Attack Time (AT)	:	1m sec. ～ 1 sec.
Decay Time (DT)	:	10m sec. ～ 10 sec.
Release Time (RT)	:	10m sec. ～ 10 sec.
5. EG Time	:	Normal/X5 selectable
6. Output Selection	:	LPF, BPF and HPF selectable.
VCA Section		
1. LFO Mod.	:	AM modulation 100% (Max.)
2. Envelope Generator (EG)		
Attack Time (AT)	:	1m sec. ～ 1 sec.
Decay Time (DT)	:	10m sec. ～ 10 sec.
Sustain Level (SL)	:	0 ～ 10
Release Time (RT)	:	10m sec. ～ 10 sec.
3. EG Time	:	Normal/X5 selectable
4. Volume	:	0 ～ Max.
Trigger Selection		
1. EXT	:	Trigger occurs when EXT input is applied.
2. SINGLE	:	When several keys are depressed simultaneously, only the first key depressed causes trigger to be generated.
3. MULTI	:	Each key depressed permits trigger to be generated (with priority given to upper tones).
LFO		
Speed	:	0.1 ～ 100Hz
Waveform	:	Sine wave and saw-tooth wave selectable
EXT		
Trigger Level	:	
Sensitivity	:	0 and –20dB selectable
Noise	:	White noise oscillation
OUT PUT LEVEL/IMPEDANCE		
	:	0dBm/600Ω (Max.)
		–20dBm/600Ω (Normal)
Power Requirements	:	AC 50/60Hz, 12W
ICs, Transistors and Diodes Employed		
	:	18 ICs, 17 transistors and 15 diodes
Dimensions	:	710mm (W) x 290mm (D) x 155mm (H)
Weight	:	8 kg approx.

PANEL LAYOUT (パネルレイアウト)



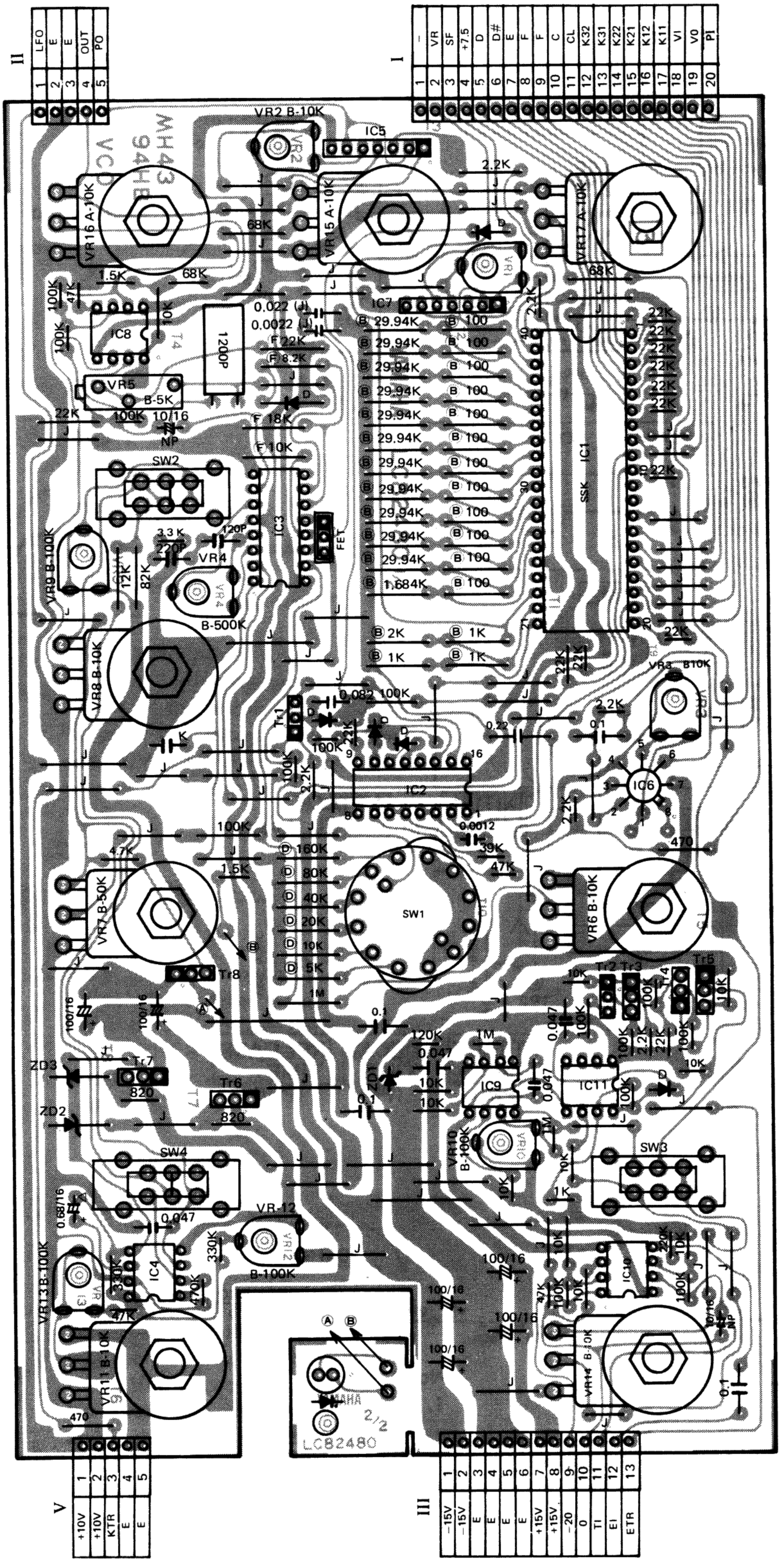
VCO Circuit Diagram



Note)

1. Transistor
   - Tr1,4,7 : 2SA561
   - Tr2,3,5,6,8 : 2SC458
2. FET : 2SK30
3. Diode
   - D : 1S1555
   - ZD1 : 1S1715P
   - ZD2,3 : 02Z7.5A
4. IC
   - IC1 : YM24800
   - IC2 : TC4049
   - IC3 : IG00153
   - IC4 : IG00150
   - IC5,7 : TA7504
   - IC6 : TA7505
   - IC8 ～11 : NJM4558

VCO Circuit Board & Wiring

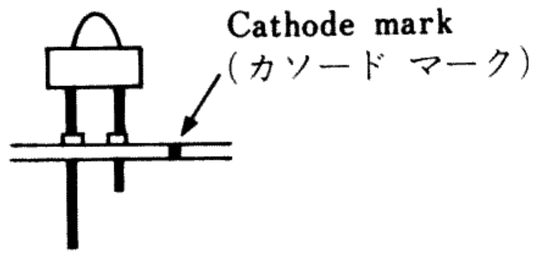


View from the printed pattern side of the circuit board.

パターン側から見た部品配置です。

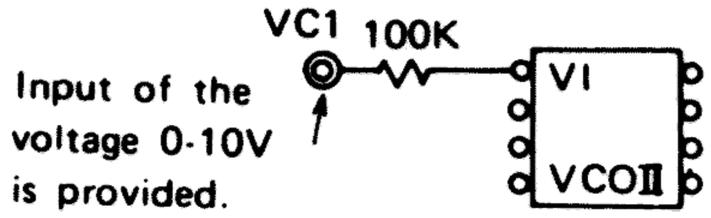
(Note)

1. Transistor (トランジスタ)
   - Tr1,4,7 : 2SA561
   - Tr2,3,5,6,8 : 2SC458
   - FET : 2SK30
2. IC
   - IC1 : YM24800
   - IC2 : TC4049
   - IC3 : IG00153
   - IC4 : IG00150
   - IC5,7 : TA7504
   - IC6 : TA7505
   - IC8～11 : NJM4558
3. Diode (ダイオード)
   - D : 1S1555
   - ZD1 : 1S1715P
   - ZD2,3 : 02Z7.5A
4. Resistor (抵抗)
   - marks : ±0.1%
   - marks : ±0.5%
   - marks : ±1%
5. △ marks : Tantalum capacitor
6. SW2～4 : 2 circuit 2 contact NON-SHORTING
7. LED : SLP1328 (発光ダイオード)

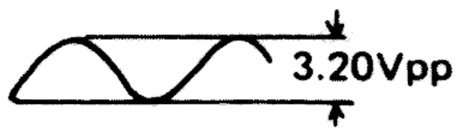


VCO II (IG00150)

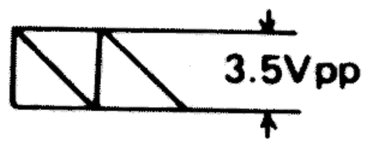
1. VI ..... Input of the control voltage.
   The frequency is variable in accordance with the voltage supplied.



2. GND ..... Earth
3. C ..... Capacitor for determination of the frequency.
4. Vee ..... −15V input power source.
5. Vcc ..... +15V input power source.
6. SIO ..... Output of sine wave.



7. SO ..... Output of sawtooth wave



8. Iadj ..... Setting for standard electric current.
   The standard electric current is set so as to be the output 200Hz when VC1 is 10V and VC2 is zero volt.

VCO III (IG00153)

This IC is used for voltage controlled oscillator.
Many defferent frequencies are produced by the voltage supplied.

1. FT ..... Resistor for determination of the feet.
   The electric current is provided to the pin from transposition changing circuit so that the octave can be determined.

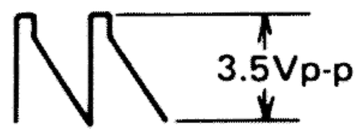
2. KV ..... Input of the key voltage
   The input of the voltage is provided to the pin in corporation with the keys held down.

   High voltage ..... High frequency
   Low voltage ..... Low frequency

Input Voltage	Output Frequency
0.250V	130.8Hz (C2)
0.500V	261.6Hz (C3)
1.000V	523.2Hz (C4)
2.000V	1046.0Hz (C5)
4.000V	2093.0Hz (C6)

Transposition "normal"

3. } OFF-SET .... Zero adjustment of input
4. } buffer circuit
5. Vee ..... −15V input power source.
6. Com .... Phase compensation for input buffer amplifier.
   Normally, the output (KV + 1V) is supplied to the pin.
7. OUT .... Output

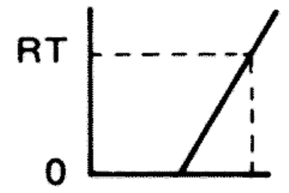


As to the frequency, refer to the Pin No.2 (KV).

8. GND ..... Earth
9. Vref ..... Input of the standard voltage.
10. CT ..... Circuit for time constant.

The following wave shape is produced.

11. RT ..... Circuit for time constant.

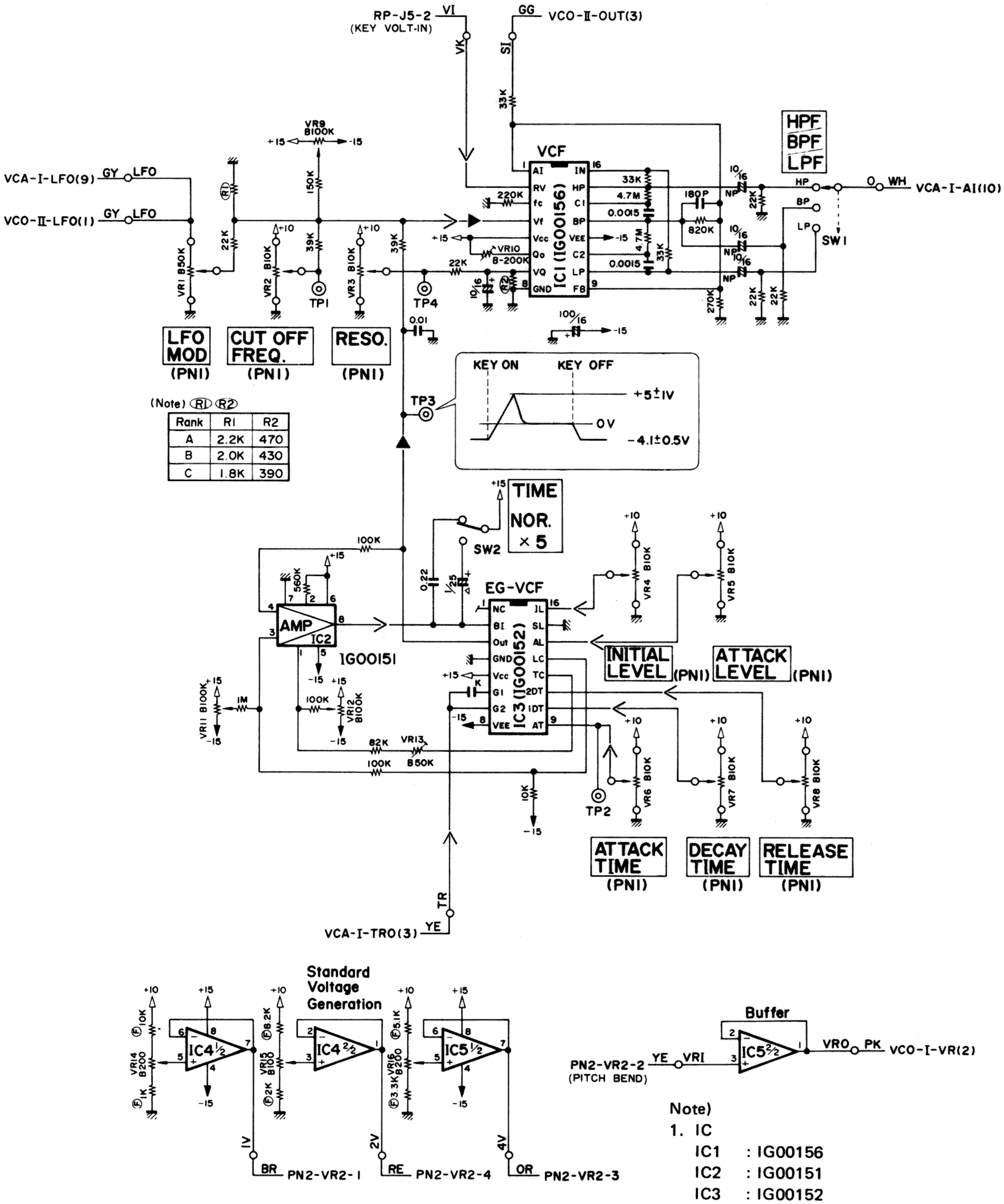


Determines the discharging voltage level.

12. T1 ..... Input for the comparator.
    Input of the wave shape (⋀⋀) is provided. from the pin no. 14 (TO).
13. Iref ····· Input of the standard electronic current
14. TO ..... Output from time constant circuit.
    ⋀⋀ The following wave shape is produced.
15. VIB ..... Input for vibrato control wave.
    Input of the control wave is provided by VCO lever of SUB-OSC.
16. Vcc ..... +15V input power source.

←- - - Explanation for IC
（ＩＣ説明）

VCF Circuit Diagram



Note)

1. IC
   - IC1 : IG00156
   - IC2 : IG00151
   - IC3 : IG00152
   - IC4,5 : NJM4558
2. R1, R2

Rank of IC1	R1	R2
A	2.2K	470
B	2.0K	430
C	1.8K	390

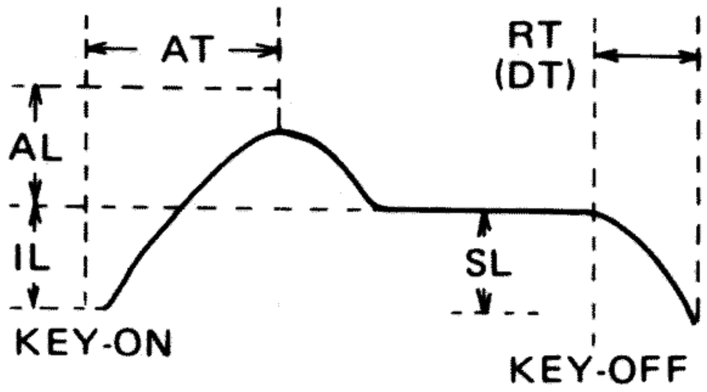
VCF-EG (IG00152)

This IC generates envelope wave shape which is supplied to VCF and control the tone color.

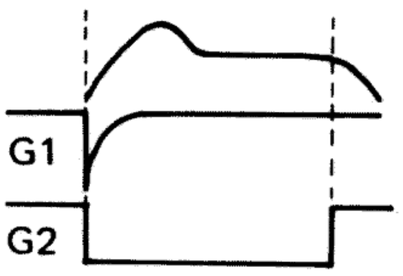
1. NC ..... Not connected
2. BI ..... Input of buffer amplifier.
3. OUT .... Output of buffer amprifier.

The buffer amplifier is built in for the purpose of matching inpedance.

Output wave shape



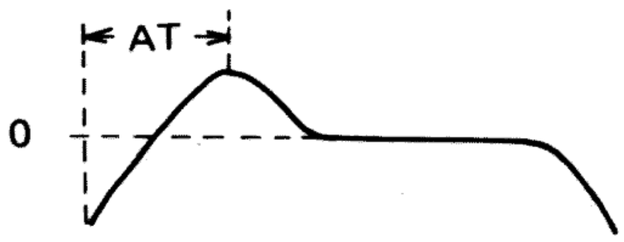
4. GND .... Earth
5. Vcc ..... +15V input power source.
6. G1 ..... Gate 1
7. G2 ..... Gate 2



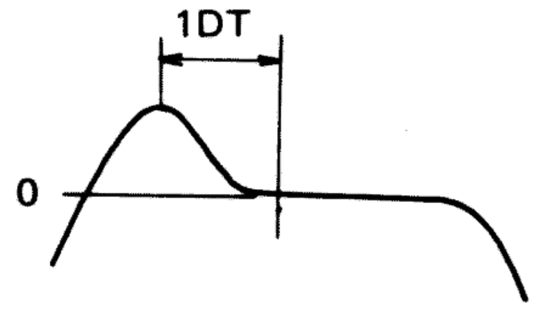
AT starting data

Key ON-OFF data

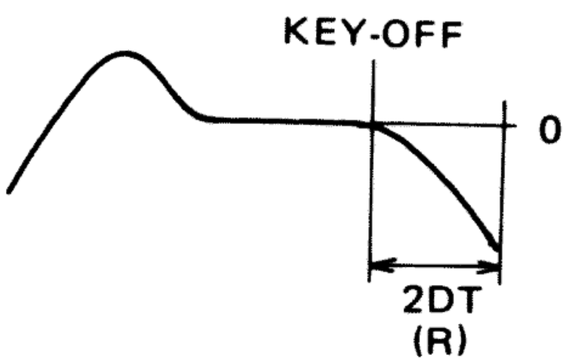
8. Vee ..... −15V input power source.
9. AT ..... Input of buffer voltage for determination of the attack time.
   Input of the voltage between zero V and 10V is provided and the attack time is controlled from 1 mS until 1S.



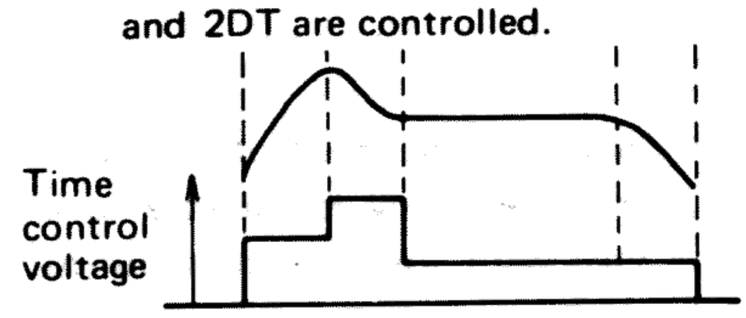
10. 1DT ..... Input of buffer voltage for determination of the decay time.
    Input of the voltage between zero V and 10V is provided and the first decay time is controlled from 10mS until 10 S.



11. 2DT ..... Input of buffer voltage for determination of the release time.
    Input of the voltage between zero V to 10V is provided and the time from KEY-ON until release is controlled from 10m second until 10 second.

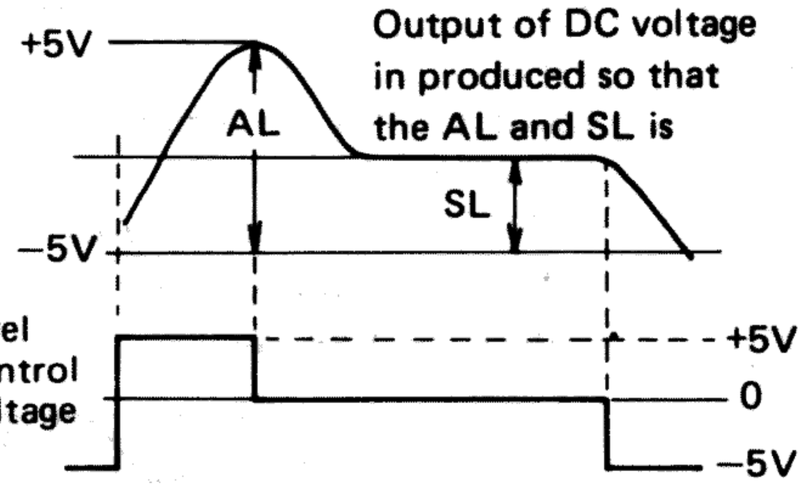


12. TC ..... Output of the time control.
    Output of DC voltage is produced so that the each time of attack, 1DT and 2DT are controlled.



The higher the voltage, the shorter the time and the lower the voltage the longer the time.

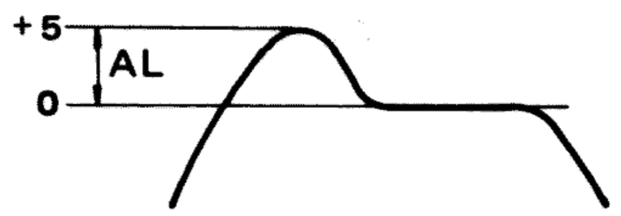
13. LC ..... Output of level control.



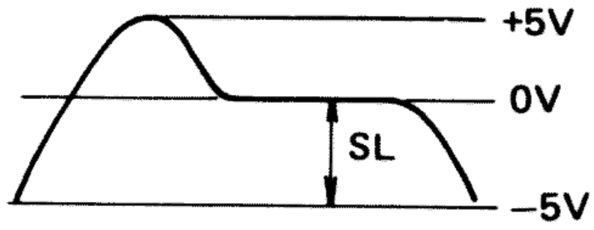
Output of DC voltage in produced so that the AL and SL is

The higher the voltage, the higher the level and the lower the voltage the lower the level.

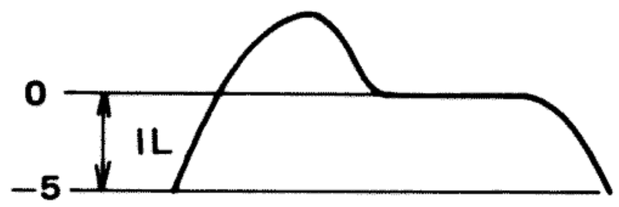
14. AL..... Input of butter voltage for determination of attack level.
    Input of the voltage between (0V~ 10V is provided and the attack level is controlled from 0V until +5V.



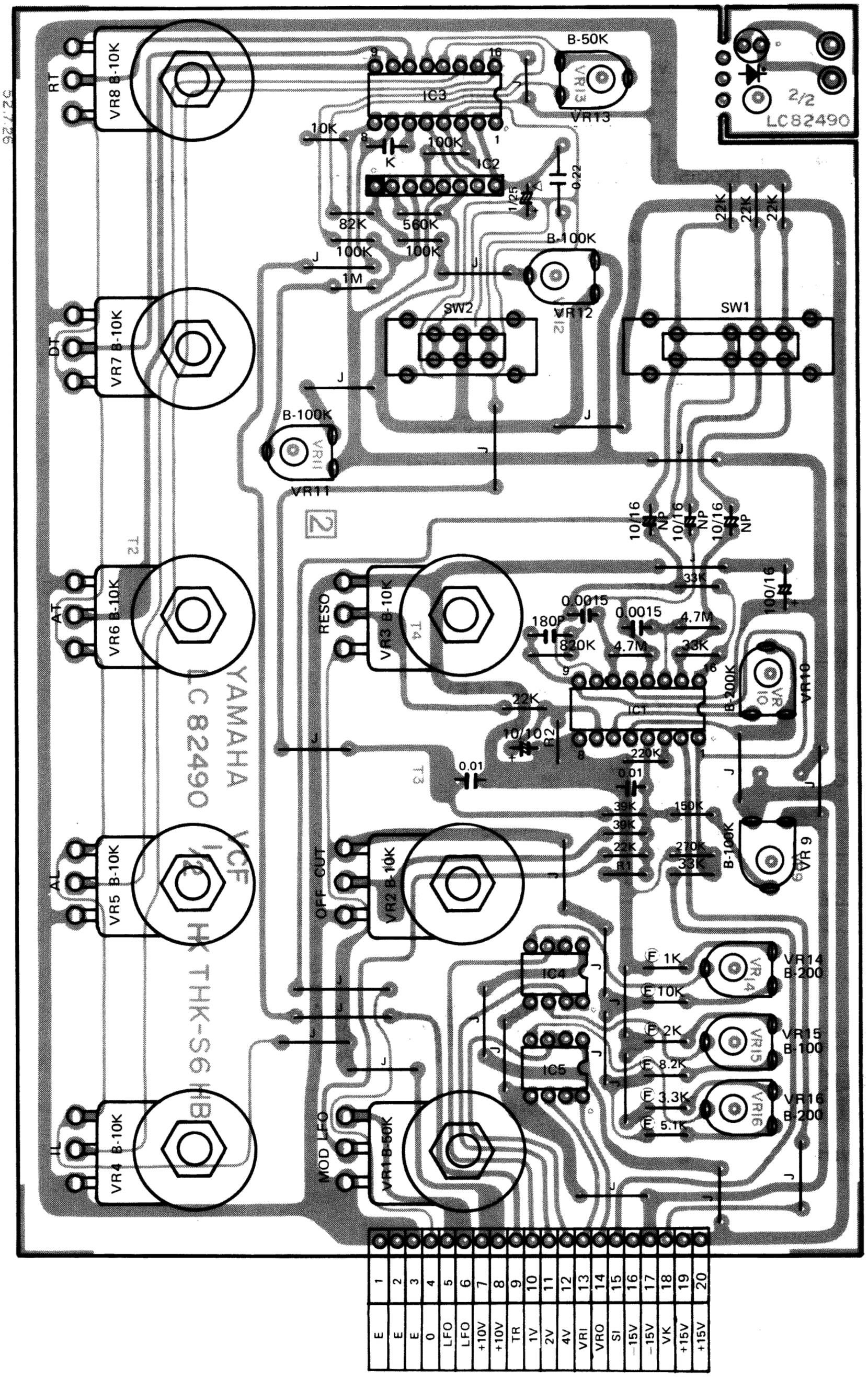
15. SL ..... Input of buffer voltage for determination of the sustain level.
    Normally fixed to zero(0) volt.



16. IL ..... Input of buffer voltage for determination of the initial level.
    Input of the voltage between zero 0V and ten 10V is provided and the initial level is controlled from zero to minus 5 volt.



VCF Circuit Board & Wiring

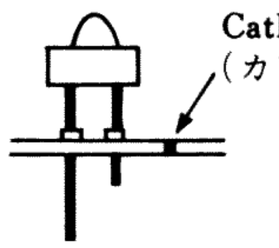


View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)

1. IC
   - IC1 : IG00156
   - IC2 : IG00151
   - IC3 : IG00152
   - IC4,5 : NJM4558
2. K marks : 1000pF ceramic capacitor
3. △ marks : Tantalum capacitor
4. LED : SLP1328

（発光ダイオード）

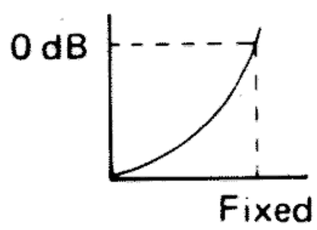


5. Slide SW（スライドSW）
   - SW1 : 3 contact NON-Shorting
   - SW2 : 2 contact Shorting
6. R1, R2

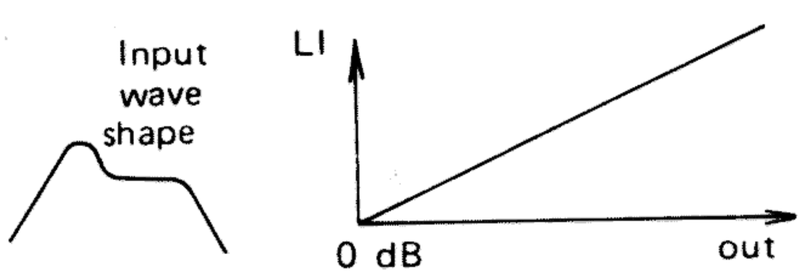
Rank of IC1	R1	R2
A	2.2K	470
B	2.0K	430
C	1.8K	390

VCA IC (IG00151)

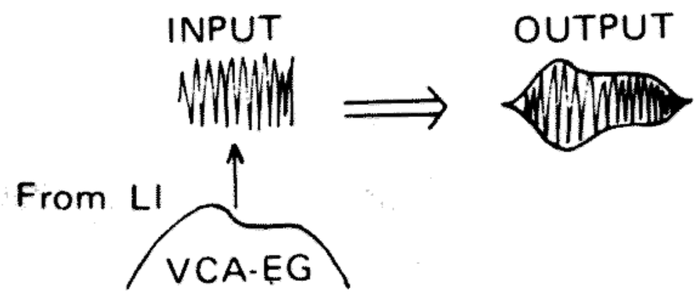
1. EI ..... Input voltage for level control.
   Input of the control voltage is provided for changing the level expotenen tially.



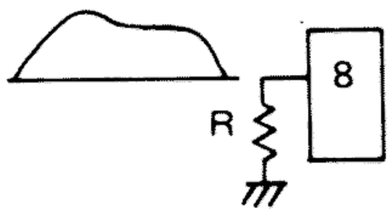
2. LI ..... Input of level control voltage.
   Input of the control voltage is provided for linear change of the level.



3. +IN ..... Input
   Input of the level modulated signal is provided.



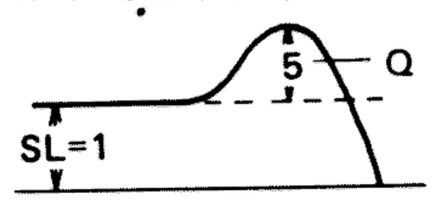
4. −IN ..... Negative feed back.
   Normally unused.
5. Vee ..... −15V input power source.
6. Vcc ..... +15V input power source.
7. GND ..... Earth
8. OUT ..... Output
   Output of the following wave shape is produced.



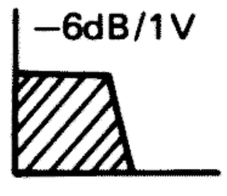
For checking, connect the resistor of 10K～30K ohm as illustrated.

VCF IC (IG00156)

1. AI ..... Signal Input
   Input signals from VCO and WSC are provided to this pin.
2. KV ..... Key voltage input
   In order to change the tone color according to the tone range of key-board, the degignated voltage of the key will supplied to the pin. (0.25-4.0V)
3. fc ..... Adjustment of the cut off frequency.
   Set the control currency of the cut off frequency.
4. Vf ..... Input of the cut off voltage.
   Input voltage of cut off frequency is supplied to this pin so that the tone color can be changed. The center point of the cut off frequency can be also set.
   When the VK is 0.25V and Vf is 5V, the cut off frequency is set to just 1KHz.
5. Vcc ..... +15V input power source
6. Q0 ..... Q adjustment.
   The Q control current sets the Q equal to 5, when VQ is 0 volt.

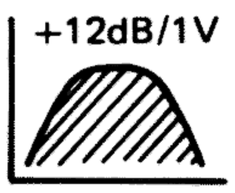


7. VQ ..... Input of the voltage for Q control.
   Q is variable according to the control voltage supplied.
   When the control voltage is 0V (Max.), Q=5
   When the control voltage is 10V (Min.), Q=0.5
8. GND .... Earth
9. FB ..... Q feed back
   This is the feed back output pin for the Q control by which the Q is determined.
10. LP ..... Low-pass output



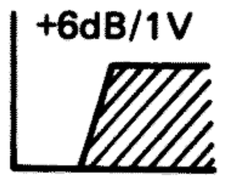
The output of lower frequencies are produced.

11. C2 ..... C pin for determination of the cut off frequency.
12. Vee ..... −15V power source.
13. BP ..... Band-pass output.



The output of intermediate frequences are produced.

14. C1 ..... C pin for determination of the cut off frequency.
15. HP ..... Hi-pass output

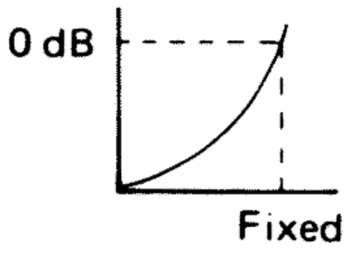


The output of higher frequencies are produced.

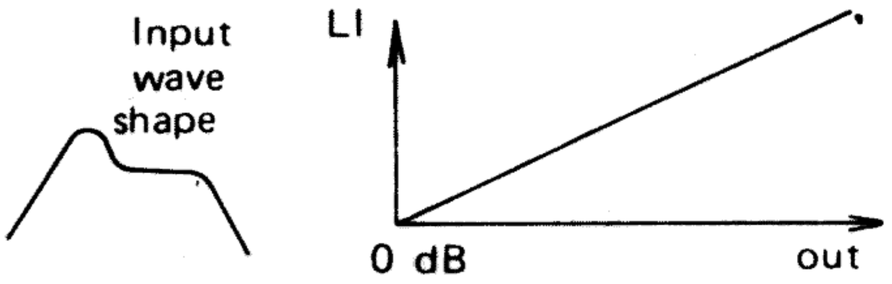
16. IN ..... Input of feed back
    The input signal for determination of cut off frequency.

VCA IC (IG00151)

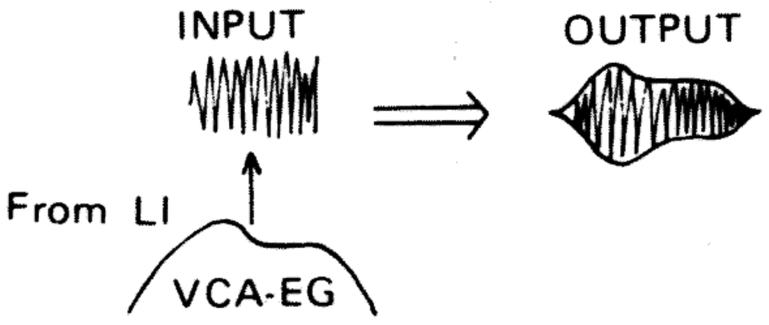
1. EI ..... Input voltage for level control.
   Input of the control voltage is provided for changing the level expotenentially.



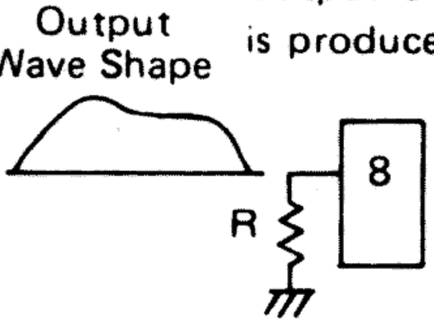
2. LI ..... Input of level control voltage.
   Input of the control voltage is provided for linear change of the level.



3. +IN ..... Input
   Input of the level modulated signal is provided.



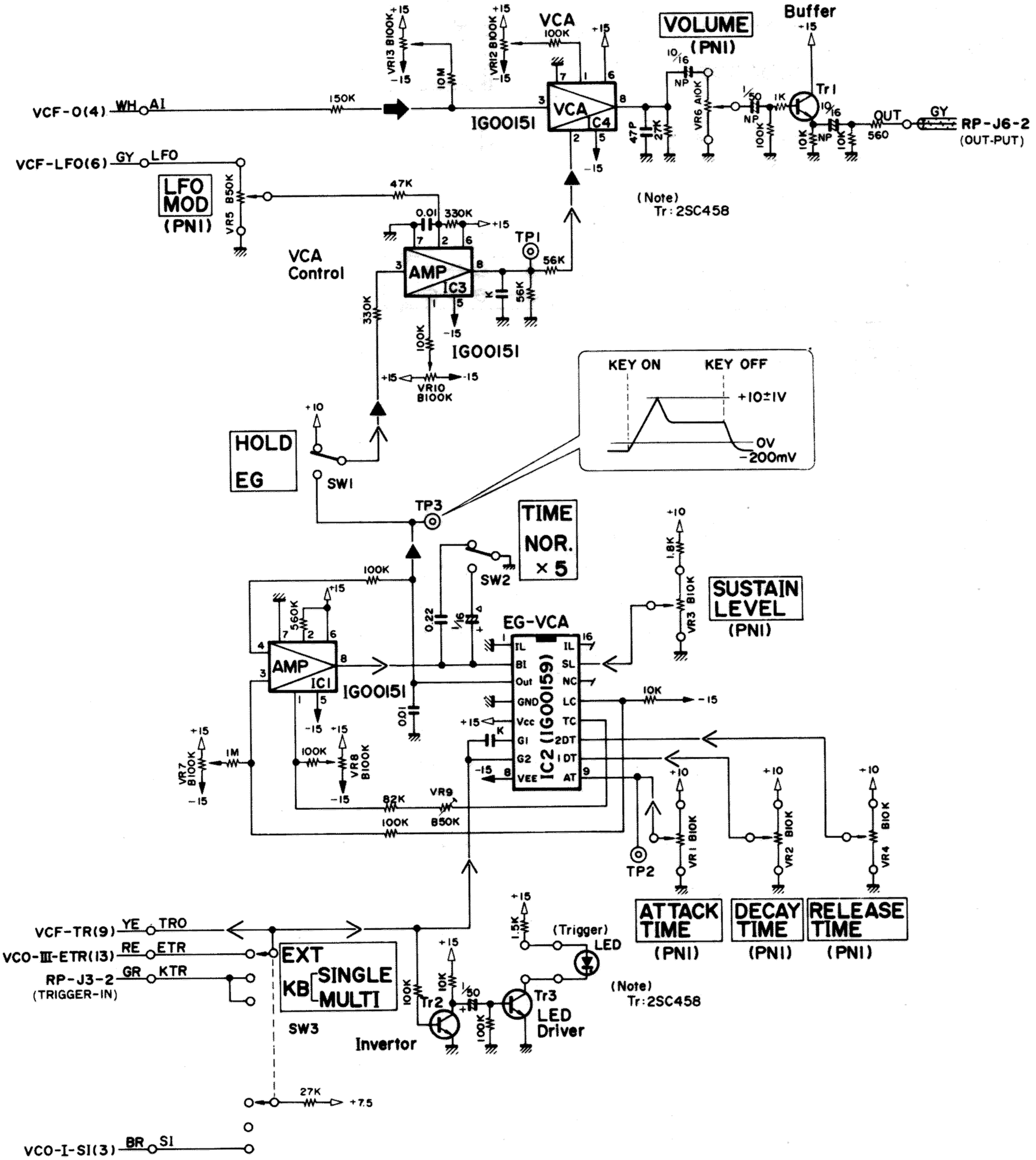
4. −IN ..... Negative feed back.
   Normally unused.
5. Vee ..... −15V input power source.
6. Vcc ..... +15V input power source.
7. GND ..... Earth
8. OUT ..... Output
   Output of the following wave shape is produced.



For checking, connect the resistor of 10K~30K ohm as illustrated.

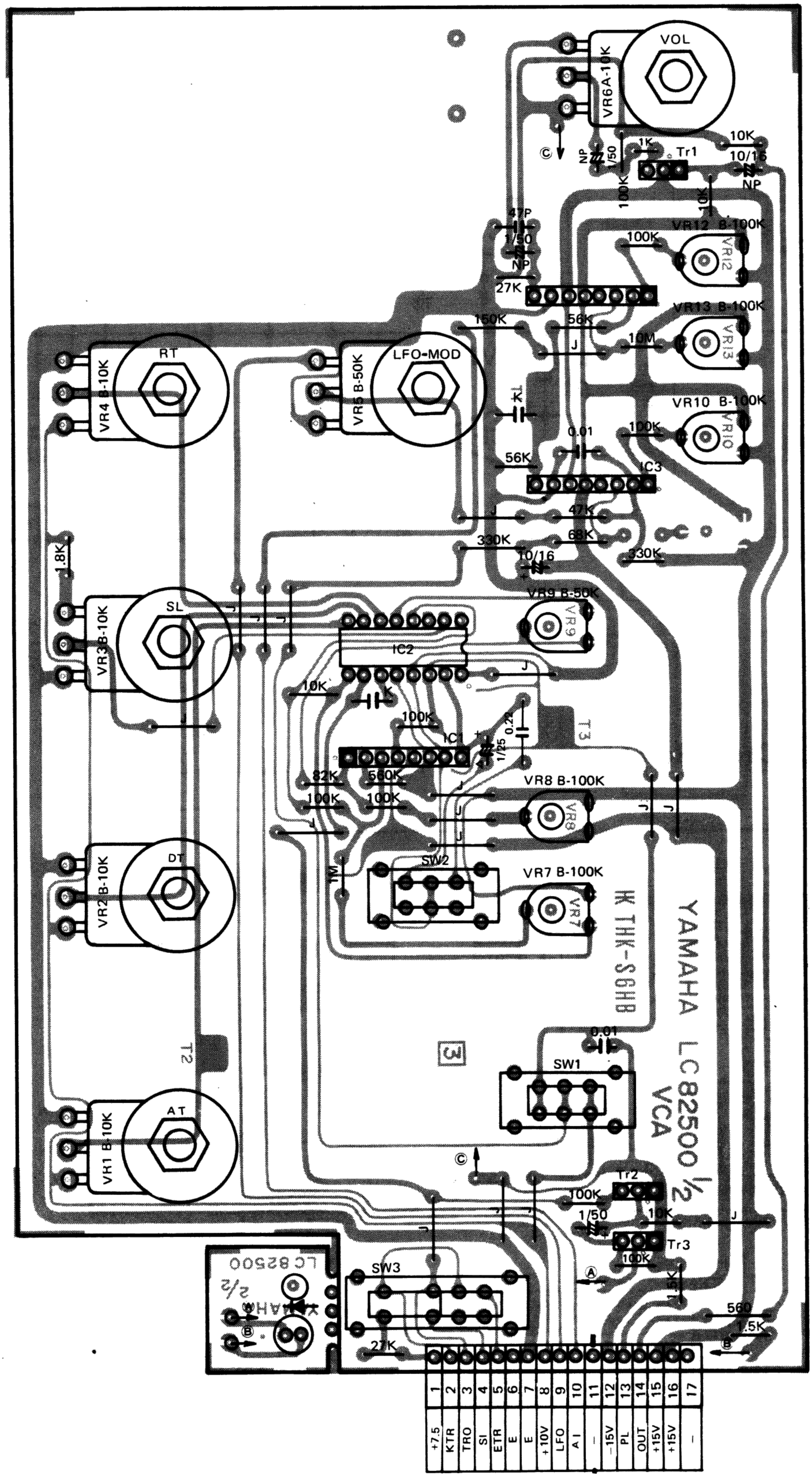
- - - - - Explanation for IC
（ＩＣ説明）

VCA Circuit Diagram



Note:
1. Transistor
   Tr1,2,3 : 2SC458
2. IC
   IC1,3,4 : IG00151
   IC2 : IG00159

VCA Circuit Board & Wiring



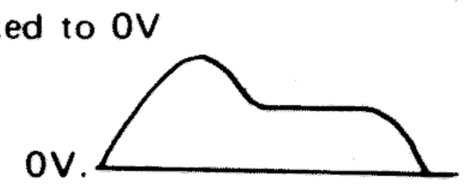
View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)
1. Transistor（トランジスタ）
   Tr1,2,3 : 2SC458
2. IC
   IC1,3,4 : IG00151
   IC2 : IG00159
3. △ marks : Tantalum capacitor
4. Slide SW（スライドSW）
   SW1,2 : 2 contact Non-Shorting
   SW3 : 3 contact Shorting

VCA-EG IC (IG00159)

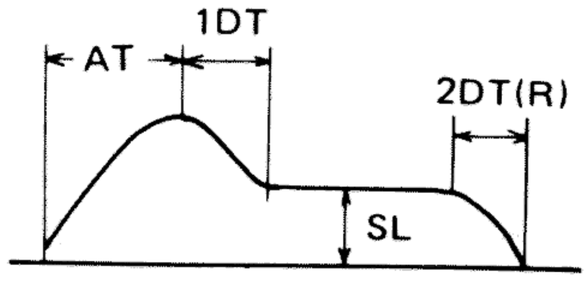
This IC generates envelope wave shape which is supplied to VCA and control the tone volume.

1. IL ..... Input of initial level.

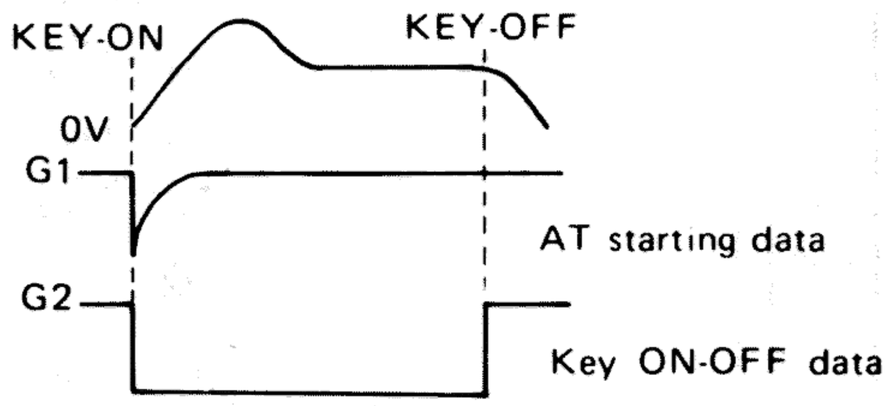


2. BI ..... Input of buffer amplifier.
3. OUT .... The buffer amplifier is built in for the purpose of matching inpedance.

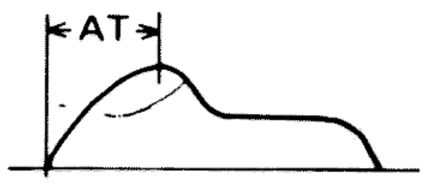
Output wave shape.



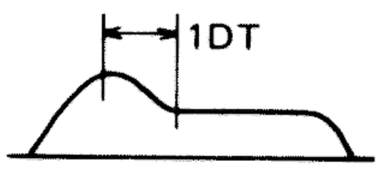
4. GND ..... Earth
5. Vcc ..... +15V input power source.
6. G1 ..... Gate 1
7. G2 ..... Gate 2



8. Vee ..... +15V input power source.
9. AT ..... Input of buffer voltage for determination of attack time.
   Input of the voltage between zero V and 10V is provided and the attack time is controlled from 1 mS until 1S.

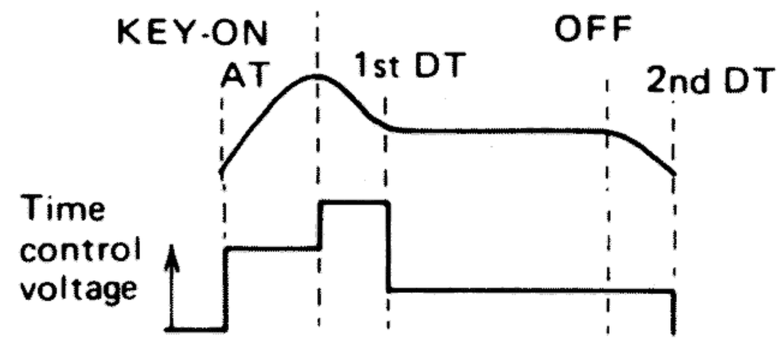


10. 1DT ..... Input of buffer voltage for determination of decay time.
    Input of the voltage between zero V and 10V is provided and the decay time is controlled from 10 m second until 10 second.



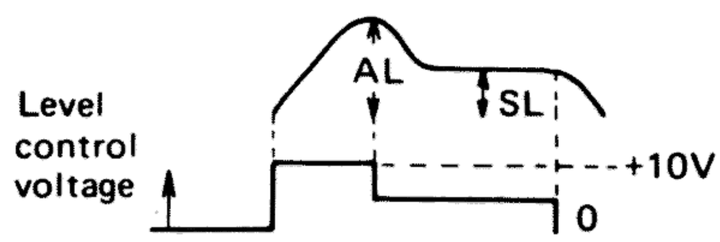
11. 2DT ..... Input of buffer voltage for determination of release time.
    Input of the voltage between zero V and 10V is provided and the time key-off untill release is controlled from 10 mS until 10 S.

12. TC ..... Output of time control.
    Output of the DC voltage is produced so that the each time of Attack, 1st Decay and 2nd Decay are controlled.



The higher the voltage, the shorter the time and the lower the voltage, the longer the time.

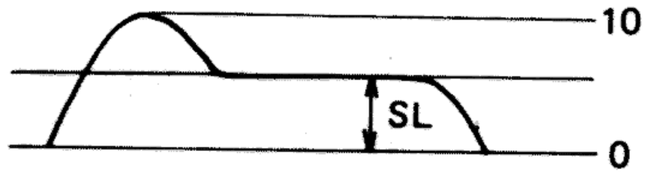
13. LC ..... Output of level control



Output of the DC voltage for AL and SL control is provided.

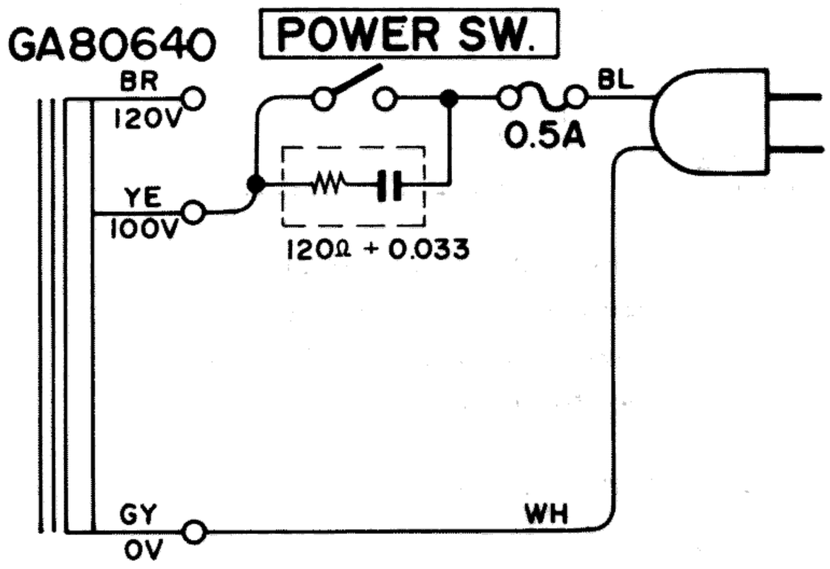
The higher the voltage , the higher the level and the lower the voltage, the lower the level.

14. NC..... Not connected.
15. SL ..... Input of buffer voltage for determination of the sustain level.
    Input of the voltage between zero V and 10V is provided so that the sustain level can be controlled.

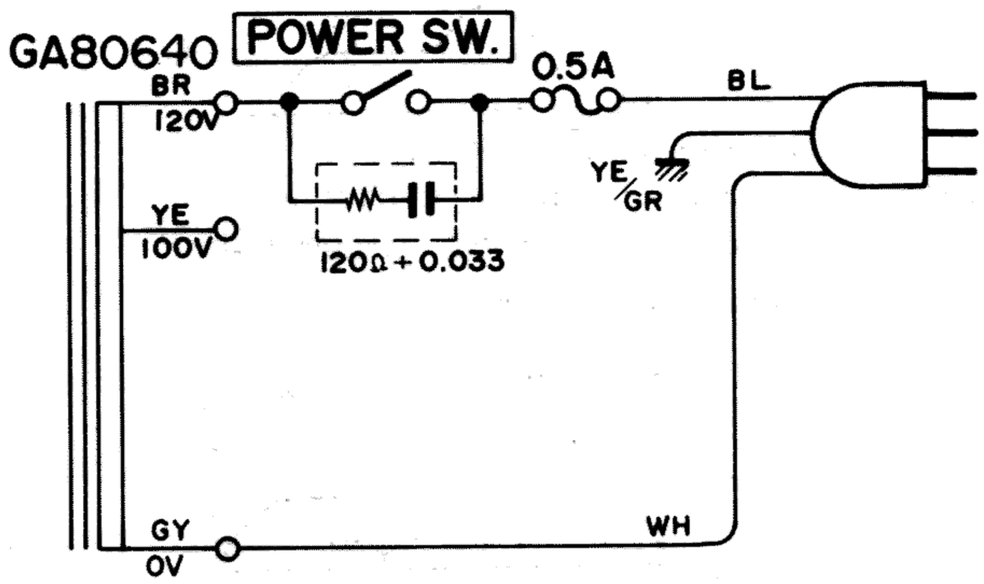


16. NC ..... Not connected.

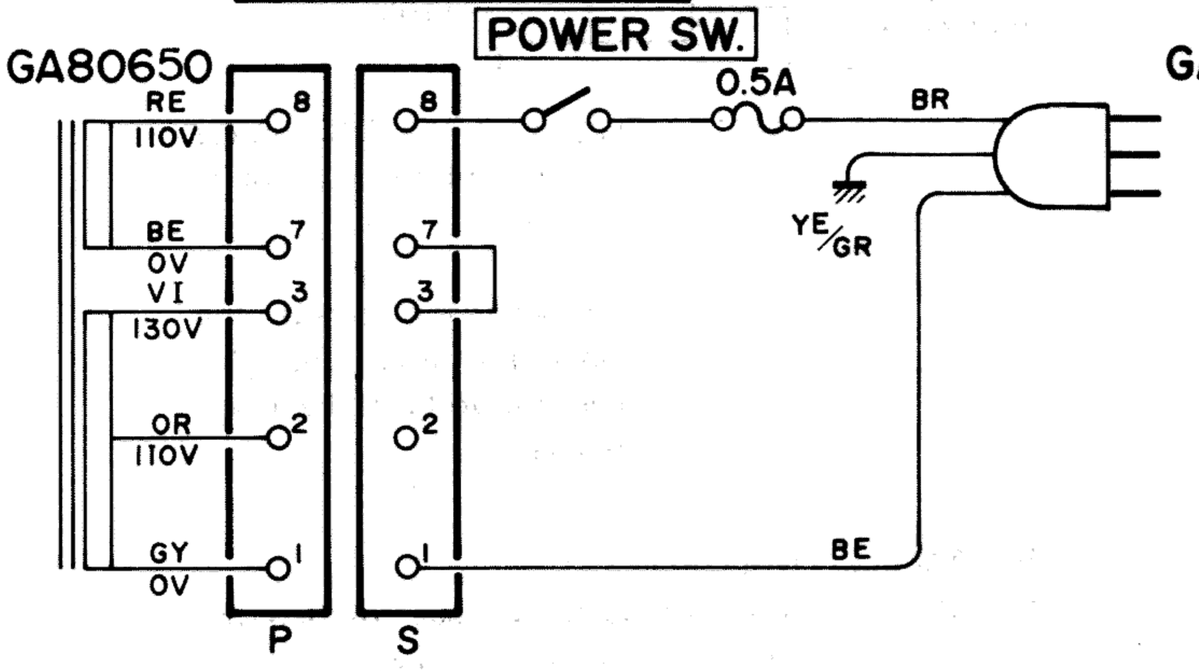
Japan Spec.



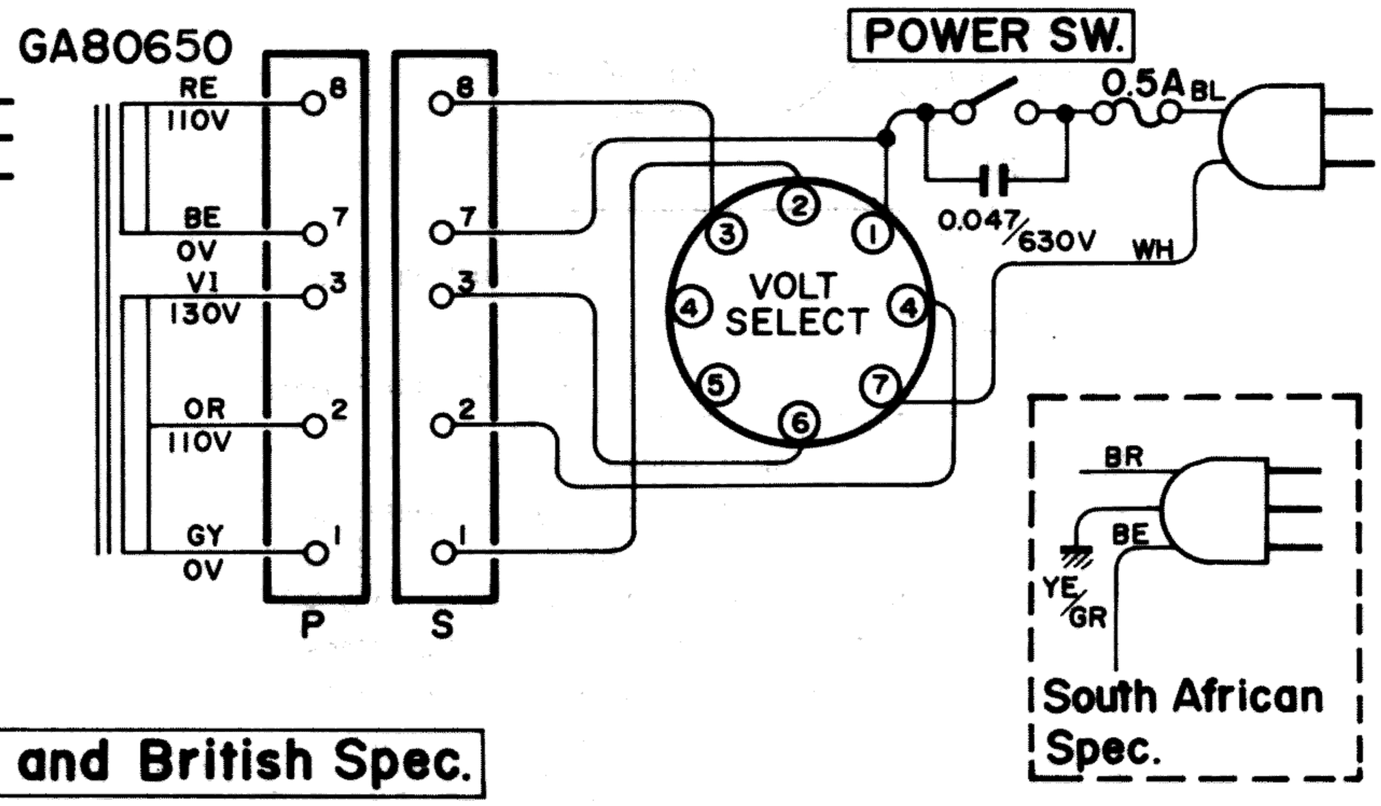
US American and Canadian Spec.



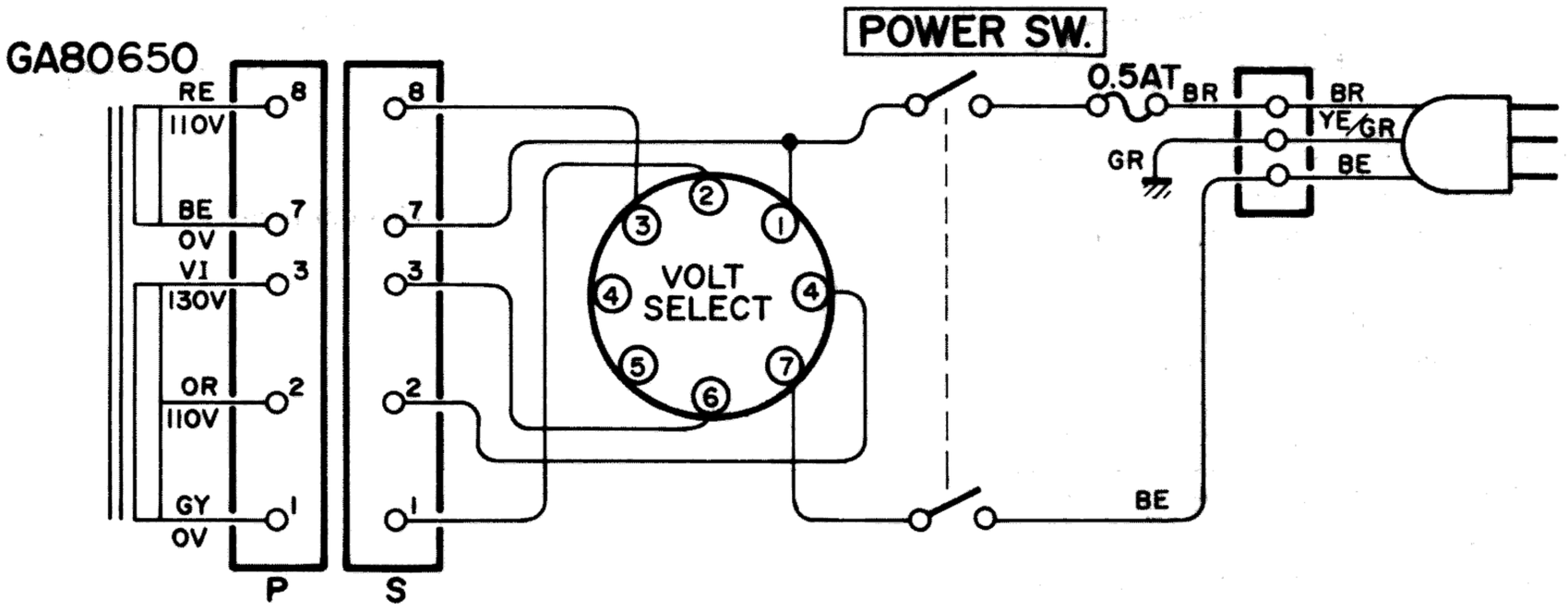
Australian Spec.



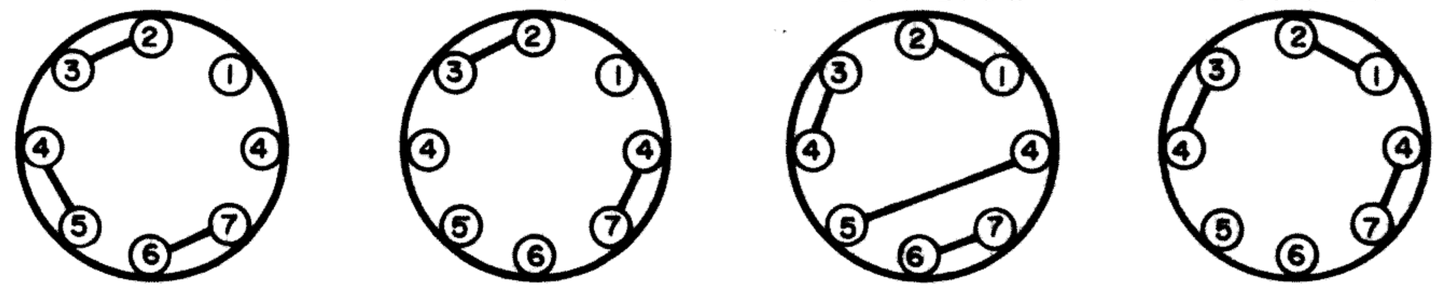
GENERAL and South African Spec.



North European and British Spec.



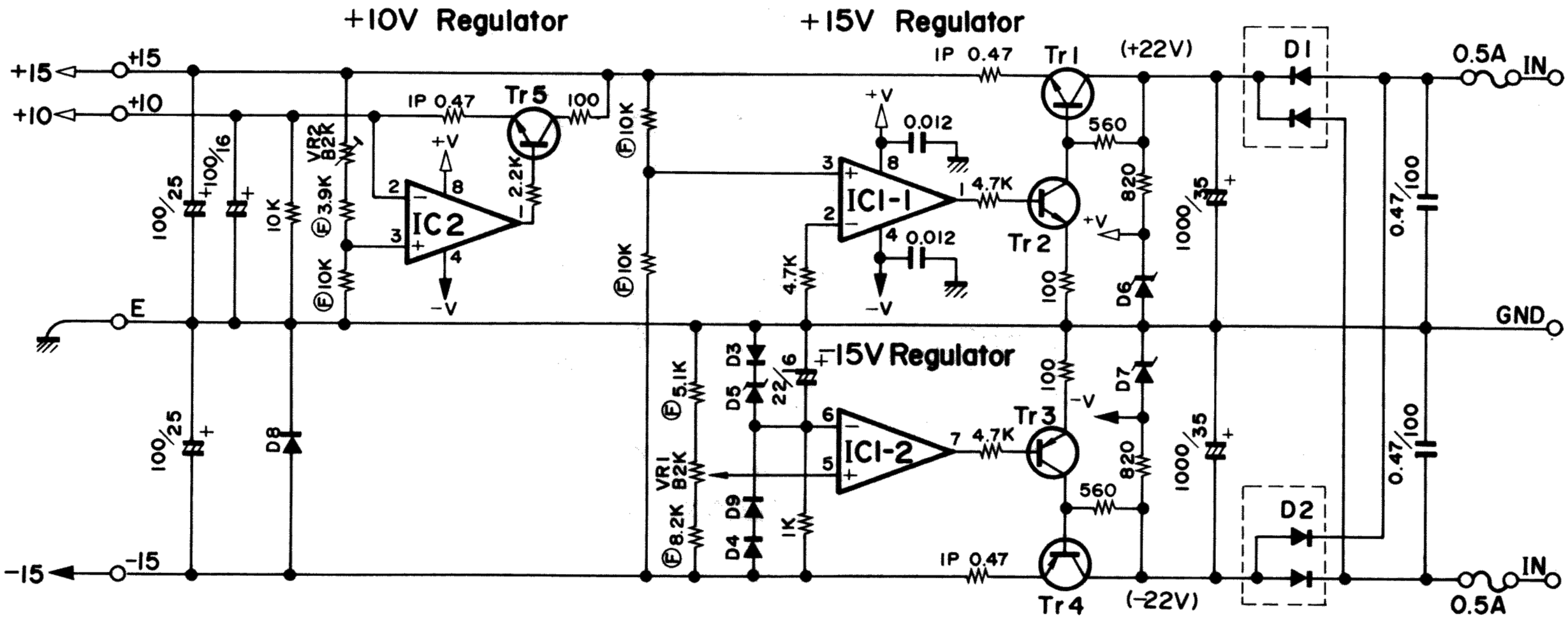
ACTUAL CONNECTIONS ON VOLTAGE SELECTOR



CS-10 (S/# 1001～)

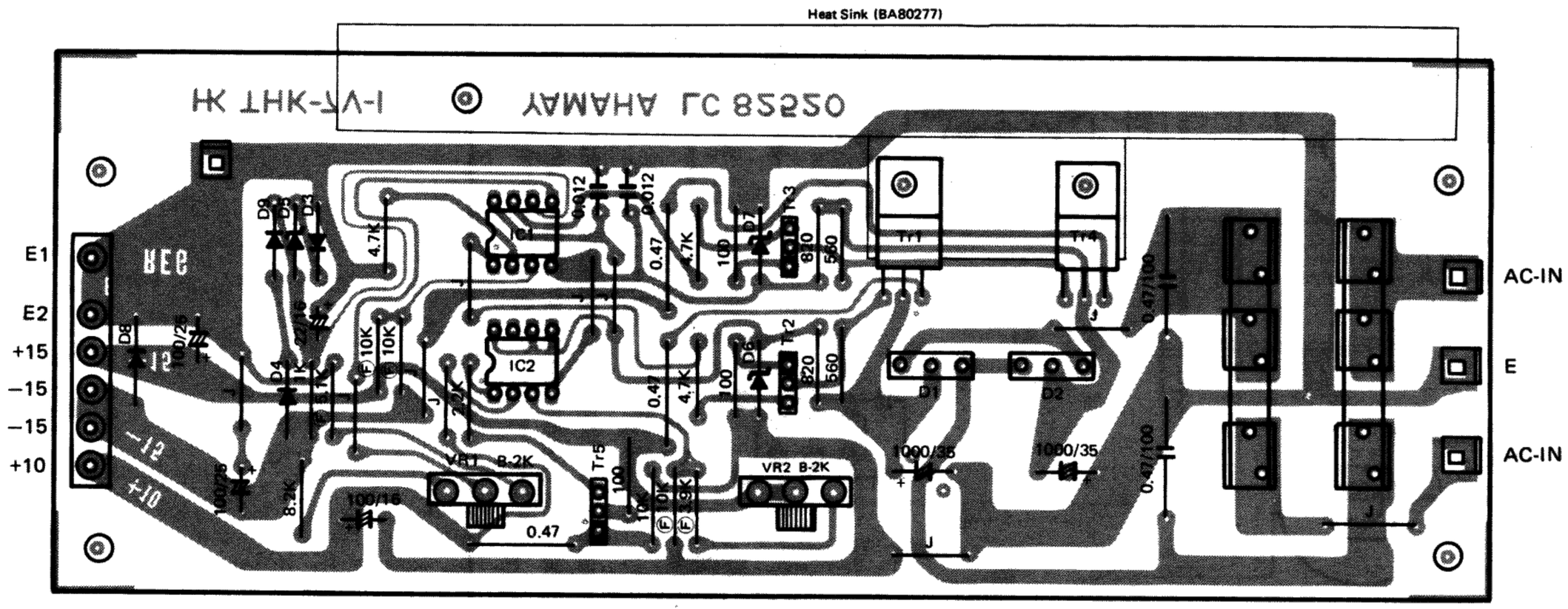
←- - - - Primary
(一次側)

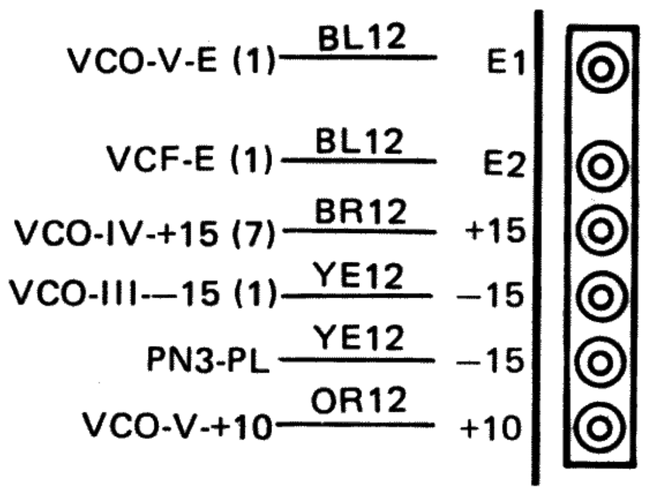
REG Circuit Diagram



KEC-90098-75 ⚠2

REG Circuit Board & Wiring



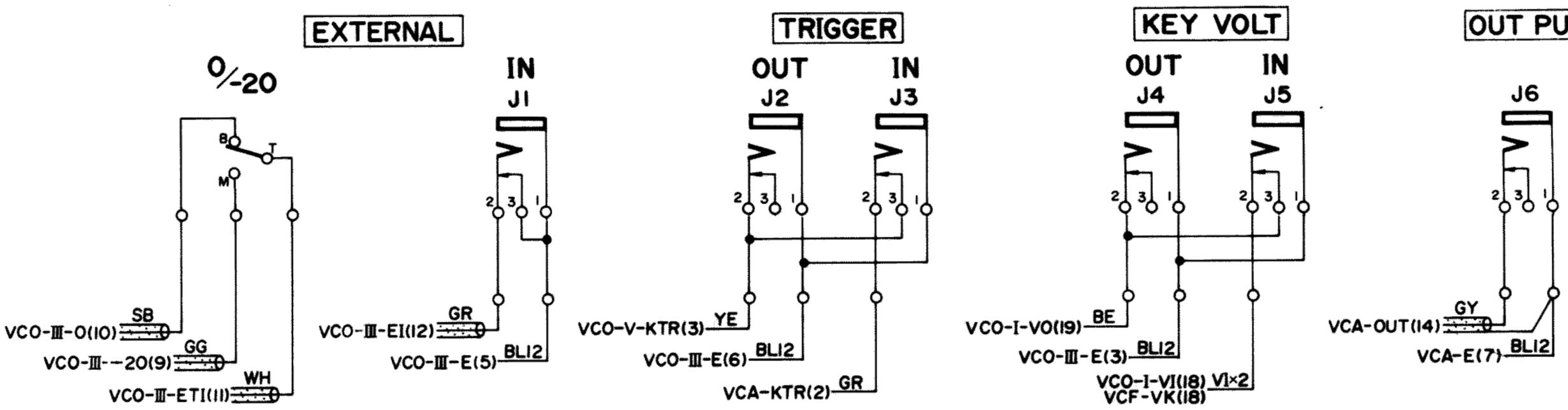


(Note)

1. IC 1,2 : NJM4558
2. Transistor (トランジスタ)
   Tr1 : 2SD235
   Tr2 : 2SC458
   Tr3 : 2SA561
   Tr4 : 2SA490
   Tr5 : 2SC509
3. Diode (ダイオード)
   D1 : 10DC-1
   D2 : 10DC-1R
   D3,4.9 : 1S1555
   D5 : 02Z5.6A
   D6,7 : WZ150
   D8 : 10E-1
4. Fuse (ヒューズ)
   North European, British : 0.5AT (MINI)
   Other : 0.5A (UL)

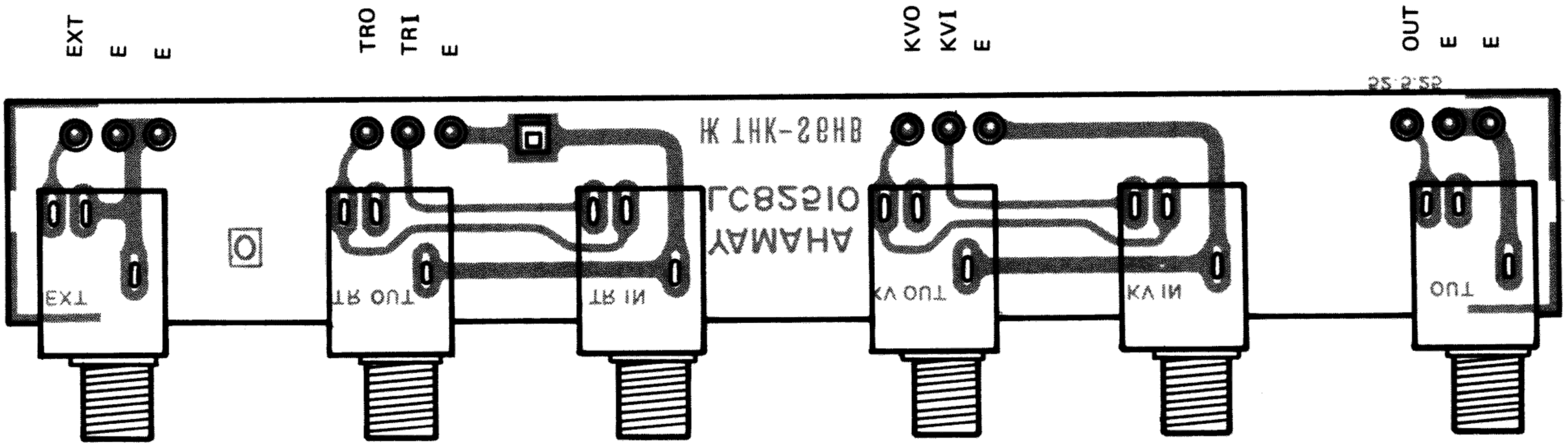
KEP-NA80280-77⚠

REAR PANEL Circuit Diagram

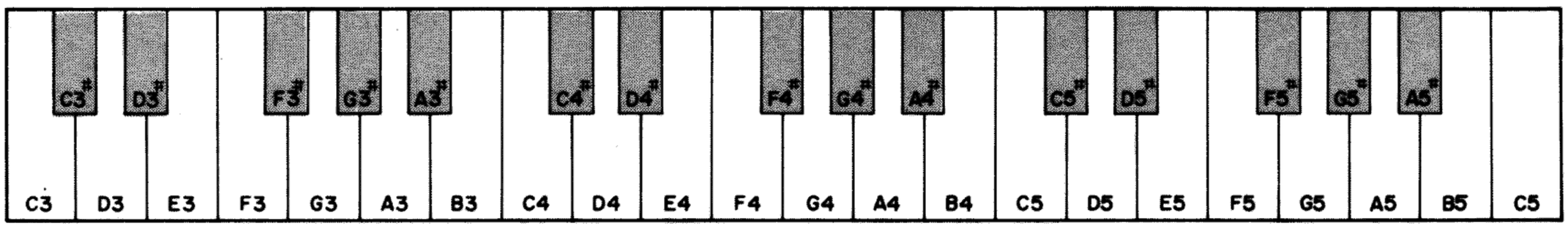


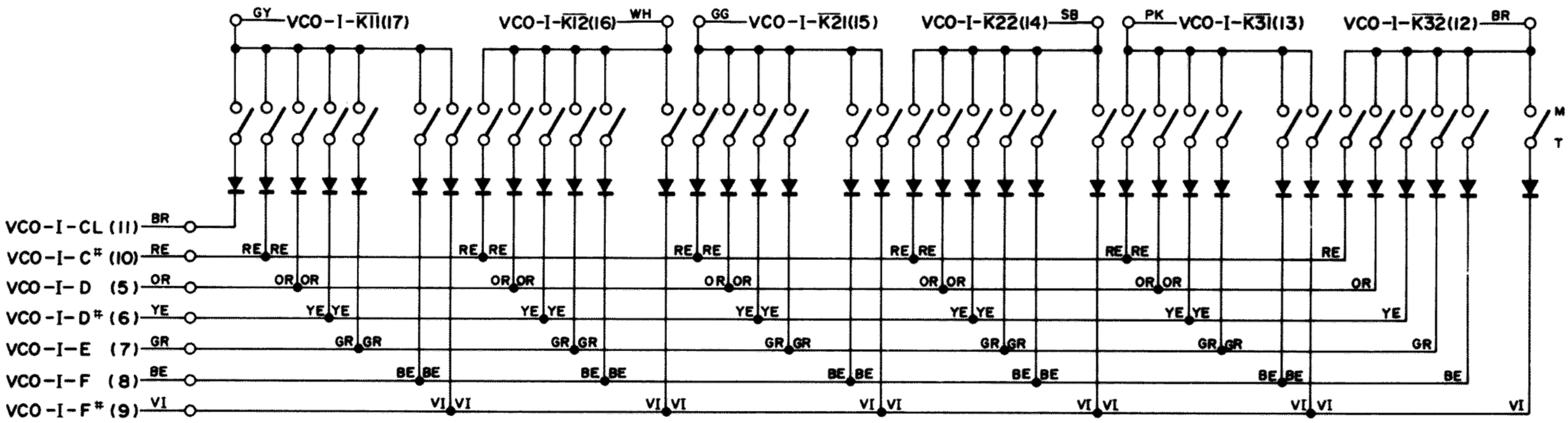
KEC-90100-75 ⚠ ½

REAR PANEL Circuit Board & Wiring



Key Switch Circuit Diagram

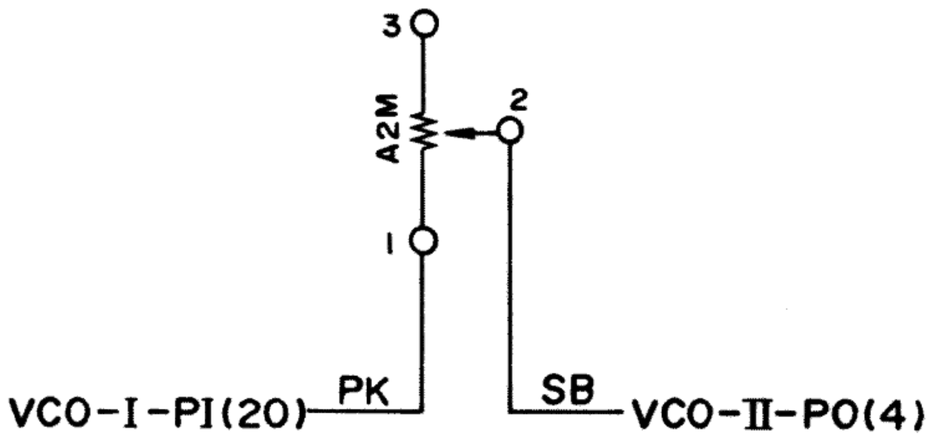




PN2 Circuit Diagram

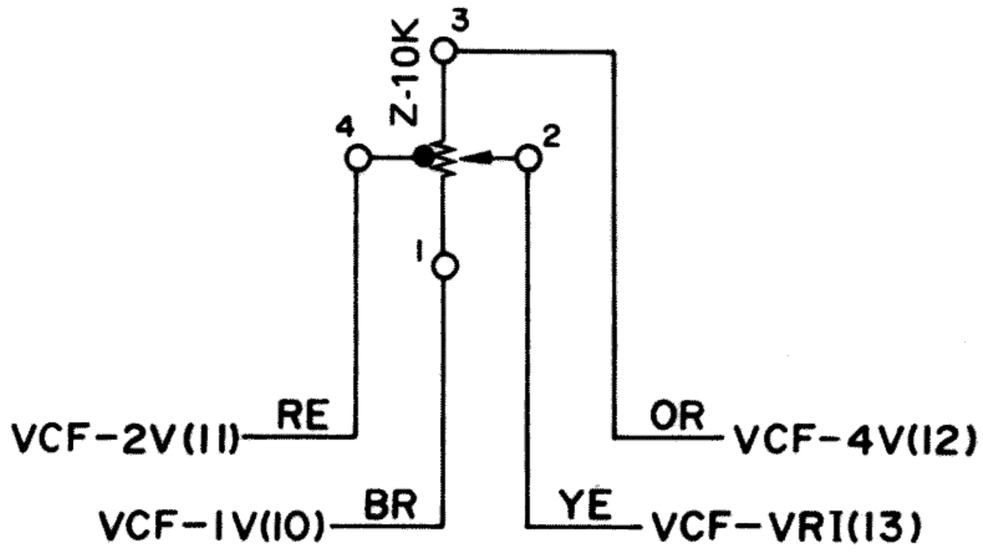
PORTAMENTO

VR1



PITCH BEND

VR2



Standerd for circuit inspecpion and adjustment

ADJUSTMENT OF VCO SECTION

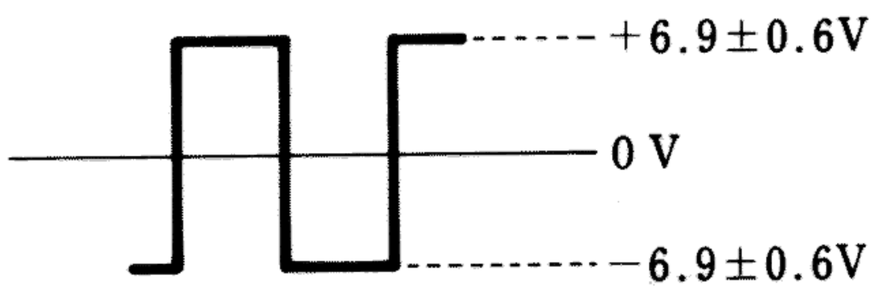
1. Power Supply for Key Assignor

   +7V Adjustment : Make sure that voltage of +6.9 ± 0.6V is present at TP7.

   −7V Adjustment : Make sure that voltage of −6.9 ± 0.6V is present at TP8.

2. Key Assignor Clock

   Make sure that a waveform as in the figure below is obtainable at TP9.



f= 9 ± 1 KHz

3. Key Assignor

   Set the Pitch Bend Lever to "0" position (VR terminal → 2,000V), turn on the C_3 key, then make sure that voltage of 500 ± 0.5mV is present at TP1.

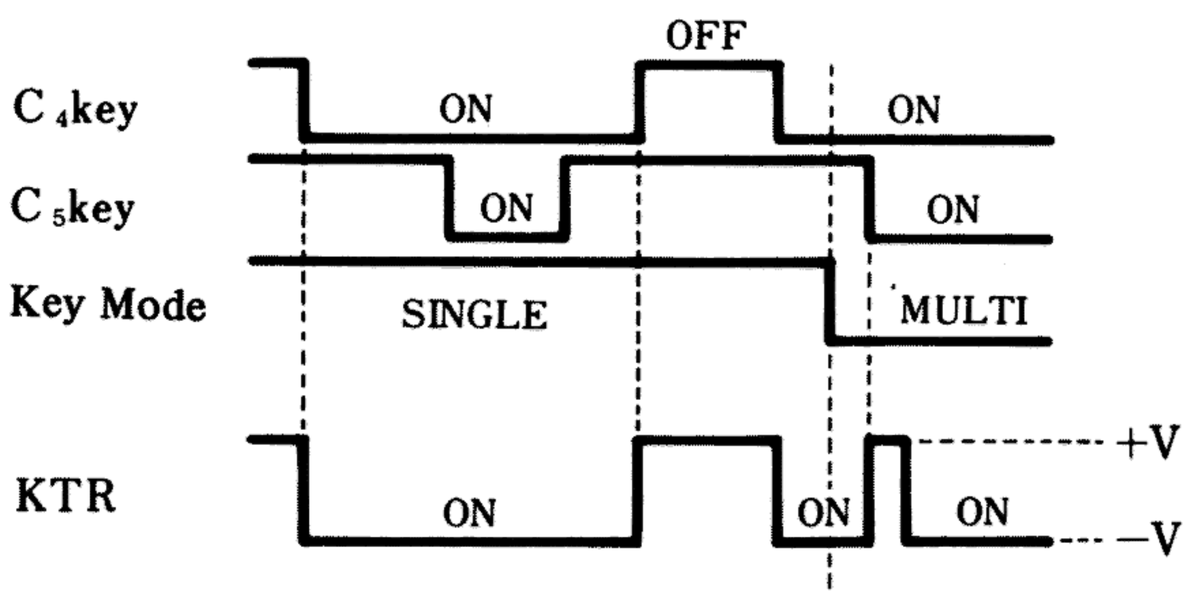
   Adjust VR1 until TP2 has the same potential as that at TP1. Then make certain that 250 ± 0.25mV is present at TP3, and adjust VR2 so that the PO terminal has the same potential as that at TP3.

   Adjust VR3 until the potential at the VO terminal becomes identical to that at the PO terminal.

   When the Pitch Bend Lever is set to "+" position, the potential at each point mentioned above should be doubled; with the lever set to "−", the potential should be reduced by half. Then, turn off the C_3 key, turn on the C_6 key, and confirm that 2.00 ± 0.002V is present at the VO terminal.

4. Key Mode Change Circuit

   Turn on and off the C_4 and C_5 keys as in the figure below, change the key mode from SINGLE to MULTI, and make sure that the KTR terminal output is as shown in the figure.

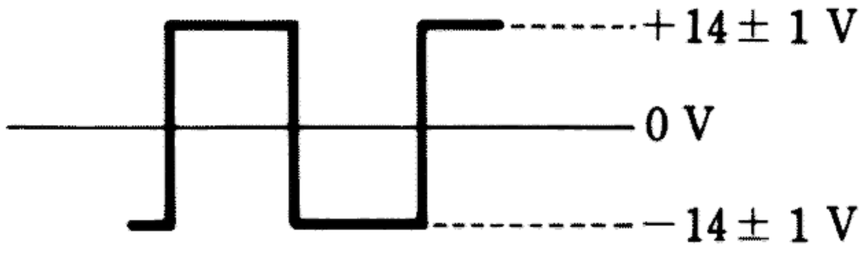


During SINGLE Mode, as long as a key remains depressed, operating other keys has no effect on the KTR, which is kept ON.

During MULTI Mode, depressing keys successively permits KTR to turn ON one after another with priority given to higher tones.

5. VCO III

a) Adjust the TUNE Vol. until a voltage smaller than ±0.5V is present at TP10, set FEET SW, LFO MOD and PW/PWM Vol. to "8' ", "0" and "0" respectively, turn on the C_6 key, and apply a voltage of 2.00 + 0.002V to the VI terminal. Now, adjust VR5 so that a waveform of 2107.28Hz ± 0.1% as shown in the figure below is obtainable at TP4.
Turn on the C_3 key, apply 250 ± 0.25mV to VI terminal, then adjust VR4 so that a waveform of 263.41Hz ± 0.1% is obtainable. Repeat these adjustments until the frequency error becomes 0.1%.



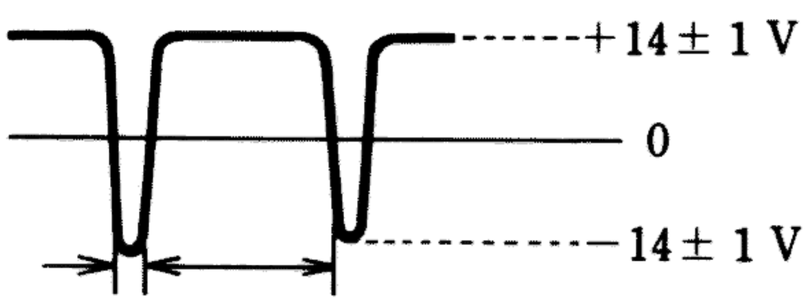
b) Turn on the C_6 key, then make sure that the frequency ranges from 2169 to 2194Hz or from 2024 to 2047 when the TUNE Vol. is set to the "+" or "−" position.

c) Set the TUNE Vol. to the center position, and confirm that the frequency varies as shown in the table below.

FEET	Frequency [Hz]
64′	260.38～266.47
32′	523.79～529.87
16′	1047.57～1059.74
8′	2107.28 ±0.1%
4′	4190.28～4238.96
2′	8380.55～8477.93

6. Waveform Converter Circuit

a) Set the FEET, PWM/PW and PW/PWM Vol. to "8' ", "PW" and "10" positions respectively, then adjust VR9 until a waveform as shown in the figure below is obtainable at TP4.



Adjust the ratio 1.5 : 8.5

b) Set the FEET and PW/PWM Vol. to "8' " and "0". Then, make sure that a waveform as in Fig. 1 or 2 is obtainable at the OUT terminal when the ◺ or ⊓ Vol. is set to "10".

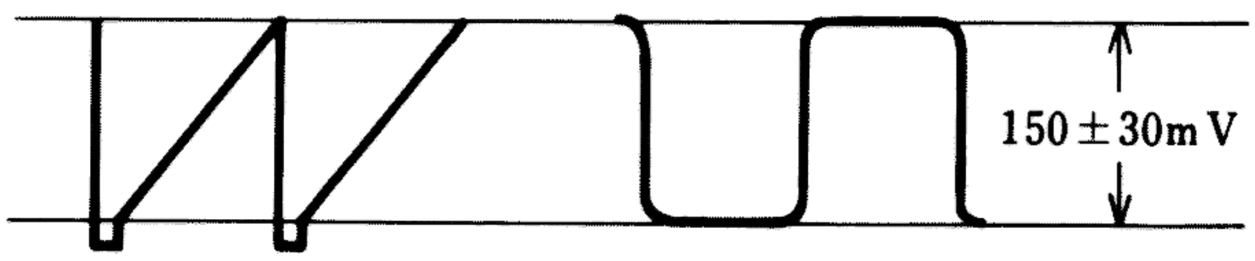


Fig. 1 Fig. 2

7. Noise Generator Circuit

Set the EXT/NOISE Switch to "Noise" position and EXT/NOISE Vol. to "10" position, then adjust VR10 so that a waveform of +2 ± 1dBm as shown in the figure below is obtained at TP5.

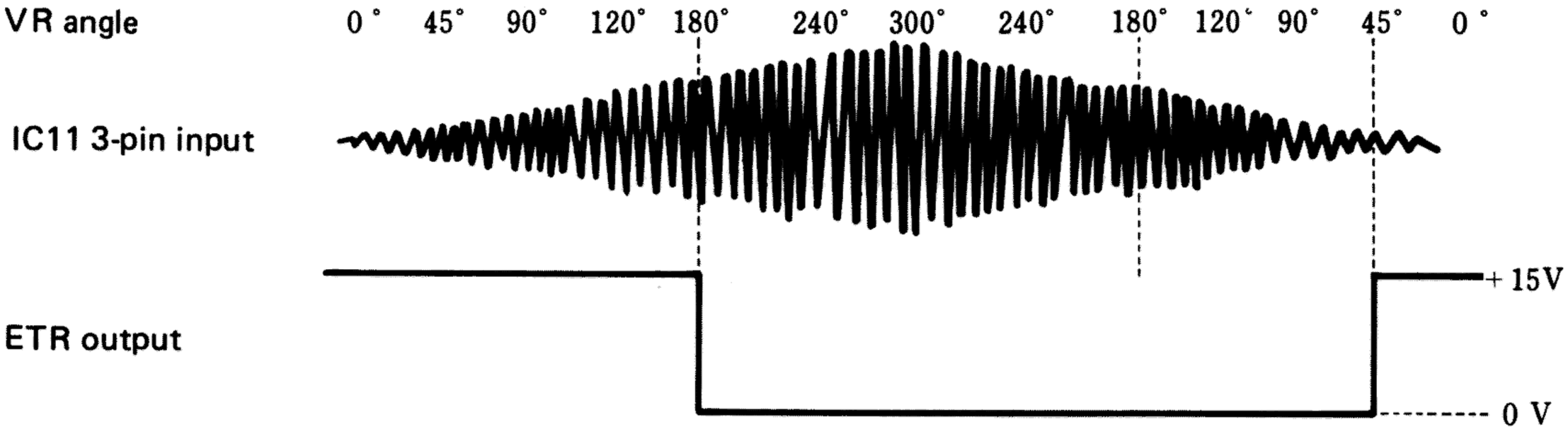
+ 2 ± 1 dB

8. EXT Amplifier Circuit

a) Apply a sine wave of 1kHz, −30dBm to the EI terminal, and make sure that the same waveform having −10 ± 2dBm is obtained at the O terminal.
Ascertain that output of +10 ± 2dBm is obtained at −20 terminal.

9. EXT Trigger Circuit

Apply a sine wave of 1kHz, −14dBm to the ETI terminal, set the Trigger Level Vol. to "0" position, then make certain that the potential at the ETR terminal varies as shown in the figure as the Trigger Level Vol. is turned clockwise.



10. LFO Oscillation Circuit

Set the LFO Speed Vol. and ∩/⊼ Switches to "S" and "⊼" positions, and make sure that a waveform as in Fig. 1 is obtained at the LFO terminal. Adjust VR12 until the frequency becomes 0.1Hz. Then, set the LFO Speed Vol. to "F", and adjust VR13 until the frequency becomes 100Hz. In this case, light-emitting diodes should light according to the frequency. Confirm that a waveform as in Fig. 2 is obtained when ∩/⊼ Switch is set to " " position.

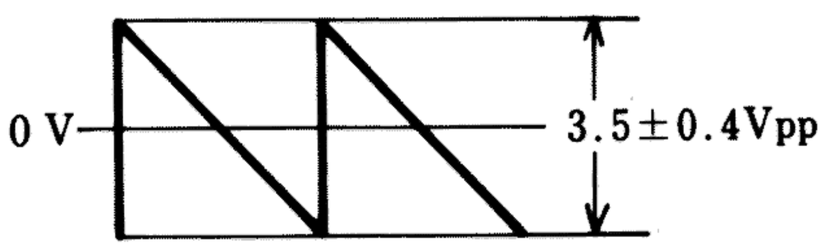


Fig. 1

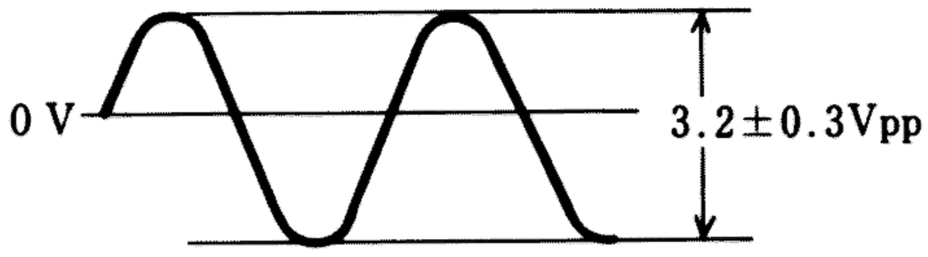


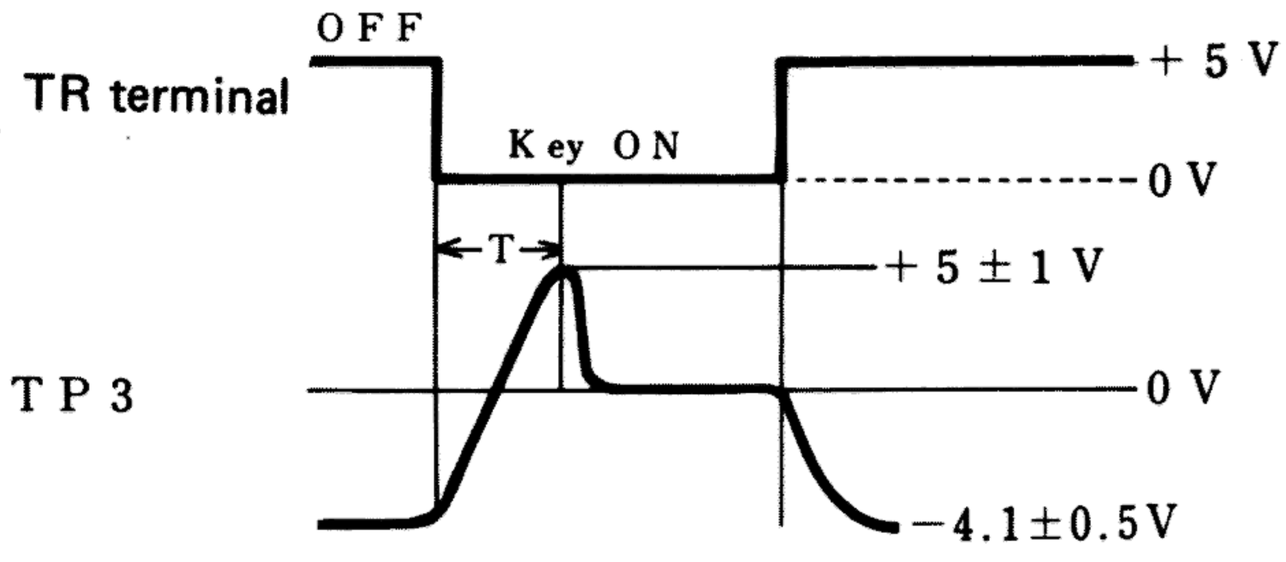
Fig. 2

ADJUSTMENT OF VCF SECTION

1. Envelope Generator Circuit

a) Adjust the Attack Time Vol. until a voltage of 8.0 ± 0.1V is present at TP2. Set the Decay Time and Release Time Vol. to "S", Attack Level and Initial Level Vol. to "5" and NORMAL/X5 Switch to "NORMAL", turn on a key (with 0V being present at the TR terminal), then adjust VR11 until a voltage smaller than 0 ± 50mV is present at TP3.

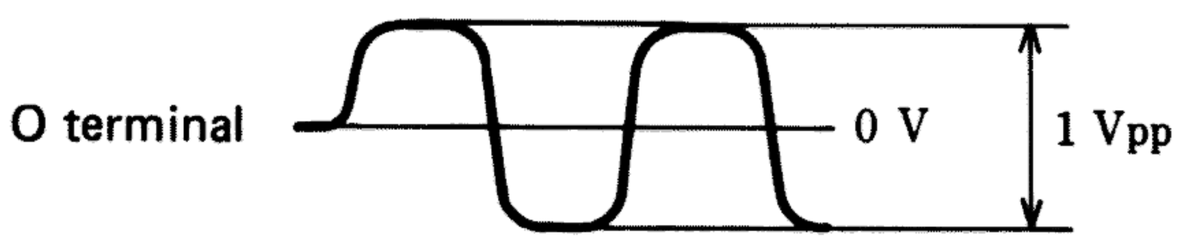
b) Turn the key on and off (with 0V and +5V present at the TR terminal), and make sure that a waveform as in Fig. 2 is obtained at TP3. In this case, adjust VR12 until T equals 4m sec.
Adjust the Attack Time Vol. until a voltage of 3.0 ± 0.1V is present at TP2, and depress a key. If T is longer or shorter than 125m sec, adjust VR13 so that T becomes even longer or shorter, then, supply 8V at TP2, and adjust for 4m sec. Repeat the adjustment until both T's are within ±5%.



c) Make sure that T becomes 3.3 – 6.1 times as large when the NORMAL/X5 Switch is set to "X5" position.

2. VCF Circuit

Set switches as in 1-a) with the LFO MOD Vol. set to "0" position. Adjust the Cut Off Frequency Vol. until 5.0 ± 0.1V is present at TP1, and adjust the Resonance Vol. until 5.0 ± 0.1V is present at TP4. Set the HPF/BPF/LPF, VCO FEET, and Switches to "LPF", "2' ", "0" and "10" respectively, turn on the C_3 key, then adjust VR9 for the maximum value and VR10 for 1 Vp-p until a waveform as in the figure below is obtained at the O terminal.



Set the Cut Off Frequency Vol. to "H" position, turn on a key, then make certain that a waveform as in Fig. 1 is obtained. Set the Resonance Vol. to "L" position, and ascertain that a waveform as shown in Fig. 2 is obtainable.

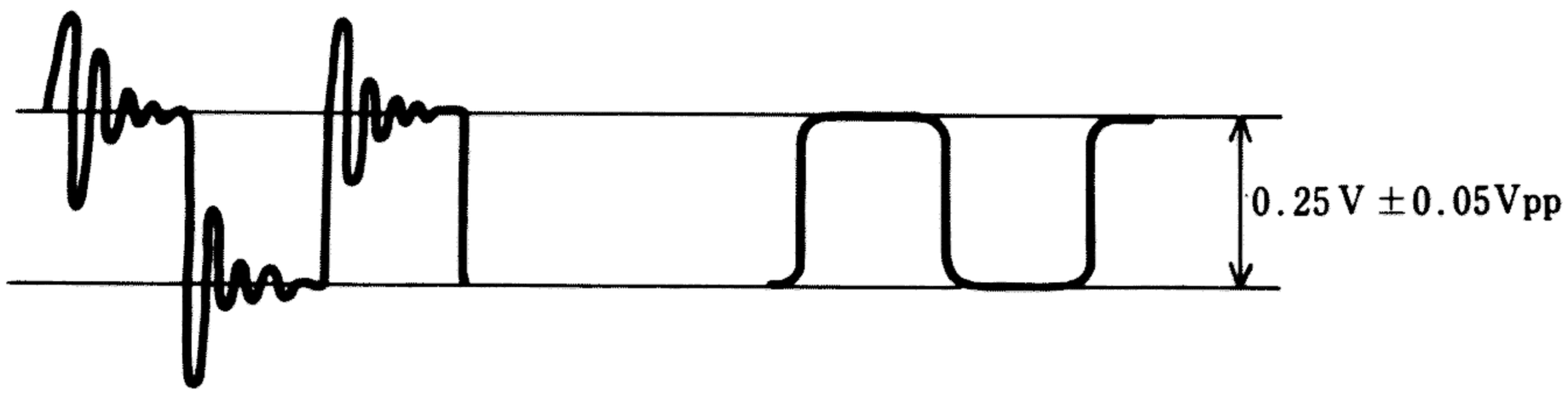


Fig. 1

Fig. 2

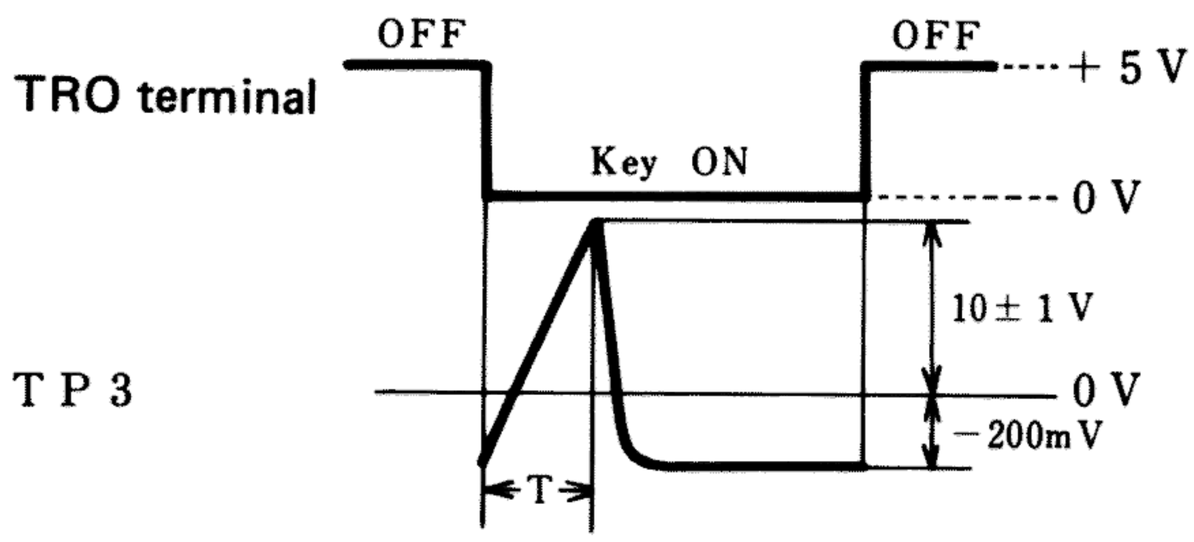
3. Standard Voltage Generator Circuit

Set the Pitch Bend Lever to "–", "0" and "+", then adjust VR14, VR15 and VR16 until 1.00 ± 0.001V, 2.00 ± 0.002V and 4 ± 0.004V are obtained respectively at VRO terminal.

PITCH BEND	VRO Terminal Voltage	Adjustment VR
+	4.00±0.004V	VR16
0	2.00±0.002V	VR15
–	1.00±0.001V	VR14

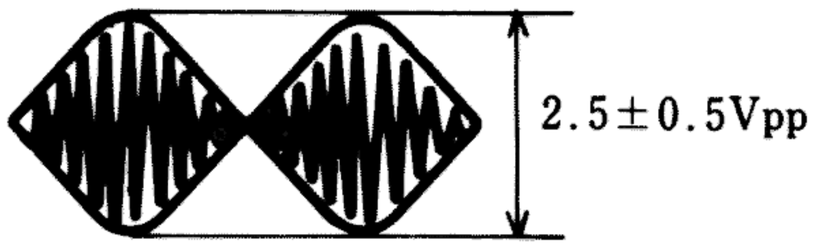
ADJUSTMENT OF VCA SECTION

1. Envelope Generator Circuit
   a) Adjust the Attack Time Vol. until 8.0 ± 0.1V is present at TP2. Set the Decay Time and Release Time Vol. to "S", Sustain Level Vol. to "0" and NORMAL/X5 Switch to "NORMAL", turn on a key (with 0V present at TRO terminal), then adjust VR7 until −200 ± 20mV is present at TP3.
   b) After the adjustment in item 1-a) is completed, turn on a key and make sure that a waveform as in Fig. 2 is obtained at TP3. In this case, adjust VR8 until T equals 4m sec. Adjust the Attack Time Vol. until a voltage of 3.0 ± 0.1V is present at TP2. If T is longer or shorter than 125m sec, adjust VR9 so that T becomes even longer or shorter. Then, supply 8V to TP2, and adjust for 4m sec. Repeat the adjustment until both T's are within ±5%.



   c) Make sure that T becomes 3.3 – 6.1 times as large when the NORMAL/X5 Switch is set to "X5" position.

2. VCA Circuit
   a) Set the HOLD/EG Switch and LFO MOD Vol. to "Hold" and "0" respectively, then adjust VR10 until 2.5 ± 0.1V is obtained at TP1.
   b) After the adjustment in item 2-a) is completed, apply a sine wave of 1kHz, 5Vp-p to the AI terminal. Then, set the VOLUME to the "10" position, and adjust VR12 until a sine wave of 1.5 ± 0.2V is obtained at the OUT terminal.
   c) Set the LFO MOD Vol. to "10", apply a sine wave of 100Hz, 3Vp-p to the LFO terminal, then make sure that a waveform as in the figure below is obtainable at the OUT terminal. Then, apply 0Vp-p to the AI terminal, and adjust VR13 until a waveform having the smallest peak-to-peak level is obtained at the OUT terminal.



3. LED Lighting Circuit
   Turn a key on and off (with 0V and +5V present at the TRO terminal), and confirm that the LED lights in accordance with the key operation.

ADJUSTMENT OF REG SECTION

1. −15V Adjustment (+15V Adjustment)

   Adjust VR1 until a voltage of −15.00V is present across −15V and E terminals. Then, make sure that a voltage of +15 ± 0.15V is present across +15V and E terminals.

2. +10V Adjustment

   Adjust VR2 until a voltage of +10.00V is present across +10V and E terminals.

3. Load Characteristics

   When no load is applied, the fluctuation should be smaller than ±0.5% and should show neither oscillation nor abnormal voltage.

   Make sure that the regulator's response to load fluctuation is within 50m sec. When connecting Mylar capacitors of 0.47μF across each terminal and the E terminal, make sure that neither oscillation nor abnormal voltage is generated and the response time is within 50m sec.

4. First Stage Voltage and Output Voltage

   When load is fully applied, the output voltage fluctuation should be smaller than ±0.1% for the first stage voltage fluctuation of ±15%, and the regulator should respond within 50m sec to a drastic change in the first stage voltage.

5. Ripple Noise

   When load is fully applied, make sure that ripple noise smaller than 5mVp-p is present at each output terminal.