AIRFONIX

9 月 16 日

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RF module Reference Manual

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: To assure continued compliance, (example - use only shielded interface cables when connecting to computer or peripheral devices). Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

That be strictly restricted to integration into battery powered host devices.

IMPORTANT NOTE:

This module is intended for OEM integrator. The OEM integrator is still responsible for the FCC compliance requirement of the end product, which integrates this module.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: PSH-A710820D ". If the size of the end product is larger than the palm of the hand, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

Overview

PCT 433MHz -15dBm module is designed for low cost 433MHz ISM band wireless applications using AMICCOM A7108 FSK transceiver. This module features a fully programmable frequency synthesizer by SPI. The maximum data rate is 250kbps. Maximum output power is -15dBm.

A7108 is a monolithic low-IF architecture CMOS FSK/GFSK TRX for wireless applications in the 433MHz ISM bands. In addition, this device is especially suitable for the 470MHz wireless AMR (Auto Meter Reading) in China.

A7108 is one of AMICCOM's high performance Sub 1GHz family chips. This device offers a low cost solution with advanced radio features such as high output power amplifier up to -15 dBm (433MHz band, excluding LPF and HPF) and low phase noise receiver (- 114 dBm @ 10Kbps, -110dBm @50Kbps). Therefore, A7108 is very suitable for long LOS (line-of-sight) applications without the need to add an external LNA or PA.

The on-chip data rate divider supports programmable on-air data rates from 2K to 250Kbps to satisfy different system requirements. For a battery powered system, A7108 supports fast PLL settling time (35 us), XTAL settling time (500 us) and on-chip Regulator settling time (450 us) to reduce average power consumption.

For packet handling, A7108 supports direct mode as well as FIFO mode. In the RX direct mode, GIO1 or GIO2 can be serially output the raw data from the digital demodulator. In the TX direct mode, MCU can serially feed the digital data to GIO1 or GIO2 which is connected to the modulator. In the other hand, a packet in FIFO mode, the preamble is self-generated and the physical packet ID is programmable up to 8 bytes. The built-in separated 64-bytes TX/RX FIFO is treated as payload for data buffering including CRC of error detection, FEC of error correction, data whitening for data encryption / decryption, and Manchester encoding.

Additional device features such as on-chip regulator, low battery detect, carrier detect, preamble detect, frame sync in FIFO mode, AGC (Auto Gain Control), AFC (Auto Frequency compensation), Auto calibration (VCO and IF Filter), programmable IF Filter, multi Xtal sources, on-chip Xtal compensated capacitors, and RSSI for the clear channel assistance are used to simplify system development and cost. Overall, A7108 is a high performance and a highly integrated ISM bands TRX with low BOM cost.

1.Features:

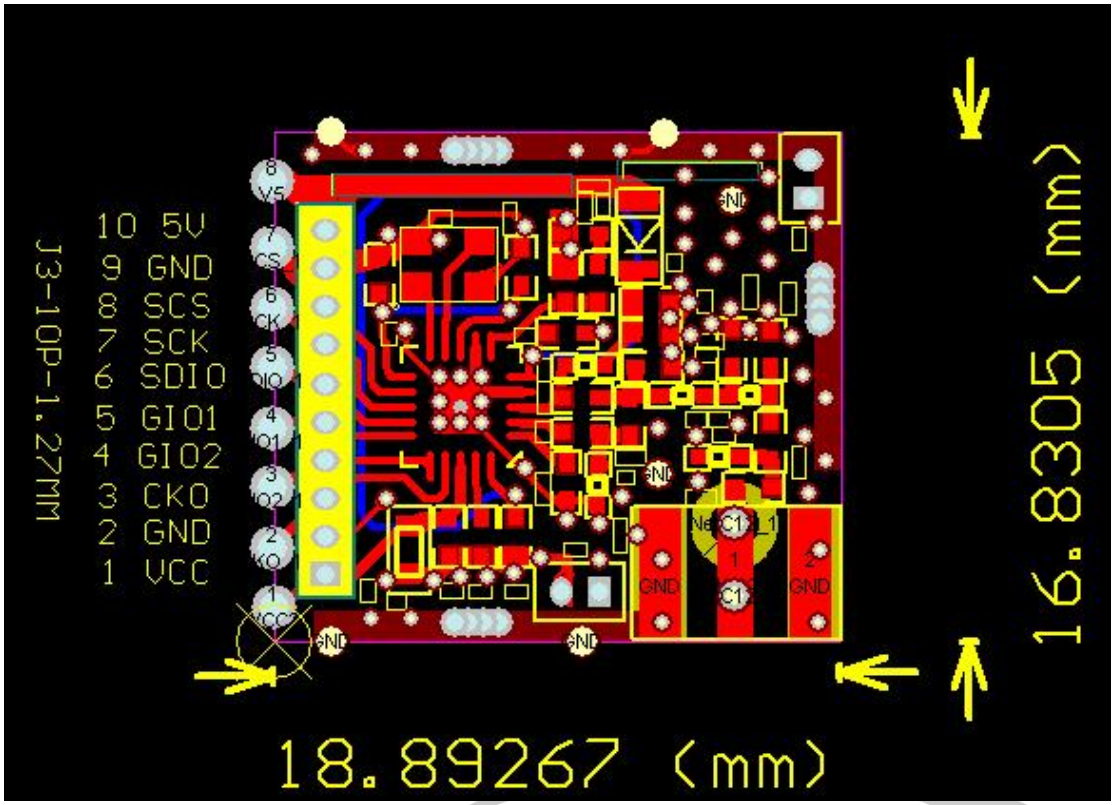
- Small size (19*18mm, 10 pins).
- Frequency band: 433MHz.
- FSK and GFSK modulation.
- Supports 3-wire or 4-wire SPI.
- Deep sleep current (0.2uA).
- Low sleep current (2 uA).
- TX Current consumption 433MHz: 30mA @ 10dBm, 70mA @ 17dBm.
- On chip regulator, supports input voltage 3.3V .

- Programmable data rate from 2Kbps to 250Kbps.
- Physical 64 bytes TX/RX FIFO buffers.
- FIFO extension up to 256 bytes.
- High RX sensitivity 433.92MHz.
  - -117dBm at 2Kbps on-air data rate.
  - -114dBm at 10Kbps on-air data rate.
  - -110dBm at 50Kbps on-air data rate.
  - -107dBm at 100Kbps on-air data rate.
  - -106dBm at 150Kbps on-air data rate.
  - -103dBm at 250Kbps on-air data rate.

Typical Applications

- Wireless ISM band data communication
- Remote Control
- RKE (Remote Keyless Entry)
- Wireless Energy Management
- Home Automation
- AMR (Auto Meter Reading)

2.Pin Configurations



Interface:

Pin No.	Symbol	Function Description
1	VCC	3.3V power supply
2	GND	Ground
3	CK0	Multi-function clock output
4	GIO2	Multi-function IO 2/SPI data output
5	GIO1	Multi-function IO 1/SPI data output
6	SDIO	SPI Data I/O
7	SCK	SPI Clock
8	SCS	SPI Chip Selection
9	GND	Ground
10	5V	5V power supply

3.Specification

(Ta=25℃, **VDD=3.3V**, F_{XTAL} =12.8MHz, FSK modulation with Matching circuit and low/high pass filter, On Chip Regulator = **1.8V**, **RFO is powered by VDD = 3.3V**, unless otherwise noted.)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	℃
Supply Voltage		3.0	3.3	3.6	V
Current Consumption	Deep Sleep Mode		0.2		uA
	Sleep Mode		2		uA
	Idle Mode(Xtal off)		0.25		mA
	Standby Mode(Xtal on)		1.5		mA
Current Consumption 433MHz band	PLL mode		8.5		mA
	RX mode (AGC Off)		13.5		mA
	RX mode (AGC On)		14.5		mA
	TX -15dBm (TBG=0, TDC=0, PAC=0)		16		mA
					mA
					mA
					mA
					mA
					mA
					mA
					mA
					mA

4.Control Register

A7108 chip contains 28 x 16-bit control registers, and can read or write data via 3-wire or 4-wire SPI interface（SCS, SCK, SDIO, GIOx）. All control registers are listed below.

Control Register Table

Add/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Systemclock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
01h PLL I	W	RXCC	RXCP1	RXCP0	MDIV	RRC3	RRC2	RRC1	RRC0	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
04h PLL IV	W	ROSCS	RSIS	CKX2	MD1	PDL2	PDL1	PDL0	MD0	VCS1	VCS0	CPS	CPC1	CPC0	SDPW	NSDO	EDI
05h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	--	CRCINV	RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
06h PA0(TX I)	W	--	LODV1	LODV0	TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
06h PA1(WORI)	W	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0	WOR_SL9	WOR_SL8	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
	R	--	--	--	--	--	--	--	--	VBD	RCO6	RCO5	RCO4	RCO3	RCO2	RCO1	RCO0
06h PA2(WOR2)	W	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0	HWCKS	WN3	WN2	WN1	WN0	CALWR	RCOSE	TSEL	TWSOE	RCOT1	RCOT0
	R	--	--	--	--	--	--	--	--	--	--	CALWR	--	--	--	--	--
06h PA3(RFI)	W	QCLIM	RF23D1	RF23D0	PRRC1	PRRC0	PRIC1	PRIC0	RMP1	RMP0	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RHM7	RHM6	RHM5	RHM4	RHM3	RHM2	RHM1	RHM0	RLM7	RLM6	RLM5	RLM4	RLM3	RLM2	RLM1	RLM0
06h PA4(PM)	W	CST	POWRS	CELS	STS	LVR	RGS	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
06h PA5(RTH)	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
06h PA6(AGC)	W	--	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0	HDM	AGCE	MXD	EXRSI	LGM1	LGM0	MGM1	MGM0
	R	--	--	--	--	--	--	--	--	--	--	--	--	LGC1	LGC0	MGC1	MGC0
06h PA7(AGC2)	W	--	--	--	--	--	--	--	--	--	--	--	--	TXIB1	TXIB0	RSA1	RSA0
06h PA8(GPIO)	W	WRCKS	MCNT1	MCNT0	DDPC	GIO2S3	GIO2S2	GIO2S1	GIO2S0	G2I	G2OE	GIO1S3	GIO1S2	GIO1S1	GIO1S0	G1I	G1OE
06h PA9(CKO)	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCT
06h PA10(VCB)	W	--	--	--	--	--	--	--	--	--	--	--	VCOC3	VCOC2	VCOC1	VCOC0	MVCS
	R	--	--	--	--	--	--	--	--	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
06h PA11(CHG1)	W	--	--	--	--	FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
	R	--	--	--	--	FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
06h PA12(CHG2)	W	--	--	--	--	FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
	R	--	--	--	--	FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
07h TX II	W	MCNTR	DPR2	DPR1	DPR0	BT1	BT0	TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
	R	ID15	ID14	ID13	ID12	ID11	ID10	ID09	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
08h RX I	W	ETH2	DMT	MPL1	MPL0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	IFBW1	IFBW0	ULS	HGM
09h RX II	W	RXDI	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
	R	--	--	--	--	--	--	--	ADCO8	ADCO7	ADCO6	ADCO5	ADCO4	ADCO3	ADCO2	ADCO1	ADCO0
0Ah ADC	W	ARSSI	RADC	AVSEL1	AVSEL0	MVSEL1	MVSEL0	XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	PWR	XEM	PLLEM	TRSM	TREM	--			ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
0Bh FIFO	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
0Ch Code	W	ERSSM	IDL1	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL0	PML1	PML0
0Dh Pin control	W	RFT2	RFT1	RFT0	PRS	SCMDS	PCS1	PCS0	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MFBS	MFB3	MFB2	MFB1	MFB0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
0Fh	W	DFCD	VBS	SWT	RSSC	VCC	--	WORE	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
Modecontrol	R	--	--	--	RSSC	VCC	FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM

Legend: -- = unimplemented

Control Register Description

System clock (Address: 00h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h System clock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
Reset		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SDR[6:0]: Data Rate Divider.

If DMOS (08h) = 0, $Data\,rate = \frac{1}{128} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$ (recommended).

If DMOS (08h) = 1, $Data\,rate = \frac{1}{64} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$

GRS: Reference Clock Selection for the internal PLL CLK Generator.

[0]: PLL CLK Gen. = F_{CGRF} x 48, where F_{CGRF} is from below GRC divider

[1]: PLL CLK Gen. = F_{CGRF} x 32

GRC[4:0]: Generation Reference Clock Divider.

GRC [4:0] is the clock divider to generate a PFD clock for the internal CLK Generator.

$$f_{CGRF} = \frac{f_{xtal}}{GRC[4:0]+1}$$

CSC[2:0]: System Clock Divider setting.

CSC is the clock divider of F_{MSCK} to generate the wanted data clock and IF calibration clock where F_{MSCK} is either from Xtal itself (CGS = 0) or from the internal CLK Generator (CGS = 1).

$$f_{CSCK} = \frac{f_{MSCK}}{CSC[2:0]+1}$$

F_{CSCK} shall be set appropriately, otherwise, IF Filter calibration will be failure.

Please refer to chapter 12 for details.

PLL I (Address: 01h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h PLL I	W	RXCC	RXCP1	RXCP0	MDIV	RRC3	RRC2	RRC1	RRC0	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Reset		0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0

RXCC: Reserved for internal usage. Shall be [0].

RXCP[1:0]: Reserved for internal usage. Shall be [00].

MDIV: RF Divider Range setting.

[0]: Range of IP[7:0] is 32~67.

[1]: Range of IP[7:0] is 68 ~ 255.

RRC[3:0]: RF PLL Reference Counter.

RRC [3:0] is the clock divider to generate a PFD clock for RF_PLL to lock the wanted LO frequency.

$$f_{PFD} = \frac{f_{xtal}}{RRC[3:0]+1}$$, please refer to Chapter 13 for details.

IP[7:0]: LO frequency Integer Part setting.

Pease refer to Chapter 13 for detail.

PLL II (Address: 02h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FP[15:0]: LO Frequency Fractional Part setting.

$$f_{RF} = \frac{1}{n} f_{PFD} \cdot (IP[7:0] + \frac{FP[15:0]}{2^{16}})$$ (unit: Hz)

where f_{RF} is the wanted RF frequency and ***n*** is the VCO divider.

where $f_{PFD} = f_{xtal} / (RRC[3:0] + 1)$, is the comparison frequency of RF_PLL.

Where n = 4 by setting MD = [10] for 433M band

Note1: MD[1:0] is located at address 04h [Bit12, Bit8].

Note2: please refer to Chapter 13 for details.

PLL III (Address: 03h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC34	MC24	MC1	MC0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AFC: Auto Frequency Compensation selection. Recommend AFC = [1].

[0]: manual

[1]: auto

MC[14:0]: PLL Fractional Part Compensation value.

[Write]：Manual setting to LO fractional part compensation value when AFC = [0].

[Read]：Frequency offset value when AFC = [1].

PLL IV (Address: 04h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h PLL IV	W	ROSCS	RSIS	CKX2	MD1	PDL2	PDL1	PDL0	MD0	VCS1	VCS0	CPS	CPC1	CPC0	SDPW	NSDO	EDI
Reset		0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0

ROSCS: RC Oscillator for WOR (Wake-On-RX) function.

[0]: single mode

[1]: differential mode

RSIS: Reserved. RSIS shall be [0].

CKX2: Reserved. CKX2 shall be [0].

MD[1:0]: RF Band select, [Bit12, Bit8].

[10]: RF in 433MHz

Note: MD[1:0] is used for the wanted RF formula (02h) and the wanted Fdev (06h, page0).

PDL[2:0]: PLL Settling Delay Time setting.

PDL [2:0]	PLL Delay Timer	Note
000	20 us	
001	40 us	
010	60 us	
011	80 us	Recommend
100	100 us	
101	120 us	
110	140 us	
111	160 us	

VCS[1:0]: VCO Current setting. Recommend VCS = [01].

CPS: Charge Pump tri-state setting. Recommend CPS = [1].

[0]: Tri-state.**[1]:** Normal operation.

CPC[1:0]: Charge Pump Current setting. Recommend CPC = [01].

[00]: 0.5mA. **[01]:** 1mA. **[10]:** 1.5mA. **[11]:** 2mA.

SDPW: Pulse Width of sigma-delta modulator. SDPW shall be [1].

NSDO: Mash sigma delta order setting. Recommend NSDO = [0].

[0]: order 2. **[1]:** order 3.

EDI: Dither Noise setting. Recommend EDI = [0].

[0]: Disable. **[1]:** Enable.

Crystal (Address: 05h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	CRCDNP	CRCINV	RTOE	RTCI	RTC1	RTC0	RTCE	XCC	XCP1	XCP0	CGS	XS
Reset		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

PGAS[3:0]: Page selector for the 06h register.

CRCDNP: CRC Mode. Shall be [0]

[0]: CRC-CCITT (X_{16}+ X_{12}+ X_5+ 1). **[1]:** Reserved.

CRCINV: CRC Inverted Select.

[0]: disable. **[1]:** enable

RTOE: Reserved. Shall be set to [0].

RTCI: Reserved. Shall be set to [0].

RTC[1:0]: Reserved. Shall be set to [00].

RTCE: Reserved. Shall be set to [0].

XCC: Crystal Current setting. Recommend XCC = [0].

[0]: Low current. **[1]:** High current.

XCP[1:0]: Crystal Regulating Couple setting. Recommend XCP = [00].

CGS: Clock Generation Selection.

[0]: disable, main clk, F_{MSCK}, is from Xtal itself.

[1]: enable, main clk, F_{MSCK}, is from the internal CLK Generator. Please refer to chapter 12 for details.

XS: Crystal Oscillator Selection. Recommend XS = [1].

[0]: disable, use external clock source from XI pin.

[1]: enable, use Xtal from XI and XO pin.

Pin Control (Address: 0Dh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh Pin control	W	RFT2	RFT1	RFT0	PRS	SCMDS	PCS1	PCS	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RFT [2:0]: RF Analog Pin Configuration. Recommend RFT= [000].

{XADS, RFT[2:0]}	BP_BG (Pin 19)	RSSI (Pin 1)
[0000]	Band-gap voltage	RSSI voltage

[0001]	Analog temperature voltage	RSSI voltage
[0010]	Band-gap voltage	No connection
[0011]	Analog temperature voltage	No connection
[0100]	BPF positive in phase output	BPF negative in phase output
[0101]	BPF positive quadrature phase output	BPF negative quadrature phase output
[0110]	RSSI voltage	No connection
[0111]	RSSI voltage	No connection
[1000]	Band-gap voltage	External ADC input source
[1001]	Analog temperature voltage	External ADC input source
[1010]	Band-gap voltage	External ADC input source
[1011]	Analog temperature voltage	External ADC input source
[1100]	No connection	External ADC input source
[1101]	No connection	External ADC input source
[1110]	No connection	External ADC input source
[1111]	No connection	External ADC input source

PRS: Read frequency mode when AFC=1. Recommend PRS= [0].

[0]: no frequency compensation.

[1]: frequency offset in AFC mode

SCMDS: Strobe Command select. Recommend SCMDS= [1].

[0]: register control. **[1]:** strobe control.

PCS1: PWR Setting. Shall be [1].

[0]: Reserved.

[1]: PWR is controlled by register or strobe command.

PCS: TRE and TRS pin control. Shall be [0].

[0]: TRE and TRS are controlled by register or strobe command.

[1]: Reserved.

IRQI: IRQ Pin Output invert. Shall be [0].

IRQ[1:0]: Reserved. Use GIOP instead. Shall be [00].

IRQE: Reserved. Use GIOP instead. Shall be [0].

CKOI: CKO pin output invert. Use 06h page 9 instead. Shall be [0].

CKO[1:0]: CKO Pin Output select. Use 06h page 9 CKOS instead. Shall be [00].

CKOE: CKO Pin Output enable. Use 06h page 9 instead. Shall be [0].

SCKI: 3-wire SPI - Clock Inverted. Recommend SCKI= [0].

[0]: Normal. **[1]:** Inverted

Calibration (Address: 0Eh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
Reset		0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

MSCRC: CRC Filtering Enable. Recommend MSCRC = [1].

[0]: Disable.

[1]: Enable.

For FIFO mode only, if MSCRC = 1, A7108 will ignore the coming packet once CRC error occurs. That means, this device will not exit RX mode but keep WTR signal high. Therefore, MCU will not be disturbed by this unsuccessful packet.

VTL[2:0]: VT low threshold setting for VCO calibration. Recommend VTL = [100].

[000]: VTL=0.1V. **[001]:** VTL=0.2V. **[010]:** VTL=0.3V. **[011]:** VTL=0.4V. **[100]:** VTL=0.5V. **[101]:** VTL=0.6V.

[110]: VTL=0.7V. **[111]:** VTL=0.8V.

VTH[2:0]: VT high threshold setting for VCO calibration. Recommend VTH = [100].

[000]: VTH=Vdd-0.1V. **[001]:** VTH=Vdd-0.2V. **[010]:** VTH=Vdd-0.3V. **[011]:** VTH=Vdd-0.4V. **[100]:** VTH=Vdd-0.5V.

[101]: VTH=Vdd-0.6V. **[110]:** VTH=Vdd-0.7V. **[111]:** VTH=Vdd-0.8V.

MVBS: VCO band calibration select. Recommend MVBS = [0].

[0]: Auto. **[1]:** Manua

MVB[2:0]: VCO bank manual setting. VCO frequency increases when MVB decreases. Recommend MVB = [000].

MIFS: IF Filter Calibration Select. Recommend MIFS = [0].

[0]: Auto. **[1]:** Manual.

MIF[3:0]: IF filter Manual Setting. Recommend MIF = [0000].

FCD [4:0]: IF Filter Auto Calibration Deviation from Goal (read only).

DVT[1:0]: VT output (Read Only).

[00]: VT< VTL< VTH.

[01]: VTL< VT< VTH.

[10]: No used.

[11]: VTL< VTH< VT.

VBCF: VCO Band Auto Calibration Flag (Read Only).

[0]: Pass. **[1]:** Fail.

VB[2:0]: VCO Bank Auto Calibration Result (Read Only).

FBCF: IF Filter Auto Calibration Flag (Read Only).

[0]: Pass. **[1]:** Fail.

FB[3:0]: IF Filter Auto Calibration Result (Read Only).

Mode control (Address: 0Fh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh Mode control	W	DFCD	VBS	SWT	RSSC	VCC	--	WORE	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
	R	--	--	--	RSSC	--	FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DFCD: Data Filter by CD. The received packet is filtered if the input power level is below RTH (0Ah).

[0]: Disable. **[1]:** Enable.

VBS: VCO Band adjustment for 433MHz.

[1]: For 433MHz band

SWT: Reserved. Recommend SWT = [0].

RSSC: RSSI Calibration.

[0]: Disable. **[1]:** Enable.

VCC: VCO Current Calibration.

[0]: Disable. **[1]:** Enable.

WORE: WOR or TWOR Enable.

[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.

[0]: Direct mode. **[1]:** FIFO mode.

CER: Chip enable by register.

[0]: chip turn-off. **[1]:** chip turn-on.

PLLE: PLL enable by register.

[0]: PLL off. **[1]:** PLL on.

TRSR: TRX Mode select by register.

[0]: RX mode. **[1]:** TX mode.

When bit TRER=1, the chip will enter TX or RX mode by TRSR register.

TRER: TRX mode enable by register.

[0]: Reserved.

[1]: By register control (CER and TRSR). In FIFO mode, this bit will be cleared after end of packet encountered.

VBC: VCO Bank Calibration enable (Auto clear when done).

[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank Calibration enable (Auto clear when done).

[0]: Disable . **[1]:** Enable.

ADCM: ADC measurement (Auto clear when done).

[0]: Disable. **[1]:** Enable.

	Non-Rx mode	RX mode
[0]	None	None
[1]	Temperature measurement	RSSI, carrier detect or external signal source conversion

FECF: FEC flag. (FECF is read clear.)

[0]: FEC pass. **[1]:** FEC error.

CRCF: CRC flag. (CRCF is read clear.)

[0]: CRC pass. **[1]:** CRC error.

5.SPI Format:

The A7108 communicates with a host MCU via 3-wire SPI interface (SCS, SCK, SDIO) or 4-wire SPI (SDO from GIO1 or GIO2) with a max data rate 10Mbps. A SPI transition is a 24-bits sequence which consists of an 8-bits address and a 16-bits data word. The MCU should set SCS (SPI chip select) pin low in order to access A7108. Via the SPI interface, user can access the **control registers** and issue **Strobe commands**. The SPI data will be latched into the registers at the rising edge of SCK. When reading registers from the RF chip, after input the wanted register address, the bit data will be transferred from the falling edge of SCK.

SPI Format

Address Byte(8 bits)								Data words(16 bits)													
R/W	Command			Address				Data													
A7	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Address Byte (8 bits):

Bit A7: R/W bit

[0]: Write.

[1]: Read.

Bit A6~A4: Command

[00x]: read/write control register.

[01x]: read/write ID code.

[10x]: read/write FIFO register.

[110]: reset TX/RX FIFO pointer.

[111]: RF chip Reset (soft reset and all registers will be clean to initial value).

Bit A3~A0: Address of control register

Strobe Command table:

Address Byte (8 bits)								description
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	A3	A2	A1	A0	Write control register
1	0	0	x	A3	A2	A1	A0	Read control register
0	0	1	x	x	X	x	x	Write ID code command
1	0	1	x	x	X	x	x	Read ID code command
0	1	0	x	x	X	x	x	TX FIFO write command
1	1	0	x	x	X	x	x	RX FIFO read command
X	1	1	1	x	X	x	x	Software Reset command
0	1	1	0	x	X	x	x	TX FIFO address pointer reset command
1	1	1	0	x	X	x	x	RX FIFO address pointer reset command
0	0	0	1	0	0	0	0	Sleep mode
0	0	0	1	0	0	1	0	Idle mode
0	0	0	1	0	1	0	0	Standby mode
0	0	0	1	0	1	1	0	PLL mode
0	0	0	1	1	0	0	0	RX mode
0	0	0	1	1	0	1	0	TX mode
0	0	0	1	1	1	0	0	Deep sleep mode (tri-state)
0	0	0	1	1	1	1	1	Deep sleep mode (pull-high)

Remark: X (Don't care).

Data Words (16-bits) : On-chip registers in sequence of D15~D0.

6.State machine:

A7108 has seven major operation modes from current consumption point of view as shown in Table 14.1. From accessing data point of view, if FMS=1 (0Fh), FIFO mode is enabled, otherwise, A7108 is in direct mode.

Key Strobe Commands

A7108 has below 7 operation modes in current consumption point of view. Those are,

(1) Deep Sleep mode

(2) Sleep mode

(3) Idle mode

(4) Standby mode

(5) PLL mode

(6) TX mode

(7) RX mode

After power on reset or software reset or deep sleep mode, user has to do calibration process because all control registers are in initial values. The calibration process of A7108 is very easy, user only needs to issue Strobe commands and enable calibration registers. If so, the calibrations are automatically completed by A7108's internal state machine. Next Table shows a summary of key circuitry among those strobe commands.

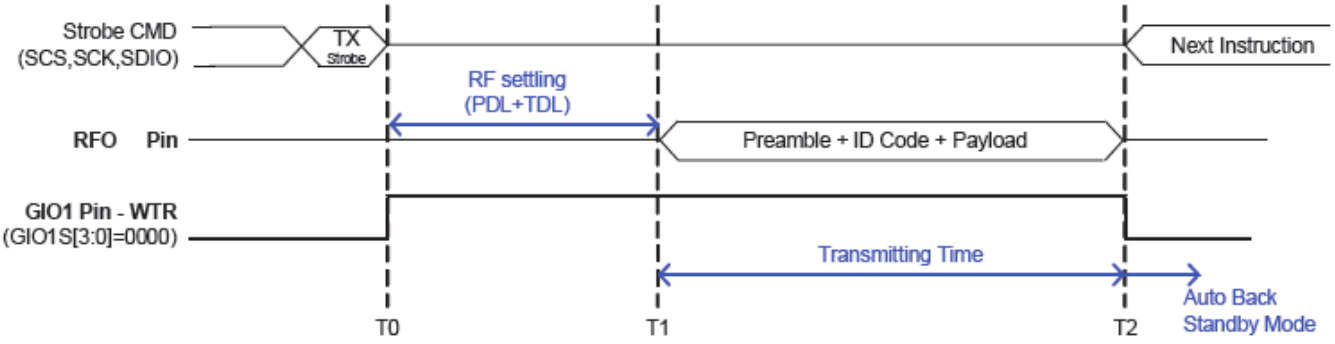
Mode	Register retention	Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Deep Sleep (Tri-state)	No	OFF	OFF	OFF	OFF	OFF	OFF	(0001-1100)b
Deep Sleep (pull-high)	No	OFF	OFF	OFF	OFF	OFF	OFF	(0001-1111)b
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	(0001-0000)b
Idle	Yes	ON	OFF	OFF	OFF	OFF	OFF	(0001-0010)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(0001-0100)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(0001-0110)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(0001-1000)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(0001-1010)b
SW RST								(x111-xxxx)b

Remark: x means "don't care"

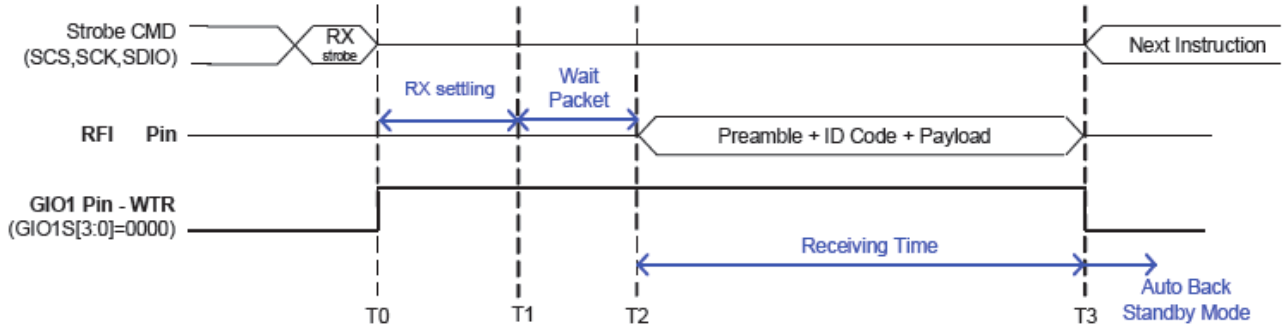
FIFO mode

This mode is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet data transmission, only one Strobe command is needed. Once transmission is done, A7108 is auto back to standby mode. Figure 14.1 and Figure 14.2 are TX and RX timing diagram respectively. Figure 14.3 illustrates state diagram of FIFO mode.

TX timing of FIFO Mode



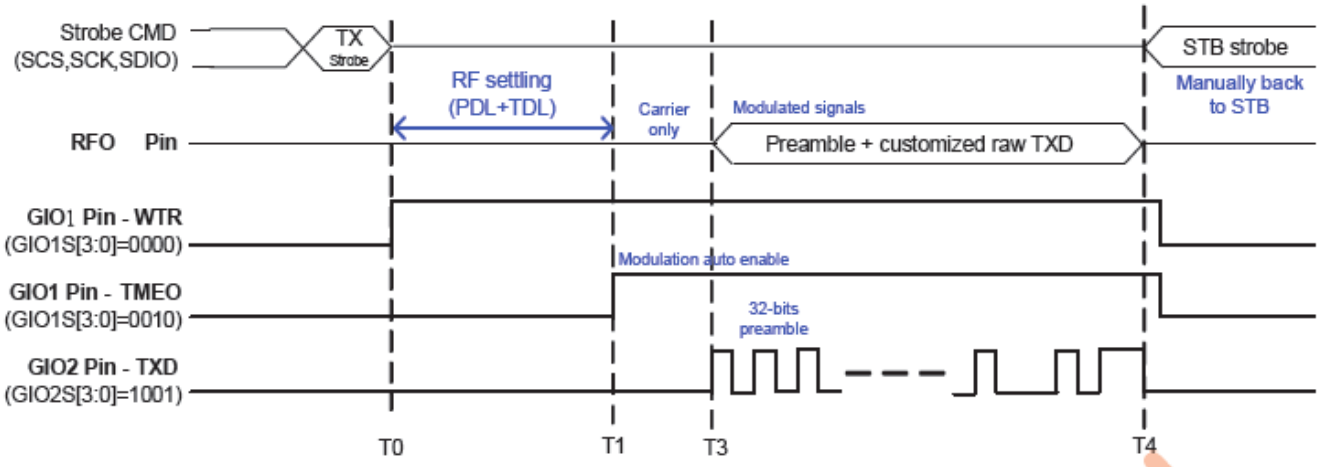
RX timing of FIFO Mode



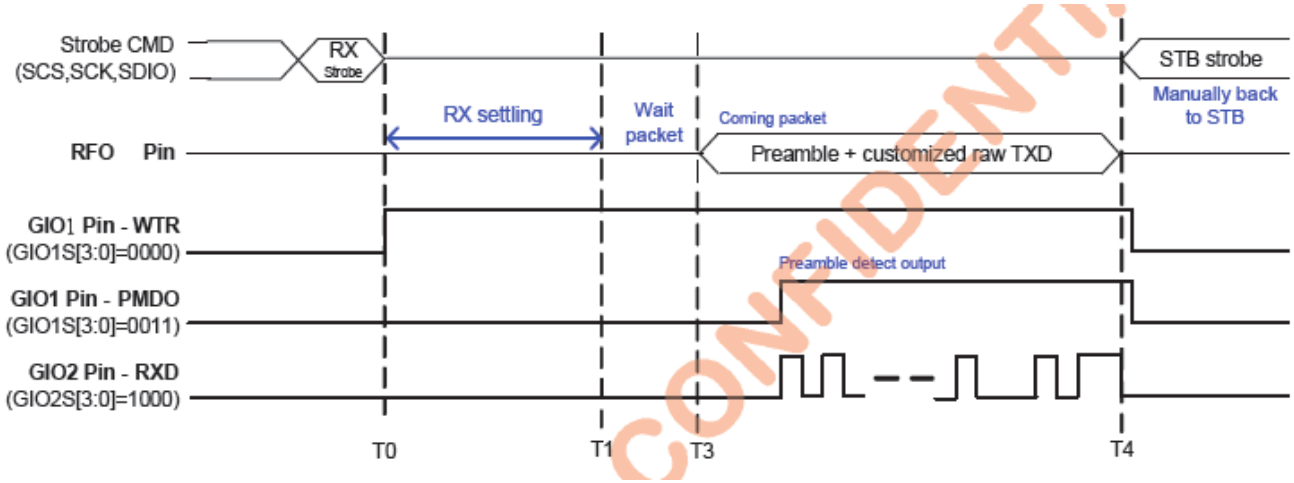
Direct mode

This mode is suitable to let MCU to drive customized packet to A7108 directly by setting FMS = 0. In TX mode, MCU shall send customized packet in bit sequence (simply called raw TXD) to GIO1 or GIO2 pin. In RX mode, the receiving raw bit streams (simply called RXD) can be configured output to GIO1 or GIO2 pin. Be aware that a customized packet shall be preceded by a 32 bits preamble to let A7108 get a suitable DC estimation voltage. After calibration flow, for every state transition, user has to issue Strobe command to A7108 for fully control. This mode is also suitable for the requirement of versatile packet format. Figure 14.4 and Figure 14.5 are TX and RX timing diagram in direct mode respectively. Figure 14.3 illustrates state diagram of direct mode.

TX timing of Direct Mode



RX timing of Direct Mode



7.Calibration:

A7108 needs calibration process during initialization with 2 calibration items, they are IF CAL (IF Filter calibration) and VCO band CAL (VCO band calibration).

1. VCO Bank Calibration is to select best VCO frequency bank for the calibrated frequency.

2. IF Filter Bank Calibration is to calibrate IF filter bandwidth and center frequency.

Please notice that VCO Current, Bank and Deviation should be calibrated in PLL mode by sequence. IF Filter Bank and RSSI could be calibrated in either standby or PLL mode.

IF Calibration Process

Under the Stand by state (XOSC is on), set bit MIFS=0(auto calibration) or bit MIFS=1(Manual calibration) to execute the IF calibration. When the mode control register bit FBC=1, the chip will enter CAL state, and starts the calibration process.

If RF chip is not in the STB state when bit FBC is set to 1, RF chip will not start the calibration process until it enters the STB state.

Once the calibration is completed, bit FBC will be cleared to 0 automatically, and RF chip will leave from CAL state and back to STB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7108 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock).

VCO band Calibration Process

Before the VCO band calibration, user should first set operating frequency in PLL I and PLL II registers, meanwhile, the range of VT (VTH[2:0], VTL[2:0]) and VCO also needs to be set properly.

Under the Stand by state (XOSC is on), set bit MVBS=0(auto calibration) or bit MVBS=1(manual calibration) to execute the VCO band calibration. After setting the mode control register bit VBC=1, the chip will enter CAL state, and starts the calibration process. If RF chip is not in the STB state when bit VBC is set to 1, RF chip will not start the calibration process until it entering STB state. When the calibration is completed, bit VBC will be cleared to 0 automatically, and chip will leave from CAL state and back to STB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state.

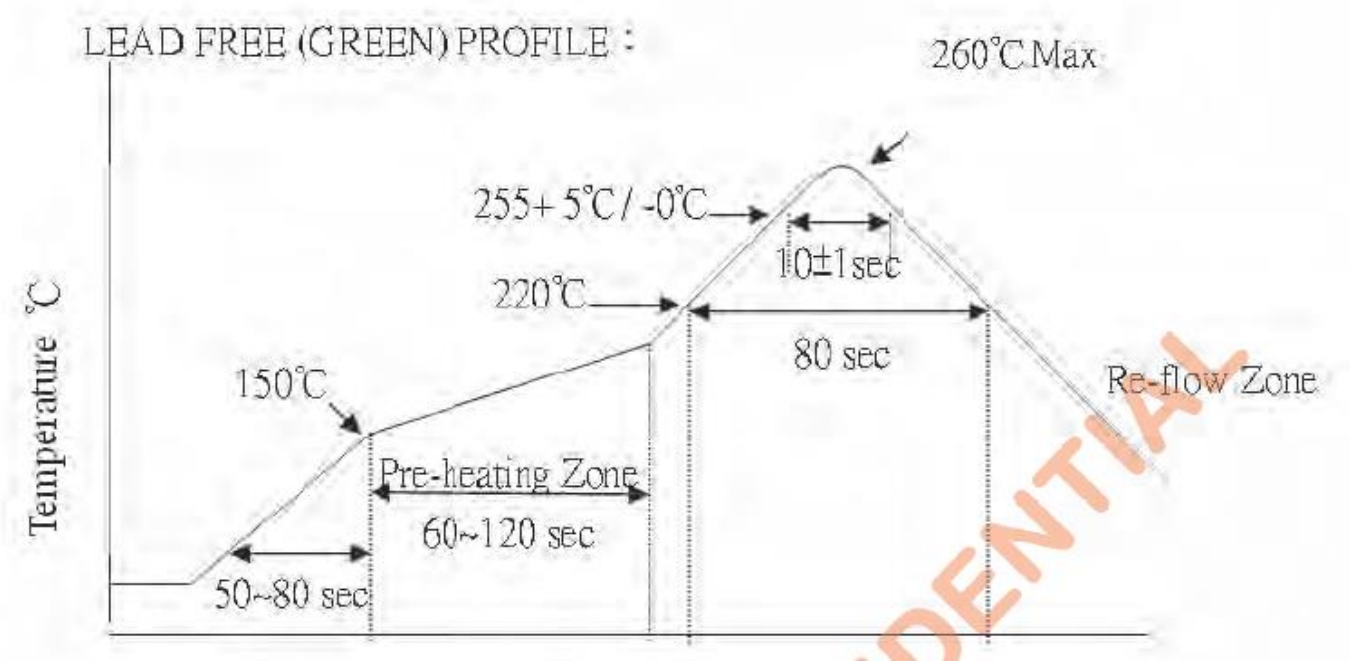
The maximum time required for A7108 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock).

The maximum time required for A7108 RF chip to perform VCO band Calibration process is about 4 * PLL settling time.

Calibration (Address: 0Eh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh Calibration	W		VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0

8.Reflow Profile:



9.Note: