

M27

GSM GPRS Wireless Module

User Manual

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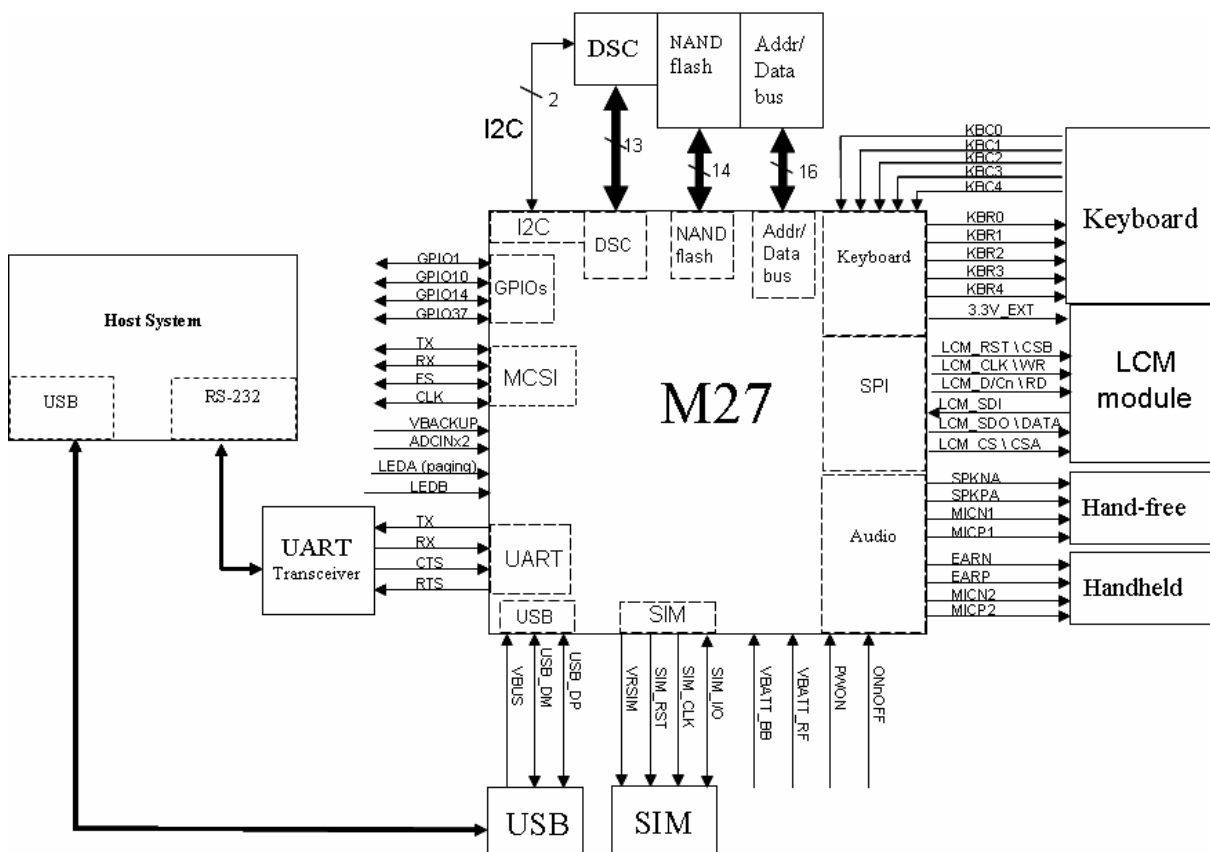
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1. Overview

This design guide is based mainly on the M27 evaluation board (EVB). The M27 EVB enables you to evaluate the M27 module and peripheral design. In addition, it provides sample firmware that you can use as a starting point to develop code. To give the users the system concept of the interconnections between the host and M27 module, a system block diagram is provided as the following:



The reference schematics for M27 peripherals will be given in details in this design guide. Since the interconnections between the host and M27 vary by application, we tend to give only reference designs of general functions, such as AT command by RS232, re-download mechanisms, and flow control of USB, etc.

2. M27 Key Features at a glance

M27 provides basic features (see in the following table) for our customers, and provide compile tool to our customers, it will gives you maximum flexibility for easy integration with the Man-Machine Interface (MMI).

| Feature | Implementation |
|-------------------------|---|
| Power supply | Single supply voltage 3.3V- 4.5V |
| Power saving | Minimizes power consumption in SLEEP mode to 3mA |
| Charging | Supports charging monitoring |
| Frequency bands | <ul style="list-style-type: none"> ● Quad-band GSM850/EGSM900/DCS1800/PCS1900 ● Compliant to GSM/GPRS Phase 2/2+ , GPRS class 10 |
| GSM class | Small MS |
| Transmit power | <ul style="list-style-type: none"> ● Class 4 (2W) at GSM850 ● Class 4 (2W) at EGSM900 ● Class 1 (1W) at DCS1800 ● Class 1 (1W) at PCS1900 |
| Audio interfaces | Two analog audio interfaces. |
| Audio features | Speech codec modes: <ul style="list-style-type: none"> ◆ Half Rate (ETS 06.20) ◆ Full Rate (ETS 06.10) ◆ Enhanced Full Rate (ETS 06.50 / 06.60 / 06.80) ◆ Adaptive Multi Rate (AMR) |
| Serial interfaces: UART | <ul style="list-style-type: none"> ● 1.8V Bi-directional bus for AT commands and data UART. ● 6-wire serial interface. Supports RTS/CTS Hardware handshake and software XON/XOFF flow control. ● Auto baud rate detects 1200 to 115200 bps ● UART can be used for CSD service and send AT command of controlling module. ● UART can be multiplexing function, you can use USB at the same time |
| LCM interface | <ul style="list-style-type: none"> ● Support 1.8V SPI interface(CS, SDO,D/Cn, CLK, RST) |
| Phonebook management | Supported phonebook types: SM, FD,LD, ME |
| SIM Application Toolkit | Supports SAT class 3, GSM 11.14 Release 98 |
| Ringing tones | Offers a choice of different ringing tones / melodies, easily selectable with AT commands |
| Temperature range | <ul style="list-style-type: none"> ● Operational temperature : -20 °C ~ +80 °C ● Functional temperature : -30 °C ~ +85 °C |

| | |
|--------------------------|--|
| | <ul style="list-style-type: none"> ● Storage temperature : -40°C ~ +85 °C |
| SMS | <ul style="list-style-type: none"> ● MT, MO, CB, Text and PDU mode |
| SIM interface | <ul style="list-style-type: none"> ● Supported SIM card: 1.8V/3V ● External SIM card holder has to be connected via interface connector (note that card holder is not part of M27) |
| External antenna | Connected via 50 Ohm antenna connector or antenna pad |
| Real time clock | Implemented |
| Physical characteristics | Size: 45.7 x 43 x 6.8 mm Weight: 11.0g |

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3. Design Guide Organization

The rest of the manual is organized as follows:

| | |
|-------------------|---|
| Section 4 | Pin out definition of M27 module is given along with the RF antenna placement and trace guidelines. In addition, the recommended power on; and handshaking sequences are shown. |
| Section 5 | Reference schematics for M27 peripheral, i.e., SIM, Audio, Keyboard, LCM, Paging indicator, Camera, NAND flash, and Micro SD. |
| Section 6 | The UART interface. |
| Section 7 | The USB interface and USB charger solution.. |
| Section 8 | GPIO mapping. |
| Section 9 | Level shifter design. |
| Section 10 | Layout notice |
| Section 11 | Antenna Interface |

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4. Pin Assignment of M27 module

The following is the pin out definition of the M27 module

| | | | |
|-----------------|----|-----|---------------------|
| VBATBB | 1 | 2 | VBAT_PA |
| GND | 3 | 4 | VBAT_PA |
| ADCIN | 5 | 6 | VBAT_PA |
| VRIO | 7 | 8 | VBAT_PA |
| LEDA | 9 | 10 | GND |
| LEDB | 11 | 12 | GND |
| ON/OFF | 13 | 14 | PWON |
| VBACKUP | 15 | 16 | VBUS |
| SIM_CLK | 17 | 18 | USB_DP |
| SIM_IO | 19 | 20 | USB_DM |
| VRSIM | 21 | 22 | ADCIN2(ADC5) |
| SIM_RST | 23 | 24 | TX1 |
| GND | 25 | 26 | RX1 |
| MICIP1 | 27 | 28 | RTS1 |
| MICIN1 | 29 | 30 | CTS1 |
| MICIP2 | 31 | 32 | GPIO37(RI) |
| MICIN2 | 33 | 34 | GPIO14(DCD) |
| GND | 35 | 36 | KBC0 |
| EARP | 37 | 38 | KBC1 |
| EARN | 39 | 40 | KBC2 |
| GND | 41 | 42 | KBC3 |
| SPKPA | 43 | 44 | KBC4 |
| SPKNA | 45 | 46 | KBR0 |
| GND | 47 | 48 | KBR1 |
| LCM_CS_CON | 49 | 50 | KBR2 |
| LCM_SDO_CON | 51 | 52 | KBR3 |
| LCM D/Cn CON | 53 | 54 | KBR4 |
| LCM_CLK_CON | 55 | 56 | GND |
| LCM_RST_CON | 57 | 58 | GND |
| LCM_SDI_CON | 59 | 60 | GPIO10 |
| 3.3V_EXT | 61 | 62 | nMOE |
| GND | 63 | 64 | DB0 |
| GND | 65 | 66 | DB1 |
| GND | 67 | 68 | DB2 |
| nCS2 | 69 | 70 | DB3 |
| nCS1 | 71 | 72 | DB4 |
| ADD19 | 73 | 74 | DB5 |
| ADD18 | 75 | 76 | DB6 |
| ADD17 | 77 | 78 | DB7 |
| ADD16 | 79 | 80 | RnW |
| I2C_2_SDA | 81 | 82 | CAM_DB0 |
| I2C_2_SCL | 83 | 84 | CAM_DB1 |
| nCAM_RST | 85 | 86 | CAM_DB2 |
| GPIO1 | 87 | 88 | CAM_DB3 |
| CAM_FWDN | 89 | 90 | CAM_DB4 |
| CAM_HS | 91 | 92 | CAM_DB5 |
| CAM_XCLK | 93 | 94 | CAM_DB6 |
| CAM_LCLK | 95 | 96 | CAM_DB7 |
| MSCI_TX(GPIO45) | 97 | 98 | MSCI_RX(GPIO46) |
| MSCI_FS(GPIO44) | 99 | 100 | MSCI_CK(AUDIO_PATH) |

NAND flash interface (14 pin assignment)

| | | | |
|-------|----|----|--------|
| NDF_0 | 1 | 2 | ND_RE |
| NDF_1 | 3 | 4 | ND_CLE |
| NDF_2 | 5 | 6 | ND_ALE |
| NDF_3 | 7 | 8 | ND_RDY |
| NDF_4 | 9 | 10 | ND_CE1 |
| NDF_5 | 11 | 12 | ND_WE |
| NDF_6 | 13 | 14 | NDF_7 |

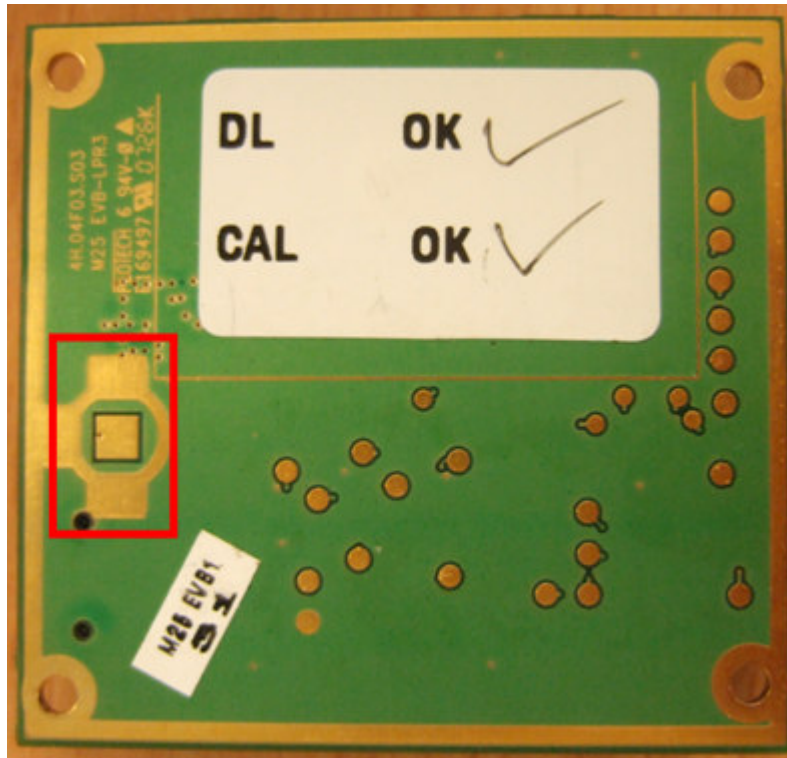
Note: For pin 97, 98, 99,100- MCSI and GPIO mixed pins, they have different functions depending on the MODE field of the pin configuration register. **Mode 0**→GPIO function, **Mode 1**→MCSI function

4.1. M27 Module Placement

In M27 module, we have one 50ohm antenna port (interfaced by Antenna pad and grounding) for signal transfer. In addition, the RF signal will be impacted by high frequency noise interference. We strongly suggest the audio trace and SIM signal trace to be as short as possible and as far away as possible from the RF trace and power line to prevent cross coupling.

The M27 offer one approach to connecting the antenna shown in the Figure:

- Antenna pad and grounding plane placed on the bottom side.



4.2. Ground Pin

There are 12 ground pins in M27 module, they should be connected to the PCB ground plane (The ground plane in PCB should be as large as possible).

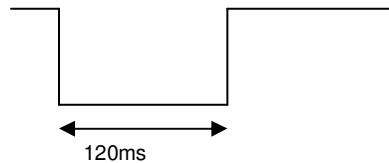
4.3. VBATRF Pin (Pin 2, Pin 4, Pin 6, Pin 8) / VBATBB Pin (Pin 1)

The “Power amplifier” is supplied by the VBATRF pins. During transmitting mode, high output power will draw a large amount of current. The width of this power trace that is connected to the VBATRF pins could not be less than **80mils**. In addition, it is better to shunt a **100uF** (low ESR) bypass capacitor on VBATRF pins to prevent voltage drop and to reduce ripple. Furthermore, another chip in the module is supplied by the VBATBB pin. The width of this trace that connected to this pin should also be wider.

4.4. PWON PIN

The pin POWON is dedicated to powering on the M27 module. The pin is initially HIGH when power is applied to the M27 module. Once the pin is pulled low for more than 120 ms. M27 will power on.

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|-------|--------|-------------|
| PWON | 14 | PU | | Input | Power On |



4.5. VBACKUP PIN

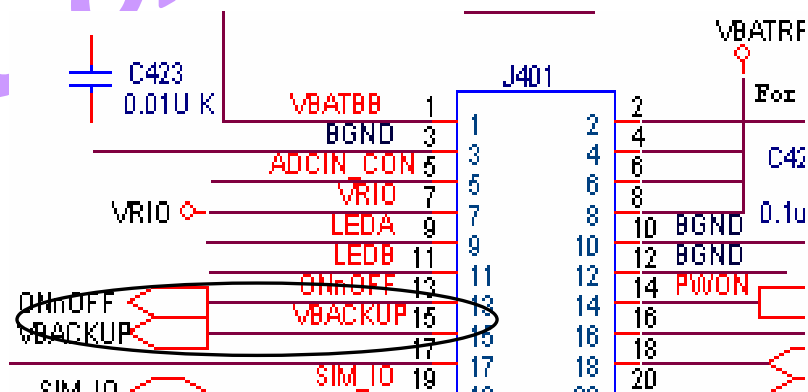
4.5.1 VBACKUP Main Feature

When main battery power (VBAT) is low or removed, real time information would be lost. For some purposes, customers would like to keep some data (e.g. RTC) in above conditions that the data can be accessed when main battery power is fed again. For example, customers need RTC continuously running while main battery is removed. To achieve this function, M27 provides VBACKUP Pin for backup battery connection. Backup battery would supply backup power to keep M27 RTC running.

4.5.2 Functional Description

To keep real time data for system application during low power or no power condition, M27 allows external battery to provide power to module built-in RTC circuit via "VBACKUP" Pin. The battery can be charged by M27 "VBACKUP" Pin as proposed in section 4.5.4. Customers could choose rechargeable battery which meets the M27 electrical specification show in next section.

If customers would like to keep real time information alive longer than an hour, Li-ion battery would be a better choice.



4.5.3 Electrical Specification

■ Power ON / Power OFF and Backup Conditions

| PARAMETER | TEST CONDITIONS | MIN | TYP | Max | UNIT |
|--|--|-----|------|-----|------|
| Battery voltage to enter ACTIV mode from OFF mode | Measured on the VBAT terminal | | 3.3 | | V |
| Battery voltage to enter BACKUP mode from ACTIV mode | VBACKUP 3.2, measured on the VBAT terminal, monitored on the ONnOFF terminal | 2.6 | 2.75 | 2.9 | V |

■ Backup Battery Charger Interface

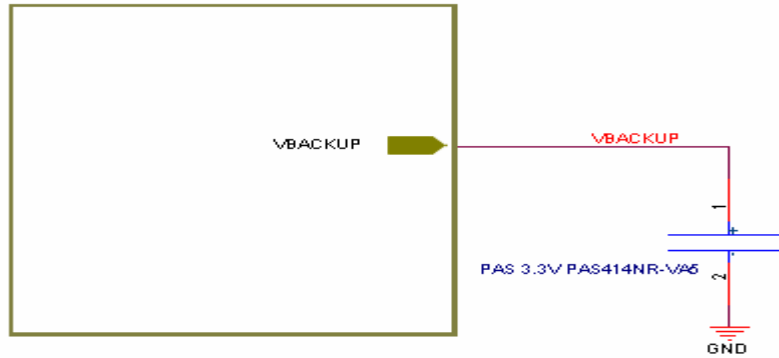
| PARAMETER | TEST CONDITIONS | MIN | TYP | Max | UNIT |
|--------------------------------------|--------------------|-----|-----|-----|------|
| Backup battery charging current | VBACKUP = 2.8 V | 350 | 500 | 900 | μA |
| End backup battery charging voltage: | IVBACKUP = -10 μA, | 2.9 | 3.1 | 3.3 | V |

■ Current consumption in BACKUP mode

| PARAMETER | TEST CONDITIONS | MIN | TYP | Max | UNIT |
|-------------------------------|--|-----|-----|-----|------|
| VBACKUP OFF mode | VBAT=3.6V, Ck=32KHz Clock ON | | 43 | 65 | μA |
| BACKUP on backup battery mode | VBACKUP=3.2V, VBAT=0V, Ck=32KHz Clock ON | | 8.6 | 12 | μA |
| | VBACKUP=0V, VBAT=2.4V, Ck=32KHz Clock ON | | 16 | 22 | |

4.5.4 General Charging Circuit

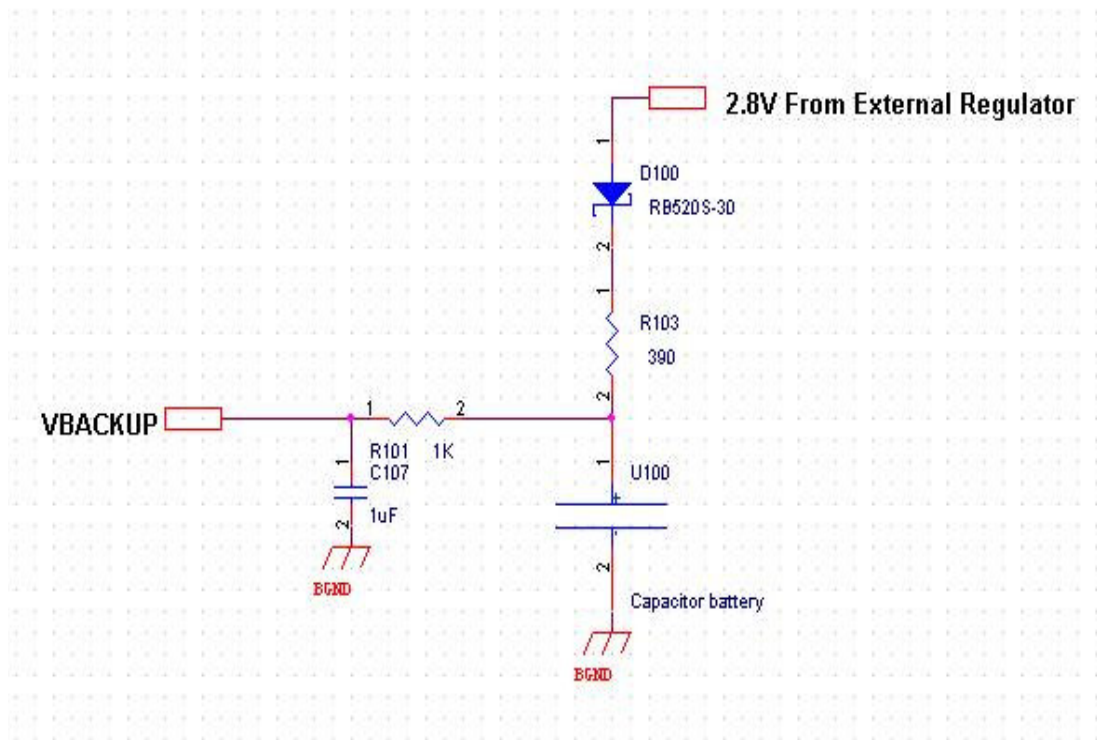
“VBACKUP” Pin is the in M27 to connect external Li-ion battery. **This reference circuit is our recommendation.**



4.5.5 VBACKUP Charging

The backup battery can be charged by an external circuit or by M27 module itself via the pad “VBACKUP”. An external circuit with a programmable voltage regulator allows recharging the backup battery. The backup battery charge starts when the following conditions are met:

- Backup battery charge is enabled by a control bit
- Charging power supply (main battery) voltage > Backup Battery voltage
- Charging power supply (main battery) voltage > 2.8V



4.6. ONnOFF PIN

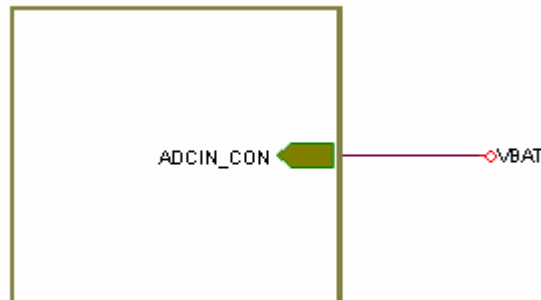
This provide Digital Baseband Rest

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|--------|--------|----------------|
| ON n OFF | 13 | PD | Output | Output | Hardware Reset |

4.7. ADCIN PIN

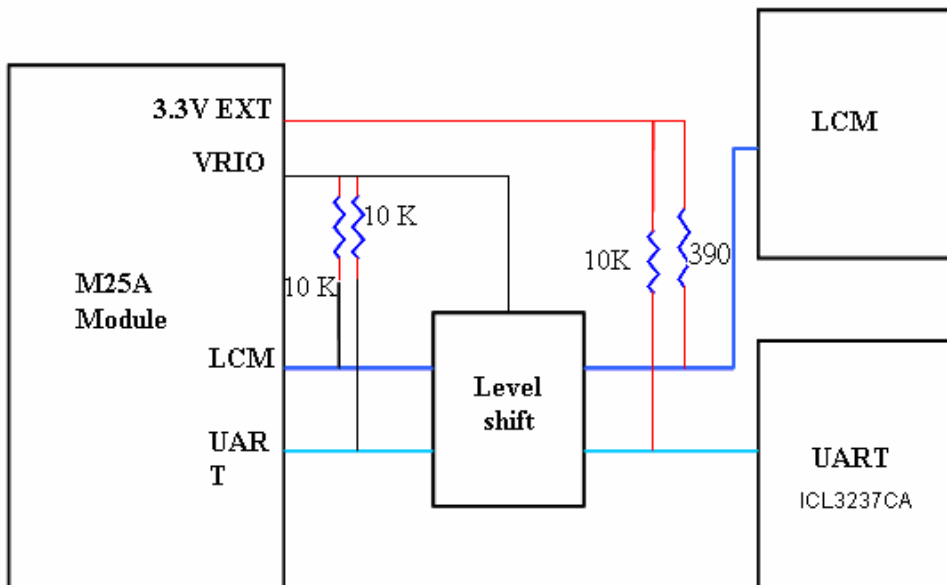
Battery monitoring is performed by the multiplexed 10-channel 10-bit ADC MADC used to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage and the backup battery voltage. The signals are converted into digital 10-bit words, stored in auxiliary ADC output registers and transmitted to an external C. **This reference circuit is our recommendation.**

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|-------|--------|--------------------------------|
| ADCIN | 5 | | Input | | Main Battery Voltage detection |
| ADCIN2 | 22 | | Input | | A/D converter |



4.8. 3.3V EXT PIN

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|-------|--------|--|
| 3.3V_EXT | 61 | | | | 3.3V Power Supply for LCM & Back light LED and UART in M27 EVB |



4.9. VRIO PIN

Power supply for external level shifters

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|-------|--------|---|
| VRIO | 7 | | | | 1.8V output voltage for external level shifters(Note) |

Note: Level shifter: *PMGD280UN* for UART, *ADG3308BRUZ-REEL* for NAND flash, Add/data bus, *SN74LVCH162244AGR*, *PCA9306DCTR* and *SN74AVC1T45YZPR* for Camera

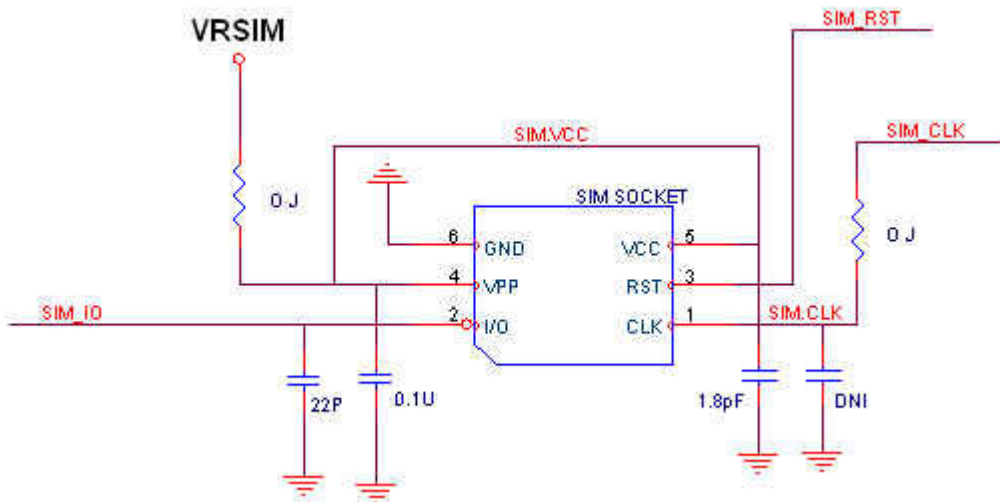
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5 Peripherals

5.1. SIM

The SIM Card digital interface in the M27 ensures the translation of logic levels between M27 and the SIM Card, for the transmission of 3 different signals: SIM_CLK; a reset signal from M27 to the SIM Card (SIM_RST); and serial data from M27 to the SIM Card (SIM_IO). The SIM card interface can be programmed to drive a 1.8V SIM Card.

6 Pin SIM Socket

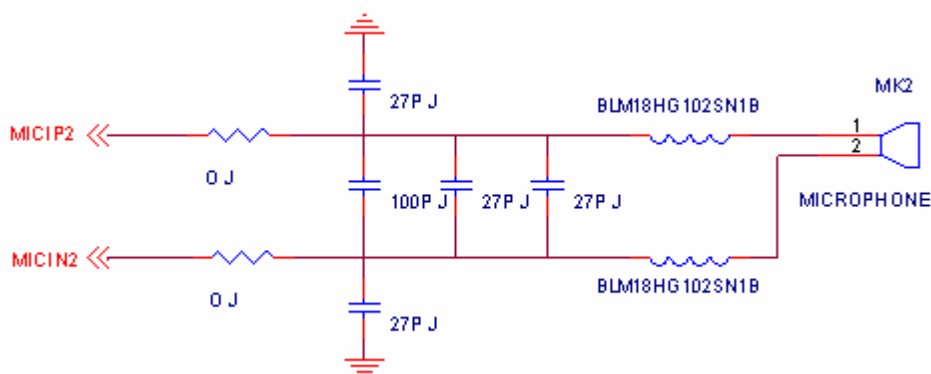


5.2. Audio

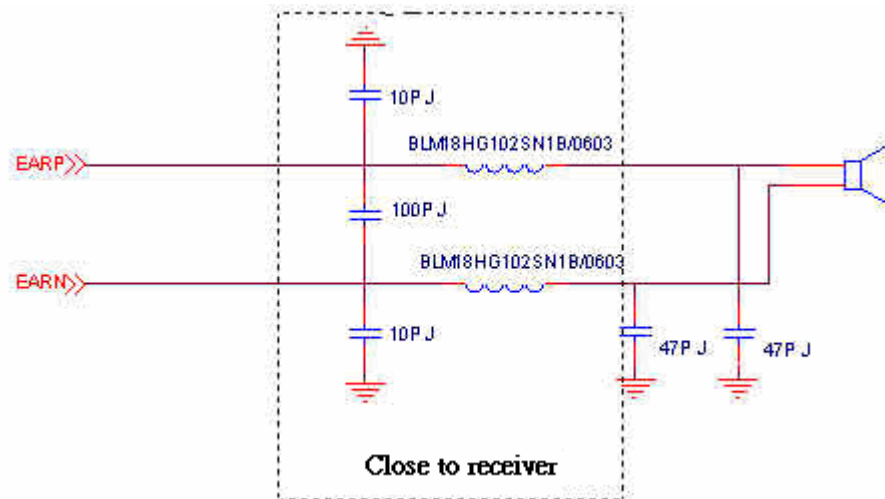
There are 2 embedded audio drivers built in the BenQ M27 module. The 2 drivers can drive different kinds of audio load (such as Handheld, or hands free).

■ Handheld

➤ Microphone 2

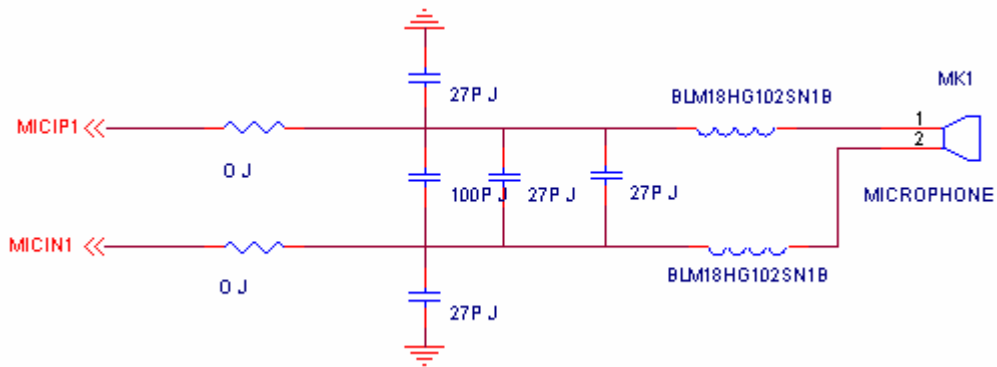


➤ **Ear output**

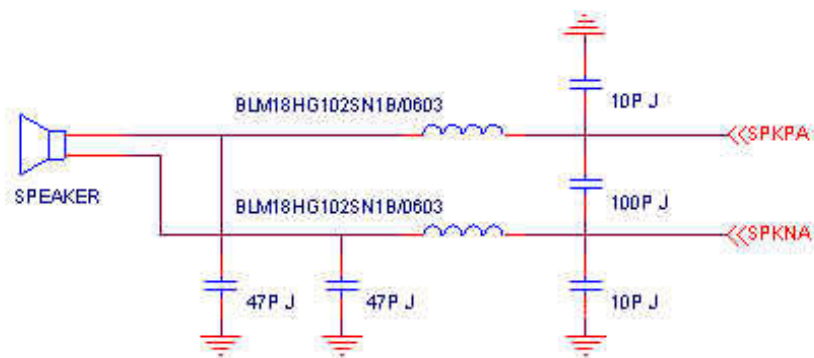


■ **Hand free**

➤ **Microphone 1**



➤ **Speaker output**



Audio Path Selection AT Commands

The M27 module provides the switching of audio paths using AT commands (In connection status):
 Default value: case (1)

- (1) AT\$HANDHELD (EARN, EARP, MICIN2, MICIP2)
- (2) AT\$HANDFREE (SPKPA, SPKNA, MICIN1, MICIP1)

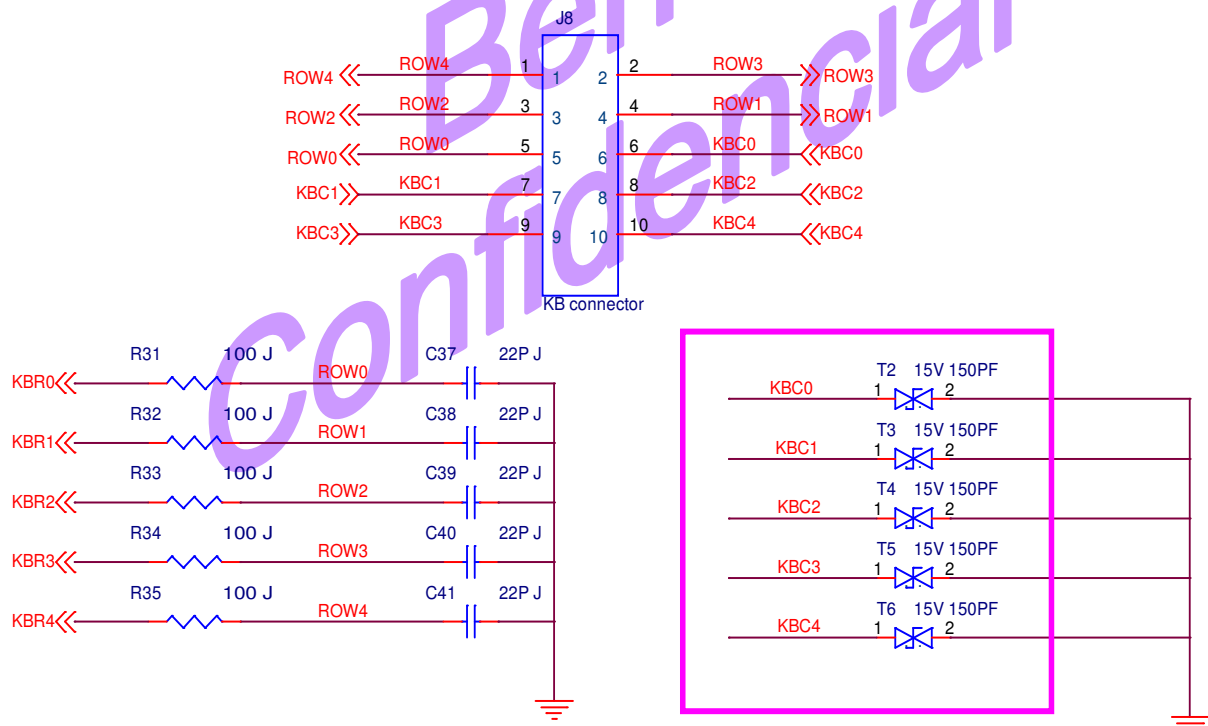
5.3. KEYBOARD

5.3.1 Keyboard Controller Overview

The keyboard controller can handle up to 5*5 keyboards, operates on a 32-kHz clock, and can generate wake-up events when the device is in sleep mode, **and this reference circuit is our recommendation.**

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|------------|--------|-------------------------------|
| KBR0 | 46 | PU | Input high | | Keypad matrix 4 Row access |
| KBR1 | 48 | PU | Input high | | Keypad matrix 4 Row access |
| KBR2 | 50 | PU | Input high | | Keypad matrix 4 Row access |
| KBR3 | 52 | PU | Input high | | Keypad matrix 4 Row access |
| KBR4 | 54 | PU | Input high | | Keypad matrix 4 Row access |
| KBC0 | 36 | | Output | | Keypad matrix 4 column access |
| KBC1 | 38 | | Output | | Keypad matrix 4 column access |
| KBC2 | 40 | | Output | | Keypad matrix 4 column access |
| KBC3 | 44 | | Output | | Keypad matrix 4 column access |
| KBC4 | 46 | | Output | | Keypad matrix 4 column access |

5.3.2 Reference circuit



Close to the Key Pad connector

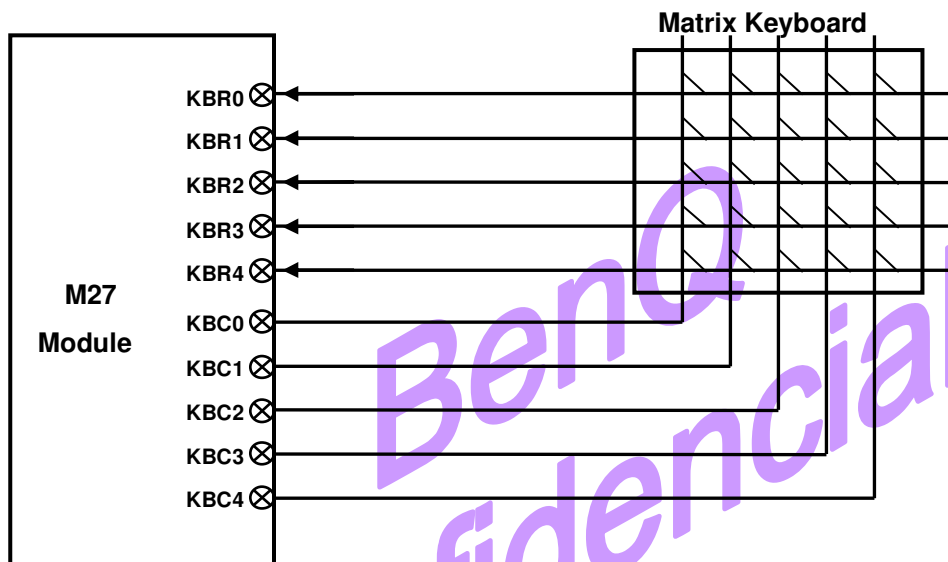
5.3.3 Main Features

The keyboard controller includes the following main features:

- Support of multi-configuration keyboards up to 5 rows x 5 columns
- Integrated programmable timer
- Programmable interrupt (IT) generation on key events
- Event detection on both key press and key release
- Multi-key press detection and decoding
- Long key detection on prolonged key press
- Programmable time-out on permanent key press or after keyboard release

5.3.4 Signals and I/O Description

Figure shows a typical 5*5 keyboard connection to the M27 keyboard controller.



5.3.5 Key Mapping

| | C0 | C1 | C2 | C3 | C4 |
|----|----------|----|------|------|--------|
| R0 | Select | Up | Down | Dial | Return |
| R1 | Vol+ | 1 | 2 | 3 | SMS |
| R2 | Vol- | 4 | 5 | 6 | ESC |
| R3 | Re-Dial | 7 | 8 | 9 | Del |
| R4 | Handfree | * | 0 | # | Set |

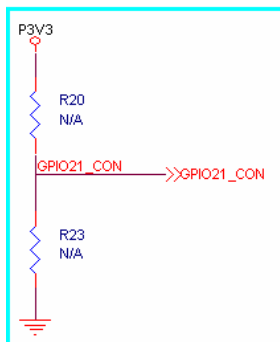
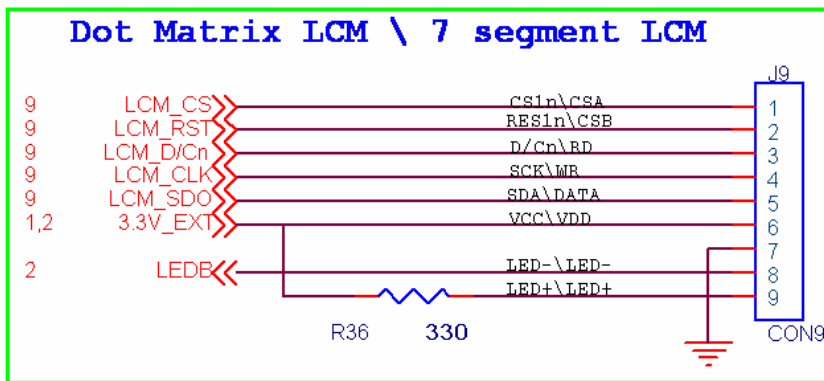
5.4. LCM (SPI interface)

M27 Provides SPI LCM interface for customer application, it gives you the flexibility to develop customized application, **and this reference circuit is our recommendation.**

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|-------|--------|--|
| 3.3_EXT | 61 | | | | Power Supply for LCM & Back light LED |
| LCM_CS | 49 | | | | Chip Select \ Chip Select A |
| LCM_SDO | 51 | | | | Serial input data \ Serial Input Data |
| LCM_D/Cn | 53 | | | | Register select Input pin (Data/Instruction) \ Read signal |
| LCM_CLK | 55 | | | | Serial Input clock \ Write signal |
| LCM_RST | 57 | | | | Reset Input Pin \ Chip Select B |
| LEDB | 11 | | | | Back light LED Sink |

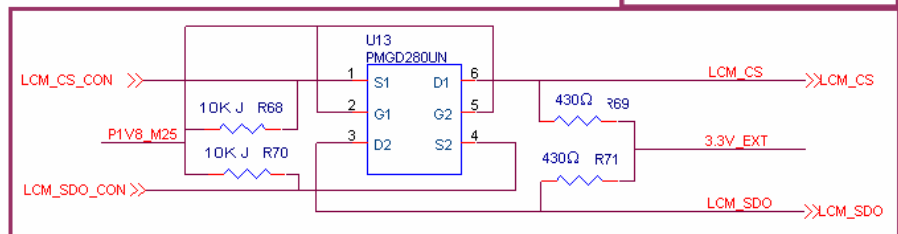
5.4.1 Reference schematics

LCM interface -Schematics



For GPIO21
 "Hi" → Dot Matrix LCM
 "Low" → 7 segment LCM

Level Shift Circuit



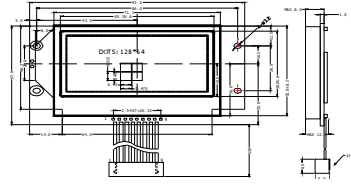
5.4.2 Dot Matrix LCM spec

Dot Matrix LCM spec

SHENZHEN WELLST WGM12864COG-21

General specifications

Display format: 128 * 64 dot matrix graphic
 Microprocessor interface: Serial
 Power level: 3.3V
 Module size: 92 x 57X8 mm



Definition of Terminals

| Pin No. | Symbol | Level | Function |
|---------|--------|-------|--|
| 1 | CS1B | L | Chip select |
| 2 | RES1B | L | Reset input pin |
| 3 | D/C | H/L | Register select input pin (Data/Instruction) |
| 4 | SCK | H/L | Serial input clock |
| 5 | SDA | H/L | Serial input data |
| 6 | VCC | 3.0V | Power supply for lcm |
| 7 | GND | 0V | Ground |
| 8 | LED- | 0V | Power supply for LED |
| 9 | LED+ | 3V | Power supply for LED |

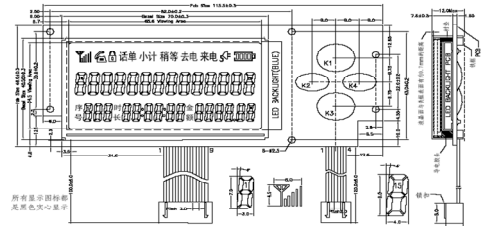
5.4.2 7 Segment LCM spec

7 segment LCM spec

深圳精銳通 WSM-6861A

General specifications

Display format: 29 Digit(7 segment)+24 Prompt
 Microprocessor interface: Serial
 Power level: 3.3V
 Module size: 115.5 x 48X12 mm



Definition of Terminals

| Pin No. | Symbol | Level | Function |
|---------|--------|---------------------|------------------------------------|
| 1 | VDD | 3.3V | Main Power |
| 2 | GND | 0V | Ground |
| 3 | DATA | CMOS (In) (Pull up) | Serial input data |
| 4 | /WR | CMOS (In) (Pull up) | Write signal (Rising edge trigger) |
| 5 | /RD | CMOS (In) (Pull up) | Read signal (Rising edge trigger) |
| 6 | /CSA | CMOS (In) (Pull up) | Chip Select A |
| 7 | /CSB | CMOS (In) (Pull up) | Chip Select B |
| 8 | LED+ | 3.3V | Power supply for LED |
| 9 | LED- | 0V | sink pin for LED |

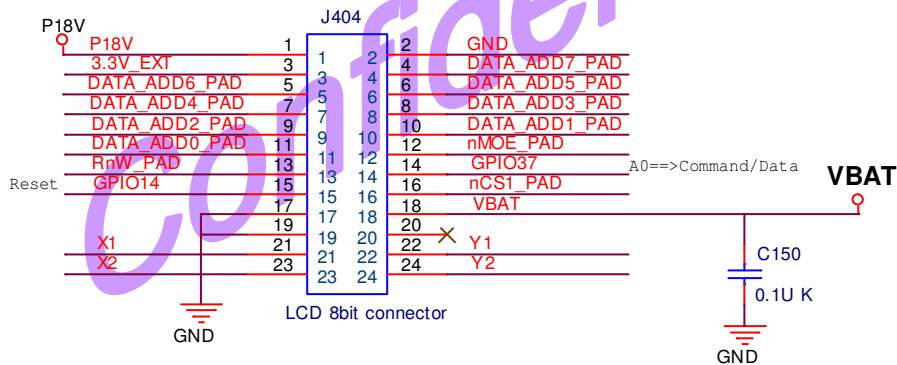
5.5. LCM (parallel bus interface)

M27 provides parallel bus (8 bit) LCM interfaces for customer application. It gives you the flexibility to develop customized application, and a reference circuit is provided here.

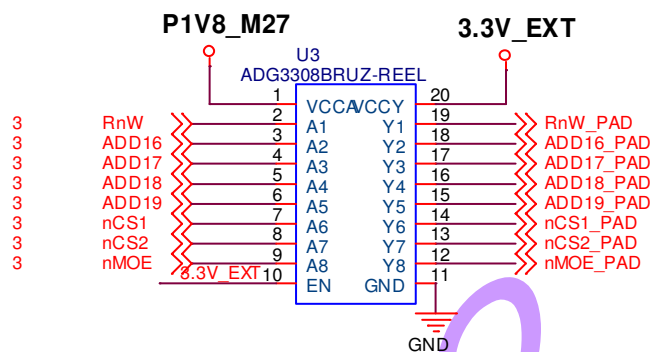
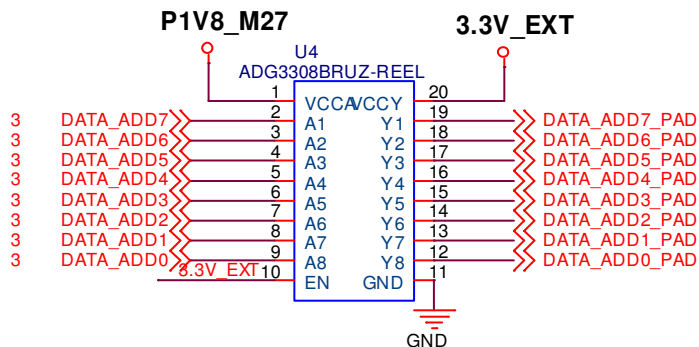
LCM parallel bus signal pins of M27 module

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|-----------|---------|------|-------|--------|--------------------|
| DATA/ADD0 | 64 | | | | Bit 0 for Data bus |
| DATA/ADD1 | 66 | | | | Bit 1 for Data bus |
| DATA/ADD2 | 68 | | | | Bit 2 for Data bus |
| DATA/ADD3 | 70 | | | | Bit 3 for Data bus |
| DATA/ADD4 | 72 | | | | Bit 4 for Data bus |
| DATA/ADD5 | 74 | | | | Bit 5 for Data bus |
| DATA/ADD6 | 76 | | | | Bit 6 for Data bus |
| DATA/ADD7 | 78 | | | | Bit 7 for Data bus |
| RnW | 80 | | | | Write signal |
| nMOE | 62 | | | | Read signal |
| GPIO37 | 32 | | | | A0==>Command/Data |
| GPIO14 | 34 | | | | Reset |
| 3.3V_EXT | 61 | | | | 3.3V power supply |

5.5.1 Reference schematics (LCM connector pins on M27 EVB)

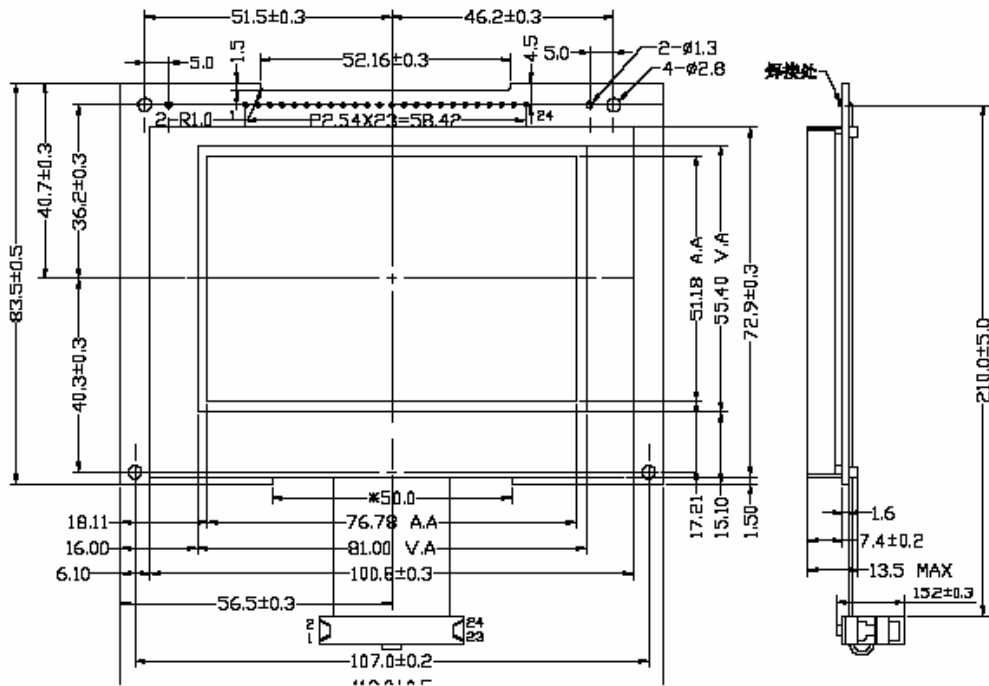


Level shifters between M27 pins and LCM connector



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5.5.2 Dimension and Pin assignment for parallel bus type LCM (YMC240160-04AAAYDGL)



注:

1. 带触摸屏;
2. 此模块必须外加VLCD电压, 值为18V左右;
3. 白背光和绿背光可互换, 橙色效果不好, 需试验。

Note:

1. Operating voltage: 3.3V
2. Drive method: 1/160Duty, 1/13Bias
3. Viewing direction: 6:00
4. Operating temp.: -20°C~60°C
5. Storage temp.: -20°C~70°C
6. Display type: FSTN, Positive
7. IC: ST7529 COG 4 GRAY SCALE
8. LED voltage: 3.3V



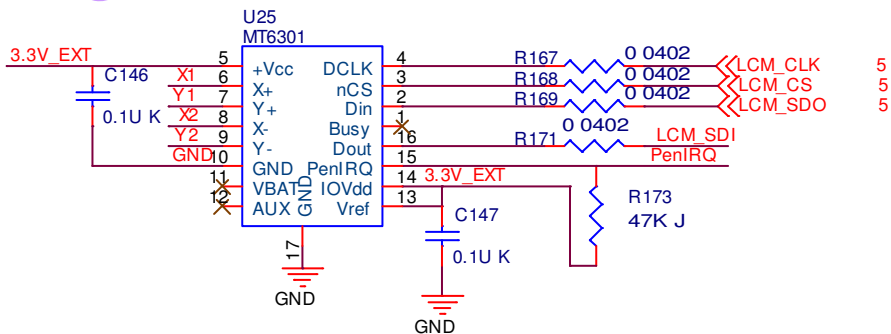
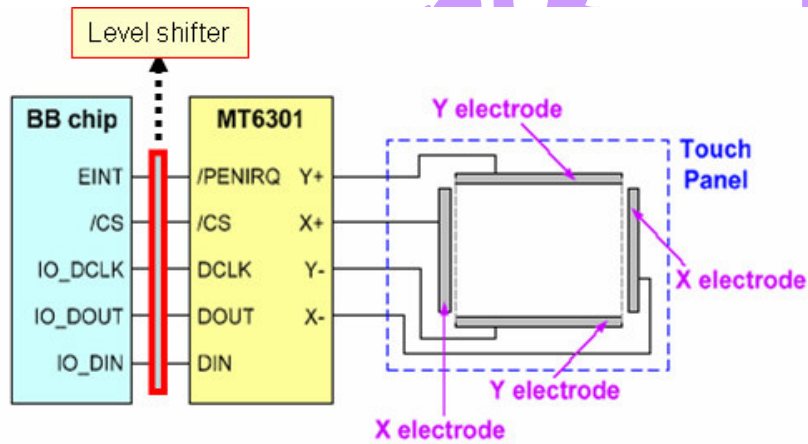
Pin assignment of parallel bus type LCM (YMC240160-04AAAYDGL)

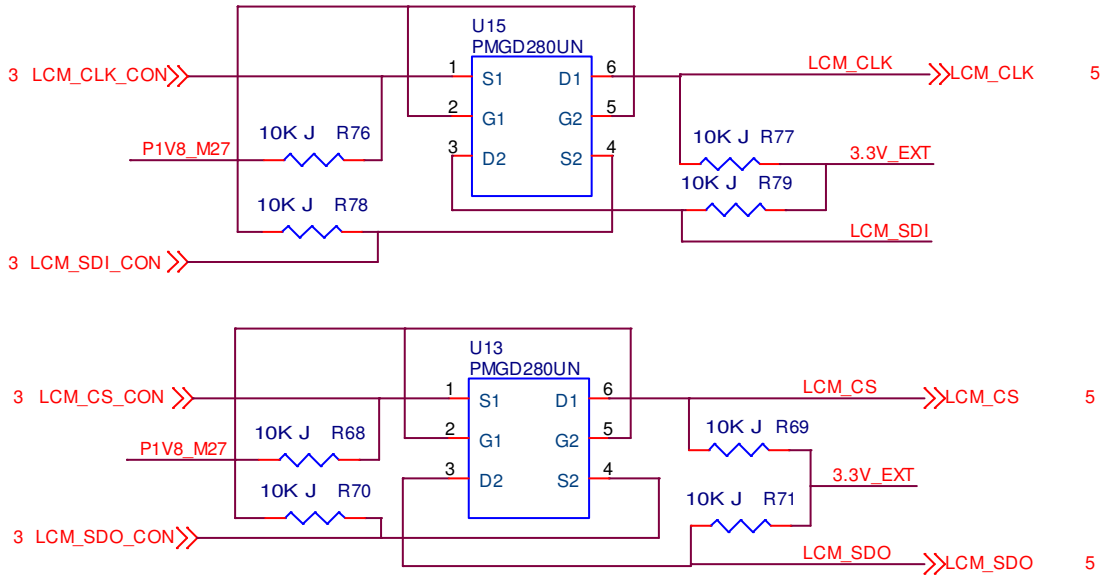
| | | | | | |
|------|----|------|----|-------|------------------------|
| +18V | 1 | VLCD | 13 | WR | |
| | 2 | VSS | 14 | AO | |
| | 3 | VDD | 15 | RST | |
| | 4 | D7 | 16 | XCS | |
| | 5 | D6 | 17 | VLED- | GND |
| | 6 | D5 | 18 | LED + | VBATT |
| | 7 | D4 | 19 | LED - | GND |
| | 8 | D3 | 20 | NC | |
| | 9 | D2 | 21 | X1 | Touch Screen Interface |
| | 10 | D1 | 22 | Y1 | |
| | 11 | D0 | 23 | X2 | |
| | 12 | RD | 24 | Y2 | |

5.6. Touch screen controller

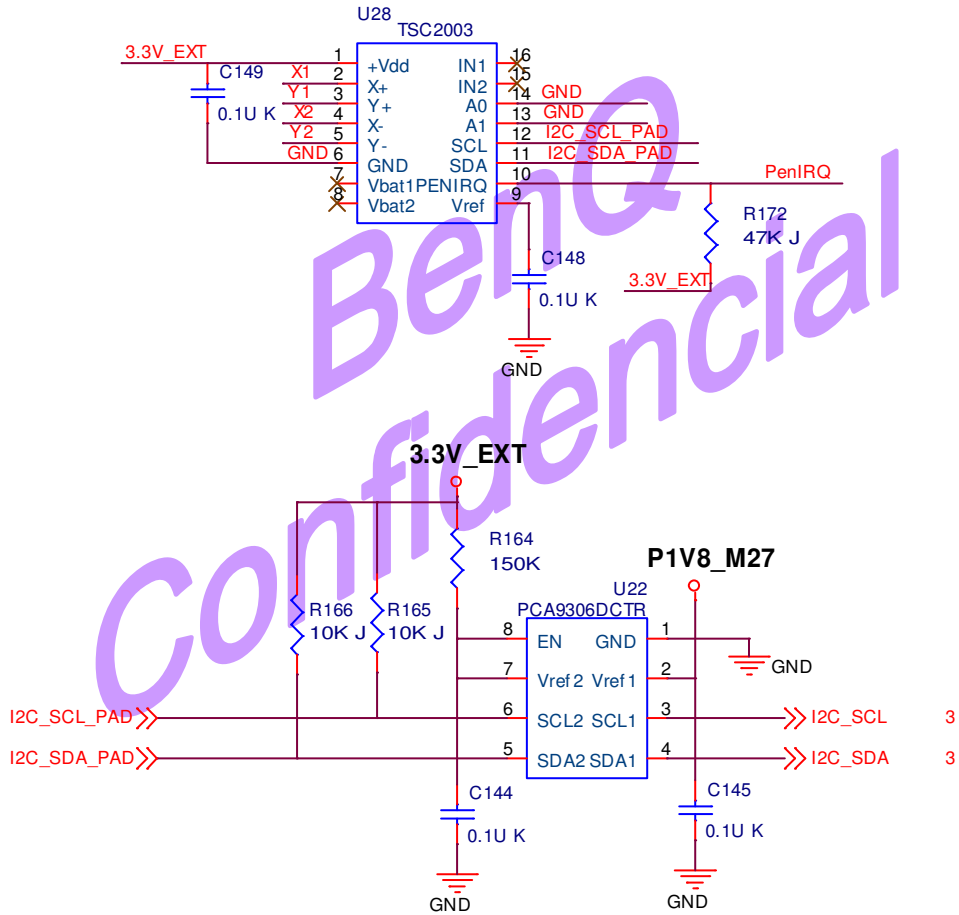
For USB charger application, there are two choices for the touch screen controller with SPI interface or I2C interface.

5.6.1 SPI type touch screen controller(MTK MT6301)





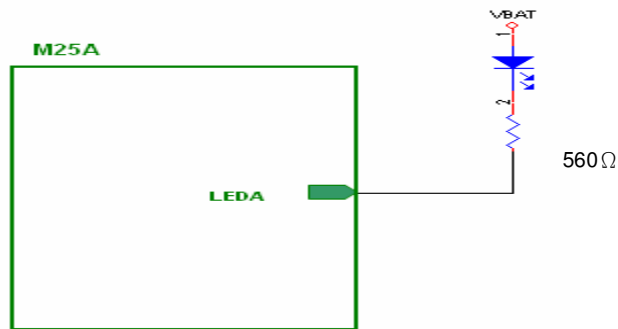
5.6.2 I²C type touch screen controller(TI TSC2003)



5.7. Paging Indicator

LEDA is dedicated for paging indication. The application circuit is shown as below. The diagram below illustrates the application schematic for LED driver inputs LEDA. In each case the current limiter resistor R has to be selected in order to be compliant with maximum current drive capability of each input.

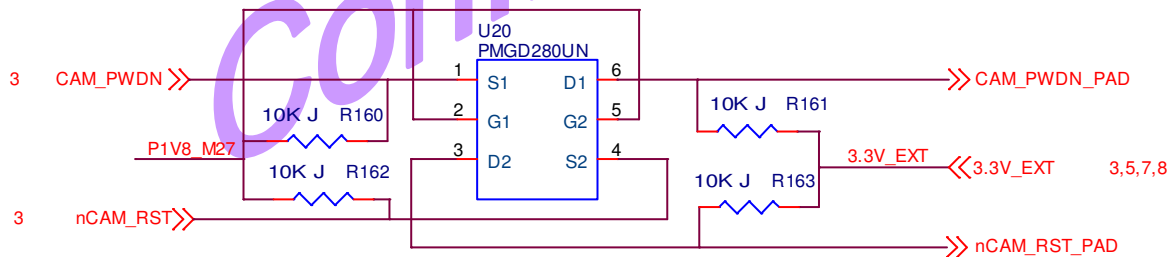
| Name | Pin | Max drive current | Highest level voltage | Lowest level voltage | supply | Description |
|------|-----|-------------------|-----------------------|----------------------|--------|------------------|
| LEDA | 9 | 20mA | VBATBB | 2.4 | VBATBB | paging indicator |

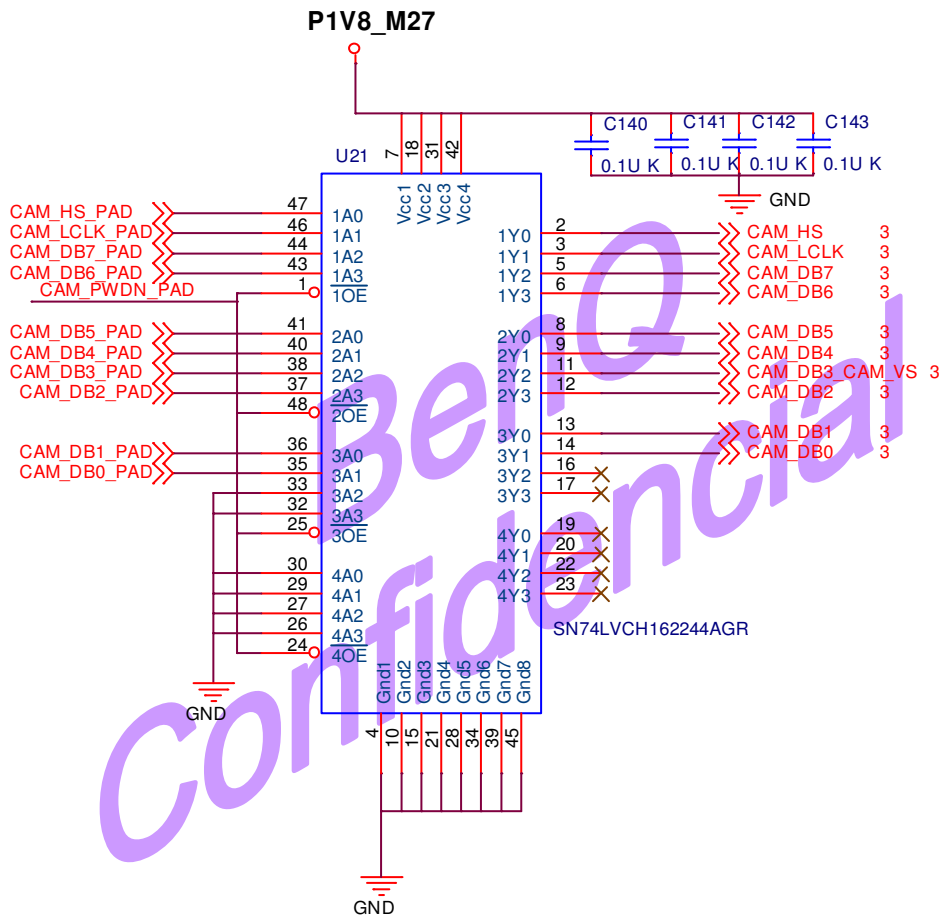
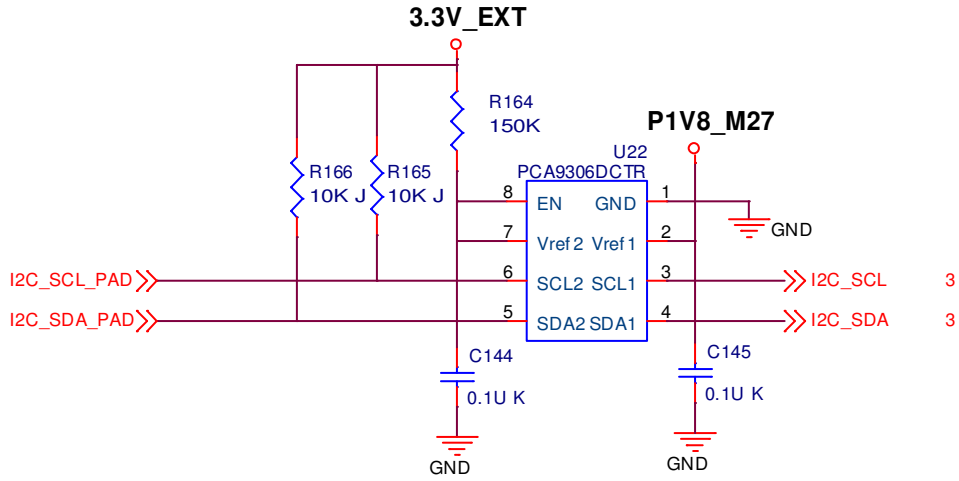


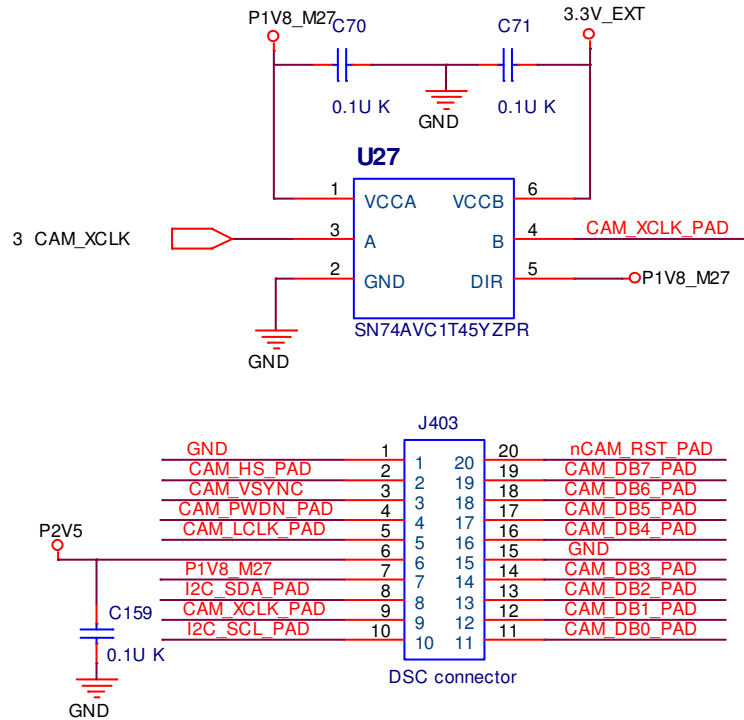
LEDA is controlled through software program using a dedicated GPIO, which is built in the M27 module, it can write program to control the LED pin state.

5.8. Camera interface

The camera interface supports data in ITU-R BT.656 format. The ITU-R BT.656 Standard specifies a method for transferring YUV422 data over an 8-bit interface. The Parallel Camera module can provide a Camera Reference clock (CAM_XCLK) to the camera sensor based on on-chip APLL (48MHz) clock sources

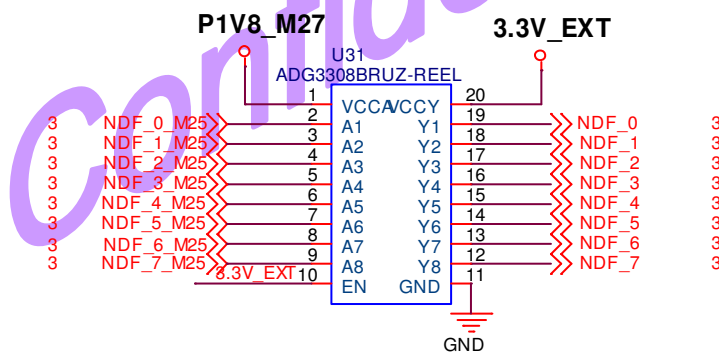


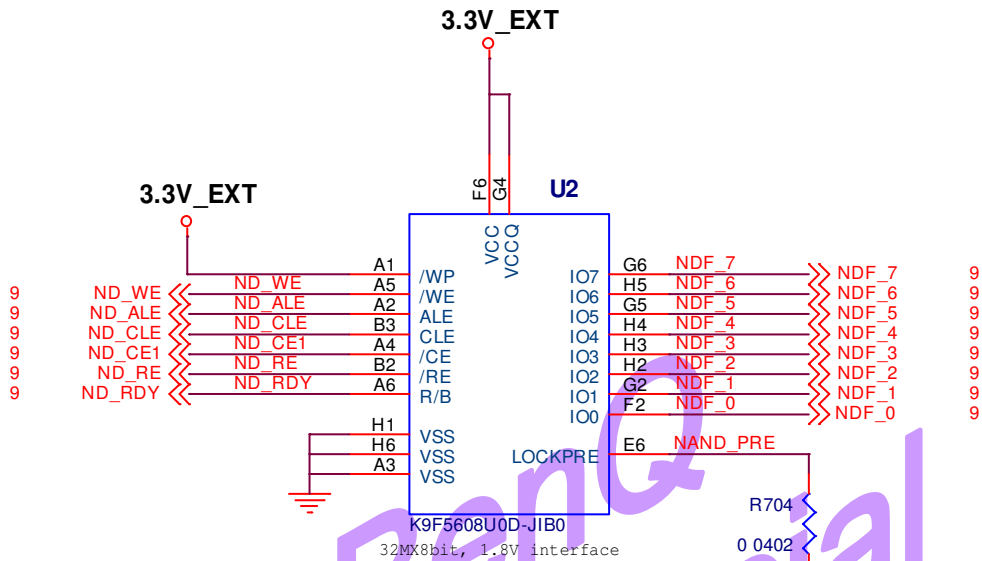
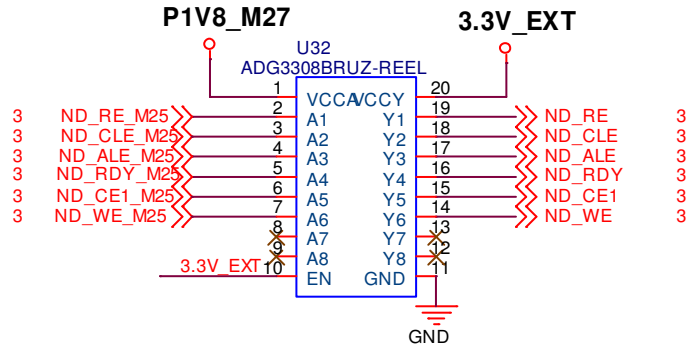




5.9. NAND flash interface

The aim of this NAND flash controller is to have a fully automatic transfer process from/to the NAND flash port. The interface implements an 8-bit parallel data bus (commands, addresses, and data are multiplexed) in addition to the control signals for selecting chip, writing/reading, command and address latching, and ready/busy status. The NAND flash chip used in M27 EVB is Samsung K9F5608U0D-JIB0 FBGA (32M x 8 Bit Memory). It is necessary to add 2 pcs of bi-directional level shifter to interface the M27 and the NAND flash chip.

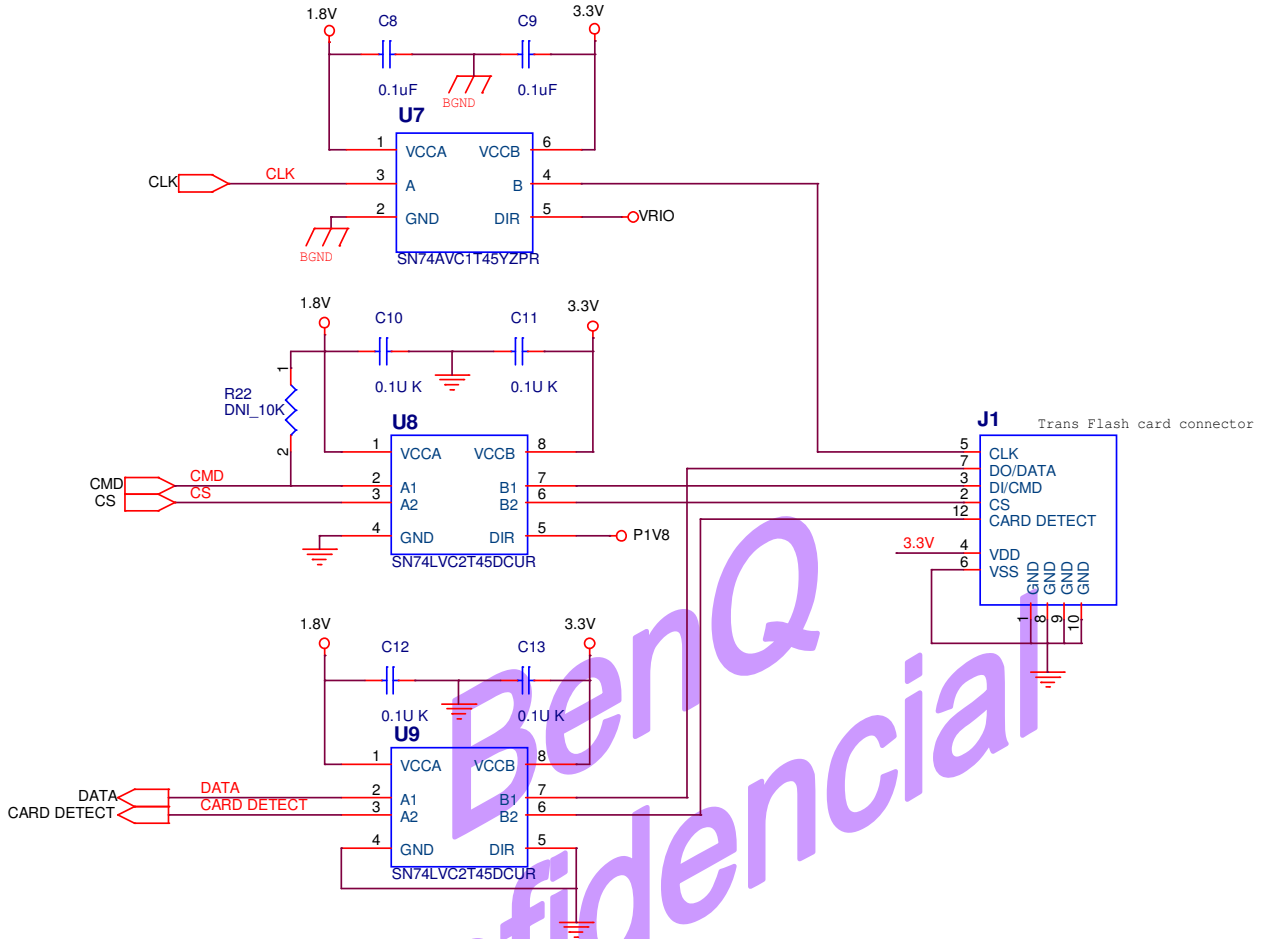




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5.10. Micro SD interface

The micro-SD card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the micro-SD card SPI channel consists of the following 4 signals: CS, CLK, DI, DO



6 UART Interface

■ UART/RS232

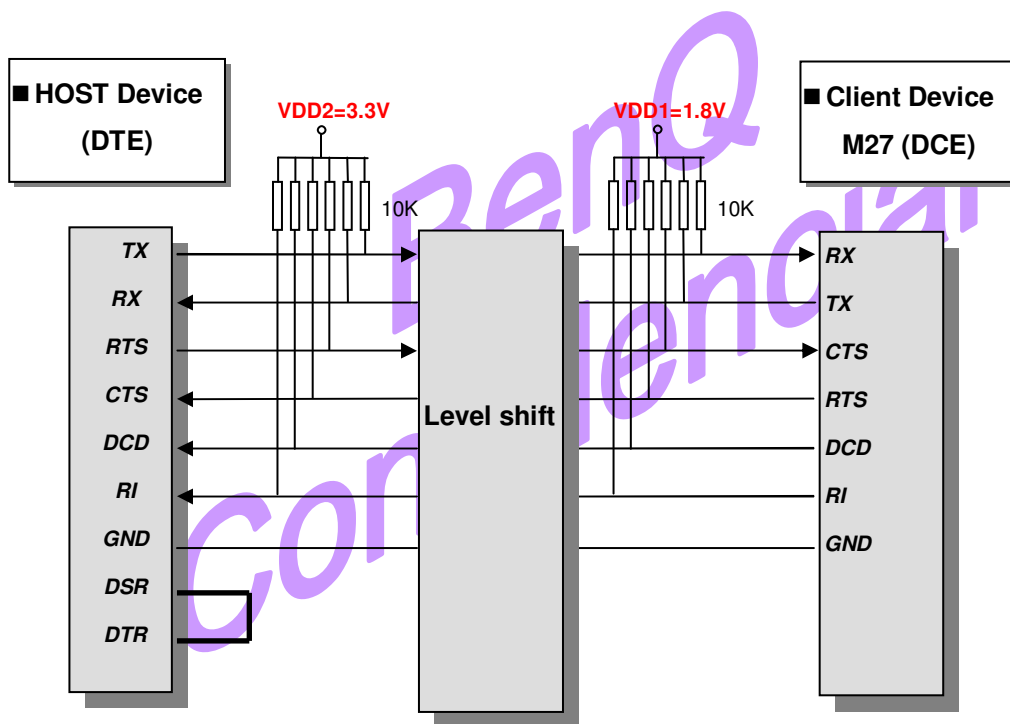
The UART includes the following additional features

- Hardware flow control (such as RTS/CTS) consists of two control signal lines between the Host (DTE) and Client (DCE) that are used to control the flow of data between the devices.
- Auto-baud rate with the possibility of baud-rates ranging from 1200 to 115.2K bits.

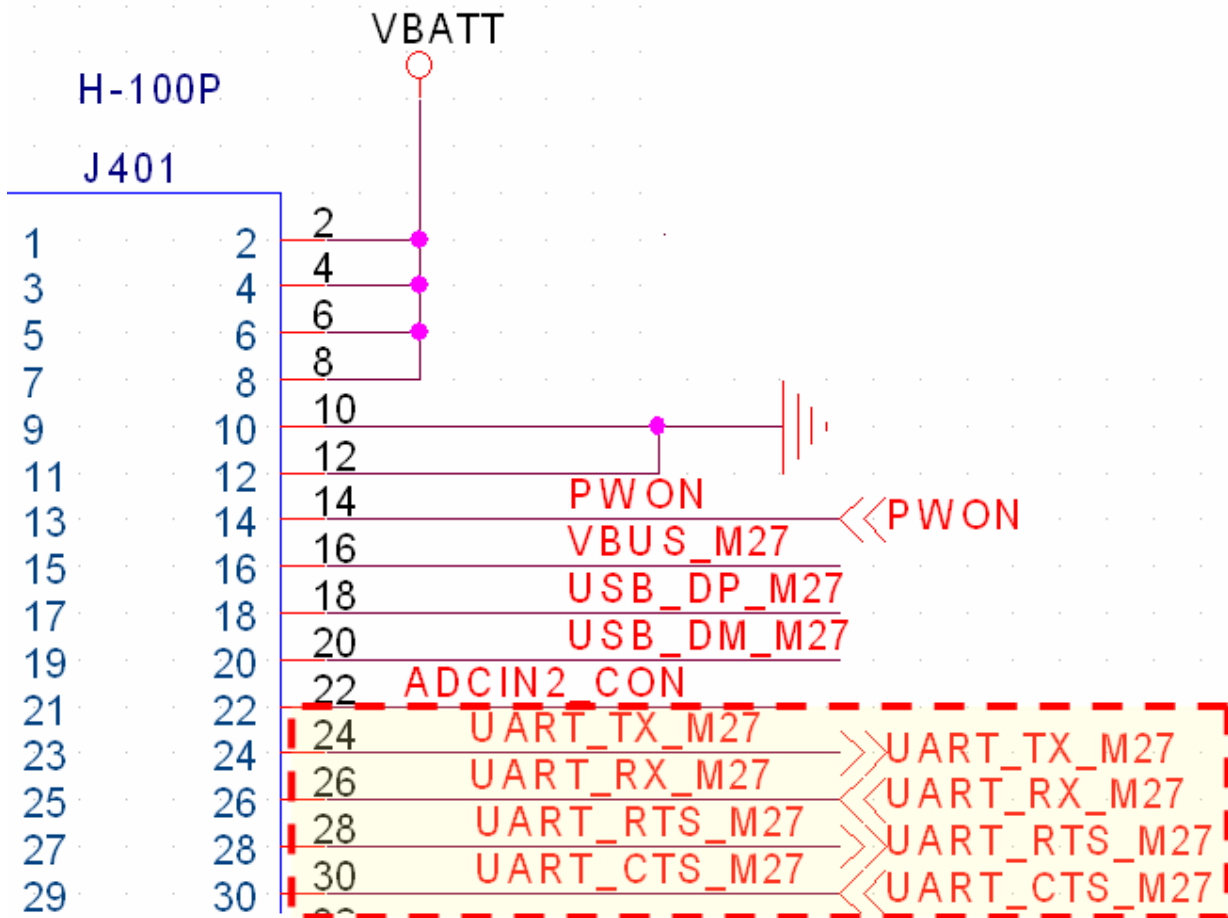
| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|------------|--------|--------------------------------|
| TX | 24 | | Output / 1 | | UART-Transmit Data(M27 side) |
| RX | 26 | PU | Input | | UART-Receive Data(M27 side) |
| RTS | 28 | | 1 | | UART-Request To Send(M27 side) |
| CTS | 30 | PD | Input | | UART-Clear To Send(M27 side) |

Note: The difference between Reset and Config in the pin definition table

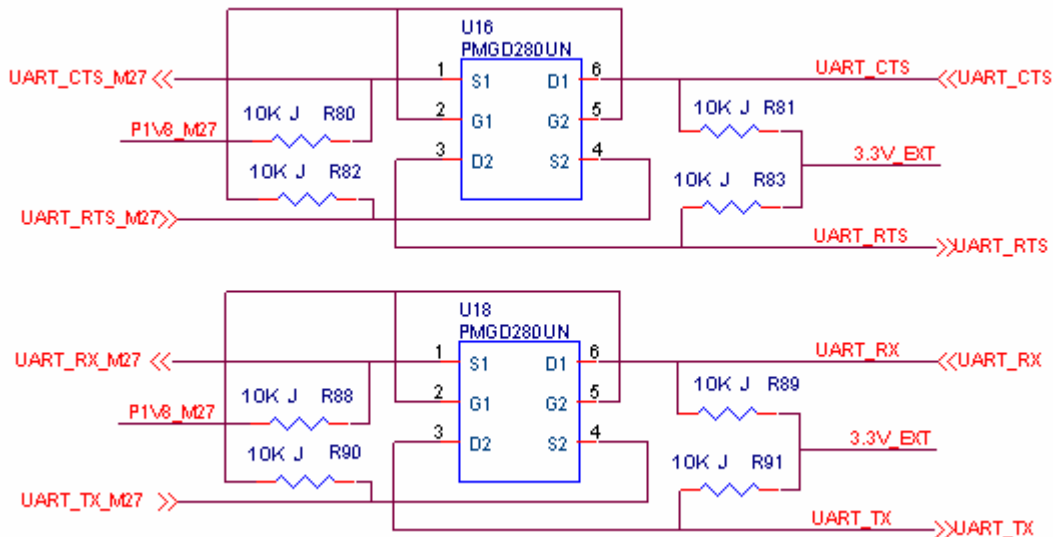
M27 only provide 1.8V UART interface. If the host (DTE) is 3.3V system, it needs additional Level shifter circuit on EVB.



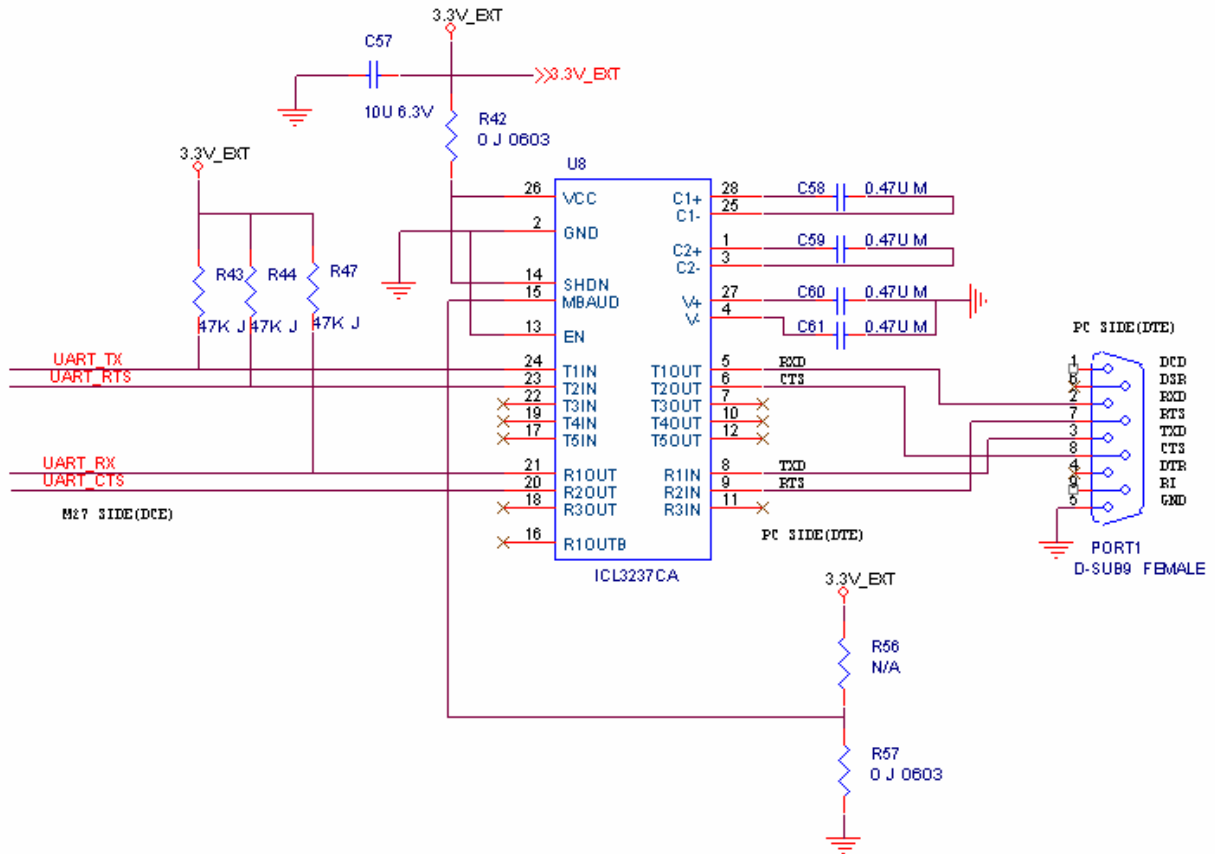
UART Interfaces



UART interface on M27



1.8V-3.3V level shifter for UART interface



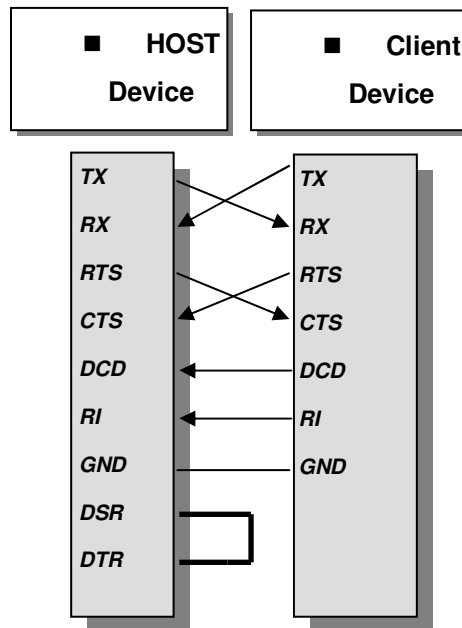
UART transceiver ICL3237A

■ **HW flow control**

When the hardware flow control type is recommended for communication between the Host(DTE) and client(DCE). Regarding the hardware flow control mechanism between the system (host side) and module (client side).

The GSM engine is designed for use as a DCE. Based on the conventions for DCE-DTE Connections it communicates with the customer application (DTE) using the following signals:

- ◆ Port/TX @ Host Device sends data to the module's /RX signal line
- ◆ Port/RX @ Host Device receives data from the module's /TX signal line
- ◆ Port/RTS @ Host Device sends data to the module's /CTS signal line
- ◆ Port/CTS @ Host Device receives data from the module's /RTS signal line



■ **Auto baud Rate Mechanism**

The M27 module UART is set at Auto-baud rate. This means when the M27 is powered on, it automatically detects the baud rate after the first AT command sent by the host Device. The baud rate is locked at the initially detected rate unless the following conditions:

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6.1 Dual external UART solution

M27 support 1 UART interface. M27 module support 4 bit address and 8 bit data bus with some associated control lines. The memory bus is Intel interface with 2 independent Read/Write control lines. For dual external UART port, there are 2 chips which are pin-to-pin compatible, except the ground plane. The one is the NXP SC16C852L, the other is EXAR XR16M2550. The function blocks and reference schematics are shown below. For single external UART solution, please refer to section 6.2.

Dual UART interface NXP SC16C852L

1.8 V dual UART, 5 Mbit/s (max.) with 128-byte FIFOs, parallel bus interface

Package →HVQFN32(5x5mm), LQFP48(9x9mm)

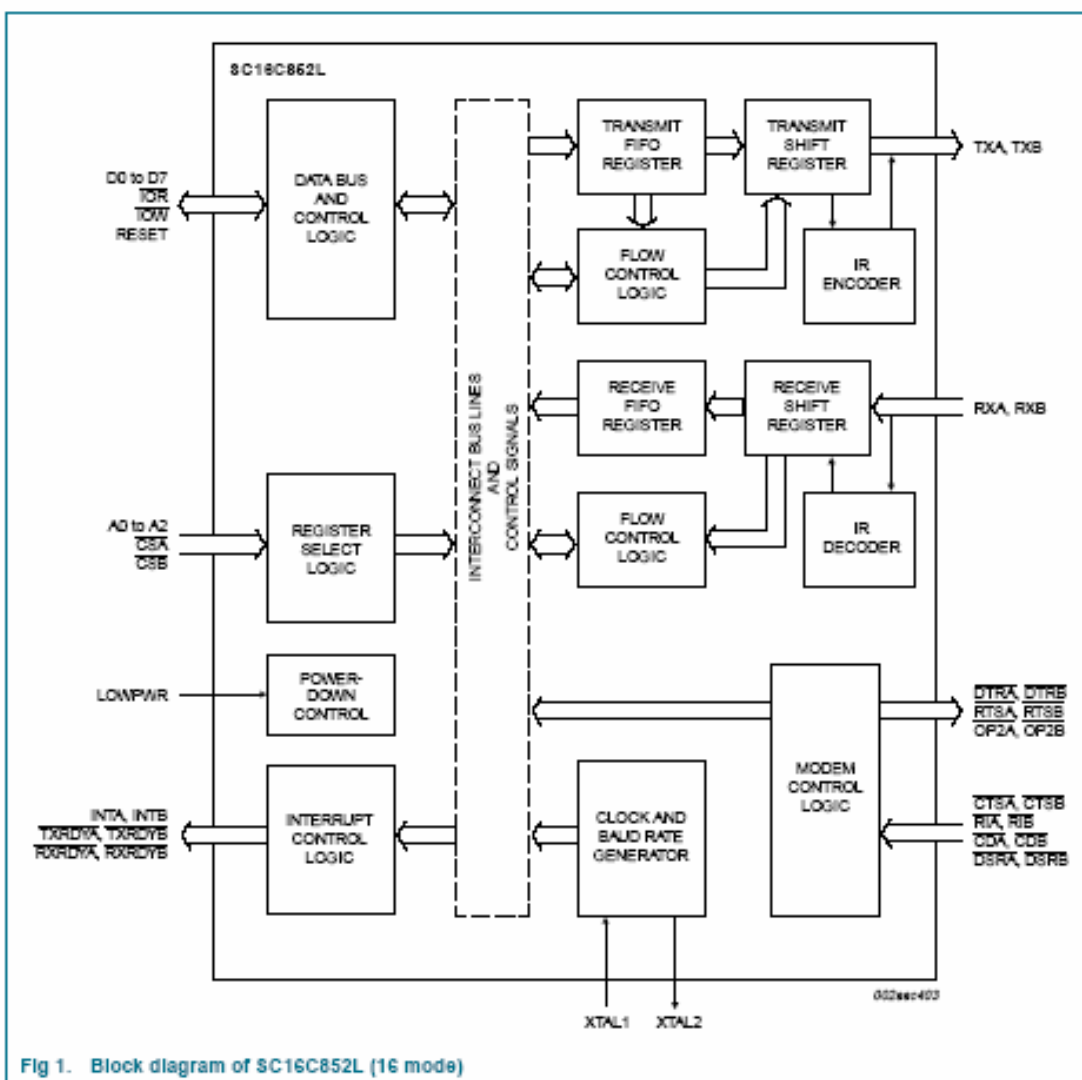


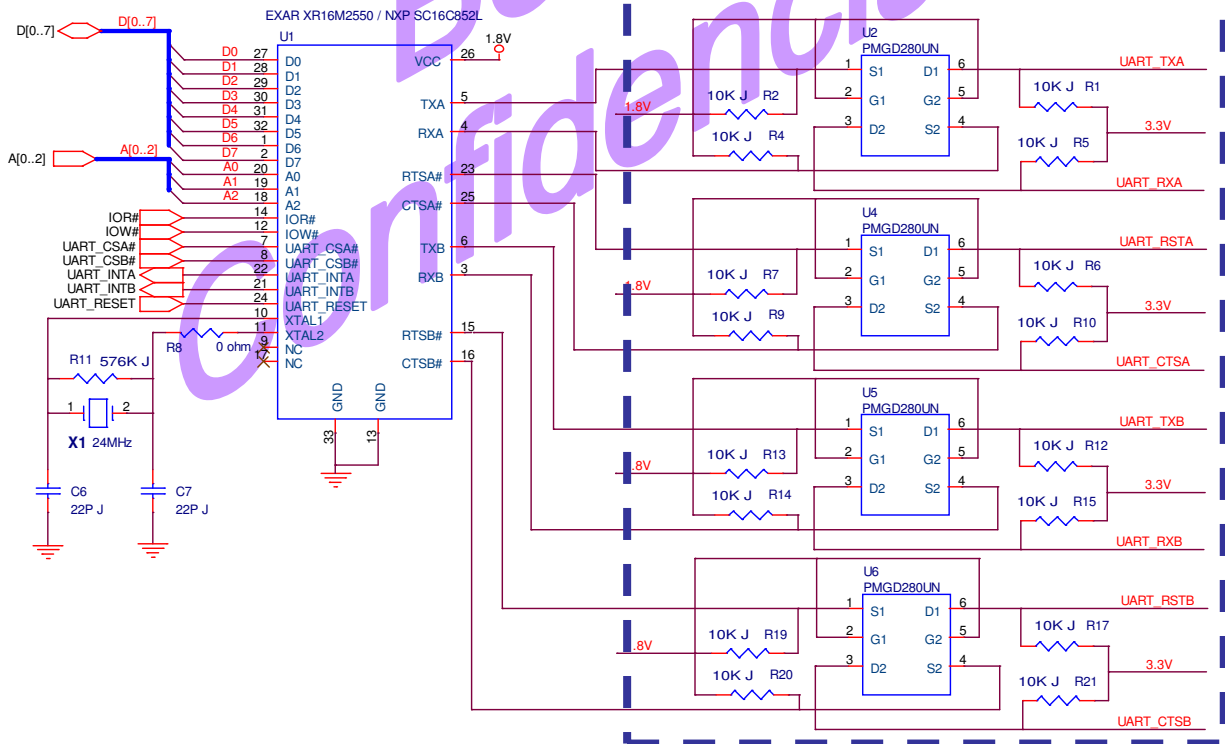
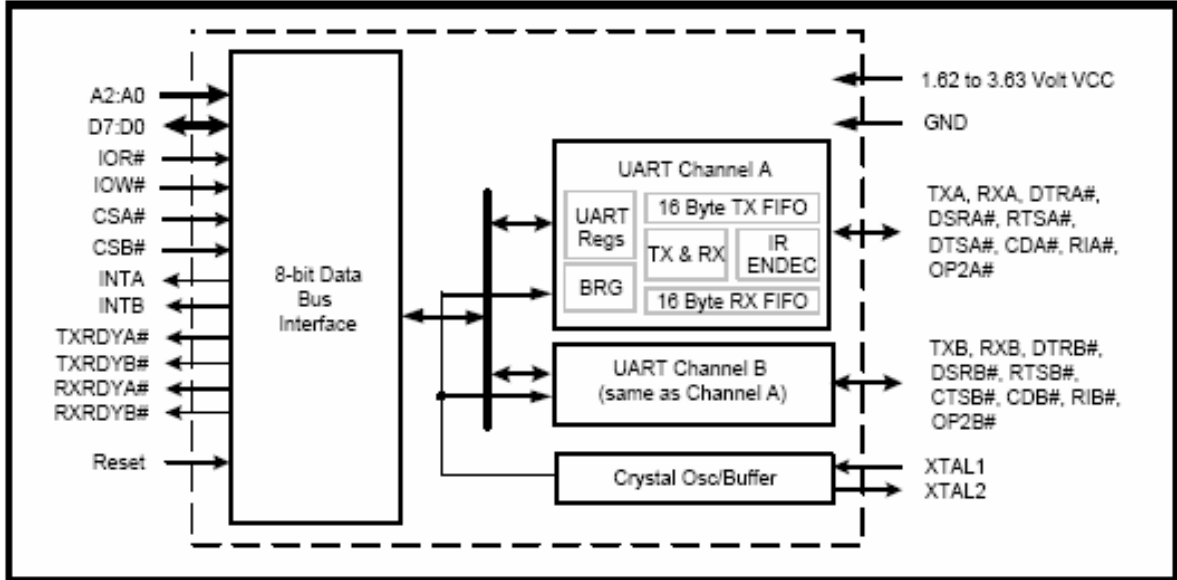
Fig 1. Block diagram of SC16C852L (16 mode)

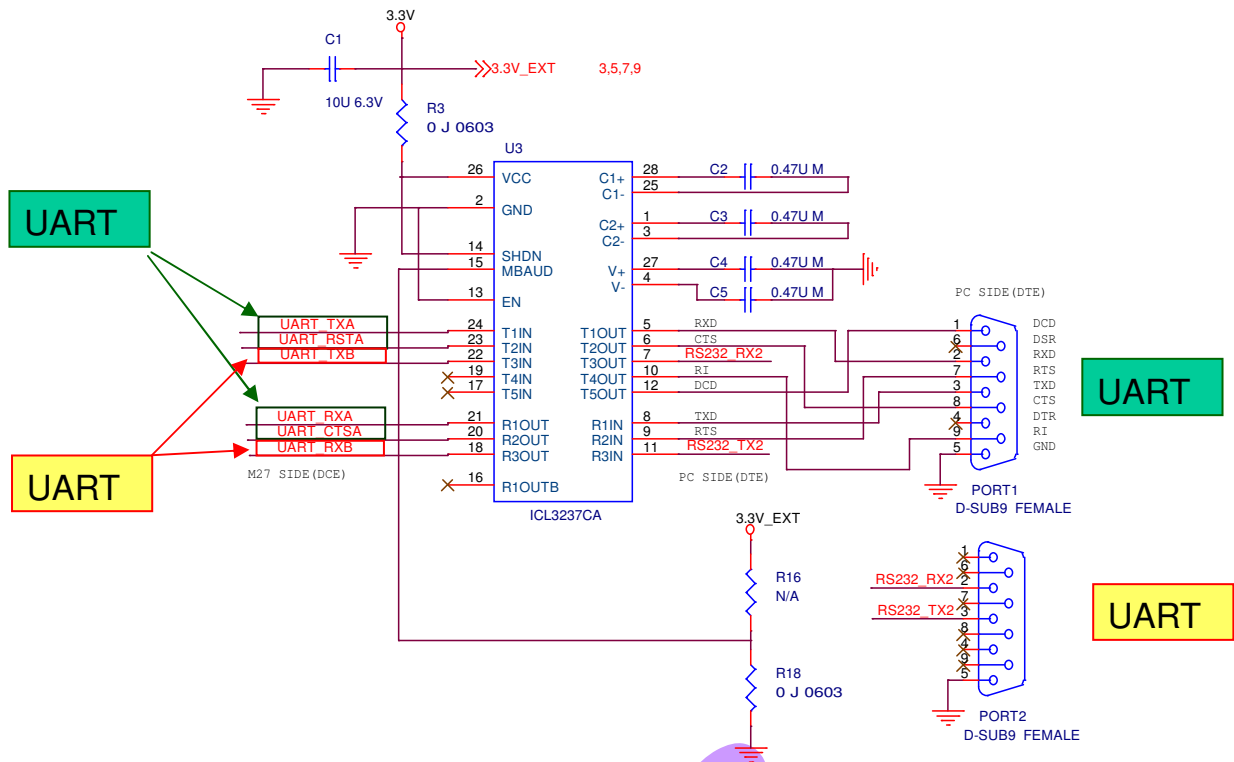
Dual UART interface EXAR XR16M2550

HIGH PERFORMANCE LOW VOLTAGE DUART WITH 16-BYTE FIFO

Package → 32 PIN QFN(5x5mm), 48 PIN TQFP (9x9mm)

FIGURE 1. XR16M2550 BLOCK DIAGRAM





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6.2 Single external UART solution

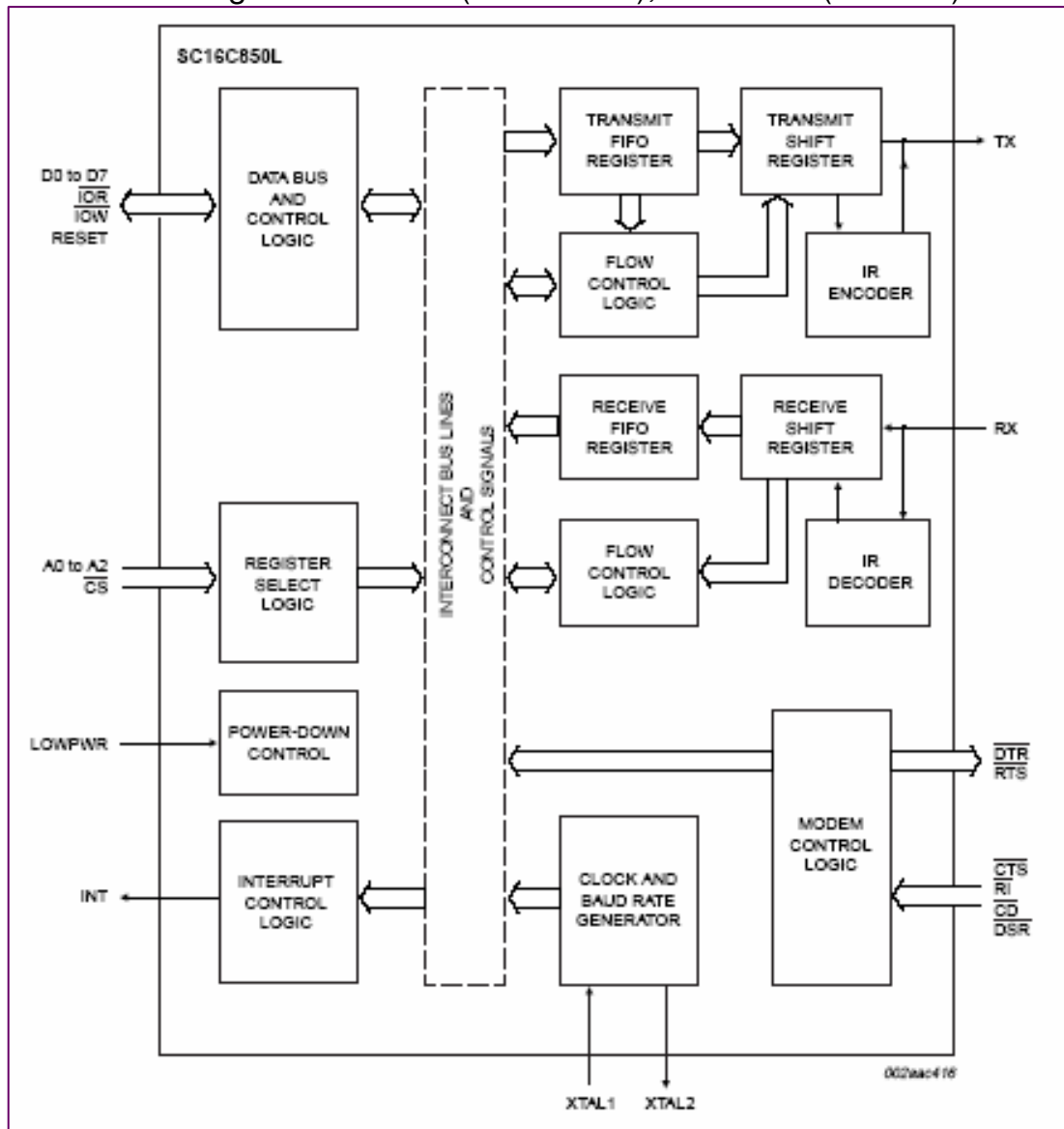
For single external UART solution, there are two options: the one is NXP SC16C850LIET, the other is EXAR XR16L570IL24. The function block and reference schematics are shown below:

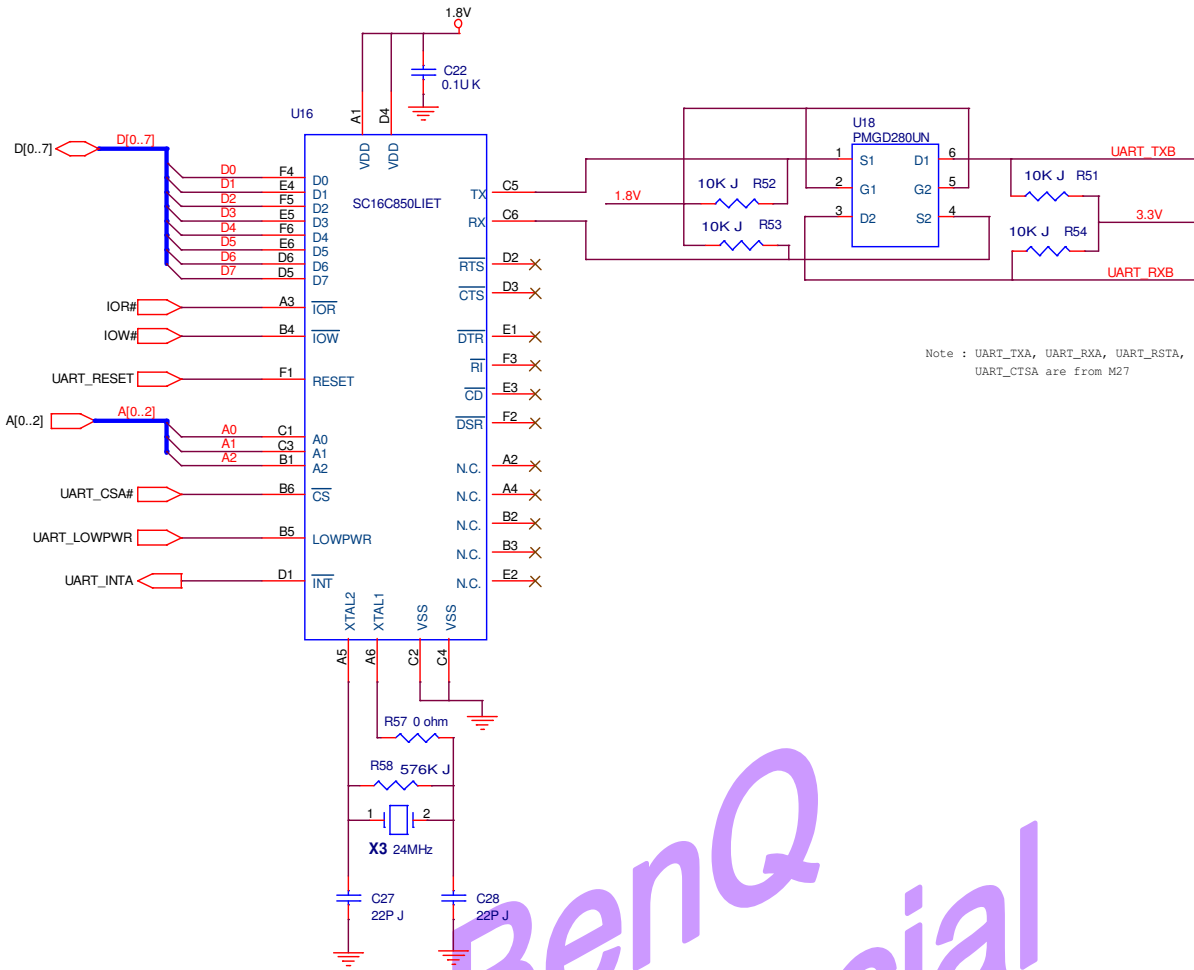
6.2.1 Single external UART solution: NXP SC16C850LIET

Single UART interface NXP SC16C850LIET

1.8 V single UART, 5 Mbit/s (max.) with 128-byte FIFOs parallel bus interface

Package → TFBGA36(3.5x3.5mm), HVQFN32(5x5mm)



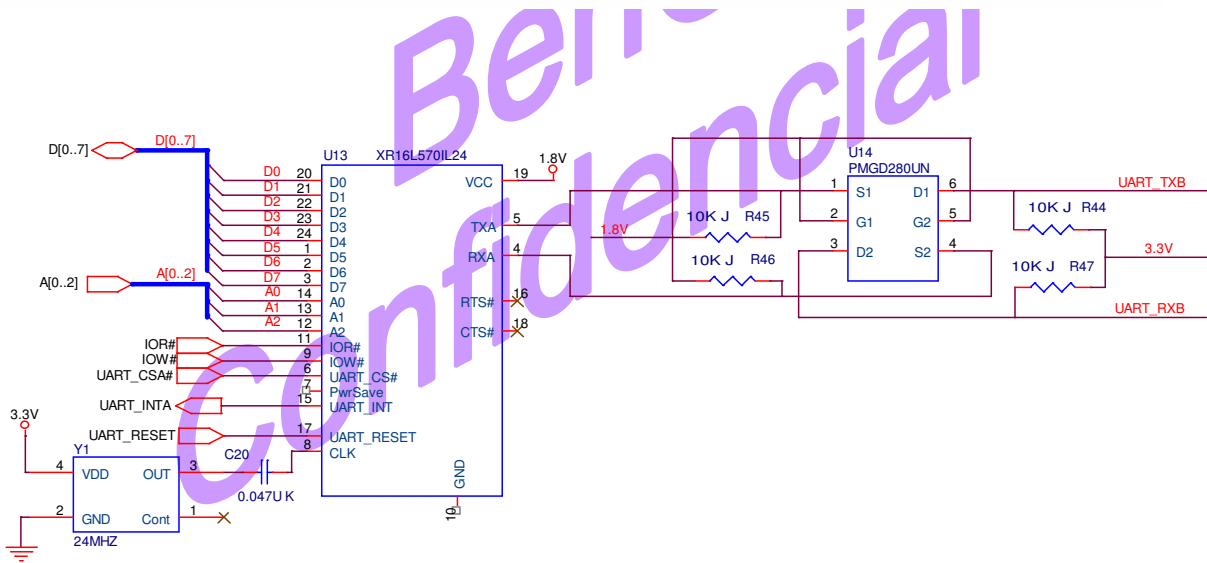
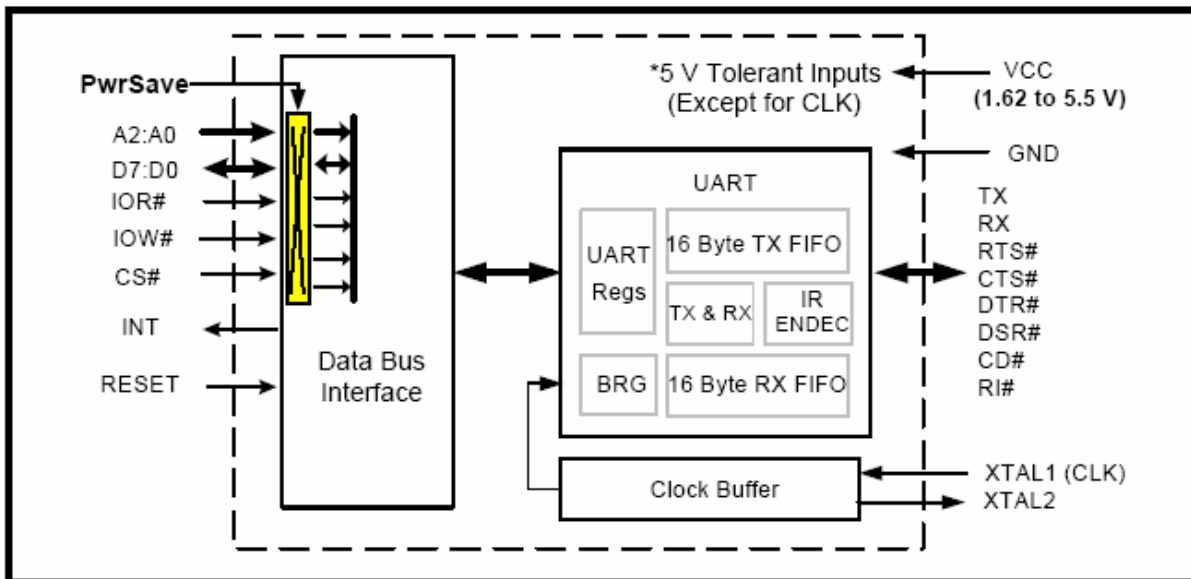


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6.2.2 Single external UART solution: EXAR XR16L570IL24

Single UART interface EXAR XR16L570IL24

SMALLEST 1.62V TO 5.5V UART WITH 16-BYTE FIFO AND POWERSAVE
 Package → 24 PIN QFN(4x4mm), 32 PIN QFN(5x5mm)



7 USB Interface

USB signals are transmitted on a twisted pair of data cables, labeled D+ and D-. These collectively use half-duplex differential signaling to combat the effects of electromagnetic noise on longer lines. D+ and D- usually operate together; They are not separate simplex connections. Transmitted signal levels are 0.0–0.3 volts for low and 2.8–3.6 volts for high.

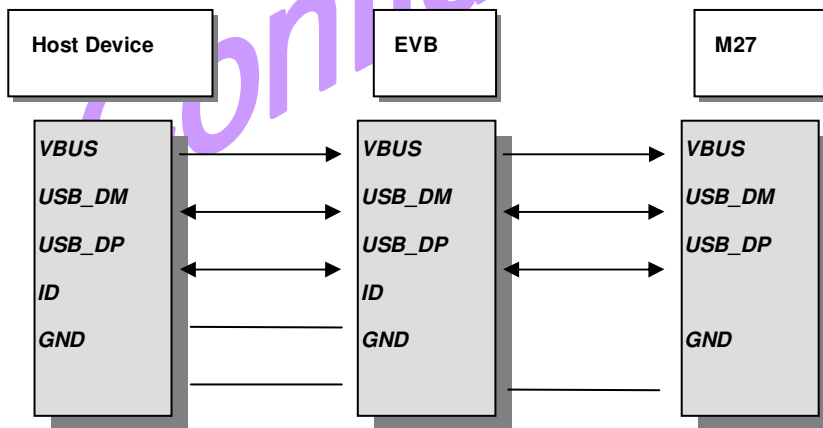
The USB supports three data rates

- **Low Speed** rate of 1.5 M bit/s (183 KiB/s).
- **Full Speed** rate of 12 M bit/s (1.5 MiB/s).

| USB connector pin out | | |
|-----------------------|-------------------------------|-------------------------------|
| Pin | Mini Function | M27 |
| 1 | V _{BUS} (4.4–5.25 V) | V _{BUS} (2.7–5.25 V) |
| 2 | D- | USB_DM |
| 3 | D+ | USB_DP |
| 4 | ID | |
| 5 | Ground | Ground |

| Pin Name | Pin Out | Pull | Reset | Config | Description |
|----------|---------|------|-------|--------|----------------------------------|
| VBUS | 16 | PD | | | Power Supply VBUS line |
| USB_DP | 18 | | | | USB data bus (positive terminal) |
| USB_DM | 20 | | | | USB data bus (negative terminal) |

Note: The difference between Reset and Config in the pin definition table



7.1 USB charger solution

For USB charger application, our suggestion is to use the Linear Technology LTC4067 as the Li-ion battery charger.

This chip manages the power supplies that would be typical for a USB powered device or from an adaptor to an intermediate voltage bus. The battery charger is a CC/CV timer terminated type capable of charge currents up to 1.25A. The adaptor input has over-voltage protection to 13V. An external MOSFET will disconnect the adaptor if the voltage exceeds 6V; protecting the input against damage in case an unregulated adaptor is accidentally plugged in.

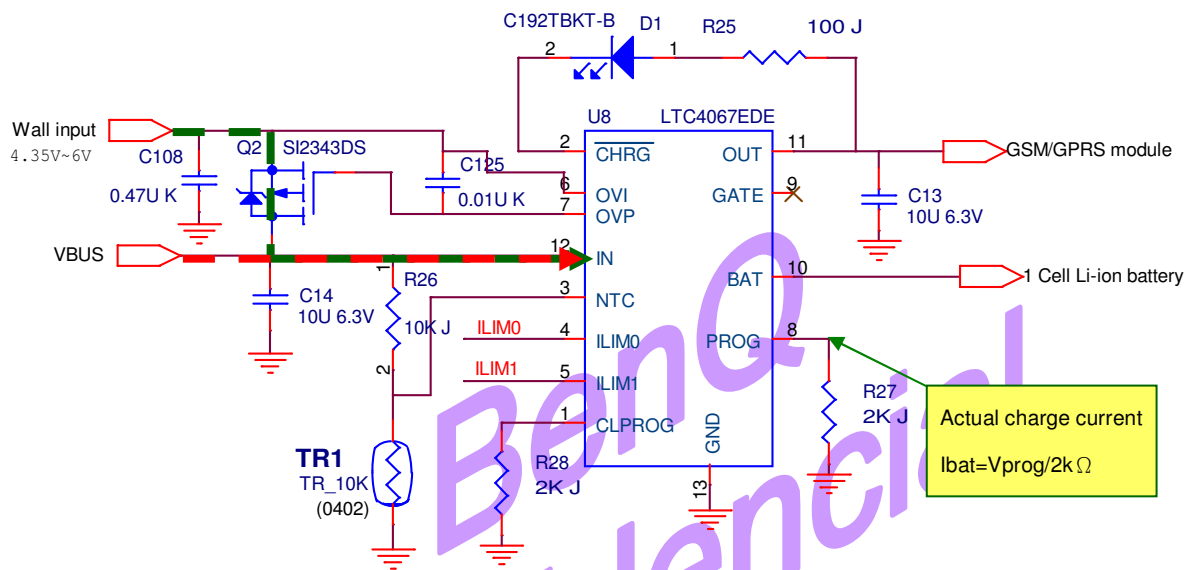
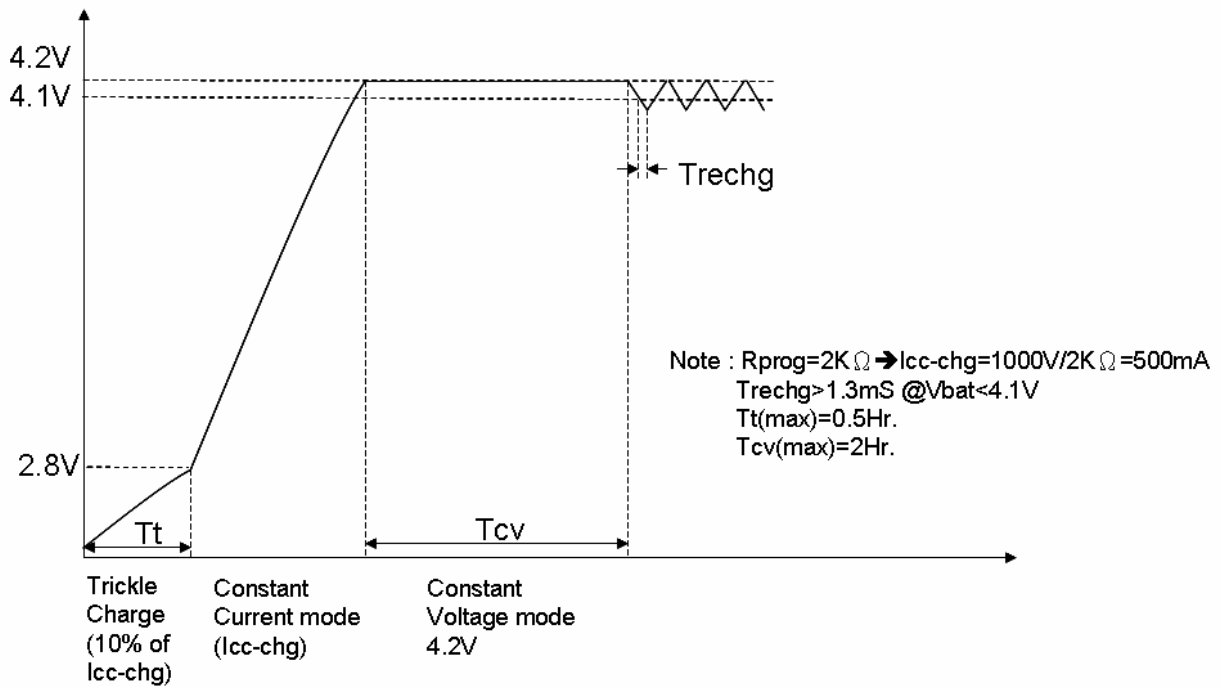


Table 1. I_{LIM} Programming

| I_{LIM0} | I_{LIM1} | I_{LIMIT} (A) | MODE |
|------------|------------|--------------------|-----------------------|
| L | H | 0 | SUSPEND |
| L | L | $200V/R_{CLPROG}$ | Low Power |
| H | H | $1000V/R_{CLPROG}$ | High Power |
| H | L | 2 | Current Limit Disable |

Note : I_{LIM0}, I_{LIM1} are 1.8V interface

Charging algorithm for LTC4067



8 GPIO MAPPING

The module provides 4 independent GPIO pins configurable in read or write mode. The function for these I/O pins is List below.

| Pin Name | Pin No | I/O | PU | Reset | Config | Description |
|----------|--------|-----|----|-------------|--------|------------------------|
| GPIO 1 | 87 | I/O | PU | Input Low | | General purpose I/O 1 |
| GPIO 10 | 60 | I/O | PU | Input Low | | General purpose I/O 10 |
| GPIO 14 | 34 | I/O | PD | Input Low | | General purpose I/O 14 |
| GPIO 37 | 32 | I/O | | Input Float | | General purpose I/O 37 |

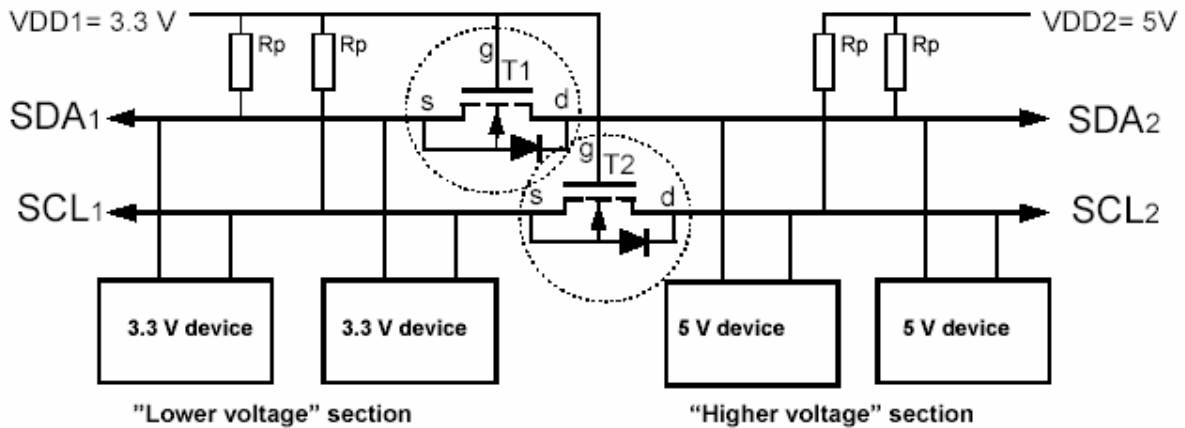
9 Level Shifter Design

9.1 Introduction

The bi-directional level shifter circuit described in this application note consists of one discrete MOS-FET for each bus line. In spite of its surprising simplicity, it not only fulfills the requirement of bi-directional level shifting without a direction control signal, but it also has the next additional features:

- Isolating of a powered-down bus section from the rest of the bus system,
- Protection of the "Lower voltage" side against high voltage spikes at the 'Higher voltage' side.

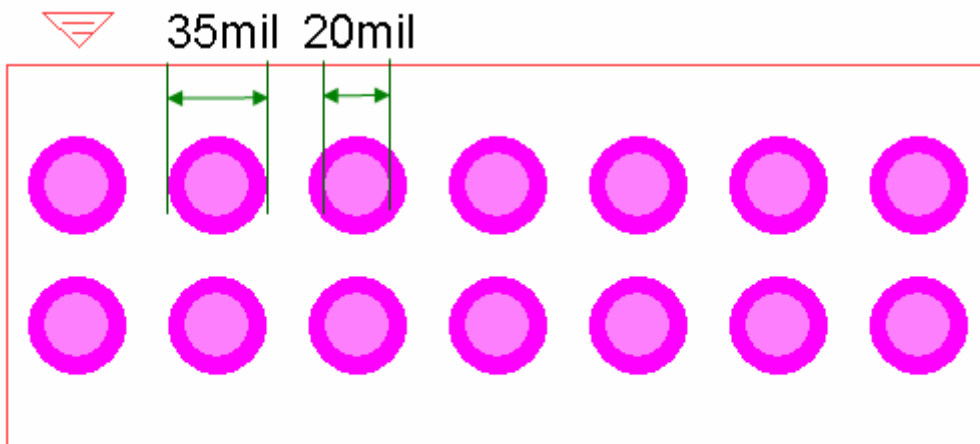
The bi-directional level shifter can be used in standard mode (0 to 100 kbit/s) or in fast mode (0 to 400 kbit/s) I2C-bus systems, without any change. The following descriptions apply for both modes.



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10. Layout notice

10.1 THT hole and pad size for 2x7 connector



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11. Antenna Interface

11.1 Antenna Installation & Consideration

M27 is capable of sustaining a total mismatch at the antenna pad without any damage, even when transmitting at maximum RF power. The RF interface has an impedance of 50Ω. M27 must be applied to 50 ohm load/ antenna, or else the output power will degrade seriously. Antenna supplier needs to ensure that the impedance of the operating frequency range is closed to 50Ω.

The external antenna must be matched properly to achieve best performance regarding radiated power, DC-power consumption, modulation accuracy and harmonic suppression. Antenna matching networks are not included on the M27 PCB and should be placed in the host application.

Due to the Antenna selection is more important for the wireless performance, this application will provide the Antenna requirements for mobile quad-band modules (GSM850, EGSM, DCS and PCS) (Table11.1~Table11.4).

Table11.1. Frequency Bands

| Item | Description | Requirement |
|------|---------------------|--|
| 1 | Transmit Bands (TX) | GSM850: 869 ~ 894 MHz EGSM: 880 ~ 915 MHz DCS: 1710 ~ 1785 MHz PCS: 1850 ~ 1910 MHz |
| 2 | Receive Bands (RX) | GSM850: 824 ~ 849 MHz EGSM: 925 ~ 960 MHz DCS: 1805 ~ 1880 MHz PCS: 1930 ~ 1990 MHz |

Table11.2. VSWR

| Item | Description | Requirement |
|------|-------------|---|
| 1 | VSWR | $\leq 2 : 1$ |
| 2 | Measurement | Network analyzer is used to measure VSWR, and the result must be measured with the matching circuit provided by Antenna vendor. |

Table11.3. Gain

| Item | Description | Requirement |
|------|--------------|--|
| 1 | Average gain | ≥ 0 dBi |
| 2 | Peak gain | ≥ 0.5 dBi The gain deviation (Peak gain – minimum gain) of all angles in H-plane should be less than 4dB in low, middle and high channels. The higher gain in DCS/PCS band would be preferred. |
| 3 | Measurement | The same as the Table11.2 item2. measure the radiation pattern at the lowest, middle and highest frequency for each band. And it must be measured in Chamber, including XY, XZ and YZ planes. |

Table11.4. Power Rating

| Item | Description | Requirement |
|------|------------------|--|
| 1 | .Maximum Value: | 2W(CW) |
| 2 | Measuring Method | A 50 Ω coaxial cable is connected to the 50 Ω feeding point on the PCB. The power is applied for 10 minutes at the middle frequency of each Tx band. After the test then measure the VSWR. |
| 3 | Criteria | The antenna shall satisfy the VSWR as described in Table11.2. No visual deterioration shall occur during or after the test. |

11.2 Antenna Pad & Cable Soldering

The antenna can be soldered to the antenna pad. For proper grounding connect the antenna to the ground plane on the bottom of M27 which must be connected to the ground plane of the application.(Fig.11.1)

Notes on soldering:

- To prevent damage to the module and to obtain long-term solder joint properties you are advised to maintain the standards of good engineering practice for soldering.
- Be sure to solder the antenna core to the pad and the shielding of the coax cable to the ground plane of the module next to the antenna pad. The direction of the cable is not relevant from the electrical point of view.

M27 material properties:

- M27 PCB: FR4
- Antenna pad: Gold plated pad

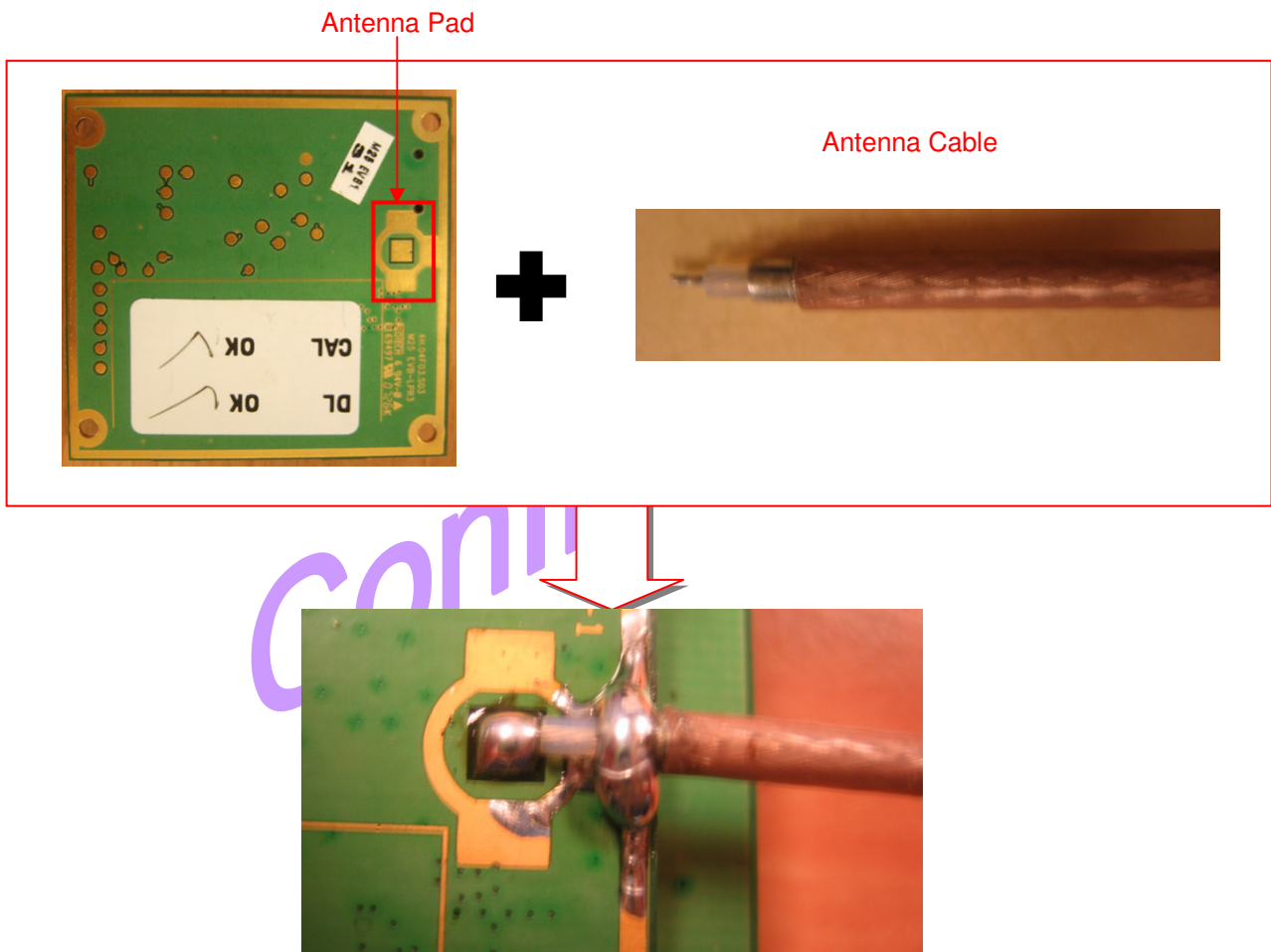


Fig.11.1 Antenna Pad & Cable Soldering

FCC ID: VRSM27

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- 1.this device may not cause harmful interference, and
- 2.this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Maximum antenna gain allowed for use with this device is 0dBi.

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following test:

“Contains FCC ID: VRSM27” .

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