Build a Smarter World

EC21 Hardware Design

LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2016-04-15	Yeoman CHEN	Initial
1.1	2016-09-22	Yeoman CHEN/ Frank WANG/ Lyndon LIU	1. Updated frequency bands in Table 1. 2. Updated transmitting power, supported maximum baud rate of main UART, supported internet protocols, supported USB drivers of USB interface, and temperature range in Table 2. 3. Updated timing of turning on module in Figure 12. 4. Updated timing of turning off module in Figure 13. 5. Updated timing of resetting module in Figure 16. 6. Updated main UART supports baud rate in Chapter 3.11. 7. Added notes for ADC interface in Chapter 3.13. 8. Updated GNSS Performance in Table 21. 9. Updated operating frequencies of module in Table 23. 10. Added current consumption in Chapter 6.4. 11. Updated RF output power in Chapter 6.5. 12. Added RF receiving sensitivity in Chapter 6.6.
1.3	2017-01-24	Lyndon LIU/ Rex WANG	1. Updated frequency bands in Table 1. 2. Updated function diagram in Figure 1. 3. Updated pin assignment (top view) in Figure 2. 4. Added BT interface in Chapter 3.18.2. 5. Updated reference circuit of wireless connectivity interfaces with FC20 module in Figure 29. 6. Updated GNSS performance in Table 24. 7. Updated module operating frequencies in Table 26. 8. Added EC21-AUV current consumption in Table 38. 9. Updated EC21-A conducted RF receiving sensitivity of in Table 42. 10. Added EC21-J conducted RF receiving sensitivity in

			Table 48.
1.4	2017-03-01	Geely YANG	Deleted the LTE band TDD B41 of EC21-CT
1.5	2018-03-05	Annice ZHANG/ Lyndon LIU/ Frank WANG	1. Updated functional diagram in Figure 1. 2. Updated frequency bands in Table 1. 3. Updated UMTS and GSM features in Table 2. 4. Updated description of pin 40/136/137/138. 5. Updated PWRKEY pulled down time to 500ms in chapter 3.7.1 and reference circuit in Figure 10. 6. Updated reference circuit of (U)SIM interface in Figure 17&18. 7. Updated reference circuit of USB interface in Figure 19. 8. Updated PCM mode in Chapter 3.12. 9. Updated USB_BOOT reference circuit in Chapter 3.20. 10. Added SD card interface in Chapter 3.13. 11. Updated module operating frequencies in Table 26. 12. Updated EC21 series modules current consumption in Chapter 6.5. 13. Updated EC21 series modules conducted RF receiving sensitivity in Chapter 6.6. 14. Added thermal consideration description in Chapter 6.8. 15. Updated dimension tolerance information in Chapter 7. 16. Added storage temperature range in Table 2 and Chapter 6.3. 17. Updated RF output power in Table 42. 18. Updated antenna requirements in Table 29. 19. Updated GPRS multi-slot classes in Table 55. 20. Updated storage information in Chapter 8.1

Contents

Table Index

Figure Index

1 Introduction

This document defines the EC21 module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC21 module. Associated with application note and user guide, customers can use EC21 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC21 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for the customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals,clinics or other health care facilities. These requests are desinged to prevent possible interference with sensitive medical equipment.
	Cellular terminals or mobiles operating over radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid (U)SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

EC21 is a series of LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication module with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides GNSS[1)] and voice functionality[2)] for customers' specific applications. EC21 contains nine variants: EC21-E, EC21-A, EC21-V, EC21-AU, EC21-AUT, EC21-AUV, EC21-J, EC21-KL and EC20-CEL. Customers can choose a dedicated type based on the region or operator. The following table shows the frequency bands of EC21 series module.

Table 1: Frequency Bands of EC21 Series Module

Modules[2)]	LTE Bands	UMTS Bands	GSM	Rx-diversity	GNSS[1)]
EC21-E	FDD: B1/B3/B5/B7/B8/B20	WCDMA: B1/B5/B8	900/1800	Y	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS
EC21-A	FDD: B2/B4/B12	WCDMA: B2/B4/B5	N	Y	
EC21-V	FDD: B4/B13	N	N	Y	
EC21-AU[3)]	FDD: B1/B2/B3/B4/B5/B7/B8/ B28 TDD: B40	WCDMA: B1/B2/B5/B8	850/900/ 1800/1900	Y	
EC21-AUT	FDD: B1/B3/B5/B7/B28	WCDMA: B1/B5	N	Y	
EC21-AUV	FDD: B1/B3/B5/B8/B28	B1/B5/B8	N	Y	N
EC21-J	FDD: B1/B3/B8/B18/B19/B26	N	N	Y	N
EC21-KL	FDD: B1/B3/B5/B7/B8	N	N	Y	N
EC20-CEL	FDD: B1/B3/B5	N	N	N	N

NOTES

1. [1)] GNSS function is optional.
2. [2)] EC21 series module (EC21-E, EC21-A, EC21-V, EC21-AU, EC21-AUT, EC21-AUV, EC21-J, EC21-KL and EC20-CEL) contains **Telematics** version and **Data-only** version. **Telematics** version supports voice and data functions, while **Data-only** version only supports data function.
3. [3)] B2 band on EC21-AU module does not support Rx-diversity.
4. Y = Supported. N = Not supported.

With a compact profile of 29.0mm × 32.0mm × 2.4mm, EC21 can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC21 is an SMD type module which can be embedded into applications through its 144-pin pads, including 80 LCC signal pads and 64 other pads.

2.2. Key Features

The following table describes the detailed features of EC21 module.

Table 2: Key Features of EC21 Module

Features	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 1 FDD and TDD Support 1.4MHz~20MHz RF bandwidth Support MIMO in DL direction LTE-FDD: Max 10Mbps (DL)/5Mbps (UL)

	LTE-TDD: Max 8.96Mbps (DL)/3.1Mbps (UL)
UMTS Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max 42Mbps (DL) HSUPA: Max 5.76Mbps (UL) WCDMA: Max 384Kbps (DL)/384Kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL)/85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL)/ 236.8Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/ CMUX*/HTTPS*/ SMTP*/ MMS*/FTPS*/SMTPS*/SSL*/FILE* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 8-bit A-law*, μ-law* and 16-bit linear data formats Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging, firmware upgrade and voice over USB* Support USB serial drivers for: Windows XP, Windows Vista, Windows

	7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1, Android 4.x/5.x/6.x/7.x
UART Interface	**Main UART:** Used for AT command communication and data transmission Baud rates reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console and log output 115200bps baud rate
SD Card Interface	Support SD 3.0 protocol
SGMII Interface	Support 10/100/1000Mbps Ethernet connectivity
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interface	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (29.0±0.15)mm × (32.0±0.15)mm × (2.4±0.2)mm Weight: approx. 4.9g
Temperature Range	Operation temperature range: -35°C ~ +75°C[1)] Extended temperature range: -40°C ~ +85°C[2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EC21 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

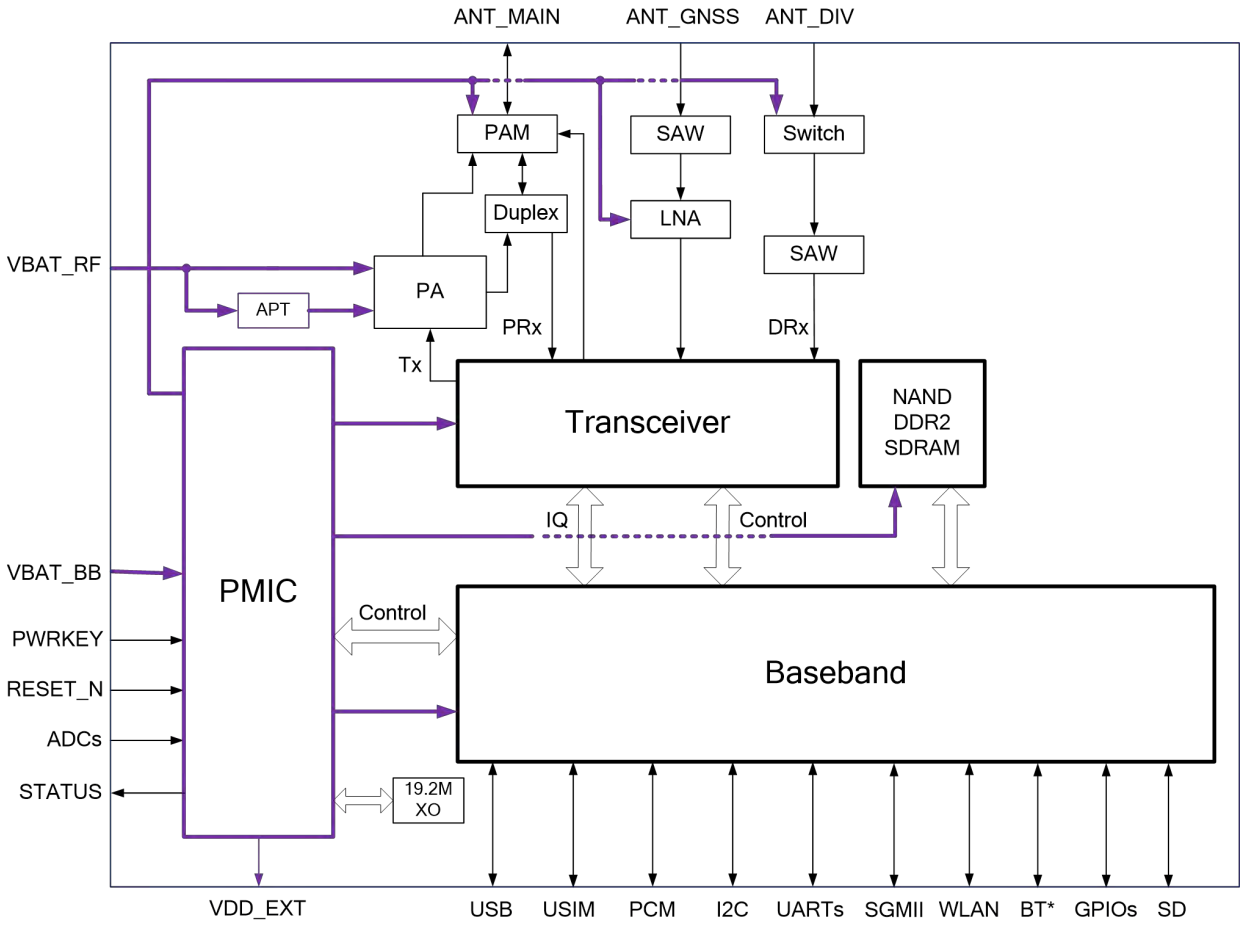


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications with EC21, Quectel supplies an evaluation board (EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

EC21 is equipped with 80 LCC pads plus 64 LGA pads that can be connected to cellular application platform. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- ADC interfaces
- Status indication
- SGMII interface
- Wireless connectivity interfaces
- USB_BOOT interface

3.2. Pin Description

The following tables show the pin definition of EC21 module.

Table 3: I/O Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a burst transmission.
VDD_EXT	7	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46,		Ground		

	48, 50~54, 56, 72, 85~112				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	20	DI	Reset signal of the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module operating status	The drive current should be less than 0.9mA.	Require external pull-up. If unused, keep it open.
NET_MODE	5	DO	Indicate the module network registration mode	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. It cannot be pulled up before startup. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	PI	USB detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	Typical: 5.0V If unused, keep it open.
USB_DP	69	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω. If unused, keep it open.
USB_DM	70	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω. If unused, keep it open.

(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM card		
USIM_VDD	14	PO	Power supply for (U)SIM card	For 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V For 3.0V (U)SIM: Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	For 1.8V (U)SIM: V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V (U)SIM: V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	16	DO	Clock signal of (U)SIM card	For 1.8V (U)SIM: V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V (U)SIM: V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_RST	17	DO	Reset signal of (U)SIM card	For 1.8V (U)SIM: V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V (U)SIM: V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	62	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DCD	63	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
CTS	64	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RTS	65	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DTR	66	DI	Data terminal ready, sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.
TXD	67	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RXD	68	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	11	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC0	45	AI	General purpose analog to digital converter	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC1	44	AI	General purpose analog to digital converter	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock. Used for external codec		External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data. Used for external codec		External pull-up resistor is required. 1.8V only. If unused, keep it

					open.

SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_ DATA3	28	IO	SD card SDIO bus DATA3	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_ DATA2	29	IO	SD card SDIO bus DATA2	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_ DATA1	30	IO	SD card SDIO bus DATA1	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:**	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.

				V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	
SDC2_ DATA0	31	IO	SD card SDIO bus DATA0	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_CLK	32	DO	SD card SDIO bus clock	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_CMD	33	IO	SD card SDIO bus command	**1.8V signaling:** V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}min=-0.3V V_{IL}max=0.58V V_{IH}min=1.27V V_{IH}max=2.0V **3.0V signaling:** V_{OL}max=0.38V V_{OH}min=2.01V V_{IL}min=-0.3V V_{IL}max=0.76V V_{IH}min=1.72V V_{IH}max=3.34V	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.

SD_INS_DET	23	DI	SD card insertion detect	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
VDD_SDIO	34	PO	SD card SDIO bus pull-up power	$I_O$max=50mA	1.8V/2.85V configurable. Cannot be used for SD card power. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EPHY_RST_N	119	DO	Ethernet PHY reset	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}max=0.58V V_{IH}min=1.27V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V V_{IL}max=0.71V V_{IH}min=1.78V	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.

USIM2_VDD	128	PO	SGMII MDIO pull-up power source		Configurable power source. 1.8V/2.85V power domain. External pull-up for SGMII MDIO pins. If unused, keep it open.
SGMII_TX_M	123	AO	SGMII transmission - minus		If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmission - plus		If unused, keep it open.
SGMII_RX_P	125	AI	SGMII receiving - plus		If unused, keep it open.
SGMII_RX_M	126	AI	SGMII receiving - minus		If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna pad		50Ω impedance If unused, keep it open.
ANT_MAIN	49	IO	Main antenna pad		50Ω impedance
ANT_GNSS	47	AI	GNSS antenna pad		50Ω impedance If unused, keep it open.
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Cannot be pulled up before startup. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. At low voltage level, module can enter into airplane mode. If unused, keep it

					open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to enter into emergency download mode.	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Active high. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 18, 23, 43, 55, 73~84, 113, 114, 116, 117, 140-144.		Reserved		Keep these pins unconnected.

NOTES

1. "*" means under development.
2. Pads 24~27 are multiplexing pins used for audio design on EC21 module and BT function on FC20 module.

3.3. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.

Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Airplane Mode	**AT+CFUN** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

3.4. Power Saving

3.4.1. Sleep Mode

EC21 is able to reduce its current consumption to a minimum value during the sleep mode. The following section describes power saving procedures of EC21 module.

3.4.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

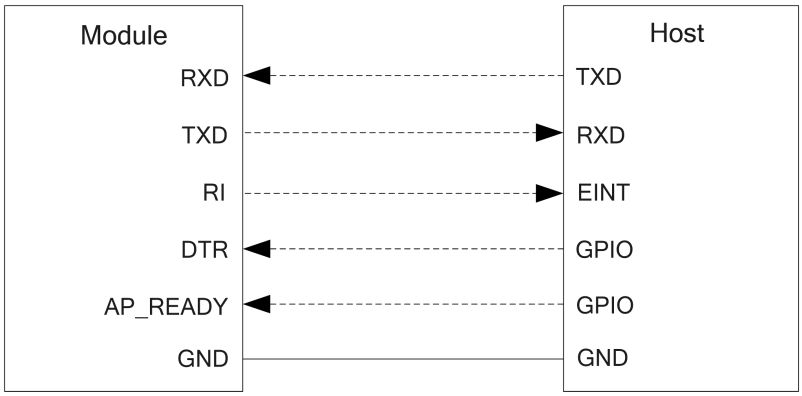


Figure 3: Sleep Mode Application via UART

- Driving the host DTR to low level will wake up the module.
- When EC21 has a URC to report, RI signal will wake up the host. Refer to ***Chapter 3.17*** for details about RI behaviors.
- AP_READY will detect the sleep state of the host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"*** command for details.

NOTE

"*" means under development.

3.4.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

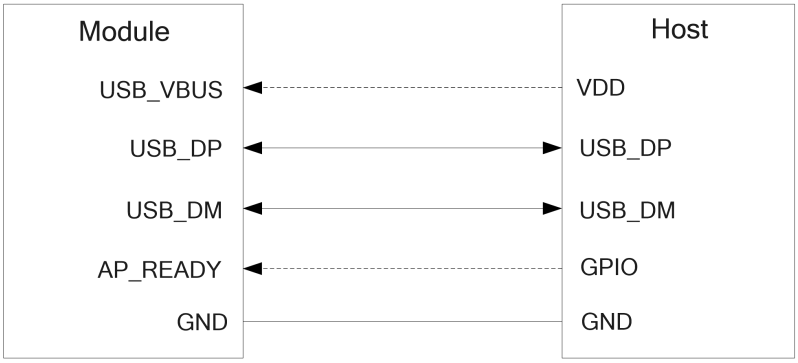


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC21 through USB will wake up the module.
- When EC21 has a URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.4.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter into the sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

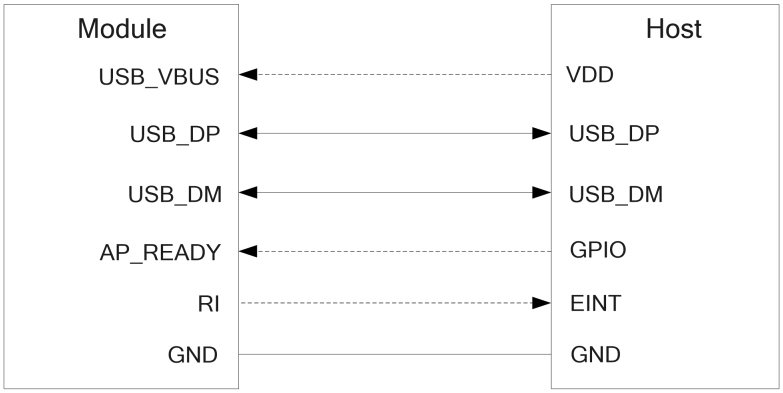


Figure 5: Sleep Mode Application with RI

- Sending data to EC21 through USB will wake up the module.
- When EC21 has a URC to report, RI signal will wake up the host.

3.4.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected via an additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

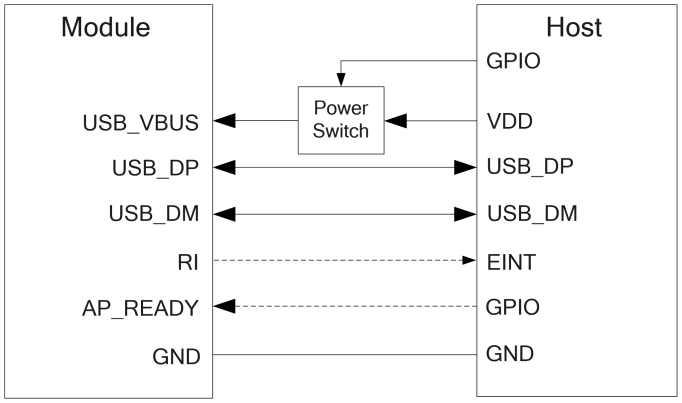


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Refer to ***document [1]*** for more details about EC21 power management application.

3.4.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUN command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTES

1. W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command. This command is under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.5. Power Supply

3.5.1. Power Supply Pins

EC21 provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part.	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part.	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	Ground	-	0	-	V

3.5.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

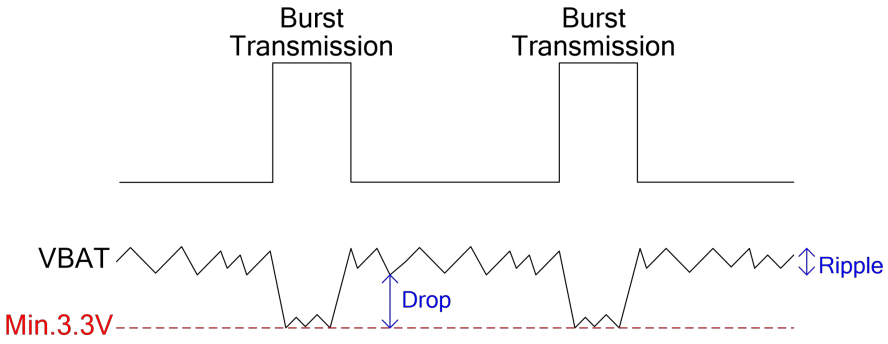


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm; and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested that a zener diode whose reverse zener voltage is 5.1V and dissipation power is more than 0.5W should be used. The following figure shows the star structure of the power supply.

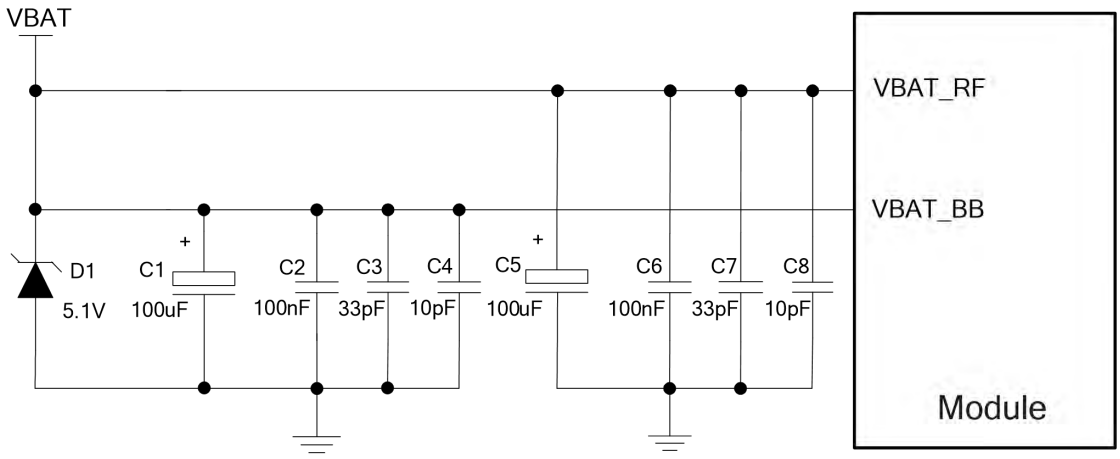


Figure 8: Star Structure of the Power Supply

3.5.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3A.

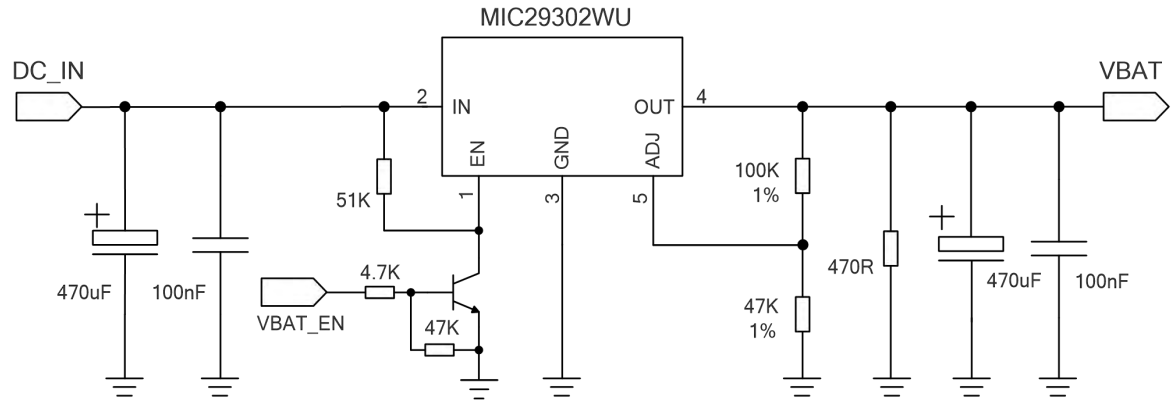


Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.

3.5.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.6. Turn on and off Scenarios

3.6.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EC21 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

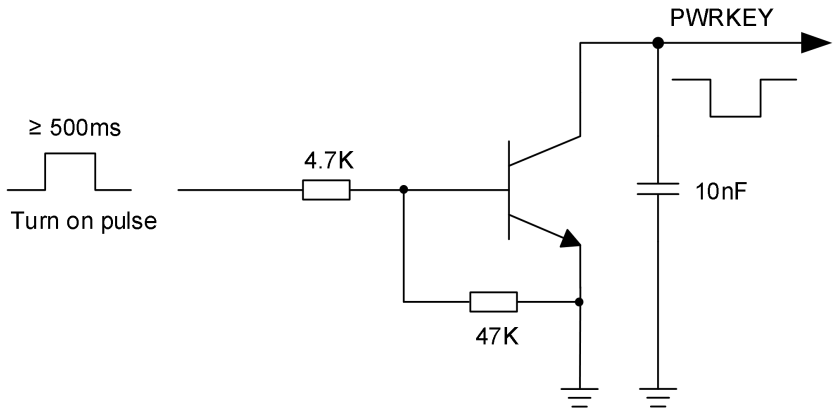


Figure 10: Turn on the Module by Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

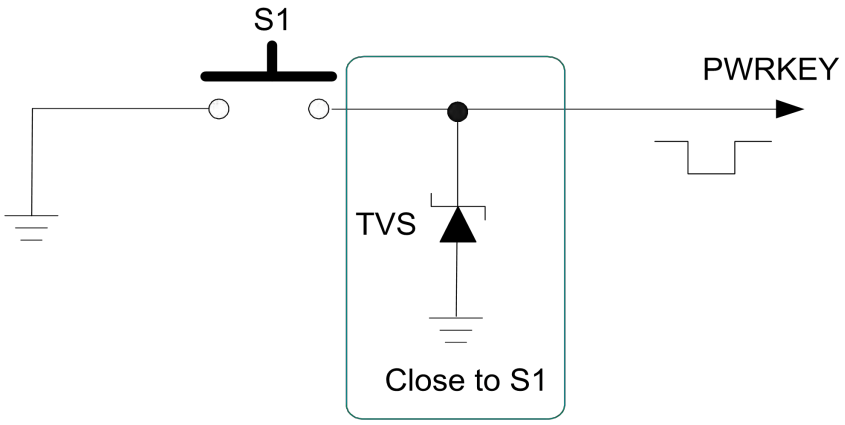


Figure 11: Turn on the Module by Using Button

The turn on scenario is illustrated in the following figure.

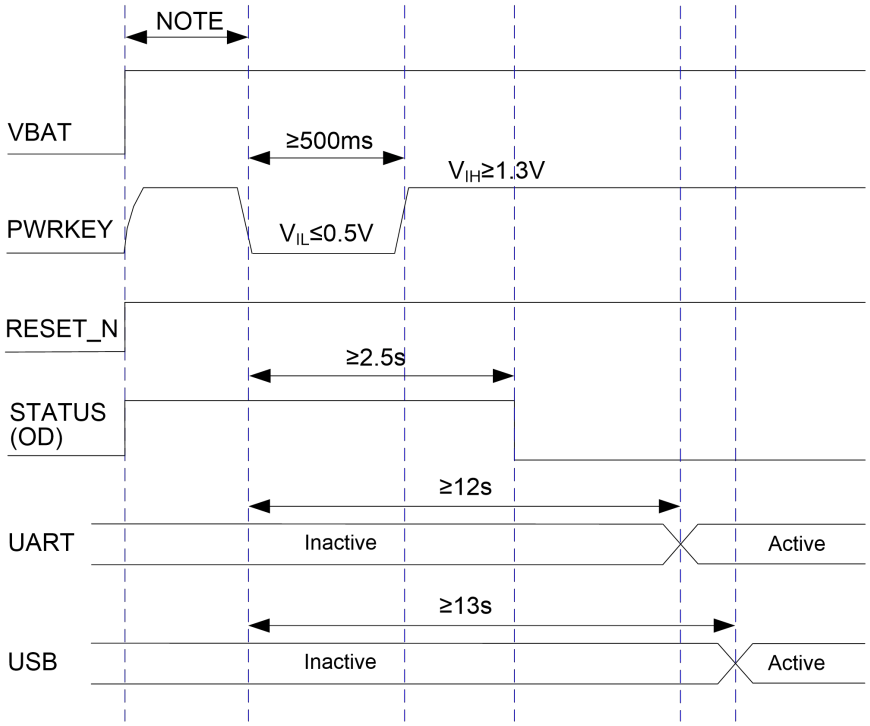


Figure 12: Timing of Turning on Module

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.6.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD** command.

3.6.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

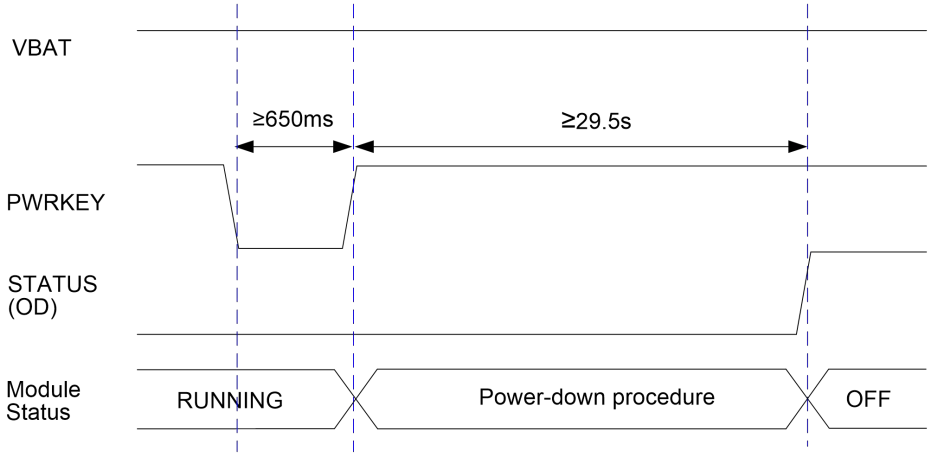


Figure 13: Timing of Turning off Module

3.6.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turn off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise the module will be turned on again after successfully turn-off.

3.7. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for time between 150ms and 460ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment

RESET_N	20	DI	Reset the module	1.8V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

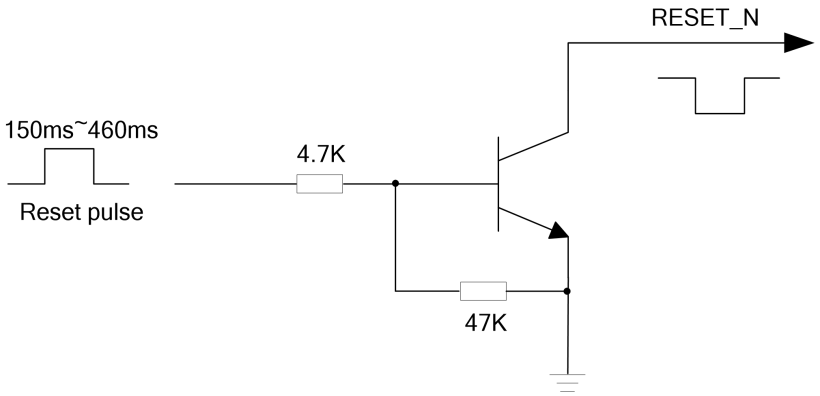


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

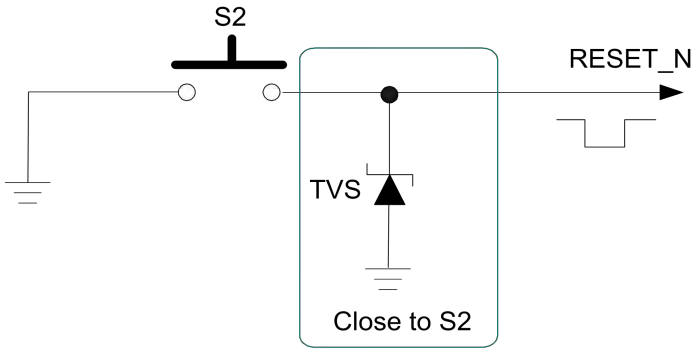


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

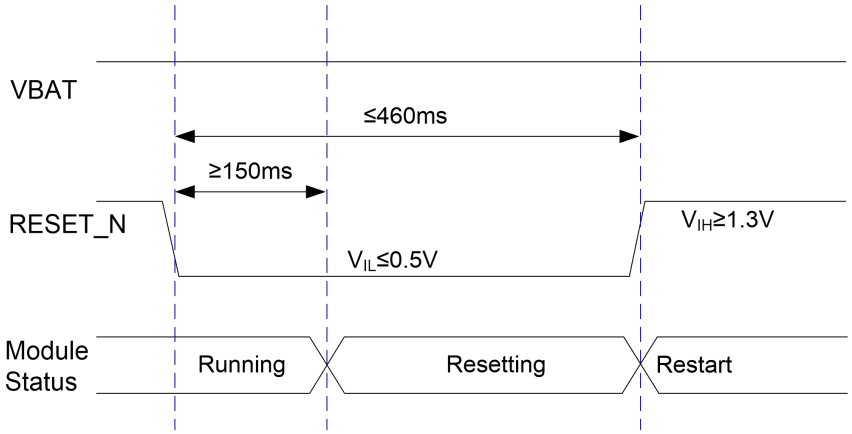


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 9: Pin Definition of the (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	
USIM_CLK	16	DO	Clock signal of (U)SIM card	
USIM_RST	17	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	1.8V power domain. If unused, keep it open.
USIM_GND	10		Specified ground for (U)SIM card	

EC21 supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and

high level detections, and is disabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command for details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

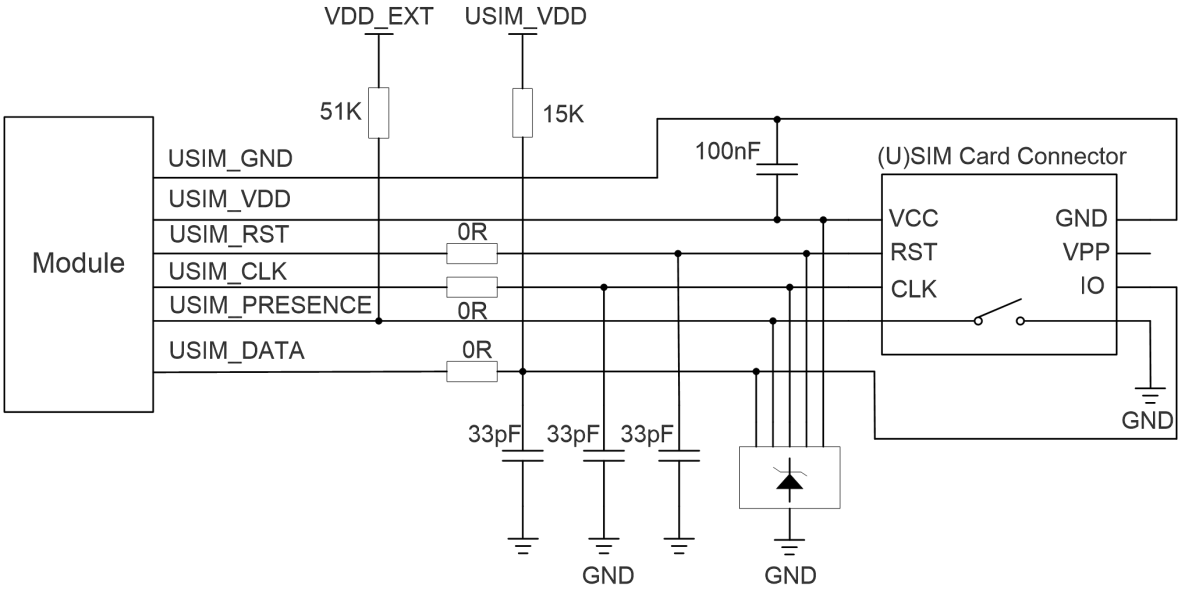


Figure 17: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

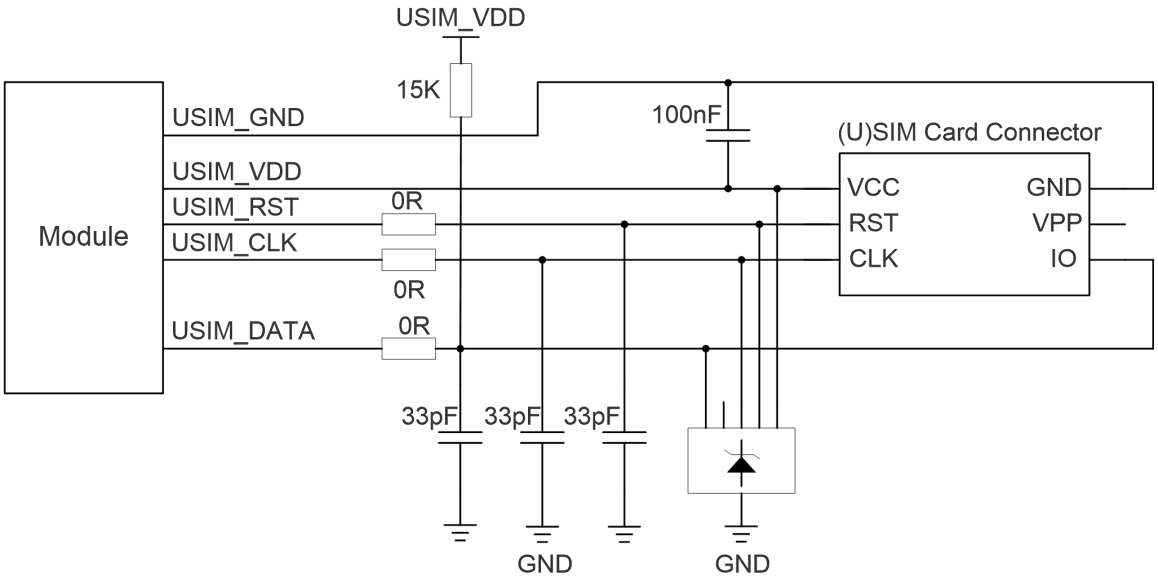


Figure 18: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please

follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1uF, and place it as close to (U)SIM card connector as possible. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15pF. The 0Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33pF capacitors are used for filtering interference of GSM900MHz. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.9. USB Interface

EC21 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 10: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	IO	USB differential data bus (+)	Require differential impedance of 90Ω
USB_DM	70	IO	USB differential data bus (-)	Require differential impedance of 90Ω
USB_VBUS	71	PI	Used for detecting the USB connection	Typically 5.0V
GND	72		Ground	

For more details about the USB 2.0 specification, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' designs. The following figure shows a reference circuit of USB interface.

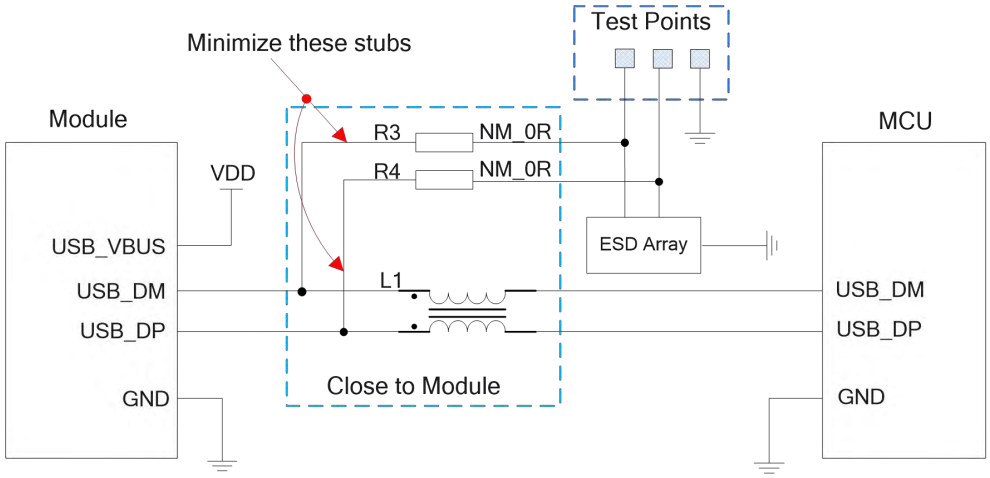


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTES

1. EC21 module can only be used as a slave device.
2. "*" means under development.

3.10. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps and 921600bps baud rates, and the default is 115200bps. The interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 11: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Ring indicator	1.8V power domain
DCD	63	DO	Data carrier detection	
CTS	64	DO	Clear to send	
RTS	65	DI	Request to send	
DTR	66	DI	Data terminal ready	
TXD	67	DO	Transmit data	
RXD	68	DI	Receive data	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Transmit data	1.8V power domain
DBG_RXD	11	DI	Receive data	1.8V power domain

The logic levels are described in the following table.

Table 13: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interface. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

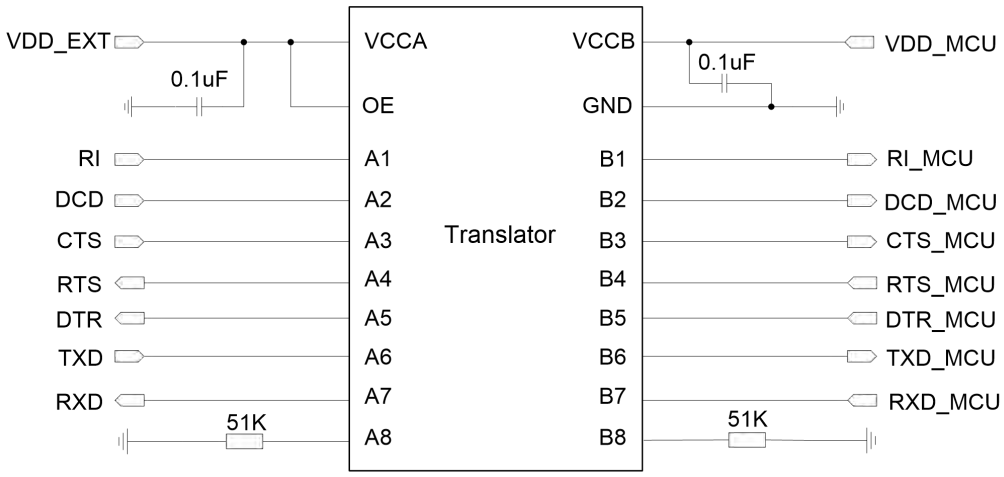


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

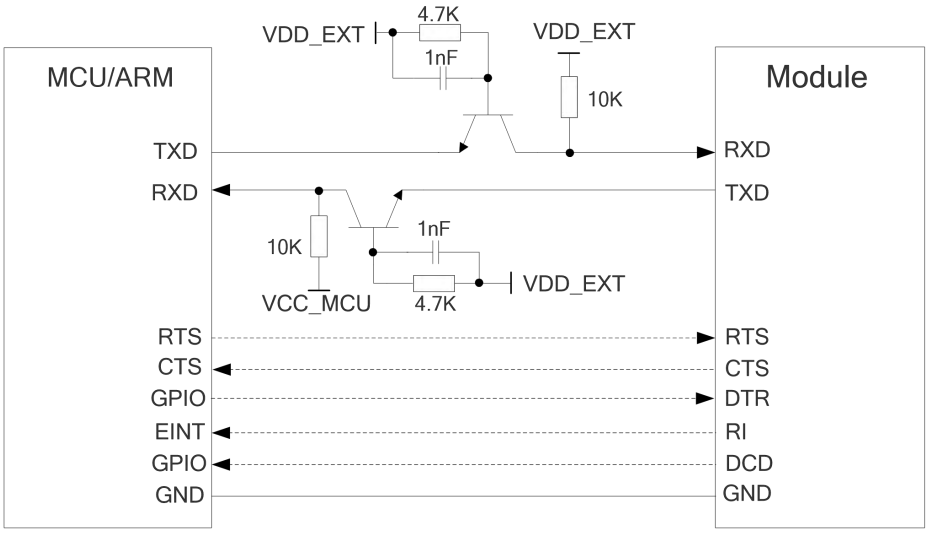


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.11. PCM and I2C Interfaces

EC21 provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC.

EC21 supports 8-bit A-law* and μ-law*, and also 16-bit linear data formats. The following figures show the primary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8kHz PCM_SYNC and 256kHz PCM_CLK.

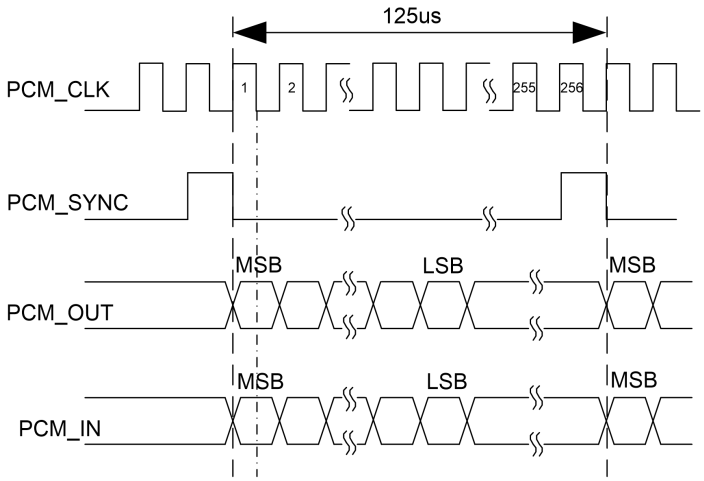


Figure 22: Primary Mode Timing

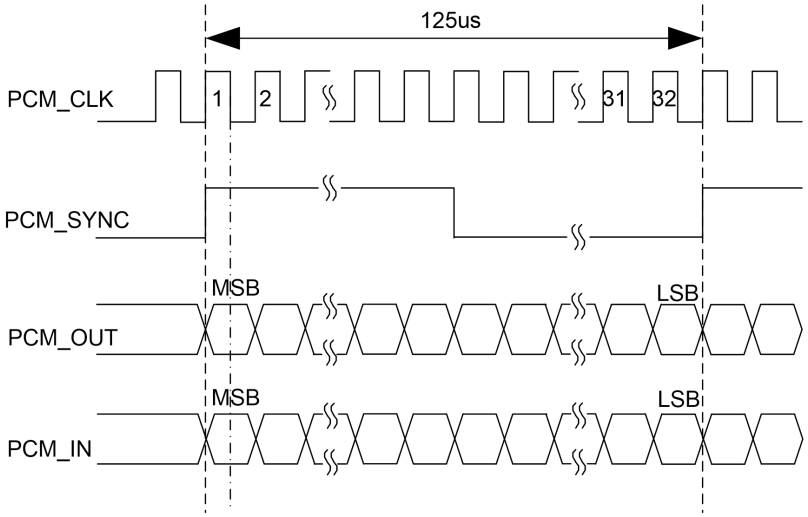


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8V power domain
PCM_OUT	25	DO	PCM data output	1.8V power domain

PCM_SYNC	26	IO	PCM data frame synchronization signal	1.8V power domain
PCM_CLK	27	IO	PCM data bit clock	1.8V power domain
I2C_SCL	41	OD	I2C serial clock	Require external pull-up to 1.8V
I2C_SDA	42	OD	I2C serial data	Require external pull-up to 1.8V

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048KHz PCM_CLK and 8KHz PCM_SYNC. Please refer to ***document [2]*** about **AT+QDAI** command for details.

The following figure shows a reference design of PCM interface with external codec IC.

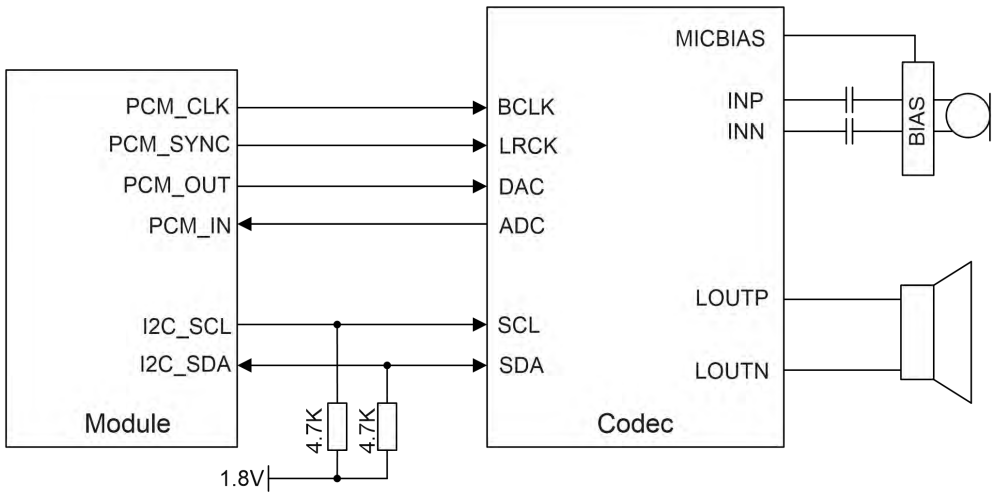


Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTES

1. "*" means under development.
2. It is recommended to reserve RC (R=22Ω, C=22pF) circuits on the PCM lines, especially for PCM_CLK.
3. EC21 works as a master device pertaining to I2C interface.

3.12. SD Card Interface

EC21 supports SDIO3.0 interface for SD card.

The following table shows the pin definition of SD card interface.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	IO	SD card SDIO bus DATA3	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_DATA2	29	IO	SD card SDIO bus DATA2	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_CLK	32	DO	SD card SDIO bus clock	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
SDC2_CMD	33	IO	SD card SDIO bus command	SDIO signal level can be selected according to SD card supported level, more details please refer to SD 3.0 protocol. If unused, keep it open.
VDD_SDIO	34	PO	SD card SDIO bus pull up power	1.8V/2.85V configurable. Cannot be used for SD card power. If unused, keep it open.

SD_INS_DET	23	DI	SD card insertion detection	1.8V power domain. If unused, keep it open.

The following figure shows a reference design of SD card.

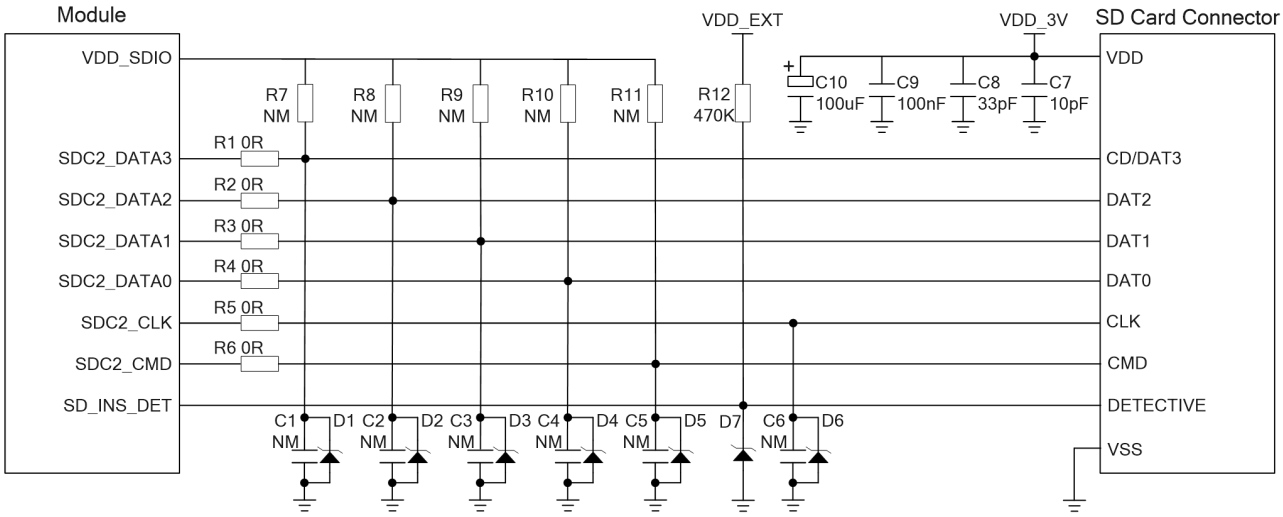


Figure 25: Reference Circuit of SD card

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10KΩ~100KΩ and the recommended value is 100KΩ. VDD_SDIO should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15pF.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total trace length inside the module is 27mm, so the exterior total trace length should be less than 23mm.

3.13. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. **AT+QADC=1** command can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 16: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	45	General purpose analog to digital converter
ADC1	44	General purpose analog to digital converter

The following table describes the characteristic of ADC function.

Table 17: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		bits

NOTES

1. ADC input voltage must not exceed VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.14. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 18: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE[1)]	5	DO	Indicate the module's network registration status	1.8V power domain Cannot be pulled up before startup
NET_STATUS	6	DO	Indicate the module's network activity status	1.8V power domain

Table 19: Working State of Network Connection Status/Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

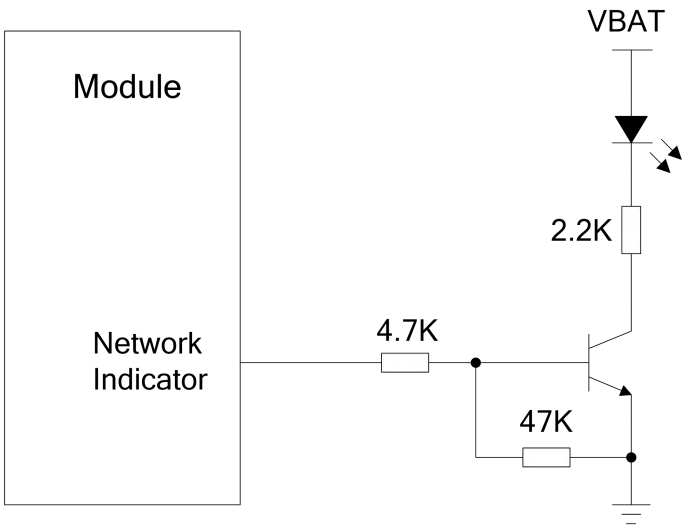


Figure 26: Reference Circuit of the Network Indicator

3.15. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. Customers can connect it to a GPIO of DTE with a pull up resistor, or as the LED indication circuit shown below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and customers can choose either one according to their application demands.

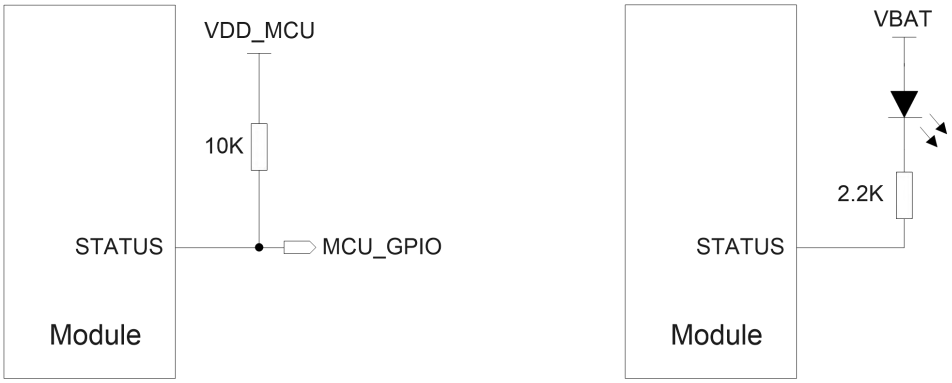


Figure 27: Reference Circuits of STATUS

3.16. Behaviors of RI

AT+QCFG="risignaltype","physical" command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behavior can be configured flexibly. The default behavior of the RI is shown as below.

Table 21: Behavior of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120ms low pulse when a new URC returns

The RI behavior can be changed by **AT+QCFG="urc/ri/ring"** command. Please refer to ***document [2]*** for details.

3.17. SGMII Interface

EC21 includes an integrated Ethernet MAC with an SGMII interface and two management interfaces, key features of the SGMII interface are shown below:

- IEEE802.3 compliance
- Support 10M/100M/1000M Ethernet work mode
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch
- Management interfaces support dual voltage 1.8V/2.85V

The following table shows the pin definition of SGMII interface.

Table 22: Pin Definition of the SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8V/2.85V power domain
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8V power domain

SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	1.8V/2.85V power domain
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V/2.85V power domain
USIM2_VDD	128	PO	SGMII MDIO pull-up power source	Configurable power source. 1.8V/2.85V power domain. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	123	AO	SGMII transmission-minus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	124	AO	SGMII transmission-plus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	125	AI	SGMII receiving-plus	Connect with a 0.1uF capacitor, close to EC21 module.
SGMII_RX_M	126	AI	SGMII receiving-minus	Connect with a 0.1uF capacitor, close to EC21 module.

The following figure shows the simplified block diagram for Ethernet application.

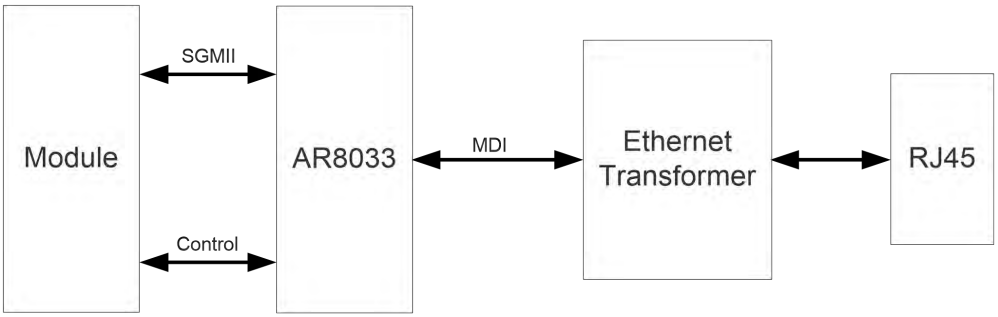


Figure 28: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

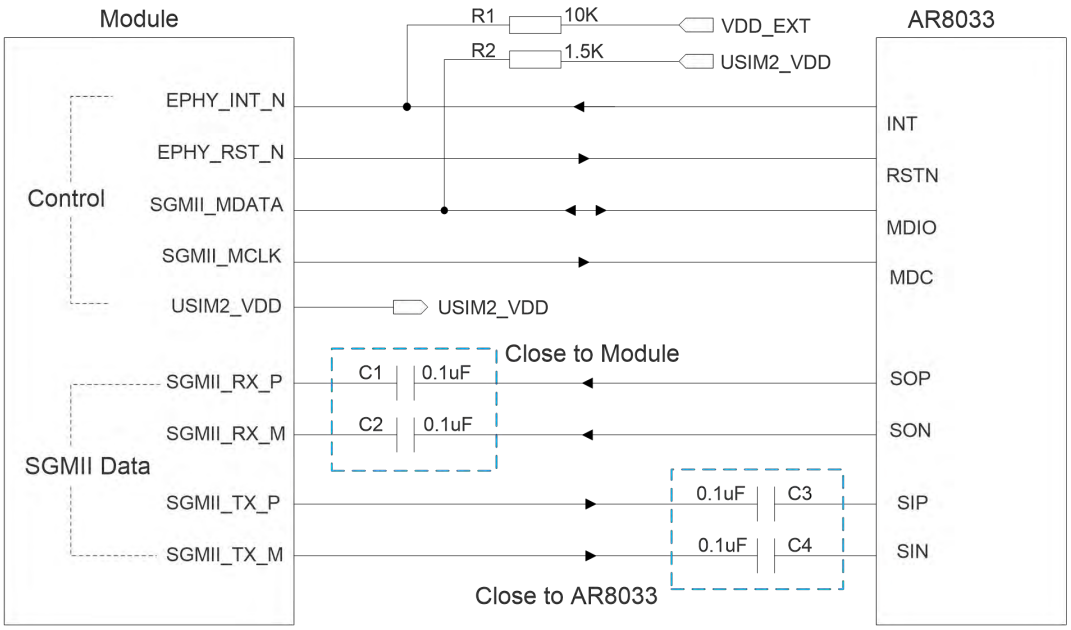


Figure 29: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability in customers' applications, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- Keep the maximum trace length less than 10-inch and keep skew on the differential pairs less than 20mil.
- The differential impedance of SGMII data trace is 100Ω±10%, and the reference ground of the area should be complete.
- Make sure the trace spacing between SGMII RX and TX is at least 3 times of the trace width, and the same to the adjacent signal traces.

Table 24: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module enter into emergency download mode	1.8V power domain. Active high. It is recommended to reserve test point.

The following figure shows a reference circuit of USB_BOOT interface.

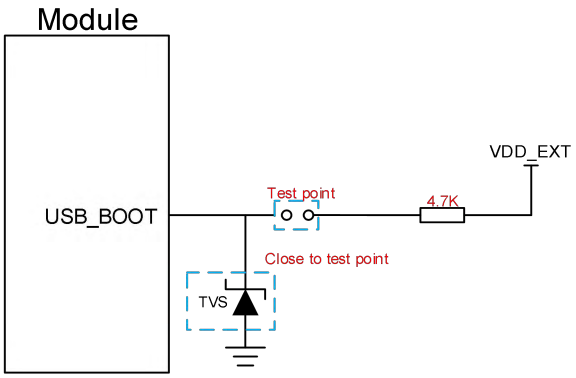


Figure 31: Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1. General Description

EC21 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EC21 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, EC21 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows the GNSS performance of EC21.

Table 25: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s

	Hot start @open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	<1.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers' designs.

- Maximize the distance among GNSS antenna, main antenna and the Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50Ω characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation consideration.

5 Antenna Interfaces

EC21 antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The impedance of the antenna port is 50Ω.

5.1. Main/Rx-diversity Antenna Interfaces

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 26: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna pad	50Ω impedance
ANT_DIV	35	AI	Receive diversity antenna pad	50Ω impedance

5.1.2. Operating Frequency

Table 27: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824~849	869~894	MHz
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
PCS1900	1850~1910	1930~1990	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B2	1850~1910	1930~1990	MHz

WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE FDD B1	1920~1980	2110~2170	MHz
LTE FDD B2	1850~1910	1930~1990	MHz
LTE FDD B3	1710~1785	1805~1880	MHz
LTE FDD B4	1710~1755	2110~2155	MHz
LTE FDD B5	824~849	869~894	MHz
LTE FDD B7	2500~2570	2620~2690	MHz
LTE FDD B8	880~915	925~960	MHz
LTE FDD B12	699~716	729~746	MHz
LTE FDD B13	777~787	746~756	MHz
LTE FDD B18	815~830	860~875	MHz
LTE FDD B19	830~845	875~890	MHz
LTE FDD B20	832~862	791~821	MHz
LTE FDD B26	814~849	859~894	MHz
LTE FDD B28	703~748	758~803	MHz
LTE TDD B40	2300~2400	2300~2400	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

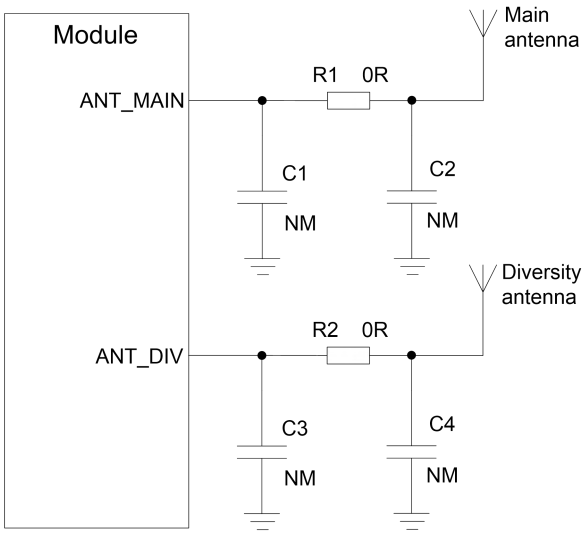


Figure 32: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default.
3. Place the π-type matching components (R1, C1, C2, R2, C3, C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures

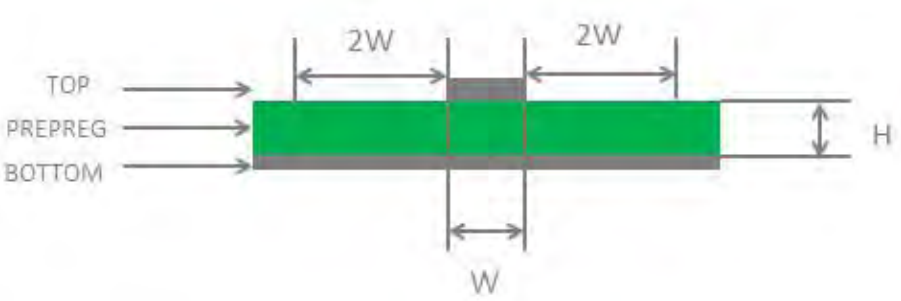


Figure 33: Microstrip Line Design on a 2-layer PCB

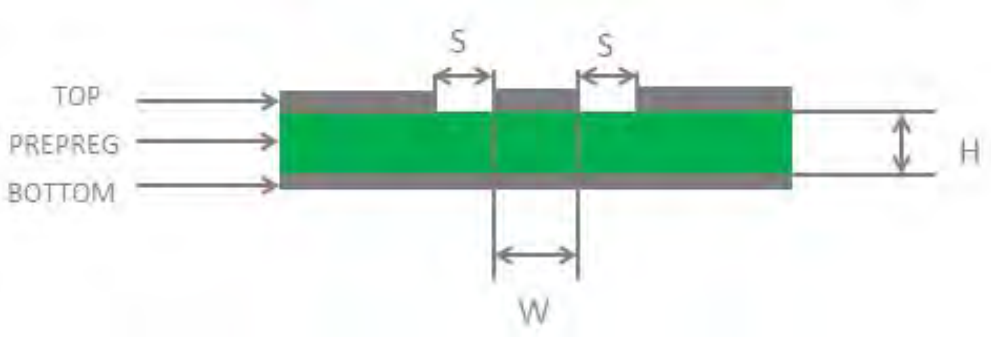


Figure 34: Coplanar Waveguide Line Design on a 2-layer PCB

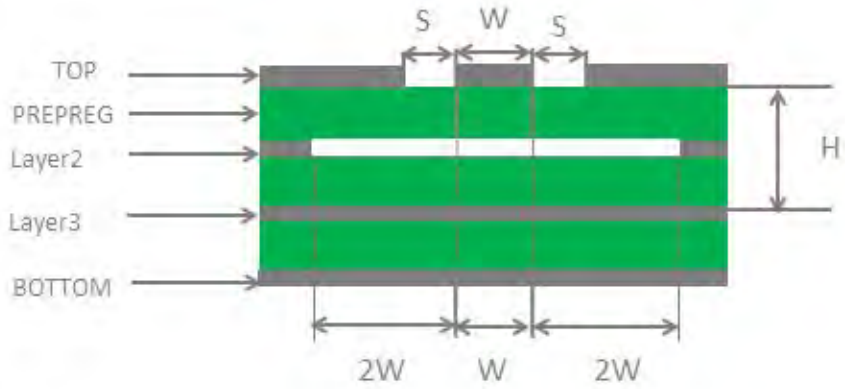


Figure 35: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

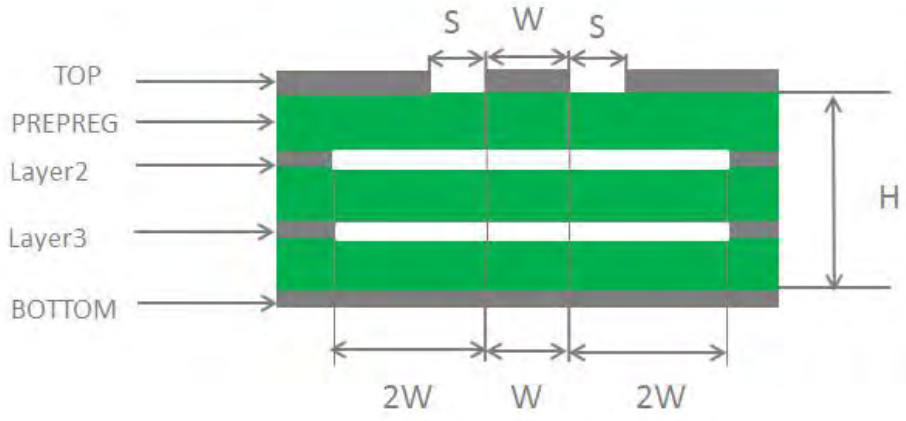


Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 28: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna	50Ω impedance

Table 29: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna is shown as below.

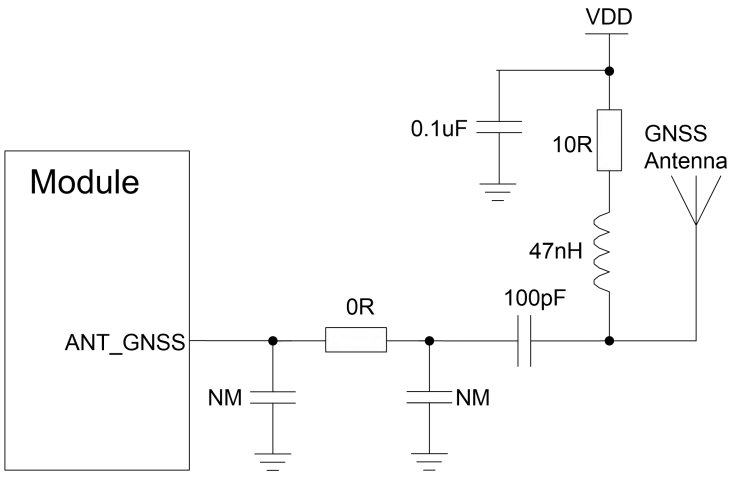


Figure 37: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 30: Antenna Requirements

Type	Requirements
GNSS[1)]	Frequency range: 1561MHz~1615MHz Polarization: RHCP or linear VSWR: <2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: <1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: <17 dB
GSM/WCDMA/LTE	VSWR: ≤2 Efficiency: > 30%

	Max Input Power: 50 W Input Impedance: 50Ω Cable insertion loss: <1dB (GSM850, GSM900, WCDMA B5/B8, LTE-FDD B5/B8/B12/B13/B18/B19/B20/B26/B28) Cable insertion loss: <1.5dB (DCS1800, PCS1900, WCDMA B1/B2/B4, LTE B1/B2/B3/B4) Cable insertion loss <2dB (LTE-FDD B7, LTE-TDD B40)

NOTE

[1] It is recommended to use a passive antenna when the module supports B13 or B14, because harmonics will be generated when using an active antenna, which will affect the GNSS performance

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

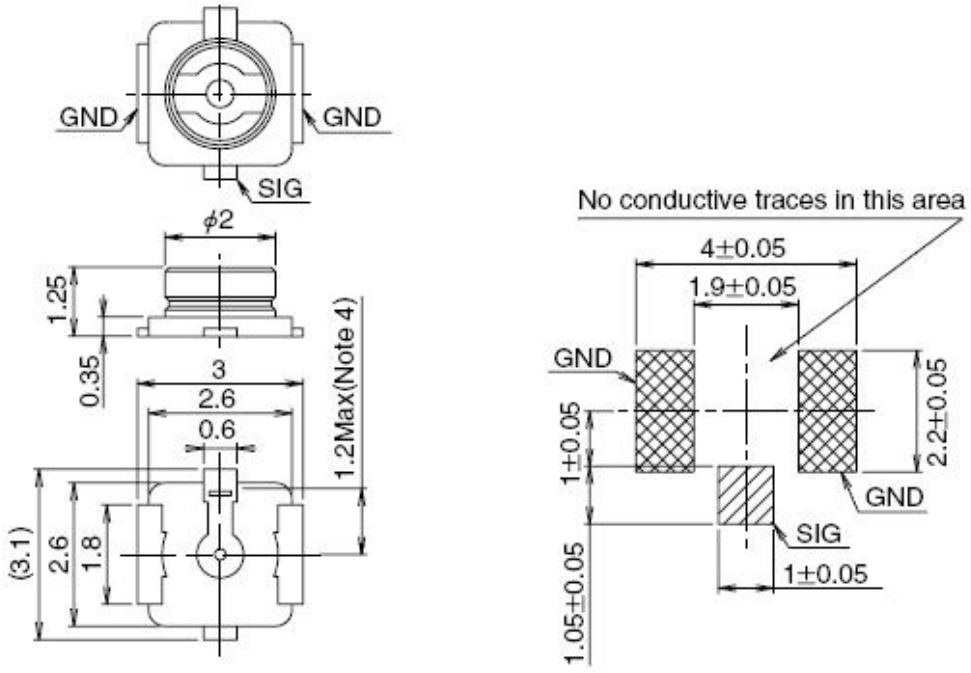


Figure 38: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

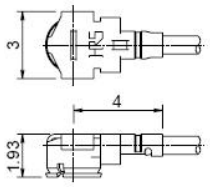
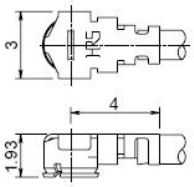
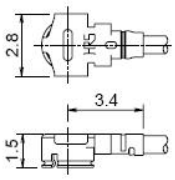
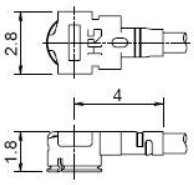
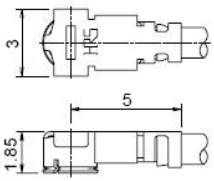
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

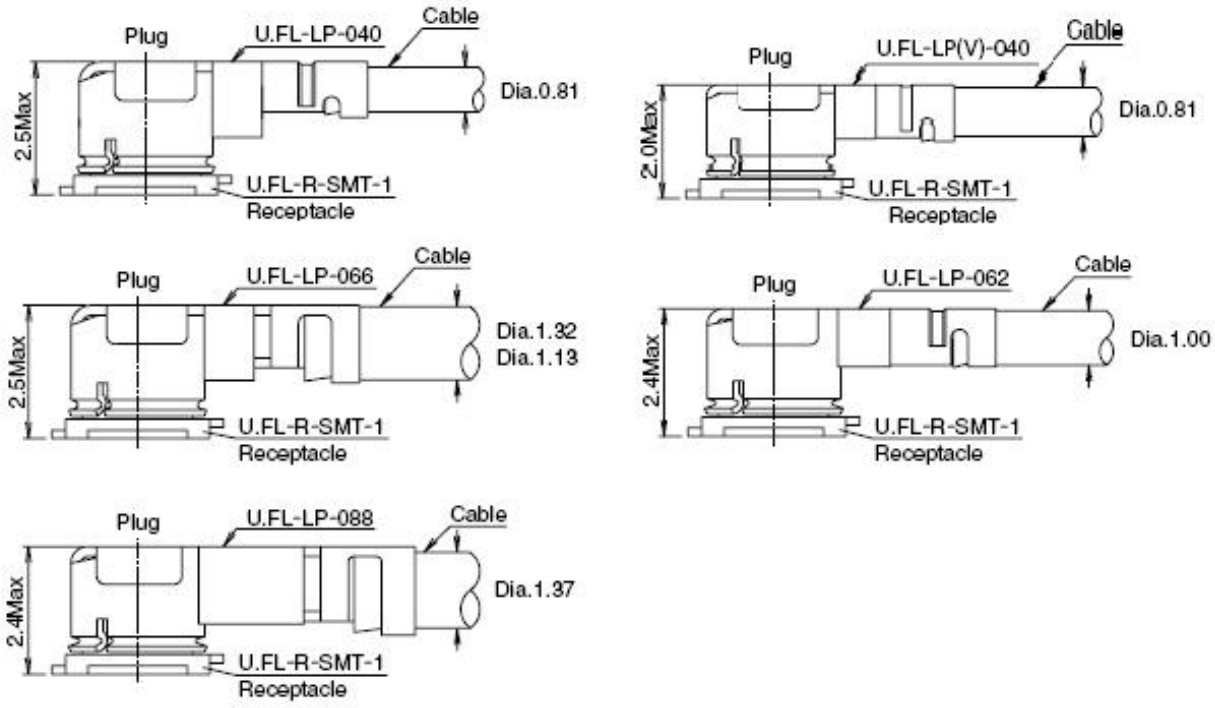


Figure 40: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 32: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on GSM900			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on GSM900		1.8	2.0	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 33: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range[1)]	-35	+25	+75	ºC
Extended Temperature Range[2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The values of current consumption are shown below.

Table 34: EC21-E Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	13	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.4	mA
		GSM900 @DRX=9 (USB disconnected)	1.8	mA
		DCS1800 @DRX=9 (USB disconnected)	1.8	mA
		WCDMA PF=64 (USB disconnected)	2.4	mA
		WCDMA PF=128 (USB disconnected)	1.9	mA
		FDD-LTE PF=64 (USB disconnected)	3.2	mA
		FDD-LTE PF=128 (USB disconnected)	2.1	mA
	Idle state (GNSS OFF)	GSM900 @DRX=5 (USB disconnected)	22.0	mA
		GSM900 @DRX=5 (USB connected)	32.0	mA
		WCDMA PF=64 (USB disconnected)	22.5	mA
		WCDMA PF=64 (USB connected)	32.7	mA
		LTE-FDD PF=64 (USB disconnected)	22.5	mA
		LTE-FDD PF=64 (USB connected)	32.5	mA
	GPRS data transfer (GNSS OFF)	GSM900 4DL/1UL @32.3dBm	220	mA
		GSM900 3DL/2UL @32.18dBm	387	mA
		GSM900 2DL/3UL @30.3dBm	467	mA
		GSM900 1DL/4UL @29.4dBm	555	mA
		DCS1800 4DL/1UL @29.6dBm	185	mA
		DCS1800 3DL/2UL @29.1dBm	305	mA

		DCS1800 2DL/3UL @28.8dBm	431	mA
		DCS1800 1DL/4UL @29.1dBm	540	mA
	EDGE data transfer (GNSS OFF)	GSM900 4DL/1UL @26dBm	148	mA
		GSM900 3DL/2UL @26dBm	245	mA
		GSM900 2DL/3UL @25dBm	338	mA
		GSM900 1DL/4UL @25dBm	432	mA
		DCS1800 4DL/1UL @26dBm	150	mA
		DCS1800 3DL/2UL @25dBm	243	mA
		DCS1800 2DL/3UL @25dBm	337	mA
		DCS1800 1DL/4UL @25dBm	430	mA
	WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @22.5dBm	659	mA
		WCDMA B1 HSUPA @21.11dBm	545	mA
		WCDMA B5 HSDPA @23.5dBm	767	mA
		WCDMA B5 HSUPA @21.4dBm	537	mA
		WCDMA B8 HSDPA @22.41dBm	543	mA
		WCDMA B8 HSUPA @21.2dBm	445	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.45dBm	807	mA
		LTE-FDD B3 @23.4dBm	825	mA
		LTE-FDD B5 @23.4dBm	786	mA
		LTE-FDD B7 @23.86dBm	887	mA
		LTE-FDD B8 @23.5dBm	675	mA
		LTE-FDD B20 @23.57dBm	770	mA
	GSM voice call	GSM900 PCL=5 @32.8dBm	336	mA
		PCS1800 PCL=0 @29.3dBm	291	mA
	WCDMA voice call	WCDMA B1 @23.69dBm	683	mA

	WCDMA B5 @23.61dBm	741	mA
	WCDMA B8 @23.35dBm	564	mA

Table 35: EC21-A Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.25	mA
		WCDMA PF=64 (USB disconnected)	2.03	mA
		WCDMA PF=128 (USB disconnected)	1.65	mA
		LTE-FDD PF=64 (USB disconnected)	2.31	mA
		LTE-FDD PF=128 (USB disconnected)	1.85	mA
	Idle state (GNSS OFF)	WCDMA PF=64 (USB disconnected)	23.1	mA
		WCDMA PF=64 (USB connected)	32.8	mA
		LTE-FDD PF=64 (USB disconnected)	22.8	mA
		LTE-FDD PF=64 (USB connected)	32.8	mA
	WCDMA data transfer (GNSS OFF)	WCDMA B2 HSDPA @21.54dBm	479.0	mA
		WCDMA B2 HSUPA @22.19dBm	530.0	mA
		WCDMA B4 HSDPA @22.15dBm	539.0	mA
		WCDMA B4 HSUPA @21.82dBm	531.0	mA
		WCDMA B5 HSDPA @22.22dBm	454.0	mA
		WCDMA B5 HSUPA @21.45dBm	433.0	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B2 @23.11dBm	721.0	mA
		LTE-FDD B4 @23.16dBm	748.0	mA
		LTE-FDD B12 @23.25dBm	668.0	mA
	WCDMA voice call	WCDMA B2 @22.97dBm	565.0	mA

	WCDMA B4 @22.91dBm	590.0	mA
	WCDMA B5 @23.06dBm	493.0	mA

Table 36: EC21-V Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.07	mA
		LTE-FDD PF=64 (USB disconnected)	2.85	mA
		LTE-FDD PF=128 (USB disconnected)	2.26	mA
	Idle state (GNSS OFF)	LTE-FDD PF=64 (USB disconnected)	22.0	mA
		LTE-FDD PF=64 (USB connected)	32.0	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B4 @22.77dBm	762.0	mA
		LTE-FDD B13 @23.05dBm	533.0	mA

Table 37: EC21-AUT Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.99	mA
		WCDMA PF=64 (USB disconnected)	2.1	mA
		WCDMA PF=128 (USB disconnected)	1.7	mA
		LTE-FDD PF=64 (USB disconnected)	2.9	mA
		LTE-FDD PF=128 (USB disconnected)	2.4	mA
	Idle state	WCDMA PF=64 (USB disconnected)	22.0	mA
		WCDMA PF=64 (USB connected)	32.0	mA
		LTE-FDD PF=64 (USB disconnected)	23.6	mA
		LTE-FDD PF=64 (USB connected)	33.6	mA

	WCDMA data (GNSS OFF)	WCDMA B1 HSDPA @22.59dBm	589.0	mA
		WCDMA B1 HSUPA @22.29dBm	623.0	mA
		WCDMA B5 HSDPA @22.22dBm	511.0	mA
		WCDMA B5 HSUPA @21.64dBm	503.0	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.38dBm	813.0	mA
		LTE-FDD B3 @22.87dBm	840.0	mA
		LTE-FDD B5 @23.12dBm	613.0	mA
		LTE-FDD B7 @22.96dBm	761.0	mA
		LTE-FDD B28 @23.31dBm	650.0	mA
	WCDMA voice call	WCDMA B1 @24.21dBm	687.0	mA
		WCDMA B5 @23.18dBm	535.0	mA

Table 38: EC21-AUV Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.15	mA
		WCDMA PF=64 (USB disconnected)	2.06	mA
		WCDMA PF=128 (USB disconnected)	1.65	mA
		LTE-FDD PF=64 (USB disconnected)	2.46	mA
		LTE-FDD PF=128 (USB disconnected)	1.86	mA
	Idle state (GNSS OFF)	WCDMA PF=64 (USB disconnected)	22.0	mA
		WCDMA PF=64 (USB connected)	32.0	mA
		LTE-FDD PF=64 (USB disconnected)	23.5	mA
		LTE-FDD PF=64 (USB connected)	33.5	mA
	WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @22.59dBm	623.0	mA
		WCDMA B1 HSUPA @22.47dBm	628.0	mA
		WCDMA B5 HSDPA @22.95dBm	605.0	mA

		WCDMA B5 HSUPA @22.87dBm	610.0	mA
		WCDMA B8 HSDPA @22.37dBm	549.0	mA
		WCDMA B8 HSUPA @22.09dBm	564.0	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.28dBm	789.0	mA
		LTE-FDD B3 @23.2dBm	768.0	mA
		LTE-FDD B5 @23.05dBm	669.0	mA
		LTE-FDD B8 @23.21dBm	693.0	mA
		LTE-FDD B28 @22.9dBm	795.0	mA
	WCDMA voice call	WCDMA B1 @23.43dBm	672.0	mA
		WCDMA B5 @23.32dBm	616.0	mA
		WCDMA B8 @23.31dBm	592.0	mA

Table 39: EC21-J Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.85	mA
		LTE-FDD PF=64 (USB disconnected)	2.20	mA
		LTE-FDD PF=128 (USB disconnected)	1.46	mA
	Idle state (GNSS OFF)	LTE-FDD PF=64 (USB disconnected)	23.5	mA
		LTE-FDD PF=64 (USB connected)	33.8	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.35dBm	734.0	mA
		LTE-FDD B3 @22.95dBm	778.0	mA
		LTE-FDD B8 @22.81dBm	722.0	mA
		LTE-FDD B18 @23.15dBm	677.0	mA
		LTE-FDD B19 @23.17dBm	688.0	mA
		LTE-FDD B26 @23.37dBm	723.0	mA

Table 40: EC21-KL Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.08	mA
		LTE-FDD PF=64 (USB disconnected)	2.1	mA
		LTE-FDD PF=128 (USB disconnected)	1.4	mA
	Idle state (GNSS OFF)	LTE-FDD PF=64 (USB disconnected)	24.8	mA
		LTE-FDD PF=64 (USB connected)	33.5	mA
	LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.0dBm	771.0	mA
		LTE-FDD B3 @23.36dBm	780.0	mA
		LTE-FDD B5 @23.56dBm	628.0	mA
		LTE-FDD B7 @23.32dBm	754.0	mA
		LTE-FDD B8 @23.33dBm	680.0	mA

Table 41: GNSS Current Consumption of EC21 Series Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (AT+CFUN=0)	Cold start @Passive Antenna	58	mA
		Lost state @Passive Antenna	58	mA
	Tracking (AT+CFUN=0)	Instrument Environment	33	mA
		Open Sky @Passive Antenna	35	mA
		Open Sky @Active Antenna	43	mA

6.5. RF Output Power

The following table shows the RF output power of EC21 module.

Table 42: RF Output Power

Frequency	Max.	Min.
GSM850/GSM900	33dBm±2dB	5dBm±5dB
DCS1800/PCS1900	30dBm±2dB	0dBm±5dB
GSM850/GSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800/PCS1900 (8-PSK)	26dBm±3dB	0dBm±5dB
WCDMA bands	24dBm+1/-3dB	<-49dBm
LTE-FDD bands	23dBm±2dB	<-39dBm
LTE-TDD bands	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

The following tables show the conducted RF receiving sensitivity of EC21 series module.

Table 43: EC21-E Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
GSM900	-109.0dBm	/	/	-102.0dBm
DCS1800	-109.0dBm	/	/	-102.0dbm
WCDMA Band 1	-110.5dBm	/	/	-106.7dBm
WCDMA Band 5	-110.5dBm	/	/	-104.7dBm
WCDMA Band 8	-110.5dBm	/	/	-103.7dBm
LTE-FDD B1 (10M)	-98.0dBm	-98.0dBm	-101.5dBm	-96.3dBm
LTE-FDD B3 (10M)	-96.5dBm	-98.5dBm	-101.5dBm	-93.3dBm

LTE-FDD B5 (10M)	-98.0dBm	-98.5dBm	-101.0dBm	-94.3dBm
LTE-FDD B7 (10M)	-97.0dBm	-94.5dBm	-99.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-97.0dBm	-97.0dBm	-101.0dBm	-93.3dBm
LTE-FDD B20 (10M)	-97.5dBm	-99.0dBm	-102.5dBm	-93.3dBm

Table 44: EC21-A Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
WCDMA B2	-110.0dBm	/	/	-104.7dBm
WCDMA B4	-110.0dBm	/	/	-106.7dBm
WCDMA B5	-110.5dBm	/	/	-104.7dBm
LTE-FDD B2 (10M)	-98.0dBm	-98.0dBm	-101.0dBm	-94.3dBm
LTE-FDD B4 (10M)	-97.5dBm	-99.0dBm	-101.0dBm	-96.3dBm
LTE-FDD B12 (10M)	-96.5dBm	-98.0dBm	-101.0dBm	-93.3dBm

Table 45: EC21-V Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
LTE-FDD B4 (10M)	-97.5dBm	-99.0dBm	-101.0dBm	-96.3dBm
LTE-FDD B13 (10M)	-95.0dBm	-97.0dBm	-100.0dBm	-93.3dBm

Table 46: EC21-AUT Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
WCDMA B1	-110.0dBm	/	/	-106.7dBm
WCDMA B5	-110.5dBm	/	/	-104.7dBm
LTE-FDD B1 (10M)	-98.5dBm	-98.0dBm	-101.0dBm	-96.3dBm
LTE-FDD B3 (10M)	-98.0dBm	-96.0dBm	-100.0dBm	-93.3dBm

LTE-FDD B5 (10M)	-98.0dBm	-99.0dBm	-102.5dBm	-94.3dBm
LTE-FDD B7 (10M)	-97.0dBm	-95.0dBm	-98.5dBm	-94.3dBm
LTE-FDD B28 (10M)	-97.0dBm	-99.0dBm	-102.0dBm	-94.8dBm

Table 47: EC21-KL Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
LTE-FDD B1 (10M)	-98.0dBm	-99.5dBm	-100.5dBm	-96.3dBm
LTE-FDD B3 (10M)	-97.0dBm	-97.5dBm	-99.5dBm	-93.3dBm
LTE-FDD B5 (10M)	-98.0dBm	-99.5dBm	-100.5dBm	-94.3dBm
LTE-FDD B7 (10M)	-96.0dBm	-96.0dBm	-98.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-97.0dBm	-99.0dBm	-101.0dBm	-93.3dBm

Table 48: EC21-J Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
LTE-FDD B1 (10M)	-97.5dBm	-98.7dBm	-100.2dBm	-96.3dBm
LTE-FDD B3 (10M)	-96.5dBm	-97.1dBm	-100.5dBm	-93.3dBm
LTE-FDD B8 (10M)	-98.4dBm	-99.0dBm	-101.2dBm	-93.3dBm
LTE-FDD B18 (10M)	-99.5dBm	-99.0dBm	-101.7dBm	-96.3dBm
LTE-FDD B19 (10M)	-99.2dBm	-99.0dBm	-101.4dBm	-96.3dBm
LTE-FDD B26 (10M)	-99.5dBm	-99.0dBm	-101.5dBm	-93.8dBm

Table 49: EC21-AUV Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
WCDMA B1	-109.5dBm	/	/	-106.7dBm
WCDMA B5	-111.0dBm	/	/	-104.7dBm

WCDMA B8	-111.0dBm	/	/	-103.7dBm
LTE-FDD B1 (10M)	-97.7dBm	-97.5dBm	-101.3dBm	-96.3dBm
LTE-FDD B3 (10M)	-98.2dBm	-98.6dBm	-102.7dBm	-93.3dBm
LTE-FDD B5 (10M)	-98.7dBm	-98.2dBm	-102.5dBm	-94.3dBm
LTE-FDD B8 (10M)	-98.2dBm	-98.2dBm	-102.3dBm	-93.3dBm
LTE-FDD B28 (10M)	-98.0dBm	-98.7dBm	-102.1dBm	-94.8dBm

Table 50: EC21-AU Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
GSM850	-109.0dBm	/	/	-102.0dBm
GSM900	-109.0dBm	/	/	-102.0dBm
DCS1800	-109.0dBm	/	/	-102.0dBm
PCS1900	-109.0dBm	/	/	-102.0dBm
WCDMA B1	-110.0dBm	/	/	-106.7dBm
WCDMA B2	-110.0dBm	/	/	-104.7dBm
WCDMA B5	-111.0dBm	/	/	-104.7dBm
WCDMA B8	-111.0dBm	/	/	-103.7dBm
LTE-FDD B1 (10M)	-97.2dBm	-97.5dBm	-100.2dBm	-96.3dBm
LTE-FDD B2 (10M)	-98.2dBm	/	/	-94.3dBm
LTE-FDD B3 (10M)	-98.7dBm	-98.6dBm	-102.2dBm	-93.3dBm
LTE-FDD B4 (10M)	-97.7dBm	-97.4dBm	-100.2dBm	-96.3dBm
LTE-FDD B5 (10M)	-98.0dBm	-98.2dBm	-101.0dBm	-94.3dBm
LTE-FDD B7 (10M)	-97.7dBm	-97.7dBm	-101.2dBm	-94.3dBm
LTE-FDD B8 (10M)	-99.2dBm	-98.2dBm	-102.2dBm	-93.3dBm
LTE-FDD B28 (10M)	-98.6dBm	-98.7dBm	-102.0dBm	-94.8dBm

LTE-TDD B40 (10M)	-97.2dBm	-98.4dBm	-101.2dBm	-96.3dBm

NOTE

1) SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

6.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics.

Table 51: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.

- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

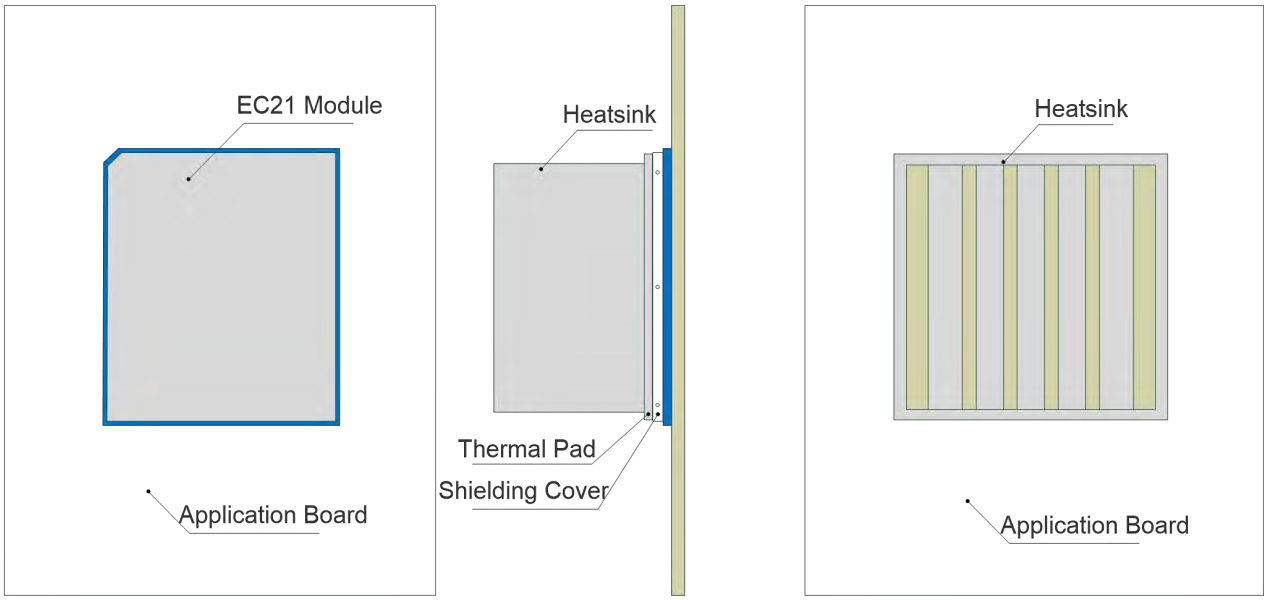


Figure 41: Referenced Heatsink Design (Heatsink at the Top of the Module)

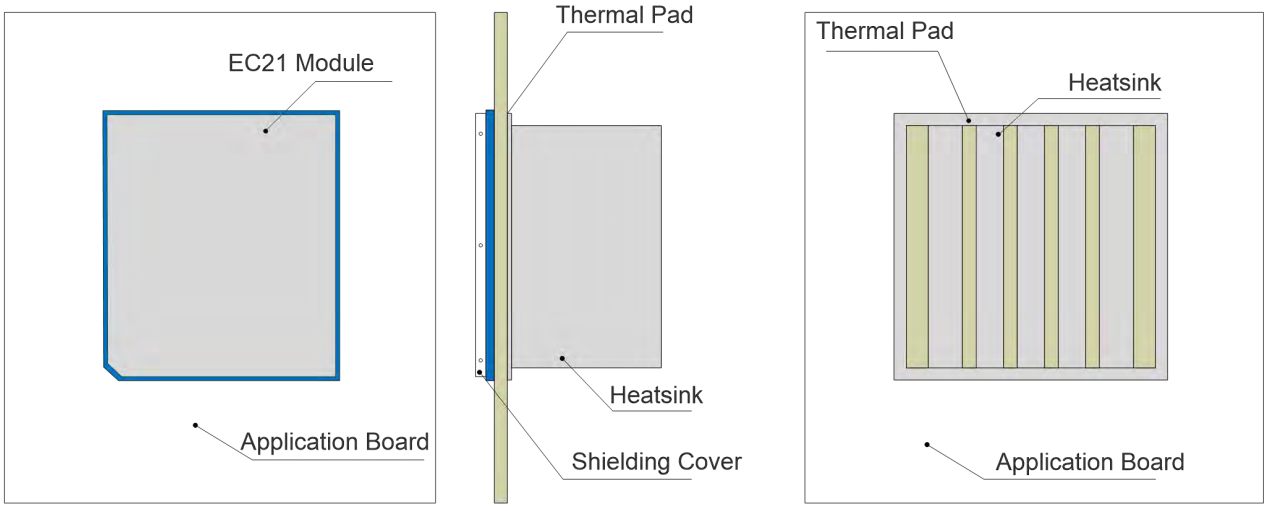


Figure 42: Referenced Heatsink Design (Heatsink at the Bottom of Customers' PCB)

NOTE

The module offers the best performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command and get the maximum BB chip temperature from the first returned value.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

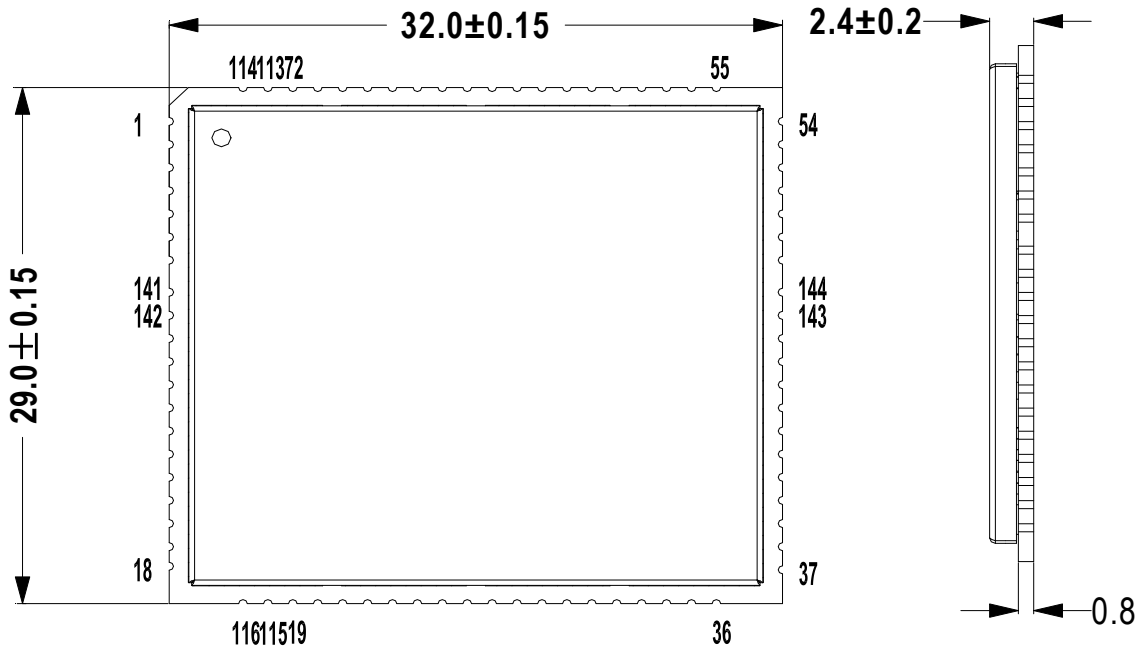


Figure 43: Module Top and Side Dimensions

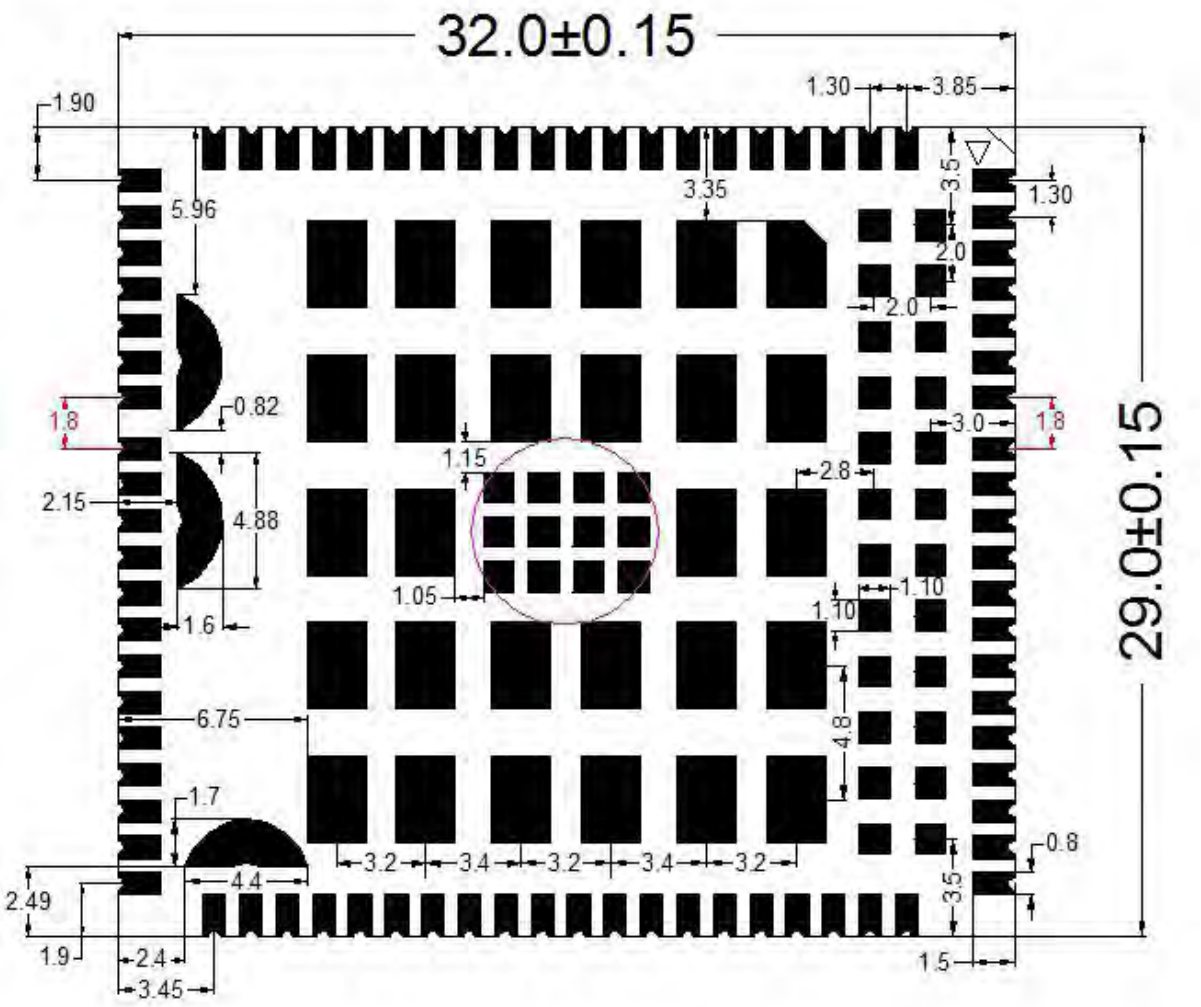


Figure 44: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

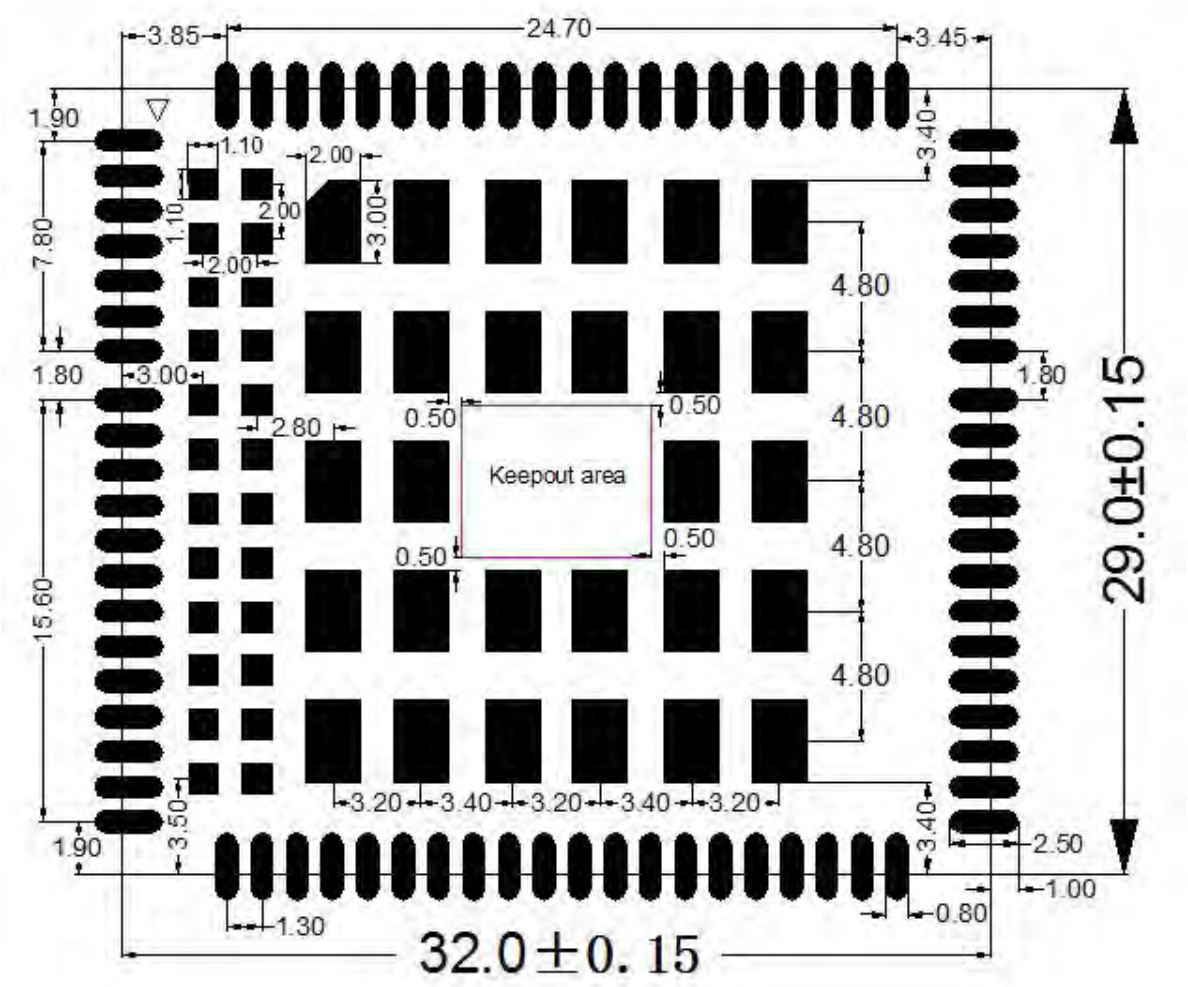


Figure 45: Recommended Footprint (Top View)

NOTES

1. The keep out area should not be designed.
2. For easy maintenance of the module, please keep about 3mm between the module and other components in the host PCB.

7.3. Design Effect Drawings of the Module

Figure 46: Top View of the Module

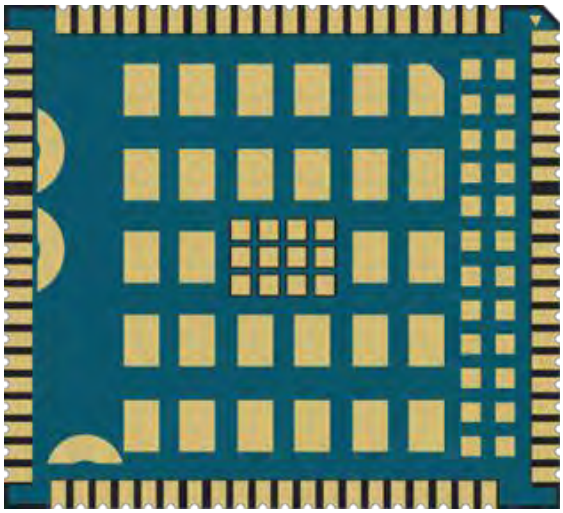


Figure 47: Bottom View of the Module

NOTE

These are design effect drawings of EC21 module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EC21 is stored in a vacuum-sealed bag. The storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

- Mounted within 168 hours at the factory environment of ≤30ºC/60%RH
- Stored at <10%RH

3. Devices require baking before mounting, if any circumstances below occurs:

- When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
- Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.20mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 235ºC~245ºC (for SnAg3.0Cu0.5 alloy). The absolute maximum reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

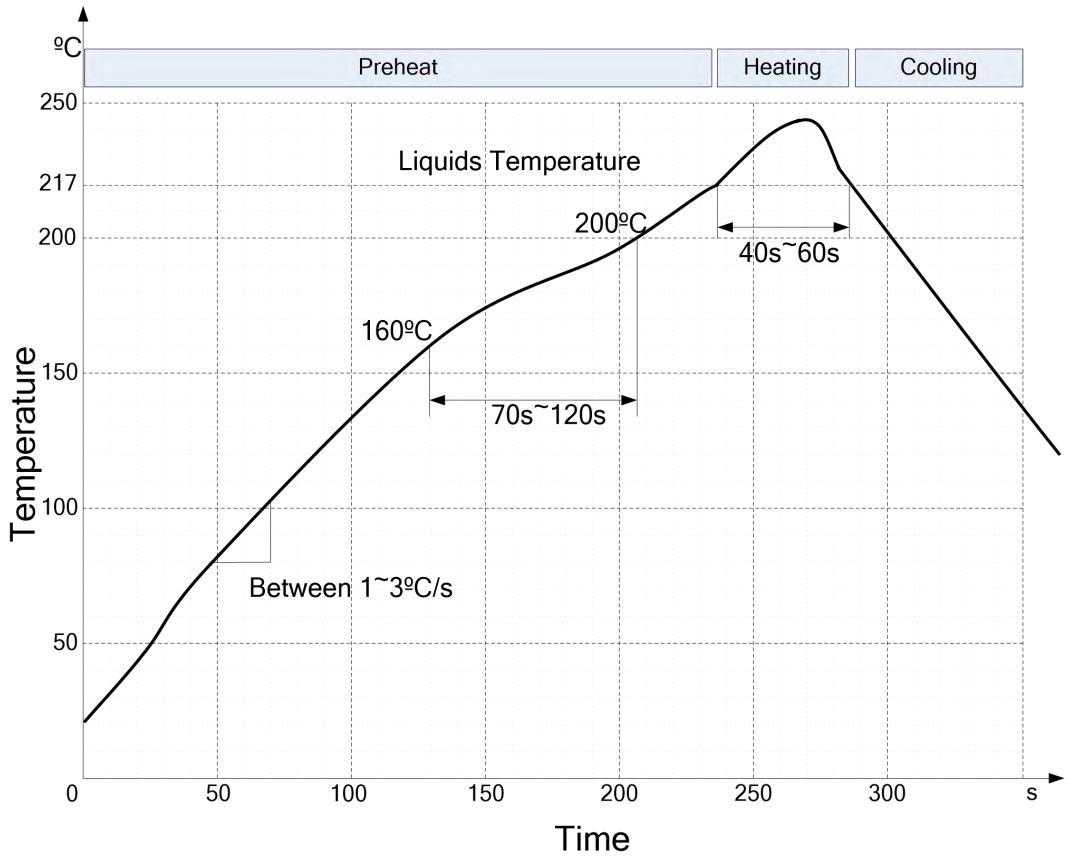


Figure 48: Reflow Soldering Thermal Profile

NOTE

During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module label with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc.

8.3. Packaging

EC21 is packaged in tape and reel carriers. One reel is 11.88m long and contains 250pcs modules. The figure below shows the packaging details, measured in mm.

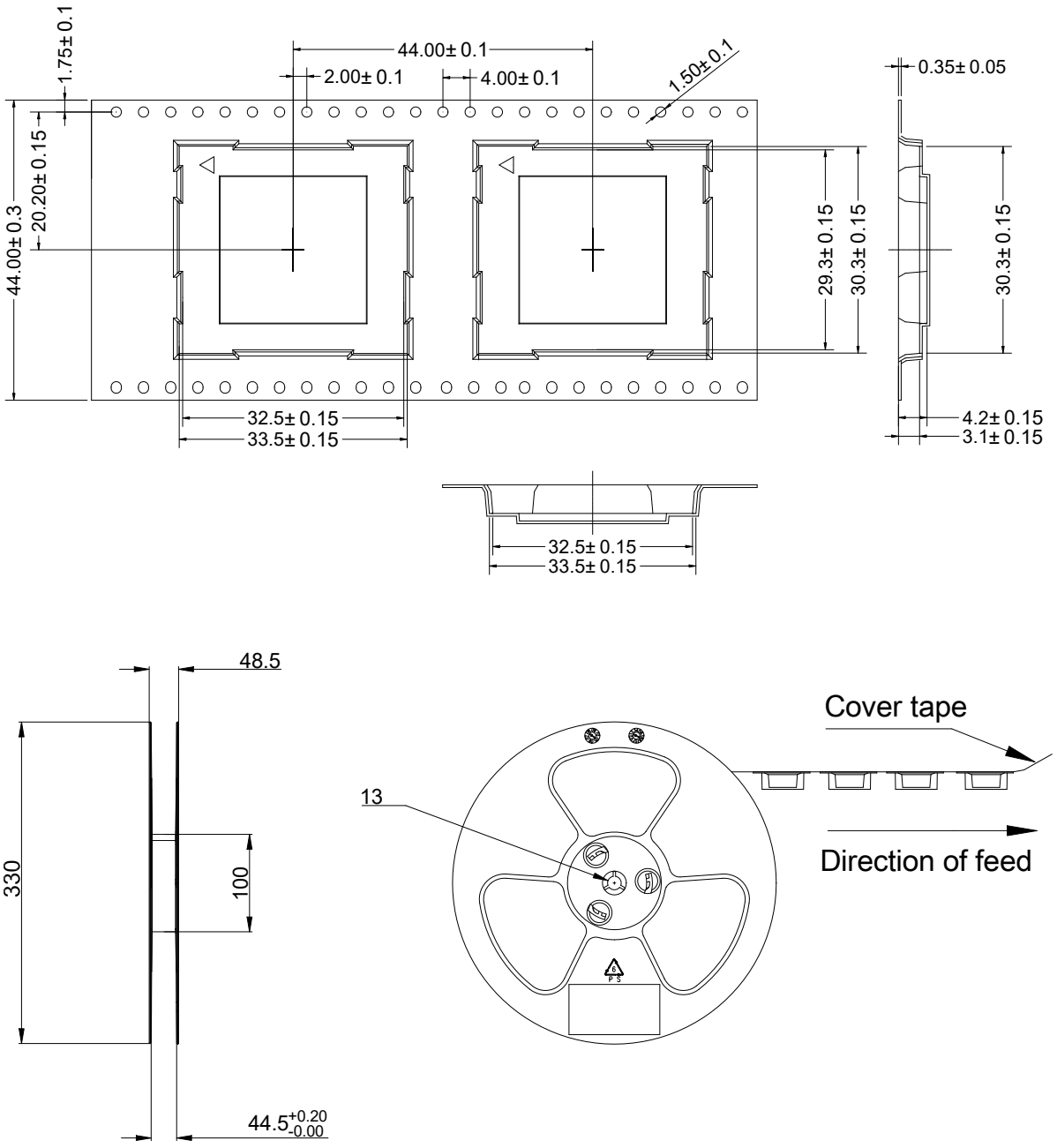


Figure 49: Tape and Reel Specifications

9 Appendix A References

Table 52: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EG9x&EM05_Power_Management_Application_Note	Power management application notefor EC25, EC21, EC20 R2.0, EC20 R2.1, EG95, EG91 and EM05 modules
[2]	Quectel_EC25&EC21_AT_Commands_Manual	EC25 and EC21 AT commands manual
[3]	Quectel_EC25&EC21_GNSS_AT_Commands_Manual	EC25 and EC21 GNSS AT commands manual
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[5]	Quectel_EC21_Reference_Design	EC21 reference design
[6]	Quectel_RF_Layout_Application_Note	RF layout application note

Table 53: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink

DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol

PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value

V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

10 Appendix B GPRS Coding Schemes

Table 54: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 55: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 56: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time- averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR201609EC21V.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

❒GSM/850/GSM1900/ WCDMA B2/B5/LTE B2/B4/B5/B7: <4dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labelled withan FCC ID - Section 2.926 (see 2.2 Certification (labelling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labelling requirements,options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is notvisible when installed in the host, or (2) if the host is marketed so that end users do not havestraightforward commonly used methods for access to remove the module so that the FCC ID ofthe module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID:XMR201606EC21A" or "Contains FCC ID: XMR201609EC21V" mustbe used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a

computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.