EG61-NAHardware Design

LTEModule Series

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About the Document

History

Revision	Date	Author	Description
1.0	2019-01-04	Ward WANG/ Frank WANG	Initial

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1 Introduction

This document defines the EG61-NAmodule and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical andmechanical details, as well as other related information of EG61-NA module. Associated with application note and user guide, customers can use EG61-NA module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EG61-NA module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

1.2. FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR201903EG61NA.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- ❒ WCDMA Band2/ LTE Band2:≤8dBi
- ❒ WCDMA Band4/ LTE Band4/66:≤5dBi
- ❒ WCDMA Band5/ LTE Band5:≤9.42dBi
- ❒ LTE Band12:≤8.73dBi
- ❒ LTE Band13:≤9.17dBi
- ❒ LTE Band71:≤8.55dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XMR201903EG61NA" or "Contains FCC ID: XMR201903EG61NA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

1.3. IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF

The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre

antenne ou un autre émetteur.

To comply with IC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- ❒WCDMA Band2/ LTE Band2:≤8dBi
- ❒WCDMA Band4/ LTE Band4/66:≤5dBi
- ❒WCDMA Band5/ LTE Band5:≤6.1dBi
- ❒LTE Band12:≤5.61dBi
- ❒LTE Band13:≤5.93dBi
- ❒LTE Band71:≤5.45dBi

The host product shall be properly labelled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:
“Contains IC: 10224A-20193EG61NA” or “where: 10224A-20193EG61NA is the module’s certification number”.
Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.
L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:
"Contient IC: 10224A-20193EG61NA " ou "où: 10224A-20193EG61NA est le numéro de certification du module".

2 Product Concept

2.1. General Description

EG61-NAmodule is an embedded 4G wireless communication module with receive diversity. It supportsLTE-FDD/WCDMA wireless communication, andprovides data connectivity on LTE-FDD,HSPA+, HSDPA, HSUPA, WCDMAnetworks. It can also provide voice functionality[1)]to meet customers' specific application demands. The following table shows the frequency bands of EG61-NA module.

Table 1: Frequency Bands of EG61-NA Module

Module	LTE Bands (with Rx-diversity)	WCDMA (with Rx-diversity)	GSM	GNSS
EG61-NA	FDD: B2/B4/B5/B12/B13/B66/ B71	B2/B4/B5	Not supported	GPS, GLONASS, BeiDou/Galileo, QZSS

With a compact profile of 31.0mm ×25.0mm ×2.3mm, EG61-NA can meet almost all requirements for M2M applications such as automotive, smart metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EG61-NA is an SMD type module which can be embedded into applications through its 106 LGA pads.

EG61-NA is integrated with internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for customers to use these internet service protocols easily.

2.2. Key Features

The following table describes the detailed features of EG61-NA module.

Table 2: Key Features of EG61-NA Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands
LTE Features	Support up to non-CA Cat 1 FDD Support 1.4MHz~20MHz RF bandwidth Support MIMO in DL direction LTE-FDD: Max 10Mbps (DL)/5Mbps (UL)
UMTS Features	Support 3GPP R8 HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation HSDPA: Max 7.2Mbps (DL) HSUPA: Max 5.76Mbps (UL) WCDMA: Max 384Kbps (DL)/384Kbps (UL)
Internet Protocol Features	SupportTCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/CMUX*/HTTPS*/ SMTP*/MMS*/FTPS*/SMTPS*/SSL*/FILE* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIMInterfaces	Support 1.8V and 3.0V (U)SIM cards
Audio Features	Support one digital audio interface: PCM interface WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave mode, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave only);the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission,GNSS NMEA sentences output,software debugging, firmware upgrade and voice over USB* Support USB serial drivers for: Windows 7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1~4.14, Android 4.x/5.x/6.x/7.x/8.x, etc.

UART Interface	**Main UART:** Used for AT command communication and data transmission Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console and log output 115200bps baud rate
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NETLIGHTpin for network activitystatusindication
Antenna Interface	Including main antenna interface (ANT_MAIN), Rx-diversity antenna (ANT_DIV) interface and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (31.0±0.15)mm × (25.0±0.15)mm × (2.3±0.2)mm Package: LGA Weight: TBD
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EG61-NA and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

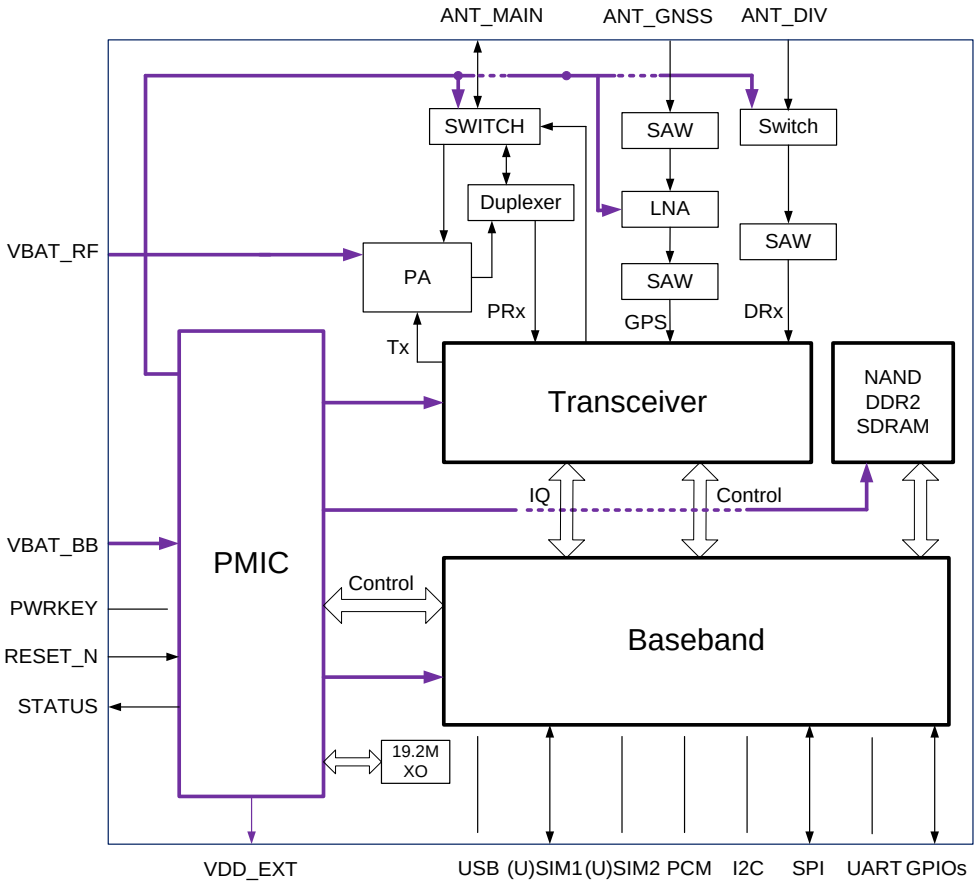


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications conveniently with EG61-NA, Quectel supplies anevaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

EG61-NAis equipped with 62-pin 1.1mm pitch SMT pads plus 44-pin ground/reserved pads that can be connected to customers' cellular application platforms. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIMinterfaces
- USB interface
- UART interfaces
- PCMand I2C interfaces
- SPI interface
- Statusindication

3.2. Pin Assignment

The following figure shows the pin assignment of EG61-NA module.

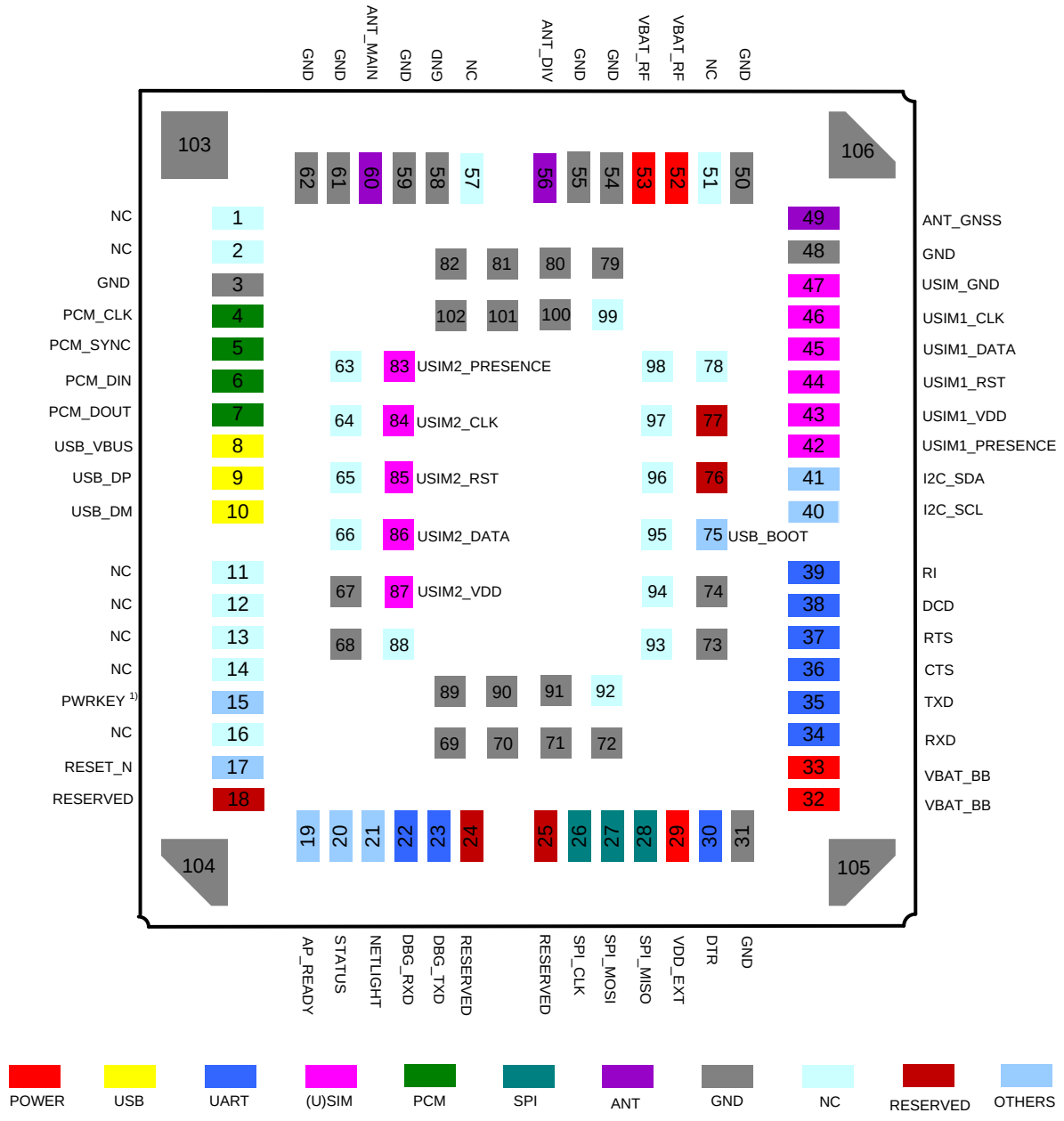


Figure 2: Pin Assignment (Top View)

NOTES

1. [1)]PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
2. Keep all RESERVEDpins and unused pins unconnected.
3. GND pads should be connected to ground in the design.

3.3. Pin Description

The following tables show the pin definition and description of EG61-NA.

Table 3: IO Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
OD	Open drain
PI	Power input
PO	Power output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	52,53	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a transmitting burst.

VDD_EXT	29	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~106		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turnon/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	17	DI	Reset signal of the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	Pull-up to 1.8V internally. Activelow. If unused,keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module operation status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
NETLIGHT	21	DO	Indicate the module's network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	PI	USB detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	Typical:5.0V If unused, keep it open.
USB_DP	9	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
USB_DM	10	IO	USB differential data bus (-)	Compliant with USB 2.0 standard	Require differential impedance of 90Ω.

				specification.	
(U)SIMInterfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	47		Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM1_VDD	43	PO	Power supply for (U)SIMcard	**For 1.8V(U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V(U)SIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM1_DATA	45	IO	Data signal of (U)SIMcard	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM1_CLK	46	DO	Clock signal of (U)SIMcard	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM1_RST	44	DO	Reset signal of (U)SIMcard	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	

USIM1_ PRESENCE	42	DI	(U)SIMcard insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USIM2_VDD	87	PO	Power supply for (U)SIMcard	**For 1.8V(U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V(U)SIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM2_DATA	86	IO	Data signal of (U)SIMcard	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM2_CLK	84	DO	Clock signal of (U)SIMcard	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM2_RST	85	DO	Reset signal of (U)SIMcard	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM2_ PRESENCE	83	DI	(U)SIMcard insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Main UART Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	39	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DCD	38	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
CTS	36	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RTS	37	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DTR	30	DI	Data terminal ready. Sleep mode control.	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
TXD	35	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RXD	34	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	23	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	22	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	6	DI	PCM data input	V_{IL}min=-0.3V	1.8V power domain.

				V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	If unused, keep it open.
PCM_DOUT	7	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	5	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	4	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.

I2C Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	OD	I2C serial clock. Used for external codec		An external pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data. Used for external codec		An external pull-up resistor is required. 1.8V only. If unused, keep it open.

SPI Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_CLK	26	DO	Clock signal of SPI interface	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SPI_MOSI	27	DO	Master output slave input of SPI interface	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.

SPI_MISO	28	DI	Master input slave output of SPI interface	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	49	AI	GNSS antenna pad		50Ω impedance. If unused, keep it open.
ANT_DIV	56	AI	Receive diversity antenna pad		50Ω impedance. If unused, keep it open.
ANT_MAIN	60	IO	Main antenna pad		50Ω impedance. If unused, keep it open.
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AP_READY	19	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USB_BOOT	75	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NC	1, 2, 11~14, 16, 51,57, 63~66, 78, 88, 92~99		NC		Keep these pins unconnected.
RESERVED	18, 24,25 76, 77		Reserved		Keep these pins unconnected.

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module hasregistered on network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network settingand data transfer rate.
Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

EG61-NA is able to reduce its current consumption to a minimum value during the sleep mode. The following sectionsdescribe the power saving procedures of EG61-NA module.

3.5.1.1. UART Application

If the host communicates with the module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCLK=1**commandto enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

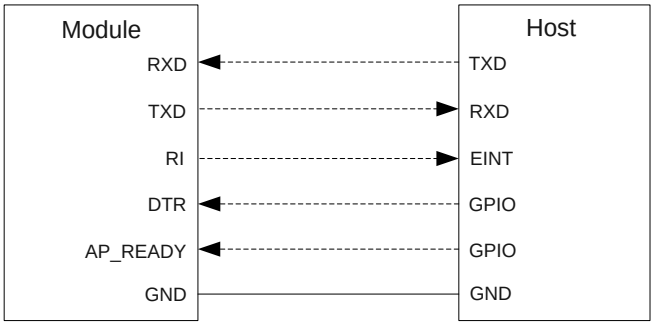


Figure 3: Sleep Mode Application via UART

Driving the host DTR to low level will wake up the module.

- When EG61-NA has a URC to report, RI signal will wake up the host. Refer to ***Chapter 3.16*** for details about RI behavior.
- AP_READY will detect the sleep state of host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"***commandfor details.

NOTE

"*" means under development.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter into sleep mode.

- Execute **AT+QSCLK=1**commandto enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

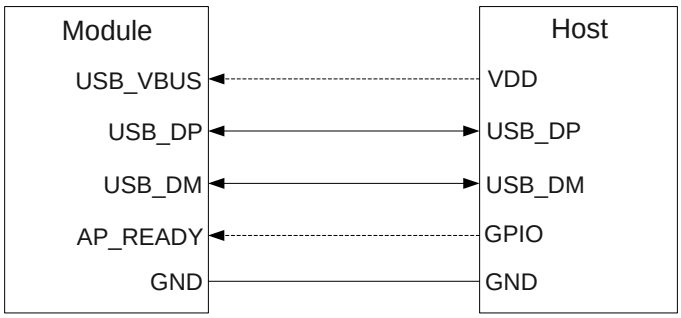


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EG61-NAthrough USB will wake up the module.
- When EG61-NAhas a URC to report, the module will send remote wake-up signals via USB busso as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are threepreconditions to let the module enter into the sleep mode.

- Execute **AT+QSCLK=1**commandto enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

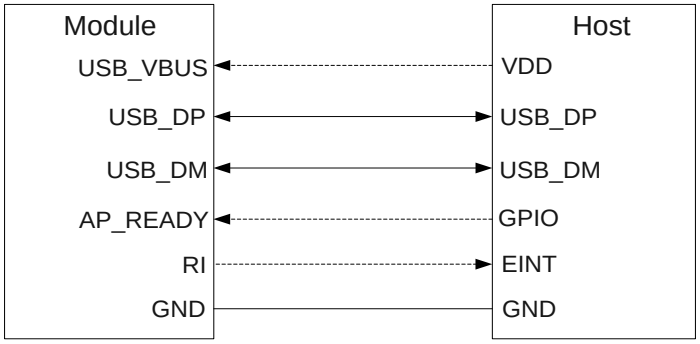


Figure 5: Sleep Mode Application with RI

- Sending data to EG61-NAthrough USB will wake up the module.
- When EG61-NAhas a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected with an externalcontrol circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1**commandto enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

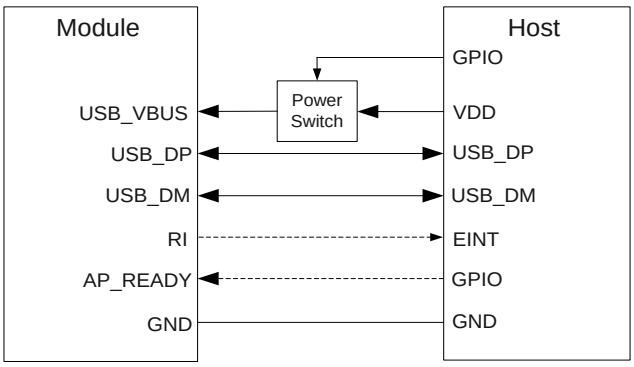


Figure 6: Sleep Mode Application without Suspend Function

Switching onthe power switch tosupply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.Refer to ***document [1]*** for more details about EG61-NA power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set viathe following ways.

Hardware:

The W_DISABLE# pin is pulled up by default.Driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUNcommandprovides the choice of functionality levels as shown below:

- **AT+CFUN=0:** Minimum functionality mode.Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command and this command is under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EG61-NA provides four VBAT pins for connection with anexternal power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module'sRF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52,53	Power supply for module's RF part.	3.3	3.8	4.3	V
VBAT_BB	32,33	Power supply for module's baseband part.	3.3	3.8	4.3	V
GND	3, 31, 48,50, 54, 55,58, 59, 61,62, 67~74, 79~82,89~91, 100~106	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3Vto4.3V. Please make sure thatthe input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network.The voltage drop will be less in 3G and 4G networks.

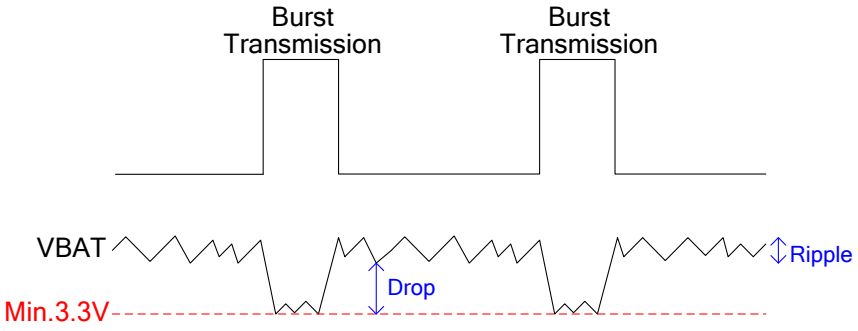


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR(ESR=0.7Ω) should be used, and amulti-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to usethree ceramic capacitors (100nF, 33pF, 10pF)for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, andthe width of VBAT_RF trace should be no less than 2mm.In principle, the longerthe VBAT trace is, the wider it will be.

In addition, in order to get a stable power source,it is recommended to use a TVS diode of Model WS4.5D3HV. The following figure shows the star structure of the power supply.

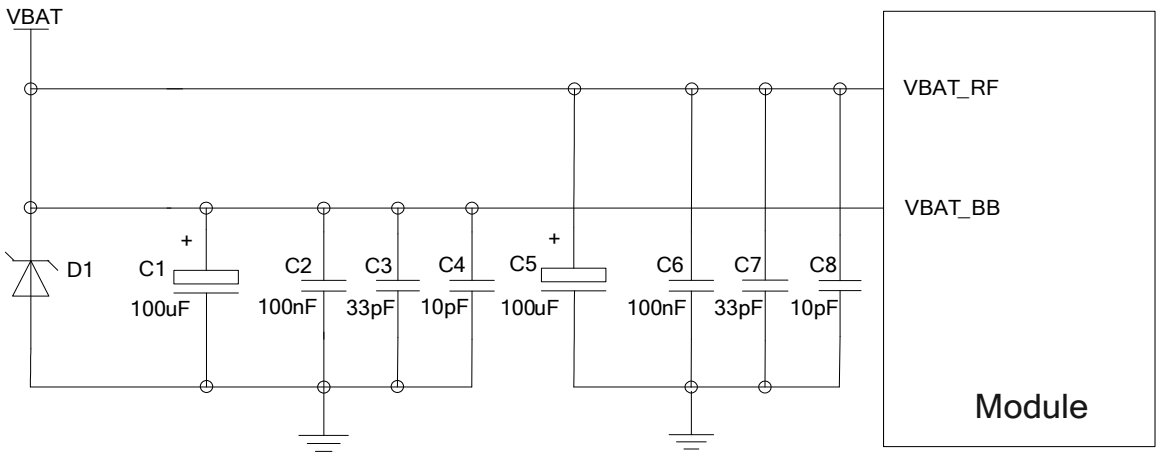


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, asthe performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be usedto supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typicaloutput ofthe power supply is about 3.8V and the maximum load current is 3A.

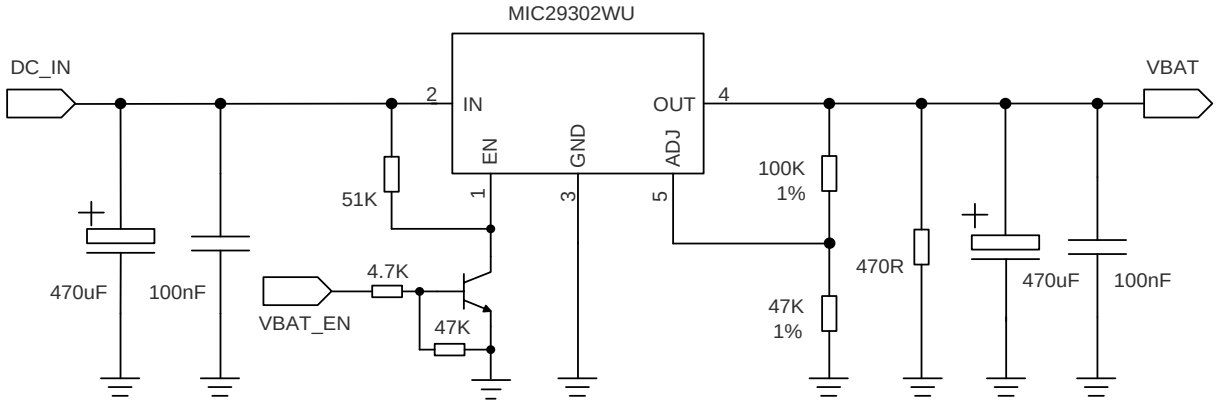


Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shutdown by PWRKEY or AT command, the power supply can be cut off.

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.7. Turn-on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definitionof PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EG61-NA is in powerdownmode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY.After STATUS pin outputting a high level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

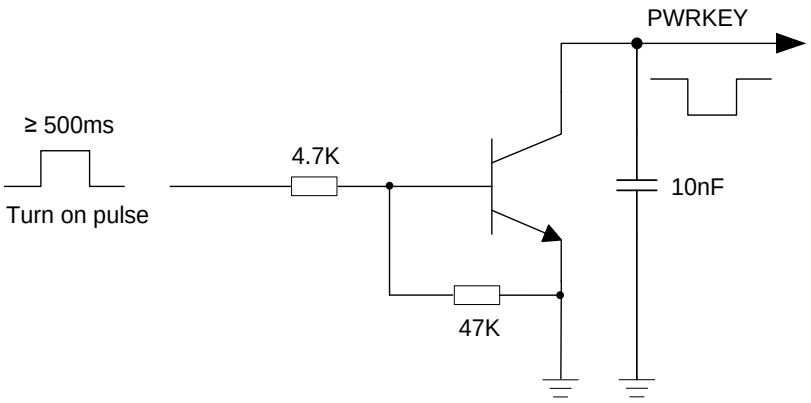


Figure 10: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, aTVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shownin the following figure.

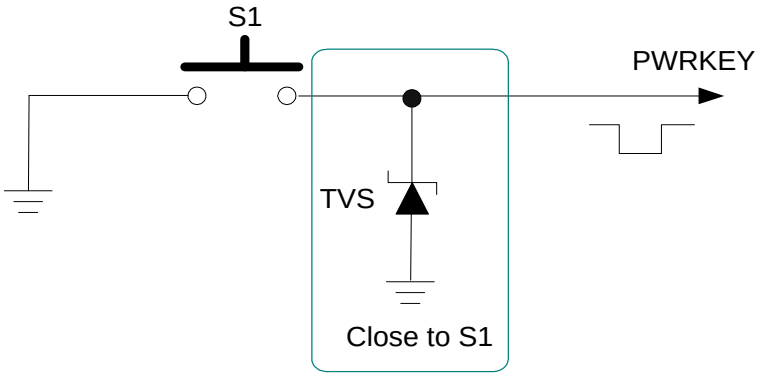


Figure 11: Turn on the Module Using Button

The turn on scenario is illustrated in the following figure.

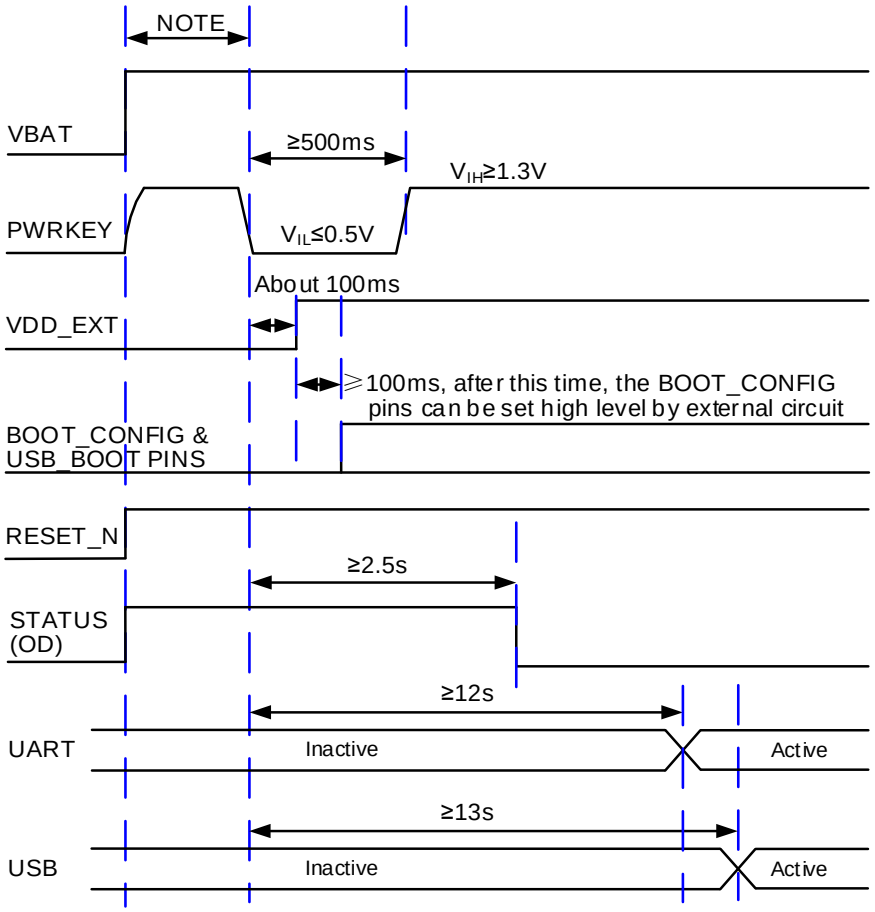


Figure 12: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin, and the time between them is no less than 30ms.
2. The recommended pull-up level range is 1.3V~2.1V if a pull-up circuit is added on PWRKEY pin.

3.7.2. Turn off Module

Either of the following methodscan be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD**command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated inthe following figure.

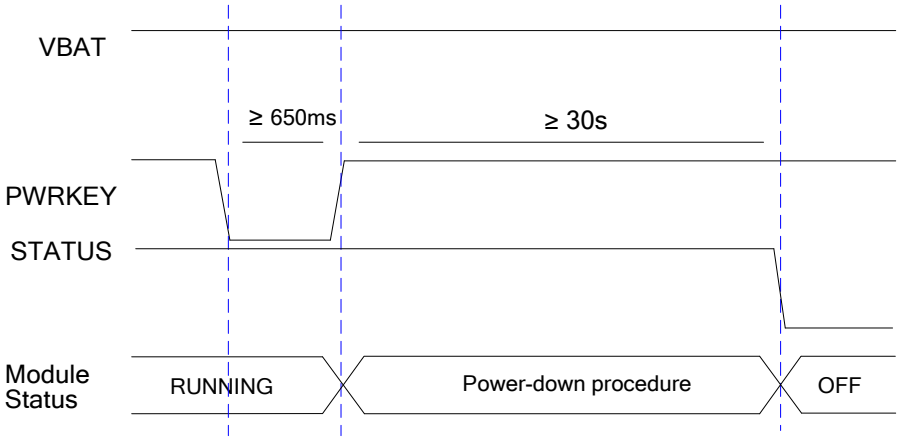


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD**commandto turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to***document [2]*** for details about the **AT+QPOWD**command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise the module will be turned on again after successful turn-off.

3.8. Reset the Module

The RESET_N pin can be used to reset the module.The module can be reset by driving RESET_N to a low level voltage for 150ms~460ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

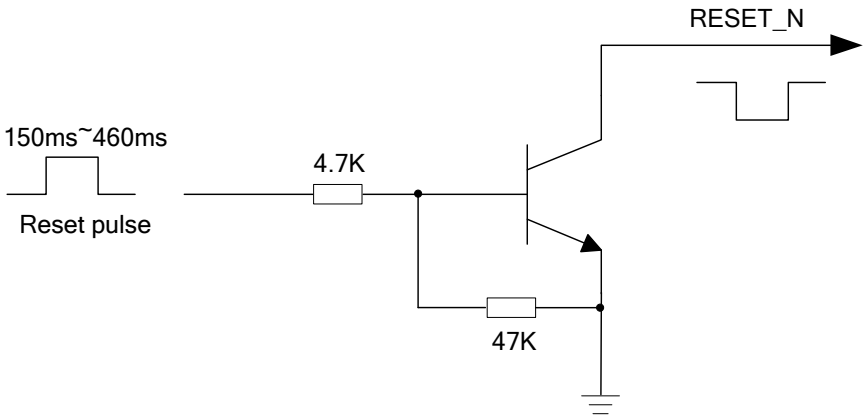


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

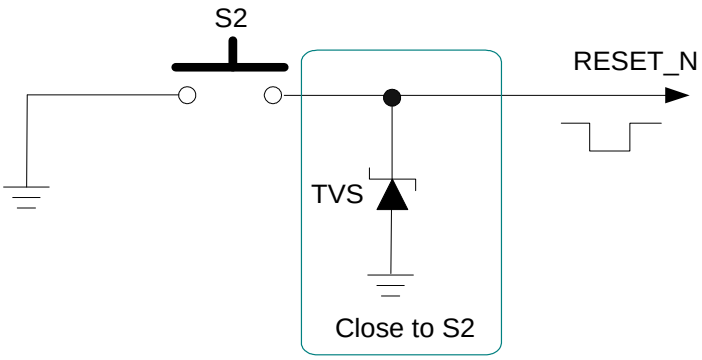


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated inthe following figure.

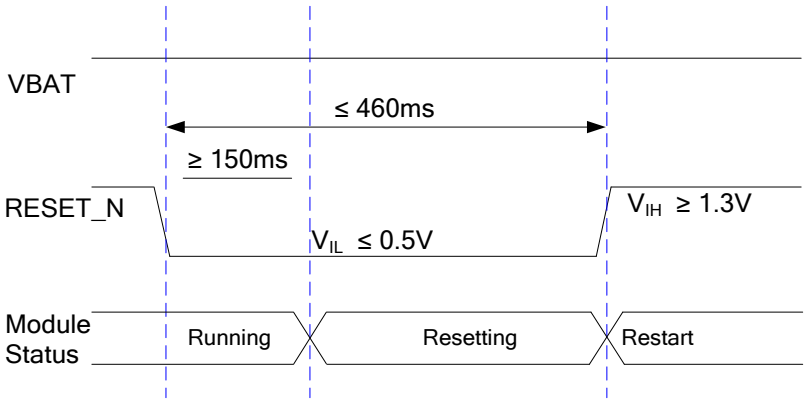


Figure 16: Timing of Resetting Module

NOTES

1. RESET_N is only used when the module fails to be shut down via **AT+QPOWD** command and the PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interfaces

EG61-NAprovides two (U)SIMinterfaces, andonly one (U)SIMcard can work at a time.The (U)SIM1 and (U)SIM2cardscan be switched by **AT+QDSIM***command.For more details, please refer to ***document [2]***.

The(U)SIMinterfacescircuitrymeet ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIMcards are supported.

Table 9: Pin Definition of (U)SIMInterfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	Power supply for (U)SIM1 card	Either 1.8V or 3.0V is supported by the module automatically.
USIM1_DATA	45	IO	Data signal of (U)SIM1 card	
USIM1_CLK	46	DO	Clock signal of (U)SIM1card	
USIM1_RST	44	DO	Reset signal of (U)SIM1 card	
USIM1_ PRESENCE	42	DI	(U)SIM1 card insertion detection	

USIM_GND	47		Specified ground for (U)SIMcard	
USIM2_VDD	87	PO	Power supply for (U)SIM2 card	Either 1.8V or 3.0V is supported by the module automatically.
USIM2_DATA	86	IO	Data signal of (U)SIM2 card	
USIM2_CLK	84	DO	Clock signal of (U)SIM2 card	
USIM2_RST	85	DO	Reset signal of (U)SIM2 card	
USIM2_ PRESENCE	83	DI	(U)SIM2 card insertion detection	

EG61-NA supports (U)SIMcard hot-plug via the USIM_PRESENCE (USIM1_PRESENCE/USIM2_PRESENCE) pin. The functionsupports low level and high level detections, andis disabled by default. Pleaserefer to ***document [2]*** about **AT+QSIMDET**command for details.

The following figure shows a reference design for (U)SIM interface with an8-pin (U)SIMcard connector.

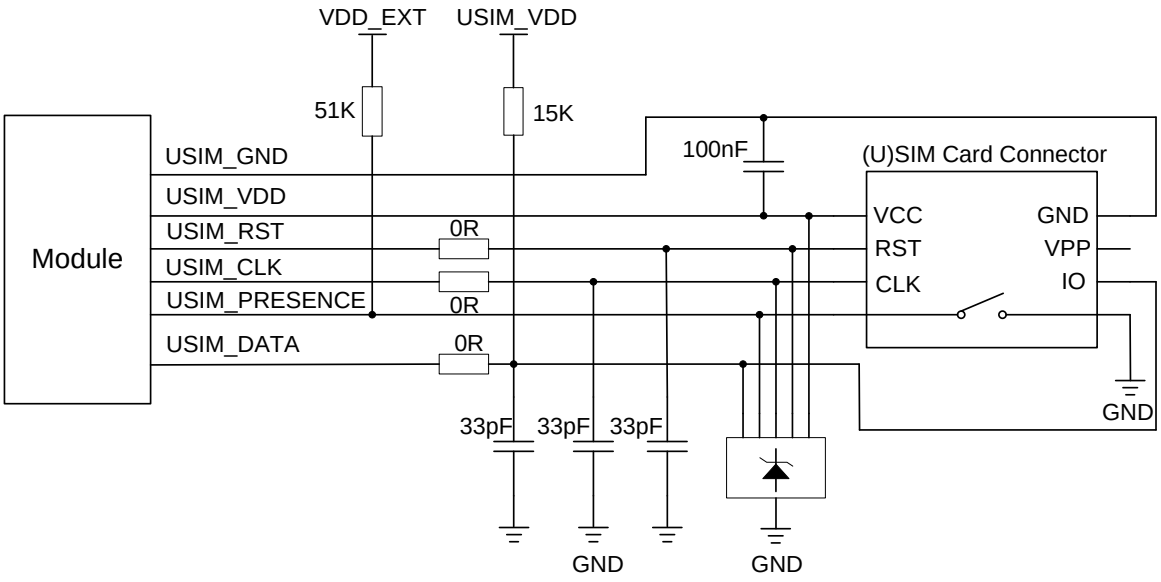


Figure 17: Reference Circuitof (U)SIMInterface with an 8-Pin (U)SIMCard Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. Areference circuit of (U)SIM interface with a 6-pin (U)SIMcard connector is illustrated inthe following figure.

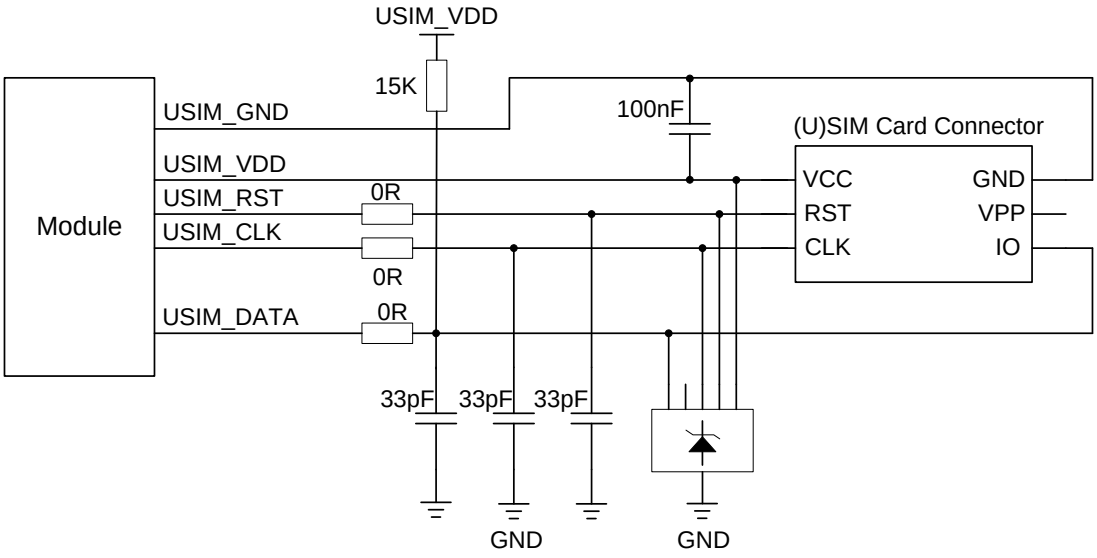


Figure 18: Reference Circuitof (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground trace between the module and the (U)SIMcard connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1uF, and place it as close to (U)SIM card connector as possible.If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15pF. The 0Ω resistors should be added in series between the module and the (U)SIM card to facilitatedebugging. The 33pF capacitors are used for filtering interference of GSM900MHz.Please note that the (U)SIM peripheral circuit should be close to the (U)SIMcard connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

NOTE

"*" means under development.

3.10. USB Interface

EG61-NA contains one integrated Universal Serial Bus (USB) interfacewhich complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output,software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	IO	USB differential data bus (+)	Require differential impedance of 90Ω.
USB_DM	10	IO	USB differential data bus (-)	Require differential impedance of 90Ω.
USB_VBUS	8	PI	USB detection	Typically 5.0V
GND	3		Ground	

More details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' design. The following figure shows areference circuit of USB interface.

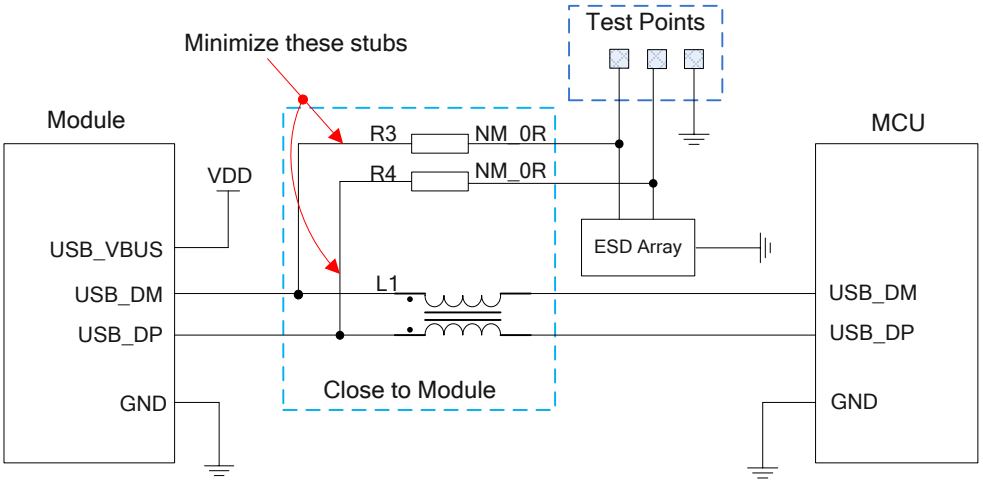


Figure 19: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and customer'sMCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should beadded in series between the module and the test points so as to facilitate debugging, and the resistors are
not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. Theextra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding onnot only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection component on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTES

1. EG61-NA module can only be used as a slave device.
2. "*" means under development.

3.11. UART Interfaces

The module provides two UART interfaces: the main UART interface and thedebug UART interface. The following shows their features.

- The main UART interface supports 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps and 921600bpsbaud rates, and the default is 115200bps. The interface can be used for data transmission and AT command communication.
- The debug UART interface supports 115200bpsbaud rate. It is used forLinux console and log output.

The following tables show the pin definition of the two UART interfaces.

Table 11: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	39	DO	Ring indicator	
DCD	38	DO	Data carrier detection	
CTS	36	DO	Clear to send	
RTS	37	DI	Request to send	1.8V power domain
DTR	30	DI	Sleep mode control	
TXD	35	DO	Transmit data	
RXD	34	DI	Receive data	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Transmit data	1.8V power domain
DBG_RXD	22	DI	Receive data	1.8V power domain

The logic levels are described in the following table.

Table 13:Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interface. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows areference design.

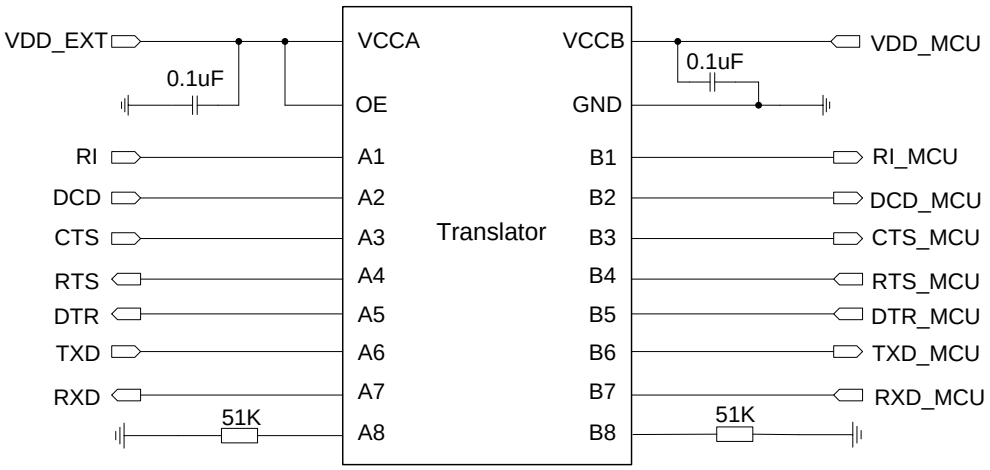


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com formore information.

Another example with transistor translation circuit is shown as below. Thecircuitdesign of dotted line section can refer to the circuitdesign of solid linesection, in terms of both module input and output circuit design. Please pay attention to the direction of connection.

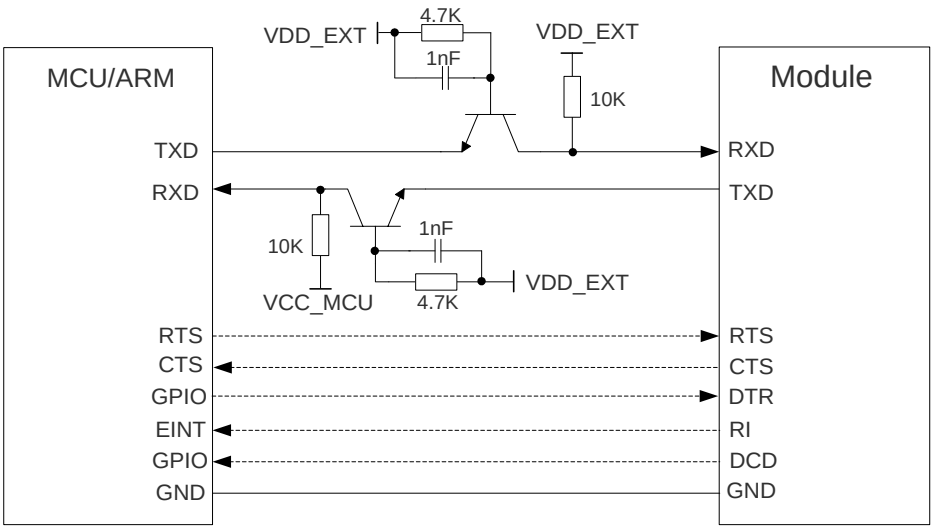


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.12. PCM and I2C Interfaces

EG61-NA provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC.

EG61-NA supports 16-bit linear data format. The following figures show theprimary mode's timing relationship with 8KHz PCM_SYNC and 2048KHz PCM_CLK, as well asthe auxiliary mode's timing relationship with 8KHz PCM_SYNC and 256KHz PCM_CLK.

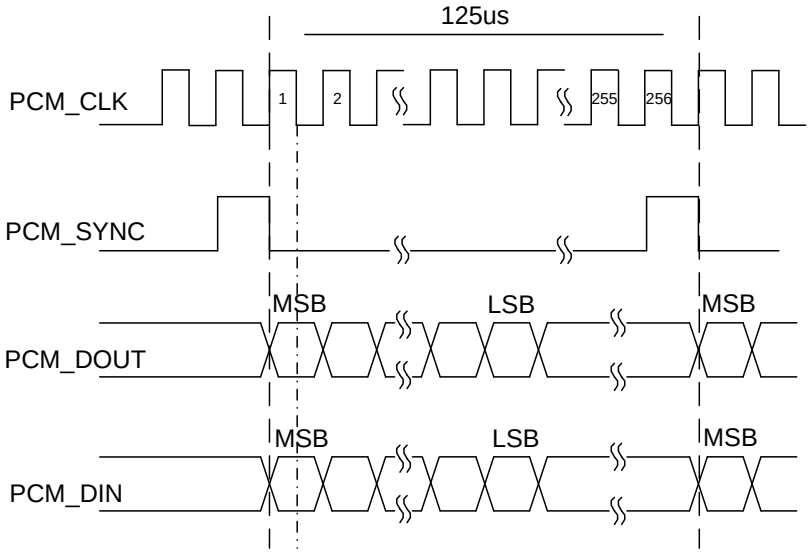


Figure 22: Primary Mode Timing

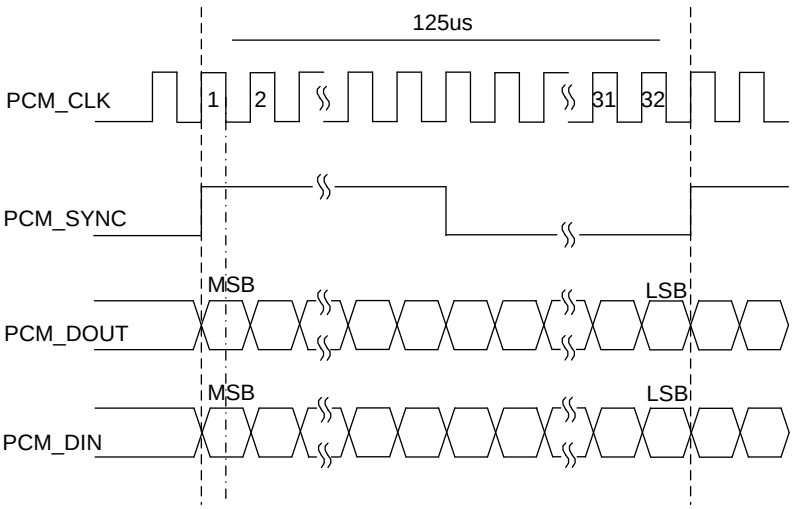


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	6	DI	PCM data input	1.8V power domain
PCM_DOUT	7	DO	PCM data output	1.8V power domain
PCM_SYNC	5	IO	PCM data frame synchronization signal	1.8V power domain
PCM_CLK	4	IO	PCM data bit clock	1.8V power domain
I2C_SCL	40	OD	I2C serial clock	Require an external pull-up to 1.8V
I2C_SDA	41	OD	I2C serial data	Require an external pull-up to 1.8V

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronizationformat with 2048KHzPCM_CLK and 8KHz PCM_SYNC.Please refer to ***document [2]*** about**AT+QDAI**command for details.

The following figure shows areference design of PCM interface with external codec IC.

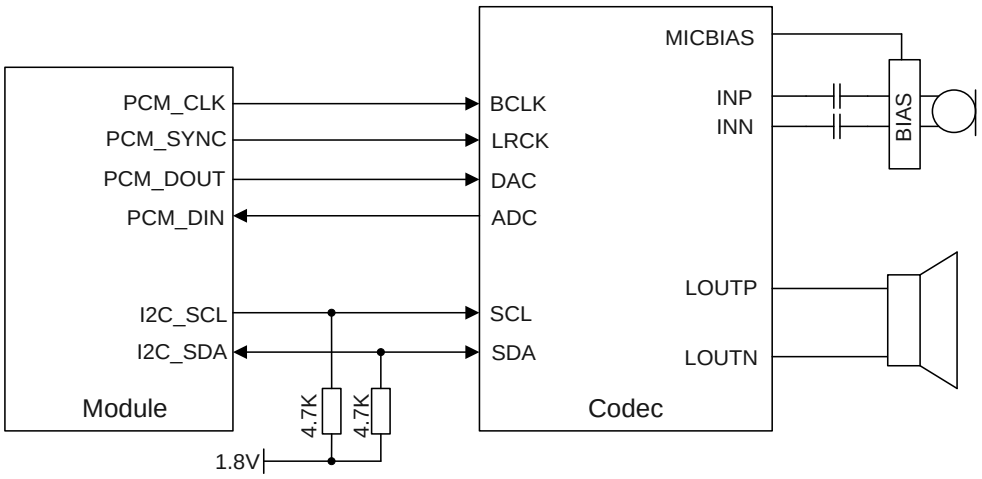


Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. EG61-NA works as a master device pertaining to I2C interface.

3.13. SPI Interface

SPI interface of EG61-NAacts asthe master only. It provides a duplex, synchronous and serial communication link with the peripheral devices. It isdedicated to one-to-one connection, withoutchip select.Its operation voltage is 1.8V with clock rates up to 50MHz.

The following table shows the pin definition of SPI interface.

Table 15: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	Clock signal of SPI interface	1.8V power domain
SPI_MOSI	27	DO	Master output slave input of SPI interface	1.8V power domain
SPI_MISO	28	DI	Master input slave output of SPI interface	1.8V power domain

The following figure shows areference design of SPI interface with peripherals.

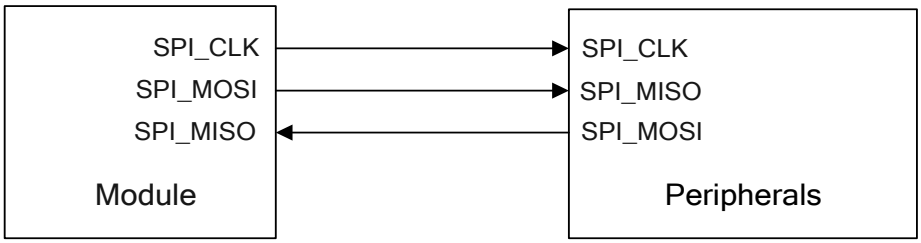


Figure 25: Reference Circuit of SPI Interface with Peripherals

3.14. Network Status Indication

The module provides one network indication pin: NETLIGHT. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network status.

Table 16: Pin Definition of Network StatusIndicator

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module’snetwork activity status	1.8V power domain

Table 17: Working State of the Network Status Indicator

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

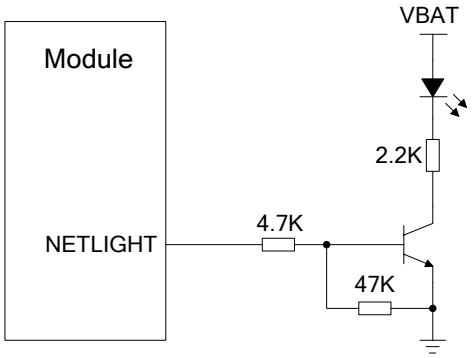


Figure 26: Reference Circuit of the Network Status Indicator

3.15. STATUS

The STATUS pin is set as the module's operation status indicator. It will output high level when the module is powered on. The following table describes the pin definition of STATUS.

Table 18: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8V power domain

A reference circuit is shown as below.

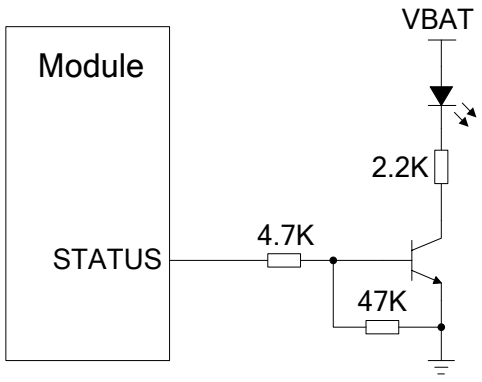


Figure 27: Reference Circuits of STATUS

3.16. Behaviors of RI

AT+QCFG="risignaltype","physical"command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior ofRI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behavior can be configured flexibly. The default behaviors of the RI are shown as below.

Table 19: Default Behaviors of RI

State	Response
Idle	RI keeps athigh level
URC	RI outputs 120ms low pulse when a new URC returns

The default RI behaviorscan be changed by **AT+QCFG="urc/ri/ring"**command.Please refer to ***document [2]*** for details.

3.17. USB_BOOT Interface

EC61-NA provides a USB_BOOT pin. Customers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 20: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. It is recommended to reserve the pin as test point.

The following figures show the reference circuit of USB_BOOT interface and timing sequence of Entering into emergency download mode.

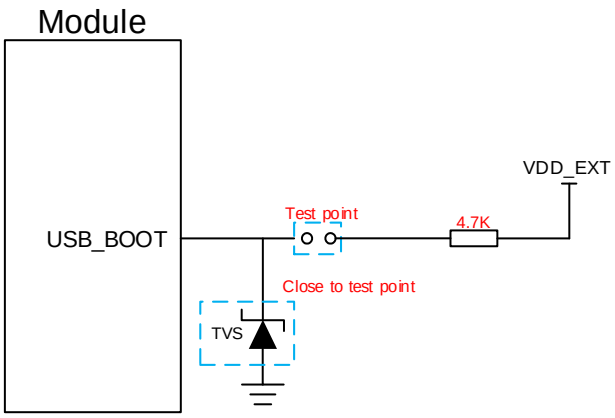


Figure 28: Reference Circuit of USB_BOOT Interface

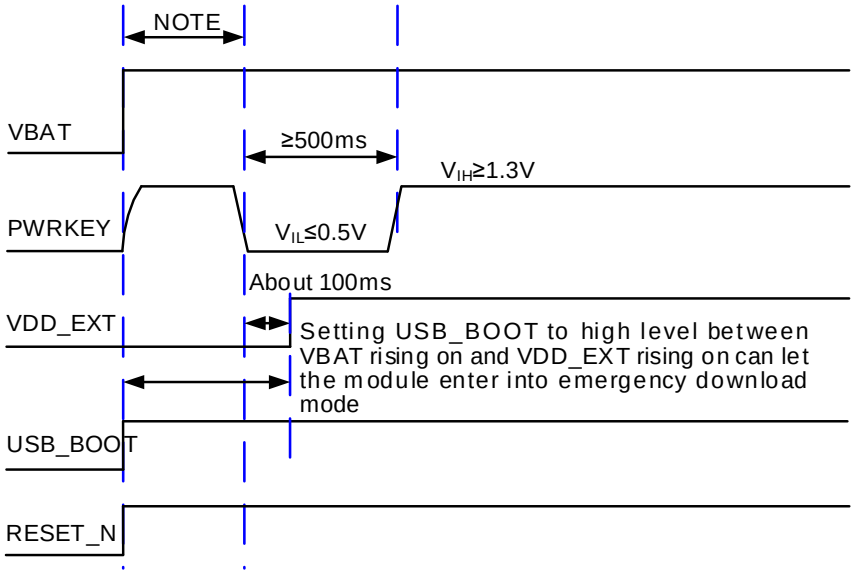


Figure 29: Timing Sequence for Entering into Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin, and the time between themis no less than 30ms.
2. The recommended pull-up level range is 1.3V~2.1V if a pull-up circuit is added on PWRKEY pin.

4 GNSS Receiver

4.1. General Description

EG61-NA includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EG61-NA supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, EG61-NA GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EG61-NA.

Table 21: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-145	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	34.4	s
		XTRA enabled	15.6	s
	Warm start @open sky	Autonomous	28.6	s
		XTRA enabled	2.2	s
	Hot start	Autonomous	2.3	s

	@open sky	XTRA enabled	2.1	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	4	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers' design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50Ω.

Please refer to ***Chapter 5*** for GNSS reference design and antenna installation information.

5 Antenna Interfaces

EG61-NA antenna interfaces include a main antenna interface andanRx-diversity antennainterface which is used toresist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface which is only supported on EG61-NA.The impedance of the antenna port is 50Ω.

5.1. Main/Rx-diversityAntenna Interfaces

5.1.1. Pin Definition

The pin definitionof main antenna and Rx-diversityantenna interfaces is shown below.

Table 22: Pin Definition of RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna pad	50Ωimpedance
ANT_DIV	49	AI	Receive diversityantenna pad	50Ωimpedance
ANT_DIV	56	AI	Receive diversity antenna pad	50Ω impedance

5.1.2. Operating Frequency

Table 23: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE FDD B2	1850~1910	1930~1990	MHz
LTE FDD B4	1710~1755	2110~2155	MHz

LTE FDD B5	824~849	869~894	MHz
LTE FDD B12	699~716	729~746	MHz
LTE FDD B13	777~787	746~756	MHz
LTE-FDDB66	1710~1780	2100~2200	MHz
LTE-FDD B71	663~698	617~652	MHz

5.1.3. Reference Design of RF Antenna Interface

Areference design of ANT_MAIN and ANT_DIVantenna pads is shown as below. Aπ-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

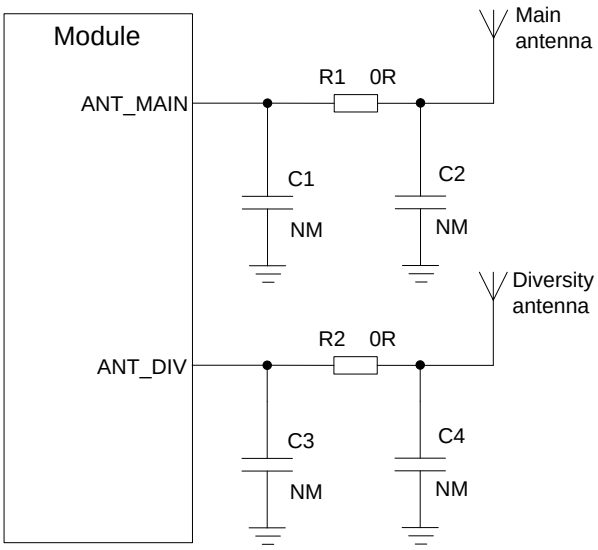


Figure 30: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and theRx-diversityantenna to improve the receiving sensitivity.
2. ANT_DIV function is enabledby default.**AT+QCFG="diversity",0**command can be used to disable receive diversity.
3. Place the π-type matching components (R1/C1/C2, R2/C3/C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The

impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

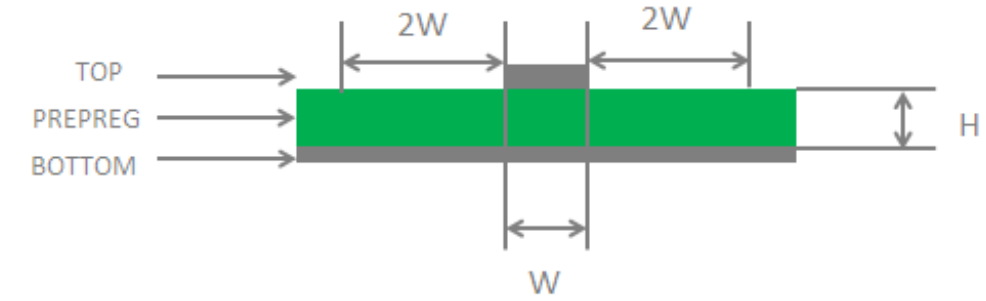


Figure 31: Microstrip Line Design on a 2-layer PCB

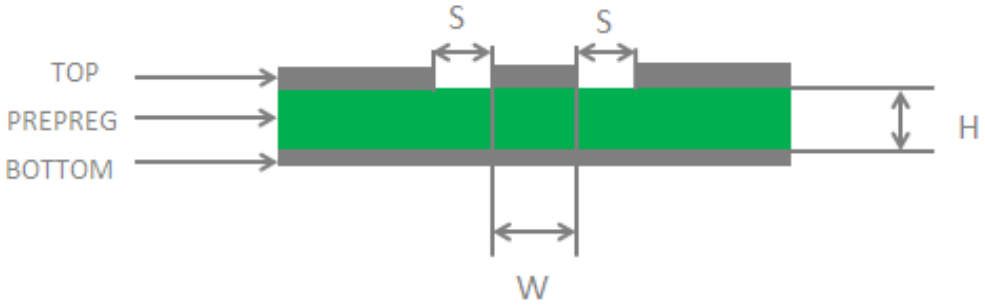


Figure 32: Coplanar Waveguide Line Design on a 2-layer PCB

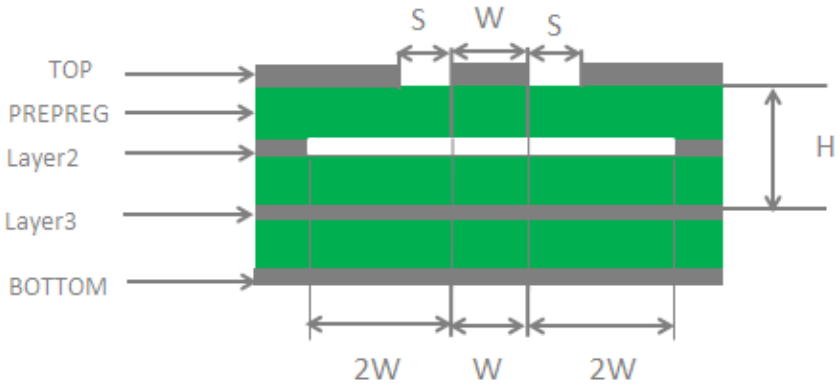


Figure 33: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

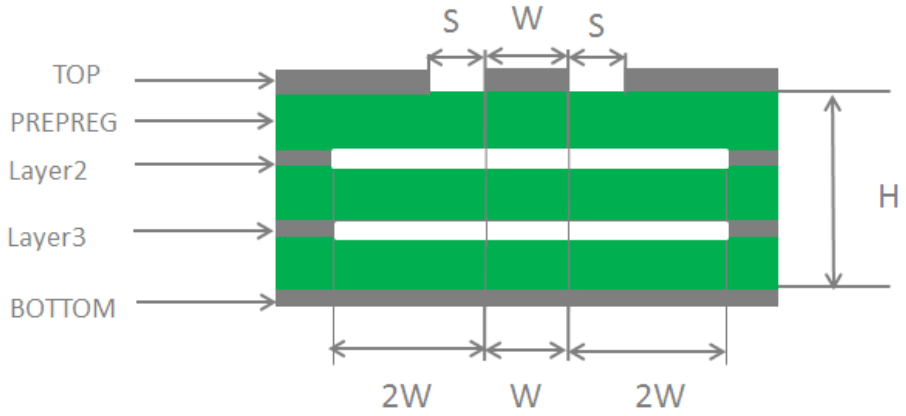


Figure 34: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedanceof RF tracesas 50Ω.
- The GND pins adjacent to RF pins should not bedesigned as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pinsand the RFconnector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground viasaround RF traces and the reference ground could help to improve RF performance. The distance between the ground viasand RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [4]***.

5.2. GNSS Antenna Interface

The GNSS antenna interface is only supported on EG61-NA.The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 24: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna	50Ωimpedance

Table 25: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
Galileo	1575.42±2.046	MHz
BeiDou	1561.098±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

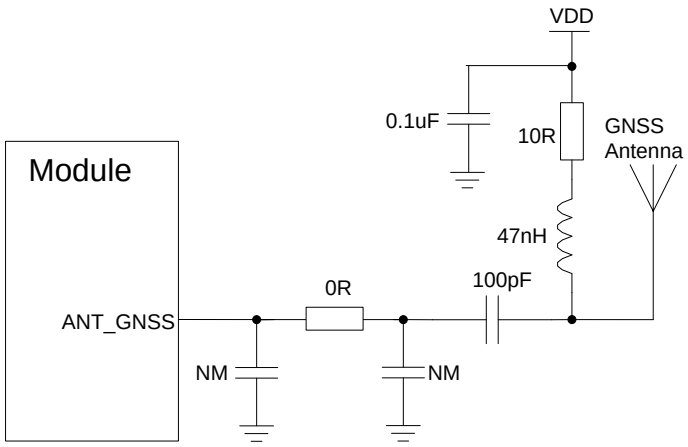


Figure 35: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 26: Antenna Requirements

Type	Requirements
GNSS[1)]	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: < 17dB
WCDMA/LTE	VSWR: ≤2 Efficiency: > 30% Max Input Power: 50 W Input Impedance: 50Ω Cable insertion loss: <1dB (WCDMA B5 LTE B5/B12/B13/B71) Cable Insertion Loss: <1.5dB (WCDMAB2/B4, LTE B2/B4/B66)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

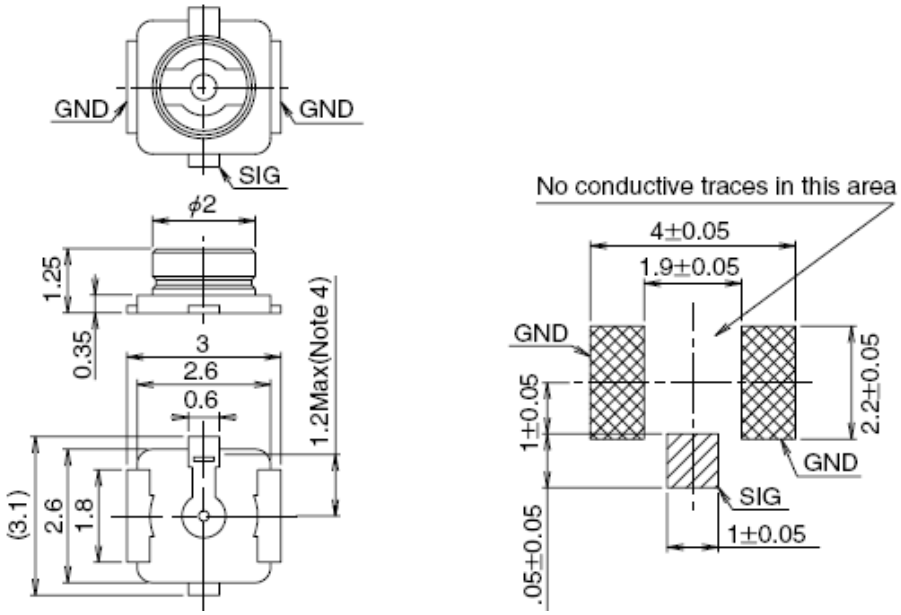


Figure 36: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

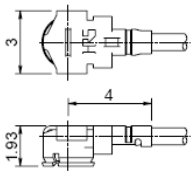
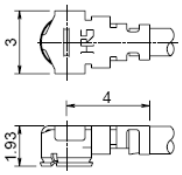
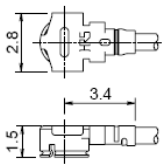
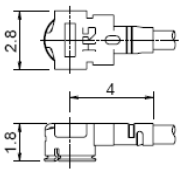
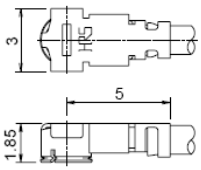
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37:Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

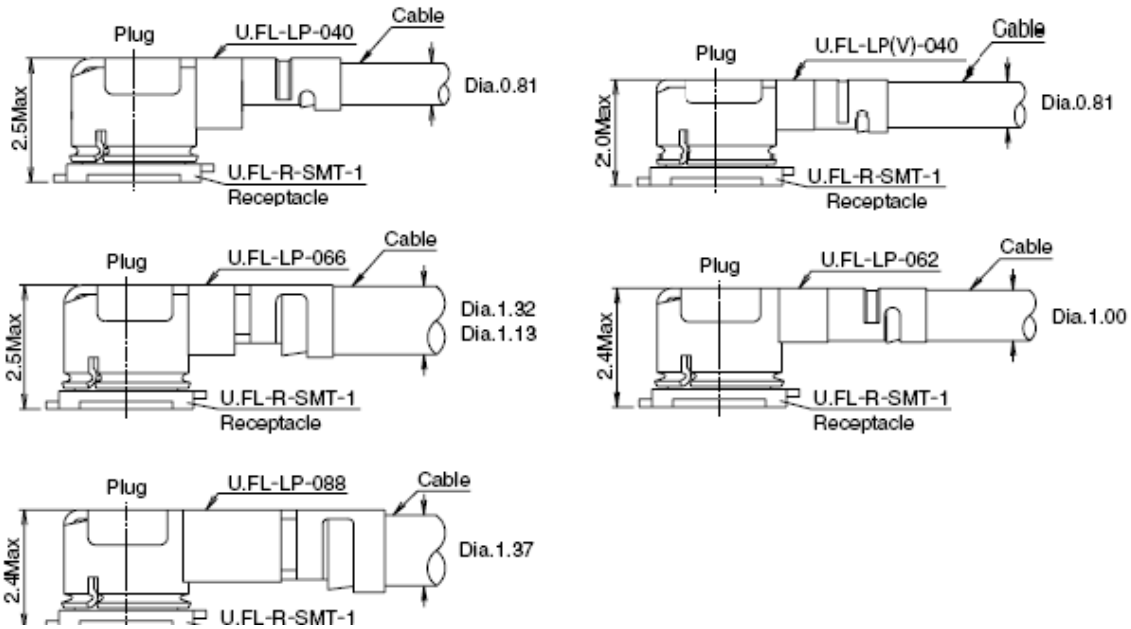


Figure 38:Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and RadioCharacteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 27: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	TBD	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 28: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V

	Voltage drop during burst transmission	Maximum power control level on LTE			400	mV
I_{VBAT}	Peak supply current (during transmissionslot)	Maximum power control level on LTE				A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperaturesare listed in the following table.

Table 29: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range[1)]	-35	+25	+75	ºC
ExtendedTemperatureRange[2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operation temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The values of current consumption are shown below.

Table 30: EG61-NA Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	12	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.646	mA
		WCDMA PF=64 (USB disconnected)	1.483	mA
		WCDMA PF=64 (USB suspend)	1.844	mA
		WCDMA PF=512 (USB disconnected)	0.912	mA
		LTE-FDD PF=64 (USB disconnected)	1.96	mA
		LTE-FDD PF=64 (USB suspend)	2.152	mA
		LTE-FDD PF=256 (USB disconnected)	1.219	mA
	Idle state	WCDMA PF=64 (USB disconnected)	17.225	mA
		WCDMA PF=64 (USB connected)	27.656	mA
		LTE-FDDPF=64 (USB disconnected)	18.09	mA
		LTE-FDDPF=64 (USB connected)	28.768	mA
	WCDMA datatransfer	WCDMA B2 HSDPA@21.69dBm	592.0	mA
		WCDMA B2 HSUPA@21.76dBm	606.0	mA
		WCDMA B4 HSDPA@23.22dBm	604.0	mA
		WCDMA B4 HSUPA@22.49dBm	606.0	mA
		WCDMA B5 HSDPA@23.22dBm	551.0	mA
		WCDMA B5 HSUPA@22.46dBm	546.0	mA
	LTE datatransfer	LTE-FDD B2 @22.89dBm	705.0	mA
		LTE-FDD B4 @22.91dBm	754.0	mA

		LTE-FDD B5 @23.2dBm	602.0	mA
		LTE-FDD B12 @23.0dBm	714.0	mA
		LTE-FDD B13 @23.16dBm	663.0	mA
		LTE-FDD B66 @22.90dBm	746.3	mA
		LTE-FDD B71 @22.93dBm	718.0	mA
	WCDMA voice call	WCDMA B2 @22.96dBm	647.0	mA
		WCDMA B4 @23.35dBm	607.0	mA
		WCDMA B5 @23.36dBm	550.0	mA

Table 31: GNSS Current Consumption of EG61-NA

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	52.765	mA
		Lost state @Passive Antenna	52.306	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	34.547	mA
		Open Sky @Passive Antenna	TBD	mA
		Open Sky @Active Antenna	TBD	mA

6.5. RF Output Power

The following table shows the RF output power of EG61-NA module.

Table 32: RF Output Power

Frequency	Max.	Min.
WCDMA B2/B4/B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2/B4/B5/B12/B13 B66/B71	23dBm±2dB	<-39dBm

6.6. RF Receiving Sensitivity

The following tables show the conducted RF receiving sensitivity of EG61-NA module.

Table 33: EG61-NA Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	-109dBm	-110dBm	/	-104.7dBm
WCDMA B4	-109dBm	-110dBm	/	-106.7dBm
WCDMA B5	-110.5dBm	-110.5dBm	/	-104.7dBm
LTE-FDD B2 (10M)	-97.7	-98.7	-101.7	-94.3dBm
LTE-FDD B4 (10M)	-97.7	-98.2	-100.2	-96.3dBm
LTE-FDD B5 (10M)	-99.7	-99.4	-102.7	-94.3dBm
LTE-FDD B12 (10M)	-98.7	-99.2	-101.7	-93.3dBm
LTE-FDD B13 (10M)	-98.7	-98.9	-102.2	-93.3dBm
LTE-FDD B66 (10M)	-97.7	-98.3	-101.2	-95.8dBm
LTE-FDD B71 (10M)	-99.2	-99	-102.2	-93.5dBm

6.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics.

Table 34: Electrostatic Discharge Characteristics

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±12	KV

ANT_MAIN,ANT_DIV	±8	±12	KV
ANT_GNSS	±6	±10	KV
Other Interfaces	TBD	TBD	KV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or bothof them according to their application structure.

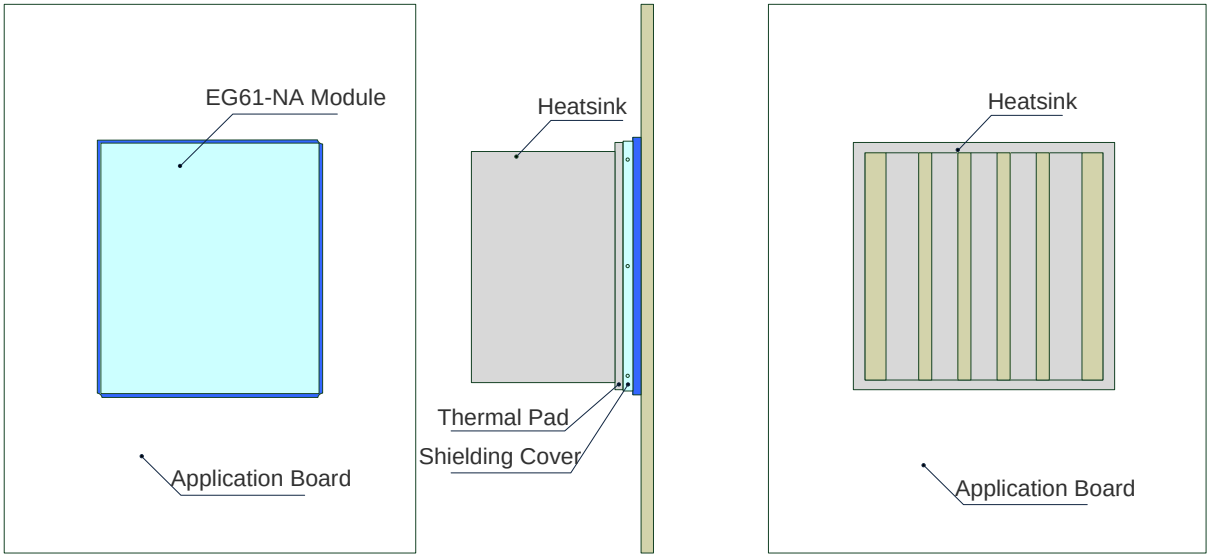


Figure 39: Referenced Heatsink Design (Heatsink at the Top of the Module)

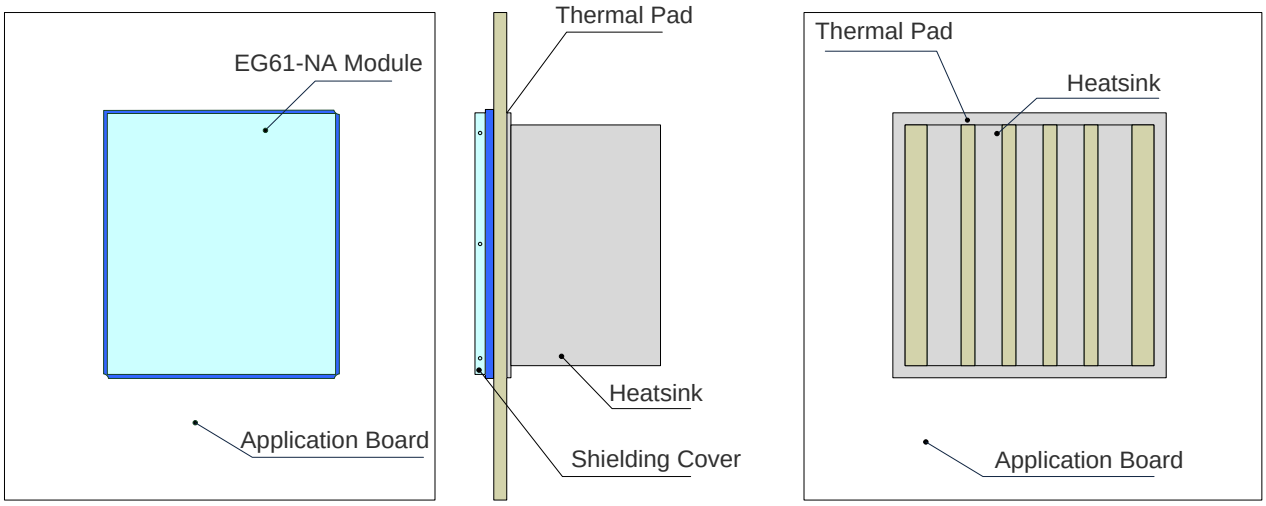


Figure 40: Referenced Heatsink Design (Heatsink at the Bottom of Customers' PCB)

NOTES

1. The module offers the best performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command and get the

maximum BB chip temperature from the first returned value.

2. For more detailed guidelines on thermal design, please refer to ***document [5]***.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module.All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

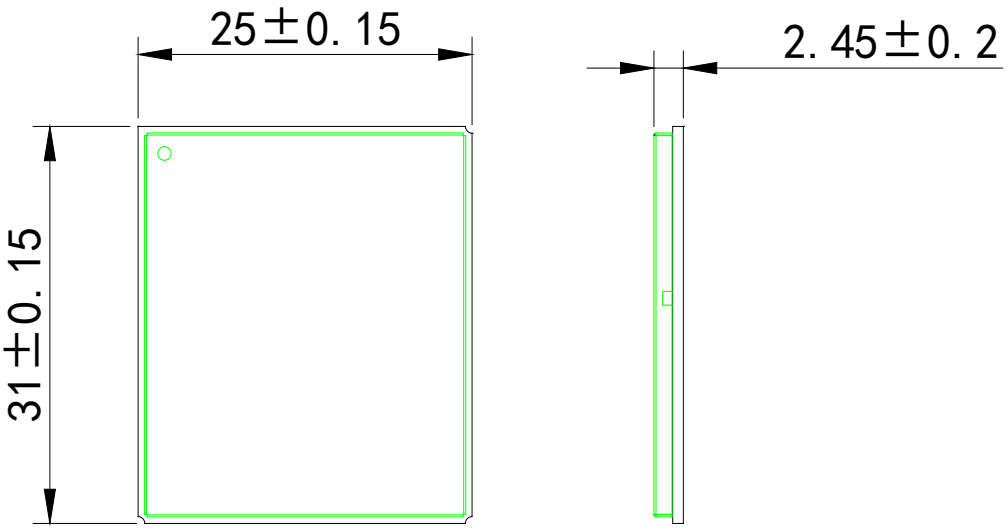


Figure 41: Module Top and Side Dimensions

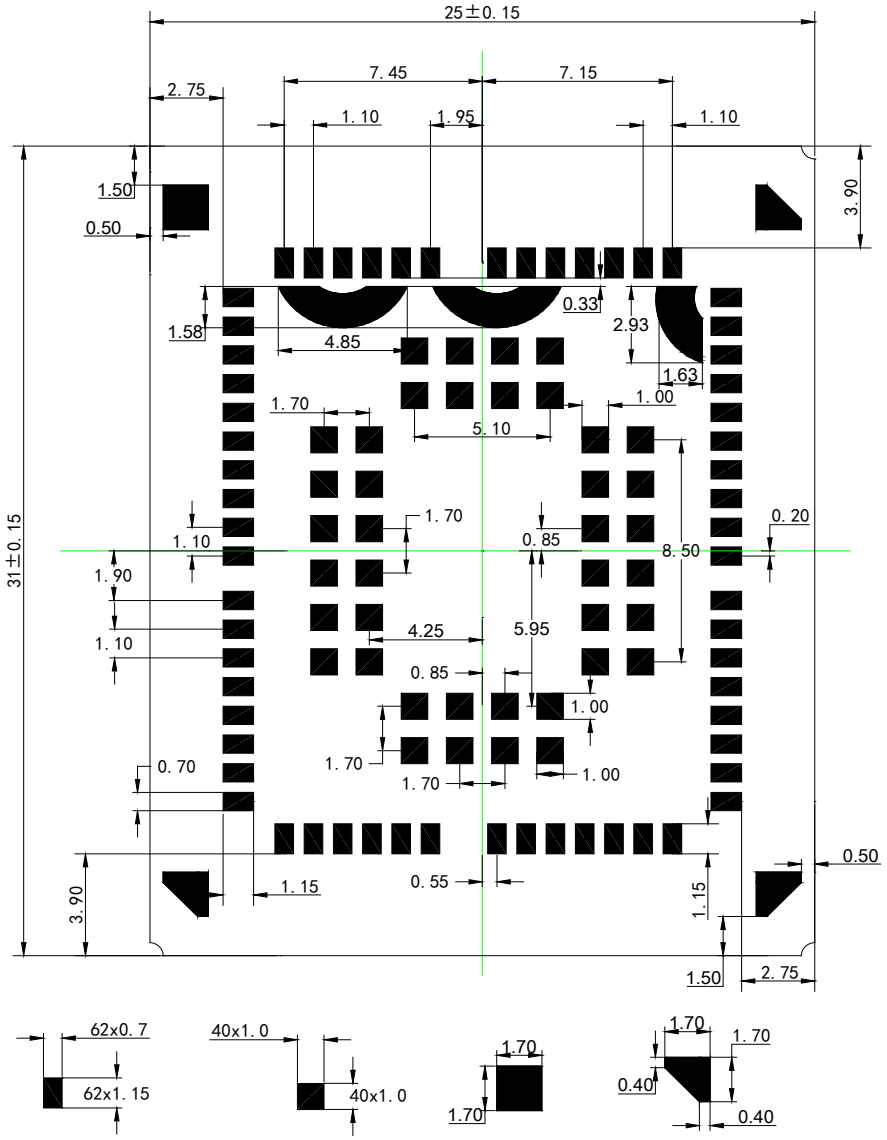


Figure 42: Module Bottom Dimensions (TopView)

7.2. Recommended Footprint

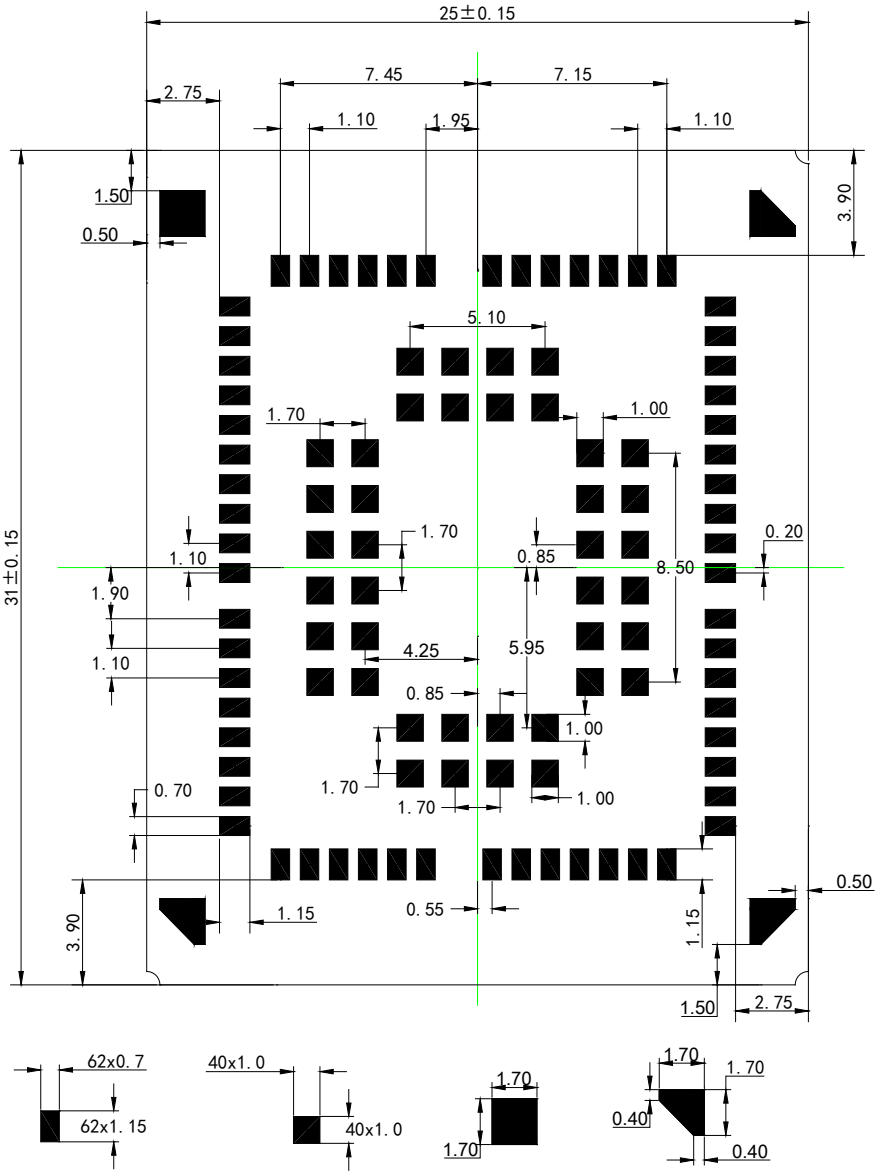


Figure 43: Recommended Footprint (Top View)

NOTE

For easymaintenance of the module, please keep about 3mm between the module and other components in thehost PCB.

7.3. Design Effect Drawings of the Module

Figure 44: Top View of the Module

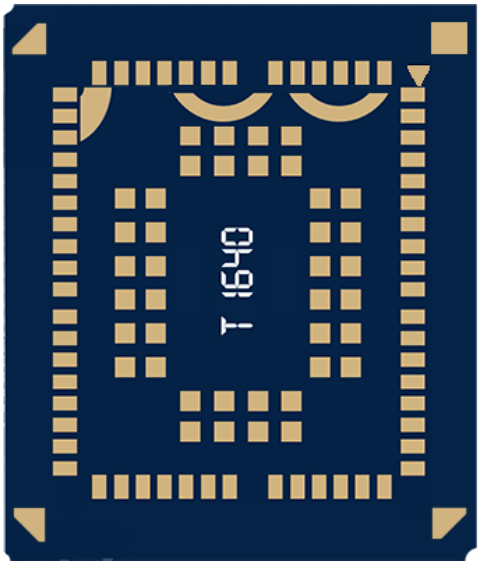


Figure 45: Bottom View of the Module

NOTE

These are design effect drawings of EG61-NA module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EG61-NAis stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are listed below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤30º C/60%RH.
   - Stored at <10% RH.

3. Devices require bake before mounting, if any circumstances below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30º C/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properlyso as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, thethickness of stencil for the module is recommended to be 0.15mm~0.18mm. For more details, please refer to***document [3]***.

It is suggested that the peak reflow temperature is 240ºC ~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

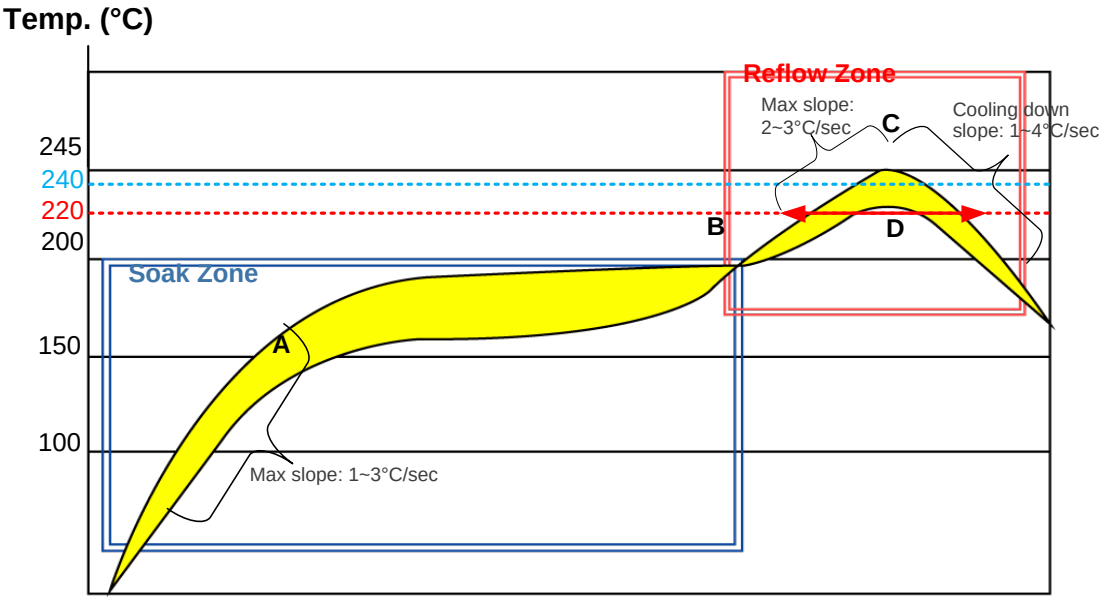


Figure 46: Reflow Soldering Thermal Profile

Table 35: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec
Reflow Zone	

Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	240°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the 2Dbarcode is still readable, although white rust may be found.

8.3. Packaging

EG61-NAis packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The reel is 330mm in diameter and each reel contains 250pcs modules. The following figures show the packaging details, measured in mm.

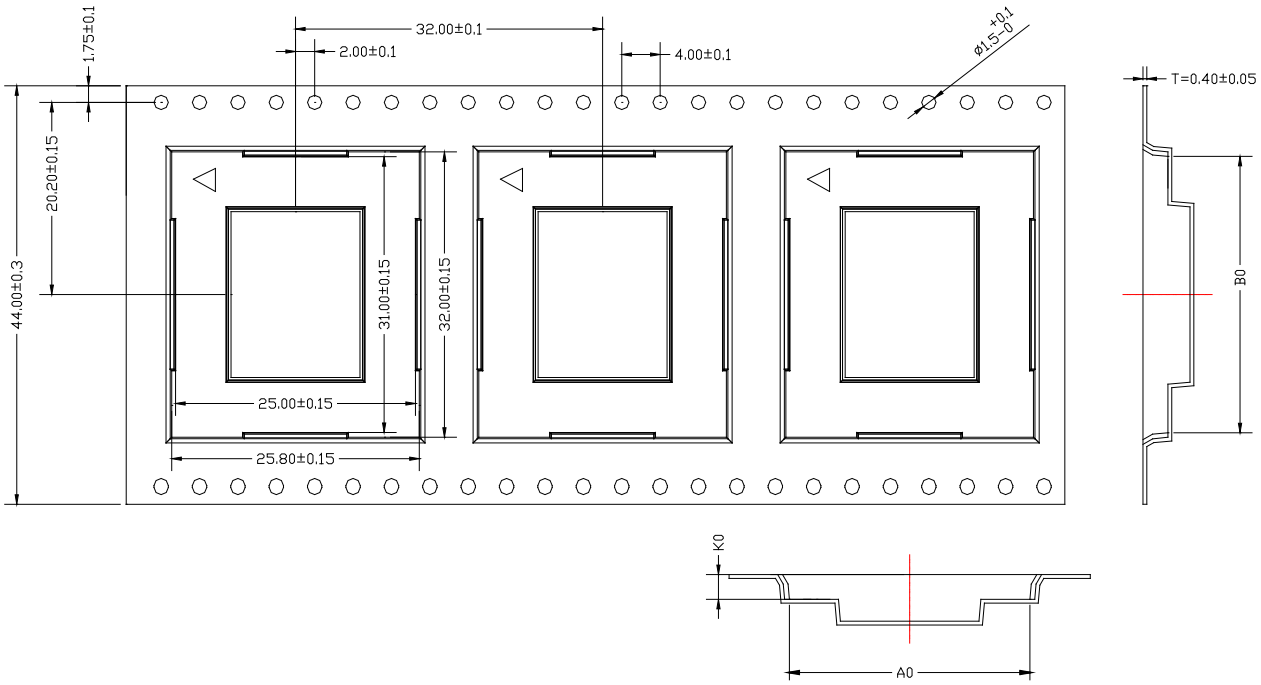


Figure 47: Tape Dimensions

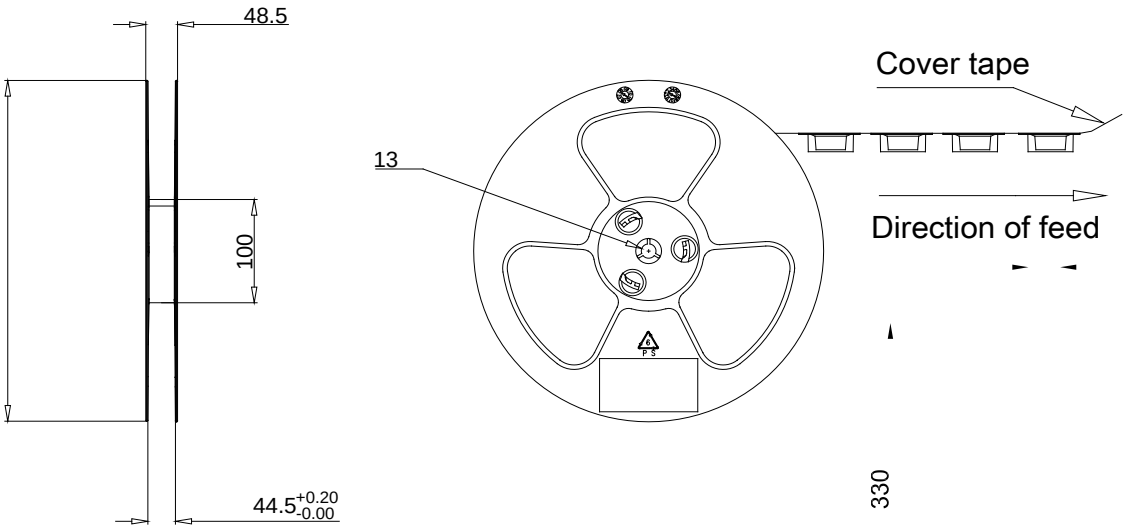


Figure 48: Reel Dimensions

9 Appendix A References

Table 36: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EG9x&EM05_Power_Management_Application_Note	Power Management Application Note for EC25, EC21, EC20 R2.0, EC20 R2.1, EG61-NA, EG91 and EM05
[2]	Quectel_EG61-NA_AT_Commands_Manual	AT Commands Manual for EG61-NA
[3]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal design guide for LTE modules including EC25, EC21, EC20 R2.0, EC20 R2.1, EG91, EG95, EG25-G, EP06, EG06, EM06 and AG35.

Table 37: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
HSPA+	High Speed Packet Access+
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink

DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GSM	Global System For Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol

QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
$V_O$ax	Maximum Output High Level Voltage Value
$V_O$in	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value

VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access