# RM502Q-GL

# Hardware Design

**5G Module Series**

Rev. RM502Q-GL_Hardware_Design_V1.0

Date: 2020-07-06

Status: Preliminary

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# About the Document

## Revision History

| Version | Date | Author | Description |
|---|---|---|---|
| 1.0 | 2020-07-06 | Kingson ZHANG/ Qiqi WANG | Initial |

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# 1 Introduction

This document defines RM502Q-GL module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document helps customers quickly understand the interface specifications, electrical and mechanical details, as well as other related information of RM502Q-GL module. To facilitate its application in different fields, reference design is also provided for reference. Associated with application notes and user guides, customers can use the module to design and set up mobile applications easily.

## 1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating RM502Q-GL module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

| | |
|---|---|
|  | Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving. |
|  | Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft. |
|  | Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities. |
|  | Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. |
|  | The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment. |
|  | In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc. |

# 2 Product Concept

## 2.1. General Description

RM502Q-GL is a 5G NR/LTE-A/UMTS/HSPA+ wireless communication module with receive diversity. It provides data connectivity on 5G NR SA and NSA, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA networks with standard PCI Express M.2 interface.

It supports embedded operating systems such as Windows, Linux and Android, and also provides GNSS and voice functionality to meet specific application demands.

The following table shows the frequency bands and GNSS type of RM502Q-GL module.

**Table 1: Frequency Bands and GNSS Type of RM502Q-GL Module**

| Mode | RM502Q-GL |
|---|---|
| 5G NR | n1/n2/n3/n5/n7/n8/n12/n20/n25/n28/n38/n40/n41/n48/n66/n71/n77/n78 |
| LTE-FDD | B1/B2/B3/B4/B5/B7/B8/B9/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28/B29/B30/B32/B66/B71 |
| LTE-TDD | B34/B38/B39/B40/B41/B42/B43/B46/B48 |
| WCDMA | B1/B2/B3/B4/B5/B8/B19 |
| GNSS | GPS/GLONASS/BeiDou/Galileo |

**NOTE**

LTE-FDD B29/B32 and LTE-TDD B46 support receving only.

RM502Q-GL can be applied in the following fields:

- Rugged tablet PC and laptop computer
- Remote monitor system
- Vehicle system
- Wireless POS system
- Smart metering system
- Wireless router and switch
- Other wireless terminal devices

## 2.2. Key Features

The following table describes key features of RM502Q-GL.

**Table 2: Key Features of RM502Q-GL**

| Feature | Details |
|---|---|
| Function Interface | PCI Express M.2 Interface |
| Power Supply | Supply voltage: 3.135–4.4 V<br>Typical supply voltage: 3.7 V |
| Transmitting Power | Class 3 (24 dBm +1/-3 dB) for WCDMA bands<br>Class 3 (23 dBm ±2 dB) for LTE bands<br>Class 3 (23 dBm ±2 dB) for 5G NR bands<br>Class 2 (26 dBm ±2 dB) for LTE B38/B40/B41/B42/B43 bands HPUE [1)]<br>Class 2 (26 dBm +2/-3 dB) for 5G NR n41/n77/n78 bands HPUE [1)] |
| 5G NR Features | Support 3GPP Rel.15<br>Support uplink 256QAM and downlink 256QAM<br>Support downlink 4 × 4 MIMO on n1/n2/n3/n7/25/n38/n40/n41/n48/n66/n77/n78<br>Support uplink 2 × 2 UL MIMO on n41/n77/n78<br>Support SCS 15 kHz and 30 kHz<br>Support SA and NSA operation modes<br>Support NSA on n41/n77/n78<br>Support SA on all the 5G bandsSupport Option 3X, 3 A, and Option 2<br>NSA TDD: Max 2.5 Gbps(DL)/650 Mbps (UL)<br>SA TDD: Max 2.1 Gbps(DL)/900 Mbps (UL) |
| LTE Features | Support up to CA Cat 16 FDD and TDD<br>Support uplink QPSK, 16QAM and 64QAM and 256QAM modulation<br>Support downlink QPSK, 16QAM and 64QAM and 256QAM modulation<br>Support 1.4 MHz to 20 MHz (5 × CA) RF bandwidth<br>Support downlink 4 × 4 MIMO on |

| | |
|---|---|
| | B1/B2/B3/B4/B7/B25/B30/B38/B39/B40/B41/B42/B43/B48/B66 LTE: Max 1.0 Gbps(DL)/200 Mbps (UL) |
| UMTS Features | Support 3GPP R8 DC-HSDPA, HSPA +, HSDPA, HSUPA and WCDMA<br>Support QPSK, 16QAM and 64QAM modulation<br>DC-HSDPA: Max 42 Mbps (DL)<br>HSUPA: Max 5.76 Mbps (UL)<br>WCDMA: Max 384 kbps (DL)/384 kbps (UL) |
| Internet Protocol Features | Support QMI/NTP* protocols<br>Support the protocols PAP and EIRP usually used for PPP connections |
| SMS | Text and PDU modes<br>Point-to-point MO and MT<br>SMS cell broadcast<br>SMS storage: ME by default |
| (U)SIM Interfaces | ● Support (U)SIM card: Class B (3.0 V) and Class C(1.8 V)<br>● (U)SIM1 and (U)SIM2 interfaces<br>● Support Dual SIM Single Standby* |
| USB Interface | ● Compliant with USB 3.1 and 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0.<br>● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output and voice over USB*<br>● Support USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x/5.x/6.x/7.x/8.x/9.x/10 |
| PCIe × 1 Interface | Complaint with PCIe GEN3, support 8 Gbps per lane, PCIe × 1.<br>Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output |
| Rx-diversity | Support 5G NR/LTE/WCDMA Rx-diversity |
| GNSS Features | Gen9 Lite of Qualcomm<br>Protocol: NMEA 0183<br>Data Update Rate: 1 Hz |
| AT Commands | Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands |
| Antenna Interfaces | ANT0, ANT1, ANT2_GNSSL1, and ANT3 |
| Physical Characteristics | Size: (52.0 ±0.15) mm × (30.0 ±0.15) mm × (2.3 ±0.2) mm<br>Weight: approx. 8.6 g |
| Temperature Range | Operation temperature range: -30°C to +60°C [2)]<br>Restricted Operation temperature range: -30°C to -20°C, +60°C to +75°C<br>Extended temperature range: -40°C to -30°C, +75°C to +85°C [3)]<br>Storage temperature range: -40°C to +90°C |
| Firmware Upgrade | USB 2.0 interface, PCIe interface and DFOTA |

| | |
|---|---|
| RoHS | All hardware components are fully compliant with EU RoHS directive |

**NOTES**

1. [1] HPUE is only for single carrier.
2. [2] Within operation temperature range, the module meets 3GPP specifications.
3. [3] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced, while one or more specifications, such as $P_{out}$ may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.
4. "*" means under development.

## 2.3. Functional Diagram

The following figure shows a block diagram of RM502Q-GL.

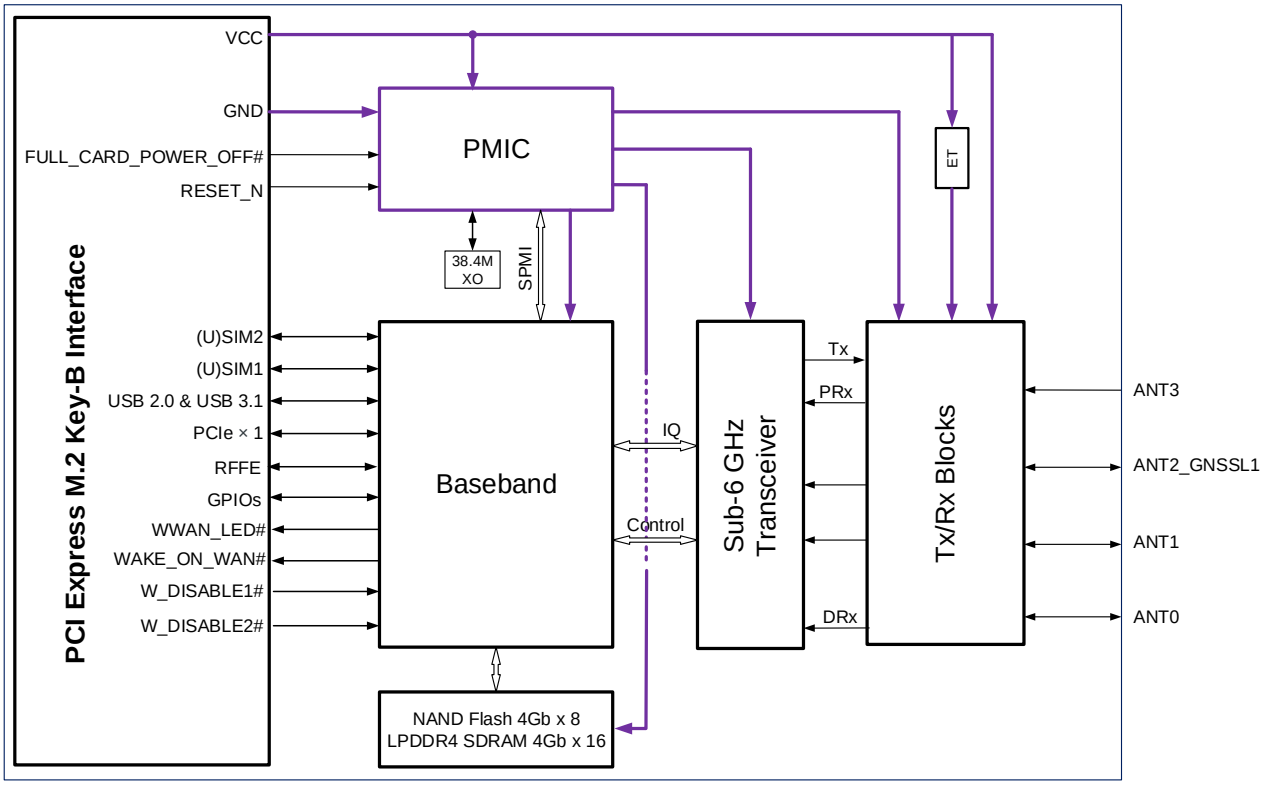



**Figure 1: Functional Diagram**

## 2.4. Evaluation Board

To help with the development of applications conveniently with RM502Q-GL, Quectel supplies the evaluation board (PCIe Card EVB), a USB to RS-232 converter cable, a USB type-C cable, antennas and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

# 3 Application Interfaces

The physical connections and signal levels of RM502Q-GL comply with *PCI Express M.2 specification*. This chapter mainly describes the definition and application of the following interfaces/pins of RM502Q-GL:

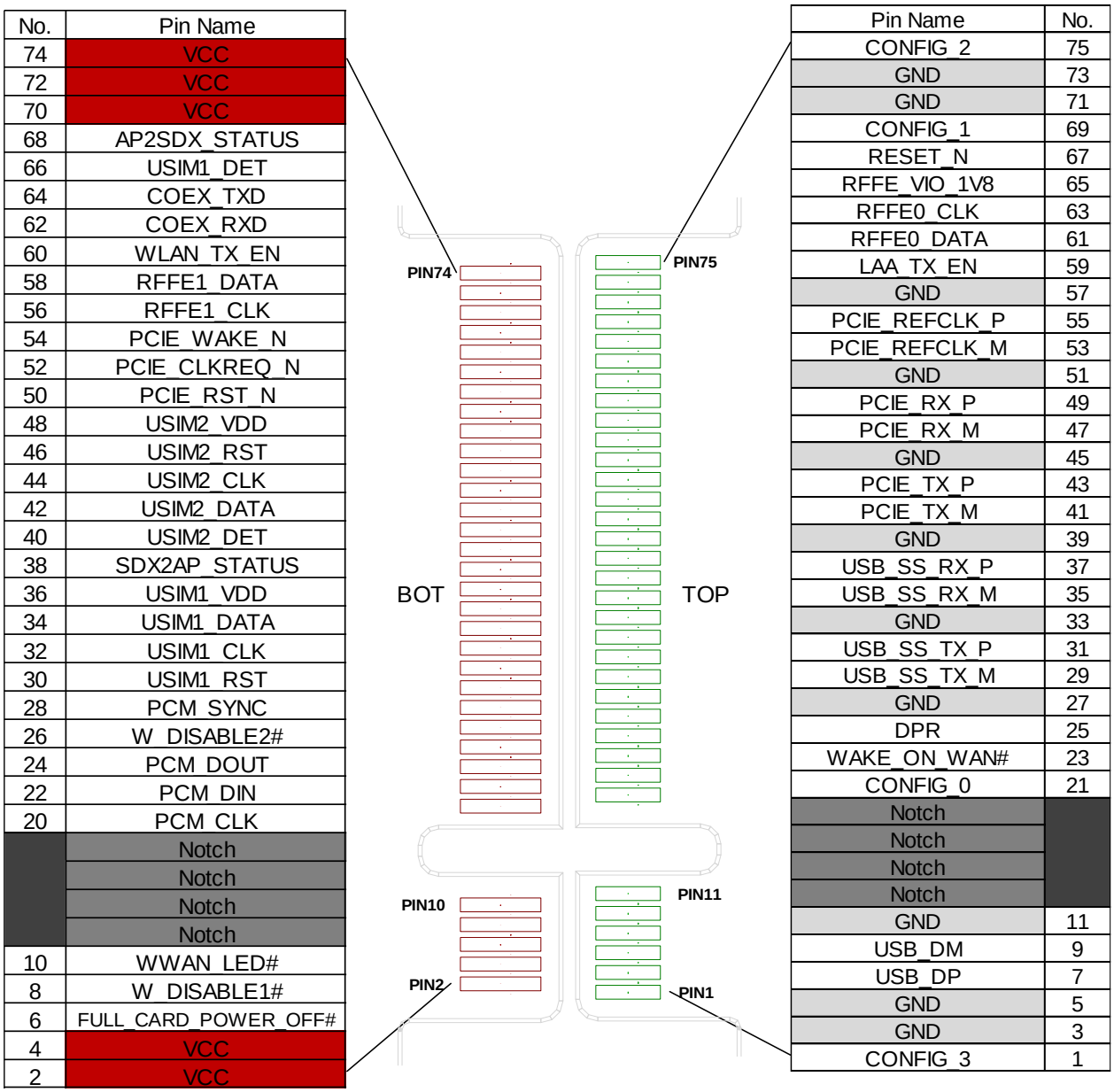
- Power supply
- (U)SIM interfaces
- USB interface
- PCIe interface
- PCM interface*
- Control and indication interfaces*
- COEX UART interface*
- Antenna tuner control interface*
- Configuration pins

**NOTE**

"*" means under development.

## 3.1. Pin Assignment

The following figure shows the pin assignment of RM502Q-GL. The top side contains RM502Q-GL module and antenna connectors.




| No. | Pin Name |
|---|---|
| 74 | VCC |
| 72 | VCC |
| 70 | VCC |
| 68 | AP2SDX_STATUS |
| 66 | USIM1_DET |
| 64 | COEX_TXD |
| 62 | COEX_RXD |
| 60 | WLAN_TX_EN |
| 58 | RFFE1_DATA |
| 56 | RFFE1_CLK |
| 54 | PCIE_WAKE_N |
| 52 | PCIE_CLKREQ_N |
| 50 | PCIE_RST_N |
| 48 | USIM2_VDD |
| 46 | USIM2_RST |
| 44 | USIM2_CLK |
| 42 | USIM2_DATA |
| 40 | USIM2_DET |
| 38 | SDX2AP_STATUS |
| 36 | USIM1_VDD |
| 34 | USIM1_DATA |
| 32 | USIM1_CLK |
| 30 | USIM1_RST |
| 28 | PCM_SYNC |
| 26 | W_DISABLE2# |
| 24 | PCM_DOUT |
| 22 | PCM_DIN |
| 20 | PCM_CLK |
| | Notch |
| | Notch |
| | Notch |
| | Notch |
| 10 | WWAN_LED# |
| 8 | W_DISABLE1# |
| 6 | FULL_CARD_POWER_OFF# |
| 4 | VCC |
| 2 | VCC |

| Pin Name | No. |
|---|---|
| CONFIG_2 | 75 |
| GND | 73 |
| GND | 71 |
| CONFIG_1 | 69 |
| RESET_N | 67 |
| RFFE_VIO_1V8 | 65 |
| RFFE0_CLK | 63 |
| RFFE0_DATA | 61 |
| LAA_TX_EN | 59 |
| GND | 57 |
| PCIE_REFCLK_P | 55 |
| PCIE_REFCLK_M | 53 |
| GND | 51 |
| PCIE_RX_P | 49 |
| PCIE_RX_M | 47 |
| GND | 45 |
| PCIE_TX_P | 43 |
| PCIE_TX_M | 41 |
| GND | 39 |
| USB_SS_RX_P | 37 |
| USB_SS_RX_M | 35 |
| GND | 33 |
| USB_SS_TX_P | 31 |
| USB_SS_TX_M | 29 |
| GND | 27 |
| DPR | 25 |
| WAKE_ON_WAN# | 23 |
| CONFIG_0 | 21 |
| Notch | |
| Notch | |
| Notch | |
| Notch | |
| GND | 11 |
| USB_DM | 9 |
| USB_DP | 7 |
| GND | 5 |
| GND | 3 |
| CONFIG_3 | 1 |

**Figure 2: Pin Assignment**

## 3.2. Pin Description

**Table 3: Definition of I/O Parameters**

| Type | Description |
|---|---|
| AI | Analog Input |
| AO | Analog Output |
| DI | Digital Input |
| DO | Digital Output |
| IO | Bidirectional |
| OD | Open Drain |
| PI | Power Input |
| PO | Power Output |

The following table shows the pin definition and description of RM502Q-GL.

**Table 4: Pin Description**

| Pin No. | M.2 Socket 2 PCIe-based Pinout | RM502Q-GL Pin Name | I/O | Description | Comment |
|---|---|---|---|---|---|
| 1 | CONFIG_3 | CONFIG_3 | DO | Not connected internally | |
| 2 | 3.3 V | VCC | PI | Power supply | $V_{min}$ = 3.135 V<br>$V_{norm}$ = 3.7 V<br>$V_{max}$ = 4.4 V |
| 3 | GND | GND | | Ground | |
| 4 | 3.3 V | VCC | PI | Power supply | $V_{min}$ = 3.135 V<br>$V_{norm}$ = 3.7 V<br>$V_{max}$ = 4.4 V |
| 5 | GND | GND | | Ground | |
| 6 | FULL_CARD_ POWER_OFF# | FULL_CARD_ POWER_OFF# | DI | Turn on/off of the module. When it is at low level, the | Internally pulled down with a |

| | | | | | |
|---|---|---|---|---|---|
| | (I)(0/1.8 V) | | | module is turned off. When it is at high level, the module is turned on. | 100k Ω resistor |
| 7 | USB_D+ | USB_DP | AI, AO | USB 2.0 differential data (+) | |
| 8 | W_DISABLE1# (I)(0/1.8 V) | W_DISABLE1# | DI | Airplane mode control. Active LOW. | 1.8/3.3 V power domain |
| 9 | USB_D- | USB_DM | AI, AO | USB 2.0 differential data (-) | |
| 10 | GPIO_9/LED_1# (OD)(0/3.3 V) | WWAN_LED# | OD | RF status indication LED | It is an open drain and active LOW signal. |
| 11 | GND | GND | | Ground | |
| 12 | Key | Notch | | Notch | |
| 13 | Key | Notch | | Notch | |
| 14 | Key | Notch | | Notch | |
| 15 | Key | Notch | | Notch | |
| 16 | Key | Notch | | Notch | |
| 17 | Key | Notch | | Notch | |
| 18 | Key | Notch | | Notch | |
| 19 | Key | Notch | | Notch | |
| 20 | GPIO_5 /AUDIO_0 | PCM_CLK | IO | PCM data bit clock | 1.8 V power domain |
| 21 | CONFIG_0 | CONFIG_0 | DO | Not connected internally | |
| 22 | GPIO_6 /AUDIO_1 | PCM_DIN | DI | PCM data input | 1.8 V power domain |
| 23 | GPIO_11 /WOWWAN# | WAKE_ON_WAN# | OD | Wake up the host. Active LOW. | Open drain |
| 24 | GPIO_7 /AUDIO_2 | PCM_DOUT | DO | PCM data output | 1.8 V power domain |
| 25 | DPR (I)(0/1.8 V) | DPR | DI | Dynamic power reduction. High level by default. | 1.8 V power domain |
| 26 | GPIO_10 /W_DISABLE2# | W_DISABLE2# | DI | GNSS disable control. Active LOW. | 1.8/3.3 V power domain |
| 27 | GND | GND | | Ground | |

| | | | | | |
|---|---|---|---|---|---|
| 28 | GPIO_8<br>/AUDIO_3 | PCM_SYNC | IO | PCM data frame sync | 1.8 V power domain |
| 29 | PETn1 | USB_SS_TX_M | AO | USB 3.1 transmit data (-) | |
| 30 | UIM_RESET(O) | USIM1_RST | DO | (U)SIM1 card reset | 1.8/3.0 V power domain |
| 31 | PETp1 | USB_SS_TX_P | AO | USB 3.1 transmit data (+) | |
| 32 | UIM_CLK(O) | USIM1_CLK | DO | (U)SIM1 card clock | 1.8/3.0 V power domain |
| 33 | GND | GND | | Ground | |
| 34 | UIM_DATA(I/O) | USIM1_DATA | IO | (U)SIM1 card data | 1.8/3.0 V power domain |
| 35 | PERn1 | USB_SS_RX_M | AI | USB 3.1 receive data (-) | |
| 36 | UIM_PWR(O) | USIM1_VDD | PO | Power supply for (U)SIM1 card | 1.8/3.0 V power domain |
| 37 | PERp1 | USB_SS_RX_P | AI | USB 3.1 receive data (+) | |
| 38 | NC | SDX2AP_STATUS | DO | Status indication to AP | 1.8 V power domain |
| 39 | GND | GND | | Ground | |
| 40 | GPIO_0<br>/SIM_DET2 | USIM2_DET | DI | (U)SIM2 card insertion detection | Internally pulled up to 1.8 V |
| 41 | PETn0 | PCIE_TX_M | AO | PCIe transmit data (-) | |
| 42 | GPIO_1<br>/SIM_DAT2 | USIM2_DATA | IO | (U)SIM2 card data | 1.8/3.0 V power domain |
| 43 | PETp0 | PCIE_TX_P | AO | PCIe transmit data (+) | |
| 44 | GPIO_2<br>/SIM_CLK2 | USIM2_CLK | DO | (U)SIM2 card clock | 1.8/3.0 V power domain |
| 45 | GND | GND | | Ground | |
| 46 | GPIO_3<br>/SIM_RST2 | USIM2_RST | DO | (U)SIM2 card reset | 1.8/3.0 V power domain |
| 47 | PERn0 | PCIE_RX_M | AI | PCIe receive data (-) | |
| 48 | GPIO_4<br>(SIM_PWR2) | USIM2_VDD | PO | Power supply for (U)SIM2 card | 1.8/3.0 V power domain |
| 49 | PERp0 | PCIE_RX_P | AI | PCIe receive data (+) | |
| 50 | PERST# | PCIE_RST_N | DI | PCIe reset.<br>Active LOW. | Open drain |

| | | | | | |
|---|---|---|---|---|---|
| 51 | GND | GND | | Ground | |
| 52 | CLKREQ# | PCIE_CLKREQ_N | DO | PCIe clock request.<br>Active LOW. | Open drain |
| 53 | REFCLKn | PCIE_REFCLK_M | AI, AO | PCIe reference clock (-) | |
| 54 | PEWAKE# | PCIE_WAKE_N | DO | PCIe PME wake.<br>Active LOW. | Open drain |
| 55 | REFCLKp | PCIE_REFCLK_P | AI, AO | PCIe reference clock (+) | |
| 56 | NC | RFFE1_CLK | DO | RFFE1 serial interface clock | 1.8 V power domain |
| 57 | GND | GND | | Ground | |
| 58 | NC | RFFE1_DATA | DO | RFFE1 serial interface data | 1.8 V power domain |
| 59 | ANTCTL0 (O)(0/1.8 V) | LAA_TX_EN | DO | Notification from SDR to WL when LTE transmitting | 1.8 V power domain |
| 60 | COEX3 | WLAN_TX_EN | DI | Notification from WL to SDR while transmitting | 1.8 V power domain |
| 61 | ANTCTL1 (O)(0/1.8 V) | RFFE0_DATA | DO | RFFE0 serial interface data | 1.8 V power domain |
| 62 | COEX2 | COEX_RXD | DI | LTE/WLAN coexistence receive data | 1.8 V power domain |
| 63 | ANTCTL2 (O)(0/1.8 V) | RFFE0_CLK | DO | RFFE0 serial interface clock | 1.8 V power domain |
| 64 | COEX1 | COEX_TXD | DO | LTE/WLAN coexistence transmit data | 1.8 V power domain |
| 65 | ANTCTL3 (O)(0/1.8 V) | RFFE_VIO_1V8 | PO | Power supply for RFFE | 1.8 V power output |
| 66 | SIM_DETECT | USIM1_DET | DI | (U)SIM1 card insertion detection | Internally pulled up to 1.8 V |
| 67 | RESET# (I)(0/1.8 V) | RESET_N | DI | Reset the module.<br>Active LOW. | Internally pulled up to 1.8 V with a 100k Ω resistor |
| 68 | SUSCLK(32 kHz) | AP2SDX_STATUS | DI | Status indication from AP | 1.8 V power domain |
| 69 | CONFIG_1 | CONFIG_1 | DO | Connected to GND internally | |
| 70 | 3.3 V | VCC | PI | Power supply | $V_{min}$ = 3.135 V<br>$V_{norm}$ = 3.7 V<br>$V_{max}$ = 4.4 V |

| | | | | | |
|---|---|---|---|---|---|
| 71 | GND | GND | | Ground | |
| 72 | 3.3 V | VCC | PI | Power supply | Vmin = 3.135 V<br>Vnorm = 3.7 V<br>Vmax = 4.4 V |
| 73 | GND | GND | | Ground | |
| 74 | 3.3 V | VCC | PI | Power supply | Vmin = 3.135 V<br>Vnorm = 3.7 V<br>Vmax = 4.4 V |
| 75 | CONFIG_2 | CONFIG_2 | DO | Not connected internally | |

**NOTE**

Keep all NC, reserved and unused pins unconnected.

## 3.3. Power Supply

The following table shows pin definition of VCC pins and ground pins.

**Table 5: Definition of VCC and GND Pins**

| Pin No. | Pin Name | I/O | Power Domain | Description |
|---|---|---|---|---|
| 2, 4, 70, 72, 74 | VCC | PI | 3.135-4.4 V | 3.7 V typical DC supply |
| 3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73 | GND | | | Ground |

### 3.3.1. Decrease Voltage Drop

The power supply range of the module is from 3.135 V to 4.4 V. Please ensure that the input voltage will never drop below 3.135 V, otherwise the module will be powered off automatically. The following figure shows the maximum voltage drop during radio transmission in 3G/4G/5G networks.

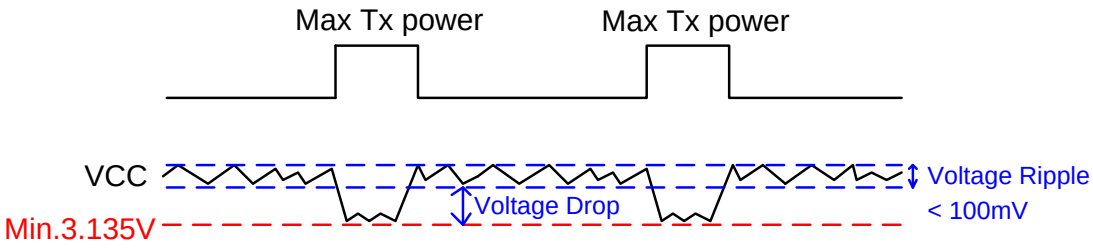



**Figure 3: Power Supply Limits during Radio Transmission**

The main power supply from an external system must be a single voltage source. To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) array also should be used due to its ultra-low ESR. It is recommended to use four ceramic capacitors (1 µF, 100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VCC pins. The width of VCC trace should be no less than 2 mm. In principle, the longer the VCC trace is, the wider it should be.

In addition, in order to get a stable power source, it is recommended to use a zener diode with a reverse zener voltage of 5.1 V and a dissipation power of more than 0.5 W. The following figure shows a reference circuit of VCC.

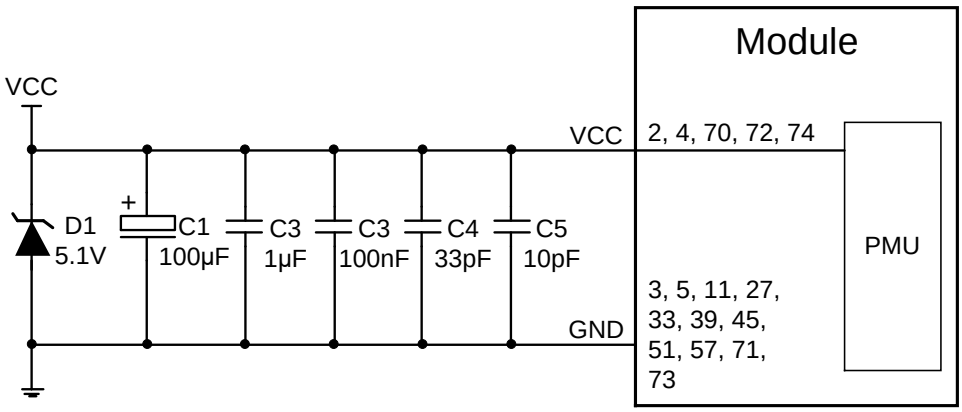



**Figure 4: Reference Circuit of VCC Pins**

### 3.3.2. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply is capable of providing a sufficient current of at least 3 A. If the voltage drop between the input and output is not too high, it is suggested that an LDO is used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VCC = 3.7 V Typ.), a buck DC-DC converter is preferred as the power supply.

The following figure shows a reference design for +5 V input power source based on an DC-DC TPS54319. The typical output of the power supply is about 3.7 V and the maximum load current is 3 A.

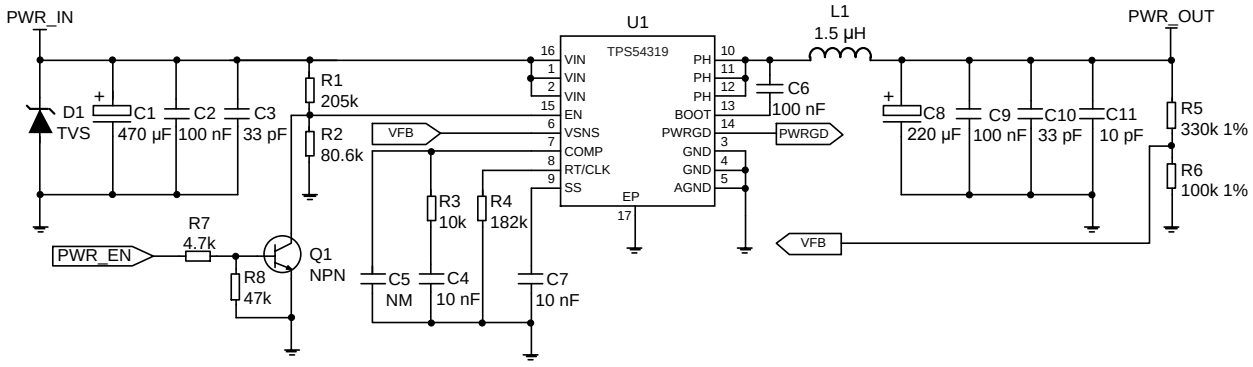



**Figure 5: Reference Design of Power Supply**

**NOTE**

In order to avoid damages to the internal flash, please do not switch off the power supply directly when the module is working. It is suggested that the power supply can be cut off after the module is powered off by pulling down the FULL_CARD_POWER_OFF# pin for more than 10 s.

## 3.4. Turn on and off Scenarios

### 3.4.1. Turn on the Module

FULL_CARD_POWER_OFF# asynchronous signal is an Active Low input that is used to turn off the entire module. When the input signal is asserted high ( ≥ 1.19 V) the Module will be enabled. When the input signal is driven low signal ( ≤ 0.2 V) or Tri-stated, it will force the module to shut down.

This input signal is 3.3 V tolerant and can be driven by either 1.8 V or 3.3 V GPIO. Also, it has internally pulled down with a 100 kΩ resistor.

The following table shows the definition of FULL_CARD_POWER_OFF#.

.

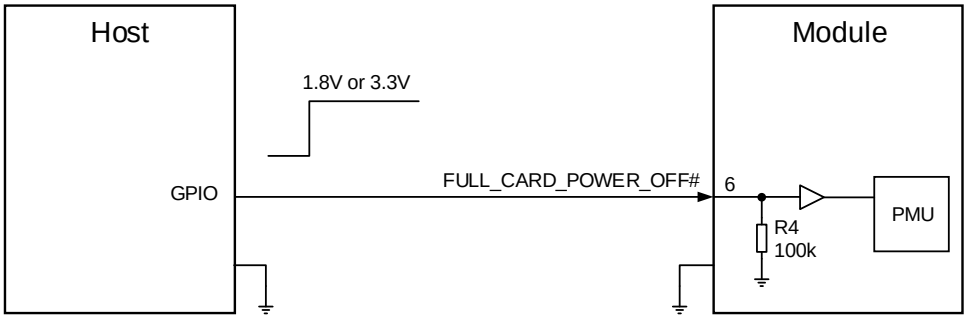
**Table 6: Definition of FULL_CARD_POWER_OFF# Pin**

| Pin No. | Pin Name | Description | DC Characteristics | Comment |
|---|---|---|---|---|
| 6 | FULL_CARD_POWER_OFF# | Turn on/off of the module.<br>When it is at low level, the module is powered off. | $V_{IH(max)}$ = 4.4 V<br>$V_{IH(min)}$ = 1.19 V<br>$V_{IL(max)}$ = 0.2 V | Internally pulled down with a 100 kΩ resistor |

| | |
|---|---|
| | When it is at high level, the module is powered on. |

#### 3.4.1.1. Turn on the Module with a Host GPIO

It is recommended to use a host GPIO to control FULL_CARD_POWER_OFF#. A simple reference circuit is illustrated in the following figure.



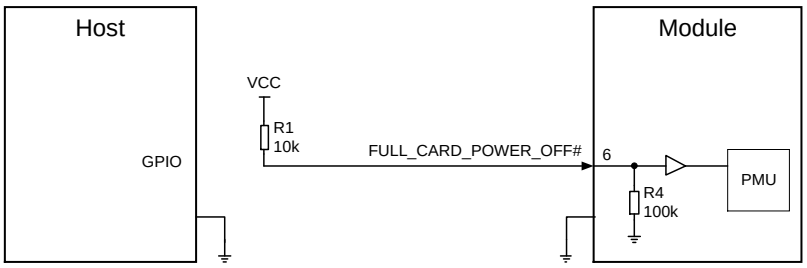

**Note:** The voltage of pin 6 should be no less than 1.19V when it is at HIGH level.

**Figure 6: Turn on the Module with a Host GPIO**

#### 3.4.1.2. Turn on the Module Automatically

If FULL_CARD_POWER_OFF# is pulled up to VCC with a 5–10 kΩ resistor, the module will be powered on automatically when the power supply for VCC is applied.

A reference circuit is shown in the following figure.

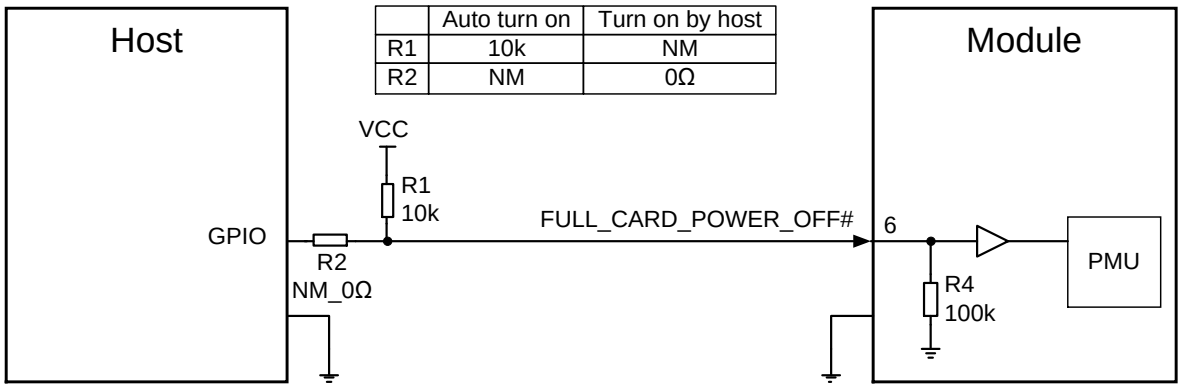



**Notes:**
1. The voltage of pin 6 should be no less than 1.19V when it is at HIGH level.
2. The VCC represents the power supply of the module.

**Figure 7: Turn on the Module Automatically**

#### 3.4.1.3. Turn on the Module with Compatible Design

The following figure shows a compatible design to turn on the module automatically after power-up or by host.




| | Auto turn on | Turn on by host |
|---|---|---|
| R1 | 10k | NM |
| R2 | NM | 0Ω |

**Notes:**
1. The voltage of pin 6 should be no less than 1.19V when it is at HIGH level.
2. The VCC represents the power supply of the module.

**Figure 8: Turn on the Module with Compatible Design**

The turn-on scenario is illustrated in the following figure.

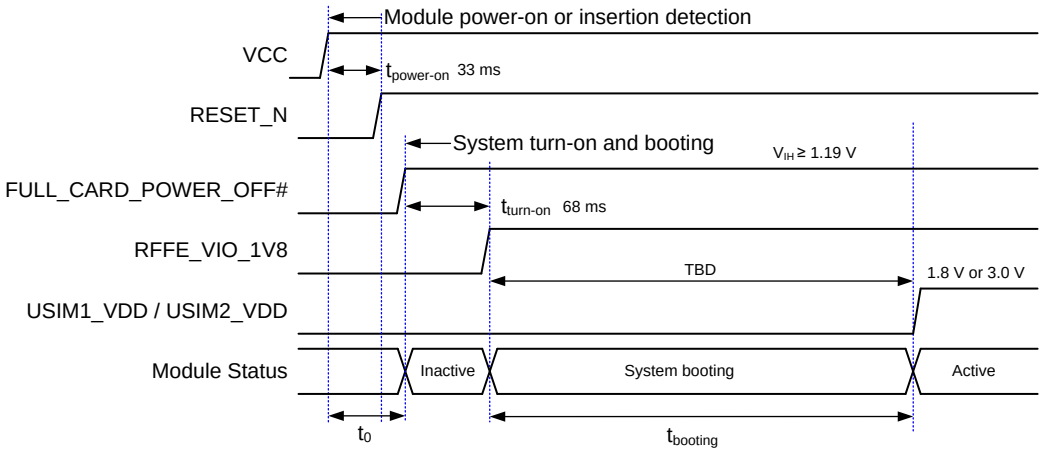



**Figure 9: Turn-on Timing of the Module**

**NOTES**

1. $t_{power-on}$ is time the interval between VCC and RESET_N HIGH level, which is a typically 33 ms. It is measured when RESET_N is not pulled down by the host device.
2. $t_{turn-on}$ is the time interval between FULL_CARD_POWER_OFF# HIGH level and RFFE_VIO_1V8(an

internal LDO output) HIGH level, which is typically 68 ms.

3. $t_0$ is the time interval between VCC and FULL_CARD_POWER_OFF# HIGH level. It could be 0 by turning on the module automatically as shown in ***Figure 7***, or any other time decided by the host as shown in ***Figure 6***.

$t_{booting}$ is the time interval between RFFE_VIO_1V8 HIGH level and the USIM_VDD power-on.

## 3.4.2. Turn off the Module

### 3.4.2.1. Turn off the Module through FULL_CARD_POWER_OFF#

In ***Figure 6***, pulling down the FULL_CARD_POWER_OFF# pin will turn off the module. The turn off scenario is illustrated in the following figure.

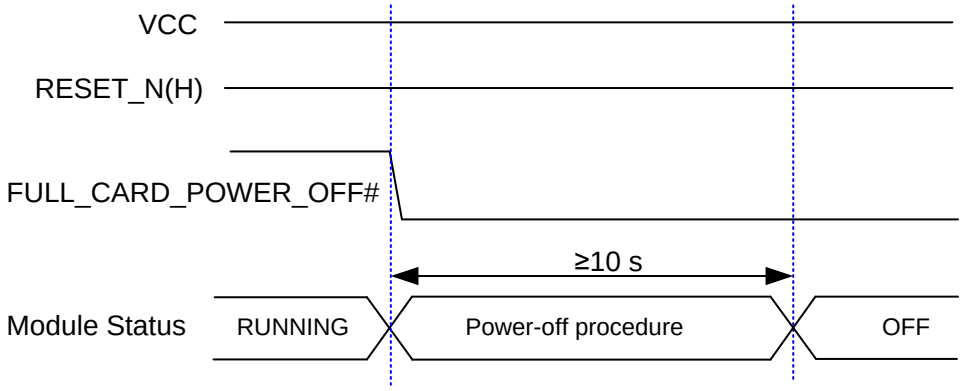



**Figure 10: Turn-off Timing through FULL_CARD_POWER_OFF#**

### 3.4.2.2. Turn off the Module through AT Command

It is a safe way to use **AT+QPOWD** command to turn off the module. For more details about the command, please refer to ***document [2]***.

For the circuit design of ***Figure 6***, please pull down FULL_CARD_POWER_OFF# pin, or cut off power supply of VCC after the module USB/PCIe is removed. Otherwise, the module will be powered on again.

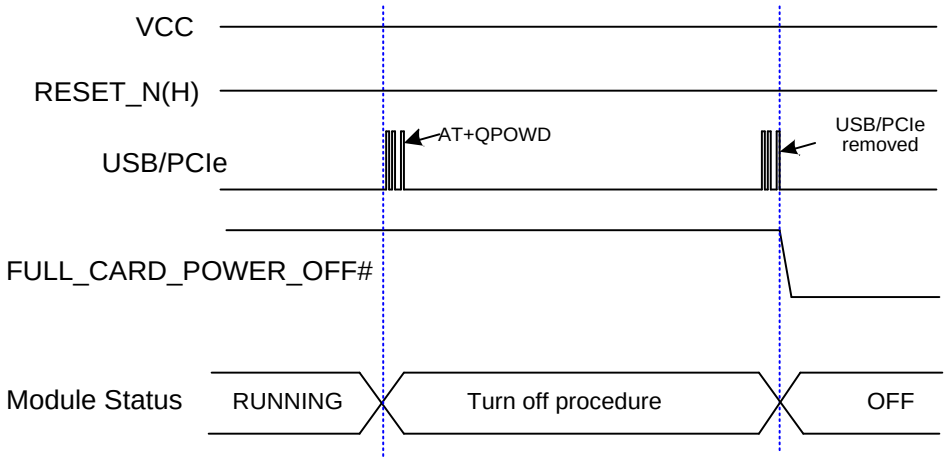



**Figure 11: Turn-off Timing through AT Command and FULL_CARD_POWER_OFF#**

For the circuit design of ***Figure 7*****,** please cut off power supply of VCC after the module USB/PCIe is removed, as illustrated in ***Figure 11***. Otherwise, the module will be powered on again.

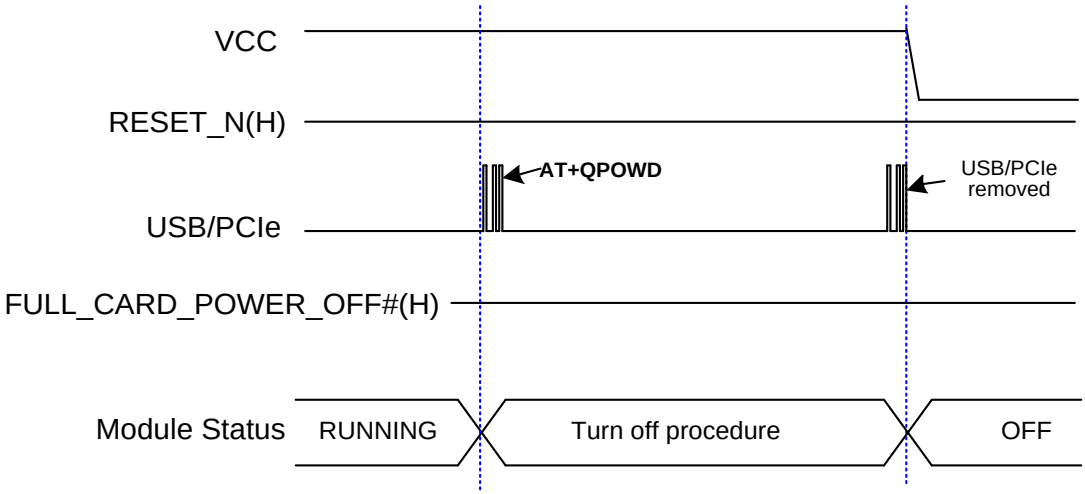



**Figure 12: Turn-off Timing through AT Command and Power Supply**

**NOTE**

Please pull down FULL_CARD_POWER_OFF# pin immediately or cut off the power supply VCC when the host detects that the module USB/PCIe is removed.

## 3.5. Reset

RESET_N is an asynchronous and active low signal (1.8 V logic level). Whenever this pin is active, the modem will immediately be placed in a Power On Reset(POR) condition.

CAUTION: Triggering the RESET# signal will lead to loss of all data in the modem and the removal of system drivers. It will also disconnect the modem from the network.

**Table 7: Definition of RESET_N Pin**

| Pin No. | Pin Name | Description | DC Characteristics | Comment |
|---|---|---|---|---|
| 67 | RESET_N | Reset the module | $V_{IH(max)}$ = 2.1 V<br>$V_{IH(min)}$ = 1.3 V<br>$V_{IL(max)}$ = 0.5 V | Internally pulled up to 1.8 V with a 100 kΩ resistor |

The module can be reset by pulling down the RESET_N pin for 200–700 ms. An open collector/drain driver or button can be used to control the RESET_N pin.

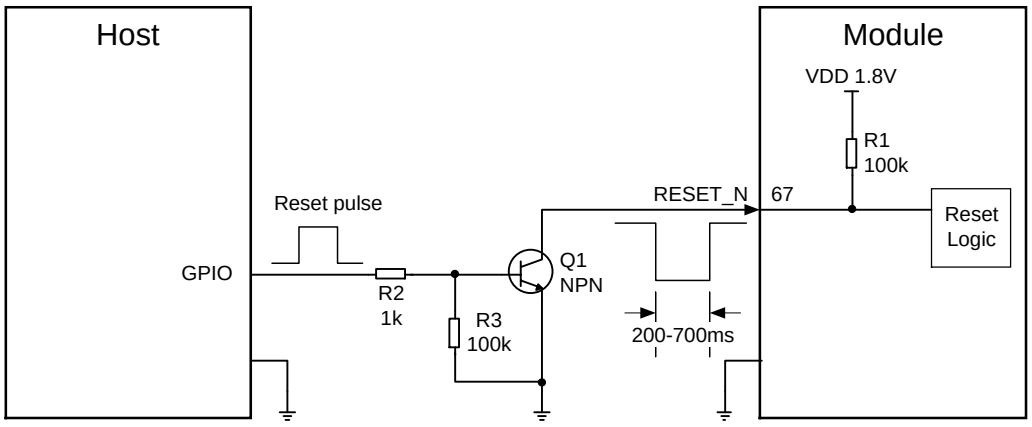



**Figure 13: Reference Circuit of RESET_N with NPN Driving Circuit**

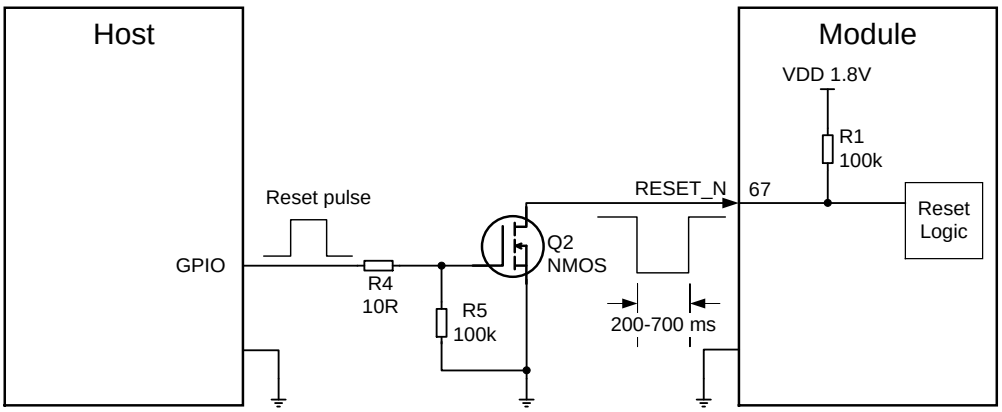
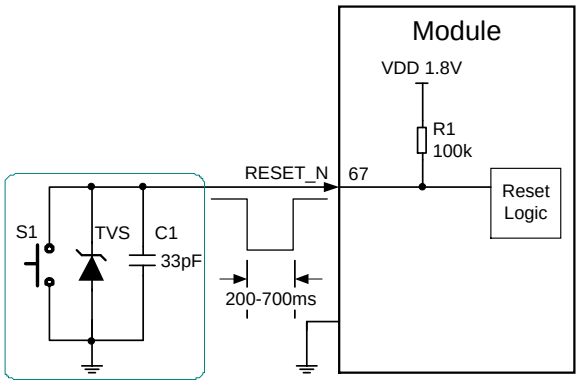



**Figure 14: Reference Circuit of RESET_N with NMOS Driving Circuit**




**Note:** The capacitor C1 is recommended to be less than 47pF.

**Figure 15: Reference Circuit of RESET_N with Button**

The reset scenario is illustrated in the following figure.

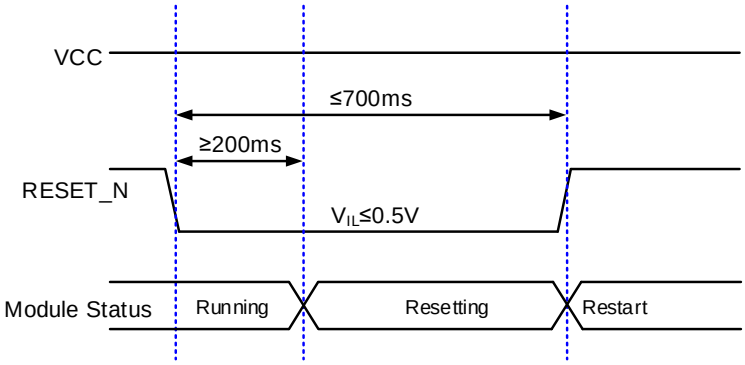



**Figure 16: Resetting Timing of the Module**

## 3.6. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported, and Dual SIM Single Standby* function is supported.

**Table 8: Pin Definition of (U)SIM Interfaces**

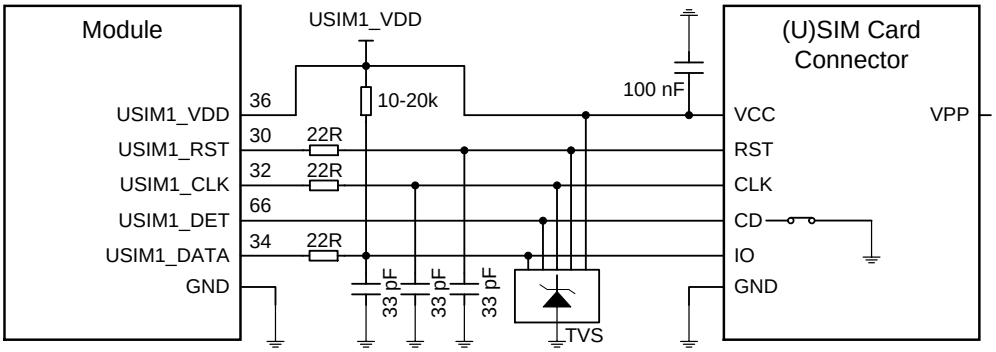
| Pin No. | Pin Name | I/O | Description | Comment |
|---|---|---|---|---|
| 36 | USIM1_VDD | PO | Power supply for (U)SIM1 card | Class B (3.0 V) and Class C (1.8 V) |
| 34 | USIM1_DATA | IO | (U)SIM1 card data | 1.8/3.0 V power domain |
| 32 | USIM1_CLK | DO | (U)SIM1 card clock | 1.8/3.0 V power domain |
| 30 | USIM1_RST | DO | (U)SIM1 card reset | 1.8/3.0 V power domain |
| 66 | USIM1_DET | DI | (U)SIM1 card insertion detection. | Internally pulled up |
| 48 | USIM2_VDD | PO | Power supply for (U)SIM2 card | Either 1.8 V or 3.0 V is supported automatically. |
| 42 | USIM2_DATA | IO | (U)SIM2 card data | 1.8/3.0 V power domain |
| 44 | USIM2_CLK | DO | (U)SIM2 card clock | 1.8/3.0 V power domain |
| 46 | USIM2_RST | DO | (U)SIM2 card reset | 1.8/3.0 V power domain |
| 40 | USIM2_DET | DI | (U)SIM2 card insertion detection. | Internally pulled up to 1.8 V |

**NOTE**

"*" means under development.

RM502Q-GL supports (U)SIM card hot-plug via the USIM_DET pin, which is a level trigger pin. With a normally closed (U)SIM card connector, the USIM_DET is normally short-circuited to ground when a (U)SIM card is not inserted, and the USIM_DET will change from low to high level when the (U)SIM card is inserted. The rising edge indicates insertion of the (U)SIM card. When the (U)SIM card is removed, the USIM_DET will change from high to low level. This falling edge indicates the absence of the (U)SIM card.

The following figure shows a reference design of (U)SIM interface with a normally closed (NC) (U)SIM card connector.



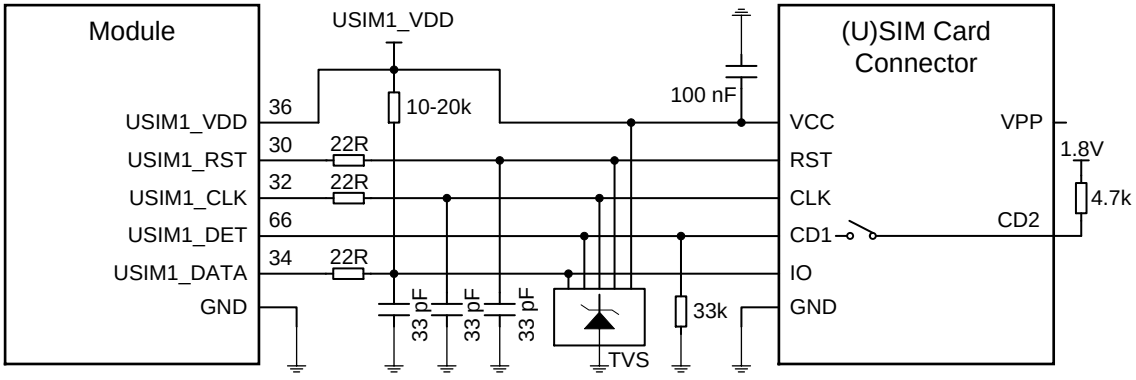

**Note:** All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

**Figure 17: Reference Circuit of Normally Closed (U)SIM Card Connector**

**Normally Closed (U)SIM Card Connector:**

- When the (U)SIM is absent, CD is short-circuited to ground and USIM_DET is at low level.
- When the (U)SIM is inserted, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design of (U)SIM interface with a normally open (NO) (U)SIM card connector.



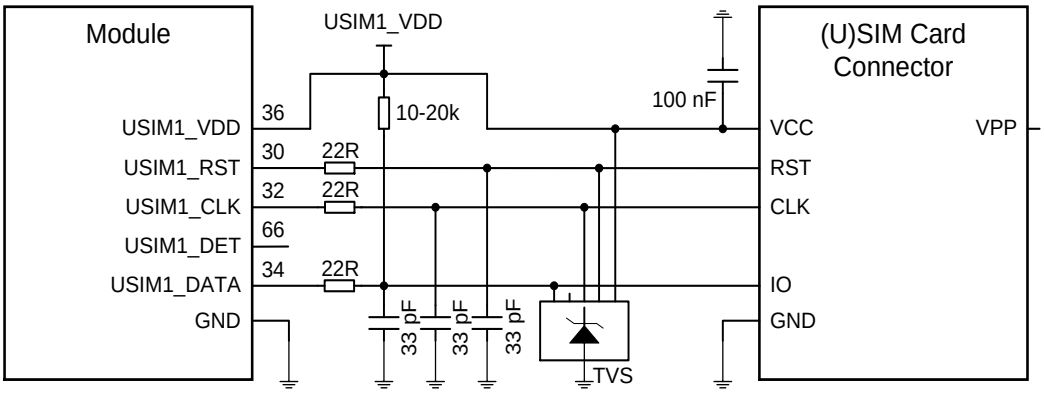

**Note:** All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

**Figure 18: Reference Circuit of Normally Open (U)SIM Card Connector**

**Normally Open (U)SIM Card Connector:**

- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at low level.
- When the (U)SIM is inserted, CD1 is short-circuited to 1.8 V and USIM_DET is at high level.

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.




**Note:** All these resistors, capacitors and TVS should be close to (U)SIM card connector in PCB layout.

**Figure 19: Reference Circuit of a 6-Pin (U)SIM Card Connector**

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signal traces away from RF and VCC traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 10 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used to filter out RF interference.
- The pull-up resistor on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.

## 3.7. USB Interface

RM502Q-GL provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.1 & 2.0 specifications and supports super speed (10) on USB 3.1 and high speed (480 Mbps) and full speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB*.

Please note that only USB 2.0 can be used for firmware upgrade currently.

The following table shows the pin definition of USB interface.

**Table 9: Pin Definition of USB Interface**

| Pin No. | Pin Name | I/O | Description | Comment |
|---|---|---|---|---|
| 7 | USB_DP | AI/AO | USB 2.0 differential data bus (+) | Require differential impedance of 90 Ω |
| 9 | USB_DM | AI/AO | USB 2.0 differential data bus (-) | |
| 29 | USB_SS_TX_M | AO | USB 3.1 transmit data (-) | Require differential impedance of 90 Ω |
| 31 | USB_SS_TX_P | AO | USB 3.1 transmit data (+) | |
| 35 | USB_SS_RX_M | AI | USB 3.1 receive data (-) | Require differential impedance of 90 Ω |
| 37 | USB_SS_RX_P | AI | USB 3.1 receive data (+) | |

**NOTE**

"*" means under development.

For more details about the USB 3.1 & 2.0 specifications, please visit http://www.usb.org/home.

The USB 2.0 interface is recommended to be reserved for firmware upgrade in designs. The following figure shows a reference circuit of USB 3.1 & 2.0 interface.

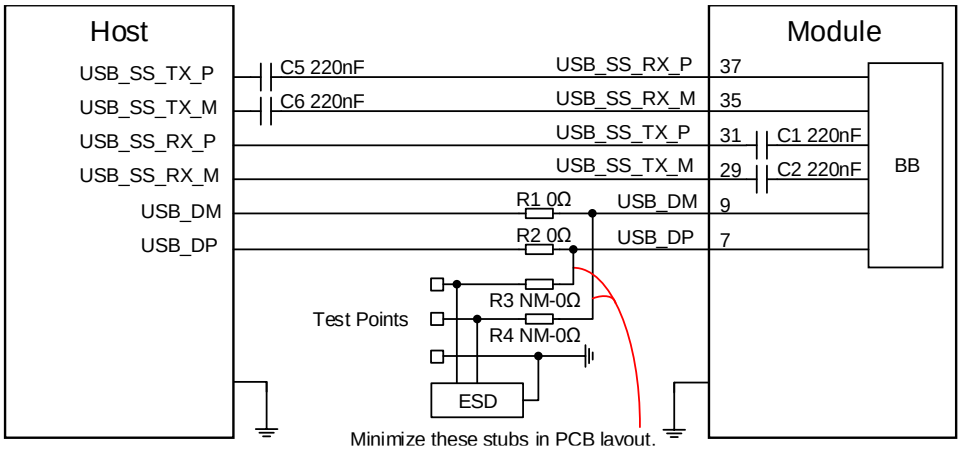



**Figure 20: Reference Circuit of USB 3.1 & 2.0 Interface**

AC coupling capacitors C5 and C6 must be placed close to the host and close to each other. C1 and C2 have been integrated inside the module, so do not place these two capacitors on customers' schematic and PCB. In order to ensure the signal integrity of USB 2.0 data traces, R1, R2, R3 and R4 must be placed close to the module, and the stubs must be minimized in PCB layout.

In order to ensure that the USB interface designs corresponds with USB specifications, please comply with the following principles:

- Do not route USB traces under or close to crystals, oscillators, magnetic components, RF signal traces or other high noisy signal traces. It is important to route USB differential pairs in inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- The impedance of USB 3.1 & 2.0 differential trace is 90 Ω.
- For USB 2.0 signal traces, the trace length must be less than 120 mm, the differential data pair matching is less than 2 mm (15 ps).
- If USB connector is used, please keep the ESD protection components as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection components on USB 2.0 data traces. The capacitance value of ESD protection components should be less than 2.0 pF for USB 2.0.
- If possible, reserve four 0 Ω resistors (R1–R4) on USB_DP and USB_DM as shown in the above figure.

## 3.8. PCIe Interface

RM502Q-GL provides one integrated PCIe (Peripheral Component Interconnect Express) interface which complies with the *PCI Express Base Specification, Revision 3.0* and supports up to 8 Gbps per lane.

- PCI Express Base Specification Revision 3.0 compliance
- Data rate up to 8 Gbps per lane

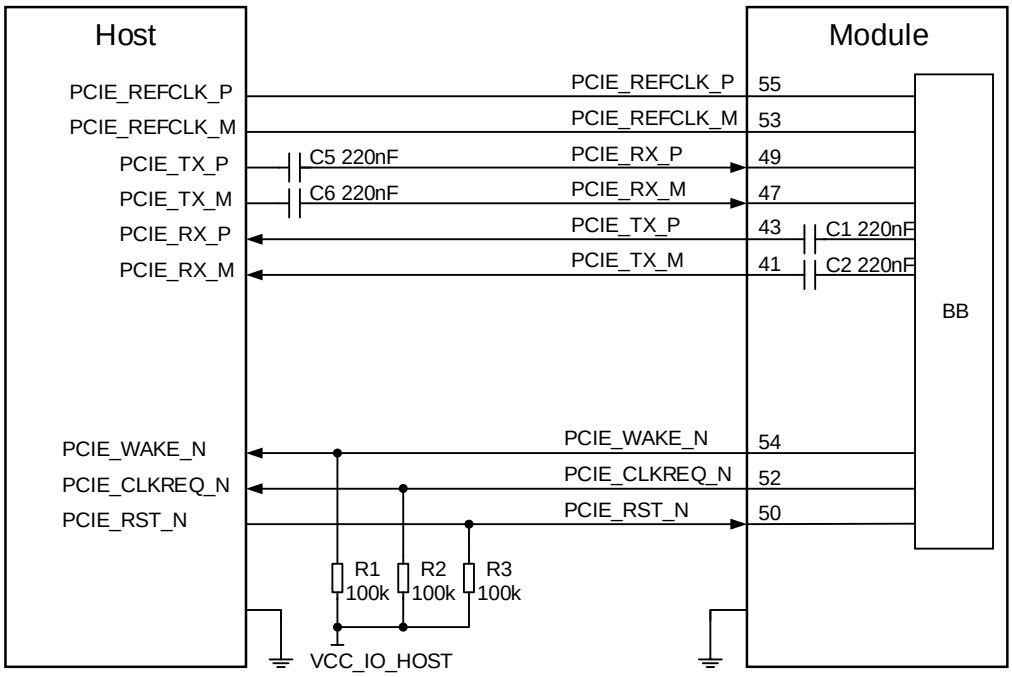
The following table shows the pin definition of PCIe interface.

**Table 10: Pin Definition of PCIe Interface**

| Pin No. | Pin Name | I/O | Description | Comment |
|---|---|---|---|---|
| 55 | PCIE_REFCLK_P | AI/AO | PCIe reference clock (+) | 100 MHz. Require differential impedance of 85 Ω |
| 53 | PCIE_REFCLK_M | AI/AO | PCIe reference clock (-) | |
| 49 | PCIE_RX_P | AI | PCIe receive data (+) | Require differential impedance of 85 Ω |
| 47 | PCIE_RX_M | AI | PCIe receive data (-) | |
| 43 | PCIE_TX_P | AO | PCIe transmit data (+) | Require differential impedance of 85 Ω |
| 41 | PCIE_TX_M | AO | PCIe transmit data (-) | |
| 50 | PCIE_RST_N | DI | PCIe reset.<br>Active LOW. | Open drain |
| 52 | PCIE_CLKREQ_N | DO | PCIe clock request.<br>Active LOW. | Open drain |
| 54 | PCIE_WAKE_N | DO | PCIe PME wake.<br>Active LOW. | Open drain |

### 3.8.1. Endpoint Mode

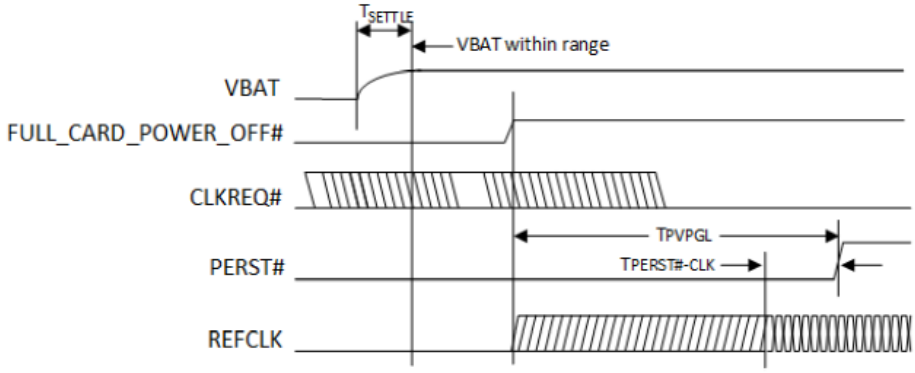
RM502Q-GL supports endpoint (EP) mode. In this mode, the module is configured as a PCIe EP device. The following figure shows a reference circuit of PCIe EP mode.




**Note:** The voltage level of VCC_IO_HOST depends on the host side due to the open drain in pins 50, 52 and 54.

**Figure 21: PCIe Interface Reference Circuit (EP Mode)**

In order to ensure the signal integrity of PCIe interface, AC coupling capacitors C5 and C6 should be placed close to the host on PCB. C1 and C2 have been integrated inside the module, so do not place these two capacitors on customers' schematic and PCB.




| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{PVPGL}$ | Power Valid* to PERST# input inactive | Implementation specific; recommended 50 ms | | ms |
| $T_{PERST\#-CLK}$ | REFCLK stable before PERST# inactive | 100 | | µs |

**Figure 22: PCIe Power-on Timing Requirements of M.2 Specification**

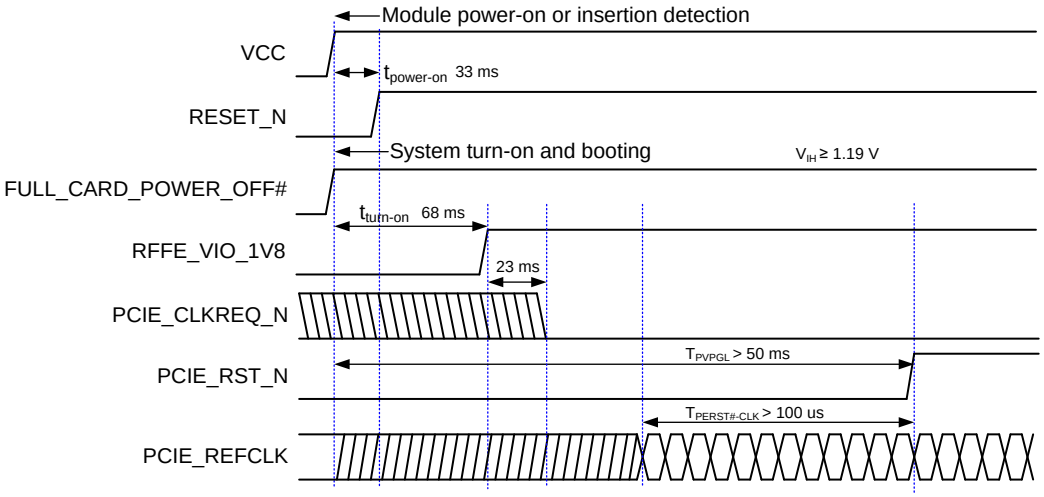



**Figure 23: PCIe Power-on Timing Requirements of the Module**

The following principles of PCIe interface design should be complied with, so as to meet PCIe V2.1 specification.

- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces.
- It is important to route the PCIe differential signal traces in inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- For PCIe signal traces, the recommended maximum length for TX and RX differential data pairs is less than 250 mm, and the intra-lane length matching of TX and RX differential data pairs is less than 0.7 mm (5 ps).

### 3.8.2. USB Version and PCIe Version

Begin with ES2 (Engineering Samples 2), RM502Q-GL supports USB version and PCIe only version described as below:

**USB version**

- Support all USB 2.0/3.1 features
- Support MBIM/QMI/QRTR/AT
- Support switch between USB and PCIe by AT command

USB is the default communication interface between RM502Q-GL module and a host. If PCIe interface is desired, an AT command under USB interface mode could be used. For more details about the AT command, please refer to ***document [2]***.

It is suggested that USB 2.0 interface could be reserved for firmware upgrade.

**USB-AT-based PCIe Version**

- Support MBIM/QMI/QRTR/AT
- Support switch back to USB interface by AT command
- Support Non-X86 systems, need to be initiated in X86 system to meet BIOS PCIe early initial requirement

When RM502Q-GL module works at USB-AT-based PCIe version, it supports MBIM/QMI/QRTR/AT, and can be switched back to USB version by AT command. But it does not support firmware upgrade by PCIE interface, therefore RM502Q-GL USB 2.0 interface must be reserved for firmware upgrade.

Please note that the USB-AT-based PCIe version cannot support BIOS PCIe early initial in X86 systems, but it could be initiated by other module which supports BIOS PCIe early initial. And Non-X86 systems does not have this problem.

**eFuse-based PCIe version**

- Support MBIM/QMI/QRTR/AT
- Support Non-X86 Systems and X86 system (could meet BIOS PCIe early initial)

If RM502Q-GL works at eFuse-based PCIe interface by burnt eFuse, the module cannot be switched back to USB version.

Please note that PCIe firmware upgrade may not be supported on non-Qualcomm AP chips. If the host does not support firmware upgrade at the PCIe only version, then RM502Q-GL USB 2.0 interface (pins 7 and 9) and two test points (VREG_L6E_1P8 and FORCE_USB_BOOT, reserved on bottom side) must be used for firmware upgrade. Also, the firmware could be upgraded by the PCIe Card EVB, which could be inserted into a PC. For more details, please refer to ***document [1]***.

## 3.9. PCM Interface*

RM502Q-GL supports audio communication via Pulse Code Modulation (PCM) digital interface. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave
- Auxiliary mode (long frame synchronization): the module works as master only

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 256 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC only.

RM502Q-GL supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

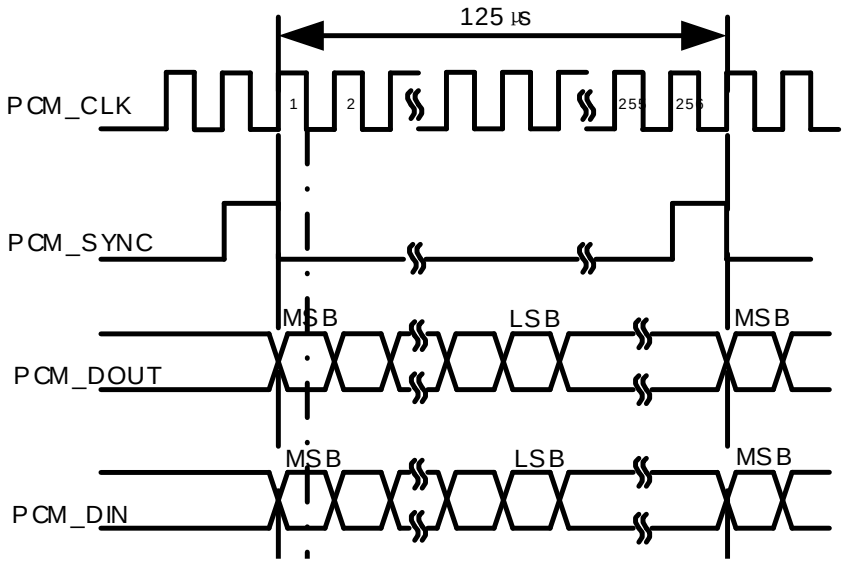



**Figure 24: Primary Mode Timing**

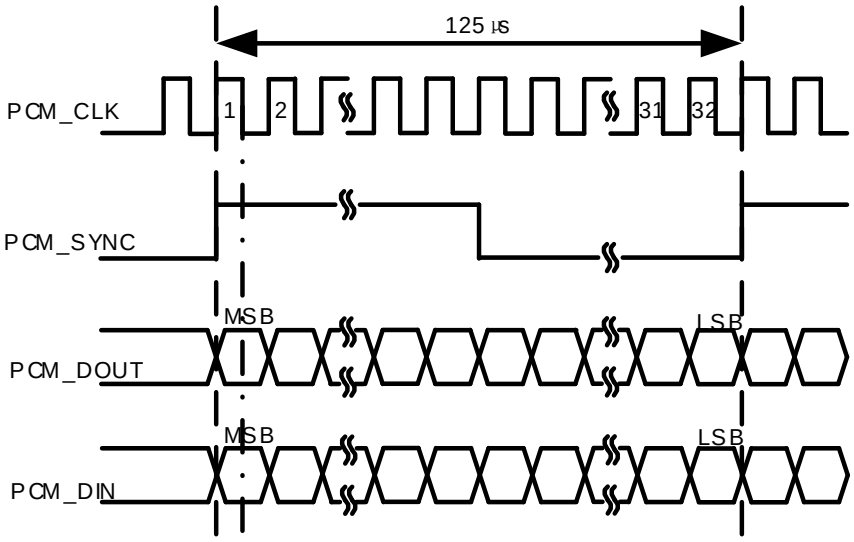



**Figure 25: Auxiliary Mode Timing**

The following table shows the pin definition of PCM interface which can be applied on audio codec design.

**Table 11: Pin Definition of PCM Interface***

| Pin No. | Pin Name | I/O | Description | Comment |
|---|---|---|---|---|
| 20 | PCM_CLK | IO | PCM data bit clock | 1.8 V power domain<br>In master mode, it is an output signal.<br>In slave mode, it is an input signal.<br>If unused, keep it open. |
| 22 | PCM_DIN | DI | PCM data input | 1.8 V power domain |
| 24 | PCM_DOUT | DO | PCM data output | 1.8 V power domain |
| 28 | PCM_SYNC | IO | PCM data frame sync | 1.8 V power domain |

The clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. Please refer to ***document [2]*** for details about **AT+QDAI** command.

**NOTE**

"*" means under development.

## 3.10. Control and Indication Interfaces

The following table shows the pin definition of control and indication pins.

**Table 12: Pin Definition of Control and Indication Interfaces**

| Pin No. | Pin Name | I/O | Description | Comment |
|---|---|---|---|---|
| 8 | W_DISABLE1#* | DI | Airplane mode control. Active LOW. | 1.8/3.3 V |
| 10 | WWAN_LED#* | OD | It is an open drain and active low signal.<br>Indicate RF status of the module. | |
| 23 | WAKE_ON_WAN#* | OD | Wake up the host.<br>It is an open drain and active low signal. | |
| 25 | DPR* | DI | Dynamic power reduction. High level by default. | 1.8 V |
| 26 | W_DISABLE2#* | DI | GNSS disable control. Active LOW. | 1.8/3.3 V |
| 38 | SDX2AP_STATUS | DO | Status indication to AP | 1.8 V power domain |

| | | | | |
|---|---|---|---|---|
| 68 | AP2SDX_STATUS | DI | Status indication from AP | 1.8 V power domain |

**NOTE**

"*" means under development.

### 3.10.1. W_DISABLE1#*

RM502Q-GL provides a W_DISABLE1# pin to disable or enable airplane mode through hardware operation. The W_DISABLE1# pin is pulled up by default. Driving it low will set the module to airplane mode. In airplane mode, the RF function will be disabled.

The RF function can also be enabled or disabled through software AT commands. The following table shows the RF function status of the module.

**Table 13: RF Function Status**

| W_DISABLE1# Level | AT Commands | RF Function Status |
|---|---|---|
| High Level | **AT+CFUN=1** | Enabled |
| High Level | **AT+CFUN=0**<br>**AT+CFUN=4** | Disabled |
| Low Level | **AT+CFUN=0**<br>**AT+CFUN=1**<br>**AT+CFUN=4** | Disabled |

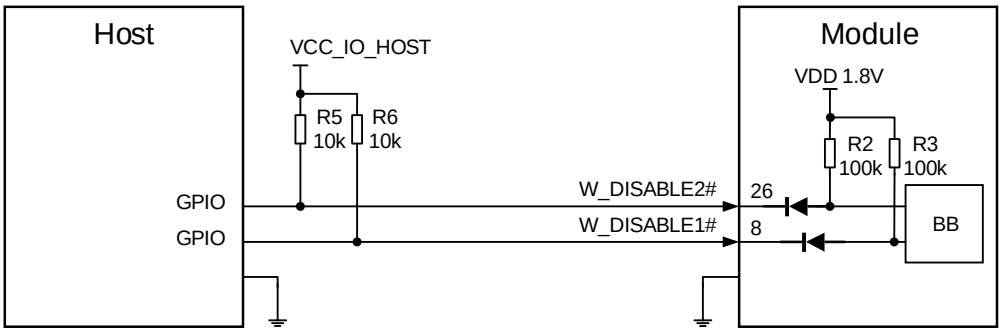
### 3.10.2. W_DISABLE2#*

RM502Q-GL provides a W_DISABLE2# pin to disable or enable the GNSS function. The W_DISABLE2# pin is pulled up by default. Driving it low will disable the GNSS function. The combination of W_DISABLE2# pin and AT commands can control the GNSS function.

**Table 14: GNSS Function Status**

| W_DISABLE2# Level | AT Commands | GNSS Function Status |
|---|---|---|
| High Level | **AT+QGPS=1** | Enabled |
| High Level | **AT+QGPSEND** | Disabled |
| Low Level | **AT+QGPS=1** | |
| Low Level | **AT+QGPSEND** | |

A simple level shifter based on diodes is used on W_DISABLE1# pin and W_DISABLE2# pin which are pulled up to a 1.8 V voltage in the module, as shown in the following figure. So the control signals (GPIO) of the host device could be a 1.8 V or 3.3 V voltage level. W_DISABLE1# and W_DISABLE2# are active low signals, and a reference circuit is shown as below.



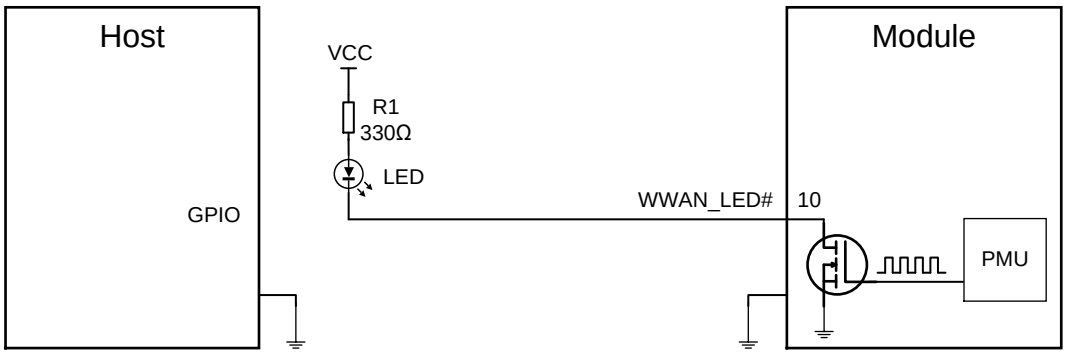

**Notes:** The voltage level of VCC_IO_HOST could be 1.8V or 3.3V typically.

**Figure 26: W_DISABLE1# and W_DISABLE2# Reference Circuit**

### 3.10.3. WWAN_LED#*

The WWAN_LED# signal is used to indicate RF status of the module, and its sink current is up to 10 mA.

In order to reduce current consumption of the LED, a current-limited resistor must be placed in series with the LED, as illustrated in the figure below. The LED is ON when the WWAN_LED# signal is at low level.




**Note:** This VCC could be the power supply of the module.

**Figure 27: WWAN_LED# Reference Circuit**

The following table shows the RF status indicated by WWAN_LED# signal.

**Table 15: Network Status Indications of WWAN_LED# Signal**

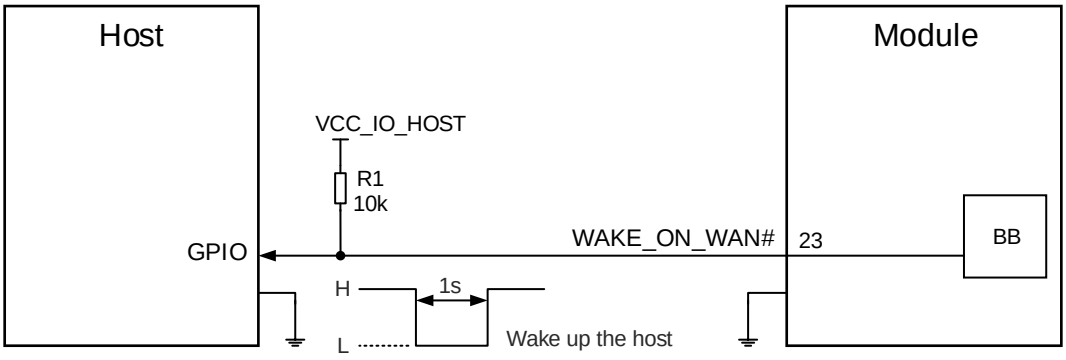
| WWAN_LED# Level | Description |
|---|---|
| Low Level (LED ON) | RF function is turned on |
| High Level (LED OFF) | RF function is turned off if any of the following occurs:<br>● The (U)SIM card is not powered.<br>● W_DISABLE1# is at low level (airplane mode enabled).<br>● **AT+CFUN=4** (RF function disabled). |

### 3.10.4. WAKE_ON_WAN#*

The WAKE_ON_WAN# is an open drain pin, which requires a pull-up resistor on the host. When a URC returns, a 1 s low level pulse signal will be outputted to wake up the host. The module operation status indicated by WAKE_ON_WAN# is shown as below.

**Table 16: State of the WAKE_ON_WAN# Signal**

| WAKE_ON_WAN# State | Module Operation Status |
|---|---|
| Output a 1 s low level pulse signal | Call/SMS/Data is incoming (to wake up the host) |
| Always at high level | Idle/Sleep |




**Note:** The voltage level on VCC_IO_HOST depends on the host side due to the open drain in pin 23.

**Figure 28: WAKE_ON_WAN# Signal Reference Circuit**

### 3.10.5. DPR*

RM502Q-GL provides a DPR (Dynamic Power Reduction) pin for body SAR (Specific Absorption Rate) detection. The signal is sent from a host system proximity sensor to RM502Q-GL module to provide an input trigger, which will reduce the output power in radio transmission.

**Table 17: Function of the DPR Signal**

| DPR Level | Function |
|---|---|
| High/Floating | Max transmitting power will NOT back off |
| Low | Max transmitting power will back off by executing **AT+QCFG="sarcfg"** command |

**NOTE**

Please refer to ***document [2]*** for more details about **AT+QCFG="sarcfg"** command.

### 3.10.6. STATUS*

RM502Q-GL provides two status indication pins for communication with IPQ807x device. Pin 38 (SDX2AP_STATUS) outputs the status indication signal to IPQ807x device, and pin 68 (AP2SDX_STATUS) inputs the status indication signal from IPQ807x device.

## 3.11. Cellular/WLAN Interface*

RM502Q-GL provides a cellular/WLAN COEX interface, the following table shows the pin definition of this interface.

**Table 18: Pin Definition of COEX Interface**

| Pin No. | Pin Name | I/O | Description | Comment |
|---|---|---|---|---|
| 62 | COEX_RXD | DI | LTE/WLAN coexistence receive data | 1.8 V power domain |
| 64 | COEX_TXD | DO | LTE/WLAN coexistence transmit data | 1.8 V power domain |
| 59 | LAA_TX_EN | DO | Notification from SDR to WL when LTE transmitting | 1.8 V power domain |
| 60 | WLAN_TX_EN | DI | Notification from WL to SDR while transmitting | 1.8 V power domain |

**NOTE**

"*" means under development.

## 3.12. Antenna Tuner Control Interface*

ANTCTL[1:2] are used for antenna tuner control and should be routed to an appropriate antenna control circuit. More details about the interface will be added in the future version of this document.

**Table 19: Pin Definition of Antenna Tuner Control Interface**

| Pin No. | Pin Name | I/O | Description | DC Characteristics |
|---|---|---|---|---|
| 61 | SDR_GRFC15 | DO | GRFC interface dedicated for external antenna tuner control | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V<br>$V_{OH}$max = 1.8 V |
| 63 | SDR_GRFC14 | DO | | |

**NOTE**

support based on CS2 and later.

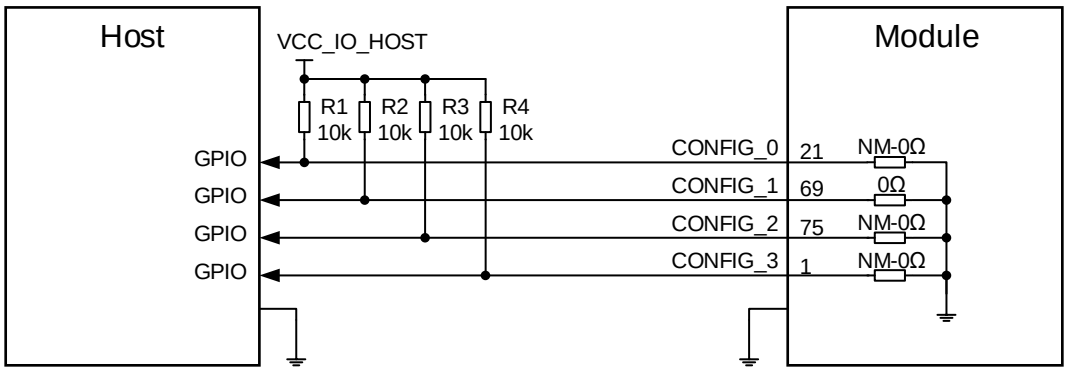
## 3.13. Configuration Pins

RM502Q-GL provides four configuration pins, which are defined as below.

**Table 20: Definition of Configuration Pins**

| Pin No. | Pin Name | I/O | Power Domain | Description |
|---|---|---|---|---|
| 21 | CONFIG_0 | DO | 0 | NC internally |
| 69 | CONFIG_1 | DO | 0 | Connected to GND internally |
| 75 | CONFIG_2 | DO | 0 | NC internally |
| 1 | CONFIG_3 | DO | 0 | NC internally |

The following figure shows a reference circuit of these four pins.




**Note:** The voltage level of VCC_IO_HOST depends on the host side and could be 1.8V or 3.3V.

**Figure 29: Recommended Circuit of Configuration Pins**

**Table 21: Configuration Pins List of M.2 Specification**

| Config_0 (Pin 21) | Config_1 (Pin 69) | Config_2 (Pin 75) | Config_3 (Pin 1) | Module Type and Main Host Interface | Port Configuration |
|---|---|---|---|---|---|
| NC | GND | NC | NC | Quectel defined | N/A |

# 4 GNSS Receiver

## 4.1. General Description

RM502Q-GL includes a fully integrated global navigation satellite system solution that supports Gen9-Lite of Qualcomm (GPS, GLONASS, BeiDou/Compass, and Galileo).

The module supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, RM502Q-GL GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

## 4.2. GNSS Performance

The following table shows GNSS performance of RM502Q-GL series module.

**Table 22: GNSS Performance**

| Parameter | Description | Conditions | Typ. | Unit |
|---|---|---|---|---|
| Sensitivity (GNSS) | Cold start | Autonomous | TBD | dBm |
| | Reacquisition | Autonomous | TBD | dBm |
| | Tracking | Autonomous | TBD | dBm |
| TTFF (GNSS) | Cold start @ open sky | Autonomous | TBD | s |
| | | XTRA enabled | TBD | s |
| | Warm start @ open sky | Autonomous | TBD | s |
| | | XTRA enabled | TBD | s |
| | Hot start @ open sky | Autonomous | TBD | s |
| | | XTRA enabled | TBD | s |
| Accuracy (GNSS) | CEP-50 | Autonomous @ open sky | TBD | m |

**NOTES**

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after the loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

# 5 Antenna Connection

RM502Q-GL provides four antenna interfaces, the impedance of antenna port is 50 Ω.

## 5.1. RF Antenna Interfaces

### 5.1.1. Antenna Pin Definition

The pin definition of RF antenna interfaces is shown below.

**Table 23: Pin Definition of RF Antenna Interfaces**

| Pin Name | I/O | Description | Comment |
|---|---|---|---|
| ANT0 | AI/AO | Antenna0 interface, 5GNR (n41/n77/n78 TRx1) & LTE LMHB TRx0 & B42/B43/B48 MIMO1 | 50 Ω impedance |
| ANT1 | AI/AO | Antenna1 interface, 5GNR (n77/n78 DRx) & n41 TRx0 & LTE MHB MIMO1 & B42/B43/B48 DRX & LAA PRx | 50 Ω impedance |
| ANT2_ GNSSL1 | AI/AO | Antenna2 interface, 5GNR (n77/n78 MIMO2, n41 DRx) & LTE MHB MIMO2 & B42/B43/B48 MIMO2 & LAA DRx & GNSS L1 | 50 Ω impedance |
| ANT3 | AI/AO | Antenna3 interface, 5GNR (n77/n78 TRx0, n41 MIMO2) & LTE LMHB DRx & B42/B43/B48 TRx0 | 50 Ω impedance |

**NOTE**

LTE LMHB TRx0 also supports 5G NR FDD low, middle and high bands in SA mode (under development).

### 5.1.2. RF Antenna Port Mapping

**Table 24: RM502Q-GL RF Antenna Mapping**

| 4G | 5G NR | | Antenna | LB (MHz) | MHB (MHz) | n77/78 (MHz) | NOTE |
|---|---|---|---|---|---|---|---|
| | n41 | n77/n78 | | | | | |
| LB/MHB TRx0, B42/B43/B48 MIMO1 | TRx1 | TRx1 | ANT0 | 617 to 960 | 1452 to 2690 | 3300 to 4200 | |
| LB/MHB DRx, B42/B43/B48 TRx0 | Div1 | TRx0 | ANT3 | 617 to 960 | 1452 to 2690 | 3300 to 4200 | |
| MHB PRx MIMO, B42/B43/B48 DRX, LAA PRX | TRx0 | Div0 | ANT1 | – | 1452 to 2690 | 3300 to 4200 | |
| MHB DRx MIMO, B42/B43/B48 MIMO2, LAA DRx | Div0 | Div1 | ANT2_ GNSSL1 | – | 1452 to 2690 | 3300 to 4200 | |

n77 group also includes B42/B48 function.

### 5.1.3. Operating Frequency

**Table 25: RM502Q-GL Module Operating Frequencies**

| Band Name | Transmit (MHz) | Receive (MHz) | LTE-FDD | LTE-TDD | UMTS | 5G NR |
|---|---|---|---|---|---|---|
| IMT (2100) | 1920–1980 | 2110–2170 | B1 | – | B1 | n1 |
| PCS (1900) | 1850–1910 | 1930–1990 | B2 | – | B2 | n2 |
| DCS (1800) | 1710–1785 | 1805–1880 | B3 | – | B3 | n3 |
| AWS | 1710–1755 | 2110–2155 | B4 | – | B4 | – |
| Cell (850) | 824–849 | 869–894 | B5 | – | B5 | n5 |
| JCELL (800) | 830–840 | 875–885 | – | – | B6 | – |

| | | | | | | |
|---|---|---|---|---|---|---|
| IMT-E (2600) | 2500–2570 | 2620–2690 | B7 | – | – | n7 |
| EGSM (950) | 880–915 | 925–960 | B8 | – | B8 | n8 |
| J1700 | 1750–1785 | 1845–1880 | B9 | – | B9 | – |
| 700 lower A–C | 699–716 | 729–746 | B12 | – | – | n12 |
| 700 upper C | 777–787 | 746–756 | B13 | – | – | – |
| 700 D | 788–798 | 758–768 | B14 | – | – | – |
| B17 | 704–716 | 734–746 | B17 | – | – | – |
| B18 | 815–830 | 860–875 | B18 | – | – | – |
| B19 | 830–845 | 875–890 | B19 | – | B19 | – |
| EU800 | 832–862 | 791–821 | B20 | – | – | n20 |
| PCS + G | 1850–1915 | 1930–1995 | B25 | – | – | – |
| B26 | 814–849 | 859–894 | B26 | – | – | – |
| 700 APAC | 703–748 | 758–803 | B28 | – | – | n28 |
| FLO | – | 717–728 | B29 | – | – | – |
| WCS | 2305–2315 | 2350–2360 | B30 | – | – | – |
| L-band | – | 1452–1496 | B32 | – | – | – |
| B34 | 2010–2025 | 2010–2025 | – | B34 | – | – |
| B38 | 2570–2620 | 2570–2620 | – | B38 | – | n38 |
| B39 | 1880–1920 | 1880–1920 | – | B39 | – | – |
| B40 | 2300–2400 | 2300–2400 | – | B40 | – | n40 |
| B41/B41-XGP | 2496–2690 | 2496–2690 | – | B41 | – | n41 |
| B42 | 3400–3600 | 3400–3600 | – | B42 | – | – |
| B43 | 3600–3800 | 3600–3800 | – | B43 | – | – |
| B46 | 5150–5925 | 5150–5925 | – | B46 | – | – |
| B48 | 3550–3700 | 3550–3700 | – | B48 | – | n48 |
| B66 | 1710–1780 | 2110–2200 | B66 | – | – | n66 |
| B71 | 663–698 | 617–652 | B71 | – | – | n71 |
| n77 | 3300 – 4200 | 3300 – 4200 | – | – | – | n77 |

| | | | | | | |
|---|---|---|---|---|---|---|
| n78 | 3300 – 3800 | 3300 – 3800 | – | – | – | n78 |

### 5.1.4. Reference Design of RF Antenna Interface

A reference design of antenna interface is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

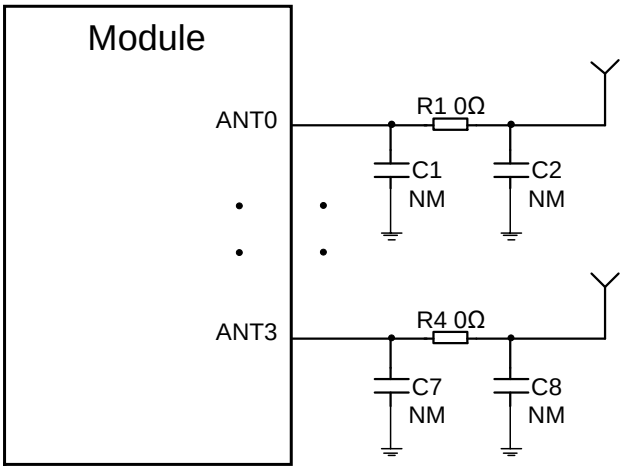



**Figure 30: Reference Circuit of RF Antenna**

**NOTES**

1. Keep the characteristic impedance for antenna trace as 50 Ω.
2. Place the π-type matching components as close to the antenna as possible.
3. Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antenna traces.
4. Keep 75 dB PCB isolation between two antenna traces.
5. Keep 15 dB isolation between each antenna to improve the receiving sensitivity.
6. It is suggested to keep 20 dB isolation between 5G NR UL MIMO Tx0 and Tx1 antennas.

## 5.2. GNSS Antenna Interface

The following table shows frequency specification of GNSS antenna connector.

**Table 26: GNSS Frequency**

| Type | Frequency | Unit |
|---|---|---|
| GPS/Galileo/QZSS | 1575.42 ±1.023 (L1) | MHz |
| Galileo | 1575.42 ±2.046 (E1) | MHz |
| QZSS | 1575.42 (L1) | MHz |
| GLONASS | 1597.5–1605.8 | MHz |
| BeiDou | 1561.098 ±2.046 | MHz |

**NOTES**

1. Keep the characteristic impedance for ANT_GNSS trace as 50 Ω.
2. Place the π-type matching components as close to the antenna as possible.
3. Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antenna traces.
4. Keep 75 dB isolation between two antenna traces.
5. Keep 15 dB isolation between each antenna to improve the receiving sensitivity.

## 5.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the signal layer to reference ground (H), and the space between RF trace and ground (S). Microstrip or coplanar waveguide is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

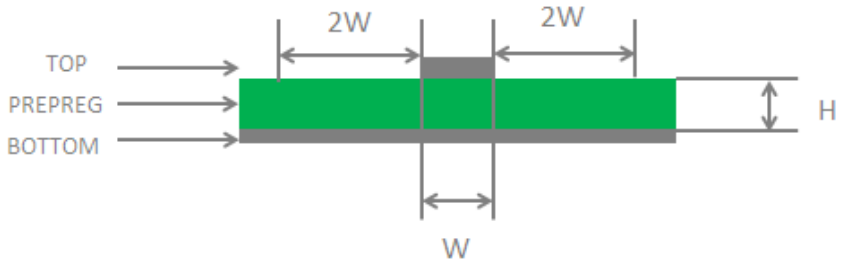



**Figure 31: Microstrip Design on a 2-layer PCB**

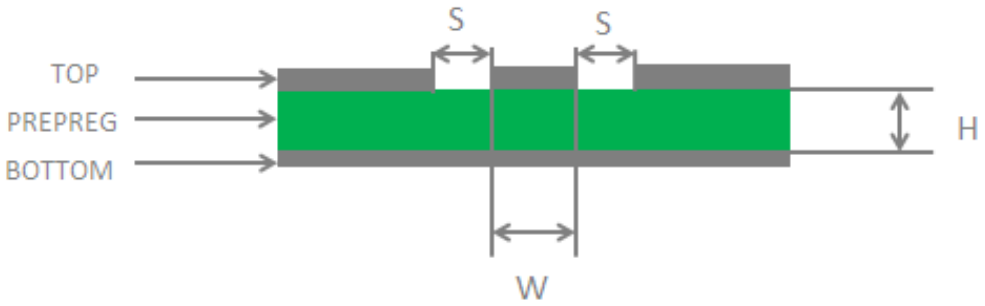



**Figure 32: Coplanar Waveguide Design on a 2-layer PCB**

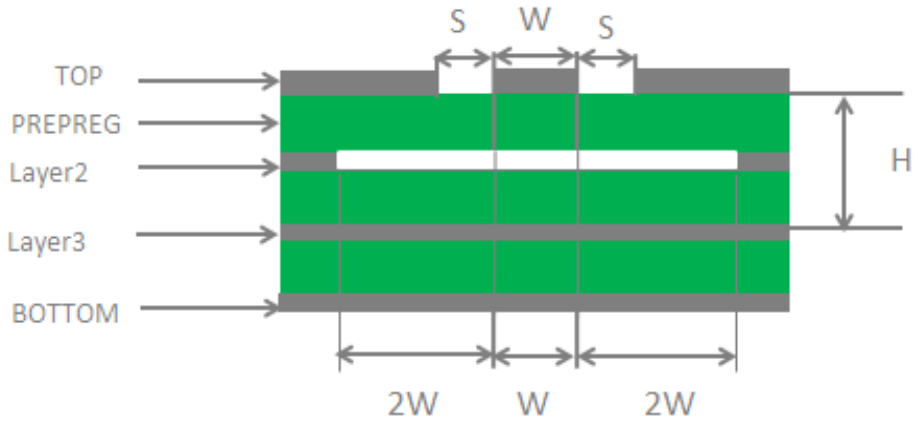



**Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)**

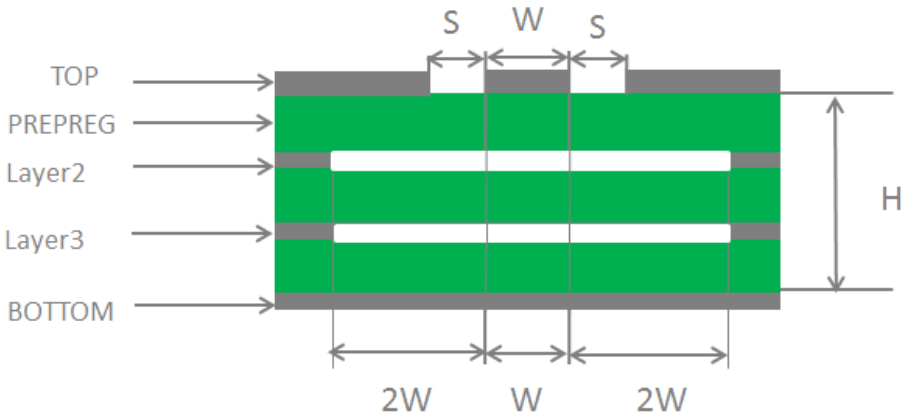



**Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible. All the right angle traces should be changed to curved ones, and the recommended angle is 135°.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground improves RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [4]***.

## 5.4. Antenna Connectors

The ANT0, ANT1, ANT2_GNSSL1 and ANT3 antenna connectors are shown as below.


**Figure 35: Antenna Connectors on the Module**

### 5.4.1 RF Bands Supported by Antenna Connectors

**Table 27: RF Bands Supported by RM502Q-GL Antenna Connectors**

| Pin Name | Description | Frequency |
|---|---|---|
| ANT0 | Antenna0 interface, 5GNR (n41/n77/n78 TRx1) & LTE LMHB TRx0 & B42/B43/B48 MIMO1 | 600–5000 MHz |
| ANT1 | Antenna1 interface, 5GNR (n77/n78 DRx) & N41 TRx0 & LTE MHB MIMO1 & B42/B43/B48 DRX & LAA PRx | 1100–6000 MHz |
| ANT2_GNSSL1 | Antenna2 interface, 5GNR (n77/n78 MIMO2, N41 DRx) & LTE MHB MIMO2 & B42/B43/B48 MIMO2 & LAA DRx & GNSS L1 | 1400–6000 MHz |
| ANT3 | Antenna3 interface, 5GNR (n77/n78 TRx0, N41 MIMO2) & LTE LMHB DRx & B42/B43/B48 TRX | 600–5000 MHz |

**NOTE**

n77 group also includes B42/B48 function.

## 5.5. Antenna Installation

### 5.5.1. Antenna Requirements

The following table shows the requirements on WCDMA, LTE, 5G NR antenna and GNSS antenna.

**Table 28: Antenna Requirements**

| Type | Requirements |
|---|---|
| GNSS | Frequency range: 1559–1606 MHz<br>Polarization: RHCP or linear<br>VSWR: < 2 (Typ.)<br>Passive antenna gain: >0 dBi |
| WCDMA/LTE/5G NR | VSWR: ≤ 3<br>Efficiency: > 30%<br>Input Impedance: 50 Ω<br>WCDMA LB, LTE LB: Cable insertion loss: < 1 dB<br>WCDMA MB, LTE MB: Cable insertion loss: < 1.5 dB<br>LTE HB, 5G NR TDD MHB: Cable insertion loss < 2 dB |

### 5.5.2. Recommended RF Connector for Antenna Installation

RM502Q-GL is mounted with standard 2 mm × 2 mm receptacle RF connectors for convenient antenna connection.

The connector dimensions are illustrated as below:

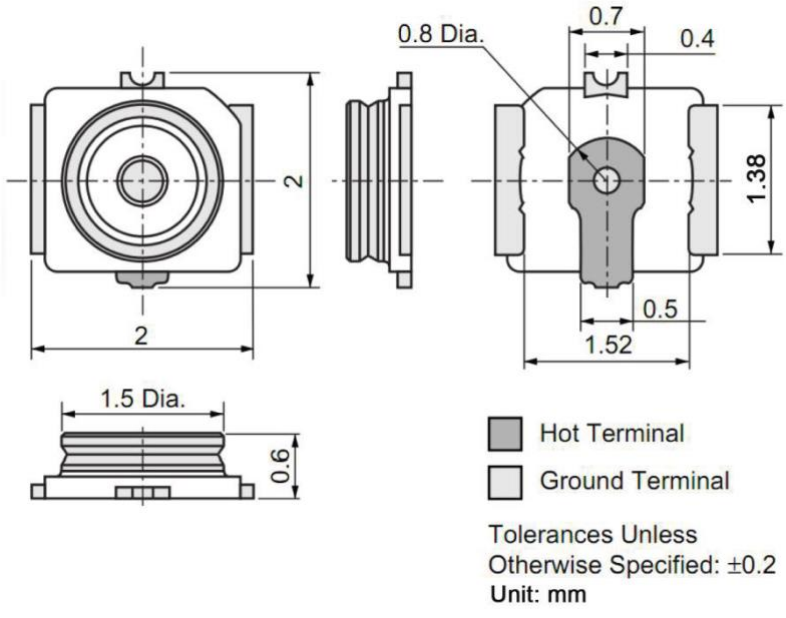


**Figure 36: RM502Q-GL RF Connector Dimensions (Unit: mm)**

**Table 29: Major Specifications of the RF Connector**

| Item | Specification |
|---|---|
| Nominal Frequency Range | DC to 6 GHz |
| Nominal Impedance | 50 Ω |
| Temperature Rating | -40°C to +85°C |
| Voltage Standing Wave Ratio (VSWR) | Meet the requirements of:<br>Max 1.3 (DC–3 GHz)<br>Max 1.45 (3–6 GHz) |

The receptacle RF connector used in conjunction with RM502Q-GL will accept two types of mating plugs that will meet a maximum height of 1.2 mm using a Ø0.81 mm coaxial cable or a maximum height of 1.45 mm utilizing a Ø1.13 mm coaxial cable.

The following figure shows the specifications of mating plugs using Ø0.81 mm coaxial cables.

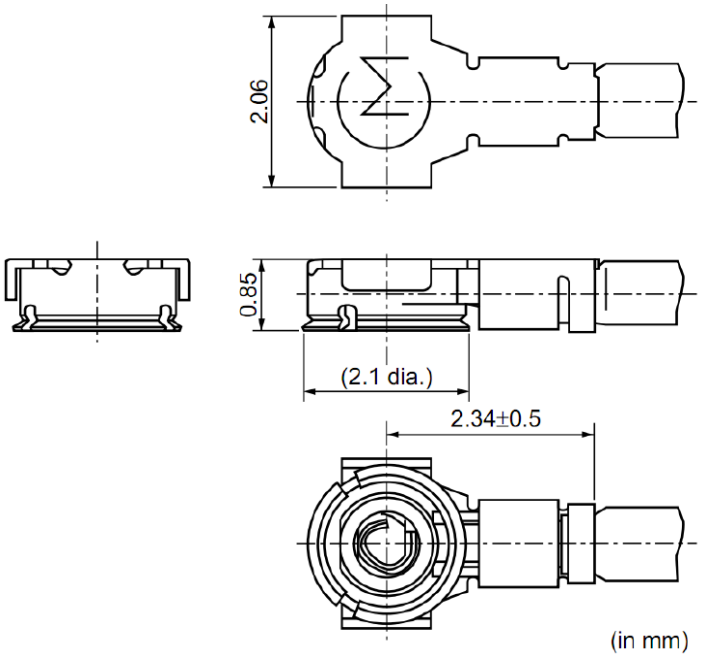



**Figure 37: Specifications of Mating Plugs Using Ø0.81 mm Coaxial Cables**

The following figure illustrates the connection between the receptacle RF connector on RM502Q-GL and the mating plug using a Ø0.81 mm coaxial cable.

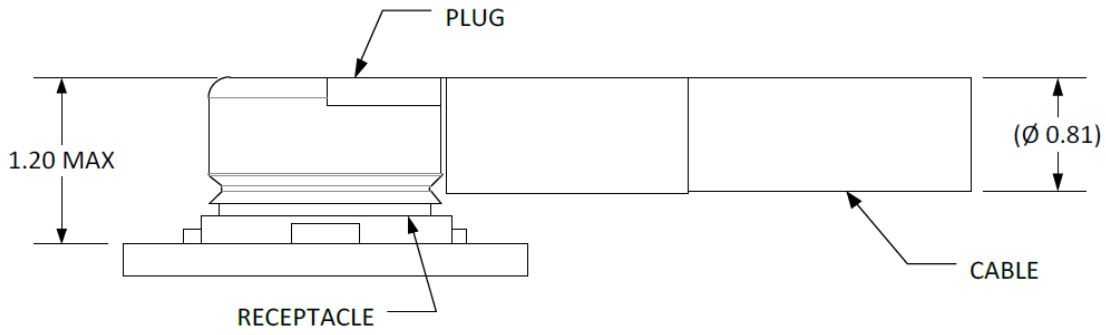



**Figure 38: Connection between RF Connector and Mating Plug Using Ø0.81 mm Coaxial Cable**

The following figure illustrates the connection between the receptacle RF connector on RM502Q-GL and the mating plug using a Ø1.13 mm coaxial cable.

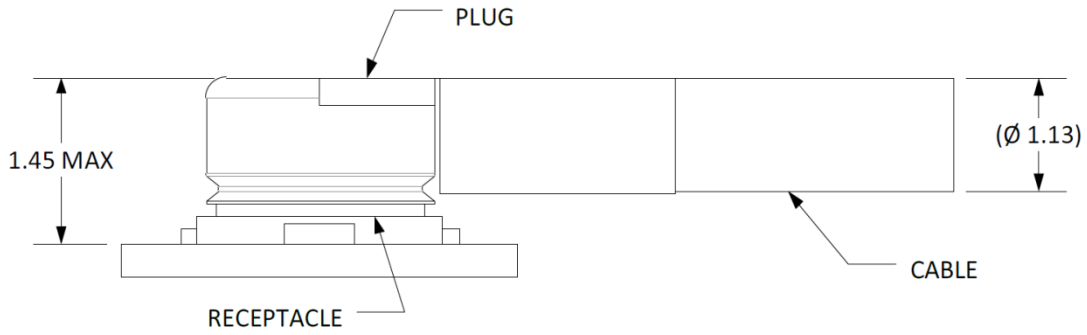



**Figure 39: Connection between RF Connector and Mating Plug Using Ø1.13 mm Coaxial Cable**

# 6 Electrical, Reliability and Radio Characteristics

## 6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

**Table 30: Absolute Maximum Ratings**

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| VCC | -0.3 | 4.7 | V |
| Voltage at Digital Pins | -0.3 | 2.3 | V |

## 6.2. Power Supply Requirements

The typical input voltage of RM502Q-GL is 3.7 V, as specified by *PCIe M.2 Electromechanical Specification Rev 1.0*. The following table shows the power supply requirements of RM502Q-GL.

**Table 31: Power Supply Requirements**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Power Supply | 3.135 | 3.7 | 4.4 | V |
| Voltage Ripple | | – | 30 | 100 | mV |
| Voltage Drop | | – | – | 165 | mV |

## 6.3. I/O Requirements

**Table 32: I/O Requirements**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7 × $V_{DD18}$ [1)] | $V_{DD18}$ +0.3 | V |
| $V_{IL}$ | Input low voltage | -0.3 | 0.3 × $V_{DD18}$ | V |
| $V_{OH}$ | Output high voltage | $V_{DD18}$-0.5 | $V_{DD18}$ | V |
| $V_{OL}$ | Output low voltage | 0 | 0.4 | V |

**NOTE**

[1)] $V_{DD18}$ is the I/O power domain of the module.

## 6.4. Operation and Storage Temperatures

**Table 33: Operation and Storage Temperatures**

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Operation Temperature Range[1)] | -30 | +25 | +60 | ºC |
| Extended Temperature Range[2)] | -40 | +25 | +85 | ºC |
| Storage temperature Range | -40 | +25 | +90 | ºC |

**NOTES**

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like $P_{out}$ might reduce in their values and exceed the specified tolerances. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

## 6.5. Current Consumption

**Table 34: RM502Q-GL Current Consumption**

| Parameter | Description | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $I_{VBAT}$ | OFF state | **Power down** | TBD | μA |
| | Sleep state | **AT+CFUN=0** (USB disconnected) | TBD | mA |
| | | WCDMA PF = 64 (USB disconnected) | TBD | mA |
| | | WCDMA PF = 128 (USB disconnected) | TBD | mA |
| | | WCDMA PF = 512 (USB disconnected) | TBD | mA |
| | | LTE-FDD PF = 32 (USB disconnected) | TBD | mA |
| | | LTE-FDD PF = 64 (USB disconnected) | TBD | mA |
| | | LTE-FDD PF = 128 (USB disconnected) | TBD | mA |
| | | LTE-TDD PF = 32 (USB disconnected) | TBD | mA |
| | | LTE-TDD PF = 64 (USB disconnected) | TBD | mA |
| | | LTE-TDD PF = 128 (USB disconnected) | TBD | mA |
| | Idle state | WCDMA PF = 64 (USB disconnected) | TBD | mA |
| | | WCDMA PF = 64 (USB connected) | TBD | mA |
| | | LTE-FDD PF = 64 (USB disconnected) | TBD | mA |
| | | LTE-FDD PF = 64 (USB connected) | TBD | mA |
| | | LTE-TDD PF = 64 (USB disconnected) | TBD | mA |
| | | LTE-TDD PF = 64 (USB connected) | TBD | mA |
| $I_{VBAT}$ | WCDMA data transfer (GNSS OFF) | WCDMA B1 HSDPA CH10700 @ 23 dBm | TBD | mA |
| | | WCDMA B1 HSUPA CH10700 @ 23 dBm | TBD | mA |
| | | WCDMA B2 HSDPA CH9800 @ 23 dBm | TBD | mA |
| | | WCDMA B2 HSUPA CH9800 @ 23 dBm | TBD | mA |

| | | | | |
|---|---|---|---|---|
| $I_{VBAT}$ | WCDMA data transfer (GNSS OFF) | WCDMA B3 HSDPA CH1338 @ 23 dBm | TBD | mA |
| | | WCDMA B3 HSUPA CH1338 @ 23 dBm | TBD | mA |
| | | WCDMA B4 HSDPA CH1638 @ 23 dBm | TBD | mA |
| | | WCDMA B4 HSUPA CH1638 @ 23 dBm | TBD | mA |
| | | WCDMA B5 HSDPA CH4407 @ 23 dBm | TBD | mA |
| | | WCDMA B5 HSUPA CH4407 @ 23 dBm | TBD | mA |
| | | WCDMA B6 HSDPA CH4400 @ 23 dBm | TBD | mA |
| | | WCDMA B6 HSUPA CH4400 @ 23 dBm | TBD | mA |
| | | WCDMA B8 HSDPA CH3012 @ 23 dBm | TBD | mA |
| | | WCDMA B8 HSUPA CH3012 @ 23 dBm | TBD | mA |
| | | WCDMA B19 HSDPA CH738 @ 23 dBm | TBD | mA |
| | | WCDMA B19 HSUPA CH738 @ 23 dBm | TBD | mA |
| $I_{VBAT}$ | LTE data transfer (GNSS OFF) | LTE-FDD B1 CH300 @ 23 dBm | TBD | mA |
| | | LTE-FDD B2 CH900 @ 23 dBm | TBD | mA |
| | | LTE-FDD B3 CH1575 @ 23 dBm | TBD | mA |
| | | LTE-FDD B4 CH2175 @ 23 dBm | TBD | mA |
| | | LTE-FDD B5 CH2525 @ 23 dBm | TBD | mA |
| | | LTE-FDD B7 CH3100 @ 23 dBm | TBD | mA |
| | | LTE-FDD B8 CH3625 @ 23 dBm | TBD | mA |
| | | LTE-FDD B9 CH3975 @ 23 dBm | TBD | mA |
| | | LTE-FDD B12 CH5095 @ 23 dBm | TBD | mA |
| | | LTE-FDD B13 CH5230 @ 23 dBm | TBD | mA |
| | | LTE-FDD B14 CH5330 @ 23 dBm | TBD | mA |
| | | LTE-FDD B17 CH5790 @ 23 dBm | TBD | mA |
| | | LTE-FDD B18 CH5925 @ 23 dBm | TBD | mA |
| | | LTE-FDD B19 CH6075 @ 23 dBm | TBD | mA |

| | | | | |
|---|---|---|---|---|
| $I_{VBAT}$ | LTE Data transfer (GNSS OFF) | LTE-FDD B20 CH6300 @ 23 dBm | TBD | mA |
| | | LTE-FDD B25 CH8365 @ 23 dBm | TBD | mA |
| | | LTE-FDD B26 CH8865 @ 23 dBm | TBD | mA |
| | | LTE-FDD B28 CH9435 @ 23 dBm | TBD | mA |
| | | LTE-FDD B30 CH9820 @ 23 dBm | TBD | mA |
| | | LTE-TDD B34 CH36275 @ 23 dBm | TBD | mA |
| | | LTE-TDD B38 CH38000 @ 23 dBm | TBD | mA |
| | | LTE-TDD B39 CH38450 @ 23 dBm | TBD | mA |
| | | LTE-TDD B40 CH39150 @ 23 dBm | TBD | mA |
| | | LTE-TDD B41 CH40620 @ 23 dBm | TBD | mA |
| | | LTE-TDD B42 CH42590 @ 23 dBm | TBD | mA |
| | | LTE-TDD B43 CH44590 @ 23 dBm | TBD | mA |
| | | LTE-TDD B48 CH55990 @ 23 dBm | TBD | mA |
| | | LTE-FDD B66 CH66886 @ 23 dBm | TBD | mA |
| | | LTE-FDD B71 CH68761 @ 23 dBm | TBD | mA |
| $I_{VBAT}$ | 5G NR data transfer (GNSS OFF) | 5G NR-TDD n41 CH501204 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n41 CH518598 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n41 CH535998 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n77 CH620668 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n77 CH650000 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n77 CH679332 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n78 CH620668 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n78 CH636666 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n78 CH652666 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n1 CH423000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n1 CH428000 @ 23 dBm | TBD | mA |

| | | | | |
|---|---|---|---|---|
| $I_{VBAT}$ | 5G NR data transfer (GNSS OFF) | 5G NR-FDD n1 CH433000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n2 CH387000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n2 CH392000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n2 CH397000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n3 CH362000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n3 CH368500 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n3 CH375000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n5 CH174800 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n5 CH176300 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n5 CH177800 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n7 CH525000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n7 CH531000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n7 CH537000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n8 CH186000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n8 CH188500 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n8 CH191000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n12 CH146800 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n12 CH147500 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n12 CH148200 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n20 CH159200 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n20 CH161200 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n20 CH163200 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n28 CH152600 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n28 CH156100 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n28 CH159600 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n38 CH515000 @ 23 dBm | TBD | mA |

| | | | | |
|---|---|---|---|---|
| $I_{VBAT}$ | 5G NR data transfer (GNSS OFF) | 5G NR-TDD n38 CH519000 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n38 CH523000 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n40 CH461000 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n40 CH470000 @ 23 dBm | TBD | mA |
| | | 5G NR-TDD n40 CH479000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n66 CH423000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n66 CH429000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n66 CH435000 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n71 CH124400 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n71 CH126900 @ 23 dBm | TBD | mA |
| | | 5G NR-FDD n71 CH129400 @ 23 dBm | TBD | mA |
| $I_{VBAT}$ | WCDMA voice call | WCDMA B1 CH10700 @ 23 dBm | TBD | mA |
| | | WCDMA B2 CH9800 @ 23 dBm | TBD | mA |
| | | WCDMA B3 CH1338 @ 23 dBm | TBD | mA |
| | | WCDMA B4 CH1638 @ 23 dBm | TBD | mA |
| | | WCDMA B5 CH4408 @ 23 dBm | TBD | mA |
| | | WCDMA B6 CH4175 @ 23 dBm | TBD | mA |
| | | WCDMA B8 CH3012 @ 23 dBm | TBD | mA |
| | | WCDMA B19 CH338 @ 23 dBm | TBD | mA |

## 6.6. RF Output Power

The following table shows the RF output power of RM502Q-GL module.

**Table 35: RF Output Power**

| Mode | Frequency | Max. | Min. |
|---|---|---|---|
| WCDMA | WCDMA bands | 24 dBm +1/-3 dB (Class 3) | < -50 dBm |
| LTE | LTE bands | 23 dBm ±2 dB (Class 3) | < -40 dBm |
| | LTE HPUE bands (B38/B40/B41/B42/B43) | 26 dBm ±2 dB (Class 2) | < -40 dBm |
| 5G NR | 5G NR bands | 23 dBm ±2 dB (Class 3) | < -40 dBm (BW: 5–20 MHz)[1)] |
| | 5G NR HUPE bands (n41/n77/n78) | 26 dBm +2/-3 dB (Class 2) | < -40 dBm (BW: 5–20 MHz)[1)] |

**NOTE**

[1)] For 5G NR TDD bands, the normative reference for this requirement is *TS 38.101-1 [2] clause 6.3.1*

## 6.7. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of RM502Q-GL module.

**Table 36: RM502Q-GL Conducted RF Receiving Sensitivity**

| Mode | Frequency | Primary | Diversity | SIMO[1)] | 3GPP (SIMO) |
|---|---|---|---|---|---|
| WCDMA | WCDMA B1 | TBD | TBD | TBD | -106.7 dBm |
| | WCDMA B2 | TBD | TBD | TBD | -104.7 dBm |
| | WCDMA B3 | TBD | TBD | TBD | -103.7 dBm |
| | WCDMA B4 | TBD | TBD | TBD | -106.7 dBm |
| | WCDMA B5 | TBD | TBD | TBD | -104.7 dBm |
| WCDMA | WCDMA B8 | TBD | TBD | TBD | -103.7 dBm |
| | WCDMA B19 | TBD | TBD | TBD | -104.7 dBm |
| LTE | LTE-FDD B1 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-FDD B2 (10 MHz) | TBD | TBD | TBD | -94.3 dBm |
| | LTE-FDD B3 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |
| | LTE-FDD B4 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-FDD B5 (10 MHz) | TBD | TBD | TBD | -94.3 dBm |
| | LTE-FDD B7 (10 MHz) | TBD | TBD | TBD | -94.3 dBm |
| | LTE-FDD B8 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |
| | LTE-FDD B9 (10 MHz) | TBD | TBD | TBD | -95.3 dBm |
| | LTE-FDD B12 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |
| | LTE-FDD B13 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |
| | LTE-FDD B14 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |
| | LTE-FDD B17 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |
| | LTE-FDD B18 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-FDD B19 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-FDD B20 (10 MHz) | TBD | TBD | TBD | -93.3 dBm |

| | | | | | |
|---|---|---|---|---|---|
| LTE | LTE-FDD B25 (10 MHz) | TBD | TBD | TBD | -92.8 dBm |
| | LTE-FDD B26 (10 MHz) | TBD | TBD | TBD | -93.8 dBm |
| | LTE-FDD B28 (10 MHz) | TBD | TBD | TBD | -94.8 dBm |
| | LTE-FDD B30 (10 MHz) | TBD | TBD | TBD | -95.3 dBm |
| | LTE-FDD B32 (10 MHz) | TBD | TBD | TBD | -95.3 dBm |
| | LTE-TDD B34 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-TDD B38 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-TDD B39 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-TDD B40 (10 MHz) | TBD | TBD | TBD | -96.3 dBm |
| | LTE-TDD B41 (10 MHz) | TBD | TBD | TBD | -94.3 dBm |
| | LTE-TDD B42 (10 MHz) | TBD | TBD | TBD | -95 dBm |
| | LTE-TDD B43 (10 MHz) | TBD | TBD | TBD | -95 dBm |
| | LTE-TDD B48 (10 MHz) | TBD | TBD | TBD | -95 dBm |
| 5G NR | 5G NR-FDD n1 (20 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -94.0 dBm |
| | 5G NR-FDD n2 (20 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -92.0 dBm |
| | 5G NR-FDD n3 (20 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -91.0 dBm |
| | 5G NR-FDD n5 (10 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -95.0 dBm |
| | 5G NR-FDD n7 (20 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -92.0 dBm |
| | 5G NR-FDD n8 (10 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -94.0 dBm |
| | 5G NR-FDD n12 (10 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -94.0 dBm |
| | 5G NR-FDD n20 (10 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -94.0 dBm |
| | 5G NR-FDD n25 (20 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -90.5 dBm |
| | 5G NR-FDD n28 (10 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -96.0 dBm |
| | 5G NR-TDD n38 (20 MHz) (SCS: 30 kHz) | TBD | TBD | TBD | -94.0 dBm |
| | 5G NR-TDD n40 (20 MHz) (SCS: 30 kHz) | TBD | TBD | TBD | -94.0 dBm |

| | | | | | |
|---|---|---|---|---|---|
| | 5G NR-TDD n41 (20 MHz) (SCS: 30 kHz) | TBD | TBD | TBD | -92.0 dBm |
| | 5G NR-FDD n66 (20 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -93.5 dBm |
| | 5G NR-FDD n71 (10 MHz) (SCS: 15 kHz) | TBD | TBD | TBD | -94.0 dBm |
| | 5G NR-TDD n77 (20 MHz) (SCS: 30 kHz) | TBD | TBD | TBD | -92.9 dBm |
| | 5G NR-TDD n78 (20 MHz) (SCS: 30 kHz) | TBD | TBD | TBD | -92.9 dBm |

**NOTE**

[1] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which improves Rx performance.

## 6.8. ESD Characteristics

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

**Table 37: Electrostatic Discharge Characteristics (Temperature: 25ºC, Humidity: 40%)**

| Tested Interfaces | Contact Discharge | Air Discharge | Unit |
|---|---|---|---|
| VCC, GND | ±5 | ±10 | kV |
| Antenna Interfaces | ±4 | ±8 | kV |
| Other Interfaces | ±0.5 | ±1 | kV |

## 6.9. Thermal Dissipation

RM502Q-GL is designed to work over an extended temperature range. In order to achieve a maximum performance while working under extended temperatures or extreme conditions (such as with maximum power or data rate) for a long time, it is strongly recommended to add a thermal pad or other thermally

conductive compounds between the module and the main PCB for thermal dissipation.

The thermal dissipation area (i.e. the area for adding thermal pad) is shown as below. The dimensions are measured in mm.

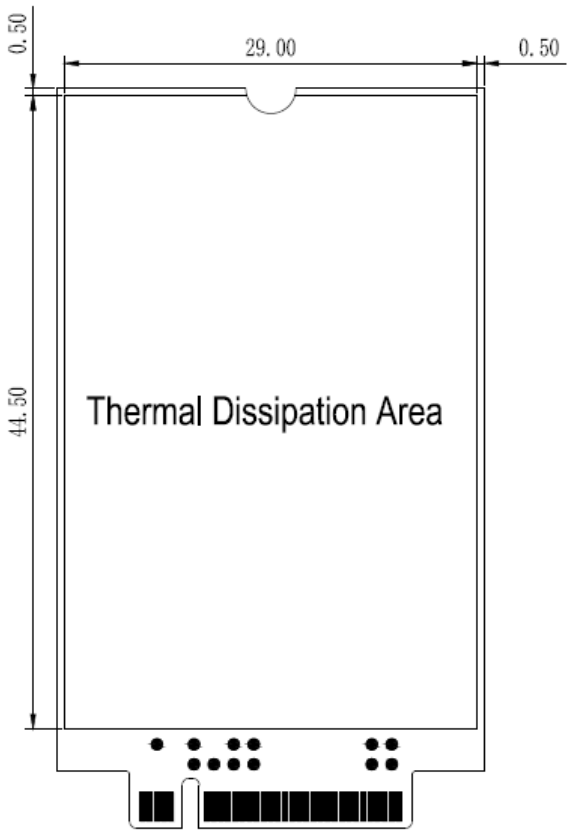



**Figure 40: Thermal Dissipation Area on Bottom Side of Module (Bottom View)**

There are other measures to enhance heat dissipation performance:

- Add ground vias as many as possible on PCB.
- Maximize airflow over/around the module.
- Place the module away from other heating sources.
- Module mounting holes must be used to attach (ground) the device to the main PCB ground.
- It is NOT recommended to apply solder mask on the main PCB where the module's thermal dissipation area is located.
- Select an appropriate material, thickness and surface for the outer housing (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.
- Customers may also need active cooling to pull heat away from the module.
- If possible, add a heatsink on the top of the module. A thermal pad should be used between the heatsink and the module, and the heatsink should be designed with as many fins as possible to increase heat dissipation area.

**NOTE**

For more detailed guidelines on thermal design, please refer to ***document [5]***.

# 7 Mechanical Dimensions and Packaging

This chapter mainly describes mechanical dimensions and packaging specifications of RM502Q-GL module. All dimensions are measured in mm, and the tolerances are ±0.05 mm unless otherwise specified.

## 7.1. Mechanical Dimensions of the Module

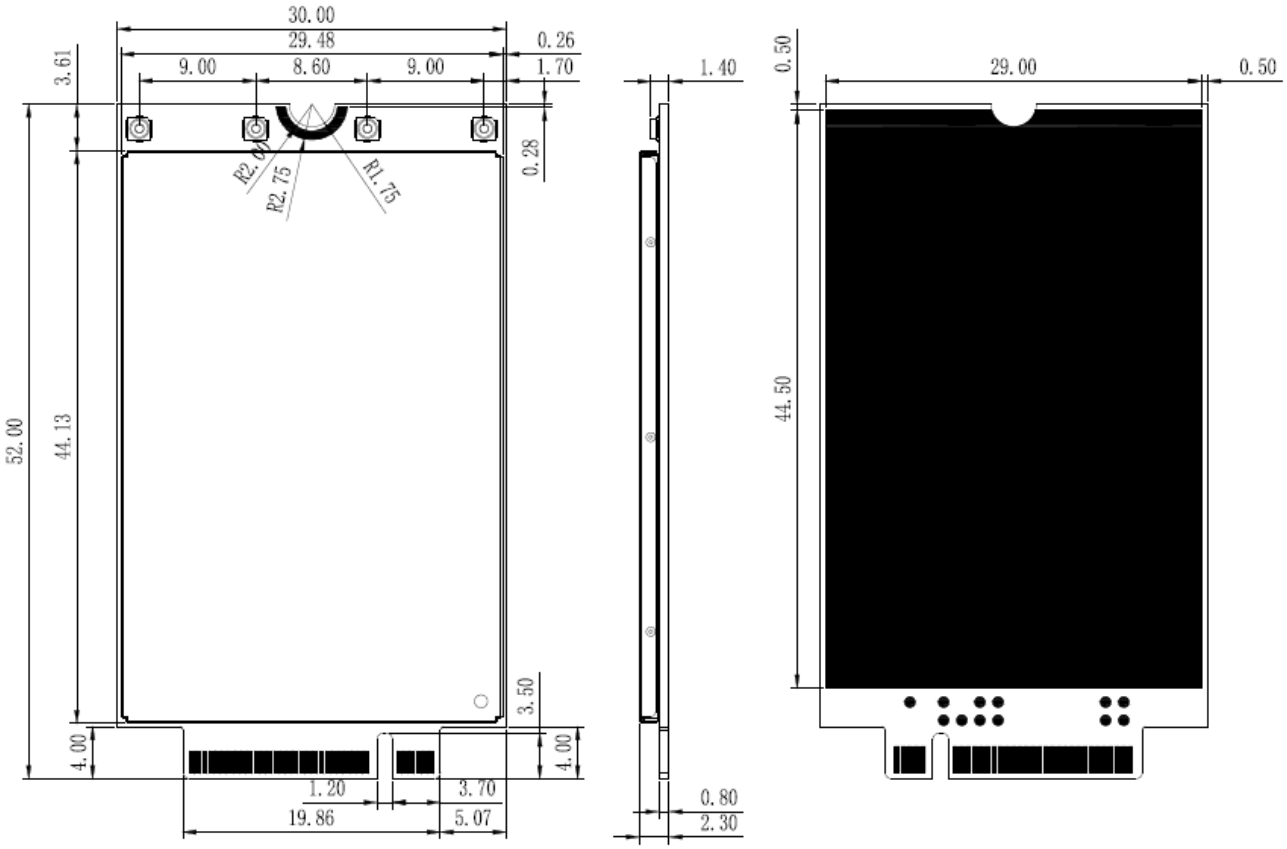
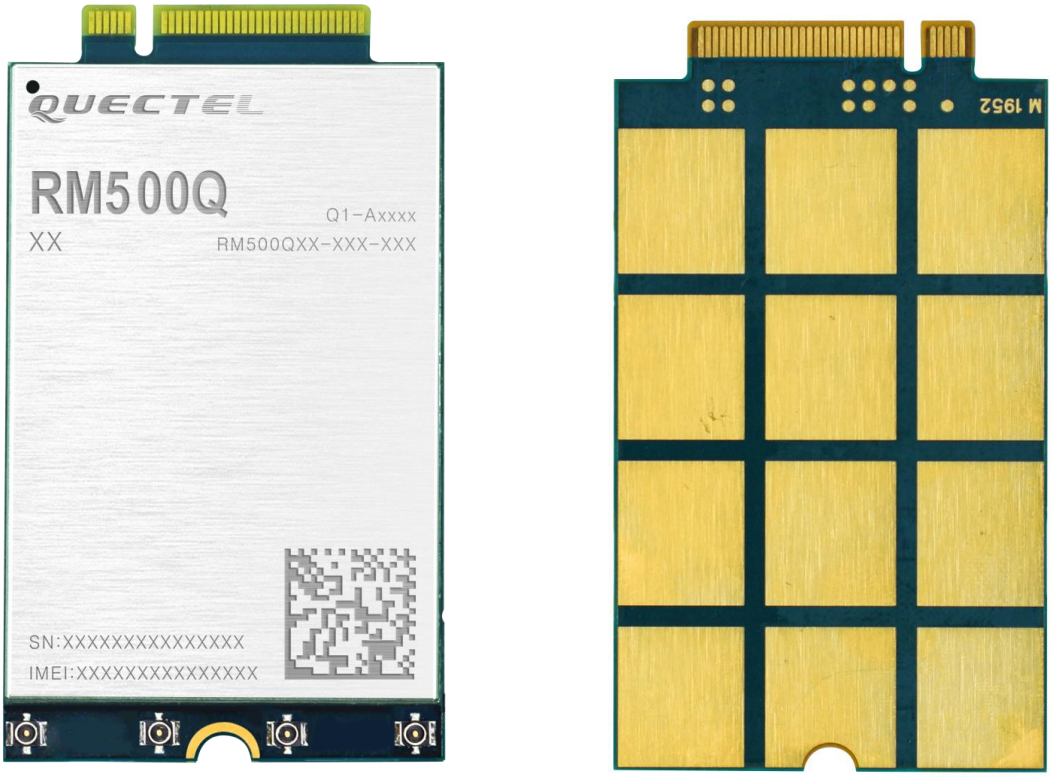



**Figure 41: Mechanical Dimensions of RM502Q-GL (Unit: mm)**

## 7.2. Top and Bottom Views of the Module




**Top View** **Bottom View**

**Figure 42: Top and Bottom Views of the Module**

**NOTE**

These are rendering images of RM502Q-GL module. For authentic appearance, please refer to the module that you receive from Quectel.

## 7.3. M.2 Connector

RM502Q-GL adopts a standard PCI Express M.2 connector which compiles with the directives and standards listed in ***document [4]***.

## 7.4. Packaging

RM502Q-GL modules are packaged in trays. The following figure shows the tray size.

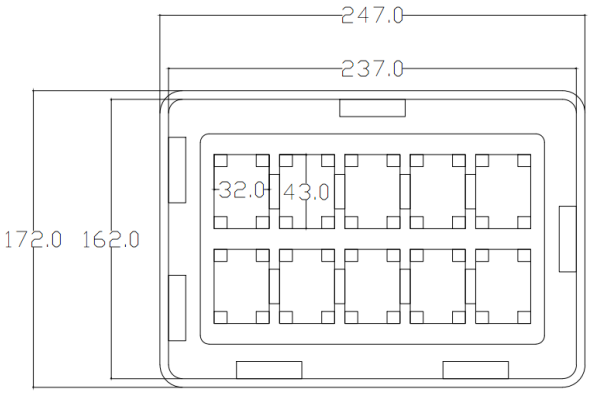



**Figure 43: Tray Size (Unit: mm)**

Each tray contains 10 modules. The smallest package contains 100 modules. Tray packaging procedures are as below.

1. Use 10 trays to package 100 modules at a time (tray size: 247 mm × 172 mm).
2. Place an empty tray on the top of the 10-tray stack.
3. Fix the stack with masking tape in "#" shape as shown in the following figure.
4. Pack the stack with conductive bag, and then fix the bag with masking tape.
5. Place the list of IMEI No. into a small carton.
6. Seal the carton and then label the seal with sealing sticker (small carton size: 250 mm × 175 mm × 128 mm).


**Figure 44: Tray Packaging Procedure**

# 8 Appendix References

**Table 38: Related Documents**

| SN. | Document Name | Remark |
|---|---|---|
| [1] | Quectel_PCIe_Card_EVB_User_Guide | PCIe card EVB user guide |
| [2] | Quectel_RG500Q&RM502Q&RM510Q_AT_Commands_Manual | AT commands manual for RG500Q, RM502Q and RM510Q |
| [3] | Quectel_RM502Q_GNSS_Application_Note | RM502Q GNSS application note |
| [4] | Quectel_RF_Layout_Application_Note | RF layout application note |
| [5] | Quectel_RM502Q_Module_Thermal_Simulation | RM502Q module thermal simulation |
| [6] | PCI Express M.2 Specification Rev3.0 | PCI express M.2 specification |

**Table 39: Terms and Abbreviations**

| Abbreviation | Description |
|---|---|
| bps | Bit Per Second |
| CHAP | Challenge Handshake Authentication Protocol |
| DC-HSPA+ | Dual-carrier High Speed Packet Access+ |
| DFOTA | Delta Firmware Upgrade Over-The-Air |
| DL | Downlink |
| DPR | Dynamic Power Reduction |
| EIRP | Equivalent Isotropically Radiated Power |
| ESD | Electrostatic Discharge |
| FDD | Frequency Division Duplexing |

| | |
|---|---|
| GLONASS | Global Navigation Satellite System (Russia) |
| GNSS | Global Navigation Satellite System |
| GPS | Global Positioning System |
| GSM | Global System for Mobile Communications |
| HR | Half Rate |
| HSPA | High Speed Packet Access |
| HSUPA | High Speed Uplink Packet Access |
| kbps | Kilo Bits Per Second |
| LAA | License Assisted Access |
| LED | Light Emitting Diode |
| LTE | Long Term Evolution |
| Mbps | Mega Bits Per Second |
| ME | Mobile Equipment |
| MIMO | Multiple-Input Multiple-Output |
| MLCC | Multiplayer Ceramic Chip Capacitor |
| MMS | Multimedia Messaging Service |
| MO | Mobile Originated |
| MT | Mobile Terminated |
| PAP | Password Authentication Protocol |
| PCB | Printed Circuit Board |
| PCIe | Peripheral Component Interconnect Express |
| PCM | Pulse Code Modulation |
| PDU | Protocol Data Unit |
| PME | Power Management Event |
| PPP | Point-to-Point Protocol |

| | |
|---|---|
| RF | Radio Frequency |
| Rx | Receive |
| SAR | Specific Absorption Rate |
| SMS | Short Message Service |
| Tx | Transmit |
| UART | Universal Asynchronous Receiver & Transmitter |
| UL | Uplink |
| URC | Unsolicited Result Code |
| USB | Universal Serial Bus |
| (U)SIM | (Universal) Subscriber Identity Module |
| $V_{IH}$ | Input High Voltage Level |
| $V_{IL}$ | Input Low Voltage Level |
| $V_{OH}$ | Output High Voltage Level |
| $V_{OL}$ | Output Low Voltage Level |
| WCDMA | Wideband Code Division Multiple Access |

Installation engineers need to be aware of the potential risk of the thermal effects of radio frequency energy and how to stay protected against undue risk.
The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

## OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

## Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

## End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2021RM502QGL” “Contains IC: 10224A-2020RM502Q”. The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

## Antenna

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed

| Test Mode | Antenna Gain (dBi) | Test Mode | Antenna Gain (dBi) |
|---|---|---|---|
| WCDMA B2 | 8.00 | LTE B38 | 2.00 |
| WCDMA B4 | 5.00 | LTE B41 | 2.00 |
| WCDMA B5 | 5.00 | LTE B48 | -2.00 |
| LTE B2 | 8.00 | LTE B66 | 5.00 |
| LTE B4 | 5.00 | LTE B71 | 5.00 |
| LTE B5 | 5.00 | n2 | 8.00 |
| LTE B7 | 8.00 | n5 | 5.00 |
| LTE B12 | 5.00 | n7 | 8.00 |
| LTE B13 | 5.00 | n12 | 5.00 |
| LTE B14 | 5.00 | n25 | 8.00 |
| LTE B17 | 5.00 | n41 | 5.00 |
| LTE B25 | 8.00 | n66 | 5.00 |
| LTE B26 | 5.00 | n71 | 5.00 |
| LTE B30 | -1.02 | n77 | 5.00 |

## Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

## Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

## List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

## This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

## Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

## Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

## Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body

Déclaration d'exposition aux radiations:
Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

## This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

## Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

## IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

## NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

## End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-2020RM502Q”.

## Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-2020RM502Q".

## Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

## Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.