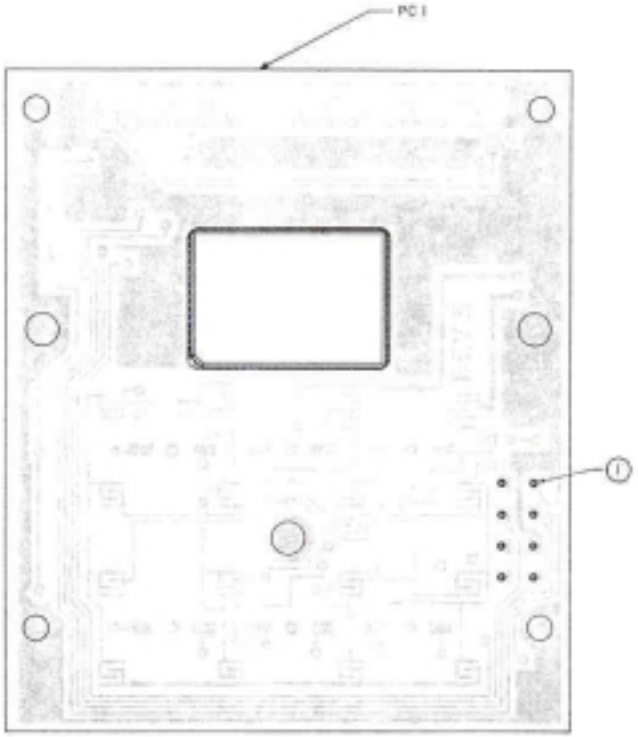
KEYBOARD/DISPLAY BOARD

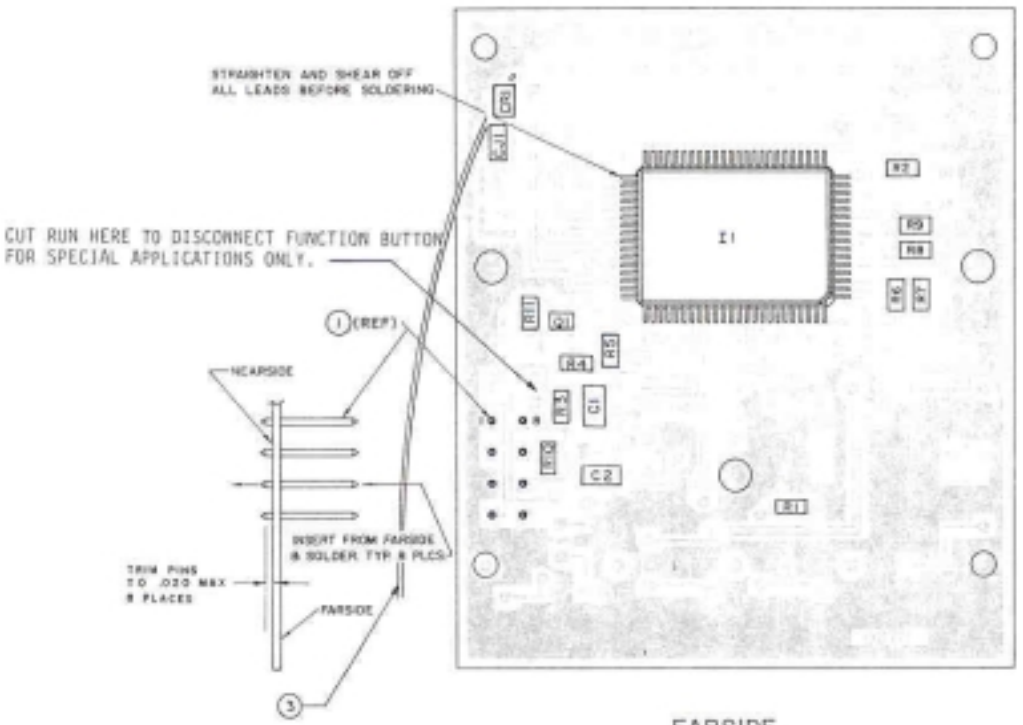
200-05878-0001 STANDARD 7 SEGMENT DISPLAY
200-05878-0059 COMMON BOM

SYMBOL		PART NUMBER	DESCRIPTION	A	UM	QUANTITY 0001	QUANTITY 0059
		200-05878-0059	KYBD/DSPLY BD	A	EA	1.00	.
C	1	186-04104-0047	CH 100KOT/A/50V		EA	.	1.00
C	2	186-04104-0047	CH 100KOT/A/50V		EA	.	1.00
CJ	1	130-03000-0025	RES CHIP 0 EW GJ		EA	1.00	.
I	1	122-05055-0001	LMP/KYBD/DSPL/PROC	A	EA	1.00	.
ITM	1	030-02174-0004	PIN CONTACT		EA	.	8.00
PC	1	009-05878-0211	PCBD KYBD/DSPL		EA	.	1.00
Q	1	087-00503-0000	RSTR NPN MMBT3903	A	EA	.	1.00
R	1	130-05103-0023	RES CH 10K EW 5%		EA	.	1.00
R	2	130-05261-0023	RES CHIP 2K EW 5%	A	EA	.	1.00
R	3	130-05103-0023	RES CH 10K EW 5%		EA	.	1.00
R	4	130-05103-0023	RES CH 10K EW 5%		EA	.	1.00
R	5	130-05104-0023	RES CH 100K EW 5%		EA	.	1.00
R	6	130-05212-0023	RES CHIP 2K EW 5%	A	EA	.	1.00
R	7	130-05202-0023	RES CHIP 2K EW 5%	A	EA	.	1.00
R	8	130-05202-0023	RES CHIP 2K EW 5%	A	EA	.	1.00
R	9	130-05202-0023	RES CHIP 2K EW 5%	A	EA	.	1.00
R	10	130-05161-0023	RES CH 100 EW 5%		EA	.	1.00
R	11	130-05203-0023	RES CHIP 20K EW 5%		EA	.	1.00
REF	1	300-05878-00x0	KYBD/DSPLY BD ASSY	A	RF	.	X
REF	2	002-05878-0010	SCH KYBD DSPL		RF	.	X

FCC ID: K95GPH51

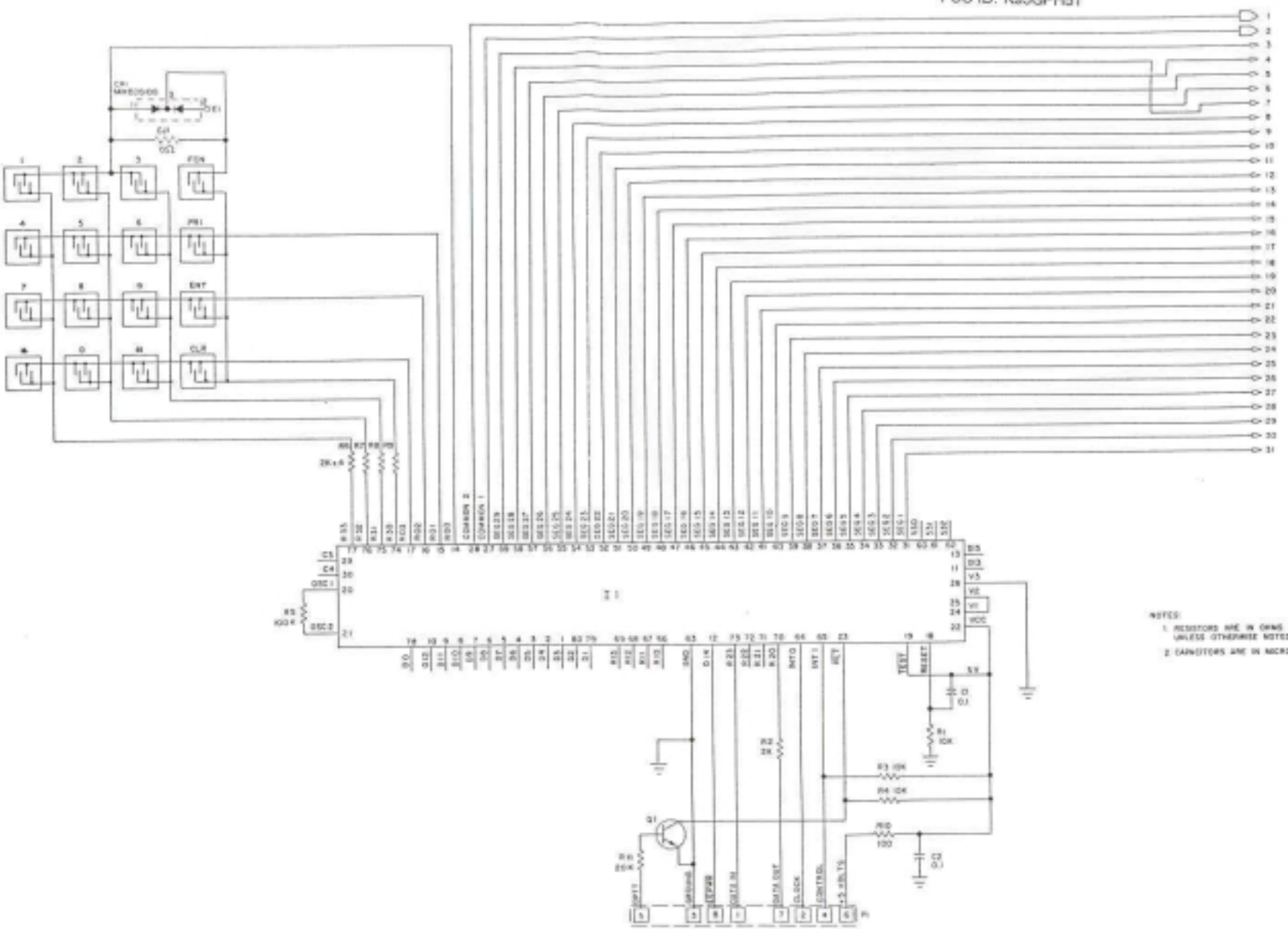


NEARSIDE



FARSIDE

FCC ID: K95GPH51

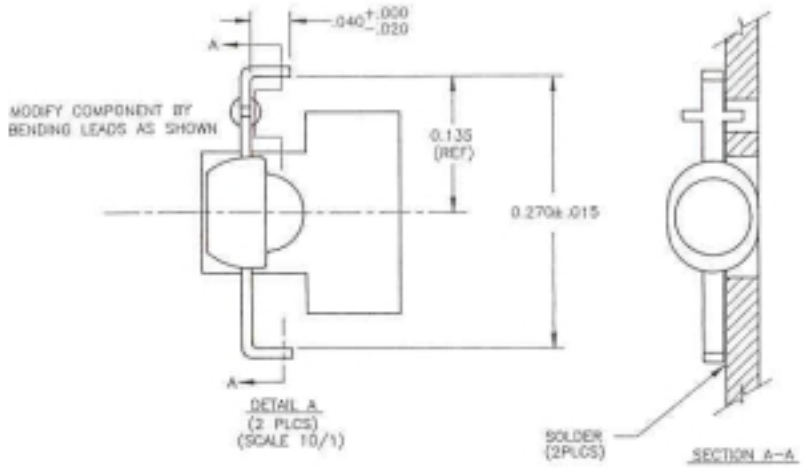


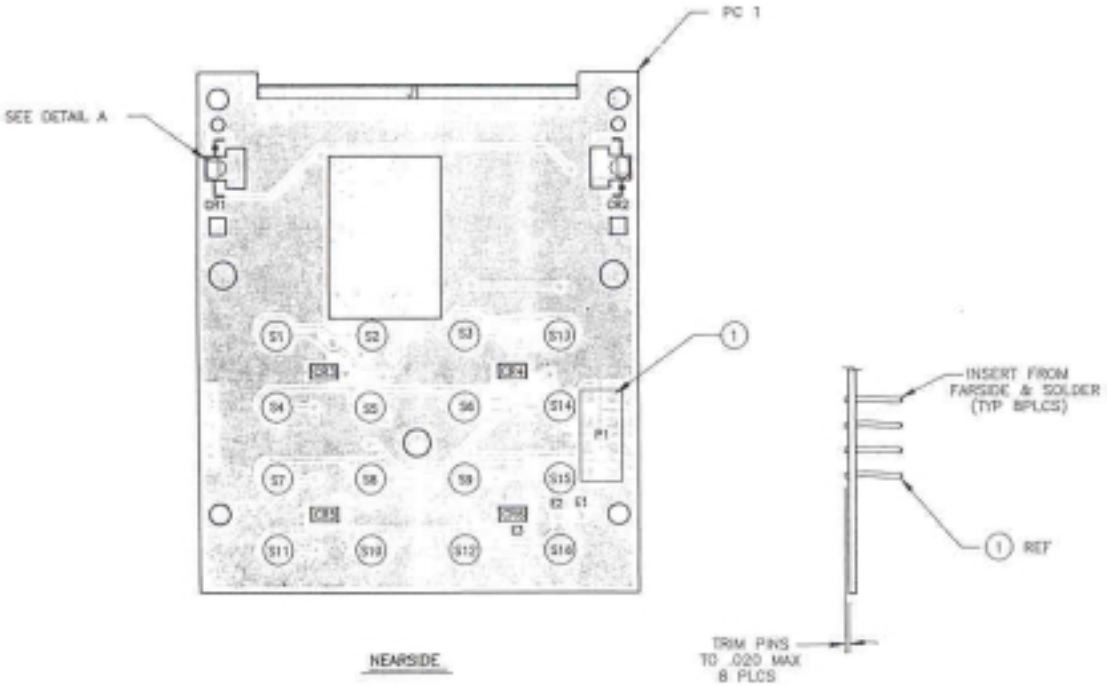
ALPHANUMERIC KEYBOARD/DISPLAY BOARD

200-06924-0000	
200-06924-0001	2 GROUP
200-06924-0002	15GROUP
200-06924-0010	2 GROUP REV1
200-06924-0011	2 GROUP REV1
200-06924-0012	15 GROUP REV1
200-06924-0098	COMMON BOM REV1
200-06924-0099	COMMON BOM

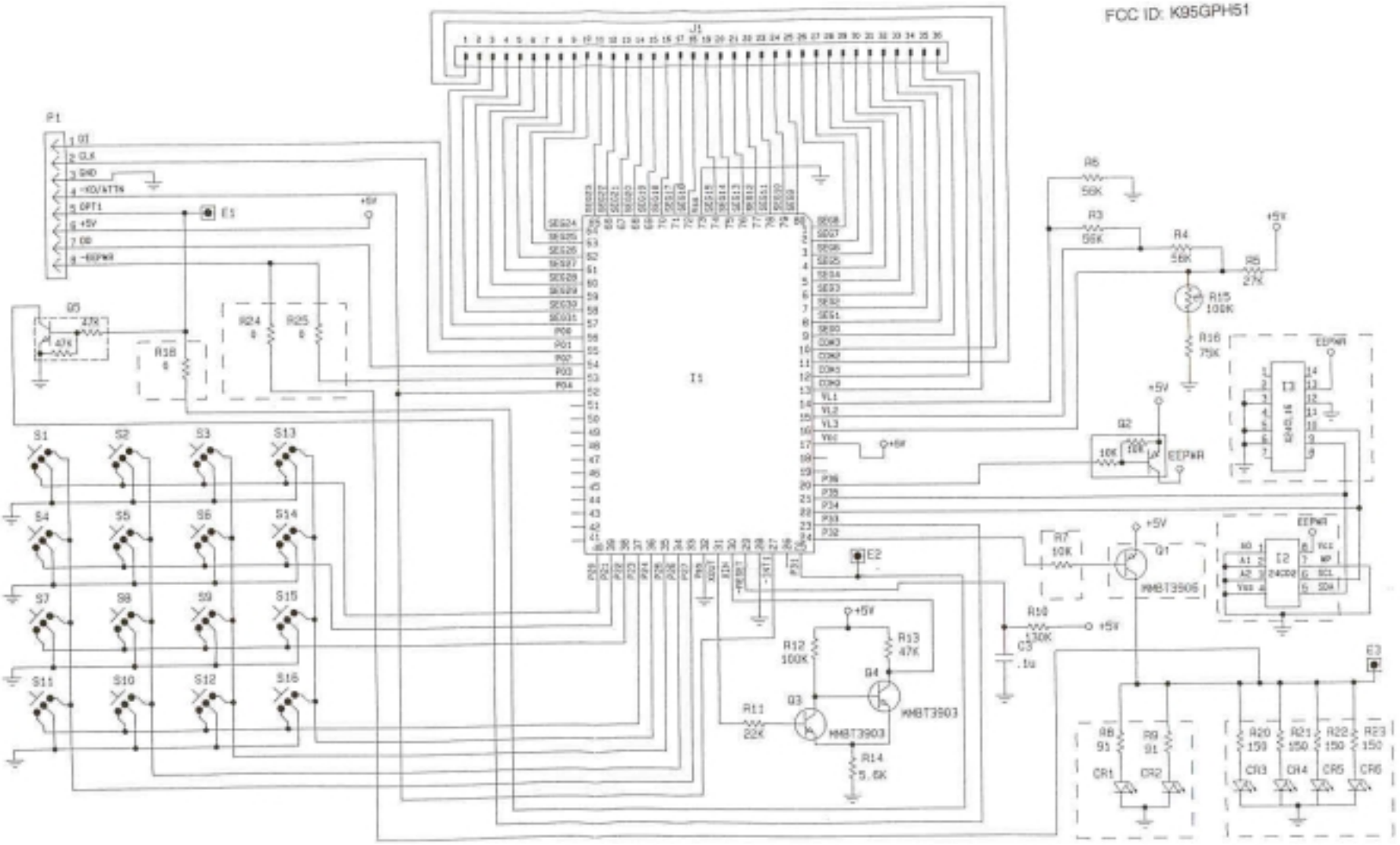
SYMBOL		PART NUMBER	DESCRIPTION	A	UM	QUANTITY							
						0000	0001	0002	0010	0011	0012	0098	0099
		009-06924-0000	PCBD KYBD ALPHA	A	EA								1.00
		009-06924-0010	PCBD KYBD ALPHAREV1	A	EA							1.00	
		200-06924-0098	COMMON BOM REV1	A	EA				1.00	1.00	1.00		
		200-06924-0099	COMMON BOM	A	EA	1.00	1.00	1.00					
C	3	108-04104-0047	CH 100KOOR/50V		EA							1.00	1.00
CR	1	007-06103-0000	LED	A	EA							1.00	1.00
CR	2	007-06103-0000	LED	A	EA							1.00	1.00
I	1	120-05006-0000	ALPHA NUMERIC PROC	A	EA								1.00
I	1	122-05006-0001	ALPHA NUMERIC PROC	A	EA							1.00	
I	2	120-02163-0000	256 X 8 EPROM	A	EA		1.00			1.00			
I	3	120-02741-0000	EEPROM 2K08	A	EA			1.00			1.00		
RM	1	030-02174-0004	PIN CONTACT		EA							8.00	8.00
Q	1	007-00085-0001	XSTR 2N3906 (SOT)		EA								1.00
Q	1	007-08084-0005	TSTR DIGITAL SO	A	EA							1.00	
Q	2	007-08084-0000	XSTR PNP 10K, 10K	A	EA								1.00
Q	2	007-08084-0004	TSTR DIGITAL SO	A	EA							1.00	
Q	3	007-08530-0000	XSTR NPN MMBT3903	A	EA							1.00	1.00
Q	4	007-08530-0000	XSTR NPN MMBT3903	A	EA							1.00	1.00
R	3	130-05563-0023	RES CHIP 56K5%EW		EA							1.00	1.00
R	4	130-05563-0023	RES CHIP 56K5%EW		EA							1.00	1.00
R	5	130-05273-0023	RES CHIP 27K EW 5%		EA							1.00	1.00
R	6	130-05563-0023	RES CHIP 56K5%EW		EA							1.00	1.00
R	7	130-05000-0005	RES CHIP 0 EW CJ		EA							1.00	
R	7	130-05103-0023	RES CH 10K EW 5%		EA								1.00
R	8	130-05201-0023	RES CHIP 200EW5%		EA							1.00	
R	8	130-05910-0023	RES CH 91.0R1%E EW		EA								1.00
R	9	130-05201-0023	RES CHIP 200EW5%		EA							1.00	
R	9	130-05910-0023	RES CH 91.0R1%E EW		EA								1.00
R	10	130-05134-0023	RES CHIP 130KEW5%		EA							1.00	1.00
R	11	130-05164-0023	RES CH 180K EW 5%		EA							1.00	
R	11	130-05223-0023	RES CHIP 22K EW 5%		EA								1.00
R	12	130-05104-0023	RES CH 100K EW 5%		EA							1.00	1.00
R	13	130-05475-0023	RES CHIP 47KEW5%		EA							1.00	1.00
R	14	130-05562-0023	RES CHIP 5.6KEW5%		EA							1.00	1.00
R	15	124-01044-0002	THRMSTR SURFACE MT	A	EA							1.00	1.00
R	16	130-05753-0023	RES CHIP 75KEW 5%		EA							1.00	1.00
R	20	130-05000-0025	RES CHIP 0 EW CJ		EA							1.00	
R	25	130-05000-0025	RES CHIP 0 EW CJ		EA								1.00
R	29	130-05683-0023	RES CHIP 68K EW 5%		EA							1.00	
R	30	130-05683-0023	RES CHIP 68K EW 5%		EA							1.00	
R	31	130-05683-0023	RES CHIP 68K EW 5%		EA							1.00	
REF	1	002-06924-0000	SCH KYBD ALPHA	A	RF								X
REF	1	200-06924-0010	KYBD ALPHA SSYREV1	A	EA							1.00	
REF	2	002-06924-0010	SCH KYBD ALPHREV1	A	EA							1.00	
REF	2	300-06924-0000	KYBD ALPHA ASSY	A	RF								X

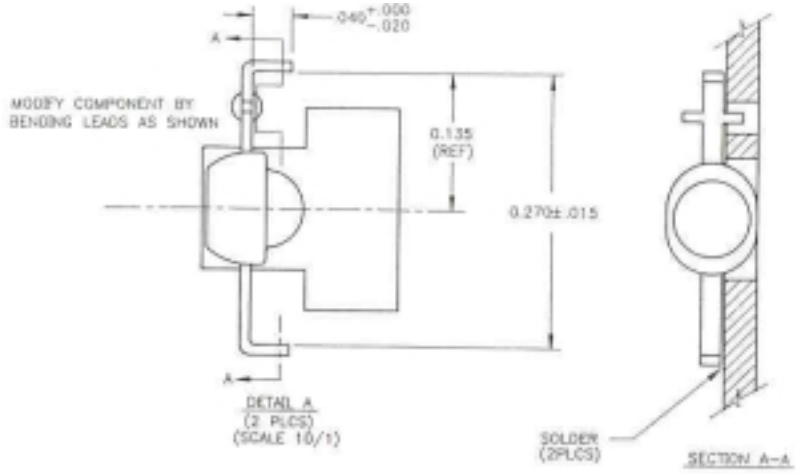
FCC ID: K95GPH51





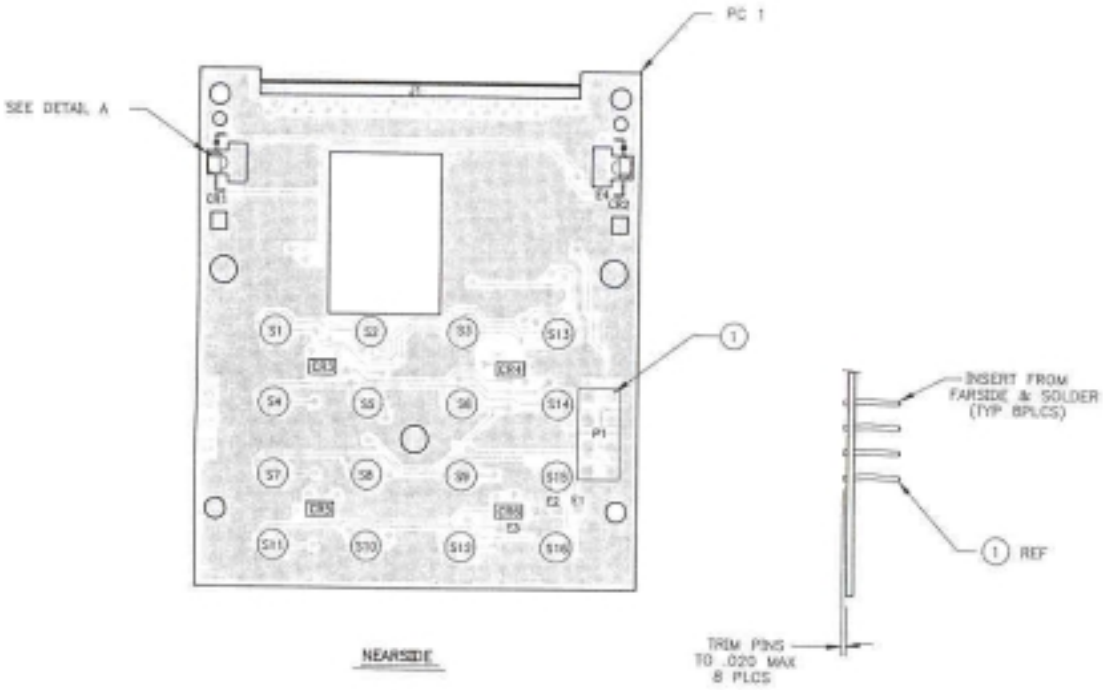
FCC ID: K95GPH51





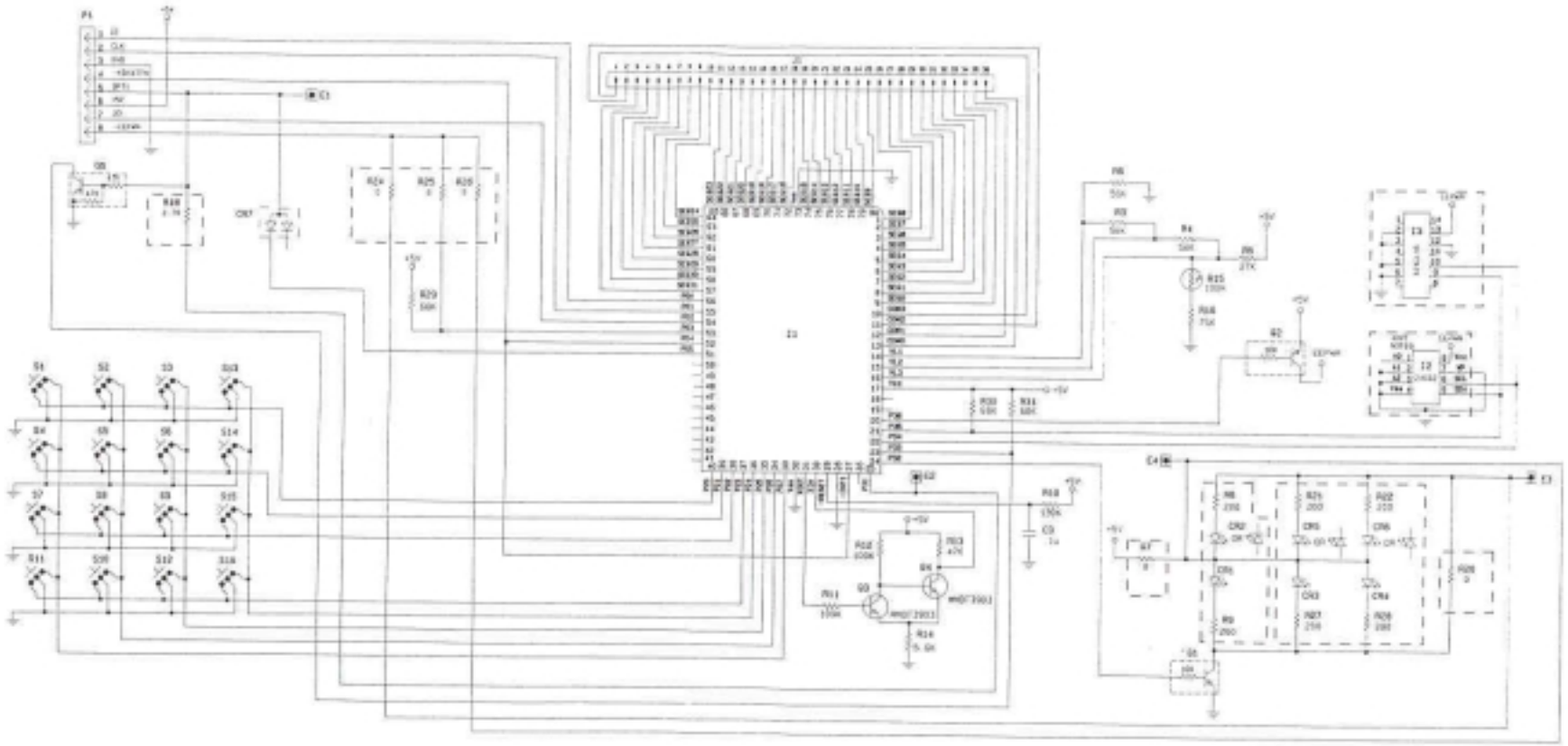
NOTES: UNLESS OTHERWISE SPECIFIED;

1. CR2 IS SHOWN IN IT'S ALTERNATE POLARITY WHICH IS STANDARD FOR RADIOS USING +5V FOR THEIR LIGHTING SUPPLY. (SEE NOTE 5 OF 002-08924-0010).



ALPHA NUMERIC DISPLAY BOARD DRAWING
330-08924-0010

FCC ID: K95GPH51



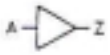
APPENDIX A
INTEGRATED CIRCUIT DATA

INTRODUCTION

This appendix contains descriptions of certain integrated circuits as an aid to understanding the operation of this equipment. Detailed information on IC's containing basic logic elements, op-amps, and other simple circuits are not included in this appendix as their theory of operation is summarized below and the operation of such circuits within this equipment may be readily understood from a review of this summary and the schematic diagrams included in Section VI of this manual.

BASIC LOGIC ELEMENTS

BUFFER



$Z = A$

A	Z
0	0
1	1

INVERTER

$Z = \overline{A}$

A	Z
0	1
1	0

OR GATE

$Z = A+B+C$

A	B	C	Z
0	0	0	0
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

NOR GATE

$Z = \overline{A+B+C}$

A	B	C	Z
0	0	0	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	0

AND GATE

$Z = ABC$

A	B	C	Z
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

NAND GATE

$Z = \overline{ABC}$

A	B	C	Z
0	0	0	1
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	0

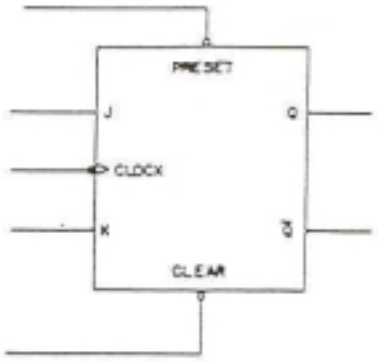
EXCLUSIVE OR GATE

$Z = A \oplus B$

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0

J K FLIP-FLOP

The flip-flop logic element is the basic data storage element of digital logic. It has two outputs that are always at opposite logic levels. That is, when one output is HI the other is LO. The flip-flop will remain in a particular state until that state is changed by an input signal.



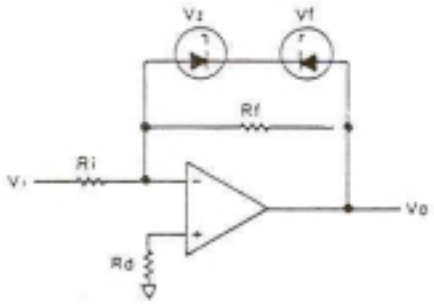
J	K	Q	$\overline{Q}$
L	L	Qo	$\overline{Q}$o
H	L	H	L
L	H	L	H
H	H	Toggle	

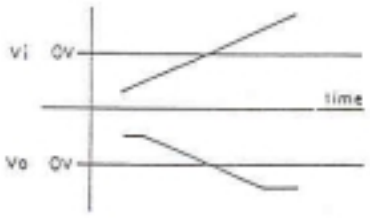
BASIC OP-AMP CIRCUITS

LIMITER

An output voltage may be limited to certain levels by selection appropriate zener diodes and placing them in parallel with the feedback resistor. Voltage limiting can be accomplished in both directions in this manner.

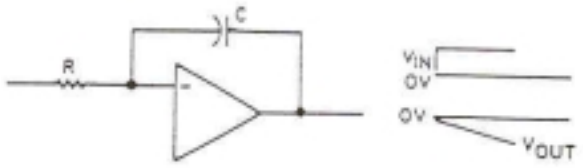
$$Vo\ (max) = Vz + Vf$$





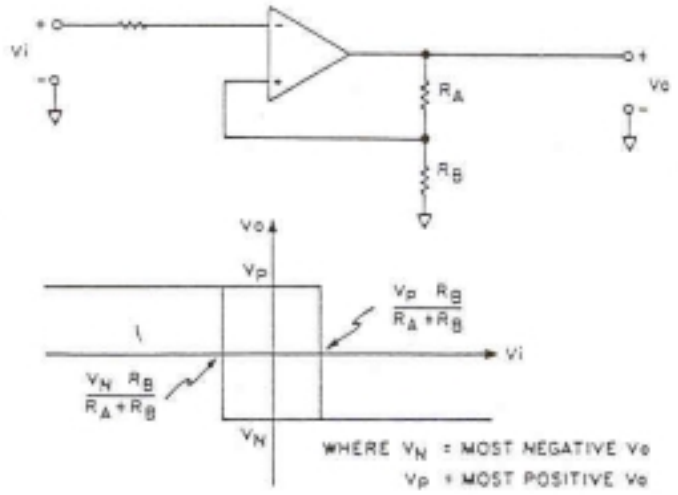
INTEGRATOR

An op-amp in which the only feedback element is a capacitor. The output of an integrator is a ramp, the slope of which is determined by the amplitude of the steady state input and the RC time constant.



ZERO CROSSING DETECTOR

The positive feed back path causes the output voltage to drive to the saturation potential of opposite polarity as the input voltage. Ideally, the output switches from one saturation level to the opposite saturation level as the input voltage passes through zero. Noise immunity demands the addition of R_B which requires that the input reach a certain magnitude after passing zero before the output will switch.

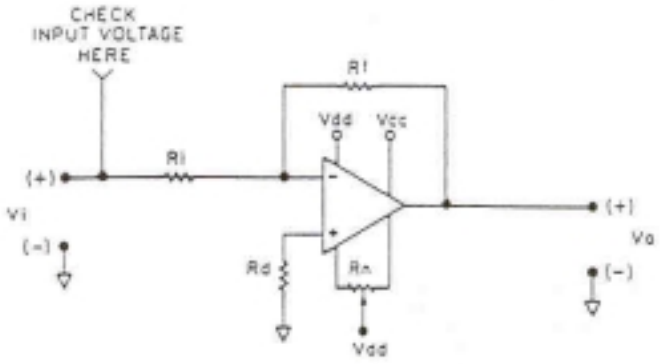


INVERTING OP-AMP AMPLIFIER

A voltage applied at the inverting (-) input will cause an output voltage [Vo] of opposite polarity as the applied voltage. The relationship of the input and output voltages is shown in the following equations:

$$Vo = (Rf/Ri)\ Vi \qquad GAIN = -(Rf/Ri)$$

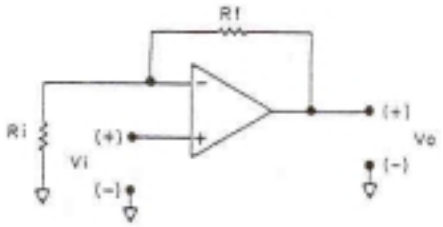
From the above equation, a zero input voltage should give a zero output if Rn has been adjusted to the null of the amplifier.



NON-INVERTING OP-AMP AMPLIFIER

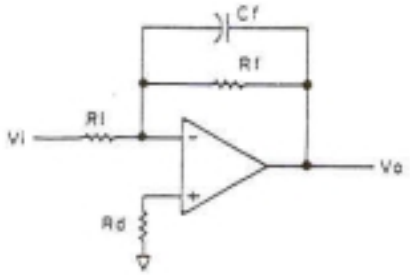
A voltage applied at the non-inverting (+) input will cause an output voltage [Vo] of the same polarity as the applied voltage. The relationship of the input and output voltages is shown in the following equations:

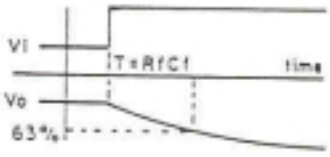
$$Vo = [1 + (Rf/Ri)]\ Vi \qquad GAIN = 1 + [Rf/Ri)$$



LOW PASS FILTER

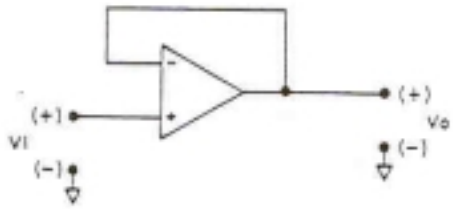
The low pass filter is a variation of an inverting op-amp circuit. The addition of capacitor Cf to the feedback network around the amplifier provides low pass filtering to the input voltage. The expression T = RfCf gives the time required for Vo to reach 63% of the final value.





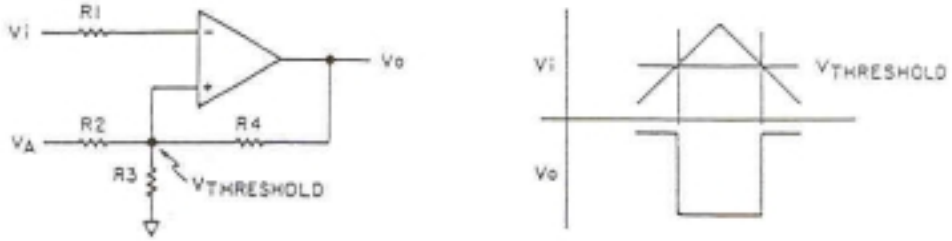
VOLTAGE FOLLOWER AMPLIFIER

This configuration is a special case of the non-inverting amplifier previously discussed, with Rf equal to zero. Therefore the relationship of the input and output voltage reduces to Vo = Vi, or unity gain. It is used to provide high input impedance and buffering action.



THRESHOLD DETECTOR

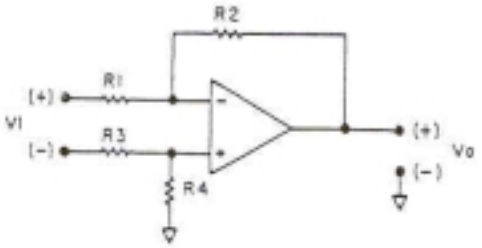
Treshold detectors use positive feedback to toggle the op-amp output when the input voltage (Vi) is above or below a voltage level (V threshold) set by R2 and R3. R4 provides the positive feedback required for a clean switch from one saturation level to another. The voltage polarity (V_A) determines the initial output state of the amplifier and the polarity of the threshold being detected.



DIFFERENTIAL AMPLIFIER

The principal use of the differential amplifier is to translate signals, from sources referenced to some level other than signal ground, to signals referenced to signal ground. The relationship of the input and output voltages is shown in the following equations:

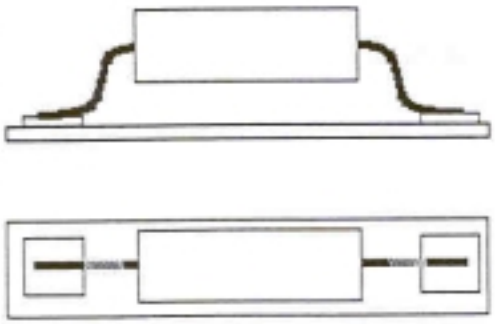
$Vo = -(Rf/RI)\ Vi$, if $R1 = R3$ and $R2 = R4$ $\qquad$ $GAIN = -(Rf/RI)$



SURFACE MOUNT COMPONENTS

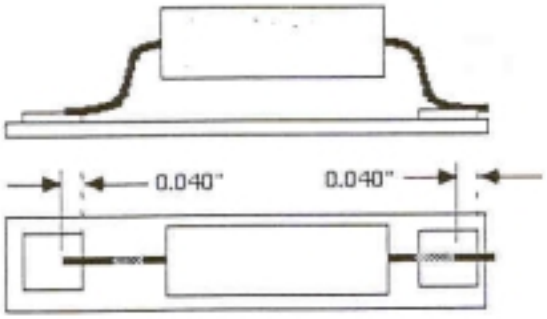
Round leaded and flat leaded components can be mounted on the surface of a board rather than through plated holes on a board.

The illustrations below demonstrate acceptable mounting practices for round leaded components on surface mount boards.



PREFERRED

Lead is centered on the pad. At least 0.040" (the thickness of a dime) is in contact with the pad. The lead does not overhang the pad.

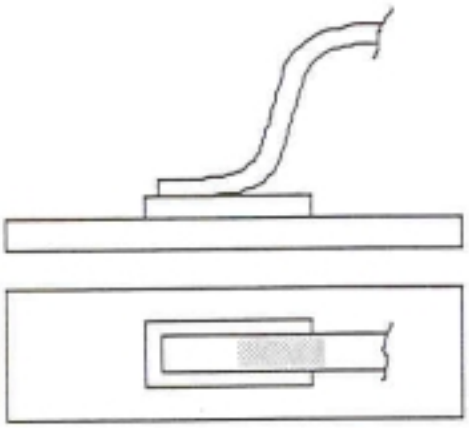


ACCEPTABLE MINIMUM

The lead has a minimum of contact area and has a slight overhang. The lead is not centered on the pad. The lead is at the edge of the pad. The contact area is not less than 0.040".

SURFACE MOUNT COMPONENTS (CON'T)

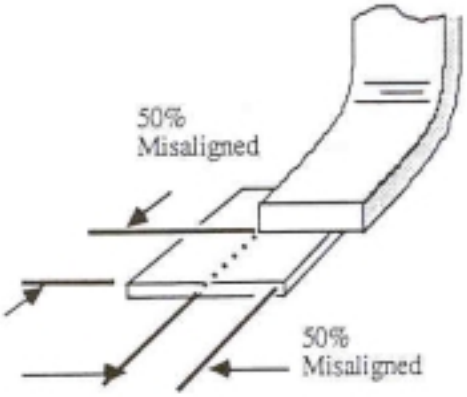
The illustrations below show acceptable ways of mounting flat leaded components.



PREFERRED

Lead is centered within the confines of the pad.

Heel rises before leaving pad area.

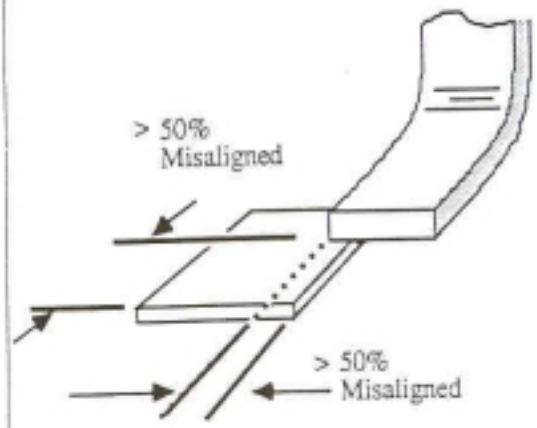


MINIMUM ACCEPTABLE

Lead misalignment is not more than 50%.

SURFACE MOUNT COMPONENTS (CON'T)

The illustration below shows an unacceptable way of mounting a flat leaded component.



UNACCEPTABLE - REWORK

Lead is misaligned with the side of the pad or the length of the pad by more than 50%.

SURFACE MOUNT COMPONENTS (CON'T)

The following illustrations show acceptable solder height, amount of fillet, conductor spacing, and amount of allowable chip float.

The illustrations below show acceptable fillet heights.

TOP VIEW

SIDE VIEW

PREFERRED

Solder fillet height is 30% of the end height.

There is complete wetting of the pad and device end termination.

When the chips are wave soldered, it is permissible for the solder to come to the top or even over the cap of the end termination.

TOP VIEW

SIDE VIEW

ACCEPTABLE

Solder fillet height is to the top of the end termination.

There is good wetting.

TOP VIEW

SIDE VIEW

MINIMUM ACCEPTABLE

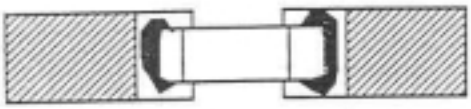
The fillet height is 10% of the end termination.

There is incomplete wetting of the pad and termination.

SURFACE MOUNT COMPONENTS (CON'T)

The illustrations below show acceptable amounts of solder applied to surface mount chips.

PREFERRED

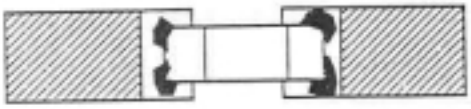


The solder fillet is continuous around the perimeter of the chip termination.

There is good wetting of the land and termination.

Fillet height is approximately 30% of the termination height.

MINIMUM ACCEPTABLE

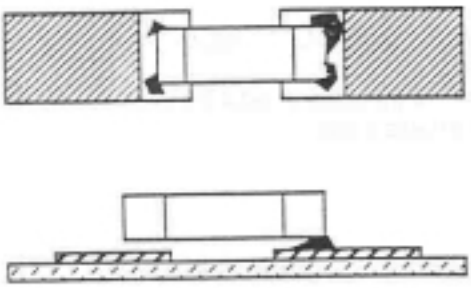


There is 50% solder coverage of the perimeter of the chip.

The fillet height is at least 10% of the termination height.

The illustration below shows a chip component that should be reworked because of insufficient solder. There is less than 50% solder coverage around the perimeter and bottom of the chip.

UNACCEPTABLE - REWORK



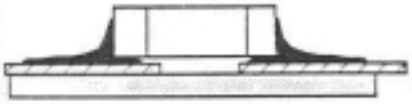
There is less than 50% solder coverage on the perimeter of the chip.

There is less than 50% solder coverage on the bottom of the chip.

The solder fillet is insufficient.

SURFACE MOUNT COMPONENTS (CON'T)

The two illustrations below show acceptable conductor spacing after solder flow. The spacing is not less than 50% of the original width or less than 0.005".



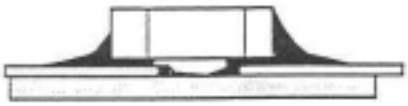
PREFERRED

The solder holds the chip to the pads and normal conductor spacings are maintained.

MINIMUM ACCEPTABLE

The spacing between the pads is reduced to 50% of the original spacing.

The illustration below shows an unacceptable chip component, where the spacing between pads is reduced by more than 50% because of excess solder. This component must be reworked.

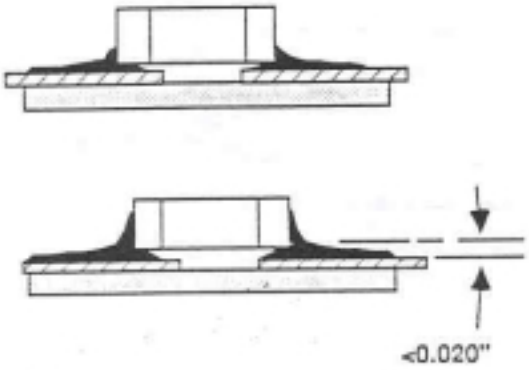


REWORK - UNACCEPTABLE

The spacing between the pads is reduced by more than 50% because of excess solder.

SURFACE MOUNT COMPONENTS (CON'T)

The illustrations below show acceptable components that have not floated higher than 0.020" above their pads.



PREFERRED

The solder height is minimal.
The fillet is concave.
There is good wetting.
The chip is raised less than 0.020".

ACCEPTABLE

The solder has floated the chip off its adhesive (if used) but the amount of float is not greater than 0.020".