Eclipse Series

RF Technology

November, 2001

T50 Transmitter
Operation and Maintenance Manual

Contents

> ## WARNING
>
> Changes or modifications not expressly approved by
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1   Operating Instructions

1.1   Front Panel Controls and Indicators

1.1.1   PTT

A front-panel push-to-talk (PTT) button is provided to facilitate bench and field tests
and adjustments. The button is a momentary action type. When keyed, audio from the
line input is disabled so that a carrier with subtone is transmitted. The front-panel
microphone input is not enabled in this mode, but it is enabled when the PTT line on
that socket is pulled to ground.

The PTT button has another function when transmission is keyed up, and the TX LED
light is showing. If there is a "forward power low" alarm (the ALARM LED flashes
three times, then pauses), pressing this will cause the ALARM LED to flash 6, 7, 8, or 9
times before the pause (see Table 2). This will indicate what has caused the low power
alarm.

1.1.2   Line

The LINE trimpot is accessible by means of a small screwdriver from the front panel of
the module.   It is used to set the correct sensitivity of either line input or the direct
audio input. It is factory preset to give 60% of rated deviation with an input of 0dBm
(1mW on 600Ω equivalent to 775mV RMS or about 2.2V peak-to-peak) at 1kHz. The
nominal 60% deviation level may be adjusted by measuring between pins 6 and 1 on the
test socket, and adjusting the pot. By this means an input sensitivity from approximately
-12dBm to +12dBm may be established.

An internal, software selectable, option, provides an extra gain step of 20dB. This,
effectively changes the input sensitivity to –32 to –8dBm.

LED Flash Cadence	Fault Condition
9 flashes, pause	External PA failure
8 flashes, pause	Low dc supply on External PA
7 flashes, pause	External PA Over Current Condition
6 flashes, pause	External PA Over Temperature
5 flashes, pause	Synthesizer unlocked
3 flashes, pause	Unable to communicate with External PA
2 flashes, pause	The current channel is not programmed or the frequency is out of range.
1 flash, pause	Low dc supply voltage
LED ON continuously	Transmitter timed out

Table 1: Interpretations of LED flash cadence (TX LED Off)

LED Flash Cadence	Fault Condition
9 flashes, pause	External PA failure (if PTT is pressed)
8 flashes, pause	Low dc supply on External PA (if PTT is pressed)
7 flashes, pause	External PA Over Current Condition(if PTT is pressed)
6 flashes, pause	External PA Over Temperature(if PTT is pressed)
4 flashes, pause	Either PLL is near operational limit
3 flashes, pause	Forward Power Out of Range(if PTT is not pressed)
2 flashes, pause	Reverse Power ratio exceeded.
1 flash, pause	Low dc supply voltage
LED ON continuously	Transmitter timed out

Table 2: Interpretations of LED flash cadence (TX LED On)

1.1.3   POWER LED

The PWR LED shows that the dc supply is connected to the receiver and that the microprocessor is not being held in a RESET state.

1.1.4   TX LED

The TX LED illuminates when the transmitter is keyed.   It will not illuminate (and an ALARM cadence will be shown) if the synthesizer becomes unlocked, or the output amplifier supply is interrupted by the microprocessor.

1.1.5   ALARM LED

The Alarm LED can indicate several fault conditions if they are detected by the self test program.   The alarm indicator shows the highest priority fault present.   See Tables 1 and 2.

2   Transmitter Options

There are NO internal jumpers in the T50.

There are many software selectable options. Some options are selected on a per channel basis, and some are defined globally (i.e. the parameter is fixed irrespective of which channel is selected). Below is a description of these global parameters

2.1   Serial I/O Parameters

There are two serial ports. There is the main serial port which is brought out to the front panel connector. This is referred to as PORT0. There is another serial port which is for factory use only. It is referred to as PORT1.

The baud rate, parity, and whether hardware flow control is enabled can be defined for PORT0. PORT0 is set by default to 57.6Kbps, with No parity, and No Hardware Flow Control.

2.2   LINE Terminators

There are two main audio inputs, plus a direct audio (TONE) input. The direct audio input is a High Impedance Balanced DC input, but the two audio inputs are AC coupled (> 10Hz) inputs which can be High Impedance(HiZ), or 600 ohm inputs. Each input can be software selected to be HiZ, or 600 ohms.

2.3   Exciter Low Battery Level

This is factory set to 24.0V, and defines the level of the DC supply that will cause an Exciter dc supply low alarm.

2.4   External PA Parameters

There are several user definable parameters associated with the external PA provided with each exciter.

These are the PA low battery alarm level (default is 26V), the PA Set Forward Power Level (defaults to 100W), the Forward Power Low Alarm Level (defaults to 90%), and the Reverse Power Alarm Level (defaults to 25% - corresponding to a VSWR of 3:1).

2.5   LOOP Volts Select

Normally the transmitter will key up if dc current is sensed flowing in either direction between Line1+ and Line1- (>=1mA). If this option is selected, then a 12Vdc supply is

applied to the pair through 660 ohms of source impedance. (It would be expected, normally, that if this option is selected, then the option to remove the 600 terminator from Line1, would also be selected). If dc current flows from having applied this potential, then the transmitter will key up.

2.6   Direct Audio (TONE) Select

Normally any signal applied to the TONE+/TONE- pair is ignored. If this option is selected then a Direct Audio input will be mixed with any audio received on either of the other two lines.

2.7   Direct Audio (TONE) High Pass Filter Select

Normally the Direct Audio, and the CTCSS outputs are passed through a 250Hz, low pass filter. This filter can be bypassed by selecting this option.

2.8   Transmit Time

This parameter defines a maximum time limit for continuous transmission. It is expressed in seconds and can be arbitrarily large (months in fact). If it is set to zero seconds, then the transmitter can stay keyed up permanently.

2.9   Channel Selectable Parameters

Each channel defines two complete set of parameters. One set of parameters is used when a transmitter keys up from the PTT-in input, and the other set is used when the transmitter keys up from the LOOP-in, the PTT switch, or the microphone PTT input.

Each set defines what frequency to use, what CTCSS sub-tone (if any) to use, what maximum line deviation to use, what tone deviation to use, what transmit delay (a delay applied from PTT-in or LOOP-in to transmission), what transmit tail (delay from PTT-in, or LOOP-in, to transmission being stopped, and No-TONE period (a period of extra transmission in which No Tone is applied after PTT-in or LOOP-in has been released.

As well as these parameters, which Line (or Lines) can be selected, and whether the Lines should have Flat frequency response or have Pre-emphasis applied. Also, it can Enable or disable the extra 20dB gain pad.

Note that both Line1 and Line 2 can be selected (each with or without pre-emphasis), and if so, then the two signals will be mixed, and the Line potentiometer will adjust the level of them both.

3   Transmitter I/O Connections

3.1   25 Pin Connector

The female D-shell, 25 pin, connector is the main interface to the transmitter. The pin connections are described in table 3.

Function	Signal	Pins	Specification
dc power	+28Vdc(in)	13, 25	+24 to 32 Vdc
	0 Vdc	1, 14	Common Voltage
	+5Vdc(out)	17	Output for external Logic(100mA)
	+12Vdc(out)	15	Output for an external relay(120mA)
Serial Communications	SCLK	12	Serial Clock
	MOSI	6	Bi-directional Data Pin
	CH_EN	18	Enables Channel Select Shift Register
	PA_CS	24	Enables PA A/D chip
	SPARE_SEL	5	Spare Select (for future use)
600Ω/HiZ Line	Line1+	8	Transformer Isolated Balanced 0dBm
	Line1-	19	Input
600Ω/HiZ Line	Line2+	10	Transformer Isolated Balanced 0dBm
	Line2-	22	Input
Direct PTT input		11	Ground to key PTT
T/R Relay driver output		23	Open collector, 250mA /12V
Sub-Audible Tone Input	Tone+	9	>10kΩ, dc coupled
	Tone-	21	

Table 3: Pin connections and explanations for the main 25-pin, D connector.

3.2   9 Pin Front Panel Connector

The female D-shell, 9 pin, front panel connector is an RS232 interface for serial communications to a terminal, a terminal emulator, or to a computer. The pin connections are described in table 4.

Function	Pins	Specification	Pin name on IBM PC
TXD	2	Transmit Data (Output)	RxD
RXD	3	Receive Data (Input)	TxD
RTS	8	Request To Send (Output)	CTS
CTS	7	Clear To Send (Input)	RTS
DTR	6	Data Terminal Ready(Output)	DSR
DSR	1	Data Set Ready (Input)	DCD
GND	5	GND	GND

Table 4: Pin connections for the front panel 9 pin D connector.

The pinout for the connector has been chosen so that a straight-through BD9 male to DB9 female cable can connect the transmitter to any male DB9 serial port on an IBM PC compatible computer.

Note that for connection to a modem, a cross-over cable will be required.

4   Channel Programming and Option Selection

Channel and tone frequency programming is most easily accomplished with RF Technology Eclipse50 software. This software can be run on an IBM compatible PC and can be used to calibrate a T50, R50, and PA50 as well as program channel information. See the Eclipse 50 users manual for further information.

But the T50 also has its own stand-alone high level interface, which can be accessed from a VT100 compatible terminal, or terminal emulator (such as HyperTerm which is available as a standard accessory with Windows).

The pertinent aspects of this High Level Interface are described below.

4.1   Setting Options

Note that any text in italics, represents data output by the T50 firmware, rather than command line data sent to the T50 firmware.

The T50, after powering up, will issue a command prompt of the form:

> *T50>*

Via a terminal, or a terminal emulator, a user can type various commands in. The basic command to read parameters is:

> *T50>* read par parameter_name

Where "parameter_name" is one of the following:

Parameter Name	Parameter Function	Default Value	Parameter Range
LOOP_GEN	Generate a LOOP potential (see 2.5)	Off	Text: Off or On
PA_SET_FWD_PWR	Output Power of the PA (see 2.4)	100.0 (Watts)	Floating point number 20.0 – 150.0
PA_LOW_BAT	Low Battery Alarm Level (see 2.4)	26.0 (Volts)	Floating Point Number < 32.0
REV_PWR_ALARM	Sets the maximum level of reverse power. At this level of reverse power, forward power is automatically decreased so that this reverse power level is never exceeded. It also sets the ratio of forward power, which if exceeded causes the reverse power alarm condition to be asserted	25.0 (% of PA_SET_FWD_PWR) 25.0 (% of current forward power)	Floating Point Number 0.0 – 99.9

Parameter Name	Parameter Function	Default Value	Parameter Range
LOW_PWR_ALARM	Level of Output Power when the low power alarm condition occurs (see 2.4)	90.0 (% of PA_SET_FWD_PWR)	Floating Point Number 0.0 – 99.9
TRANSMIT_TIME	Maximum Time that the transmitter can stay keyed up	0 (Seconds: Note that zero seconds implies no transmit time limit)	Decimal number: 0 - 9999999
BAUD_RATE0	Port 0 Baud Rate	57600 (BPS)	Decimal number: 300 - 115200
PARITY0	Port 0 Parity	None	Text: None, Even, or Odd
FLOW_CONTROL	Port 0 Flow Control	Off ("On" not yet available)	Text: Off

Table 5: Some User Defined Parameters.

Note that the parameter names have been shown in upper case, but they can be typed in upper or lower case.

A parameter can be changed, or added, by typing

> *T50>* set par parameter_name=parameter_value

As for parameter names, the parameter value can be Upper or Lower case if it is a text value, as against a numeric value.

4.2   Setting Channel Parameters

One can read the data from an existing channel by entering the command:

> *T50>* read chan chan_number

Where chan_number is a number from 0 to 99.

Entering new channel values, or modifying existing ones is possible from the command line interface, but it is not recommended.   It can be done by typing the following at a command prompt:

> *T50>* set chan chan_number parameter_list

Where chan_number is a number from 0 to 99.

The format of the parameter_list is quite complex. It has 14 fields. Each field can be separated by a colon(:), comma(,), space, or tab.

For example set chan 0 25.0,35.0,100.0,120.0,0,5,2,0,5,2,10,11,0,3

Field1: Transmit Frequency (in MHz) if PTT-in is asserted. This is 25.0 MHz in the example.

Field2: Transmit Frequency (in MHz) if the exciter is keyed up by anything but PTT-in being asserted. This is 35.0 MHz in the example.

Field3: CTCSS Tone (in Hz) if PTT-in is asserted. This is 100Hz in the example.

Field4: CTCSS Tone (in Hz) if the exciter is keyed up by anything but PTT-in being asserted. This is 120Hz in the example.

Fields 5,6,7: These define the start-up delay (in hundredths of a second), the transmit tail (in seconds), and the no tone period (in tenths of a second) if the exciter keys up from PTT-in being asserted.

Fields 8,9,10: These define the start-up delay (in hundredths of a second), the transmit tail (in seconds), and the no tone period (in tenths of a second), if the exciter keys up from anything other than PTT-in being asserted.

Field 11: Selects the line parameter if PTT-in being asserted caused the exciter to key up. In the example it has disabled the 20dB gain pad, and enabled pre-emphasis on Line 2 (Line 1 is disabled).

Field 12: Selects the line parameter if anything other than PTT-in being asserted caused the exciter to key up. In the example it has disabled the 20dB gain pad, and it would enable pre-emphasis on Line 1 and Line2 (i.e. audio on each input is mixed).

Field 13: Selects the Tone deviation and the Maximum Line deviation if the exciter keys up from PTT-in being asserted In the example, it has selected the default maximum line deviation (5kHz), and the default tone deviation of 750Hz. (See Tables 7 and 8)

Field 14: Selects the Tone deviation and the Maximum Line deviation if the exciter keys up from anything other than PTT-in being asserted. In the example, it has selected a maximum deviation of 2.5kHz, and a maximum tone deviation of 375Hz. (See Tables 7 and 8)

Least Significant BCD digit of Fields 13 or 14	Maximum Deviation
0	5.0kHz
1	4.0kHz
2	3.0kHz
3	2.5kHz
4	2.0kHz
5	1.5kHz
6	User Specified(default: 4.5kHz)

Table 7: Maximum Deviations

Most Significant BCD digit of Fields 13 or 14	Nominal Tone Deviation
0	750Hz
1	500Hz
2	375Hz
3	250Hz
4	150Hz
5	User Specified (default: 600Hz)

Table 8: Maximum Tone Deviations (when Max Dev is 5kHz)

Note that the actual maximum tone deviations depend on the maximum deviations. If a maximum deviation of 4kHz was chosen, and a nominal tone deviation of 250 Hz, the actual maximum tone deviation would be $250*4.0/5.0 = 200Hz$.

If the Eclipse50 Software is not used to program the exciter, it is recommended that the programming information is prepared using a spreadsheet and/or a text editor, and the resulting file is then downloaded, as a text file, to the firmware using, for example, HyperTerm.

Note that if using HyperTerm to download the text file, at 57600 bits per second or higher speeds, the connection properties may need to be changed to add a 10 millisecond delay after each line of text is sent.

5   Circuit Description

The following descriptions should be read as an aid to understanding the block and schematic diagrams given in the appendix of this manual.

There are 9 sheets in the schematic in all.

5.1   T50 Master Schematic (Sheet 1)

Sheet 1, referred to as the "T50 Master Schematic", is a top level sheet, showing five circuit blocks, and their interconnection with each other, as well as the interconnection with all connectors and external switches.

JP12 is the connector, on the printed circuit board, for the microphone input.

P3 represents the rear female DB25 connector.

J1 is the nominal 1W RF output (BNC) connector, which is used to connect to the External Power Amplifier.

J4 is an optional BNC connector for an external reference clock. If an external reference clock, with power level from +5 to +26dBm is attached here, the firmware will automatically track the channel VCO to the reference.

Note that the external reference frequency is limited to:

> 500kHz, or any multiple
> any multiple of 128KHz greater than or equal to 4
> any multiple of 160KHz greater than or equal to 3

P1 is the front panel DB9 RS-232 connector for attachment to a terminal, a terminal emulator, or to an IBM PC running the Eclipse50 software.

JP2 is for the attachment of an LCD display module. This has been included for later development.

JP3 is a specialised connector for test and factory configuration use only.

RV100 represents the front panel LINE potentiometer.

SW1 represents the PTT test pin.

D102, D103, and D104 represent the three front panel LEDs.

5.2   Microprocessor (Sheet 2)

Sheet 2 describes the basic microprocessor circuitry.

The core CPU is the Motorola XC68HC12A0. It is configured in 8 bit data width mode.

The CPU is clocked by a 14.7456MHz crystal oscillator circuit (top left) comprising the JFET Q202, and two switching transistors Q203 and Q204.

The CPU contains an 8 channel A/D converter whose inputs are identified as AN0, AN1, …, AN7.

AN7 and AN6 are used as LOCK detect inputs from the two Phase Locked Loop (PLL) circuits (see 5.6)

AN5 is used to sense whether or not the dc supply is within spec or not.

AN4 is multiplexed between the LINE control potentiometer and the Channel reference crystal's temperature sense. Which analogue input drives this analogue input, is defined by the state of TEMP_LEVEL_IN which is a CPU output signal.

AN3 and AN1 are inputs from the PLL circuits that sense the bias voltage on the VCO control varactor for each VCO.

AN2 is used to sense the average peak voltage of the audio input.

AN0 is used to sense the average peak voltage of the RF output.

FRDY is an output from the flash. It goes low when the Flash starts to write a byte of data, or erase a block, or erase the whole chip, and it returns to its default high state when the action requested has completed.

FPSW1 is the switch input from the PTT Test pin.

FPSW2, and FPSW3 are two pins that have been reserved for future use as switch inputs.

LOOP/VOLTS_SEL is a CPU output that when high applies 12V of dc feed to the audio output.

TONE_DEV_U/D and TONE_DEV_INC are CPU outputs that are used to control the digital potentiometer that sets the TONE deviation level. (see 5.5)

EXT_TONE_SEL is a CPU output that when low enables differential analogue input from the TONE+/TONE- pair. (see 5.5)

LINEINP_ADSEL is a serial bus select pin. It selects the quad Digital to Analogue converter (DAC) that sets the levels for the two Line input Voltage Controlled Amplifiers, the output RF power amplifier bias voltage, and the LCD bias circuit. (see 5.4)

LINEINP_DSEL is also a serial bus select pin. It is used to select the shift register that is used to control most of the analogue switches in the audio Line input circuitry, as well as the digital POT used to set the maximum deviation level. (See 5.4)

PWR_CNTRL_HIGH is a CPU output that can be low, tri-state, or high. This adjusts, slightly, the range of the power amplifier bias circuitry allowing finer control of the output power level. (see 5.4 and 5.8)

CTCSS_SEL is a serial bus select pin. It is used to select the FX805 chip(U500), which is used to generate CTCSS tones. (see 5.5)

CHAN_PLL_SEL is a serial bus select pin. It is used to select the PLL chip in the Channel PLL circuit (U604). (See 5.6)

SIGGEN_ADSEL is a serial bus select pin. It is used to select the quad DAC in the RF area. This DAC controls the reference oscillator bias voltages, and the BALANCE voltage controlled amplifier. (See 5.6)

CHAN_VCO_EN is a CPU output that enables (when high) the Channel VCO. (See 5.6 and 5.7)

EXT_REF_DIV is a CPU timer input. It is the output of the external reference clock divided by 3200. The software can measure what the reference frequency is, and then use this input to calculate the frequency error of the channel PLL reference oscillator. It can then adjust the channel reference oscillator to reduce this error to less than 0.3ppm. (See 5.6)

SPARE_SEL is a serial bus select. It has been reserved for future use, and has been brought out to the rear DB25 connector. (see 5.1)

CH_EN is a serial bus select. It is brought out to the rear panel and is used to interface to the channel encoder on the rear daughter-board. (See 5.1)

Any GPS pulses are isolated from the on-board electronics by the opto-isolator U212. The output of that opto-isolator is then connected to the GPS timer input of the CPU. The software assumes that any GPS pulses are 1 second apart and can use this input to measure the frequency error of the channel PLL reference oscillator. . It can then adjust the channel reference oscillator to reduce this error to less than 0.3ppm. (See 5.1)

TERM_EN2 and TERM_EN1 are used to enable (when low) 600 ohm termination of Line2, and Line1 respectively. (See 5.3)

Fo_MOD_2, and Fo_CHAN_2 are the Fo outputs from the Modulation PLL and the Channel PLL divided by two. They should be 200Hz square waves, except for brief periods when frequencies are being changed. (See 5.6)

LCD_DB7 is an input used to sense if the LCD display module is busy processing the last command sent to it.

ECLK is a pin that at start-up only, should have the CPU system clock of 7.3728MHz on it.

TX_LED, ALARM_LED, are CPU outputs that drive (when low) the TX LED, and the ALARM LED on.

T/R_RELAY_H, when high, drives the T/R RELAY output low, and also enables the RF power amplifier. The T/R RELAY output can activate at least one conventional 12V relay. (See 5.1)

SCLK, and MOSI are used as the core of a serial bus. SCLK is a clock pin, and MOSI is a bi-directional data pin.

PA_CS is a serial select pin. It is passed, via the rear DB25 connector to the External Power Amplifier (PA). (See 5.1)

DBGTX_TTL, DBGRX_TTL are RS232 transmit and receive (TTL) data pins which are connected to the debug port after conversion to/from RS232 compatible voltage levels by U202 and U201.

TXD_TTL, RXD_TTL, RTS_TTL, CTS_TTL, DTR_TTL, DSR_TTL, are RS232 data pins which are connected to the main front panel serial port after conversion to/from RS232 compatible voltage levels by U202 and U201.

PTT_uPHONE is a CPU input and it reflects the state of the PTT pin on the microphone handset.

TONE_INT is a CPU input that comes from the FX805 (U500). This pin is used to indicate when a Tone has been decoded, or there is some other need to service the FX805. As yet this pin is not used in the T50. (See 5.5)

LOOP_DET is a CPU pin that is asserted low if there is dc loop current detected through the centre tap input of Line2. (See 5.3)

FILTER_OFF is a CPU output that is used to by-pass, when low, the low pass filter in the Tone Input Circuitry. (See 5.5)

PTT-in is an input from the rear DB25 connector that causes the INT pin of the CPU to be asserted (low) when 1mA of current is drawn via that pin. If PTT-in is pulled to ground, through a resistance of at most 3.9kohms, it will cause INT to be asserted. If it is pulled low via a 2K2 resistor, and as many as three diodes in series, it will still cause the INT pin to be asserted. This latter example shows that quite complex diode logic can be used on this pin.

BKGD is a bi-directional I/O pin used to communicate with the core of the CPU. It is connected to the debug port and is utilised by specialised hardware to control the CPU externally, even without any firmware being present in the Flash.

DEV_H_L is a CPU output that can be used to generate a test signal in the audio path. It is currently not used. (See 5.4)

The RESET pin is both a low active input and a low active output to the CPU. If generated externally to the CPU, it forces the CPU into reset, and if the CPU executes a RESET instruction this pin will be driven low by the CPU.

Whenever there is insufficient volts ($< 4.65V$) on pin 2 of the MC33064D (U203), it will keep its RES output low. After the voltage has met the right level it will assert its output low for another 200 milliseconds. Thus the CPU will be held in reset until VCC is at the correct level. Thus the PWR_OK LED will only light when VCC is within specification, and RESET has been released.

S200 is a momentary push-button switch that, when pressed, will cause the CPU to be reset.

MOD_PLL_SEL is a serial bus select pin. It is used to select the Modulation PLL chip (U602). (See 5.6)

LCD_RS, LCD_R/W, and LCD_E are reserved for interfacing to an LCD display module. Note that this feature has not been implemented.

U205 is used to select whether the Flash or RAM is to be read or written.

U207 is a single supply, 5V, TSOP40 Flash chip of size 8, 16, or 32 Megabits, and is used to store the firmware.

U208 is a 1, or 4, Megabit Static RAM in an SOP-32 package, and is used for both code and data. The code in the RAM is copied from the Flash, at start-up.

5.3 Audio Processing Section (Sheet 3)

Sheet 3 is a schematic, which itself refers to two other sheets.

Sheet 3 shows how the two Line inputs go to audio transformers T300 and T301, are then optionally terminated by analogue switches U301B, and U301C, before being passed to the audio input stages described by Sheet 4.

It also shows how the Direct Audio (TONE) signal is passed to the Tone circuitry (sheet 5).

It also shows how dc current in Line1 will cause the opto-isolator (U300) to generate the CPU input LOOP_DET.

Relay RL300 is used to drive current back through an externally generated dc loop, when the CPU output LOOP/VOLTS_SEL is high.

The output of the Tone circuitry and the Audio circuitry is mixed (summed) and amplified by U302. It is then passed through a high order low pass filter (3.1kHz), before being attenuated by digital POT U303.

The Digital POT (U303) sets the Maximum deviation.

U302C then adds 6dB of gain before sending the audio to the modulator.

R317, D307, and C304, act as an average peak detector. This enables the CPU to determine the size of signals being handled by the audio section.

Note that the Line inputs, and the TONE input, are protected by transils and fuses against accidental connection to damaging voltages. The fuses (F300, F301, and F302) are not user replaceable.   They are surface mount devices and must be replaced by authorised service personnel.

5.4 Line Input Processing Section (Sheet 4)

The two audio inputs are passed, after transformer coupling, to sheet 4.

In Sheet 4, the two Line Inputs are input to a transconductance amplifier (U402A, and U402B). A transconductance amplifier is a current controlled, current amplifier, i.e. it amplifies input current, but its level of amplification is controlled by the level of current that is injected into pin1 or pin16. By converting a DAC output into a current, and converting the input voltage into an input current, U402A and U402B are converted into Voltage Controlled voltage Amplifiers(VCAs).

Two of the DAC outputs are converted to currents by U400B, U400C, Q401, and Q400, and these currents are used to control the gain of the transconductance amplifiers.

The input voltages are converted to current by the input load resistors R402, and R403.

The output currents are converted to voltages by resistors R420 and R424.

The outputs of the transconductance amplifiers are buffered by the darlington buffers provided with the amplifiers (U402C, and U402D).

The output of each VCA is then amplified by U405B and U405C respectively.

The level of amplification of each VCA is adjusted in software in accordance with any adjustments made to the LINE POT. The software converts the linear range of the LINE POT into a logarithmic scale, such that if the LINE POT is wound down to zero, the amplification of each VCA is reduced by 12db relative to its centre position. Similarly if the POT is wound to its maximum position, both amplifiers increase their gain by 12dB.

The outputs of these amplification stages are then attenuated. Analogue switches U404A and U404Bare used to select which attenuation circuit is used for Line 2, and U404D and U404C are used to select which attenuation circuit is used for Line 1.

If the resistive divider formed by R425, R426, and R439 is selected then the Line 2 audio signal frequency response is unaffected (it is Flat). If the reactive divider defined by C402, R431, and R439 is selected, then higher frequencies of the Line 2 audio signal are attenuated less than lower frequencies, i.e. Pre-emphasis is applied to the audio signal.

Line 1 has an identical circuit.

The outputs of these pre-emphasis/flat frequency response attenuators are then buffered by U405A, and U405D respectively.

The microphone input is amplified by U400D, after being limited by D400. It is passed through a pre-emphasis network (defined by C404, R433, and R436), and is enabled, or disabled by switch U403D.

The outputs of the Line 1 conditioning circuit, the Line 2 conditioning circuit, and the microphone input amplifier, are then mixed (summed) and amplified by U407A. Its output is, in turn, amplified by U407B, but the gain of U407B is either 2.7 or 27 depending on the state of analogue switch U403B.

The CPU is capable of injecting a clipped (saturated) signal into the audio path. This can be achieved via the two digital outputs DEV_H_L and TEST_DEV. This is currently not used.

The output of U407B is passed (signal LINE_INP) to the Line Level Sense circuitry (sheet 3) so that the CPU can determine the input line level.

U407B's output is also passed to the limiter defined by D402, and D401. Resistors R442, and R444 are used to "soften" the clipping, i.e. to "round off" the edges as the voltage hits the clipping levels. This reduces the level of the lower order harmonics produced.

U407C then buffers the output for mixing with the tone output circuitry.

The PWR_CNTRL_RAW DAC output is used to control the bias to the on-board RF amplifier (see Sheet 8). The CPU output pin PWR_CNTRL_HIGH is effectively summed with the DAC output to define three control ranges:

State of PWR_CNTRL_HIGH	PWRCNTRL Voltage Range
TriState	2.98 – 5.86
Low (0V)	0.6 – 3.0
High (5V)	3.55 - 5.96

Table 9: Power Control Ranges.

Note that in practice only the last two power ranges are used. The last is used when the External Power Amplifier is the 38-50MHz model, and the middle is used otherwise.

U401 is an octal shift register and octal latch combined. When there is a rising edge on LINEINP_DEN, the 8 shift register outputs are latched into the octal latch. The outputs of the octal latch are the outputs Q0 to Q7. Thus the last 8 data bits clocked onto MOSI, by SCLK, before LINEINP_DEN is clocked high, will appear on Q0 to Q7. This, therefore, forms an inexpensive means for the CPU to increase its number of outputs.

U406 is a quad 8 bit DAC. The CPU communicates with the DAC via SCLK, MOSI, and the select signal LINEINP_ADSEL, which is low when the DAC is selected.

U302B is used to convert the DAC output into a bias level for the LCD. The bias level, would be adjusted for temperature, and as per a calibration procedure. Note that, at this stage, the LCD display option is not developed.

5.5   Tone Generation Section (Sheet 5)

U500 is a CTCSS tone encoder and decoder. The integrated circuit is also capable of generating and receiving DCS signals, but at this stage this has not been implemented.

The CPU accesses U500 via the serial bus using MOSI, SCLK, and the low active Select signal CTCSS_SEL.

The output of the tone generator is mixed (summed) with any signals that are allowed through analogue switch U301D.

U502 is set up as a balanced differential amplifier. The resistors R530, R531, R508, R509, R510, R532, R533, and R511, are precision resistors to improve the CMRR of the differential amplifier.

U502A amplifies, as well as mixes, the two audio inputs, and its output is either passed through a low pass filter (at 250Hz), or not, depending on the state of analogue switch U301A.

The output of U502C is then attenuated by a digital POT, before being buffered by U502D.

The digital POT performs two functions. It is used to help set the maximum CTCSS tone deviation. It does this in conjunction with U500, as it is also possible for the CTCSS tones that are launched by U500 to be adjusted using software.

The second function of the digital POTs is enabled when U301D is enabled. The level of attenuation by the digital POT is adjusted (by software) in line with adjustments made by users to the LINE Potentiometer on the front panel.

R526, D502, and D503, form a limiter, that prevents any signal arriving from the TONE pair from ever exceeding 3kHz deviation.

5.6   Frequency Synthesiser (Sheet 6)

This circuit also includes Sheet 7 as a block diagram. Sheet 7 contains the schematic for the two Voltage Controlled Oscillators.

There are two complete Phase Locked Loops. One is called the Modulation PLL, and the other is referred to as the Channel PLL.

The Modulation PLL does change frequencies slightly, but by less than +/- 240kHz.

The Channel PLL is the principal PLL that changes frequencies when the exciter changes frequency.

As its name suggests, modulation is performed on the Modulation PLL.

The modulation is a conventional 2 point FM modulation. Modulation by signals, whose frequency components are well below the PLL loop frequency, is effected by modulating the reference oscillator of the Modulation PLL. Frequencies well above the PLL loop frequency are effected by modulating the Modulation VCO directly, and frequencies in the cross-over region are a combination of the two.

The heart of this schematic are the two PLL chips U602, and U604.

Each is, in fact, a dual PLL chip, but only one PLL in each is used. All that is used of the second PLL chip is its dividers. The outputs of these dividers can be switched to the FoLD output pin, which is then converted to a square wave by a further division of 2 by U606A and U606B.

By using the second PLL's dividers it is possible to divide the reference oscillator, and the VCO output down to frequencies that can be handled by the Timer inputs of the CPU, without causing excessive interrupt load to the CPU.

5.6.1   The Modulation PLL

U602 and the Modulation VCO (see Sheet 7) form the modulation PLL. U602 acts as its own crystal oscillator for its reference oscillator. X600 is a 5ppm, 12MHz, crystal. Its resonant point is adjusted by the bias applied to varactor D600.

The bias applied to varactor D600 is a combination of the potentials at two DAC outputs (MOD_ADJ and MOD_ADJ_FINE), plus the modulating signal arriving at MOD_IN (which is the same signal as MOD_OUT in Sheet 3).

The summing of these three voltages is performed by U607.

The Phase detector output of the PLL chip is then passed through the loop filter network defined by C612, R618, C625, R617, C613, and C718 (see Sheet 7). L713 is used to filter out any residual noise (outside of the audio bandwidth), including the phase detector frequency, and/or any switch-mode noise from the dc voltage rails.

The loop filter signal is then fed as a control voltage to the Modulation VCO (MOD_PLL_IN).

The output of the Modulation VCO is connected back to the PLL for phase detection via signal path MOD_VCO_OUT.

The phase detector output is also buffered and attenuated for the analogue input of the CPU. This is the function of U600, R622, and R625. In this way the CPU can monitor the VCO bias to ensure that it is within specification ($>0.5V$, and $< 4.5V$).

The FoLD pin, of U602, can be used for many purposes. It can be connected to the output of any of the 4 internal dividers, or be used as a LOCK-DETECT monitor, or as a user programmable output pin. In this circuit it is used as a LOCK-DETECT output when the frequency is being changed, but otherwise it is connected internally to the unused reference divider of U602, to deliver a 400Hz pulse train to FoLD.

U602 is set up with a phase detector frequency of 20kHz.

5.6.2   The Channel PLL

U604 and the Channel VCO (see Sheet 7) form the Channel PLL. U604 acts as its own crystal oscillator for its reference oscillator. X601 is a 5ppm, 12MHz, crystal. Its resonant point is adjusted by the bias applied to varactor D601.

The bias applied to varactor D601 is adjusted by the CHAN_ADJ DAC output.

The Phase detector output of U604 is then passed through the loop filter network defined by C622, R620, C626, R619, C623, and C725 (see Sheet 7). L718 is used to filter out any residual noise (outside of the audio bandwidth), including the phase detector frequency, and/or any switch-mode noise from the dc voltage rails.

The loop filter signal is then fed as a control voltage to the Channel VCO (CHAN_PLL_IN).

The output of the Channel VCO is connected back to the PLL for phase detection via signal path CHAN_VCO_OUT.

The phase detector output is also buffered and attenuated for the analogue input of the CPU. This is the function of U608, R623, and R624. In this way the CPU can monitor the VCO bias to ensure that it is within specification ($>0.5V$, and $< 4.5V$).

The FoLD pin, of U604, can be used for many purposes. It can be connected to the output of any of the 4 internal dividers, or be used as a LOCK-DETECT monitor, or as a user programmable output pin. In this circuit it is used as a LOCK-DETECT output when the frequency is being changed, but otherwise it is connected internally to the unused reference divider of U604, to deliver a 400Hz pulse train to FoLD.

U604 is set up with a phase detector frequency of 31.25kHz.

The signal CHAN_VCO_EN is an output from the CPU that is used to turn on (when High) or turn off (when low) the Channel VCO.

5.6.3   The External Reference Divider

The external Reference Input (EXT_REF_IN) is buffered by an attenuator network formed by R628,R633, and R630 in parallel with R635. This also forms a 50 ohm termination network for the reference input.

R628 is a 1 watt resistor, and so, in theory levels as high as +30dBm can be accepted. To be safe, though, the largest signal that is approved to be accepted is +26dBm.

Q600 is set up as a switching transistor, and with a sufficiently high input signal level (> +5dBm), it will clock U605.

U605 is set up as a divide by 128 circuit, and its output is then divided by U606 by 25.

The two unused, divide by two, stages of U606 are then used to convert the 400Hz FoLD pulse trains into 200Hz square waves for the Timer inputs of the CPU.

5.6.4   The DAC

U601 is a quad DAC. It is programmed by the CPU via the serial bus (SCLK and MOSI). It is selected by the low active signal SIGGEN_ADSEL.

Three of its outputs are used to adjust the reference oscillators.

In the presence of a GPS 1Hz pulse input, or an external reference oscillator, the software will automatically track the channel VCO to these external inputs. (GPS has priority over an external reference).

The modulation reference oscillator is always tracked as closely as possible to the Channel reference oscillator. Because of this need for very close tracking, two DAC outputs are summed. In this way, the CPU is given coarse, as well as fine control.

The CPU can sense a phase difference of 136ns in 4 seconds, i.e. as little as 0.034ppm between the two PLL reference oscillators. Each step of the MOD_ADJ_FINE DAC output will move the frequency about one eighth of this amount.

The other DAC output (BALANCE) is used to adjust the BALANCE VCA (see sheet 7).

The user programmable digital output of the DAC (MOD_VCO_EN) is used to enable the modulation VCO (when High)

5.6.5 The VCOs and the RF Output

These are more closely described in 5.7, but it is worth noting that there are three primary outputs of the VCOs. There is each VCO output itself, but also the signal VCO_OUT. This is the difference frequency between them.

Generally the modulation VCO is set to oscillate at 320MHz. To get an output of 40MHz, the Channel VCO is set to 280MHz.

But if you wanted an output frequency of, for example, 40.00125MHz, then the modulation VCO would change to 319.78125 MHz (i.e. it drops by 218.75kHz), and the Channel VCO would become 279.78MHz (i.e. dropping by 220kHz).

By such small changes in the modulation VCO (maximum delta is +/- 240kHz), each multiple of 1250Hz can be accommodated, but without any need to ever change the two phase detector frequencies.

5.7   Voltage Controlled Oscillators (Sheet 7)

JFETS Q704, and Q705 are the heart of two Colpitts oscillators.

The capacitor feedback divider for Q704 (modulation VCO) is defined by C732 and C733, and this shapes the negative impedance looking into the drain of Q704.

In the Channel VCO, C740 is effectively in series with Cgs of Q705. These, then define the negative impedance looking into the drain of Q705.

L716, in parallel with L726 forms the tank coil for the modulation oscillator, and the resonant capacitance is defined by the series combination of C750 and the capacitance across D701. L712 has +ve reactance and it acts to reduce the minimum effective capacitance seen back through C750, thereby increasing the tuning range slightly.

Similarly, L719 is the tank coil for the channel oscillator, and the resonant capacitance is defined by the series combination of C751 and the capacitance across D704. L717 has +ve reactance and it acts to reduce the minimum effective capacitance seen back through C751, thereby increasing the tuning range slightly.

The VCO frequencies are controlled by the bias applied to D701 and D704 respectively, which is set by signals MOD_PLL_IN and CHAN_PLL_IN. These signals are the phase detector outputs from the Modulation PLL and the Channel VCO respectively (see Sheet 6).
Diodes D700 and D703 are used to provide some AGC for the JFETs. These Schottky diodes will increase the –ve bias on the gate of the JFETs (thereby decreasing the drain

current) if the oscillation level should increase, and similarly the gate bias will reduce if the –ve peaks of the oscillation should reduce.

The Modulation bias is also adjusted by the modulation input (2PORT_MOD). This signal is amplified by a VCA. The BALANCE DAC output is converted to a current by U707 and Q700, and that then is used to set the gain of the VCA. The output of the VCA is then attenuated by R725/R729, and this bias is then applied to varactor D701. Note that the modulation bias is in anti-phase to the PLL bias.

Each VCO has its own gyrator feed circuit (Q707 and Q702). This is done to remove any possible noise on the voltage rails from effectively modulating either VCO.

The drain current of each VCO can be switched off or on by MOSFETs Q701 and Q703. Q701 is switched on when MOD_VCO_EN is high. MOD_VCO_EN is the user programmable digital output from DAC U601 (see Sheet 6). Q703 is switched on when the CPU output CHAN_VCO_EN (see Sheet 2) is high.

The output of each VCO is "sniffed", by a high impedance attenuator. In the modulation VCO, R737 in series with the 50 ohm input impedance of U702 forms this attenuator. In the Channel VCO, R745, R736, and the input impedance of U706 form one such attenuator, and R741 in series with the input impedance of U703 forms the other.

U702 amplifies the modulation VCO signal, which is then amplified again by U701, then filtered to reduce harmonics, before arriving at the LO input of MX700 at a level of around +5 - +7dBm.

The output of U702 is also attenuated by R733, and then re-amplified before becoming MOD_VCO_OUT. MOD_VCO_OUT is then passed to the Modulation PLL (U602, see Sheet 6). U703's primary role is to ensure that noise that becomes coupled by the PLL chip, back onto its VCO input, does not couple back into the path to the mixer. If this isn't done, then the mixer's LO input contains many harmonics of the reference oscillator.

U703 performs both an amplification role, and an isolation role similar to U703's. Its output (CHAN_VCO__OUT) is fed back to the Channel PLL (U604, see Sheet 6).

U706 and U701 are both designed to be in "gain compression", i.e. their outputs are saturating, so that significant changes in their input levels will not significantly change their output levels. U706, though, starts its gain compression at about 10dB lower than U701. In this way, variations in output level caused by variations in the parameters of the JFETS Q704, and Q705, will not significantly modify the levels of signals arriving at the mixer MX700.

The output of U706 is attenuated by the network R714, R742, and R724, and then it is filtered to reduce the VCO harmonics as much as possible. This filtered VCO output is then brought to the RF pin of the mixer at a level of about –20 to –22dBm.

The output of the mixer is then run through a low pass filter to remove frequencies other than (Fmod - Fvco). U700 then amplifies this signal to a level of about –6 to –8dBm.

The external output signal of T/R_RELAY, which is asserted low whenever the exciter is keyed up, is used to switch MOSFET Q706 off. When Q706 is off, amplifier U700 is enabled. When T/R_RELAY is high, then U700 is deprived of bias current and VCO_OUT is then completely disabled.

5.8   1W Broadband HF Power Amplifier (Sheet 8)

The HF output of Sheet 7 (VCO_OUT) becomes the primary input to this circuit (RF_IN).

This RF input is first amplified to a level of about +2 to +4dBm by U800, then it is amplified by Q801 to about +20dBm (with full bias), and then it is amplified by Q804 and Q805 to +30dBm. The output stage gain is less above about 42MHz, so that the peak output power falls to about +26dBm at 50MHz.

The effective gain of Q801 is controlled by adjusting the bias level (PWRCNTRL). This can vary from 0.6V to nearly 6V, and is adjusted by a DAC output and a CPU digital output, in Sheet 4.

The software monitors the forward power sense in the External Power Amplifier(PA) as well as the Reverse Power, temperatures, drain currents etc. It does this via the serial bus (formed by SCLK and MOSI) and the select pin for the ADC converter on the External PA (PA_CS).

The software then automatically adjusts the PWRCNTRL bias to:

1)   Keep the forward power at the level defined by parameter PA_SET_FWD_PWR (see 4.1), unless,

2)   If the reverse power is higher than PA_SET_FWD_PWR*REV_PWR_ALARM/100.0 then the forward power is reduced until the reverse power stops exceeding this limit, or,

3)   The temperature of the PA output stage FETs exceeds 120C, in which case forward power is reduced until this stops occurring.

5.9   Power Generation Section (Sheet 9)

There are three switch mode dc-dc converters in the board. These use monolithic converters based on the National LM2595. Two of the converters are 12V converters and one is a 5V converter.

The power in to the whole exciter is the voltage rail 28V.

U907 converts this down to 12V.

U908 is set up as an inverter, and uses the 12V rail to create –12V.

U909 converts the +12V rail to +5V for all the digital circuitry.

The +12V rail is used to power the two on-board relays, as well as up to one extra off-board relay. It is also dropped, via a linear regulator (U910) to produce the +10V rail, which in turn is dropped by another linear regulator U911 to produce +5Q, which, in turn, is dropped by a further linear regulator (U912) to produce +2.5V.

Similarly U913, U914, and U915 are linear regulators that produce –10V, -5V, and –2.5V from the –12V output of U908.

+10, +5Q, and +2.5V, -10V, -5V, and –2.5V rails are used in the audio and RF sections.

D911 is a 4.096V (3%) reference diode. Its output is buffered by U906 which then produces a reference voltage rail Vref, which is used by the CPU's A/D converter, and the DACs, and also in the voltage to current converters of the VCAs (see Sheet 4, and Sheet 7).

6   FIELD ALIGNMENT PROCEDURE

6.1   Standard Test Equipment

Some, or all of the following equipment will be required:

- AF signal generator, 75 - 3000Hz frequency range, with output level set to 387mV RMS and, if the microphone input is to be tested, 10mV rms output.

- Power supply set to 28Vdc, with current >10A.

- RF 50Ω load(s), 250W rated, return loss <-20dB, and total attenuation of 50dB

- Reference Oscillator. At least +5dBm output.
  The external reference frequency is limited to:

    500kHz, or any multiple,
    any multiple of 128KHz greater than or equal to 4,
    any multiple of 160KHz greater than or equal to 3
  The accuracy should be at least 0.5ppm, preferably 0.1ppm

- RF Peak Deviation Meter

- True RMS AC voltmeter, and a DC voltmeter.

- RF Power Meter (accurate to 2%, i.e. 0.17dB)

- Some means of measuring Reverse Power, and a known 3:1 mismatched load.

6.2   Invoking the Calibration Procedure

The T50 has in-built firmware to perform calibration. This firmware requests the user for information as to meter readings, and/or to attach or adjust the AF signal generator.

The firmware based calibration program can be accessed from a terminal, a terminal emulator, or the Eclipse50 terminal emulator.

As for Section 4.1, the firmware, after power up, issues the following prompt:

> *T50>*

Via a terminal, or a terminal emulator, a user can type various commands in. The basic command to start the calibration procedure is:

> *T50>* cal calibration_type

Where "calibration_type" is one of:

a)   misc: Miscellaneous parameters are defined and calibrated
b)   dev: Maximum deviations are set (automatically forces a "cal line" and a "cal tone")
c)   line: Line1, Line 2, Dir Aud (Tone), and microphone inputs are tested and calibrated.
d)   pwr: The External PA attached to this unit is calibrated.
e)   ref: The reference oscillators are adjusted and calibrated
f)   tone: The maximum tone deviations are calibrated
g)   all :   (which does all the above)

6.3   The "Miscellaneous" Calibration Procedure

> *T50>* cal misc

This procedure should not normally be invoked as part of any field maintenance.

The program will print out the Model Name and Serial Number of the exciter. If these parameters haven't already been defined (e.g. at an initial calibration, at the factory, the service personnel will be prompted to enter these values).

Then it will ask the operator to enter the value of Vref (as measured at TP913, see 5.9).

> *Measure the voltage, at TP913 (Vref)*
> *and type it on the command line...*

Unless the reference diode D911 has been replaced, this should not be done. The user should simply hit the Enter key to bypass this operation. If, though, D911 has been replaced for some reason, then, the lid of the unit should be removed, and the voltage measured. TP913 can be found just above JP12 (near the centre of the exciter).

Then the exciter low battery alarm level will be asked for. If the current value is acceptable, the User need only hit the Enter key on the keyboard. If another value is preferred, then that value can be typed in.
For example:

> *The Exciter's Low Battery Alarm is 24V*
> *If this is correct enter <RET>,*
> *else enter the new value:* 26

In this example, the low Battery Alarm level is changed to 26V.

The next request for the User should always be ignored.

> *The Exciter's default Modulation VCO Frequency is 320MHz*
> *If this is correct enter <RET>*
> *else enter the new value:*

This parameter is for future use only. Please always hit the Enter key.

Then the user will be prompted for serial port baud rates, parities etc. Please leave these parameters unchanged unless you are familiar with how to change such parameters on your PC. The Eclipse50 software will expect 57600 BPS, and No Parity, and No Flow Control. Note well, that if you do change any of these, the change will not take effect until you power down the exciter and then power it up again. (As an alternative to power cycling the exciter, and if the cover is off the exciter, you may simply press switch momentary push-button S200 (see 5.2).

The next thing the calibration program tests is the state of the LINE pot. The program will ask the user to adjust this pot. If the Potentiometer is below centre, it will ask the user to adjust it up (i.e. adjust it clockwise). If it is above centre, it will ask the user to adjust it down (i.e. adjust it counter clockwise). When the POT has been centred, or, the User hits the Enter key, the program will terminate.

This last step is normally only done as part of a factory install, and it is done to ensure that the POT is centred before being shipped to customers. For field maintenance purposes, the step should be skipped in order to leave the LINE POT at the setting formerly desired.

6.4   The "Reference" Calibration Procedure

> *T50>* cal ref

To compensate for crystal ageing and other parameters that drift, the following procedure should be performed approximately once per year.

If your exciter is fitted with the external reference option (an extra BNC connector on the rear panel), the user can connect an external reference directly to the rear BNC connector. If the exciter does not have this option, then the top cover of the exciter

should be removed and an external reference oscillator should be connected via a 50 ohm probe to J4 (just to the right of the DC voltage regulators and converters).

The external reference clock, should have a power level from +5 to +26dBm and any frequency that meets the following criteria:

> 500kHz, or any multiple,
> any multiple of 128KHz, greater than or equal to 4,
> any multiple of 160KHz, greater than or equal to 3,

No User input is required, except to hit the Enter key when the external reference is connected. The firmware will automatically adjust both reference oscillators, and save the new DAC adjustments in FLASH (as parameters) to be used to centre the oscillators each time the unit powers up.

The user should see the following output. (Note that the temperatures, frequencies, error values, serial number, etc, indicated are examples only)

> *Connect an external reference input or the clock output*
> *from a GPS receiver to the GPS input.*
> *Enter <RET> when this has been done.*
>
> *External Reference is 10.0MHz*

Ensure that the displayed reference frequency (10.0MHz in the above example) is the same as the frequency of your oscillator.

> *Waiting for a GPS clock.*
>
> *. . . . . .*

The system waits here for a GPS reference to be seen. At this stage, this method of calibrating the clocks has not been validated by RFT Engineering, so do not attempt to use this option as yet.

Then the firmware continues.

> *Have not observed a GPS clock*
>
> *System Frequency relative to external clock is 7372654.32*
> *The crystal temperature is 22C.*
>
> *Waiting up to 1 minute for clocks to stabilise.*
>
> *. . . . . .*
>
> *The crystal temperature is 22 C*
>
> *The channel ref error = 1 cnts or, 1.63 Hz*
> *The mod ref error = 1 cnts or, 1.63Hz*

The user may see the following error message.

> *The Model Name is T50*
> *and the Serial Number is 002313*
> *Please take note of the Model, DAC values, serial number and*
> *crystal temperature, and report this problem to RFT Engineering.*

If this message is seen, it indicates a potential fault condition. If the final text indicates that the channel and mod reference errors are within specification (the last text output), then the unit is able to be used, but nonetheless, it is advisable that an e-mail be sent to RF Technology indicating the problem. Such a problem may be caused by a crystal having aged to such an extent, that it is getting close to the region where it may soon, no longer be adjusted, or that, with further degradation, the low frequency performance may be compromised.

As no other calibration procedure requires the top cover to be removed, you should replace the cover, should you have had to remove it for this procedure.

6.5   The "Deviation" Calibration Procedure

> *T50>* cal dev

This procedure should not normally be invoked as part of any field maintenance. The only conceivable time that it might ever be used, would be if a non standard maximum deviation was required.

The first stage begins with the following message:

> *This procedure sets the Balance and Max Deviation Levels*
> *Connect an audio signal generator to the Line 1 inputs*
> *Set the output to be a sine wave, 388mV rms and 75Hz*
> *Disconnect the RF connection to the PA*
> *and connect a deviation meter to the exciter's BNC output.*

Note that the nominal output power of the exciter's output is 1W. Whilst the power level is not set to the maximum level, the deviation meter should either have an input power rating of at least +30dBm, or suitable attenuation is required between the exciter and the deviation meter. Note that for this test the nominal RF output frequency is 37.5MHz.

> *Enter + or - to increase or decrease the deviation,*
> *and <RET> when the deviation is 5kHz*
> *   ?*

Here the user can hit the +, p, or P, keys to increase the deviation, or -, m, or M keys to decrease it. In response, the firmware, which has opened up the maximum deviation digital POT (U303) to maximum gain is adjusting the Line1 VCA accordingly. When the deviation is as close to 5kHz as can be obtained, the User should hit their Enter key.

Then the firmware will make the following request.

> *Change the signal generator frequency to 1kHz*

When this has been done, the User needs to hit the Enter key, and the following will appear again.

> *Enter + or - to increase or decrease the deviation,*
> *and <RET> when the deviation is 5kHz*
> > *?*

In response to the +, or – keys (or m, p, M, or P), the firmware adjusts the BALANCE VCA accordingly. The user should do this until the deviation is as close to that achieved at 75Hz as possible.

That now sets the balance.

The firmware will now prompt the user for a "User specified Deviation". This is a deviation other than the following standard deviations, 5.0kHz, 4.0kHz, 3.0kHz, 2.5kHz, 2.0kHz, and 1.5kHz. At the factory, it is set to 4.5kHz.

> *Enter the User Specified Deviation (kHz):* 4.5

In this example, the user has specified 4.5kHz deviation.

Then the software will automatically set the Hi-Gain option on, which will cause the output to got to somewhere between 7 and 9kHz deviation, and it will be very clipped.

Then the user will be prompted, as it was for the Balance adjustment, to enter keys to set the deviation to as close to 5kHz as possible, whilst still being lower than 5kHz. That sets the deviation setting for U303 for 5kHz maximum deviation. This is then followed by the same procedure to set the 4kHz maximum deviation setting, then 3kHz, 2.5khz, 1.5kHz, and then the User Specified Deviation (e.g. 4.5kHz).

The least significant BCD digit of the deviation parameter, in a channel setting, selects the appropriate maximum deviation when the exciter keys up. (See 4.2 and Table 7). In this way, for example, it may be possible to allocate frequencies in the band 30-40MHz on 12.5kHz channel spacing, and on 20kHz channel spacing over the band 25-30MHz.

6.6   The "Tone Deviation" Calibration Procedure

> *T50>* cal tone

This procedure should not normally be invoked as part of any field maintenance. The only conceivable time that it might ever be used, would be if a non standard maximum tone deviation was required.

This procedure is similar to the maximum deviation procedure (See 6.5). The Line 1 and Line 2 audio paths are turned off for this procedure, as is the Direct Audio (TONE) input. The only signal sent to the modulator is a tone of 107.2Hz.

The program starts off, with the following message:

> *This procedure sets the maximum tone deviations for a*
> *Max Deviation of 5kHz.   Note that the actual maximum*
> *tone deviations automatically scale with the Max Deviation.*
> *eg a 500Hz tone deviation would be a 250Hz tone deviation*
> *when a 2.5kHz Max Deviation was chosen.*
> *Disconnect the RF connection to the PA,*
> *and connect a deviation meter to the exciter's BNC output.*
>
> *The audio is being switched off, and 107.2Hz tone generated*
> *Enter the User Specified Tone Deviation(Hz):*

The user is expected to connect up the deviation meter, and enter the User Specified Maximum Tone Deviation. This is a deviation that is different to the standard deviations of 750Hz, 500Hz, 375Hz, 250Hz, and 150Hz. The factory default for this is 600Hz.

Thence a procedure that is almost identical to that used for setting maximum deviations is used to set these tone deviations. There is one significant difference, though, and that is, as well as using + (or p, or P), and – (or m, or M) keys to step the deviation up or down, one can also use the < key, or the > key. These last two keys will step down, or up, the level of signal transmitted by U500, whereas the other keys will modify the setting of the digital POT U503 (see 5.5).

6.7   The "Line" Calibration Procedure

> *T50>* cal line

This procedure should not be used as part of any usual field maintenance, unless any component has been replaced that might affect the gain of any of the audio inputs.

Note that if the deviations are calibrated, then this procedure will be automatically invoked.

The program begins:

> *Calibrating Line 1 and Line 2 audio levels*
>
> *Attach an audio signal generator to Line 1*
> *Set the output to be a sine wave, 388mV rms and 1kHz*
> *Disconnect the RF connection to the PA*
> *and connect a deviation meter to the exciter's BNC output.*
>
> *Enter + or - to increase or decrease the deviation,*
> *and <RET> when the deviation is 3kHz*

> *?*

This is the same mechanism that is used in 6.5 and 6.6. The user enters +, p, or P to increase the Line 1 gain, to increase the deviation, or, -, m, or M to decrease the gain. The user hits the Enter key when the desired deviation is set.

> *Now attach the audio signal generator to Line 2*
>
> *Enter + or - to increase or decrease the deviation,*
> *and <RET> when the deviation is 3kHz*
> > *?*

Again the user enters +, p, or P to increase the Line 2 gain, to increase the deviation, or, -, m, or M to decrease the gain. The user hits the Enter key when the desired deviation is set.

The firmware goes on to open the microphone audio path (note that the microphone PTT switch does not need to be depressed for this). Note also that the application of a 10mV test input is a factory only test. An adequate test in field testing, would be to speak into the microphone and see that the deviation meter responded accordingly.

> *Testing the microphone input.*
> *Attach an audio signal generator to the microphone input.*
> *Set the output to be a sine wave, 10mV rms and 1kHz.*
> *Ensure that the deviation is between 2.7 and 3.3kHz*
> *Enter <RET> when measurement complete.*
> *Alert Engineering if there is a failure.*

Then the Direct Audio input (with the low pass filter off) is tested.

> *Testing the Tone input.*
> *Attach an audio signal generator to the Tone input.*
> *Set the output to be a sine wave, 388mV rms, and 1kHz.*
>
> *Enter + or - to increase or decrease the deviation,*
> *and <RET> when the deviation is 3kHz*
> > *?*

And then user then follows the same procedure as defined for setting the Line 1 and Line 2 gains. Note that the digital POT does not provide the same linearity as the VCAs used in the line input audio circuits. As such it may not be possible to set the deviation to exactly 3kHz.

6.8   The "Power" Calibration Procedure

> *T50>* cal pwr

All Power Amplifiers are calibrated ex-factory. All the important parameters, such as the forward and reverse power sense adjustment, and drain bias settings are not dependent on the exciter, and thus any factory calibrated PA50 power amplifier can be connected to, and work correctly with any T50 exciter. The frequency range of the amplifier is defined by three jumper settings on the external PA, which the CPU can

detect. Thus the CPU knows (on power up) what frequencies are, or are not, possible to be used with the PA.

The exciter does store some PA specific parameters, such as the Serial Number of the PA, and also some offset values for the pre-amp drain current, and the output stage drain current. These latter offsets improve the accuracy of the over current alarm testing, (but are not strictly necessary). In order to set these parameters, it is advised that this procedure be performed every time an exciter is used with a new External Power Amplifier. Note that many of the stages can be skipped if they have been performed before.

The program begins:

> *This procedure is used to calibrate an External Power Amplifier.*
> *The existing PA's SERIAL NO is: 002356*
> *Enter the new PA serial no:*

Simply hit the Enter key here if the Serial Number is correct.

> *Take the lid off a PA, and set all three*
> *bias Pots (R238,R239, and R240) fully clockwise.*
> *Enter <RET> when done.*

> *Now we will set the Bias currents in the PA.*

> *Attach power to the PA.*
> *Attach a calibrated millivoltmeter between TP100(+ve lead)*
> *and TP101(-ve lead). Adjust R238 until the meter reads 50mV*
> *Enter <RET> when done*

> *Attach the calibrated millivoltmeter between TP102(+ve lead)*
> *and TP103(-ve lead). Adjust R239 until the meter reads 10mV*
> *Enter <RET> when done.*

> *Adjust R240 until the meter reads 20mV*
> *Enter <RET> when done.*

Unless one of the RF power transistors has been replaced, the user should simply skip these last four stages by hitting the Enter key four times.

> *Attach the Power Amplifier to the Exciter,*
> *and ensure the PA is powered up.*
> *Attach the PA output to a reflectometer, the reflectometer to a 50dB*
> *(nominal) attenuator, and the attenuator to a calibrated power meter*
> *Enter <RET> when this has been done");*

> *Adjust C209 in the Power Amplifier*
> *until there is a minimum in the dc voltage measured at TP204*
> *Enter <RET> when done.*

> *Adjust the Forward Power Sense POT (R228) until*
> *the measured output power (adjusted for the attenuator and*
> *reflectometer losses) is equal to the Preset Forward Power.*
> *Enter <RET> when done.*

Unless something has been modified in the power sense circuits, these last three stages should be skipped by simply hitting the Enter key three times.

This next step is necessary, and it allows the firmware to compute an offset in the output stage drain current, so that the exciter's ability to measure the output stage drain current is significantly more accurate.

> *Measure the voltage across TP102(+ve lead)*
> *and TP103(-ve lead), and enter the value measured*

This next step is also necessary, and it allows the firmware to compute an offset in the pre-amp stage drain current, so that the exciter's ability to measure the pre-amp stage drain current is significantly more accurate.

> *Measure the voltage across TP100(+ve lead)*
> *and TP101(-ve lead), and enter the value measured*

The next two stages can be skipped by simply hitting the Enter key twice.

> *Attach the reflectometer to an open circuit*
> *Enter <RET> when this has been done*

> *Adjust the Reverse Power Sense POT (R227) until*
> *the displayed reverse power equals 50W.*
> *Enter <RET> when this has been done.*

This then completes all the calibration procedures.

7   SPECIFICATIONS

7.1   Overall Description

The transmitter is a frequency synthesized, narrow band, HF, FM unit, used to drive an external 120 watt amplifier. All necessary control and 600 Ω line interface circuitry is included.

7.1.1   Channel Capacity

Although most applications are single channel, it can be programmed for up to 100 channels, numbered 0-99. This is to provide the capability of programming all channels into all of the transmitters used at a given site. Where this facility is used in conjunction

with channel-setting in the rack, exciter modules may be "hot-jockeyed" or used interchangeably. This can be convenient in maintenance situations.

Channel information consists of two independent and complete sets of information, which may differ or be the same. One set defines the parameters to be used, if the unit is keyed up from PTT-in being "grounded", and the other set defines the parameters to be used if the unit is keyed up for any reason other than PTT-in being "grounded".

The parameters that can be defined on a per channel basis are:

- a) The frequency

- b) The CTCSS tone (if any) to be generated

- c) The delay from the initiation of the exciter to RF output being generated (Is specified in hundredths of a second, 0 – 999)

- d) The transmit tail; the length of time after the exciter is released before transmission stops. (Is specified in seconds 0 – 999).

- e) The No Tone period; a length of time after the expiry of (d) in which transmission continues, but with no tone being generated. (Is specified in tenths of a second, 0 –999)

- f) Whether audio from Line 1, or Line 2, or both, (or neither!) is enabled, and whether or not Pre-emphasis is required, or not, on each line, and whether or not an extra gain pad (of 20dB) is required.

- g) What Nominal Tone Deviation, and Maximum Deviation should be used (See Tables 7 and 8)

7.1.2   CTCSS

Full EIA subtone Capability is built into the modules.   The CTCSS tone can be programmed for each channel. This means that each channel number can represent a unique RF and tone frequency combination.

7.1.3   Channel Programming

The channel information is stored in non-volatile memory and can be programmed via the front panel connector using a PC, and/or RF Technology software.

7.1.4   Channel Selection

Channel selection is by eight channel select lines connected to the rear panel that mounts on the rear DB25 female connector.

A BCD active high code applied to the lines selects the required channel. This can be supplied by pre-wiring the rack connector so that each rack position is dedicated to a fixed channel. Alternatively, thumb-wheel switch panels are available.

7.1.5. Microprocessor

A microprocessor is used to control the synthesizer, tone squelch, PTT functions, external reference monitoring, calibration, fault monitoring and reporting, output power level control, volume adjustment, line selection, option setting, and facilitate channel frequency programming.

7.2   Physical Configuration

The transmitter is designed to fit in a 19 inch rack mounted sub-frame. The installed height is 4 RU (178 mm) and the depth is 350 mm. The transmitter is 63.5 mm or two Eclipse modules wide.

7.3   Front Panel Controls, Indicators, and Test Points

7.3.1   Controls

Transmitter Key - Momentary Contact Push Button

Line Input Level - screwdriver adjust multi-turn pot

7.3.2   Indicators

Power ON - Green LED

Tx Indicator - Yellow LED

Fault Indicator - Flashing Red LED

7.3.3   Test Points

There are no front panel test points. All important test points are monitored by the firmware.

7.4   Electrical Specifications

7.4.1   Power Requirements

Operating Voltage - 16 to 32 Vdc

Current Drain - 1A Maximum, typically 0.25A Standby

Polarity - Negative Ground

7.4.2   Frequency Range and Channel Spacing

The T50, as a single model, covers the full band, and all channel spacing.

Frequency	25 kHz	20kHz	15kHz	12.5 kHz	10 kHz	7.5 kHz	6.25 kHz
25 - 50 MHz	T50	T50	T50	T50	T50	T50	T50

7.4.3   Frequency Synthesizer Step Size

The specified frequency can be any multiple of 1250Hz.

7.4.4   Frequency Stability

±5 ppm over 0 to +60 C, standard

±2 ppm over -20 to +60 C, optional

7.4.5   Number of Channels

100, numbered 00 - 99

7.4.6   RF Output Impedance

50Ω

7.4.7   Output power

The T50 needs an external PA50 power amplifier.

The output power is factory set to 100W by default, the reverse power level is set to fold back the output power when the PA50 sees a load with VSWR of 3:1 or higher (i.e. when the reverse power is 25% or more of the forward power).

7.4.8   Transmit Duty Cycle

100%

7.4.9   Spurious and Harmonics

Less than 0.25μW, when connected to a PA50 operating at an output power level of 100W.

7.4.10   Carrier and Modulation Attack Time

Less than 25ms. Certain models have RF envelope attack and decay times controlled in the range 200μs$< t_{r/f} <$2ms according to regulatory requirements.

7.4.11 Modulation

Type - Two point direct FM with optional pre-emphasis

Frequency Response - $\pm$1 dB of the selected characteristic from 300-3000Hz

Maximum Deviation - Maximum deviation set on a per channel basis to 1.5, 2.0, 2.5, 3.0, 4,0, or 5.0 kHz. A User Specified Maximum deviation can be preset as well. (Please request this when ordering the unit).

7.4.12   Distortion

Modulation distortion is less than 3% at 1 kHz and 60% of rated system deviation.

7.4.13   Residual Modulation and Noise

The residual modulation and noise in the range 300 - 3000 Hz is typically less than -50dB with 5kHz maximum deviation (i.e. a test level of 3kHz).

7.4.14 600Ω Line Input Sensitivity

Adjustable from -32 to +12 dBm for rated deviation on two symmetric, independent, transformer coupled Line inputs.

7.4.15   Test Microphone Input

200Ω dynamic, with PTT

7.4.16   External Tone Input

Compatible with R500 tone output

7.4.17   T/R Relay Driver

An open drain MOSFET output is provided to operate an antenna change over relay or solid state switch. The transistor can sink up to 250mA. A 1W flywheel diode connects to the 12V rail to prevent damage to the FET from inductive kick from a relay coil.

7.4.18 Channel Select Input/Output

Coding - 8 lines, BCD coded 00 - 99

Logic Input Levels - Low for <1.5V, High for >3.5V

Internal 10K pull down resistors select channel 00 when all inputs are O/C.

7.4.19 DC Remote Keying

An opto-coupler input is provided to enable dc loop keying over balanced lines or local connections. The circuit can be connected to operate through the 600Ω line.

7.4.20 PTT in

An external input that when "grounded" with at least 1mA of current, will cause the exciter to key up. The current is drawn from the PTT in input which attempts to "pull up" anything that "grounds" it. It can be "grounded" with a short to 0V, or any resistance up to 3.9k ohm. If the resistance of the "ground connection" is less than 2.2k ohms, then up to three diodes in series can be part of the grounding path. This allows systems installers to use quite complex diode logic to enable or disable exciters.

It would normally be "grounded" by the COS output of a receiver.

7.4.21 Programmable No-Tone Period

A No-Tone period can be appended to the end of each transmission to aid in eliminating squelch tail noise which may be heard in mobiles with slow turn off decoders. The No-Tone period can be set from 0-99.9 seconds in 0.1 second increments.

7.4.22 Firmware Timers

The controller firmware includes some programmable timer functions.

Repeater Hang Time(Transmit Tail) - A short delay or ``Hang Time'' can be programmed to be added to the end of transmissions. This is usually used in talk through repeater applications to prevent the repeater from dropping out between mobile transmissions. The Hang Time can be individually set on each channel for 0 - 999 seconds.

Time Out Timer - A time-out or transmission time limit can be programmed to automatically turn the transmitter off. The time limit can be set from 0-10million seconds. The timer is automatically reset when the PTT input is released. Zero seconds disables the timer, and allows continuous transmission.

7.4.23   CTCSS

CTCSS tones can be provided by an internal encoder or by an external source connected to the external tone input. The internal CTCSS encoding is provided by a subassembly PCB module. This provides programmable encoding of any tone, accurate to 0.1Hz, including all EIA tones, from 67.0Hz to 257Hz.

7.5   Connectors

7.5.1   RF Output Connector

BNC connector on the module rear panel.

7.5.2   Power & I/O Connector

25-pin "D" Female Mounted at the top of the rear panel

7.5.3   External Reference Connector (optional)

BNC connector mounted in the middle of the rear panel connector.

A   Engineering Diagrams

There is only one printed circuit board covering all models of the T50. There is only one option for this product, which is the external reference clock option. That option adds a rear connector, and a small length of coaxial cable and a fixed coaxial cable mount to the parts list.

Unlike other products in the Eclipse range, CTCSS is no longer an option. All units have the ability to transmit CTCSS tones.

A.1   Block Diagram

Figure 1 shows the block signal flow diagram.

A.2   Circuit Diagrams

Figure 2 shows the detailed circuit diagram with component numbers and values for the main (exciter) PCB. Figure 3 shows the detailed circuit diagram with component numbers and values for the higher-power PA variation. Figure 4 shows the detailed circuit diagram with component numbers and values for the lower-power PA variation.

A.3   Component Overlay Diagrams

Figure 5 shows the PCB overlay guide with component positions for the main (exciter) PCB. Figure 6 shows the detailed circuit diagram with component numbers and values for the higher-power PA variation. Figure 7 shows the detailed circuit diagram with component numbers and values for the lower power PA variation.

B T50 Parts List

Main PCB Assembly Parts

Ref	Description	Part Number
C100	Four EMI filters in a 1206 package, 100pF	34/NFA3/1100
C101	Four EMI filters in a 1206 package, 100pF	34/NFA3/1100
C102	Four EMI filters in a 1206 package, 100pF	34/NFA3/1100
C103	Four EMI filters in a 1206 package, 100pF	34/NFA3/1100
C201	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C202	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C203	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C204	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C205	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C206	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C207	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C208	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C209	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C210	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C211	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C212	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C214	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C215	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C216	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C217	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C219	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C220	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C221	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C222	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C224	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C225	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C226	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C227	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C300	22uF Electrolytic Capacitor, 35V, Bipolar	41/BP01/022U
C301	22uF Electrolytic Capacitor, 35V, Bipolar	41/BP01/022U
C302	2n2F Cer. Cap, NPO, 1206, 5%	46/26N1/02N2
C304	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C305	10nF Cer. Cap, NPO, 1206, 5%	46/26N1/010N
C306	120pF Cer. Cap, NPO, 0603, 5%	46/63N1/120P
C307	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C308	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C309	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C310	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C311	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C312	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C400	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C401	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C402	3n3F Cer. Cap, NPO, 1206, 5%	46/26N1/03N3
C403	3n3F Cer. Cap, NPO, 1206, 5%	46/26N1/03N3
C404	3n3F Cer. Cap, NPO, 1206, 5%	46/26N1/03N3
C405	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N

Ref	Description	Part Number
C406	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C407	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C408	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C409	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C410	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C411	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C412	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C413	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C414	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C415	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C416	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C417	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C418	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C419	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C422	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C423	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C425	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C426	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C427	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C428	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C500	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C501	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C502	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C503	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C506	100pF Cer. Cap, NPO, 0603, 5%	46/63N1/100P
C507	100pF Cer. Cap, NPO, 0603, 5%	46/63N1/100P
C508	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C509	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C510	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C511	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C513	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C514	Ceramic Capacitor, 16V, 22nF, X7R, 22nF,10%	45/X7R1/022N
C515	100nF, 50V, NPO, TH, 5mm	47/2007/100N
C516	1n2F Cer. Cap, NPO, 1206, 5%	46/26N1/01N2
C600	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C601	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C602	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C603	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C604	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C605	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C606	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C607	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C608	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C609	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C610	470pF Cer. Cap, NPO, 0603, 5%	46/63N1/470P
C611	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C612	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C613	Ceramic Capacitor, 16V, 220nF, X7R, 10%	45/X7R1/220N
C614	15pF Cer. Cap, NPO, 0603, 5%	46/63N1/015P
C615	15pF Cer. Cap, NPO, 0603, 5%	46/63N1/015P
C616	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N

Ref	Description	Part Number
C617	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C619	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C620	33pF Cer. Cap, NPO, 0603, 5%	46/63N1/033P
C621	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C622	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C623	Ceramic Capacitor, 16V, 220nF, X7R, 10%	45/X7R1/220N
C624	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C625	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C626	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C627	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C628	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C629	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C630	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C631	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C634	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C635	8p2F Cer. Cap, NPO, 0603, 5%	46/63N1/08P2
C636	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C637	56pF Cer. Cap, NPO, 0603, 5%	46/63N1/056P
C638	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C639	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C640	8p2F Cer. Cap, NPO, 0603, 5%	46/63N1/08P2
C641	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C642	100pF Cer. Cap, NPO, 0603, 5%	46/63N1/100P
C643	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C644	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C645	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C646	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C648	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C649	10pF Cer. Cap, NPO, 0603, 5%	46/63N1/010P
C650	10pF Cer. Cap, NPO, 0603, 5%	46/63N1/010P
C651	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C652	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C700	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C701	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C702	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C703	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C704	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C705	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C706	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C707	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C708	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C709	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C710	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C711	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C712	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C713	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C714	150pF Cer. Cap, NPO, 0603, 5%	46/63N1/150P
C715	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C716	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C717	3p9F Cer. Cap, NPO, 0603, 5%	46/63N1/03P9
C718	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N

Ref	Description	Part Number
C719	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C720	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C721	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C722	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C723	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C724	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C725	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C726	3p9F Cer. Cap, NPO, 0603, 5%	46/63N1/03P9
C727	15pF Cer. Cap, NPO, 0603, 5%	46/63N1/015P
C728	15pF Cer. Cap, NPO, 0603, 5%	46/63N1/015P
C729	15pF Cer. Cap, NPO, 0603, 5%	46/63N1/015P
C730	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C731	15pF Cer. Cap, NPO, 0603, 5%	46/63N1/015P
C732	5p6F Cer. Cap, NPO, 0603, 5%	46/63N1/05P6
C733	12pF Cer. Cap, NPO, 0603, 5%	46/63N1/012P
C734	3p9F Cer. Cap, NPO, 0603, 5%	46/63N1/03P9
C735	3p9F Cer. Cap, NPO, 0603, 5%	46/63N1/03P9
C736	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C737	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C738	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C739	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C740	47pF Cer. Cap, NPO, 0603, 5%	46/63N1/04P7
C742	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C743	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C745	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C746	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C747	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C748	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C749	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C750	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C751	33pF Cer. Cap, NPO, 0603, 5%	46/63N1/033P
C752	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C753	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C754	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C755	47pF Cer. Cap, NPO, 0603, 5%	46/63N1/047P
C756	10pF Cer. Cap, NPO, 0603, 5%	46/63N1/010P
C757	120pF Cer. Cap, NPO, 0603, 5%	46/63N1/120P
C758	120pF Cer. Cap, NPO, 0603, 5%	46/63N1/120P
C759	47pF Cer. Cap, NPO, 0603, 5%	46/63N1/047P
C760	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C761	22pF Cer. Cap, NPO, 0603, 5%	46/63N1/022P
C762	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C763	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C764	6p8F Cer. Cap, NPO, 0603, 5%	46/63N1/06P8
C765	56pF Cer. Cap, NPO, 0603, 5%	46/63N1/056P
C770	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C771	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C772	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C773	Ceramic Capacitor, 16V, 1uF, Y5V	45/Y5X7/1U16
C774	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C775	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N

Ref	Description	Part Number
C776	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C801	100nF Cer. Cap, X7R, 1206, 10%	46/3310/100N
C802	1n2F Cer. Cap, X7R, 0603, 10%	46/63X1/01N2
C803	47pF Cer. Cap, NPO, 0603, 5%	46/63N1/047P
C804	470pF Cer. Cap, NPO, 0603, 5%	46/63N1/470P
C805	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C806	1n2F Cer. Cap, X7R, 0603, 10%	46/63X1/01N2
C807	1p8F Cer. Cap, NPO, 0603, 5%	46/63N1/01P8
C808	100nF Cer. Cap, X7R, 1206, 10%	46/3310/100N
C810	100uF Electrolytic Capacitor, 35V	41/2001/100U
C811	1p8F Cer. Cap, NPO, 0603, 5%	46/63N1/01P8
C812	100pF Cer. Cap, NPO, 0603, 5%	46/63N1/100P
C813	56pF Cer. Cap, NPO, 0603, 5%	46/63N1/056P
C815	33pF Cer. Cap, NPO, 0603, 5%	46/63N1/033P
C816	10pF Cer. Cap, NPO, 0603, 5%	46/63N1/010P
C818	68pF Cer. Cap, NPO, 0603, 5%	46/63N1/068P
C819	68pF Cer. Cap, NPO, 0603, 5%	46/63N1/068P
C820	470pF Cer. Cap, NPO, 0603, 5%	46/63N1/470P
C821	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C822	10nF Cer. Cap, X7R, 0603, 10%	46/63X1/010N
C823	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C824	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C825	220pF Cer. Cap, NPO, 0603, 5%	46/63N1/220P
C826	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C827	10 uF Electrolytic capacitor	41/2001/010U
C829	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C901	100uF SMD, low ESR Electrolytic cap, D body	41/SELD/100U
C902	470uF Electrolytic Capacitor, Low ESR, 35V	41/200L/470U
C903	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C904	3u3F SMD, Electrolytic cap, A body, 10%	42/STA1/03U3
C915	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C920	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C923	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C924	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C925	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C926	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C927	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C928	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C929	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C930	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C931	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C932	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C933	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C934	100nF, 25V, Y5V, decoupler, 0603	46/63Y1/100N
C935	470uF Electrolytic Capacitor, Low ESR, 35V	41/200L/470U
C936	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C937	100uF SMD, low ESR Electrolytic cap, D body	41/SELD/100U
C938	100uF SMD, low ESR Electrolytic cap, D body	41/SELD/100U
C939	100uF SMD, low ESR Electrolytic cap, D body	41/SELD/100U
C940	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C941	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U

Ref	Description	Part Number
C942	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C943	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C944	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
C945	33uF SMD, low ESR Electrolytic cap, C body	41/SELC/033U
D102	Radially mounted LED	21/1010/LEDR
D103	Radially mounted LED	21/1010/LEDY
D104	Radially mounted LED	21/1010/LEDG
D200	Dual Series Diode	21/3010/AV99
D202	Gen. Purpose 1N4004 diode in SMD pkg	24/SMA1/4004
D203	Zener Diode	21/1040/C3V3
D300	Bi-directional Transil	24/TRSL/012V
D301	Bidirectional Transil	24/TRSL/012V
D302	Bidirectional Transil	24/TRSL/012V
D303	Dual Series Diode	21/3010/AV99
D304	Dual Series Diode	21/3010/AV99
D305	Dual Series Diode	21/3010/AV99
D306	Gen. Purpose 1N4004 diode in SMD pkg	24/SMA1/4004
D307	Dual Schottky, Comm. Cathode, Diode	24/3BAT/54C1
D400	Dual Series Diode	21/3010/AV99
D401	Dual Series Diode	21/3010/AV99
D402	Dual Series Diode	21/3010/AV99
D403	Dual Series Diode	21/3010/AV99
D500	Dual Series Diode	21/3010/AV99
D501	Dual Series Diode	21/3010/AV99
D502	Dual Series Diode	21/3010/AV99
D503	Dual Series Diode	21/3010/AV99
D600	Voltage Controlled Capacitor	21/3060/V109
D601	Voltage Controlled Capacitor	21/3060/V109
D700	Schottky diode	21/3030/0017
D701	Voltage Controlled Capacitor	21/3060/V109
D703	Schottky diode	21/3030/0017
D704	Voltage Controlled Capacitor	21/3060/V109
D800	Dual Schottky, Comm. Cathode, Diode	24/3BAT/54C1
D906	Power Fast Schottky diode	24/BRM1/40T3
D907	Power Fast Schottky diode	24/BRM1/40T3
D908	Power Fast Schottky diode	24/BRM1/40T3
D909	Power Fast Schottky diode	24/BRM1/40T3
D910	Gen. Purpose 1N4004 diode in SMD pkg	24/SMA1/4004
D911	4.096V Reference Diode	29/VREF/0001
F300	SMD (1206 pkg), 125mA fuse	39/1206/A125
F301	SMD (1206 pkg), 125mA fuse	39/1206/A125
F302	SMD (1206 pkg), 125mA fuse	39/1206/A125
J1	BNC Connector	35/5BNC/RA01
JP12	4 Pin SIL Header	35/2501/0004
JP2	14 Pin SIL Header	35/2501/0014
JP3	10 pin DIL Header	35/7026/0010
L100	Ferrite, 1206 pkg, 120 ohm, 3A	37/P034/0001
L101	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L102	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L104	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L200	220uH Choke	37/3320/P103

Ref	Description	Part Number
L202	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L203	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L204	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L205	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L500	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L600	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L700	27nH Inductor	37/8551/027N
L701	39nH Inductor	37/8551/039N
L702	27nH Inductor	37/8551/027N
L703	27nH Inductor	37/8551/027N
L704	47nH Inductor	37/8551/047N
L705	27nH Inductor	37/8551/027N
L706	330nH Inductor	37/3320/330N
L708	330nH Inductor	37/3320/330N
L709	330nH Inductor	37/3320/330N
L710	330nH Inductor	37/3320/330N
L711	330nH Inductor	37/3320/330N
L712	220nH Inductor	37/8551/220N
L713	220uH Choke	37/3320/P103
L714	330nH Inductor	37/3320/330N
L715	330nH Inductor	37/3320/330N
L716	Inductor - Air Core, 12.5nH	37/AC51/12N5
L717	100nH Inductor	37/8551/100N
L718	220uH Choke	37/3320/P103
L719	Inductor - Air Core, 18.5nH	37/AC51/18N5
L720	220nH Inductor	37/8551/220N
L721	270nH Inductor	37/85T1/270N
L722	220nH Inductor	37/8551/220N
L723	330nH Inductor	37/3320/330N
L724	330nH Inductor	37/3320/330N
L725	3u3H Choke	37/3320/P101
L726	82nH Inductor	37/8551/082N
L800	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L801	Ferrite, 1206 pkg, 600 ohm, 200mA	37/P033/0001
L803	Inductor - Air Core, 538nH	37/AC52/558N
L804	Inductor - Air Core, 538nH	37/AC52/558N
L805	Inductor - Air Core, 120nH	37/AC52/120N
L806	Inductor - Air Core, 169nH	37/AC52/169N
L807	220uH Choke	37/3320/P103
L808	3u3H Choke	37/3320/P101
L809	180nH Inductor	37/8551/180N
L810	1uH Choke	37/3320/P200
L811	3u3H Choke	37/3320/P101
L901	33uH Choke	37/3320/P102
L902	SMD High Current, Shielded, 220uH Choke	37/MSP1/220U
L903	SMD High Current, Shielded, 330uH Choke	37/MSP1/330U
L904	SMD High Current, Shielded, 220uH Choke	37/MSP1/220U
L905	220uH Choke	37/3320/P103
L906	Ferrite, 1206 pkg, 120 ohm, 3A	37/P034/0001
L907	Ferrite, 1206 pkg, 120 ohm, 3A	37/P034/0001
L908	Ferrite, 1206 pkg, 120 ohm, 3A	37/P034/0001

Ref	Description	Part Number
L909	Ferrite, 1206 pkg, 120 ohm, 3A	37/P034/0001
M1	Tinned BeCu, used as RF screen.	94/BECU/24XH
M1C	RF Screen Cover (Small)	80/9209/0001
M2	Conductive Foam Inserts	83/0001/0000
MX700	+7dBm0 Mixer, Surface Mount	37/MIXR/P028
P1	DB9 Female with filtered pins	35/5012/009F
P3	DB25 Female with filtered pins	35/5012/025F
Q200	Gen. Purpose NPN transistor in SOT-23	27/3020/3904
Q201	N channel, Enhancement Mode MOSFET	27/30B5/5138
Q202	N Channel Junction FET(low Freq)	27/3020/5484
Q203	NPN Switching transistor in SOT-23	27/3020/2369
Q204	NPN Switching transistor in SOT-23	27/3020/2369
Q205	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q206	Gen. Purpose NPN transistor in SOT-23	27/3020/3904
Q300	N channel, Enhancement Mode MOSFET	27/30B5/5138
Q301	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q302	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q400	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q401	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q402	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q500	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q501	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q600	Gen. Purpose NPN transistor in SOT-23	27/3020/3904
Q700	Gen. Purpose PNP transistor in SOT-23	27/3010/3906
Q701	N channel, Enhancement Mode MOSFET	27/30B5/5138
Q702	Gen. Purpose NPN transistor in SOT-23	27/3020/3904
Q703	N channel, Enhancement Mode MOSFET	27/30B5/5138
Q704	N Channel Junction FET(UHF)	27/3030/J309
Q705	N Channel Junction FET(UHF)	27/3030/J309
Q706	N channel, Enhancement Mode MOSFET	27/30B5/5138
Q707	Gen. Purpose NPN transistor in SOT-23	27/3020/3904
Q801	SOD-89A RF Transistor(1W)	27/300B/FQ17
Q804	SOD-89A RF Transistor(1W)	27/300B/FQ17
Q805	SOD-89A RF Transistor(1W)	27/300B/FQ17
R100	0805, 1%, 4K7 resistor	51/8511/04K7
R101	0805, 1%, 4K7 resistor	51/8511/04K7
R102	0805, 1%, 4K7 resistor	51/8511/04K7
R103	1206 180R resistor	51/3380/0180
R104	1206 270R resistor	51/3380/0270
R105	0805, 1%, 4K7 resistor	51/8511/04K7
R201	0805, 1%, 1K resistor	51/8511/010K
R202	0805, 1%, 1K resistor	51/8511/010K
R203	0805, 1%, 1K resistor	51/8511/010K
R204	0805, 1%, 1K resistor	51/8511/010K
R205	0805, 1%, 2K2 resistor	51/8511/02K2
R206	0805, 1%, 2K2 resistor	51/8511/02K2
R207	0805, 1%, 68K resistor	51/8511/068K
R208	0805, 1%, 22K resistor	51/8511/022K
R209	0805, 1%, 330R resistor	51/8511/330R
R210	0805, 1%, 1K resistor	51/8511/010K
R211	0805, 1%, 220R resistor	51/8511/220R

Ref	Description	Part Number
R212	0805, 1%, 220R resistor	51/8511/220R
R213	0805, 1%, 1M resistor	51/8511/01M0
R214	1206 180R resistor	51/3380/0180
R215	0805, 1%, 120R resistor	51/8511/120R
R216	0805, 1%, 1K resistor	51/8511/01K0
R217	0805, 1%, 1K resistor	51/8511/010K
R218	0805, 1%, 1K resistor	51/8511/010K
R219	0805, 1%, 1K resistor	51/8511/010K
R220	0805, 1%, 1K resistor	51/8511/010K
R221	0805, 1%, 560R resistor	51/8511/560R
R222	0805, 1%, 1K resistor	51/8511/01K0
R223	0805, 1%, 1K resistor	51/8511/010K
R224	0805, 1%, 1K resistor	51/8511/010K
R225	0805, 1%, 1K resistor	51/8511/010K
R226	1206 180R resistor	51/3380/0180
R227	0805, 1%, 56R resistor	51/8511/056R
R228	0805, 1%, 1K resistor	51/8511/010K
R229	0805, 1%, 1K resistor	51/8511/010K
R230	0805, 1%, 120R resistor	51/8511/120R
R231	0805, 1%, 120R resistor	51/8511/120R
R232	0805, 1%, 560R resistor	51/8511/560R
R233	0805, 1%, 22K resistor	51/8511/022K
R234	0805, 1%, 1K resistor	51/8511/01K0
R235	0805, 1%, 4K7 resistor	51/8511/04K7
R236	0805, 1%, 22K resistor	51/8511/022K
R237	0805, 1%, 47K resistor	51/8511/047K
R238	0805, 1%, 1K resistor	51/8511/01K0
R239	0805, 1%, 1K resistor	51/8511/01K0
R240	0805, 1%, 1K resistor	51/8511/010K
R241	0805, 1%, 47R resistor	51/8511/047R
R242	0805, 1%, 47K resistor	51/8511/047K
R243	0805, 1%, 220R resistor	51/8511/220R
R244	0805, 1%, 10R resistor	51/8511/010R
R245	0805, 1%, 1K resistor	51/8511/010K
R300	0805, 1%, 27R resistor	51/8511/027R
R301	0805, 1%, 27R resistor	51/8511/027R
R302	0805, 1%, 27R resistor	51/8511/027R
R303	0805, 1%, 27R resistor	51/8511/027R
R304	0805, 1%, 330R resistor	51/8511/330R
R305	0805, 1%, 330R resistor	51/8511/330R
R306	0805, 1%, 10R resistor	51/8511/010R
R307	0805, 1%, 4K7 resistor	51/8511/04K7
R308	0805, 1%, 2K2 resistor	51/8511/02K2
R309	0805, 1%, 560R resistor	51/8511/560R
R310	0805, 1%, 560R resistor	51/8511/560R
R311	0805, 1%, 22K resistor	51/8511/022K
R312	0805, 1%, 22K resistor	51/8511/022K
R313	0805, 1%, 22K resistor	51/8511/022K
R314	0805, 1%, 1K resistor	51/8511/010K
R315	0805, 1%, 22K resistor	51/8511/022K
R316	0805, 1%, 1K resistor	51/8511/010K

Ref	Description	Part Number
R317	0805, 1%, 1K resistor	51/8511/01K0
R318	0805, 1%, 120K resistor	51/8511/120K
R319	0805, 1%, 120K resistor	51/8511/120K
R320	0805, 1%, 120K resistor	51/8511/120K
R321	0805, 1%, 68K resistor	51/8511/068K
R322	0805, 1%, 68K resistor	51/8511/068K
R323	0805, 1%, 68K resistor	51/8511/068K
R324	0805, 1%, 1K resistor	51/8511/01K0
R325	0805, 1%, 47K resistor	51/8511/047K
R326	0805, 1%, 47K resistor	51/8511/047K
R327	0805, 1%, 47K resistor	51/8511/047K
R328	0805, 1%, 1K resistor	51/8511/010K
R329	0805, 1%, 1K resistor	51/8511/010K
R330	0805, 1%, 47K resistor	51/8511/047K
R331	0805, 1%, 47K resistor	51/8511/047K
R332	0805, 1%, 68K resistor	51/8511/068K
R333	0805, 1%, 1K resistor	51/8511/01K0
R335	0805, 1%, 22K resistor	51/8511/022K
R336	0805, 1%, 22K resistor	51/8511/022K
R400	0805, 1%, 330R resistor	51/8511/330R
R401	0805, 1%, 270R resistor	51/8511/270R
R402	0805, 1%, 22K resistor	51/8511/022K
R403	0805, 1%, 22K resistor	51/8511/022K
R404	0805, 1%, 56K resistor	51/8511/056K
R405	0805, 1%, 5K6 resistor	51/8511/05K6
R406	0805, 1%, 1K resistor	51/8511/010K
R407	0805, 1%, 1K resistor	51/8511/010K
R408	0805, 1%, 5K6 resistor	51/8511/05K6
R409	0805, 1%, 120K resistor	51/8511/120K
R410	0805, 1%, 47K resistor	51/8511/047K
R411	0805, 1%, 47K resistor	51/8511/047K
R412	0805, 1%, 1K resistor	51/8511/010K
R413	0805, 1%, 1K resistor	51/8511/01K0
R414	0805, 1%, 560R resistor	51/8511/560R
R415	0805, 1%, 560R resistor	51/8511/560R
R416	0805, 1%, 560R resistor	51/8511/560R
R417	0805, 1%, 560R resistor	51/8511/560R
R418	0805, 1%, 5K6 resistor	51/8511/05K6
R419	0805, 1%, 22K resistor	51/8511/022K
R420	0805, 1%, 120K resistor	51/8511/120K
R421	0805, 1%, 22K resistor	51/8511/022K
R422	0805, 1%, 120K resistor	51/8511/120K
R423	0805, 1%, 1K resistor	51/8511/010K
R424	0805, 1%, 1K resistor	51/8511/010K
R425	0805, 1%, 22K resistor	51/8511/022K
R426	0805, 1%, 22K resistor	51/8511/022K
R427	0805, 1%, 47K resistor	51/8511/047K
R428	0805, 1%, 22K resistor	51/8511/022K
R429	0805, 1%, 22K resistor	51/8511/022K
R430	0805, 1%, 47K resistor	51/8511/047K
R431	0805, 1%, 270K resistor	51/8511/270K

Ref	Description	Part Number
R432	0805, 1%, 270K resistor	51/8511/270K
R433	0805, 1%, 270K resistor	51/8511/270K
R434	0805, 1%, 4K7 resistor	51/8511/04K7
R435	0805, 1%, 1K resistor	51/8511/01K0
R436	0805, 1%, 4K7 resistor	51/8511/04K7
R437	0805, 1%, 47K resistor	51/8511/047K
R438	0805, 1%, 47K resistor	51/8511/047K
R439	0805, 1%, 4K7 resistor	51/8511/04K7
R440	0805, 1%, 4K7 resistor	51/8511/04K7
R442	0805, 1%, 4K7 resistor	51/8511/04K7
R443	0805, 1%, 4K7 resistor	51/8511/04K7
R444	0805, 1%, 4K7 resistor	51/8511/04K7
R445	0805, 1%, 47K resistor	51/8511/047K
R446	0805, 1%, 1K resistor	51/8511/010K
R447	0805, 1%, 47K resistor	51/8511/047K
R448	0805, 1%, 1K resistor	51/8511/010K
R449	0805, 1%, 5K6 resistor	51/8511/05K6
R450	0805, 1%, 120K resistor	51/8511/120K
R451	0805, 1%, 47K resistor	51/8511/047K
R452	0805, 1%, 1K resistor	51/8511/010K
R453	0805, 1%, 1K resistor	51/8511/010K
R454	0805, 1%, 1K resistor	51/8511/010K
R455	0805, 1%, 1K resistor	51/8511/010K
R456	0805, 1%, 47K resistor	51/8511/047K
R457	0805, 1%, 1K resistor	51/8511/010K
R458	0805, 1%, 4K7 resistor	51/8511/04K7
R459	0805, 1%, 4K7 resistor	51/8511/04K7
R460	0805, 1%, 4K7 resistor	51/8511/04K7
R461	0805, 1%, 120K resistor	51/8511/120K
R462	0805, 1%, 1K resistor	51/8511/010K
R463	0805, 1%, 120K resistor	51/8511/120K
R464	0805, 1%, 270K resistor	51/8511/270K
R465	0805, 1%, 100K resistor	51/8511/100K
R466	0805, 1%, 2K2 resistor	51/8511/02K2
R467	0805, 1%, 4K7 resistor	51/8511/04K7
R500	0805, 1%, 47K resistor	51/8511/047K
R501	0805, 1%, 47K resistor	51/8511/047K
R502	0805, 1%, 47K resistor	51/8511/047K
R503	0805, 1%, 22K resistor	51/8511/022K
R504	0805, 1%, 560R resistor	51/8511/560R
R505	0805, 1%, 1K resistor	51/8511/010K
R506	0805, 1%, 1K resistor	51/8511/010K
R507	0805, 1%, 1M resistor	51/8511/01M0
R508	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R509	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R510	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R511	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R512	0805, 1%, 1K resistor	51/8511/010K
R513	0805, 1%, 1K resistor	51/8511/010K
R514	0805, 1%, 1K resistor	51/8511/010K
R516	0805, 1%, 680R resistor	51/8511/680R

Ref	Description	Part Number
R517	0805, 1%, 47K resistor	51/8511/047K
R518	0805, 1%, 47K resistor	51/8511/047K
R519	0805, 1%, 47K resistor	51/8511/047K
R520	0805, 1%, 47K resistor	51/8511/047K
R521	0805, 1%, 47K resistor	51/8511/047K
R522	0805, 1%, 68K resistor	51/8511/068K
R523	0805, 1%, 1K resistor	51/8511/01K0
R525	0805, 1%, 1K resistor	51/8511/010K
R526	0805, 1%, 2K2 resistor	51/8511/02K2
R527	0805, 1%, 47K resistor	51/8511/047K
R528	0805, 1%, 47K resistor	51/8511/047K
R529	0805, 1%, 47K resistor	51/8511/047K
R530	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R531	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R532	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R533	0805, 0.5%, 50ppm, 7K5 resistor	51/85P1/07K5
R600	0805, 1%, 4K7 resistor	51/8511/04K7
R602	0805, 1%, 27K resistor	51/8511/027K
R603	0805, 1%, 27K resistor	51/8511/027K
R604	0805, 1%, 100K resistor	51/8511/100K
R605	0805, 1%, 27K resistor	51/8511/027K
R606	0805, 1%, 5K6 resistor	51/8511/05K6
R607	0805, 1%, 5K6 resistor	51/8511/05K6
R608	0805, 1%, 2K2 resistor	51/8511/02K2
R609	0805, 1%, 1K resistor	51/8511/010K
R610	0805, 1%, 47K resistor	51/8511/047K
R611	0805, 1%, 2K2 resistor	51/8511/02K2
R612	0805, 1%, 100K resistor	51/8511/100K
R613	0805, 1%, 47R resistor	51/8511/047R
R614	0805, 1%, 47R resistor	51/8511/047R
R615	0805, 1%, 47R resistor	51/8511/047R
R616	0805, 1%, 47R resistor	51/8511/047R
R617	0805, 1%, 1K resistor	51/8511/01K0
R618	0805, 1%, 1K resistor	51/8511/01K0
R619	0805, 1%, 680R resistor	51/8511/680R
R620	0805, 1%, 680R resistor	51/8511/680R
R621	0805, 1%, 4K7 resistor	51/8511/04K7
R622	0805, 1%, 5K6 resistor	51/8511/05K6
R623	0805, 1%, 5K6 resistor	51/8511/05K6
R624	0805, 1%, 22K resistor	51/8511/022K
R625	0805, 1%, 22K resistor	51/8511/022K
R628	1218 1W 68R resistor	51/8251/068R
R629	0805, 1%, 270K resistor	51/8511/270K
R630	0805, 1%, 120R resistor	51/8511/120R
R631	0805, 1%, 47R resistor	51/8511/047R
R632	0805, 1%, 47R resistor	51/8511/047R
R633	1206 120R resistor	51/3380/0120
R634	0805, 1%, 120R resistor	51/8511/120R
R635	0805, 1%, 560R resistor	51/8511/560R
R636	0805, 1%, 220R resistor	51/8511/220R
R637	0805, 1%, 5K6 resistor	51/8511/05K6

Ref	Description	Part Number
R638	0805, 1%, 5K6 resistor	51/8511/05K6
R639	0805, 1%, 1K resistor	51/8511/010K
R646	0805, 1%, 4K7 resistor	51/8511/04K7
R647	0805, 1%, 1K resistor	51/8511/010K
R648	0805, 1%, 4K7 resistor	51/8511/04K7
R649	0805, 1%, 1K resistor	51/8511/010K
R650	0805, 1%, 5K6 resistor	51/8511/05K6
R700	0805, 1%, 120R resistor	51/8511/120R
R701	0805, 1%, 47R resistor	51/8511/047R
R702	0805, 1%, 120R resistor	51/8511/120R
R703	0805, 1%, 120R resistor	51/8511/120R
R704	0805, 1%, 120R resistor	51/8511/120R
R705	0805, 1%, 220R resistor	51/8511/220R
R706	0805, 1%, 220R resistor	51/8511/220R
R707	0805, 1%, 220R resistor	51/8511/220R
R708	0805, 1%, 4K7 resistor	51/8511/04K7
R709	0805, 1%, 1K resistor	51/8511/010K
R710	0805, 1%, 2K2 resistor	51/8511/02K2
R711	0805, 1%, 100K resistor	51/8511/100K
R713	0805, 1%, 100K resistor	51/8511/100K
R714	0805, 1%, 56R resistor	51/8511/056R
R715	0805, 1%, 1K resistor	51/8511/010K
R716	0805, 1%, 47R resistor	51/8511/047R
R717	0805, 1%, 1K resistor	51/8511/010K
R718	0805, 1%, 120R resistor	51/8511/120R
R719	0805, 1%, 1K resistor	51/8511/010K
R720	0805, 1%, 100K resistor	51/8511/100K
R722	0805, 1%, 22K resistor	51/8511/022K
R723	0805, 1%, 1K resistor	51/8511/010K
R724	0805, 1%, 56R resistor	51/8511/056R
R725	0805, 1%, 22K resistor	51/8511/022K
R726	0805, 1%, 47R resistor	51/8511/047R
R727	0805, 1%, 22K resistor	51/8511/022K
R729	0805, 1%, 10R resistor	51/8511/010R
R730	0805, 1%, 220R resistor	51/8511/220R
R731	0805, 1%, 560R resistor	51/8511/560R
R732	0805, 1%, 22K resistor	51/8511/022K
R733	0805, 1%, 330R resistor	51/8511/330R
R734	0805, 1%, 4K7 resistor	51/8511/04K7
R735	0805, 1%, 22K resistor	51/8511/022K
R736	0805, 1%, 1K resistor	51/8511/01K0
R737	0805, 1%, 1K resistor	51/8511/01K0
R738	0805, 1%, 220R resistor	51/8511/220R
R739	0805, 1%, 1K resistor	51/8511/010K
R740	0805, 1%, 120R resistor	51/8511/120R
R741	0805, 1%, 4K7 resistor	51/8511/04K7
R742	0805, 1%, 820R resistor	51/8511/820R
R743	0805, 1%, 560R resistor	51/8511/560R
R744	0805, 1%, 1K resistor	51/8511/010K
R745	0805, 1%, 220R resistor	51/8511/220R
R802	0805, 1%, 47R resistor	51/8511/047R

Ref	Description	Part Number
R803	0805, 1%, 100R resistor	51/8251/100R
R804	1206 10R resistor	51/3380/0010
R805	1206 10R resistor	51/3380/0010
R806	0805, 1%, 100R resistor	51/8251/100R
R807	0805, 1%, 100R resistor	51/8251/100R
R808	0805, 1%, 10R resistor	51/8511/010R
R809	0805, 1%, 27R resistor	51/8511/027R
R810	0805, 1%, 10R resistor	51/8511/010R
R811	0805, 1%, 27R resistor	51/8511/027R
R812	0805, 1%, 220R resistor	51/8511/220R
R813	0805, 1%, 100R resistor	51/8251/100R
R816	0805, 1%, 1K resistor	51/8511/010K
R819	7W Axial 68R resistor	55/5W51/068R
R823	0805, 1%, 4K7 resistor	51/8511/04K7
R918	0805, 1%, 47K resistor	51/8511/047K
R919	0805, 1%, 47K resistor	51/8511/047K
R920	0805, 1%, 1K resistor	51/8511/01K0
R921	0805, 1%, 560R resistor	51/8511/560R
R922	0805, 1%, 220R resistor	51/8511/220R
R923	0805, 1%, 1K resistor	51/8511/01K0
R924	0805, 1%, 560R resistor	51/8511/560R
R925	0805, 1%, 220R resistor	51/8511/220R
R926	0805, 1%, 2K2 resistor	51/8511/02K2
R927	0805, 1%, 220R resistor	51/8511/220R
R928	0805, 1%, 220R resistor	51/8511/220R
R929	0805, 1%, 220R resistor	51/8511/220R
R930	0805, 1%, 220R resistor	51/8511/220R
R931	0805, 1%, 220R resistor	51/8511/220R
R932	0805, 1%, 220R resistor	51/8511/220R
R933	0805, 1%, 560R resistor	51/8511/560R
R934	0805, 1%, 560R resistor	51/8511/560R
R935	0805, 1%, 120R resistor	51/8511/120R
R936	0805, 1%, 120R resistor	51/8511/120R
RL300	12V Telecommunications DPDT Relay	96/2000/012V
RV100	100K, 11 turn, linear Pot.	53/THH1/100K
S200	4mm SMD PB switch	31/SMPB/0001
SW1	C&K PB Switch	31/0005/E121
T300	High Isolation Audio Transformer	37/2040/5065
T301	High Isolation Audio Transformer	37/2040/5065
TP102	Test Point	35/2501/0001
TP300	Test Point	35/2501/0001
TP301	Test Point	35/2501/0001
TP302	Test Point	35/2501/0001
TP303	Test Point	35/2501/0001
TP305	Test Point	35/2501/0001
TP500	Test Point	35/2501/0001
TP501	Test Point	35/2501/0001
TP908	Test Point	35/2501/0001
TP909	Test Point	35/2501/0001
TP910	Test Point	35/2501/0001
TP911	Test Point	35/2501/0001

Ref	Description	Part Number
TP912	Test Point	35/2501/0001
TP913	Test Point	35/2501/0001
TP914	Test Point	35/2501/0001
TP915	Test Point	35/2501/0001
TP916	Test Point	35/2501/0001
TP917	Test Point	35/2501/0001
U201	Quad CMOS RS232 Driver SMD (SO-14)	29/14C8/9A01
U202	Quad CMOS RS232 Driver SMD (SO-14)	29/14C8/8001
U203	Under-voltage sensor and Reset Generator	29/MC33/064D
U204	Motorola Embedded 8/16 bit microcontroller	29/68HC/12A0
U205	One of 8 Selector	29/2030/C138
U207	4 Megabyte TSOP (Std.) 5V (only) Flash	29/P006/0001
U208	1,2,4 Megabit RAM in SOP package	29/SRAM/P013
U209	Octal Latch	29/2030/C374
U212	Hi Speed, TTL compatible, opto-isolator	26/N137/0001
U300	Opto-isolator with Darlington Output	25/1010/4N35
U301	Quad SPST Analog Switch - low Rds On	29/00DG/411C
U302	Low Power Quad Operational Amplifier	29/000L/M224
U303	32 position digital pot.	29/MAX5/161L
U400	Low Power Quad Operational Amplifier	29/000L/M224
U401	8-bit Shift reg. with output latch	29/2030/C595
U402	Transconductance Amplifier	29/0LM1/3700
U403	Quad SPST Analog Switch - low Rds On	29/00DG/411C
U404	Quad SPST Analog Switch - low Rds On	29/00DG/411C
U405	Low Power Quad Operational Amplifier	29/000L/M224
U406	Voltage Output, Quad 8 bit DAC	29/00MA/X534
U407	Low Power Quad Operational Amplifier	29/000L/M224
U500	CTCSS and DCS encoder/decoder	29/00FX/805L
U502	Low Power Quad Operational Amplifier	29/000L/M224
U503	32 position digital pot.	29/MAX5/161L
U600	Gen. Purp. R2R Op. Amp.	29/1M55/P021
U601	Voltage Output, Quad 8 bit DAC	29/00MA/X534
U602	Dual PLL	29/LMX2/335L
U603	Temperature Sensor	29/0001/LM61
U604	Dual PLL	29/LMX2/335L
U605	Dual, Ripple Carry, 4 bit binary counter	29/2030/C393
U606	Dual 4 bit, ripple carry, decade counters	29/2030/C390
U607	Gen. Purp. R2R Op. Amp.	29/1M55/P021
U608	Gen. Purp. R2R Op. Amp.	29/1M55/P021
U700	MMIC Amplifier	24/3010/VAM6
U701	MMIC Amplifier	24/3010/211L
U702	MMIC Amplifier	24/3010/VAM6
U703	MMIC Amplifier	24/3010/VAM6
U704	Transconductance Amplifier	29/0LM1/3700
U705	MMIC Amplifier	24/3010/VAM6
U706	MMIC Amplifier	24/3010/VAM6
U707	Gen. Purp. R2R Op. Amp.	29/1M55/P021
U800	MMIC Amplifier	24/3010/211L
U906	Gen. Purp. R2R Op. Amp.	29/1M55/P021
U907	Simple (Buck) Switcher, 5V, 1A output	29/REG1/0N12
U908	Simple (Buck) Switcher, 5V, 1A output	29/REG1/0N12

Ref	Description	Part Number
U909	Simple (Buck) Switcher, 5V, 1A output	29/REG2/00N5
U910	LDO Adjustable Positive Voltage Regulator (800mA)	29/00LM/1117
U911	Positive Adjustable Voltage Reg. in SO8 package	29/000L/M317
U912	Positive Adjustable Voltage Reg. in SO8 package	29/000L/M317
U913	Positive Adjustable Voltage Reg. in SO8 package	29/000L/M337
U914	Positive Adjustable Voltage Reg. in SO8 package	29/000L/M337
U915	Positive Adjustable Voltage Reg. in SO8 package	29/000L/M337
X200	14.7456 MHz Crystal, 30ppm, SMD	33/14M7/0001
X500	4.0 MHz Crystal	32/2049/04M0
X600	12.0 MHz Crystal, 5ppm, SMD	33/12M0/0001
X601	12.0 MHz Crystal, 5ppm, SMD	33/12M0/0001

C – EIA CTCSS TONES

Frequency	EIA Number
No Tone	
67.0	A1
71.9	B1
74.4	C1
77.0	A2
79.7	C2
82.5	B2
85.4	C3
88.5	A3
91.5	C4
94.8	B3
100.0	A4
103.5	B4
107.2	A5
110.9	B5
114.8	A6
118.8	B6
123.0	A7
127.3	B7
131.8	A8
136.5	B8
141.3	A9
146.2	B9
151.4	A10
156.7	B10
162.2	A11
167.9	B11
173.8	A12
179.9	B12
186.2	A13
192.8	B13
203.5	A14
210.7	B14
218.1	A15
225.7	B15
233.6	A16
241.8	B16
250.3	A17