CC3200MOD SimpleLink™ Wi-Fi® and Internet-of-Things Module Solution, a Single-Chip Wireless MCU

1 Module Overview

1.1 Features

- The CC3200MOD is a Wi-Fi Module that Consists of the CC3200R1M2RGC Single-Chip Wireless MCU. This Fully Integrated Module Includes all Required Clocks, SPI Flash, and Passives.
- Modular FCC, IC, and CE Certifications Save Customer Effort, Time, and Money
- Wi-Fi CERTIFIED™ Modules, With Ability to Request Certificate Transfer for Wi-Fi Alliance Members
- 1.27-mm Pitch LGA Package for Easy Assembly and Low-Cost PCB Design

- Applications Microcontroller Subsystem
  – ARM Cortex-M4 Core at 80 MHz
  – Embedded Memory Options
    - Integrated Serial
    - RAM (up to 256KB)
    - Peripheral Drivers in ROM
  – Hardware Crypto Engine for Advanced Hardware Security Including
    - AES, DES, and 3DES
    - SHA and MD5
    - CRC and Checksum
  – 8-Bit, Fast, Parallel Camera Interface
  – 1 Multichannel Audio Serial Port (McASP) Interface With Support for I2S Format
  – 1 SD (MMC) Interface
  – 32-Channel Micro Direct Memory Access (µDMA)
  – 2 Universal Asynchronous Receivers/Transmitters (UARTs)
  – 2 Serial Peripheral Interfaces (SPIs)
  – 1 Inter-integrated Circuit (I^2C)
  – 4 General-Purpose Timers (GPTs)
  – 16-Bit Pulse-Width Modulation (PWM) Mode
  – 1 Watchdog Timer Module
  – 4-Channel 12-Bit Analog-to-Digital Converters (ADCs)
  – Up to 25 Individually Programmable GPIO Pins
- Wi-Fi Network Processor Subsystem
  – 802.11b/g/n Radio, Baseband, and Medium Access Control
  – TCP/IP Stack
    - 8 Simultaneous TCP, UDP, or RAW Sockets
    - 2 Simultaneous TLS v1.2 or SSL 3.0 Sockets
  – Powerful Crypto Engine for Fast, Secured WLAN Connections With 256-Bit Encryption
  – Station, Access Point, and Wi-Fi Direct™ Modes
  – WPA2 Personal and Enterprise Security
  – SimpleLink Connection Manager for Managing Wi-Fi Security States
  – TX Power
    - 17 dBm at 1 DSSS
    - 17.25 dBm at 11 CCK
    - 13.5 dBm at 54 OFDM
  – RX Sensitivity
    - –94.7 dBm at 1 DSSS
    - –87 dBm at 11 CCK
    - –73 dBm at 54 OFDM
  – Application Throughput
    - UDP: 16 Mbps
    - TCP: 13 Mbps
- Power-Management Subsystem
  – Integrated DC-DC Converter With a Wide-Supply Voltage:
    - VBAT: 2.3 to 3.6 V
  – Low-Power Consumption at 3.6 V
    - Hibernate With Real-Time Clock (RTC): 7 µA
    - Low-Power Deep Sleep: <275 µA
    - RX Traffic: 59 mA at 54 OFDM
    - TX Traffic: 229 mA at 54 OFDM
  – Additional Integrated Components
    - 40.0-MHz Crystal
    - 32.768-kHz Crystal (RTC)
    - 8-Mbit SPI Serial Flash RF Filter and Passive Components
  – Package and Operating Conditions
    - 1.27-mm Pitch, 63-Pin, 20.5-mm × 17.5 mm LGA Package for Easy Assembly and Low-Cost PCB Design
    - Operating Temperature Range: –20°C to 70°C

1.2 Applications

- Internet of Things (IoT)
- Cloud Connectivity
- Home Automation
- Home Appliances
- Access Control
- Security Systems
- Smart Energy
- Internet Gateway
- Industrial Control
- Smart Plug and Metering
- Wireless Audio
- IP Network Sensor Nodes
- Wearables

1.3 Description

Start your design with the industry's first programmable FCC, IC, CE, and Wi-Fi Certified Wireless microcontroller (MCU) module with built-in Wi-Fi connectivity. Created for the Internet of Things (IoT), the SimpleLink CC3200MOD is a wireless MCU module that integrates an ARM Cortex-M4 MCU, allowing customers to develop an entire application with a single device. With on-chip Wi-Fi, Internet, and robust security protocols, no prior Wi-Fi experience is required for faster development. The CC3200MOD integrates all required system-level hardware components including clocks, SPI flash, RF switch, and passives into an LGA package for easy assembly and low-cost PCB design. The CC3200MOD is provided as a complete platform solution including software, sample applications, tools, user and programming guides, reference designs, and the TI E2E™ support community

The applications MCU subsystem contains an industry-standard ARM Cortex-M4 core running at 80 MHz.

The device includes a wide variety of peripherals, including a fast parallel camera interface, I2S, SD/MMC, UART, SPI, I2C, and four-channel ADC. The CC3200 family includes flexible embedded RAM for code and data; ROM with external serial flash bootloader and peripheral drivers; and SPI flash for Wi-Fi network processor service packs, Wi-Fi certificates, and credentials.

The Wi-Fi network processor subsystem features a Wi-Fi Internet-on-a-chip™ and contains an additional dedicated ARM MCU that completely off-loads the applications MCU. This subsystem includes an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3200MOD supports station, access point, and Wi-Fi Direct™ modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi Internet-on-a-chip includes embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols. The power-management subsystem includes integrated DC-DC converters supporting a wide range of supply voltages. This subsystem enables low-power consumption modes, such as the hibernate with RTC mode requiring less than 7 µA of current.

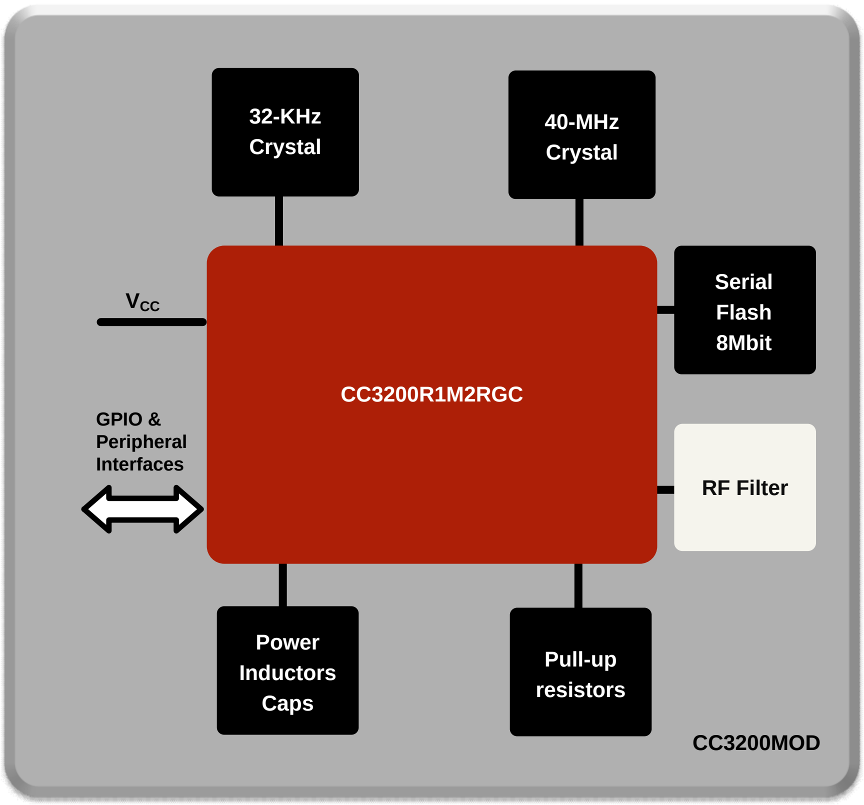
Table 1-1. Module Information(1)

PART NUMBER	PACKAGE	BODY SIZE
CC3200MODR1M2AMOB	MOB (63)	20.5 mm × 17.5 mm

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the CC3200MOD module.



(1) For 3200MOD module pin multiplexing details, refer to CC3200R device datasheet (literature number: SWAS032)

Figure 1-1. CC3200MOD Module Functional Block Diagram

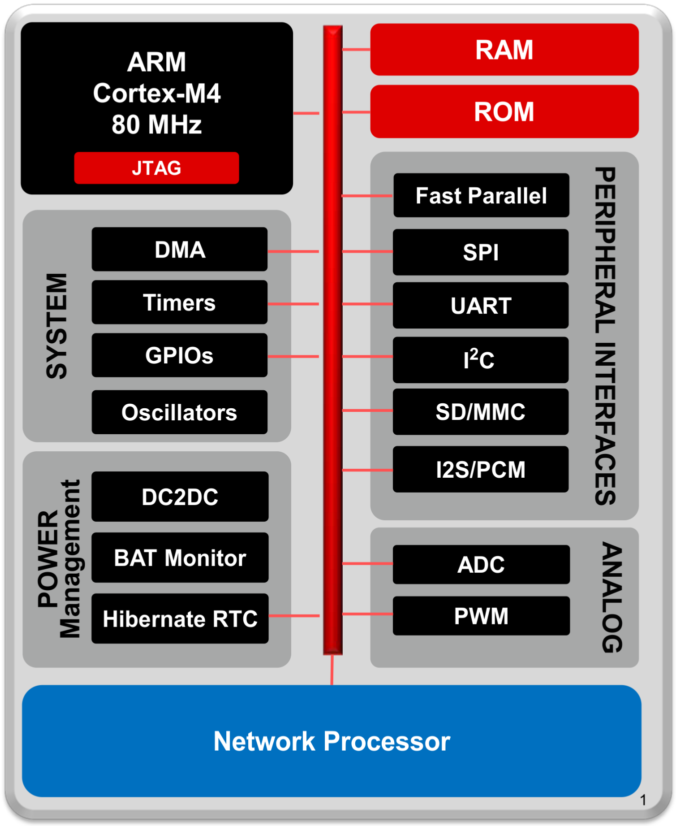


Figure 1-2. CC3200 Hardware Overview

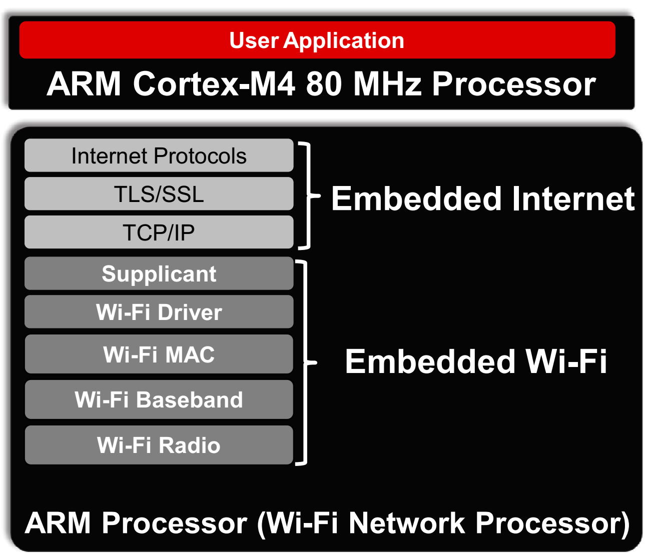


Figure 1-3. CC3200 Software Overview

Table of Contents

2 Revision History

DATE	REVISION	NOTES
November 2014	*	Initial release.

3 Terminal Configuration and Functions

3.1 CC3200MOD Pin Diagram

Figure 3-1 shows the pin diagram for the CC3200MOD.

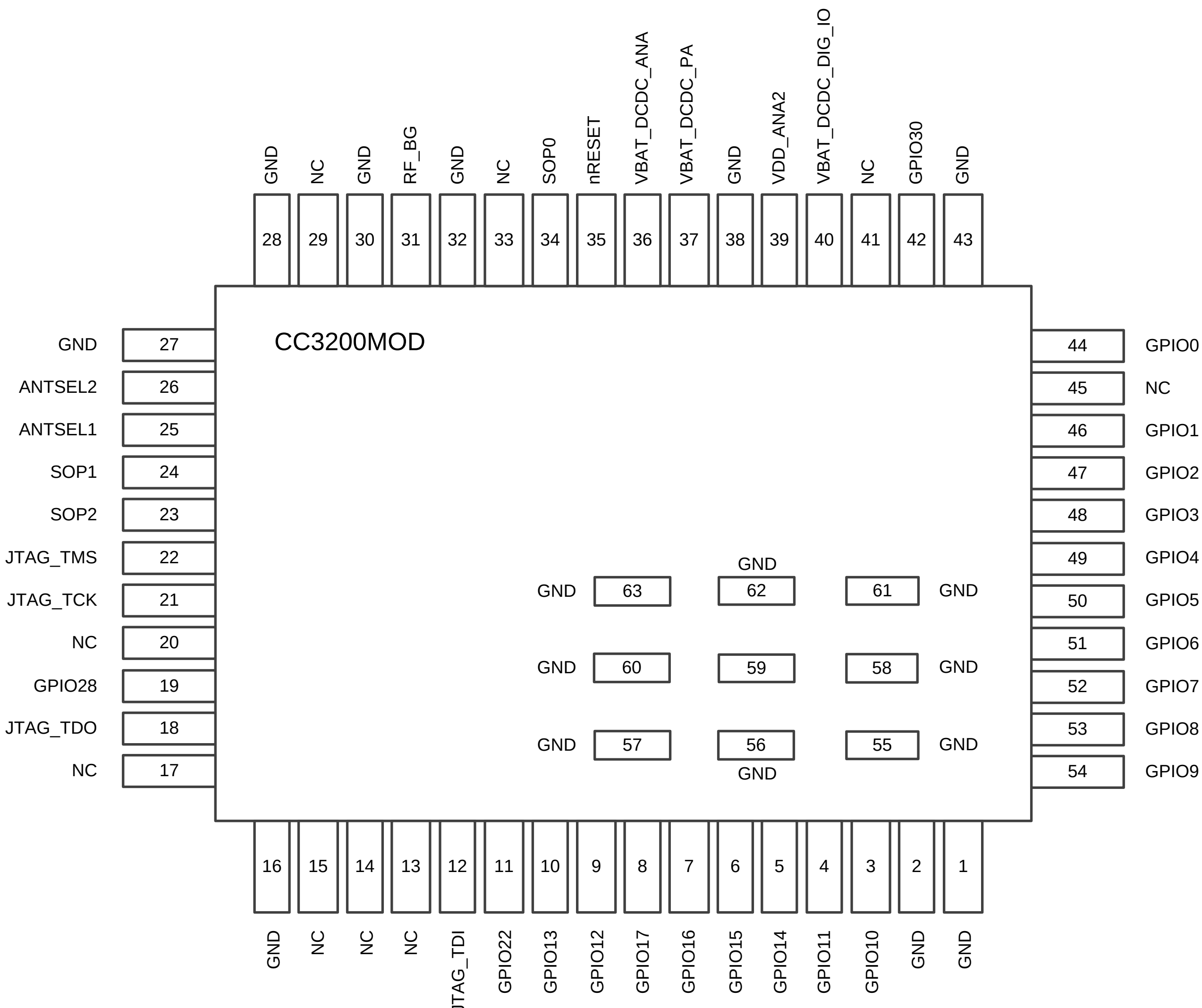


Figure 3-1. CC3200MOD Pin Diagram (Bottom View)

NOTE

Figure 3-1 shows the approximate location of pins on the module. For the actual mechanical diagram refer to Section 9.

3.2 Pin Attributes

Table 3-1 lists the pin descriptions of the CC3200MOD module. "DEVICE PIN NO" refers to the pin number of the QFN part CC3200. This is stated here because the QFN pin is referred to in the SDK.

Table 3-1. Pin Attributes

MODULE PIN NO.	MODULE PIN NAME	TYPE	DEVICE PIN NO	MODULE PIN DESCRIPTION
1	GND	-		Ground
2	GND	-		Ground
3	GPIO10	I/O	1	GPIO(1)
4	GPIO11	I/O	2	GPIO(1)
5	GPIO14	I/O	5	GPIO(1)
6	GPIO15	I/O	6	GPIO(1)
7	GPIO16	I/O	7	GPIO(1)
8	GPIO17	I/O	8	GPIO(1)
9	GPIO12	I/O	3	GPIO(1)
10	GPIO13	I/O	4	GPIO(1)
11	GPIO22	I/O	15	GPIO(1)
12	JTAG_TDI	I/O	16	GPIO(1)
13	NC	-	13	Reserved for TI
14	NC	-	14	Reserved for TI
15	NC	-	11	Reserved for TI
16	GND	-		Ground
17	NC	-	12	Reserved for TI
18	JTAG_TDO	I/O	17	GPIO(1)
19	GPIO28	I/O	18	GPIO(1)
20	NC	-	23	Unused. Do not connect.
21	JTAG_TCK	I/O	19	JTAG TCK input. Needs 100-kΩ pulldown resistor to ground.(1)
22	JTAG_TMS	I/O	20	JTAG TMS input. Leave unconnected if not used on product.(1)
23	SOP2	-	21	Add 2.7-kΩ pulldown resistor to ground needed for functional mode. Add option to pullup required for entering the UART load mode for flashing.
24	SOP1	-	34	Reserved. Do not connect.
25	ANTSEL1	I/O	29	Antenna selection control(1)
26	ANTSEL2	I/O	30	Antenna selection control(1)
27	GND	-		Ground
28	GND	-		Ground
29	NC	-	27, 28	Reserved for TI
30	GND	-		Ground
31	RF_BG	I/O	31	2.4-GHz RF input/output
32	GND	-		Ground
33	NC	-	38	Reserved for TI
34	SOP0	-	35	Optional 10-kΩ pullup if user chooses to use SWD debug mode instead of 4-wire JTAG
35	nRESET	I	32	Power on reset. Does not require external RC circuit
36	VBAT_DCDC_ANA	-	37	Power supply for the device, can be connected to battery (2.3 V to 3.6 V)
37	VBAT_DCDC_PA	-	39	Power supply for the device, can be connected to battery (2.3 V to 3.6 V)
38	GND	-		Ground

(1) For pin multiplexing details, refer to CC3200R device data sheet

Table 3-1. Pin Attributes (continued)

MODULE PIN NO.	MODULE PIN NAME	TYPE	DEVICE PIN NO	MODULE PIN DESCRIPTION
39	NC	-	47	Leave unconnected
40	VBAT_DCDC_DIG_IO	-	10, 44, 54	Power supply for the device, can be connected to battery (2.3 V to 3.6 V)
41	NC	-	25, 36, 48	Reserved for TI
42	GPIO30	I/O	53	GPIO(1)
43	GND	-		Ground
44	GPIO0	I/O	50	GPIO(1)
45	NC	-	51	Reserved for TI
46	GPIO1	I/O	55	GPIO(1)
47	GPIO2	I/O	57	GPIO(1)
48	GPIO3	I/O	58	GPIO(1)
49	GPIO4	I/O	59	GPIO(1)
50	GPIO5	I/O	60	GPIO(1)
51	GPIO6	I/O	61	GPIO(1)
52	GPIO7	I/O	62	GPIO(1)
53	GPIO8	I/O	63	GPIO(1)
54	GPIO9	I/O	64	GPIO(1)
55	GND	-		Thermal Ground
56	GND	-		Thermal Ground
57	GND	-		Thermal Ground
58	GND	-		Thermal Ground
59	GND	-		Thermal Ground
60	GND	-		Thermal Ground
61	GND	-		Thermal Ground
62	GND	-		Thermal Ground
63	GND	-		Thermal Ground

3.3 Pin Attributes and Pin Multiplexing

The module makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at module reset) and register control.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used. Table 3-2 describes the general pin attributes and presents an overview of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers. The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. Drive strength is configurable individually for each pin.
- All I/Os support 10-µA pullups and pulldowns.
- These pulls are not active and all of the I/Os remain floating while the device is in Hibernate state.
- The VIO and VBAT supply must be tied together at all times.
- All digital I/Os are nonfail-safe.

NOTE

If an external device drives a positive voltage to the signal pads and the CC3200MOD is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3200MOD can occur. To prevent current draw, TI recommends any one of the following:

- All devices interfaced to the CC3200MOD must be powered from the same power rail as the chip.
- Use level-shifters between the module and any external devices fed from other independent rails.
- The nRESET pin of the CC3200MOD must be held low until the VBAT supply to the module is driven and stable

---

Table 3-2. Pin Multiplexing

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS(1)**	**Hib(2)**	**nRESET = 0**
GPIO10	I/O	No	No	No	GPIO_PAD_CONFIG_10 (0x4402 E0C8)	0	GPIO10	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						1	I2C_SCL	I2C Clock	O (Open Drain)	Hi-Z		
						3	GT_PWM06	Pulse-Width Modulated O/P	O	Hi-Z		
						7	UART1_TX	UART TX Data	O	1		
						6	SDCARD_CLK	SD Card Clock	O	0		
						12	GT_CCP01	Timer Capture Port	I	Hi-Z		
GPIO11	I/O	Yes	No	No	GPIO_PAD_CONFIG_11 (0x4402 E0CC)	0	GPIO11	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						1	I2C_SDA	I2C Data	I/O (Open Drain)	Hi-Z		
						3	GT_PWM07	Pulse-Width Modulated O/P	O	Hi-Z		
						4	pXCLK (XVCLK)	Free Clock To Parallel Camera	O	0		
						6	SDCARD_CMD	SD Card Command Line	I/O	Hi-Z		
						7	UART1_RX	UART RX Data	I	Hi-Z		
						12	GT_CCP02	Timer Capture Port	I	Hi-Z		
						13	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	Use	Select as Wakeup Source	Config Addl Analog Mux	Muxed with JTAG	Dig. Pin Mux Config Reg	Dig. Pin Mux Config Mode Value	Signal Name	Signal Description	Signal Direction	LPDS(1)	Hib(2)	nRESET = 0
GPIO12	I/O	No	No	No	GPIO_PAD_CONFIG_12 (0x4402 E0D0)	0	GPIO12	General Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						3	McACLK	I2S Audio Port Clock O	O	Hi-Z		
						4	pVS (VSYNC)	Parallel Camera Vertical Sync	I	Hi-Z		
						5	I2C_SCL	I2C Clock	I/O (Open Drain)	Hi-Z		
						7	UART0_TX	UART0 TX Data	O	1		
						12	GT_CCP03	Timer Capture Port	I	Hi-Z		
GPIO13	I/O	Yes	No	No	GPIO_PAD_CONFIG_13 (0x4402 E0D4)	0	GPIO13	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	I2C_SDA	I2C Data	I/O (Open Drain)			
						4	pHS (HSYNC)	Parallel Camera Horizontal Sync	I			
						7	UART0_RX	UART0 RX Data	I			
						12	GT_CCP04	Timer Capture Port	I			
GPIO14	I/O		No	No	GPIO_PAD_CONFIG_14 (0x4402 E0D8)	0	GPIO14	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	I2C_SCL	I2C Clock	I/O (Open Drain)			
						7	GSPI_CLK	General SPI Clock	I/O			
						4	pDATA8 (CAM_D4)	Parallel Camera Data Bit 4	I			
						12	GT_CCP05	Timer Capture Port	I			

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS[(1)]**	**Hib[(2)]**	**nRESET = 0**
GPIO15	I/O		No	No	GPIO_PAD_CONFIG_15 (0x4402 E0DC)	0	GPIO15	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	I2C_SDA	I2C Data	I/O (Open Drain)			
						7	GSPI_MISO	General SPI MISO	I/O			
						4	pDATA9 (CAM_D5)	Parallel Camera Data Bit 5	I			
						13	GT_CCP06	Timer Capture Port	I			
						8	SDCARD_ DATA0	SD Card Data	I/O			
GPIO16	I/O		No	No	GPIO_PAD_CONFIG_16 (0x4402 E0E0)	0	GPIO16	General-Purpose I/O	I/O	Hi-Z Hi-Z Hi-Z	Hi-Z	Hi-Z
						7	GSPI_MOSI	General SPI MOSI	I/O	Hi-Z		
						4	pDATA10 (CAM_D6)	Parallel Camera Data Bit 6	I	Hi-Z		
						5	UART1_TX	UART1 TX Data	O	1		
						13	GT_CCP07	Timer Capture Port	I	Hi-Z		
						8	SDCARD_CLK	SD Card Clock	O	O		
GPIO17	I/O	Wake-Up Source	No	No	GPIO_PAD_CONFIG_17 (0x4402 E0E4)	0	GPIO17	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	UART1_RX	UART1 RX Data	I			
						7	GSPI_CS	General SPI Chip Select	I/O			
						4	pDATA11 (CAM_D7)	Parallel Camera Data Bit 7	I			
						8	SDCARD_ CMD	SD Card Command Line	I/O			

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS(1)**	**Hib(2)**	**nRESET = 0**
GPIO22	I/O	No	No	No	GPIO_PAD_CONFIG_22 (0x4402 E0F8)	0	GPIO22	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						7	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
						5	GT_CCP04	Timer Capture Port	I			
TDI	I/O	No	No	MUXed with JTAG TDI	GPIO_PAD_CONFIG_23 (0x4402 E0FC)	1	TDI	JTAG TDI. Reset Default Pinout.	I	Hi-Z	Hi-Z	Hi-Z
						0	GPIO23	General-Purpose I/O	I/O			
						2	UART1_TX	UART1 TX Data	O	1		
						9	I2C_SCL	I2C Clock	I/O (Open Drain)	Hi-Z		
TDO	I/O	Wake-Up Source	No	MUXed with JTAG TDO	GPIO_PAD_CONFIG_24 (0x4402 E100)	1	TDO	JTAG TDO. Reset Default Pinout.	O	Hi-Z	Hi-Z	Hi-Z
						0	GPIO24	General-Purpose I/O	I/O			
						5	PWM0	Pulse Width Modulated O/P	O			
						2	UART1_RX	UART1 RX Data	I			
						9	I2C_SDA	I2C Data	I/O (Open Drain)			
						4	GT_CCP06	Timer Capture Port	I			
						6	McAFSX	I2S Audio Port Frame Sync	O			
GPIO28	I/O		No		GPIO_PAD_CONFIG_28 (0x4402 E110)	0	GPIO28	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
TCK	I/O	No	No	MUXed with JTAG/ SWD-TCK		1	TCK	JTAG/SWD TCK Reset Default Pinout	I	Hi-Z	Hi-Z	Hi-Z
						8	GT_PWM03	Pulse Width Modulated O/P	O			

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS(1)**	**Hib(2)**	**nRESET = 0**
TMS	I/O	No	No	MUXed with JTAG/ SWD- TMSC	GPIO_PAD_CONFIG_29 (0x4402 E114)	1	TMS	JATG/SWD TMS Reset Default Pinout	I/O	Hi-Z	Hi-Z	Hi-Z
						0	GPIO29	General-Purpose I/O				
SOP2	O Only	No	No	No	GPIO_PAD_CONFIG_25 (0x4402 E104)	0	GPIO25	General-Purpose I/O	O	Hi-Z	Driven Low	Hi-Z
						9	GT_PWM02	Pulse Width Modulated O/P	O	Hi-Z		
						2	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
						See (5)	TCXO_EN	Enable to Optional External 40-MHz TCXO	O	O		
						See (6)	SOP2	Sense-On-Power 2	I			
ANTSEL1	O Only	No	User config not required (8)	No	GPIO_PAD_CONFIG_26 (0x4402 E108)	0	ANTSEL1(3)	Antenna Selection Control	O	Hi-Z	Hi-Z	Hi-Z
ANTSEL2	O Only	No	User config not required (8)	No	GPIO_PAD_CONFIG_27 (0x4402 E10C)	0	ANTSEL2(3)	Antenna Selection Control	O	Hi-Z	Hi-Z	Hi-Z
SOP1	Config Sense	N/A	N/A	N/A	N/A		SOP1	Sense On Power 1				
SOP0	Config Sense	N/A	N/A	N/A	N/A		SOP0	Sense On Power 0				

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS(1)**	**Hib(2)**	**nRESET = 0**
GPIO0	I/O	No	User config not required (8)	No	GPIO_PAD_CONFIG_0 (0x4402 E0A0)	0	GPIO0	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						12	UART0_CTS	UART0 Clear To Send Input (Active Low)	I	Hi-Z	Hi-Z	Hi-Z
						6	McAXR1	I2S Audio Port Data 1 (RX/TX)	I/O	Hi-Z		
						7	GT_CCP00	Timer Capture Port	I	Hi-Z		
						9	GSPI_CS	General SPI Chip Select	I/O	Hi-Z		
						10	UART1_RTS	UART1 Request To Send O (Active Low)	O	1		
						3	UART0_RTS	UART0 Request To Send O (Active Low)	O	1		
						4	McAXR0	I2S Audio Port Data 0 (RX/TX)	I/O	Hi-Z		
GPIO30	I/O	No	User config not required (8)	No	GPIO_PAD_CONFIG_30 (0x4402 E118)	0	GPIO30	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						9	UART0_TX	UART0 TX Data	O	1		
						2	McACLK	I2S Audio Port Clock O	O	Hi-Z		
						3	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
						4	GT_CCP05	Timer Capture Port	I	Hi-Z		
						7	GSPI_MISO	General SPI MISO	I/O	Hi-Z		
GPIO1	I/O	No	No	No	GPIO_PAD_CONFIG_1 (0x4402 E0A4)	0	GPIO1	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						3	UART0_TX	UART0 TX Data	O	1		
						4	pCLK (PIXCLK)	Pixel Clock From Parallel Camera Sensor	I	Hi-Z		
						6	UART1_TX	UART1 TX Data	O	1		
						7	GT_CCP01	Timer Capture Port	I	Hi-Z		

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS[1]**	**Hib[2]**	**nRESET = 0**
GPIO2	Analog Input (up to 1.8 V)/ Digital I/O	Wake-Up Source	See [10]	No	GPIO_PAD_CONFIG_2 (0x4402 E0A8)	See [5]	ADC_CH0	ADC Channel 0 Input (1.5V max)	I		Hi-Z	Hi-Z
						0	GPIO2	General-Purpose I/O	I/O	Hi-Z		
						3	UART0_RX	UART0 RX Data	I	Hi-Z		
						6	UART1_RX	UART1 RXt Data	I	Hi-Z		
						7	GT_CCP02	Timer Capture Port	I	Hi-Z		
GPIO3	Analog Input (up to 1.8 V)/ Digital I/O	No	See [10]	No	GPIO_PAD_CONFIG_3 (0x4402 E0AC)	See [5]	ADC_CH1	ADC Channel 1 Input (1.5V max)	I		Hi-Z	Hi-Z
						0	GPIO3	General-Purpose I/O	I/O	Hi-Z		
						6	UART1_TX	UART1 TX Data	O	1		
						4	pDATA7 (CAM_D3)	Parallel Camera Data Bit 3	I	Hi-Z		
GPIO4	Analog Input (up to 1.8 V)/ Digital I/O	Wake-up Source	See [10]	No	GPIO_PAD_CONFIG_4 (0x4402 E0B0)	See [5]	ADC_CH2	ADC Channel 2 Input (1.5V max)	I		Hi-Z	Hi-Z
						0	GPIO4	General-Purpose I/O	I/O	Hi-Z		
						6	UART1_RX	UART1 RX Data	I	Hi-Z		
						4	pDATA6 (CAM_D2)	Parallel Camera Data Bit 2	I	Hi-Z		
GPIO5	Analog Input (up to 1.8 V)/ Digital I/O	No	See [10]	No	GPIO_PAD_CONFIG_5 (0x4402 E0B4)	See [5]	ADC_CH3	ADC Channel 3 Input (1.5V max)	I		Hi-Z	Hi-Z
						0	GPIO5	General-Purpose I/O	I/O	Hi-Z		
						4	pDATA5 (CAM_D1)	Parallel Camera Data Bit 1	I	Hi-Z		
						6	McAXR1	I2S Audio Port Data 1 (RX/TX)	I/O	Hi-Z		
						7	GT_CCP05	Timer Capture Port	I	Hi-Z		

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	Use	Select as Wakeup Source	Config Addl Analog Mux	Muxed with JTAG	Dig. Pin Mux Config Reg	Dig. Pin Mux Config Mode Value	Signal Name	Signal Description	Signal Direction	LPDS[(1)]	Hib[(2)]	nRESET = 0
GPIO6	No	No	No	No	GPIO_PAD_CONFIG_6 (0x4402 E0B8)	0	GPIO6	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	UART0_RTS	UART0 Request To Send O (Active Low)	O	1		
						4	pDATA4 (CAM_D0)	Parallel Camera Data Bit 0	I	Hi-Z		
						3	UART1_CTS	UART1 Clear To Send Input (Active Low)	I	Hi-Z		
						6	UART0_CTS	UART0 Clear To Send Input (Active Low)	I	Hi-Z		
						7	GT_CCP06	Timer Capture Port	I	Hi-Z		
GPIO7	I/O	No	No	No	GPIO_PAD_CONFIG_7 (0x4402 E0BC)	0	GPIO7	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						13	McACLKX	I2S Audio Port Clock O	O	Hi-Z		
						3	UART1_RTS	UART1 Request To Send O (Active Low)	O	1		
						10	UART0_RTS	UART0 Request To Send O (Active Low)	O	1		
						11	UART0_TX	UART0 TX Data	O	1		
GPIO8	I/O	No	No	No	GPIO_PAD_CONFIG_8 (0x4402 E0C0)	0	GPIO8	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						6	SDCARD_IRQ	Interrupt from SD Card (Future support)	I			
						7	McAFSX	I2S Audio Port Frame Sync	O			
						12	GT_CCP06	Timer Capture Port	I			

Table 3-2. Pin Multiplexing (continued)

General Pin Attributes					Function					Pad States		
Pin Alias	**Use**	**Select as Wakeup Source**	**Config Addl Analog Mux**	**Muxed with JTAG**	**Dig. Pin Mux Config Reg**	**Dig. Pin Mux Config Mode Value**	**Signal Name**	**Signal Description**	**Signal Direction**	**LPDS(1)**	**Hib(2)**	**nRESET = 0**
GPIO9	I/O	No	No	No	GPIO_PAD_CONFIG_9 (0x4402 E0C4)	0	GPIO9	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						3	GT_PWM05	Pulse Width Modulated O/P	O			
						6	SDCARD_ DATA0	SD Cad Data	I/O			
						7	McAXR0	I2S Audio Port Data (Rx/Tx)	I/O			
						12	GT_CCP00	Timer Capture Port	I			

(1) LPDS mode: The state of unused GPIOs in LPDS is input with 500-kΩ pulldown. For all used GPIOs , the user can enable internal pulls, which would hold them in a valid state.

(2) Hibernate mode: The CC3200 device leaves the digital pins in a Hi-Z state without any internal pulls when the device enters hibernate state. This can cause glitches on output lines unless held at valid levels by external resistors.

(3) To minimize leakage in some serial flash vendors during LPDS, TI recommends the user application always enable internal weak pulldowns on FLASH_SPI_DATA and FLASH_SPI_CLK pins.

(4) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a high impedance state but pulled down for SOP mode to disable TCXO. Because of SOP functionality, the pin must be used as output only.

(5) For details on proper use, see *Drive Strength and Reset States for Analog-Digital Multiplexed Pins*.

(6) This pin is one of three that must have a passive pullup or pulldown resistor on board to configure the chip hardware power-up mode. For this reason, the pin must be output only when used for digital functions.

(7) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3200 module between two antennas. These pins should not be used for other functionalities in general.

(8) Device firmware automatically enables the digital path during ROM boot.

(9) This pin is shared by the ADC inputs and digital I/O pad cells. Important: The ADC inputs are tolerant up to 1.8 V. On the other hand, the digital pads can tolerate up to 3.6 V. Hence, care must be taken to prevent accidental damage to the ADC inputs. TI recommends that the output buffer(s) of the digital I/Os corresponding to the desired ADC channel be disabled first (that is, converted to high-impedance state), and thereafter the respective pass switches (S7, S8, S9, S10) should be enabled (see *Drive Strength and Reset States for Analog-Digital Multiplexed Pins*).

(10) Requires user configuration to enable the ADC channel analog switch. (The switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

3.4 Recommended Pin Multiplexing Configurations

Table 3-3 lists the recommended pin multiplexing configurations.

Table 3-3. Recommended Pin Multiplexing Configurations

CC3200 Recommended Pinout Grouping Use – Examples(1)											
	Home Security High-end Toys	Wifi Audio ++ Industrial	Sensor-Tag	Home Security Toys	Wifi Audio ++ Industrial	WiFi Remote w/ 7x7 keypad and audio	Sensor Door-Lock Fire-Alarm Toys w/o Cam	Industrial Home Appliances	Industrial Home Appliances Smart-Plug	Industrial Home Appliances"	GPIOs
	External 32 kHz(2)	**External 32 kHz (2)**								**External TCXO 40 MHZ (-40 to +85°C)**	
	Cam + I2S (Tx or Rx) + I2C + SPI + SWD + UART-Tx + (App Logger) 2 GPIO + 1PWM + *4 overlaid wakeup from Hib	I2S (Tx & Rx) + 1 Ch ADC + 1x 4wire UART + 1x 2wire UART + 1bit SD Card + SPI + I2C + SWD + 3 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib	I2S (Tx & Rx) + 2 Ch ADC + 2wire UART + SPI + I2C + SWD + 2 PMW + 6 GPIO + 3 GPIO with Wake-From-Hib	Cam + I2S (Tx or Rx) + I2C + SWD + UART-Tx + (App Logger) 4 GPIO + 1PWM + *4 overlaid wakeup from HIB	I2S (Tx & Rx) + 1 Ch ADC + 2x 2wire UART + 1bit SD Card + SPI + I2C + SWD + 4 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib	I2S (Tx & Rx) + 1 Ch ADC + UART (Tx Only) I2C + SWD + 15 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib	I2S (Tx or Rx) + 2 Ch ADC + 2 wire UART + SPI + I2C + 3 PMW + 3 GPIO with Wake-From-Hib + 5 GPIO SWD +	4 Ch ADC + 1x 4wire UART + 1x 2wire UART + SPI + I2C + SWD + 1 PWM + 6 GPIO + 1 GPIO with Wake-From-Hib Enable for Ext 40 MHz TCXO	3 Ch ADC + 2wire UART + SPI + I2C + SWD + 3 PWM + 9 GPIO + 2 GPIO with Wake-From-Hib	2 Ch ADC + 2wire UART + I2C + SWD + 3 PWM + 11 GPIO + 5 GPIO with Wake-From-Hib	
Pin	**Pinout #11**	**Pinout #10**	**Pinout #9**	**Pinout #8**	**Pinout #7**	**Pinout #6**	**Pinout #5**	**Pinout #4**	**Pinout #3**	**Pinout #2**	**Pinout #1**
GPIO_30	GSPI-MISO	MCASP-ACLKX	MCASP-ACLKX	GPIO_30	GPIO_30	GPIO_30	GPIO_30	UART0-TX	GPIO_30	UART0-TX	GPIO_30
GPIO_31	GSPI-CLK	McASP-AFSX	McASP-D0	GPIO_31	McASP-AFSX	McASP-AFSX	McASP-AFSX	UART0-RX	GPIO_31	UART0-RX	GPIO_31
GPIO_0	GSPI-CS	McASP-D1 (Rx)	McASP-D1	McASP-D1	McASP-D1	McASP-D1	McASP-D1	UART0-CTS	GPIO_0	GPIO_0	GPIO_0
GPIO_1	pCLK (PIXCLK)	UART0-TX	UART0-TX	PIXCLK	UART0-TX	UART0-TX	UART0-TX	GPIO-1	UART0-TX	GPIO_1	GPIO_1
GPIO_2	(wake) GPIO2	UART0-RX	UART0-RX	(wake) GPIO2	UART0-RX	GPIO_2	UART0-RX	ADC-0	UART0-RX	(wake) GPIO_2	(wake) GPIO_2
GPIO_3	pDATA7 (D3)	UART1-TX	ADC-CH1	pDATA7 (D3)	UART1-TX	GPIO_3	ADC-1	ADC-1	ADC-1	ADC-1	GPIO_3
GPIO_4	pDATA6 (D2)	UART1-RX	(wake) GPIO_4	pDATA6 (D2)	UART1-RX	GPIO_4	(wake) GPIO_4	ADC-2	ADC-2	(wake) GPIO_4	(wake) GPIO_4
GPIO_5	pDATA5 (D1)	ADC-3	ADC-3	pDATA5 (D1)	ADC-3	ADC-3	ADC-3	ADC-3	ADC-3	ADC-3	GPIO_5
GPIO_6	pDATA4 (D0)	UART1-CTS	GPIO_6	pDATA4 (D0)	GPIO_6	GPIO_6	GPIO_6	UART0-RTS	GPIO_6	GPIO_6	GPIO_6
GPIO_7	McASP-ACLKX	UART1-RTS	GPIO_7	McASP-ACLKX	McASP-ACLKX	McASP-ACLKX	McASP-ACLKX	GPIO_7	GPIO_7	GPIO_7	GPIO_7

(1) Pins marked "wake" can be configured to wake up the chip from HIBERNATE or LPDS state. In the current silicon revision, any wake pin can trigger wake up from HIBERNATE. The wakeup monitor in the hibernate control module logically ORs these pins applying a selection mask. However, wakeup from LPDS state can be triggered only by one of the wakeup pins that can be configured before entering LPDS. The core digital wakeup monitor use a mux to select one of these pins to monitor.
(2) The device supports the feeding of an external 32.768-kHz clock. This configuration frees one pin (32K_XTAL_N) to use in output-only mode with a 100K pullup.

Table 3-3. Recommended Pin Multiplexing Configurations (continued)

CC3200 Recommended Pinout Grouping Use – Examples(1)												
GPIO_8	McASP-AFSX	SDCARD-IRQ	McASP-AFSX	McASP-AFSX	SDCARD-IRQ	GPIO_8	GPIO_8	GPIO_8	GPIO_8	GPIO_8	GPIO_8
GPIO_9	McASP-D0	SDCARD-DATA	GT_PWM5	McASP-D0	SDCARD-DATA	GPIO_9	GT_PWM5	GT_PWM5	GT_PWM5	GT_PWM5	GPIO_9
GPIO_10	UART1-TX	SDCARD-CLK	GPIO_10	UART1-TX	SDCARD-CLK	GPIO_10	GT_PWM6	UART1-TX	GT_PWM6	GPIO_10	GPIO_10
GPIO_11	(wake) pXCLK (XVCLK)	SDCARD-CMD	(wake) GPIO_11	(wake) pXCLK (XVCLK)	SDCARD-CMD	GPIO_11	(wake) GPIO_11	UART1-RX	(wake) GPIO_11	(wake) GPIO_11	(wake) GPIO_11
GPIO_12	pVS (VSYNC)	I2C-SCL	I2C-SCL	pVS (VSYNC)	I2C-SCL	GPIO_12	I2C-SCL	I2C-SCL	I2C-SCL	GPIO_12	GPIO_12
GPIO_13	(wake) pHS (HSYNC)	I2C-SDA	I2C-SDA	(wake) pHS (HSYNC)	I2C-SDA	GPIO_13	I2C-SDA	I2C-SDA	I2C-SDA	(wake) GPIO_13	(wake) GPIO_13
GPIO_14	pDATA8 (D4)	GSPI-CLK	GSPI-CLK	pDATA8 (D4)	GSPI-CLK	I2C-SCL	GSPI-CLK	GSPI-CLK	GSPI-CLK	I2C-SCL	GPIO_14
GPIO_15	pDATA9 (D5)	GSPI-MISO	GSPI-MISO	pDATA9 (D5)	GSPI-MISO	I2C-SDA	GSPI-MISO	GSPI-MISO	GSPI-MISO	I2C-SDA	GPIO_15
GPIO_16	pDATA10 (D6)	GSPI-MOSI	GSPI-MOSI	pDATA10 (D6)	GSPI-MOSI	GPIO_16	GSPI-MOSI	GSPI-MOSI	GSPI-MOSI	GPIO_16	GPIO_16
GPIO_17	(wake) pDATA11 (D7)	GSPI-CS	GSPI-CS	(wake) pDATA11 (D7)	GSPI-CS	GPIO_17	GSPI-CS	GSPI-CS	GSPI-CS	(wake) GPIO_17	(wake) GPIO_17
GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22
GPIO_23	I2C-SCL	GPIO_23	GPIO_23	I2C-SCL	GPIO_23	GPIO_23	GPIO_23	GPIO_23	GPIO_23	GPIO_23	GPIO_23
GPIO_24	I2C-SDA	(wake) GPIO_24	(wake) GPIO_24	I2C-SDA	(wake) GPIO_24	(wake) GPIO_24	(wake) GPIO_24	(wake) GPIO_24	(wake) GPIO_24	GT-PWM0	(wake) GPIO_24
JTAG_TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK
JTAG_TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS
GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28
GPIO_25	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	TCXO_EN	GT_PWM2	GT_PWM2	GPIO_25 out only

3.5 Drive Strength and Reset States for Analog-Digital Multiplexed Pins

Table 3-4 describes the use, drive strength, and default state of these pins at first-time power up and reset (nRESET pulled low).

Table 3-4. Drive Strength and Reset States for Analog-Digital Multiplexed Pins

Pin	Board Level Configuration and Use	Default State at First Power Up or Forced Reset	State after Configuration of Analog Switches (ACTIVE, LPDS, and HIB Power Modes)	Maximum Effective Drive Strength (mA)
25	Connected to the enable pin of the RF switch (ANTSEL1). Other use not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
26	Connected to the enable pin of the RF switch (ANTSEL2). Other use not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
44	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
42	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
47	Analog signal (1.8 V absolute, 1.46 V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
48	Analog signal (1.8 V absolute, 1.46 V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
49	Analog signal (1.8 V absolute, 1.46 V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
50	Analog signal (1.8 V absolute, 1.46 V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4

3.6 Pad State After Application of Power To Chip But Prior To Reset Release

When a stable power is applied to the CC3200 chip for the first time or when supply voltage is restored to the proper value following a prior period with supply voltage below 1.5 V, the level of the digital pads are undefined in the period starting from the release of nRESET and until DIG_DCDC powers up. This period is less than approximately 10 ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins are required to have a definite value during this pre-reset period, an appropriate pullup or pulldown must be used at the board level. The recommended value of this external pull is 2.7 KΩ.

4 Specifications

4.1 Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the module can occur. Functional operation is not ensured under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the module.

SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
VBAT and VIO	Respect to GND	–0.5	3.3	3.8	V
Digital I/O	Respect to GND	–0.5	–	VBAT + 0.5	V
RF pins		–0.5		2.1	V
Analog pins		–0.5		2.1	V
Temperature		–40		+85	°C

4.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–40	85	°C
V_{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 (1)		–1.0	1.0	kV
		Charged device model (CDM), per JESD22-C101 (2)	All pins	–250	250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours

CONDITIONS	POH
$T_{Ambient}$ up to 85°C, assuming 20% active mode and 80% sleep mode	17,500

4.4 Recommended Operating Conditions

Function operation is not ensured outside this limit, and operation outside this limit for extended periods can adversely affect long-term reliability of the module. (1)

SYMBOL	CONDITION (2)	MIN	TYP	MAX	UNIT
VBAT and VIO	Battery mode	2.3	3.3	3.6	V
Operating temperature	–	–20	25	70	°C
Ambient thermal slew		–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) To ensure WLAN performance, the ripple on the power supply must be less than ±300 mV.

4.5 Brown-Out and Black-Out

The module enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations (such as a TX packet) cause a dip in the supply voltage, potentially triggering a brown-out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (4 contacts for a 2 x AA battery) and the wiring and PCB routing resistance.

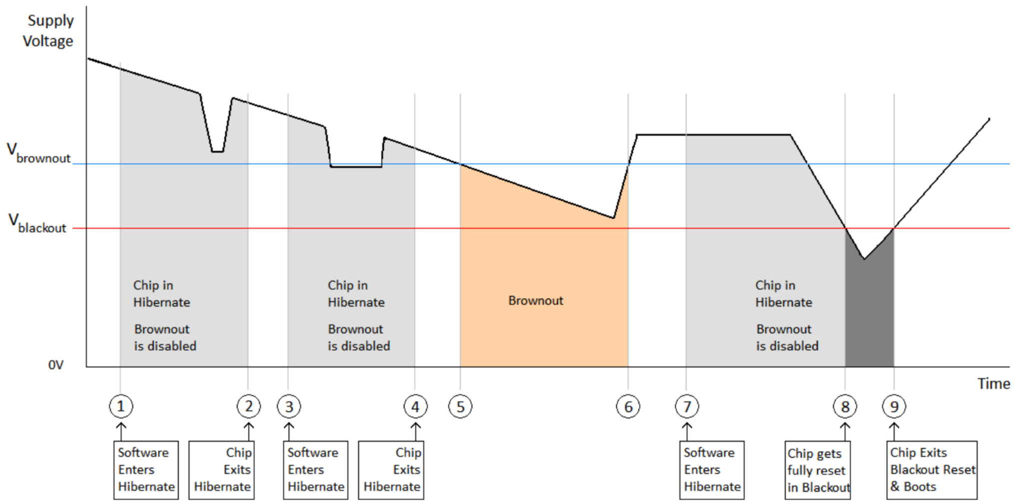


Figure 4-1. Brown-Out and Black-Out Levels (1 of 2)

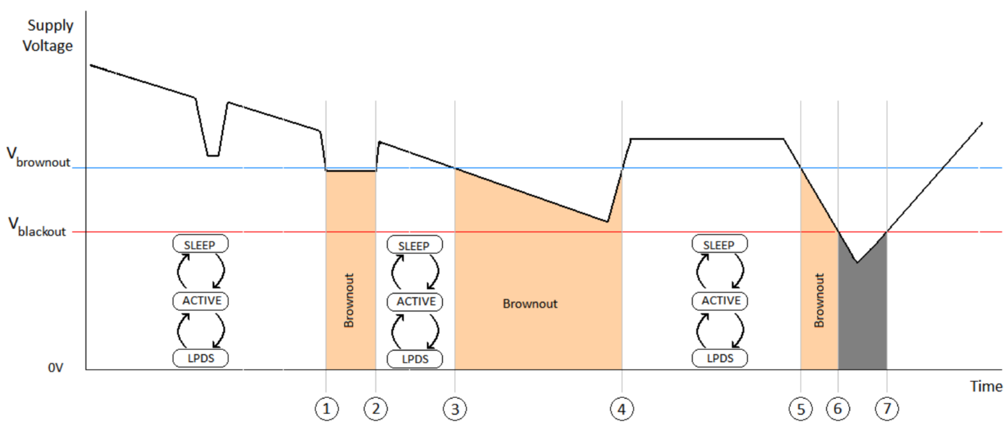


Figure 4-2. Brown-Out and Black-Out Levels (2 of 2)

In the brown-out condition, all sections of the CC3200MOD shut down within the module except for the Hibernate block (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA.

The black-out condition is equivalent to a hardware reset event in which all states within the module are lost.

4.6 Electrical Characteristics (3.3 V, 25°C)

GPIO Pins Except 29, 30, 45, 50, 52, and 53 (25°C)(1)

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × VDD		VDD + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × VDD	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage (VDD = 3.0 V)			2.4			V
V_{OL}	Low-level output voltage (VDD = 3.0 V)					0.4	V
I_{OH}	High-level source current, VOH = 2.4	2-mA Drive		2			mA
		4-mA Drive		4			mA
		6-mA Drive		6			mA
I_{OL}	Low-level sink current, VOH = 0.4	2-mA Drive		2			mA
		4-mA Drive		4			mA
		6-mA Drive		6			mA

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and mitigates any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

GPIO Pins 29, 30, 45, 50, 52, and 53 (25°C)(1)

PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				7		pF
V_{IH}	High-level input voltage			0.65 × VDD		VDD + 0.5V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × VDD	V
I_{IH}	High-level input current				50		nA
I_{IL}	Low-level input current				50		nA
V_{OH}	High-level output voltage (VDD= 3.0 V)			2.4			V
V_{OL}	Low-level output voltage (VDD= 3.0 V)					0.4	V
I_{OH}	High-level source current, V_{OH} = 2.4	2-mA Drive		1.5			mA
		4-mA Drive		2.5			mA
		6-mA Drive		3.5			mA
I_{OL}	Low-level sink current, V_{OH} = 0.4	2-mA Drive		1.5			mA
		4-mA Drive		2.5			mA
		6-mA Drive		3.5			mA
V_{IL}	nRESET(2)				0.6		V

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and mitigates any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.
(2) The nRESET pin must be held below 0.6 V to ensure the device is reset properly.

Pin Internal Pullup and Pulldown (25°C)(1)						
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{OH}	Pullup current, V_{OH} = 2.4 (VDD = 3.0 V)		5		10	µA
I_{OL}	Pulldown current, V_{OL} = 0.4 (VDD = 3.0 V)		5			µA

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to WLAN radio and mitigates any potential degradation of RF sensitivity and performance. The default drive-strength setting is 6 mA.

4.7 Thermal Resistance Characteristics for MOB Package

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\Theta_{JC}$	Junction-to-case	9.08	0.00
$R\Theta_{JB}$	Junction-to-board	10.34	0.00
$R\Theta_{JA}$	Junction-to-free air	11.60	0.00
$R\Theta_{JMA}$	Junction-to-moving air	5.05	< 1.00
Psi_{JT}	Junction-to-package top	9.08	0.00
Psi_{JB}	Junction-to-board	10.19	0.00

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.
(3) m/s = meters per second.

4.8 Reset Requirement

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operation mode level	ViH		0.65 × VBAT		V
Shutdown mode level(1)	ViL	0	0.6 V		V
Minimum time for nReset low for resetting the module		5			ms
Rise/fall times	Tr/Tf		20		µs

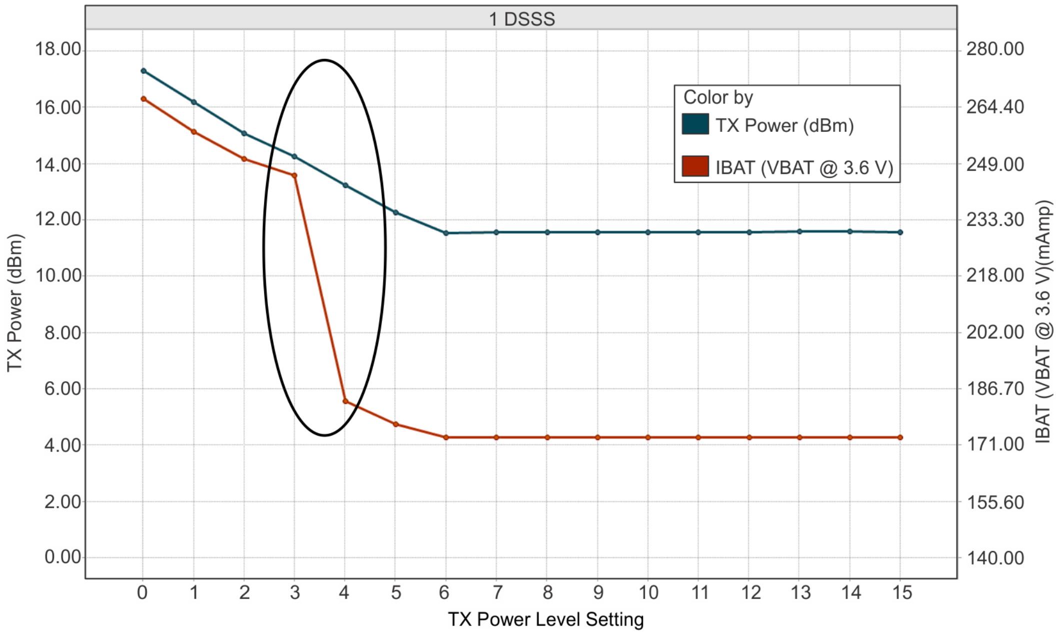
(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

4.9 Current Consumption

T_A = +25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS (1) (2)			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		278		mA
				TX power level = 4		194		
			6 OFDM	TX power level = 0		254		
				TX power level = 4		185		
			54 OFDM	TX power level = 0		229		
				TX power level = 4		166		
		RX	1 DSSS			59		
			54 OFDM			59		
	NWP idle connected (3)					15.3		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		275		mA
				TX power level = 4		191		
			6 OFDM	TX power level = 0		251		
				TX power level = 4		182		
			54 OFDM	TX power level = 0		226		
				TX power level = 4		163		
		RX	1 DSSS			56		
			54 OFDM			56		
	NWP idle connected (3)					12.2		
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		272		mA
				TX power level = 4		188		
			6 OFDM	TX power level = 0		248		
				TX power level = 4		179		
			54 OFDM	TX power level = 0		223		
				TX power level = 4		160		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS (4)					0.275		
	NWP idle connected (3)					0.875		
MCU hibernate	NWP hibernate					7		µA
Peak calibration current (5)		V_{BAT} = 3.3 V				450		mA
		V_{BAT} = 2.3 V				620		

(1) TX power level = 0 implies maximum power (see Figure 4-3 through Figure 4-5). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3200 system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) DTIM = 1
(4) The LPDS number reported is with retention of 64KB MCU SRAM. The CC3200 device can be configured to retain 0KB, 64KB, 128KB, 192KB or 256KB SRAM in LPDS. Each 64KB retained increases LPDS current by 4 µA.
(5) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms . Calibration is performed sparingly, typically when coming out of Hibernate and only if temperature has changed by more than 20°C or the time elapsed from prior calibration is greater than 24 hours.



Note: The area enclosed in the circle represents a significant reduction in current when transitioning from TX power level 3 to 4. In the case of lower range requirements (13-dbm output power), TI recommends using TX power level 4 to reduce the current.

Figure 4-3. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

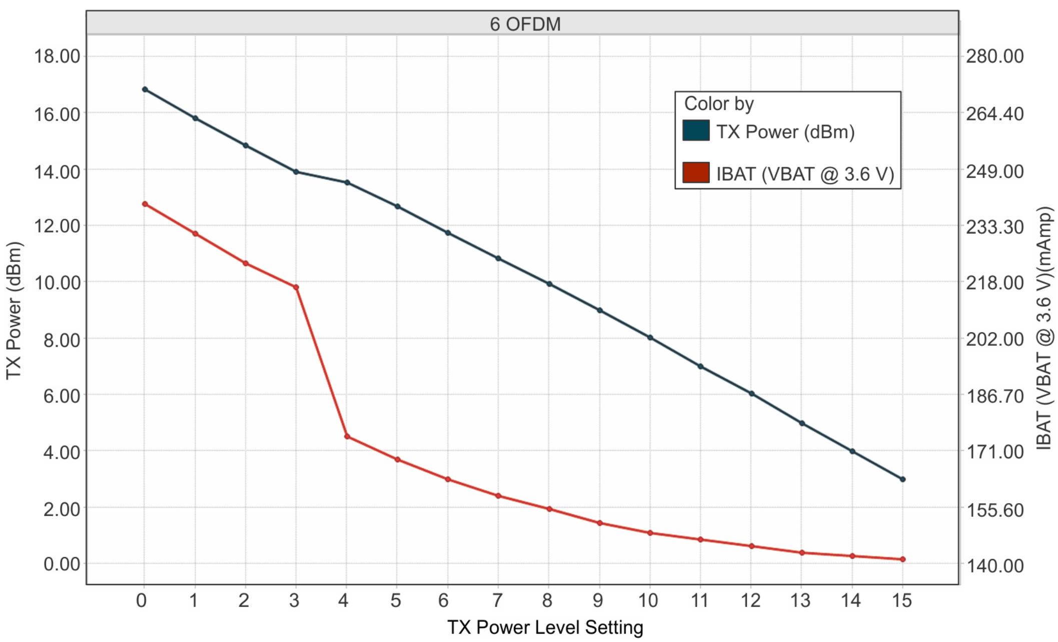


Figure 4-4. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

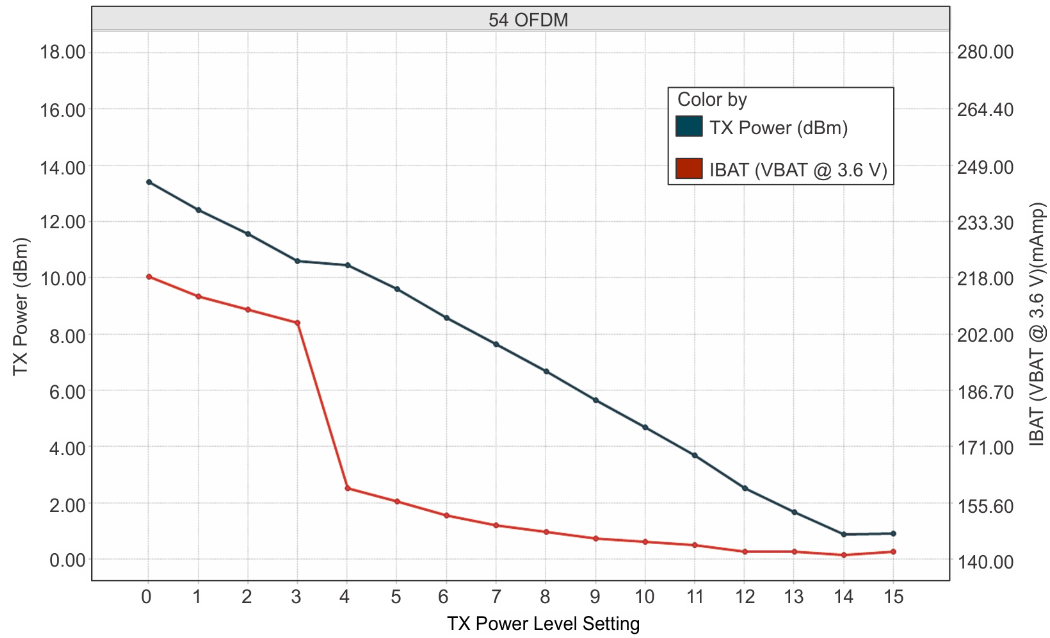


Figure 4-5. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

4.10 WLAN RF Characteristics

WLAN Receiver Characteristics

T_A = +25°C, V_{BAT} = 2.3 to 3.6 V. Parameters measured at module pin on channel 7 (2442 MHz)

PARAMETER	CONDITION (Mbps)	MIN	TYP	MAX	UNITS
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)(10% PER)(1)	1 DSSS		–94.7		dBm
	2 DSSS		–92.6		
	11 CCK		–87.0		
	6 OFDM		–89.0		
	9 OFDM		–88.0		
	18 OFDM		–85.0		
	36 OFDM		–79.5		
	54 OFDM		–73.0		
	MCS7 (Mixed Mode)		–69.0		
Maximum input level (10% PER)	802.11b		–3.0		
	802.11g		–9.0		

(1) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

4.10.1 WLAN Transmitter Characteristics(1)

T_A = +25°C, V_{BAT} = 2.3 to 3.6 V. Parameters measured at module pin on channel 7 (2442 MHz)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
Max RMS Output Power measured at 1 dB from IEEE spectral mask or EVM	1DSSS		17		dBm
	2DSSS		17		
	11CCK		17.25		
	6OFDM		16.25		
	9OFDM		16.25		
	18OFDM		16		
	36OFDM		15		
	54OFDM		13.5		
	MCS7 (Mixed Mode)		12		
Transmit center frequency accuracy		–20		20	ppm

(1) Channel-to-channel variation is up to 2 dB. The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.

4.11 Timing Characteristics

4.11.1 Reset Timing

4.11.1.1 nRESET (32K XTAL)

Figure 4-6 shows the reset timing diagram for the 32K XTAL first-time power-up and reset removal.

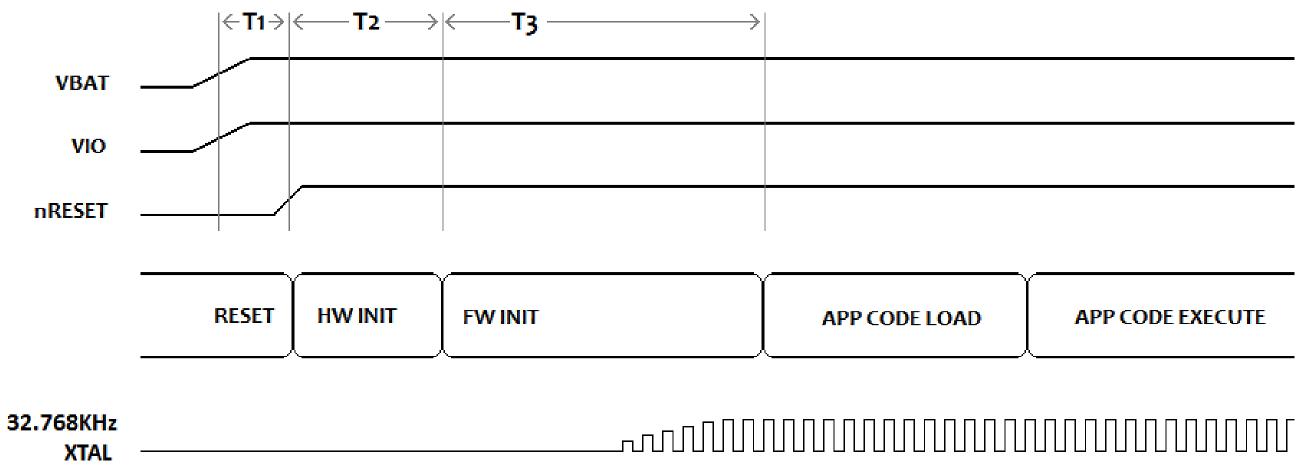


Figure 4-6. First-Time Power-Up and Reset Removal Timing Diagram (32K XTAL)

Table 4-1 describes the timing requirements for the 32K XTAL first-time power-up and reset removal.

Table 4-1. First-Time Power-Up and Reset Removal Timing Requirements (32K XTAL)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX
T1	Supply settling time	Depends on application board power supply, decap, and so on		3 ms	
T2	Hardware wakeup time			25 ms	
T3	Time taken by ROM firmware to initialize hardware	Includes 32.768-kHz XOSC settling time		1.1 s	

4.11.1.2 nRESET (External 32K)

Figure 4-7 shows the reset timing diagram for the external 32K first-time power-up and reset removal.

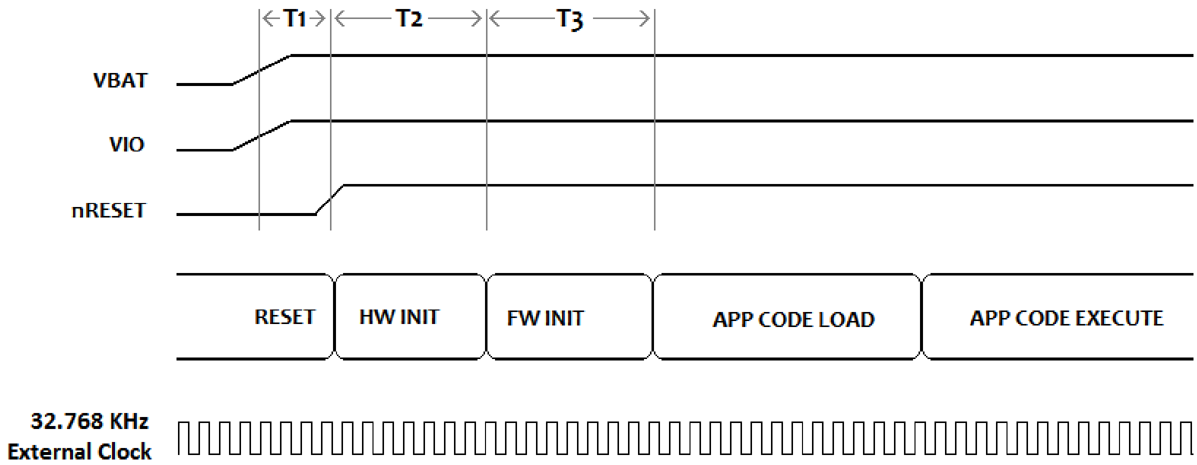


Figure 4-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32K)

Table 4-2 describes the timing requirements for the external 32K first-time power-up and reset removal.

Table 4-2. First-Time Power-Up and Reset Removal Timing Requirements (External 32K)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX
T1	Supply settling time	Depends on application board power supply, decap, and so on		3 ms	
T2	Hardware wakeup time			25 ms	
T3	Time taken by ROM firmware to initialize hardware	Time taken by ROM firmware		3 ms	

4.11.1.3 Wakeup from Hibernate

Figure 4-8 shows the timing diagram for wakeup from the hibernate state.

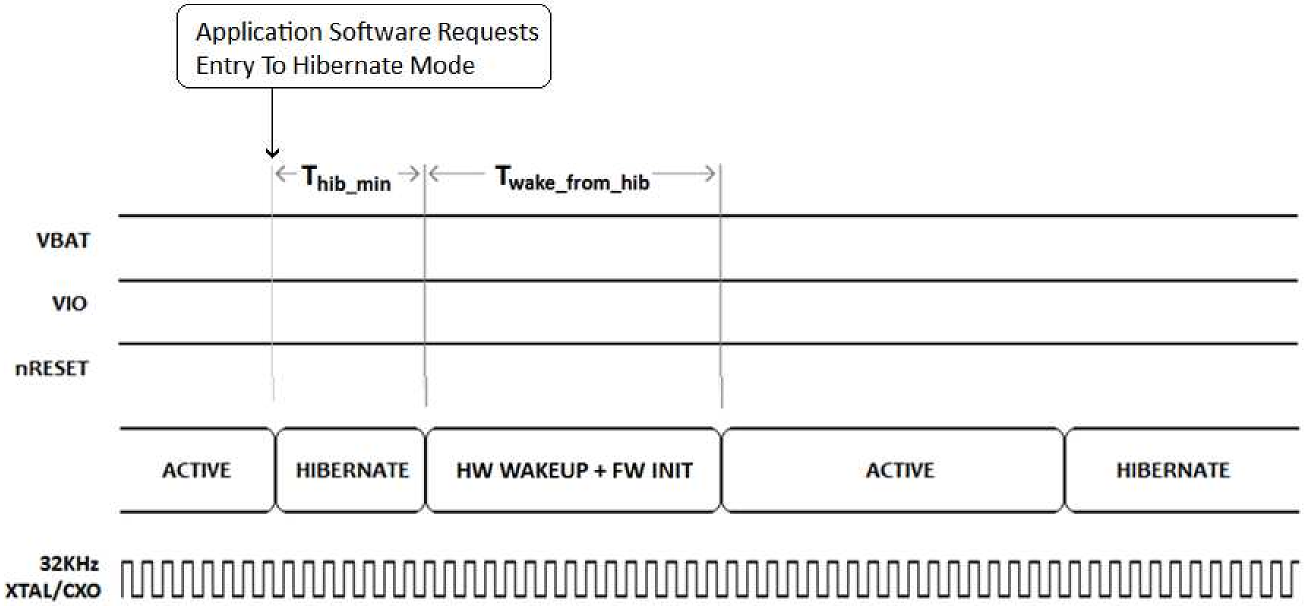


Figure 4-8. nHIB Timing Diagram

NOTE

The 32.768-kHz XTAL is kept enabled by default when the chip goes to hibernate.

Table 4-3 describes the timing requirements for nHIB.

Table 4-3. Software Hibernate Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX
T_{hib_min}	Minimum hibernate time		10 ms		
$T_{wake\_from\_hib}$ (1)	Hardware wakeup time plus firmware initialization time			50 ms (2)	

(1) Twake_from_hib can be 200 ms on rare occasions when calibration is performed. Calibration is performed sparingly, typically when exiting Hibernate and only if temperature has changed by more than 20°C or more than 24 hours have elapsed since a prior calibration.
(2) Wake-up time can extend to 75 ms if a patch is downloaded from the serial flash.

4.11.2 Peripherals

This section describes the peripherals that are supported by the CC3200 module:

- SPI
- McASP
- GPIO
- I^2C
- IEEE 1149.1 JTAG
- ADC

- Camera parallel port
- UART

4.11.2.1 SPI

4.11.2.1.1 SPI Master

The CC3200 microcontroller includes one SPI module, which can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase, a programmable timing control between chip select and external clock generation, and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 4-9 shows the timing diagram for the SPI master.

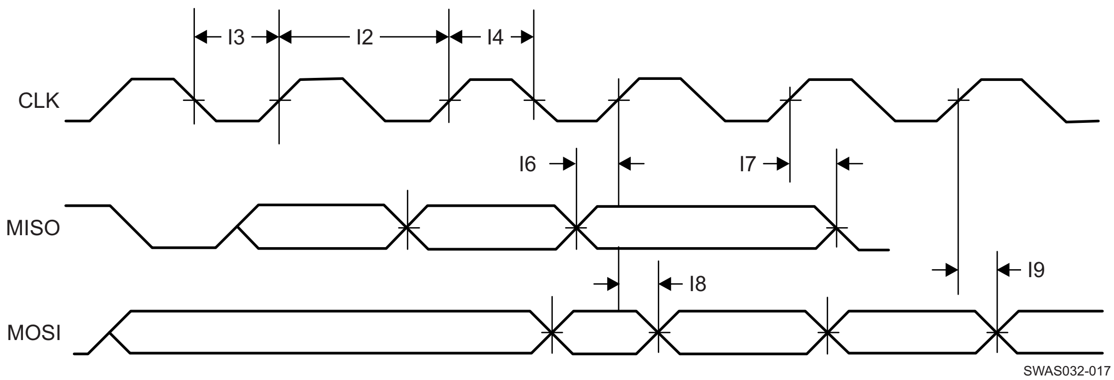


Figure 4-9. SPI Master Timing Diagram

Table 4-4 lists the timing parameters for the SPI master.

Table 4-4. SPI Master Timing Parameters

PARAMETER NUMBER	PARAMETER(1)	PARAMETER NAME	MIN	MAX	UNIT
I1	F	Clock frequency		20	MHz
I2	T_{clk}	Clock period	50		ns
I3	t_{LP}	Clock low period		25	ns
I4	t_{HT}	Clock high period		25	ns
I5	D	Duty cycle	45%	55%	
I6	t_{IS}	RX data setup time	1		ns
I7	t_{IH}	RX data hold time	2		ns
I8	t_{OD}	TX data output delay		8.5	ns
I9	t_{OH}	TX data hold time		8	ns

(1) Timing parameter assumes a maximum load of 20 pF.

4.11.2.1.2 SPI Slave

Figure 4-10 shows the timing diagram for the SPI slave.

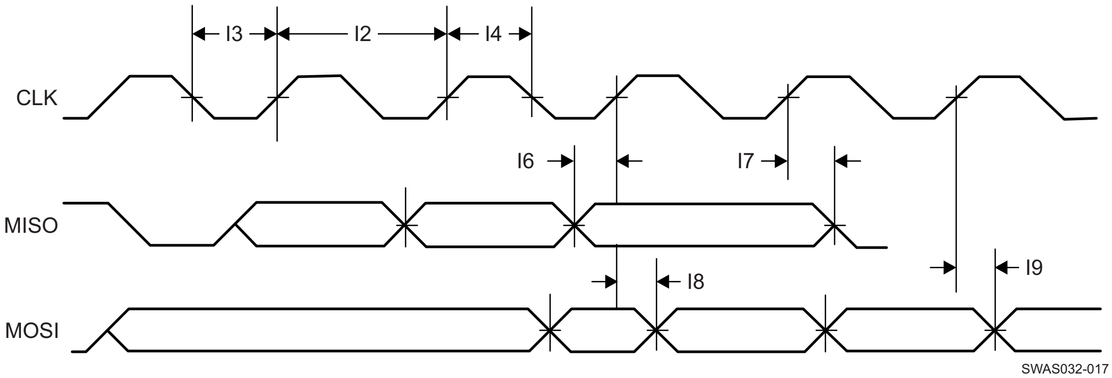


Figure 4-10. SPI Slave Timing Diagram

Table 4-5 lists the timing parameters for the SPI slave.

Table 4-5. SPI Slave Timing Parameters

PARAMETER NUMBER	PARAMETER(1)	PARAMETER NAME	MIN	MAX	UNIT
I1	F	Clock frequency @ VBAT = 3.3 V		20	MHz
		Clock frequency @ VBAT ≤ 2.1 V		12	
I2	Tclk	Clock period	50		ns
I3	tLP	Clock low period		25	ns
I4	tHT	Clock high period		25	ns
I5	D	Duty cycle	45%	55%	
I6	tIS	RX data setup time	4		ns
I7	tIH	RX data hold time	4		ns
I8	tOD	TX data output delay		20	
I9	tOH	TX data hold time		24	ns

(1) Timing parameter assumes a maximum load of 20 pF at 3.3 V.

4.11.2.2 McASP

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

4.11.2.2.1 I2S Transmit Mode

Figure 4-11 shows the timing diagram for the I2S transmit mode.

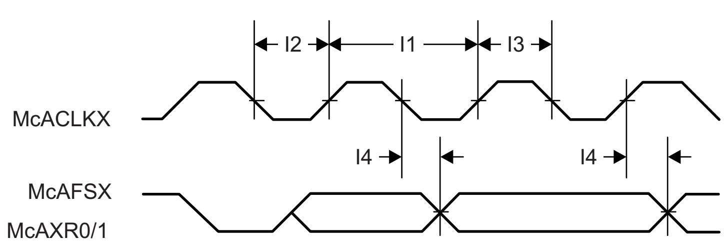


Figure 4-11. I2S Transmit Mode Timing Diagram

Table 4-6 lists the timing parameters for the I2S transmit mode.

Table 4-6. I2S Transmit Mode Timing Parameters

PARAMETER NUMBER	PARAMETER(1)	PARAMETER NAME	MIN	MAX	UNIT
I1	fclk	Clock frequency		9.216	MHz
I2	tLP	Clock low period		1/2 fclk	ns
I3	tHT	Clock high period		1/2 fclk	ns
I4	tOH	TX data hold time		22	ns

(1) Timing parameter assumes a maximum load of 20 pF.

4.11.2.2.2 I2S Receive Mode

Figure 4-12 shows the timing diagram for the I2S receive mode.

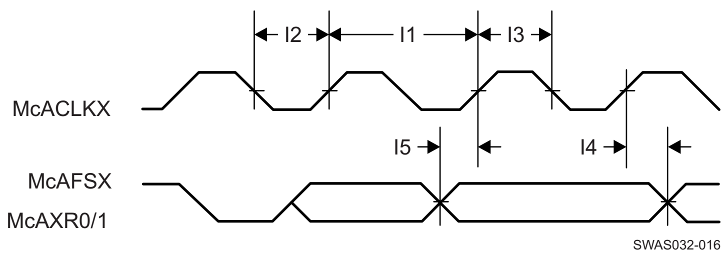


Figure 4-12. I2S Receive Mode Timing Diagram

Table 4-7 lists the timing parameters for the I2S receive mode.

Table 4-7. I2S Receive Mode Timing Parameters

PARAMETER NUMBER	PARAMETER(1)	PARAMETER NAME	MIN	MAX	UNIT
I1	fclk	Clock frequency		9.216	MHz
I2	tLP	Clock low period		1/2 fclk	ns
I3	tHT	Clock high period		1/2 fclk	ns
I4	tOH	RX data hold time		0	ns
I5	tOS	RX data setup time		15	ns

(1) Timing parameter assumes a maximum load of 20 pF.

4.11.2.3 GPIO

All digital pins of the device can be used as general-purpose input/output (GPIO) pins.The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 µA), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Figure 4-13 shows the GPIO timing diagram.

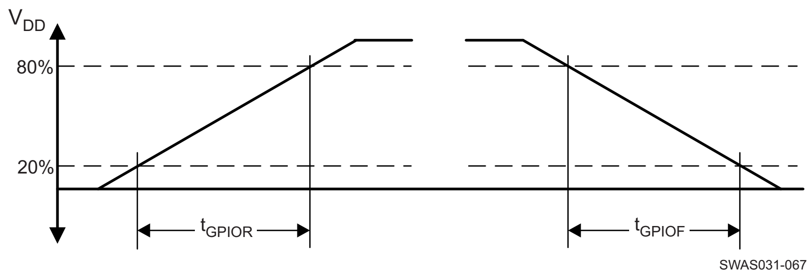


Figure 4-13. GPIO Timing

4.11.2.3.1 GPIO Output Transition Time Parameters (V_{supply} = 3.3 V)

Table 4-8 lists the GPIO output transition times for V_{supply} = 3.3 V.

Table 4-8. GPIO Output Transition Times (V_{supply} = 3.3 V)(1)(2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r (ns)			T_f (ns)		
		MIN	NOM	MAX	MIN	NOM	MAX
2	2MA_EN=1 4MA_EN=0 8MA_EN=0	8.0	9.3	10.7	8.2	9.5	11.0
4	2MA_EN=0 4MA_EN=1 8MA_EN=0	6.6	7.1	7.6	4.7	5.2	5.8
8	2MA_EN=0 4MA_EN=0 8MA_EN=1	3.2	3.5	3.7	2.3	2.6	2.9
14	2MA_EN=1 4MA_EN=1 8MA_EN=1	1.7	1.9	2.0	1.3	1.5	1.6

(1) V_{supply} = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins other than the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

4.11.2.3.2 GPIO Output Transition Time Parameters (Vsupply = 1.8 V)

Table 4-9 lists the GPIO output transition times for V_{supply} = 1.8 V.

Table 4-9. GPIO Output Transition Times (V_{supply} = 1.8 V)(1)(2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r (ns)			T_f (ns)		
		MIN	NOM	MAX	MIN	NOM	MAX
2	2MA_EN=1 4MA_EN=0 8MA_EN=0	11.7	13.9	16.3	11.5	13.9	16.7
4	2MA_EN=0 4MA_EN=1 8MA_EN=0	13.7	15.6	18.0	9.9	11.6	13.6
8	2MA_EN=0 4MA_EN=0 8MA_EN=1	5.5	6.4	7.4	3.8	4.7	5.8

(1) V_{supply} = 1.8 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins other than the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

Table 4-9. GPIO Output Transition Times (V_{supply} = 1.8 V)(1)(2) (continued)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	T_r (ns)			T_f (ns)		
		MIN	NOM	MAX	MIN	NOM	MAX
14	2MA_EN=1 4MA_EN=1 8MA_EN=1	2.9	3.4	4.0	2.2	2.7	3.3

4.11.2.3.3 GPIO Input Transition Time Parameters

Table 4-10 lists the input transition time parameters.

Table 4-10. GPIO Input Transition Time Parameters

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNIT
Input transition time (t_r,t_f), 10% to 90%		t_r	1	3	ns
		t_f	1	3	

4.11.2.4 I²C

The CC3200 microcontroller includes one I²C module operating with standard (100 Kbps) or fast (400 Kbps) transmission speeds.

Figure 4-14 shows the I²C timing diagram.

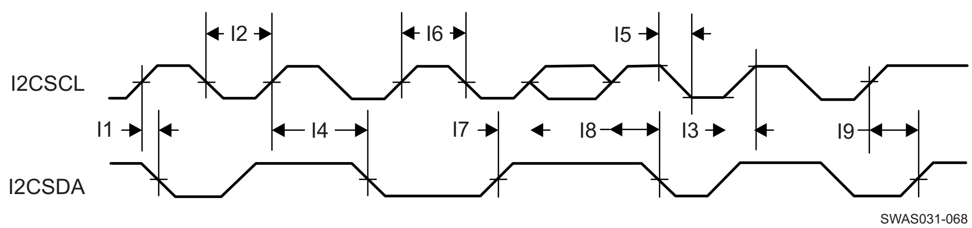


Figure 4-14. I²C Timing

Table 4-11 lists the I²C timing parameters.

Table 4-11. I²C Timing Parameters(1)

PARAMETER NUMBER	PARAMETER	PARAMETER NAME	MIN	MAX	UNIT
I2	t_{LP}	Clock low period	See (2).	-	System clock
I3	t_{SRT}	SCL/SDA rise time	–	See (3).	ns
I4	t_{DH}	Data hold time	NA	–	
I5	t_{SFT}	SCL/SDA fall time	–	3	ns
I6	t_{HT}	Clock high time	See (2).	–	System clock
I7	t_{DS}	Data setup time	tLP/2		System clock
I8	t_{SCSR}	Start condition setup time	36	–	System clock
I9	t_{SCS}	Stop condition setup time	24	–	System clock

(1) All timing is with 6-mA drive and 20-pF load.
(2) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
(3) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of external pullup. Rise time depends on the external signal capacitance and external pullup register value.

4.11.2.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1,*Test Access Port and Boundary- Scan Architecture*.

Figure 4-15 shows the JTAG timing diagram.

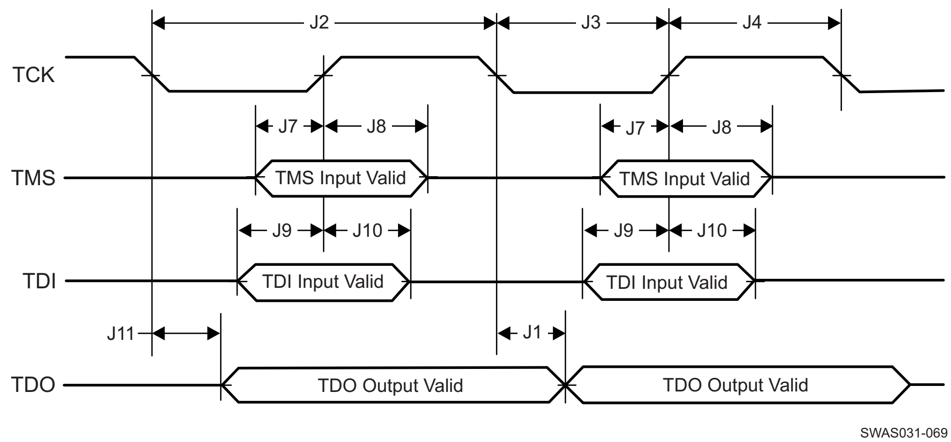


Figure 4-15. JTAG Timing

Table 4-12 lists the JTAG timing parameters.

Table 4-12. JTAG Timing Parameters

PARAMETER NUMBER	PARAMETER	PARAMETER NAME	MIN	MAX	UNIT
J1	fTCK	Clock frequency		15	MHz
J2	tTCK	Clock period		1/fTCK	ns
J3	tCL	Clock low period		tTCK/2	ns
J4	tCH	Clock high period		tTCK/2	ns
J7	tTMS_SU	TMS setup time	1		
J8	tTMS_HO	TMS hold time	16		
J9	tTDI_SU	TDI setup time	1		
J10	tTDI_HO	TDI hold time	16		
J11	tTDO_HO	TDO hold time		15	

4.11.2.6 ADC

Table 4-13 lists the ADC electrical specifications.

Table 4-13. ADC Electrical Specifications

PARAMETER	DESCRIPTION	CONDITION AND ASSUMPTIONS	MIN	TYP	MAX	UNIT
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Worst-case deviation from histogram method over full scale (not including first and last three LSB levels)	–2.5		2.5	LSB
DNL	Differential nonlinearity	Worst-case deviation of any step from ideal	–1		4	LSB
Input range			0		1.4	V

Table 4-13. ADC Electrical Specifications (continued)

PARAMETER	DESCRIPTION	CONDITION AND ASSUMPTIONS	MIN	TYP	MAX	UNIT
Driving source impedance					100	Ω
FCLK	Clock rate	Successive approximation input clock rate		10		MHz
Input capacitance				3.2		pF
Number of channels				4		
F_{sample}	Sampling rate of each ADC			62.5		KSPS
F_input_max	Maximum input signal frequency				31	kHz
SINAD	Signal-to-noise and distortion	Input frequency dc to 300 Hz and 1.4 V_{pp} sine wave input	55	60		dB
I_active	Active supply current	Average for analog-to-digital during conversion without reference current		1.5		mA
I_PD	Power-down supply current for core supply	Total for analog-to-digital when not active (this must be the SoC level test)		1		µA
Absolute offset error		FCLK = 10 MHz		±2		mV
Gain error				±2%		

Figure 4-16 shows the ADC clock timing diagram.

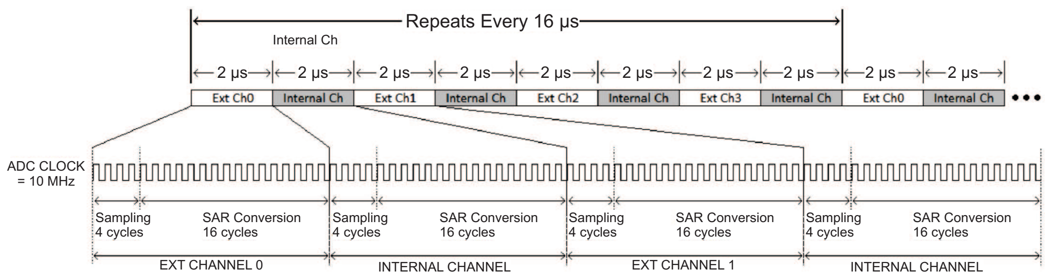


Figure 4-16. ADC Clock Timing

4.11.2.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 4-17 shows the timing diagram for the camera parallel port.

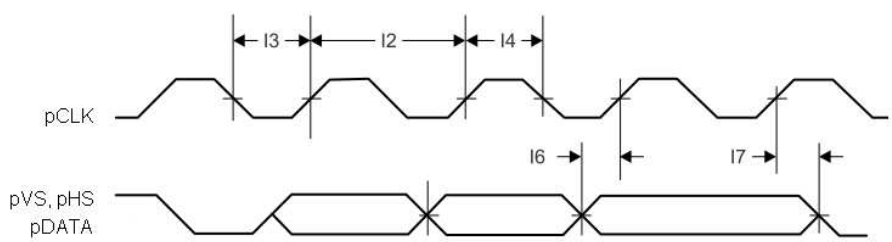


Figure 4-17. Camera Parallel Port Timing Diagram

Table 4-14 lists the timing parameters for the camera parallel port.

Table 4-14. Camera Parallel Port Timing Parameters

PARAMETER NUMBER	PARAMETER	PARAMETER NAME	MIN	MAX	UNIT
	pCLK	Clock frequency		2	MHz
I2	T_{clk}	Clock period		1/pCLK	ns
I3	t_{LP}	Clock low period		$T_{clk}/2$	ns
I4	t_{HT}	Clock high period		$T_{clk}/2$	ns
I7	D	Duty cycle		45% to 55%	
I8	t_{IS}	RX data setup time		2	ns
I9	t_{IH}	RX data hold time		2	ns

4.11.2.8 UART

The CC3200 device includes two UARTs with the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16 x 8 TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop-bit generation
- RTS and CTS hardware flow support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using µDMA
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

5 Detailed Description

5.1 Overview

The CC3200 device has a rich set of peripherals for diverse application requirements. The device optimizes bus matrix and memory management to give the application developer the needed advantage. This section briefly highlights the internal details of the CC3200 device and offers suggestions for application configurations.

5.1.1 Module Features

5.2 Functional Block Diagram

Figure 5-1 shows the functional block diagram of the CC3200MOD SimpleLink Wi-Fi solution.

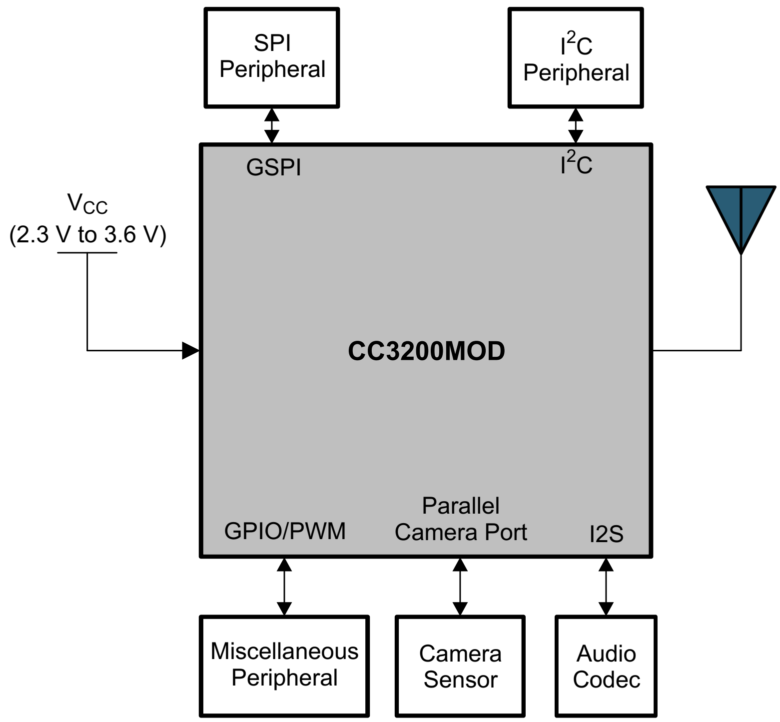


Figure 5-1. Functional Block Diagram

5.3 ARM Cortex-M4 Processor Core Subsystem

The high-performance ARM Cortex-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The ARM Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit ARM Cortex Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 unaligned accesses

- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  – Bits of priority configurable from 3 to 8
  – Dynamic reprioritization of interrupts
  – Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  – Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  – Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  – Wake-up interrupt controller (WIC) providing ultra-low power sleep mode support
- Bus interfaces:
  – Three advanced high-performance bus (AHB-Lite) interfaces: ICode, DCode, and system bus interfaces
  – Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  – Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  – Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  – Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

5.4 CC3200 Device Encryption

Figure 5-2 shows a standard MCU for the CC3200 device. Application image and user data files are not encrypted. Network certificates are encrypted using a device-specific key.

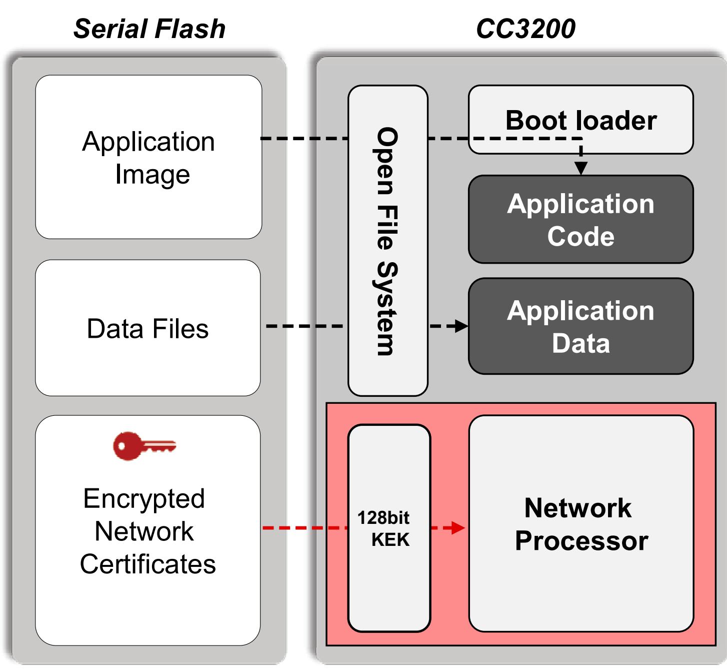


Figure 5-2. CC3200 Standard MCU

5.5 Wi-Fi Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated ARM MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3200 device supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv4 TCP/IP stack.

Table 5-1 summarizes the NWP features.

Table 5-1. Summary of Features Supported by the NWP Subsystem

ITEM	DOMAIN	CATEGORY	FEATURE	DETAILS
1	TCP/IP	Network Stack	IPv4	Baseline IPv4 stack
2	TCP/IP	Network Stack	TCP/UDP	Base protocols
3	TCP/IP	Protocols	DHCP	Client and server mode
4	TCP/IP	Protocols	ARP	Support ARP protocol
5	TCP/IP	Protocols	DNS/mDNS	DNS Address resolution and local server
6	TCP/IP	Protocols	IGMP	Up to IGMPv3 for multicast management
7	TCP/IP	Applications	mDNS	Support multicast DNS for service publishing over IP
8	TCP/IP	Applications	mDNS-SD	Service discovery protocol over IP in local network
9	TCP/IP	Applications	Web Sever/HTTP Server	URL static and dynamic response with template.
10	TCP/IP	Security	TLS/SSL	TLS v1.2 (client/server)/SSL v3.0
11	TCP/IP	Security	TLS/SSL	For the supported Cipher Suite, go to SimpleLink Wi-Fi CC3200 SDK.
12	TCP/IP	Sockets	RAW Sockets	User-defined encapsulation at WLAN MAC/PHY or IP layers
13	WLAN	Connection	Policies	Allows management of connection and reconnection policy
14	WLAN	MAC	Promiscuous mode	Filter-based Promiscuous mode frame receiver
15	WLAN	Performance	Initialization time	From enable to first connection to open AP less than 50 ms
16	WLAN	Performance	Throughput	UDP = 16 Mbps
17	WLAN	Performance	Throughput	TCP = 13 Mbps
18	WLAN	Provisioning	WPS2	Enrollee using push button or PIN method.
19	WLAN	Provisioning	AP Config	AP mode for initial product configuration (with configurable Web page and beacon Info element)
20	WLAN	Provisioning	SmartConfig	Alternate method for initial product configuration
21	WLAN	Role	Station	802.11bgn Station with legacy 802.11 power save
22	WLAN	Role	Soft AP	802.11 bg single station with legacy 802.11 power save
23	WLAN	Role	P2P	P2P operation as GO
24	WLAN	Role	P2P	P2P operation as CLIENT
25	WLAN	Security	STA-Personal	WPA2 personal security
26	WLAN	Security	STA-Enterprise	WPA2 enterprise security
27	WLAN	Security	STA-Enterprise	EAP-TLS
28	WLAN	Security	STA-Enterprise	EAP-PEAPv0/TLS
29	WLAN	Security	STA-Enterprise	EAP-PEAPv1/TLS
30	WLAN	Security	STA-Enterprise	EAP-PEAPv0/MSCHAPv2
31	WLAN	Security	STA-Enterprise	EAP-PEAPv1/MSCHAPv2
32	WLAN	Security	STA-Enterprise	EAP-TTLS/EAP-TLS
33	WLAN	Security	STA-Enterprise	EAP-TTLS/MSCHAPv2
34	WLAN	Security	AP-Personal	WPA2 personal security

5.6 Power-Management Subsystem

The CC3200 power-management subsystem contains DC-DC converters to accommodate the differing voltage or current requirements of the system. The module can operate from an input voltage ranging from 2.3 V to 3.6 V and can be directly connected to 2xAA Alkaline batteries.

The CC3200MOD is a fully integrated module based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC-DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

5.6.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the module is powered directly by the battery or preregulated 3.3-V supply. All other voltages required to operate the device are generated internally by the DC-DC converters. This scheme is the most common mode for the device as it supports wide-voltage operation from 2.3 to 3.6 V.

5.7 Low-Power Operating Mode

From a power-management perspective, the CC3200 device comprises the following two independent subsystems:

- Cortex-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Cortex-M4 application processor runs the user application loaded from an external serial flash. The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 5-2.

NOTE

Table 5-2 lists the modes by power consumption, with highest power modes listed first.

Table 5-2. User Program Modes

APPLICATION PROCESSOR (MCU) MODE	DESCRIPTION
MCU active mode	MCU executing code at 80-MHz state rate
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3 ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs defined in Table 3-2 as the wake-up source.
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The real-time clock (RTC) clock keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO (GPIO0–GPIO6).

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception.

Table 5-3. Networking Subsystem Modes

NETWORK PROCESSOR MODE	DESCRIPTION
Network active mode processing layer 3, 2, and 1	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing not required.
Network active listen mode	Special power optimized active mode for receiving beacon frames (no other frames supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power save operation. The CC3200R network processor automatically goes into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the access point. If not, the network processor returns to LPDS mode and the cycle repeats.
Network LPDS mode	Low-power state between beacons in which the state is retained by the network processor, allowing for a rapid wake up.
Network disabled	

The operation of the application and network processor ensures that the device remains in the lowest power mode most of the time to preserve battery life. Table 5-4 summarizes the important CC3200 chip-level power modes.

Table 5-4. Important Chip-Level Power Modes

POWER STATES FOR APPLICATIONS MCU AND NETWORK PROCESSOR	NETWORK PROCESSOR ACTIVE MODE (TRANSMIT, RECEIVE, OR LISTEN)	NETWORK PROCESSOR LPDS MODE	NETWORK PROCESSOR DISABLED
MCU active mode	Chip = active (C)	Chip = active	Chip = active
MCU LPDS mode	Chip = active (A)	Chip = LPDS (B)	Chip = LPDS
MCU hibernate mode	Not supported because chip is hibernated by MCU; thus, network processor cannot be in active mode	Not supported because chip is hibernated by MCU; thus, network processor cannot be in LPDS mode	Chip = hibernate (D)

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of modes A (receiving a beacon frame) and B (waiting for the next beacon).
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data spends most of the time in mode D (hibernate), jumping briefly to mode C (active) to transmit data.

5.8 Memory

5.8.1 Internal Memory

The CC3200 device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. To select the appropriate SRAM configuration, see the device variants listed in the orderable addendum at the end of this datasheet. The micro direct memory access (μDMA) controller can transfer data to and from SRAM and various peripherals. The CC3200 ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3200 API list.

5.8.1.1 SRAM

The CC3200 family provides up to 256KB of zero-wait-state, on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is located at offset 0x2000 0000 of the device memory map.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

5.8.1.2 ROM

The internal zero-wait-state ROM of the CC3200 device is at address 0x0000 0000 of the device memory and programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial flash memory is empty). The CC3200 DriverLib software library controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory to be used for other purposes.

5.8.1.3 Memory Map

Table 5-5 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 5-5. Memory Map

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x0000 0000	0x0007 FFFF	On-chip ROM (Bootloader + DriverLib)	
0x2000 0000	0x2003 FFFF	Bit-banded on-chip SRAM	
0x2200 0000	0x23FF FFFF	Bit-band alias of 0x2000 0000 through 0x200F FFFF	
0x4000 0000	0x4000 0FFF	Watchdog timer A0	
0x4000 4000	0x4000 4FFF	GPIO port A0	
0x4000 5000	0x4000 5FFF	GPIO port A1	
0x4000 6000	0x4000 6FFF	GPIO port A2	
0x4000 7000	0x4000 7FFF	GPIO port A3	
0x4000 C000	0x4000 CFFF	UART A0	
0x4000 D000	0x4000 DFFF	UART A1	
0x4002 0000	0x400 07FF	I^2C A0 (Master)	
0x4002 0800	0x4002 0FFF	I^2C A0 (Slave)	
0x4003 0000	0x4003 0FFF	General-purpose timer A0	
0x4003 1000	0x4003 1FFF	General-purpose timer A1	
0x4003 2000	0x4003 2FFF	General-purpose timer A2	
0x4003 3000	0x4003 3FFF	General-purpose timer A3	
0x400F 7000	0x400F 7FFF	Configuration registers	
0x400F E000	0x400F EFFF	System control	
0x400F F000	0x400F FFFF	µDMA	
0x4200 0000	0x43FF FFFF	Bit band alias of 0x4000.0000 through 0x400F.FFFF	
0x4401 C000	0x4401 EFFF	McASP	

Table 5-5. Memory Map (continued)

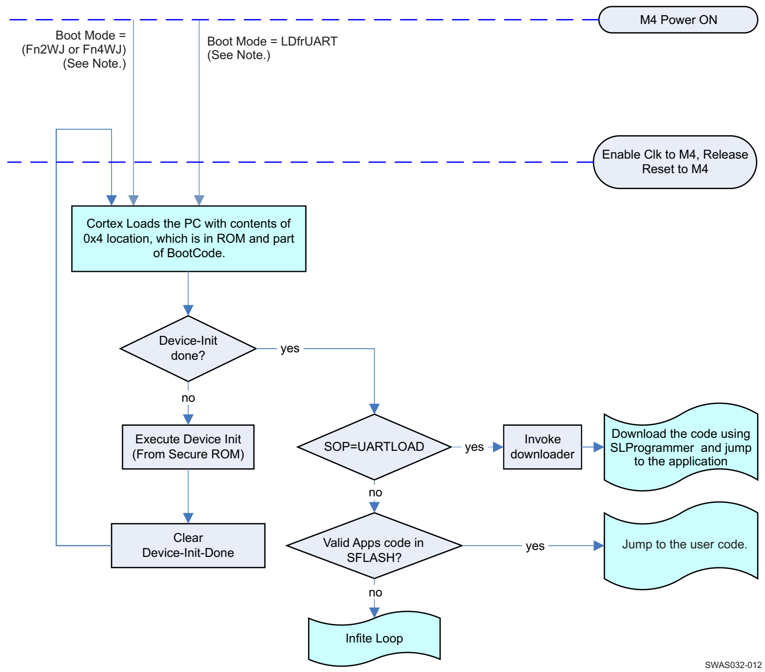
START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x4402 0000	0x4402 0FFF	SSPI	Used for external serial flash
0x4402 1000	0x4402 2FFF	GSPI	Used by application processor
0x4402 5000	0x4402 5FFF	MCU reset clock manager	
0x4402 6000	0x4402 6FFF	MCU configuration space	
0x4402 D000	0x4402 DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402 E000	0x4402 EFFF	MCU shared configuration	
0x4402 F000	0x4402 FFFF	Hibernate configuration	
0x4403 0000	0x4403 FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)	
0x4403 0000	0x4403 0FFF	DTHE registers and TCP checksum	
0x4403 5000	0x4403 5FFF	MD5/SHA	
0x4403 7000	0x4403 7FFF	AES	
0x4403 9000	0x4403 9FFF	DES	
0xE000 0000	0xE000 0FFF	Instrumentation trace Macrocell™	
0xE000 1000	0xE000 1FFF	Data watchpoint and trace (DWT)	
0xE000 2000	0xE000 2FFF	Flash patch and breakpoint (FPB)	
0xE000 E000	0xE000 EFFF	Nested vectored interrupt controller (NVIC)	
0xE004 0000	0xE004 0FFF	Trace port interface unit (TPIU)	
0xE004 1000	0xE004 1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004 2000	0xE00F FFFF	Reserved	

5.9 Boot Modes

5.9.1 Overview

The boot process of the application processor includes two phases. The first phase consists of unrestricted access to all register space and configuration of the specific device setting. In the second phase, the application processor executes user-specific code.

Figure 5-3 shows the bootloader flow chart.



Note: For definitions of the SoP mode functional configurations, see Table 5-6.

Figure 5-3. Bootloader Flow Chart

5.9.2 *Invocation Sequence/Boot Mode Selection*

The following sequence of events occur during the Cortex processor boot:

1. After power-on-reset (POR), the processor starts execution.
2. The processor jumps to the first few lines (FFL) of code in the ROM to determine if the current boot is the first device-init boot or the second MCU boot. The determination is based on the Device-Init flag in a secure register. The Device-Init flag is set out of POR. The registers in the secure region are accessible only in the device-init mode.
3. If the current boot is the first boot, the processor executes the device-init code from ROM.
4. At the end of the boot, the processor clears the Device-Init flag and changes the master ID of the processor and the DMA. These registers are part of the secure region.
5. The processor resets itself, initiating a second boot.
6. During the second boot, the processor rereads the Device-Init flag, the bit is cleared, and the processor obtains a different master ID.
7. After executing FFL and the unsecure boot code, the processor jumps to the developer code (application).
8. For the rest of the operation (until the next power cycle), the Cortex mode is designated the MCU. During this phase, access to the secure region is restricted.

5.9.3 *Boot Mode List*

The CC3200 device implements a sense-on-power (SoP) scheme to determine the device operation mode. The device can be configured to power up in one of the three following modes:

- Fn4WJ: Functional mode with a 4-wire JTAG mapped to fixed pins.
- Fn2WJ: Functional mode with a 2-wire SWD mapped to fixed pins.
- LDfrUART: UART load mode to flash the system during development and in OEM assembly line (for example, serial flash connected to the CC3200R device).

SoP values are sensed from the device pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and then determine the device opeartion mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0) Table 5-6 show the pull configurations.

Table 5-6. CC32x0 Functional Configurations

NAME	SoP[2]	SoP[1]	SoP[0]	SoP MODE	COMMENT
UARTLOAD	Pullup	Pulldown	Pulldown	LDfrUART	Factory/Lab Flash/SRAM load through UART. Device waits indefinitely for UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.
FUNCTIONAL_2WJ	Pulldown	Pulldown	Pullup	Fn2WJ	Functional development mode. In this mode, two-pin SWD is available to the developer. TMS and TCK are available for debugger connection.
FUNCTIONAL_4WJ	Pulldown	Pulldown	Pulldown	Fn4WJ	Functional development mode. In this mode, four-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection.

The recommended value of pull resistors for SOP0 and SOP1 is 100 kΩ and 2.7 kΩ for SOP2. SOP2 can be used by the application for other functions after chip power-up is complete. However, to avoid spurious SOP values from being sensed at power-up, TI strongly recommends that the SOP2 pin be used only for output signals. On the other hand, the SOP0 and SOP1 pins are multiplexed with WLAN analog test pins and are not available for other functions.

6 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Reference Schematics

Figure 6-1 shows the reference schematic for the CC3200MOD module.

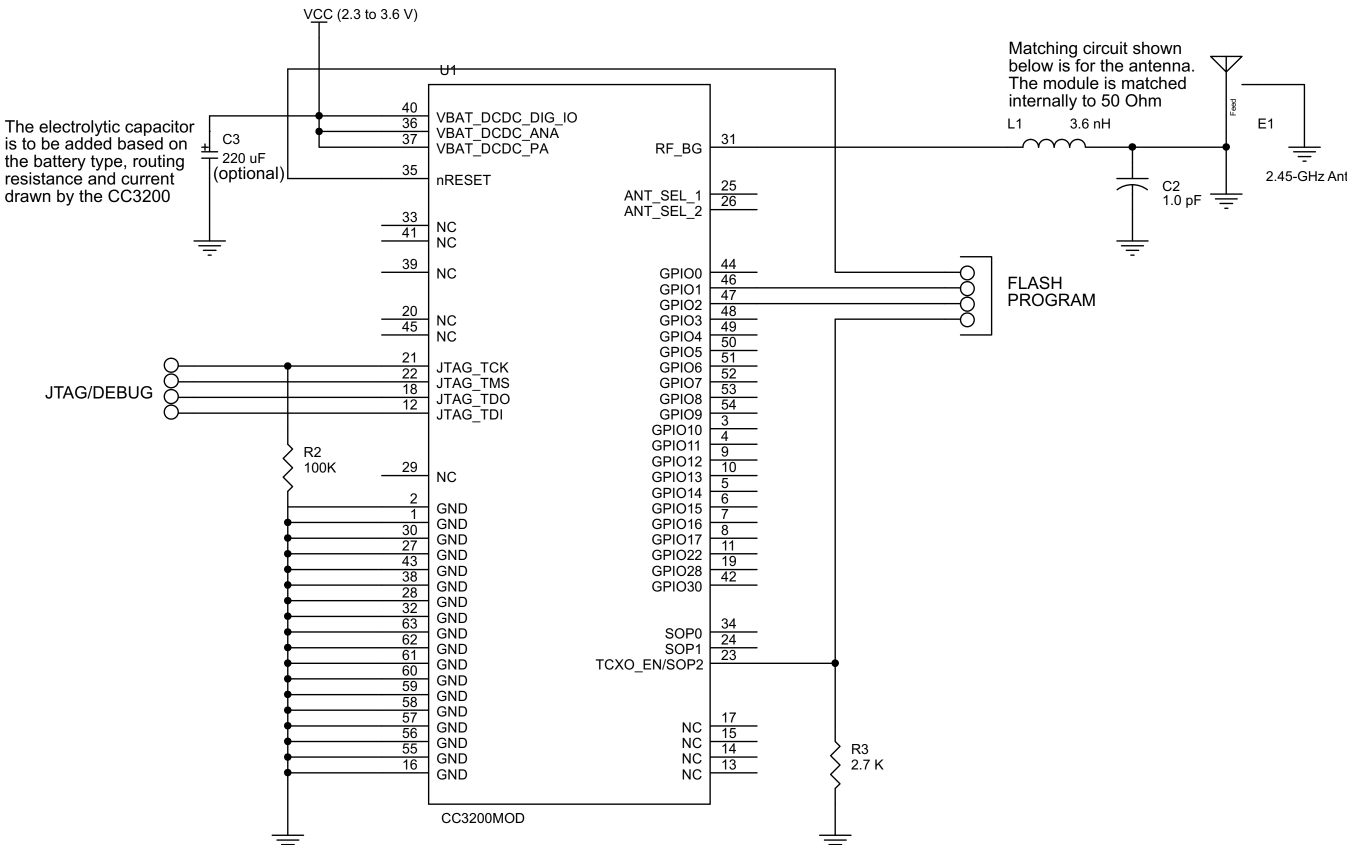


Figure 6-1. CC3200MOD Module Reference Schematic

6.2 Bill of Materials(1)

QUANTITY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	U1	CC3200MOD	Texas Instruments	CC3200MODR1M2AMOB	SimpleLink Wi-Fi MCU Module
1	E1	2.45-GHz Ant	Taiyo Yuden	AH316M245001-T	ANT *Bluetooth* WLAN ZigBee® WIMAX
1	C2	1.0 pF	Murata Electronics North America	GJM1555C1H1R0BB01D	CAP CER 1 pF 50 V NP0 0402
1	L1	3.6 nH	Murata Electronics North America	LQP15MN3N6B02D	INDUCTOR 3.6 NH 0.1 NH 0402

(1) Resistors are not shown here. Any resistor of 5% tolerance can be used.

6.3 Layout Recommendations

6.3.1 RF Section (Placement and Routing)

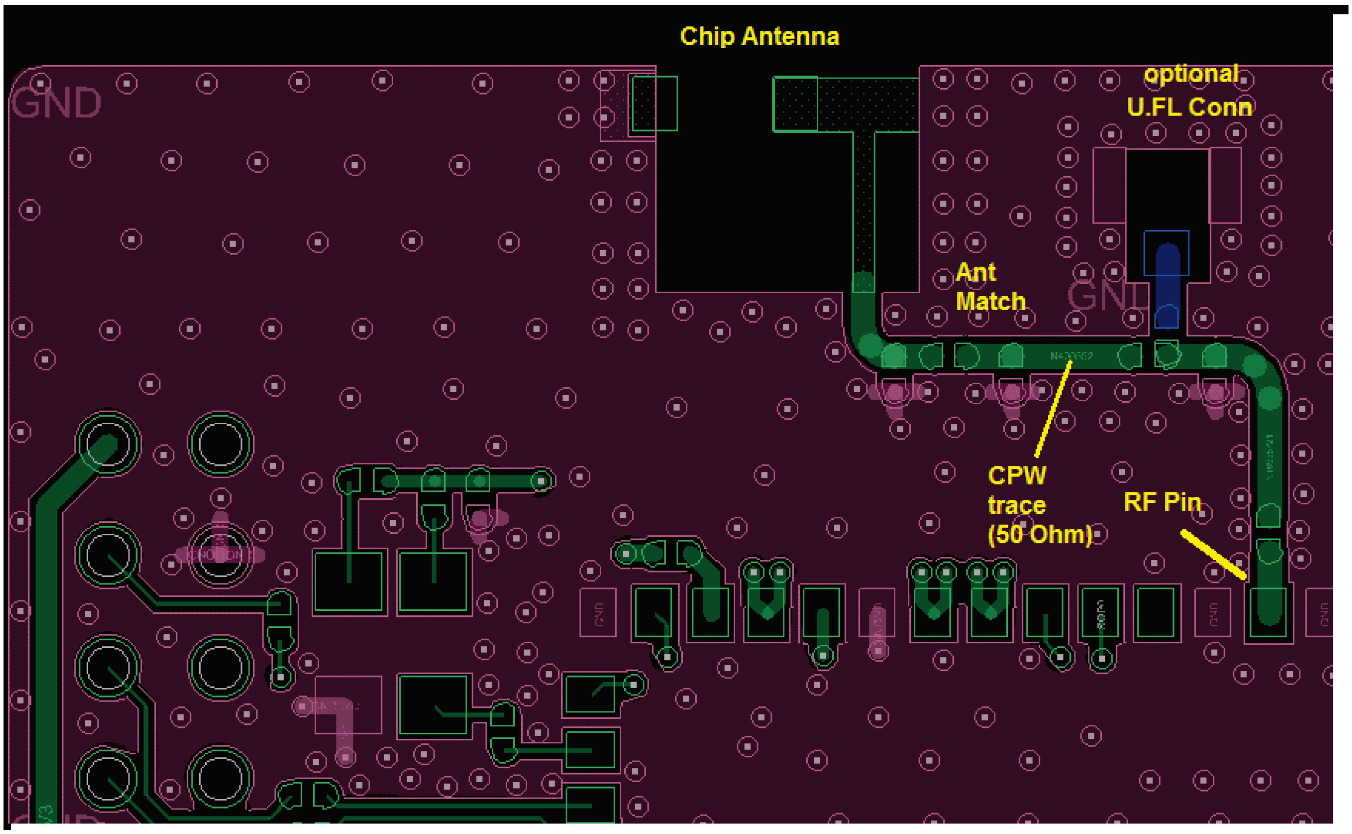


Figure 6-2. RF Section Layout

Being wireless device, the RF section gets the top priority in terms of layout. It is very important for the RF section to be laid out correctly to get the optimum performance from the device. A poor layout can cause low output power, EVM degradation, sensitivity degradation and mask violations.

6.3.2 Antenna Placement and Routing

The antenna is the element used to convert the guided waves on the PCB traces to the free space electromagnetic radiation. The placement and layout of the antenna is the key to increased range and data rates.

The following points need to be observed for the antenna.

SR NO.	GUIDELINES
1	Place the antenna on an edge or corner of the PCB
2	Make sure that no signals are routed across the antenna elements on all the layers of the PCB
3	Most antennas, including the chip antenna used on the booster pack require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4	Ensure that there is provision to place matching components for the antenna. These need to be tuned for best return loss once the complete board is assembled. Any plastics or casing should also be mounted while tuning the antenna as this can impact the impedance.
5	Ensure that the antenna impedance is 50 Ω as the device is rated to work only with a 50-Ω system.
6	In case of printed antenna, ensure that the simulation is performed with the solder mask in consideration.
7	Ensure that the antenna has a near omni-directional pattern.
8	The feed point of the antenna is required to be grounded
9	To use the FCC certification of the Booster pack board, the antenna used should be of the same gain or lesser. In addition, the Antenna design should be exactly copied including the Antenna traces.

Table 6-1. Recommended Components

CHOICE	PART NUMBER	MANUFACTURER	NOTES
1	AH316M245001-T	Taiyo Yuden	Can be placed on edge of the PCB and uses very less PCB space
2	RFANT5220110A2T	Walsim	Need to place on the corner of PCB

6.3.3 Transmission Line

The RF signal from the device is routed to the antenna using a CPW-G (Coplanar Waveguide with ground) structure. This structure offers the maximum isolation across filter gap and the best possible shielding to the RF lines. In addition to the ground on the L1 layer, placing GND vias along the line also provides additional shielding

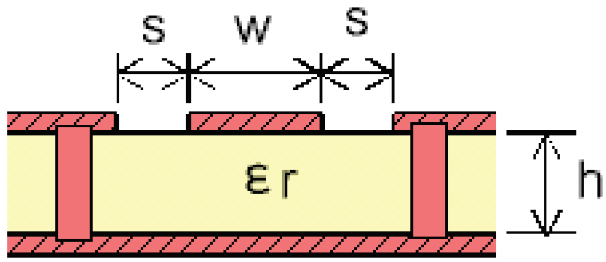


Figure 6-3. Coplanar Waveguide (Cross Section) with GND and Via Stitching

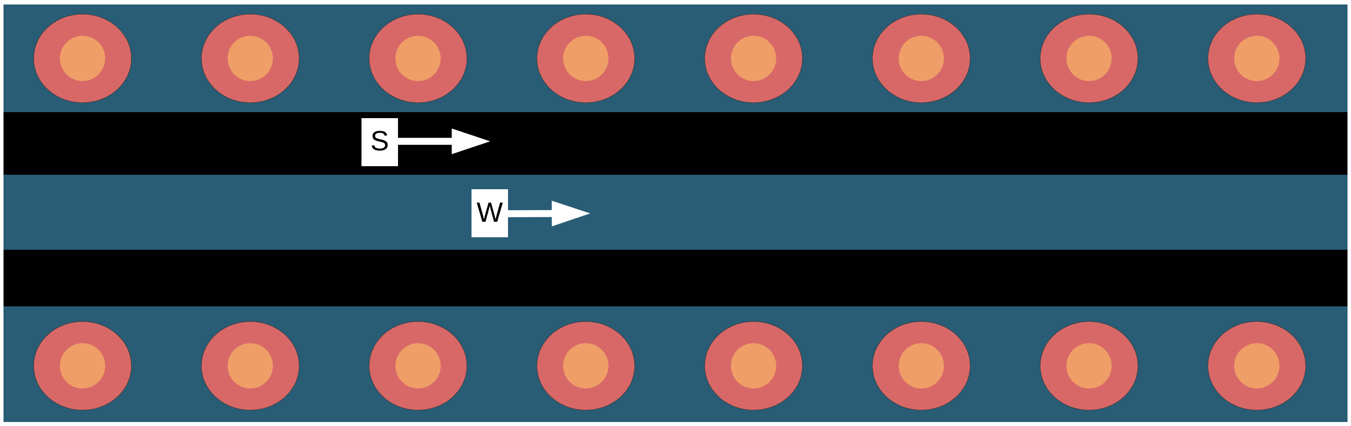


Figure 6-4. CPW with GND (Top View)

The recommended values for the PCB are provided for 4- and 2-layer boards in Table 6-2 and Table 6-3, respectively.

Table 6-2. Recommended PCB Values for 4-Layer Board (L1-L2 = 10 mils)

PARAMETER	VALUE	UNITS
W	20	mils
S	18	mils
H	10	mils
Er (FR-4 substrate)	4	

Table 6-3. Recommended PCB Values for 2-Layer Board (L1-L2 = 40 mils)

PARAMETER	VALUE	UNITS
W	35	mils
S	6	mils
H	40	mils
Er (FR-4 substrate)	3.9	

6.3.4 General Layout Recommendation

1. Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
2. Do not run signal traces underneath the module on a layer where the module is mounted.
3. RF traces must have 50-Ω impedance
4. RF trace bends must be gradual with a maximum bend of approximately 45 degrees and with trace mitered.
5. RF traces must not have sharp corners.
6. There must be no traces or ground under the antenna section.
7. RF traces must have via stitching on the ground plane beside the RF trace on both sides.
8. RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

7 Environmental Requirements and Specifications

7.1 Temperature

7.1.1 PCB Bending

The PCB bending specification shall maintain planeness at a thickness of less than 0.1 mm.

7.2 Handling Environment

7.2.1 Terminals

The product is mounted with motherboard through land grid array (LGA). To prevent poor soldering, do not touch the LGA portion by hand.

7.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product malfunction.

7.3 Storage Condition

7.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be a 12 months from the date the bag is sealed.

7.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

7.4 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12–24 hours

Baking times: 1 time

7.5 Soldering and Reflow Condition

1. Heating method: Conventional Convection or IR/convection
2. Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method.
3. Solder paste composition: Sn/3.0 Ag/0.5 Cu
4. Allowable reflow soldering times: 2 times based on the following reflow soldering profile (see Figure 7-1).
5. Temperature profile: Reflow soldering shall be done according to the following temperature profile (see Figure 7-1).
6. Peak temp: 245°C

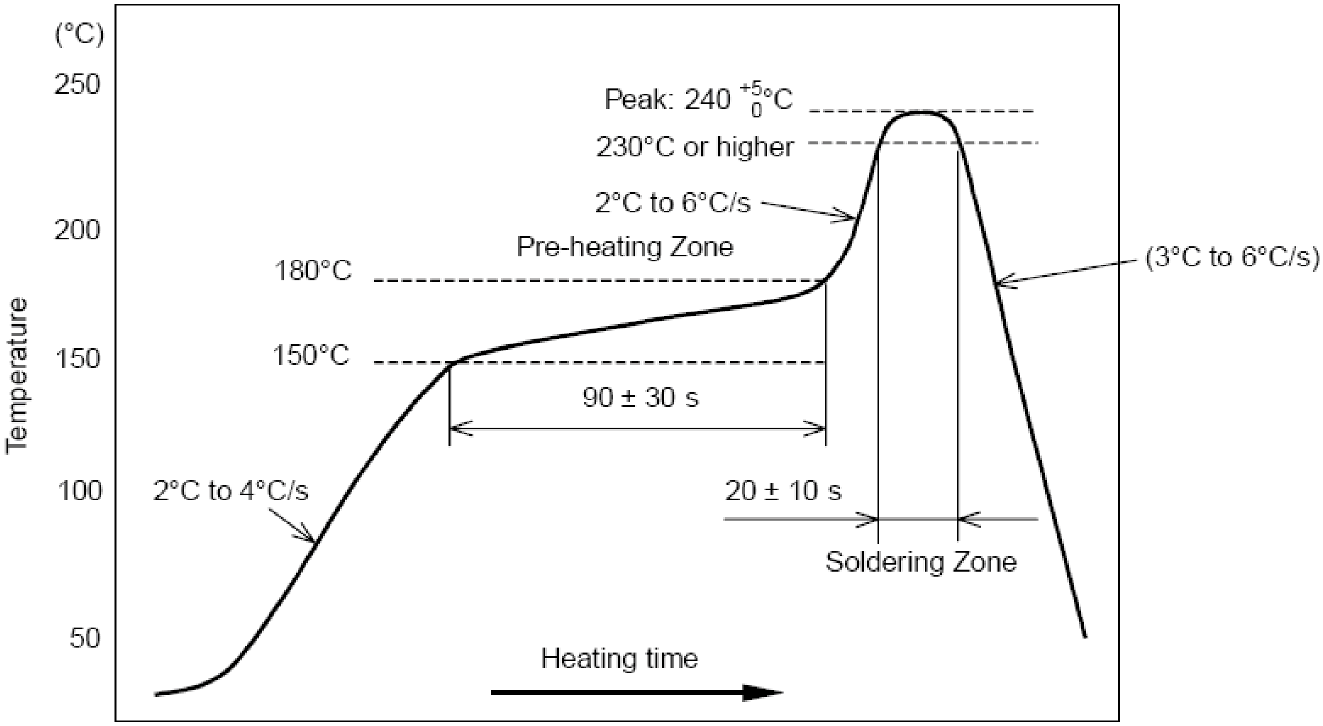


Figure 7-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)

8 Product and Documentation Support

8.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the CC3200MOD applications:

Software Development Tools: Code Composer Studio Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any CC3200MOD application.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the CC3200MOD platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.1 Firmware Updates

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in his or her module for production. To stay informed, sign up for the SDK Alert Me button on the tools page or www.ti.com/tool/cc3200sdk.

8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3200MOD and support tools (see Figure 8-1).

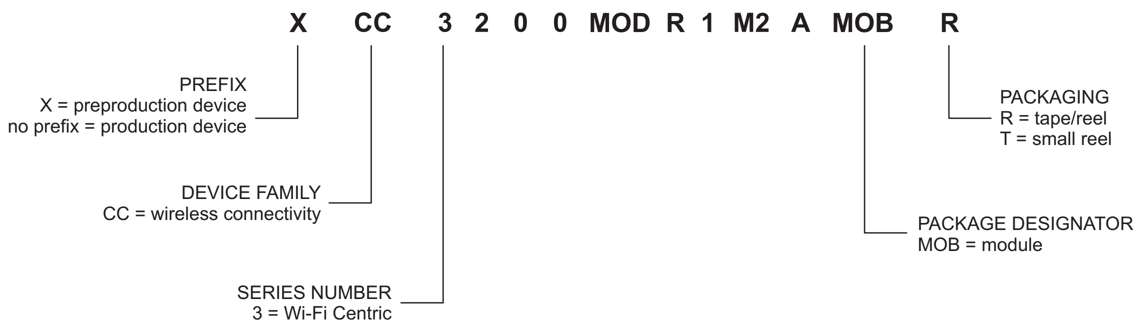


Figure 8-1. CC3200MOD Device Nomenclature

For orderable part numbers of CC3200MOD devices in the MOB package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.4 Trademarks

SimpleLink, E2E, Internet-on-a-chip, Code Composer Studio, DSP/BIOS, XDS are trademarks of Texas Instruments.
Macrocell is a trademark of Kappa Global Inc.
Wi-Fi CERTIFIED, Wi-Fi Direct are trademarks of Wi-Fi Alliance.
Wi-Fi is a registered trademark of Wi-Fi Alliance.
ZigBee is a registered trademark of ZigBee Alliance.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

Figure 9-1 shows the CC3200MOD module.

9.1 Mechanical Drawing

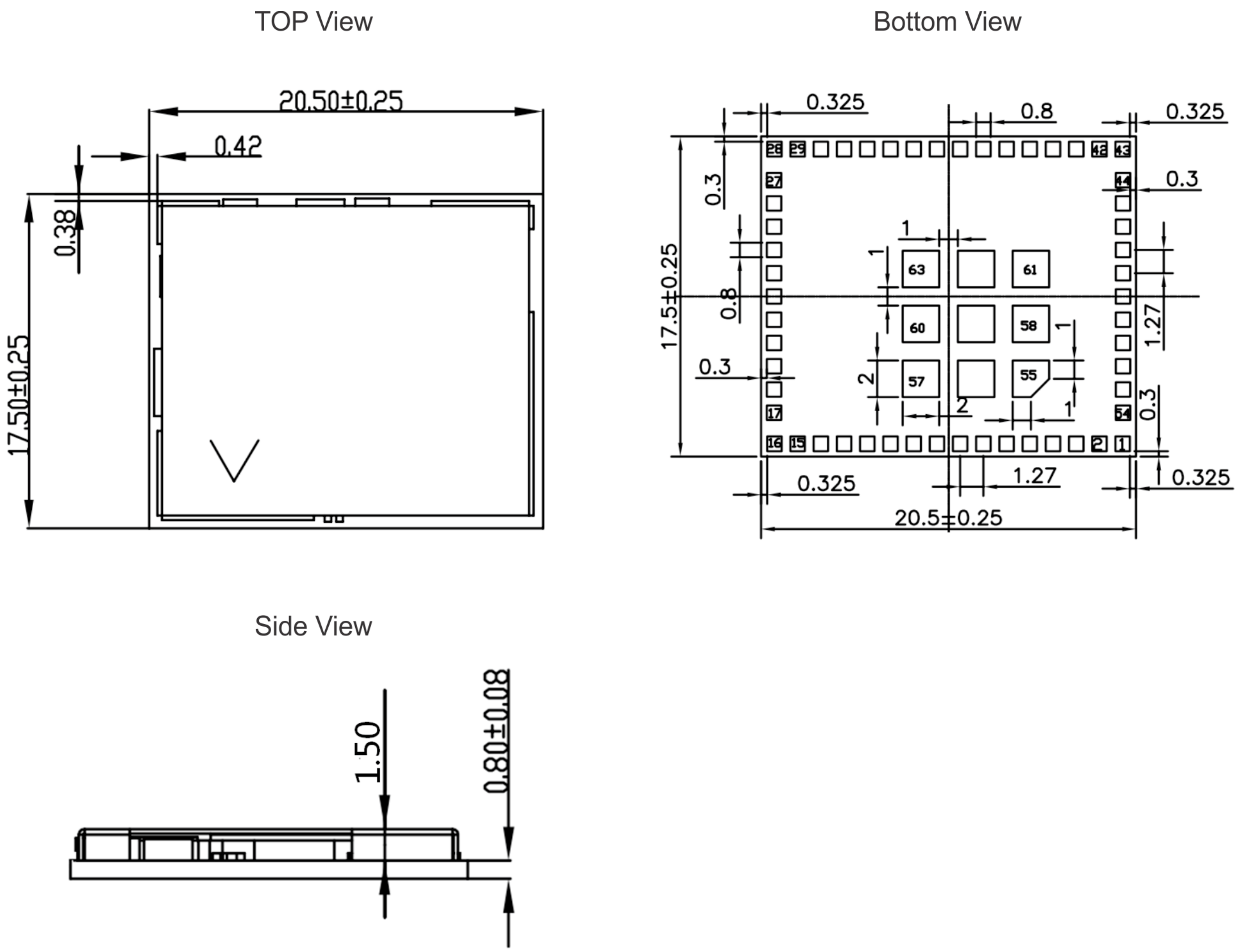


Figure 9-1. Mechanical Drawing

9.2 Package Option

We offer 2 reel size options for flexibility: a 1000-unit reel and a 250-unit reel.

9.2.1 Packaging Information

Orderable Device	Status (1)	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL, Peak Temp (3)	Op Temp (°C)	Device Marking(4) (5)
CC3200MODR1M2AMOBR	ACTIVE	MOB	63	1000	RoHS Exempt	Ni Au	3, 250°C	–20 to 70	CC3200MODR1M2AMOB
CC3200MODR1M2AMOBT	ACTIVE	MOB	63	250	RoHS Exempt	Ni Au	3, 250°C	–20 to 70	CC3200MODR1M2AMOB

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

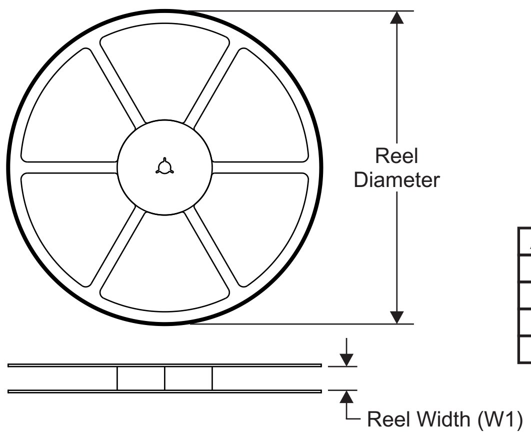
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

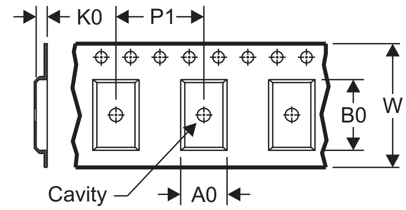
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release. In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

9.2.2 Tape and Reel Information

REEL DIMENSIONS

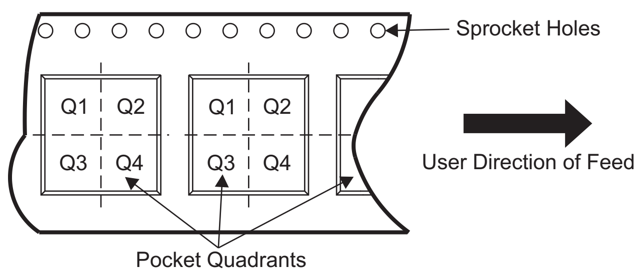


TAPE DIMENSIONS



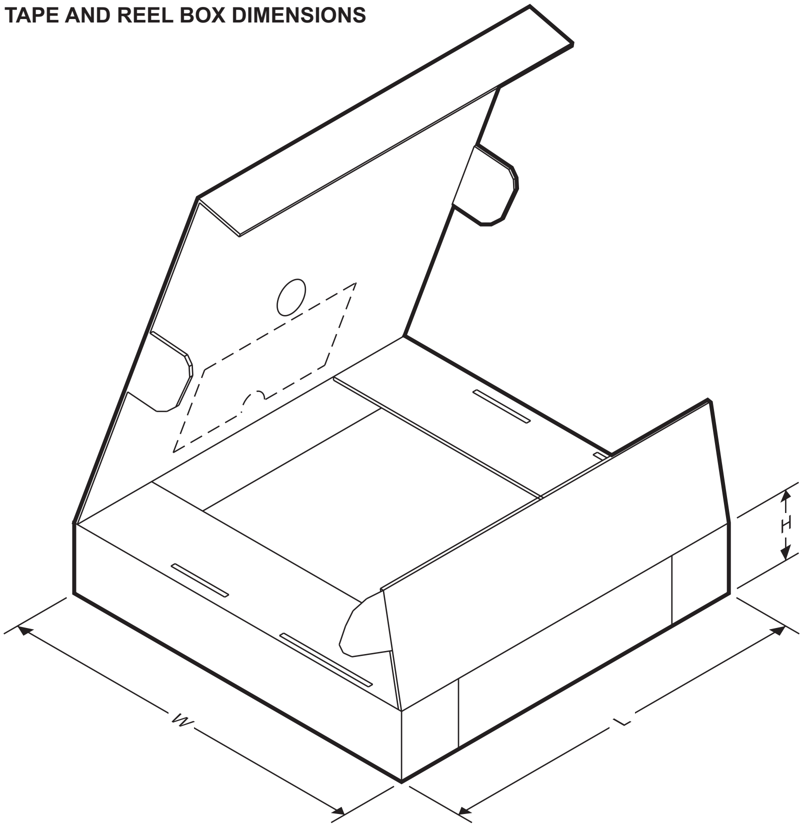
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3200MODR1M2AMOBR	MOB	63	1000	330.0±2.0	44.0	17.85±0.10	20.85±0.10	2.50±0.10	24.00±0.10	44.00±0.30	Q3
CC3200MODR1M2AMOBT	MOB	63	250	330.0±2.0	44.0	17.85±0.10	20.85±0.10	2.50±0.10	24.00±0.10	44.00±0.30	Q3

TAPE AND REEL BOX DIMENSIONS



Device	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3200MODR1M2AMOBR	MOB	63	1000	354.0	354.0	55.0
CC3200MODR1M2AMOBT	MOB	63	250	354.0	354.0	55.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3200MODR1M2AMOBR	ACTIVE			64	1000	TBD	Call TI	Call TI	-20 to 70		Samples
CC3200MODR1M2AMOBT	ACTIVE			64	250	TBD	Call TI	Call TI	-20 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.