



# REALTEK

## RTL8192E

### 802.11 b/g/n RTL8192E half miniCard

### DATASHEET



**Realtek Semiconductor Corp.**

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

[www.realtek.com.tw](http://www.realtek.com.tw)

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**USING THIS DOCUMENT**

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

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# 1. General Description

The Realtek RTL8192E is a highly integrated MIMO wireless LAN (WLAN) solution for the wireless high throughput 802.11n draft specification. It combines a MAC and 1T2R capable baseband in a single chip. When coupled with Realtek's RFIC's (RTL8256 at 2.4Ghz), the RTL8192E provides complete solution for a high throughput performance wireless client.

The RTL8192E baseband implements multiple input, multiple output (MIMO) orthogonal frequency division multiplexing (OFDM) with 1 transmit and 2 receive paths and is compatible with 802.11n Draft specification 2.0. Other features include two spatial streams transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20 MHz and 40 MHz bandwidth. Moreover, RTL8192E provides one spatial stream space-time block code (STBC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8192E also supports explicit sounding packet feedback that helps senders with beamforming capability. With 2 independent RF IC, RTL8192E can perform fast roaming without link interruption.

For legacy compatibility, direct sequence spread spectrum (DSSS), complementary code keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11n data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available along with complementary code keying to provide the data rates of 1, 2, 5.5 and 11Mbps with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provides the maximum data rate of 54 Mbps and 300 Mbps for IEEE 802.11b/g and 802.11n MIMO OFDM respectively.

The RTL8192E builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate the severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with maximal-ratio-combine (MRC) applying up to 2 receive paths are implemented. Robust interference detection and suppression are provided to protect against bluetooth, cordless phone, and microwave oven. Radar detection is supported to further protect RTL8192E from interference. Receive vector diversity for multi-stream application is implemented for efficient utilization of MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset and timing offset compensations are provided for the radio frequency front-end impairments. Selectable digital transmit and receiver FIR filters are provided to meet the requirement of transmit spectrum mask and to reject the adjacent channel interference, respectively.

The RTL8192E supports fast receiver automatic gain control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8192E MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as U-APSD, APSD, and MIMO power saving reduces the power wasted during idle time, and compensates for the extra power required to transmit MIMO OFDM. The RTL8192E provides simple legacy and 20Mhz/40Mhz co-existence mechanisms to ensure backward and network compatibility.

## 2. General Features

### General

14 x 14mm<sup>2</sup> 128-pin LQFP..

CMOS MAC and Baseband MIMO PHY Single Chip for IEEE 802.11b/g/n compatible WLAN

Complete 802.11n MIMO solution coupled with RTL8256 for 2.4G solution.

1x2 MIMO technology for extended reception robustness and exceptional throughput

Maximum PHY data rate up to 150Mbps using 20Mhz bandwidth, 300Mbps using 40Mhz bandwidth

Compatible with 802.11n draft 2.0 specification.

Backward compatible with 802.11b/g devices while operating at 802.11n data rates

200Mbps UDP throughput at 40Mhz mode.

### Host Interface

Complies with PCI Express™ Base Specification Revision 1.1

### Standards supported

802.11e QoS Enhancement (WMM, WMM-SA Client mode)

802.11h TPC, DFS, Spectrum Measurement

802.11k Radio Resource Measurement

802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services.

CCX

### MAC Features

Frame aggregation increase MAC efficiency (A-MSDU, A-MPDU)

Low latency Immediate High-Throughput Block Acknowledgement (HT-BA)

Long NAV for media reservation with CF-End for NAV release

PHY-level spoofing to enhance legacy compatibility

MIMO power saving mechanism

Channel management and co-existence

Multiple BSSID feature allowing RTL8192E to assume multiple MAC identity when used as wireless bridge

Supports Wake-On-WLAN via Magic Packet and wake-up frame

TXOP SIFS bursting guarantees multimedia bandwidth.

## Peripheral Interface

General Purpose Input/Output (8 pins)

4-wire EEPROM control interface (93C46 and 93C56)

4-wire RF control interface (RTL8256)

Configurable LED pins (2).

## PHY Features

IEEE 802.11n draft 2.0 MIMO OFDM

- 1 transmit and 2 receive paths (1T2R).
- 20MHz and 40MHz bandwidth transmission.
- Short Guard Interval (400ns).
- 1 spatial stream STBC transmission for extended coverage.
- Sounding packet.

DSSS with DBPSK and DQPSK, CCK modulations with long and short preamble.

OFDM with BPSK, QPSK, 16QAM, 64QAM, and 256QAM modulations. Convolutional coding rate: 1/2, 2/3, 3/4, and 5/6.

Maximum data rate 54Mbps in 802.11g and 300Mbps in 802.11n.

OFDM receive diversity with MRC using up to 4 receive paths. Switch diversity used for DSSS/CCK.

Hardware antenna diversity.

Selectable digital transmit and receiver FIR filters

Programmable scaling in transmitter and receiver to trade quantization noise against increasing probability of clipping.

Fast receiver automatic gain control (AGC).

On-chip ADC and DAC.



### 3. Application Diagram

#### 3.1. Single band 11n application

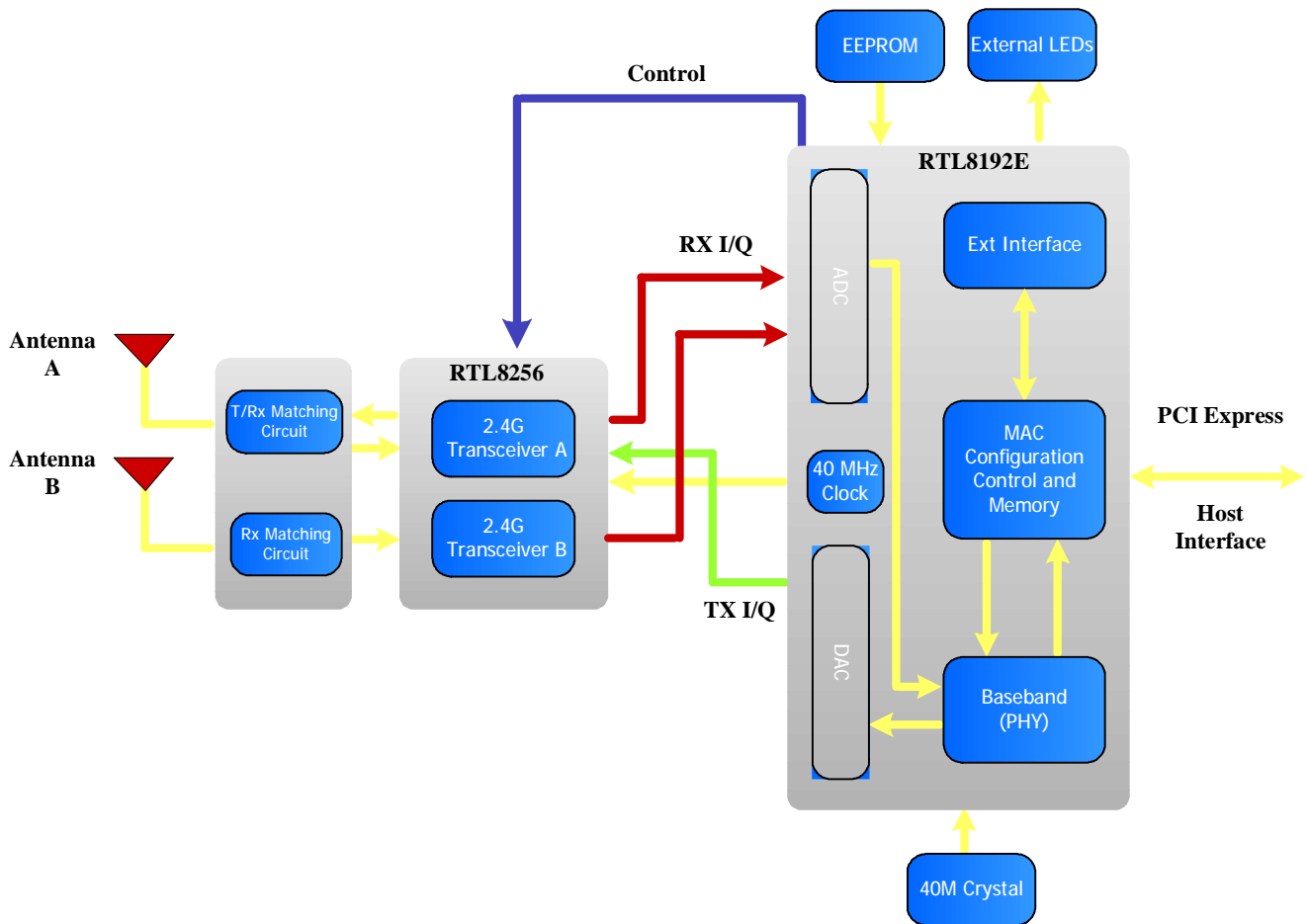


Figure 1. Single Band 11n Application Diagram

## 4. Pin Assignments

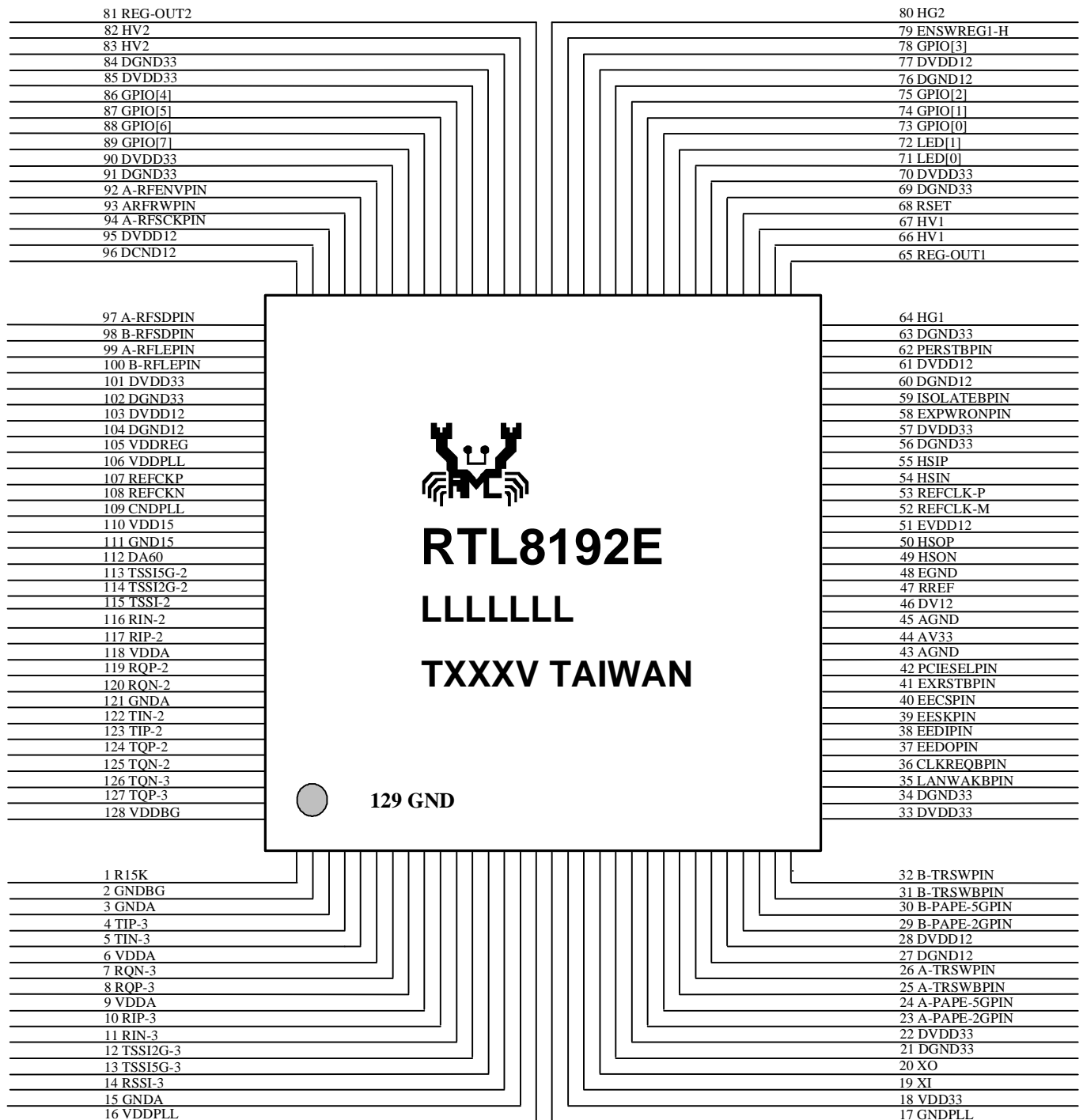


Figure 2. Pin Assignments

## 5. Pin Descriptions

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In such cases, the functions are separated with a '/' symbol. Refer to the Pin Assignments diagram on page 10 for a graphical representation.

The following signal type codes are used in the tables:

I: Input.

O: Output

T/S: Tri-State bi-directional input/output pin.

S/T/S: Sustained Tri-State.

O/D: Open Drain.

P: Power pin.

### 5.1. PCIE Transceiver Interface

**Table 1. PCIE Transceiver Interface**

Symbol	Type	Pin No	Description
HSIN/HSIP	I	54/55	Receiver differential pair
HSON/HSOP	O	49/50	Transmitter differential pair
REFCLK_N/ REFCLK_P	I	52/53	Reference clock differential pair
CLKREQB	O	36	Signal for Reference clock Enable
LANWAKEB	O	35	Signal for Link reactivation
PERSTB	I	62	Fundamental reset

### 5.2. EEPROM Interface

**Table 2. EEPROM Interface**

Symbol	Type	Pin No	Description
EESK	O	39	EESK in 93C46 (93C56) programming or auto-load mode.
EEDI	O	38	EEDI in 93C46 (93C56) programming or auto-load mode.
EEDO	I/O	37	EEDO in 93C46 (93C56) programming or auto-load mode.
EECS	O	40	EEPROM Chip Select. 93C46 (93C56) chip select.

### 5.3. Power Pins

**Table 3. Power Pins**

Symbol	Type	Pin No	Description
DVDD33	P	22, 33,57,70,85,90,101	+3.3V (Digital).
DVDD12	P	28,61,77,95,103	+1.2V (Digital)

Symbol	Type	Pin No	Description
VDDBG	P	128	+3.3V (Analog). For Bandgap and Bias
VDD33	P	18	+3.3V (Analog). For XTAL
VDDREG	P	105	+2.2V (Analog). For Voltage input of Built-In Regulator in AFE
VDDA	P	6,9,118	+1.5V (Analog). For Analog Power of AD/DA,T/RSSI of Left Corner AFE
VDD15	P	110	+1.5V (Analog). For Digital power of DAC and level shifter of Left Corner AFE
DGND33	P	21,34,56,63,69,84,91,102	Ground (Digital 3.3).
DGND12	P	27,60,76,96,104	Ground (Digital 1.2).
VDDPLL	P	16,106	+1.5V (Analog). For Analog Power of PLL.
GND A	P	3,15,121	Ground (Analog).
AGND	P	43,45,	Ground (Analog).
EGND	P	48	Ground.
GNDPLL	P	17,109	Ground.
GNDBG	P	2	Ground.
AV33	P	44	+3.3V (Analog).
DV12	P	46	+1.2V (Analog).
GND15	P	111	Ground.
EVDD12	P	51	Ground.
RREF	P	47	For Bandgap and Bias

## 5.4. LED Interface

**Table 4. LED Interface**

Symbol	Type	Pin No	Description
LED0, 1	O	71,72	LED Pins (Active low).

## 5.5. Switching Regulator

**Table 5. Switching Regulator**

Symbol	Type	Pin No	Description
HV1	I	66,67	Input DVDD33
HG1	I	64	DGND
REG_OUT1	O	65	Regulator output 1.2V
REG_OUT2	O	81	Regulator output 2.2V
HV2	I	82,83	Input DVDD33
HG2	I	80	DGND
ENSWREG_H	I	79	Built-In Switch Regulator Enable
RSET	I	68	External pull down reference resistor 96K ohm for switch regulator

## 5.6.Attachment Unit Interface

### 5.6.1. RF Chipset

RF chipset's register access is controlled by 4-wire serial interface consisting: Serial Clock Output (SCK), Serial Data Input/Output (SD), Serial Latch Enable (LE), and Serial Read/Write Select (RW). RF chipset contains two RF modules, thus uses two sets of 4-wire control interface, where the SCK and RW are shared. RTL8192E is capable of operating with 2 RF modules. The 4-wire control interface are labeled from A to B.

**Table 6. RTL8192E Attachment Interface with RF Chipset**

Symbol	Type	Pin No	Description	
REFCKP, REFCKN	O	107,108	Differential clock output to RF chip.	
A_PAPE_5GPIN	O	24	5GHz Transmit Power Amplifier Power Enable.	
A_PAPE_2GPIN	O	23	2.4GHz Transmit Power Amplifier Power Enable.	
A_TRSWPIN	O	26	Transmit/Receive path select.	
A_TRSWBPIN	O	25		
RF_A_CT RL	A_RFSD	O	94	Serial Clock Output.
	A_RFSD	I/O	97	Serial Data Input/Output.
	A_RFLE	O	99	Serial Latch Enable
	A_RFRW	O	93	Read/Write Select.
B_PAPE_5G	O	30	5GHz Transmit Power Amplifier Power Enable.	
B_PAPE_2G	O	29	2.4GHz Transmit Power Amplifier Power Enable.	
B_TRSW	O	32	Transmit/Receive path select.	
B_TRSWB	O	31	The TRSW select signal controls the direction of the Transmit/Receive switch.	
RF_B_CT RL	B_RFSD	I/O	98	Serial Data Input/Output.
	B_RFLE	O	100	Serial Latch Enable
TSSI5G_2	I	113	Input to the Transmit Power A/D Converter for 5GHz Transmit AGC Control.	
TSSI5G_3	I	13		
TSSI2G_2	I	114	Input to the Transmit Power A/D Converter for 2.4GHz Transmit AGC Control.	
TSSI2G_3	I	12		
RSSI_2	I	115	Analog Input to the Receive Power A/D Converter for Receive AGC Control.	
RSSI_3	I	14		
TIP_2	O	123	Baseband In-phase Output Data - differential positive signal for Path2	
TIN_2	O	122	Baseband In-phase Output Data - differential negative signal for Path2	
TIP_3	O	4	Baseband In-phase Output Data - differential positive signal for Path3	
TIN_3	O	5	Baseband In-phase Output Data - differential negative signal for Path3	
TQP_2	O	124	Baseband Quadrature Output Data - differential positive signal for Path2	
TQN_2	O	125	Baseband Quadrature Output Data - differential negative signal for Path2	
TQP_3	O	127	Baseband Quadrature Output Data - differential positive signal for Path3	
TQN_3	O	126	Baseband Quadrature Output Data - differential negative signal for Path3	
RIP_2	I	117	Analog input for In -phase received data – differential positive signal for Path2	
RIN_2	I	116	Analog input for In -phase received data – differential negative signal for Path2	
RIP_3	I	10	Analog input for In -phase received data – differential positive signal for Path3	

Symbol	Type	Pin No	Description
RIN_3	I	11	Analog input for In -phase received data – differential negative signal for Path3
RQP_2	I	119	Analog input for Quadrature received data – differential positive signal for Path2
RQN_2	I	120	Analog input for Quadrature received data – differential negative signal for Path2
RQP_3	I	8	Analog input for Quadrature received data – differential positive signal for Path3
RQN_3	I	7	Analog input for Quadrature received data – differential negative signal for Path3
A_RFENV	O	92	RF Chip Enable of RF A&B

## 5.7. Clock and Other Pins

**Table 7. Clock and Other Pins**

Symbol	Type	Pin No	Description
XI	I	19	40MHz OSC Input. 40Mhz Crystal input.
XO	I	20	40Mhz Crystal input.
DA60	O	112	6 bit analog signal for PHY debug
R12K	I	1	External pull down reference resistor 12K ohm for BandGap
EXRSTB	I	41	Debug purpose manual reset pin. Not connected on board.
EXPWRON	I	58	Debug purpose. Pull high to clear reset state.
PCIESEL	I	42	Weakly pull high at power on.
GPIO0	I/O	73	There are 8 General Purpose Input/Output pins. Some are used for power-on latch purposes.
GPIO1	I/O	74	
GPIO2/AuxPwr	I/O	75	Weakly pull high at power on to indicate the presence of the auxiliary power on the mainboard
GPIO3/Sel9356	I/O	78	Weakly pull high at power on to indicate the choice of EEPROM is 93C56. If left not connected, RTL8192E assumes the EEPROM in use is 93C46.
GPIO4	I/O	86	
GPIO5	I/O	87	
GPIO6	I/O	88	
GPIO7	I/O	89	

## 6. Electrical and Thermal Characteristics

### 6.1. Temperature Limit Ratings

Table 8. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

### 6.2. DC Characteristics

Below is a description of the general DC specifications for the RTL8192E.

Table 9. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
DVDD33	3.3V I/O Supply Voltage		2.97	3.3	3.63	V
DVDD12	1.2V Core Supply Voltage		1.08	1.2	1.32	V

## 7. Mechanical Dimensions

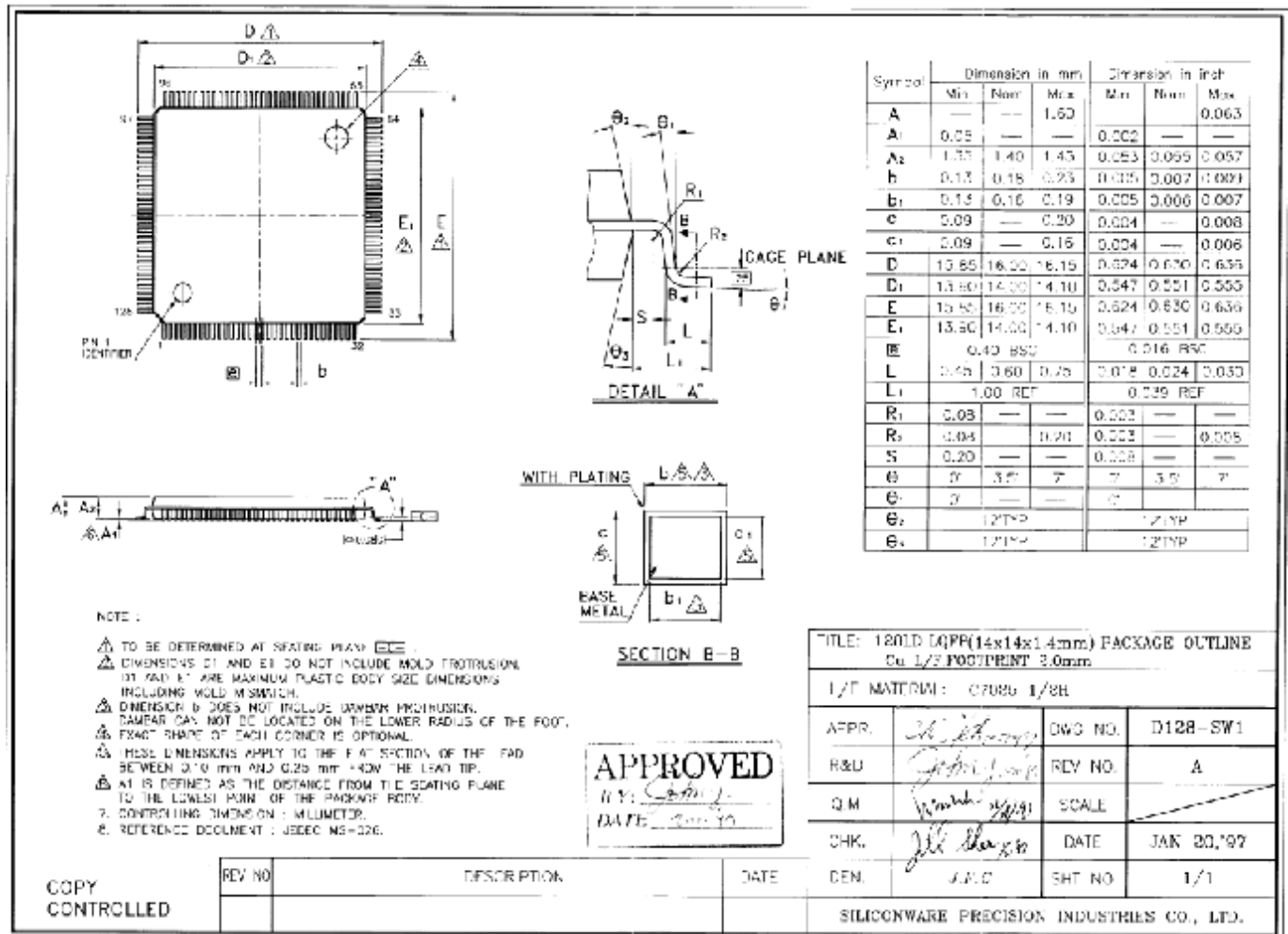


Figure 4. RTL8192E Mechanical Specification



## 8. Ordering Information

**Table 8. Ordering Information**

Part Number	Package	Status
RTL8192E-GR	LQFP-128, Green package	MP

### Functional Specifications

<b>POWER SUPPLY</b>	DC 3.2~3.5V from host equipment
<b>MODULATION TYPE</b>	CCK, DQPSK, DBPSK for DSSS 64QAM, 16QAM, QPSK, BPSK for OFDM
<b>MODULATION TECHNOLOGY</b>	DSSS, OFDM
<b>TRANSFER RATE</b>	802.11b: 11 / 5.5 / 2 / 1Mbps 802.11g: 54 / 48 / 36 / 24 / 18 / 12 / 9 / 6Mbps Draft 802.11n (20MHz, 800ns GI): 130 / 117 / 104 / 78 / 65 / 58.5 / 52 / 39 / 26 / 19.5 / 13 / 6.5Mbps Draft 802.11n (40MHz, 800ns GI): 270 / 243 / 216 / 162 / 135 / 121.5 / 108 / 81 / 54 / 40.5 / 27 / 13.5Mbps Draft 802.11n (20MHz, 400ns GI): 144.444 / 130 / 115.556 / 86.667 / 72.2 / 65 / 57.8 / 57.778 / 43.333 / 43.3 / 28.9 / 28.889 / 21.7 / 14.444 / 14.4 / 7.2Mbps Draft 802.11n (40MHz, 400ns GI): 300 / 270 / 240 / 180 / 150 / 135 / 120 / 90 / 60 / 45 / 30 / 15Mbps
<b>FREQUENCY RANGE</b>	2400MHz ~ 2483.5MHz
<b>NUMBER OF CHANNEL</b>	11 for 802.11b, 802.11g, draft 802.11n (20MHz) 7 for draft 802.11n (40MHz)

### Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

**IMPORTANT NOTE:****FCC Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IEEE 802.11b or 802.11g operation of this product in the U.S.A. is firmware-limited to channels 1 through 11.

**This device is intended only for OEM integrators under the following conditions:**

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna,
- 3) For all products market in US, OEM has to limit the operation channels in CH1 to CH11 for 2.4G band by supplied firmware programming tool. OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change. As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**IMPORTANT NOTE:** In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

**End Product Labeling :**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID: TX2-RTL8192EHMC".

**Manual Information To the End User :**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

**Industry Canada Statement**

This device complies with RSS-210 of the Industry Canada Rules. Operation is subject to the following two conditions:

- 1) this device may not cause interference and
- 2) this device must accept any interference, including interference that may cause undesired operation of the device

This device has been designed to operate with an antenna having a maximum gain of 3.95 dBi.

Antenna having a higher gain is strictly prohibited per regulations of Industry Canada. The required antenna impedance is 50 ohms.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the EIRP is not more than required for successful communication.

**IMPORTANT NOTE:****IC Radiation Exposure Statement:**

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

**Taiwan 警語：**

經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前項合法通信，指依電信法規定作業之無線電通信。

低功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

本模組於取得認證後將依規定於模組本體標示審合格籤，並要求平台上標示「本產品內含射頻模組：ID編號」

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**Realtek Semiconductor Corp.****Headquarters**

No. 2, Innovation Road II, Hsinchu Science Park,

Hsinchu, 300, Taiwan, R.O.C.

Tel: 886-3-5780211 Fax: 886-3-5776047

[www.realtek.com.tw](http://www.realtek.com.tw)