1 Features

- STM32MP157 Arm®-based dual Cortex®-A7 32 bits + Cortex®-M4 32 bits MPU in LFBGA448 package
- ST PMIC STPMIC1
- 2 × 4-Gbit DDR3L, 16 bits, 533 MHz
- 2 × 512-Mbit Quad-SPI Flash
- 32-Gbit eMMC v5.0
- 8-Gbit SLC NAND, 8 bits, 8-bit ECC, 4-KB PS
- 1-Gbit/s Ethernet (RGMII) compliant with IEEE-802.3ab
- USB Host 4-port hub
- USB OTG HS
- CAN FD
- 5.5" TFT 720×1280 pixels with LED backlight, MIPI DSI℠ interface, and capacitive touch panel
- SAI audio codec
- 5-megapixel, 8-bit camera
- 4 × ST-MEMS digital microphones
- Smartcard
- microSD™ card
- 2 user LEDs
- 2 user and reset push-buttons, 1 wake-up button
- 4-direction joystick with selection button
- 5 V / 4 A power supply
- Board connectors:
  - Ethernet RJ45
  - 4 × USB Host Type-A
  - USB OTG Micro-AB
  - SPDIF RCA input and output
  - CAN FD
  - Stereo headset jack including analog microphone input
  - Audio jack for external speakers
  - Motor control
  - External I^2C
  - LTDC
  - Trace, JTAG, RS-232
  - GPIO expansion connector (Raspberry Pi® shields capability)
  - MEMS-microphone daughterboard expansion connector
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: Virtual COM port and debug port
- STM32CubeMP1 and full mainline open-source Linux® STM32 MPU OpenSTLinux distribution (such as STM32MP1Starter) software and examples
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR™, Keil®, GCC-based IDEs

STM32 Arm Cortex MPUs are based on the Arm® Cortex®-A and Cortex®-M processors.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order an STM32MP157 Eval board, refer to Table 1. List of available products. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. List of available products

Order code	Board reference	Target STM32	Differentiating feature
STM32MP157A-EV1	• MB1262: mother board • MB1263: MPU subsystem daughterboard • MB1230: DSI display board • MB1379: camera board	STM32MP157AAA3	Basic security.
STM32MP157C-EV1		STM32MP157CAA3	Secure Boot and cryptography.

2.1 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference design or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (for illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

2.2 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

STM32MP1XXY-EVZ	Description	Example: STM32MP157C-EV1
STM32MP1	MPU series in STM32MP1 32-bit MPUs	STM32MP1 Series
XX	MPU product line in the series	STM32MP157 line
Y	Security option: • A: basic security • C: Secure Boot and cryptography	Secure Boot and cryptography
EVZ	Eval board configuration • EV1: with PMIC	PMIC

The order code is mentioned on a sticker placed on the top side of the board.

3 Development environment

3.1 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit, or macOS®
- USB Type-A to Micro-B cable

Note: macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.

3.2 Development toolchains

- Keil® MDK-ARM (see note)
- IAR™ EWARM (see note)
- GCC-based IDEs
- GCC

Note: On Windows® only.

3.3 Demonstration software

The STM32 MPU OpenSTLinux distribution and STM32CubeMP1 base demonstration software is preloaded in the microSD™ for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper should be fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered

5 Delivery recommendations

Before the first use, make sure that, no damage occurred to the board during shipment and no socketed components are loosen in their sockets or fallen into the plastic bag.

In particular, pay attention to the following components:

1. MB1263 daughterboard connected to the MB1262 mother board
2. microSD card in its MB1263/CN9 receptacle
3. LCD MB1230 daughterboard in MB1262/CN19 DSI connector, and screw, spacer and nut are in place
4. Camera module MB1379 board in MB1262/CN7 connector, and screw, spacer and nut are in place

For product information related with STM32MP157xAA3 microcontroller, visit *www.st.com* website.

6 Hardware layout and configuration

The STM32MP157x-EV1 Evaluation board is designed around the STM32MP157xAA3 target microcontroller in LFBGA 448-pin package. Figure 3 illustrates the STM32MP157x-EV1 hardware block diagram. Figure 4 shows the location of main components on the Evaluation board.

Figure 3. **STM32MP157x-EV1 hardware block diagram**

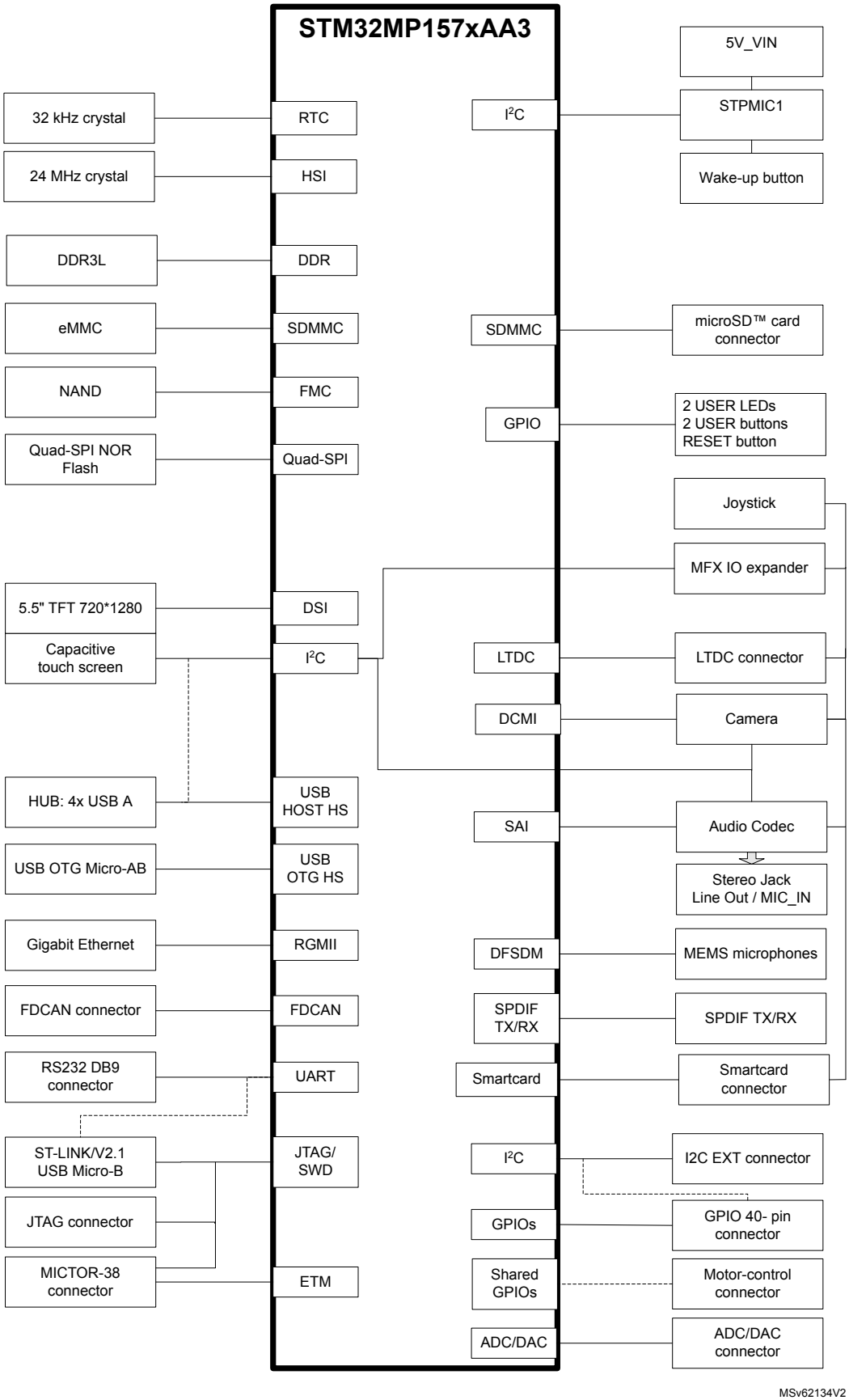
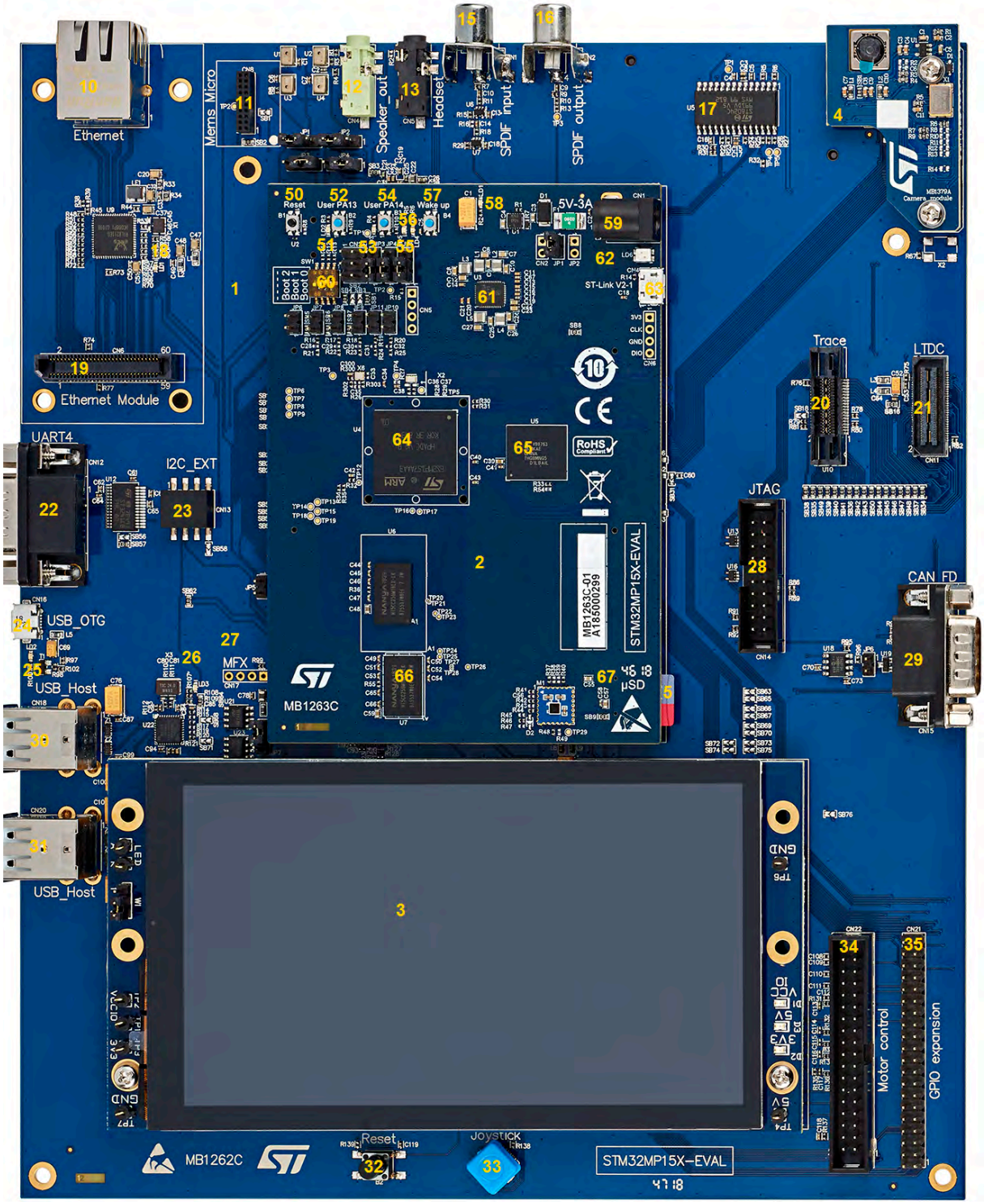


Figure 4. **STM32MP157x-EV1 board overview**



Note: Numbers in yellow refer to positions explained in Table 4, Table 5, and Table 6.

Table 4. STM32MP157x-EV1 overview

Position	Description
1	MB1262 mother board
2	MB1263 daughterboard
3	MB1230 DSI (MIPI® standard) 720p display
4	MB1379 daughterboard camera
5	microSD™ card

Table 5. MB1263 daughterboard overview

Position	Description	Position	Description
50 (**B1**)	Reset button	59 (**CN1**)	MB1263 power 5 V-3 A
51 (**LD2**)	User LED (red)	60 (**SW1**)	Boot mode selection
52 (**B2**)	User button (PA13)	61 (**U3**)	PMIC (STPMIC1A)
53 (**LD3**)	User LED (green)	62 (**LD6**)	ST-Link LED (bicolor)
54 (**B3**)	User button (PA14)	63 (**CN4**)	USB micro-B (ST-Link V2-1)
55 (**LD5**)	User LED (blue)	64 (**U4**)	STM32MP157xAA3 LFBGA448
56 (**LD4**)	User LED (orange)	65 (**U5**)	eMMC
57 (**B4**)	Wakeup button	66 (**U6/U7**)	2 x DDR3L 16 bits
58 (**LD1**)	Power LED (green)	67 (**µSD**)	microSD 3.0 card (back side slot)

Table 6. MB1262 mother board overview

Position	Description	Position	Description
10 (**CN3**)	Ethernet	11 (**CN8**)	Microphone MEMS daughterboard connector
12 (**CN4**)	Speaker audio output	13 (**CN5**)	Headset audio output
14 (**U8**)	Audio codec (Wolfson WM8994)	15 (**CN1**)	SPDIF RX
16 (**CN2**)	SPDIF TX	17 (**U5**)	Smartcard (back side slot)
18 (**LD1**)	Ethernet LED (green)	19 (**CN6**)	Ethernet daughterboard connector
20 (**U10**)	Trace connector	21 (**CN11**)	LTDC LCD TFT Display Controller (STM32 specific) connector
22 (**CN12**)	RS232 (UART4)	23 (**CN13**)	External E2P connector
24 (**CN16**)	USB micro-AB (USB OTG)	25 (**LD2**)	USB OTG LED (green)
26 (**LD3**)	USB Type-A port LED (red)	27 (**CN17**)	MFX header 4 pins
28 (**CN14**)	JTAG connector	29 (**CN15**)	CAN FD
30 (**CN18**)	2 USB Type-A port (host)	31 (**CN20**)	2 USB Type-A port (host)
32 (**B2**)	Reset button	33 (**B1**)	Joystick
34 (**CN22**)	Motor control connector	35 (**CN21**)	GPIO expansion connector
4 (**CN7**)	Camera sensor connector	-	-

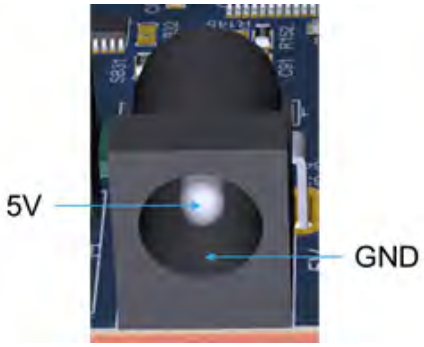
6.1 Power supply management

6.1.1 5 V power supply

STM32MP157x-EV1 Evaluation board is designed to be powered from the 5 V DC power supply provided in the package.

MB1263/LD1 Green LED turns on when this power supply is connected to the power jack MB1263/CN1.

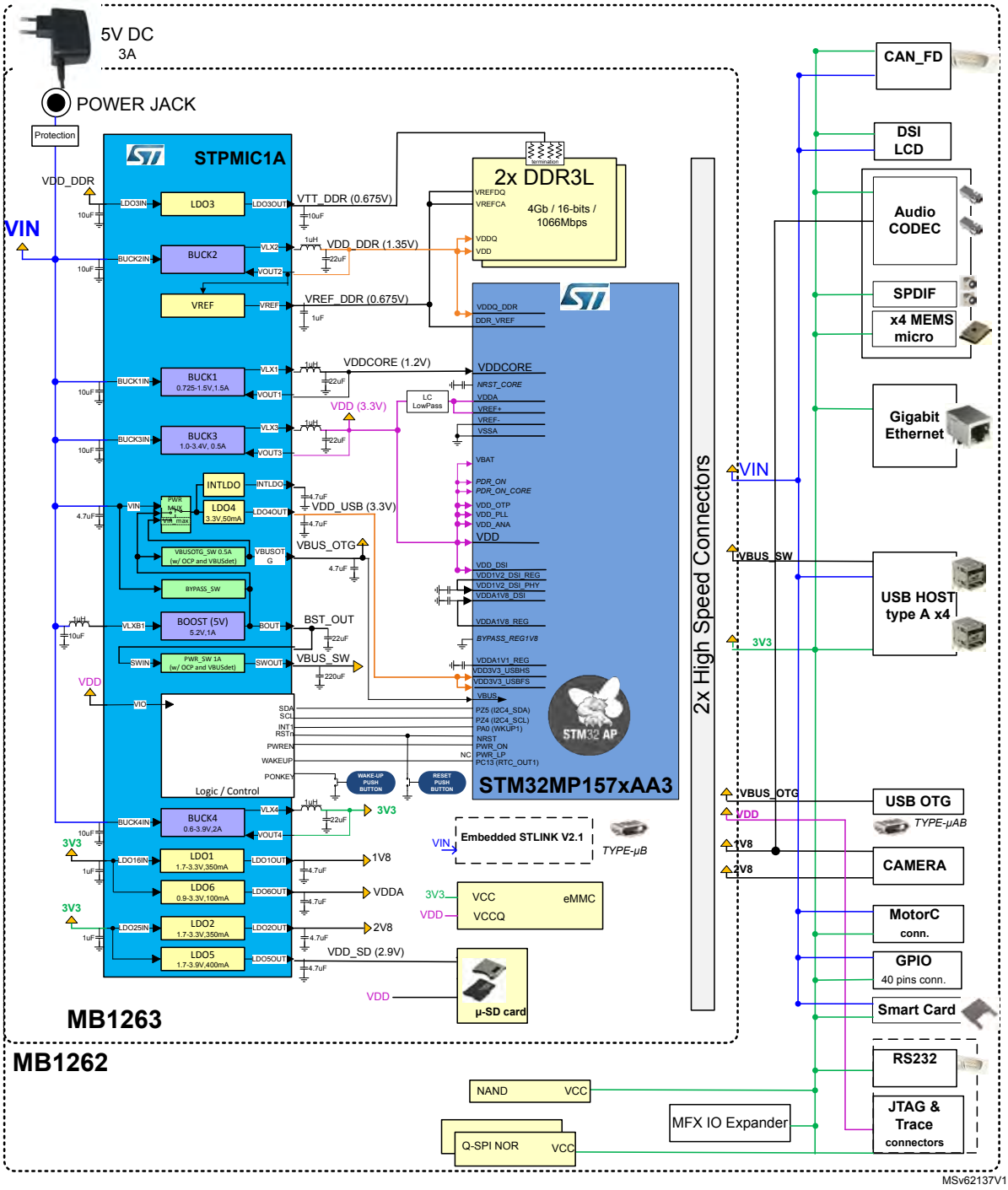
Figure 5. 5 V power supply connector: MB1263/CN1



6.1.2 Platform power tree

All supply lines required for the operation of the components on STM32MP157x-EV1 are derived from the 5 V power source. Indeed this 5 V power source is the input supply of the STPMIC1 that distributes then all the supplies to the sub-systems as described in the power tree Figure 6.

Figure 6. **STM32MP157x-EV1platform power tree**



6.1.3 STPMIC1

For general information concerning the STPMIC1, please refer to STPMIC1 datasheet at the *www.st.com* website.

6.2 Clocks

Two clocks are available on STM32MP157x-EV1 for STM32MP157xAA3 target microcontroller.

6.2.1 LSE clock

- External 32.768 kHz crystal

6.2.2 HSE clock

- External 24 MHz crystal

6.3 Reset sources

The reset signal of the STM32MP157x-EV1 platform is active low.

Sources of the platform reset are:

- Two reset buttons MB1263/B1 and MB1262/B2 (BLACK buttons)
- STM32MP157xAA3: internal voltage monitor, SW request or Watchdog
- STPMIC1
- JTAG/SWD connector MB1262/CN14
- ETM Trace Mictor-38 connector MB1262/U10
- Embedded ST-LINK/V2-1

The STM32MP157xAA3 also drives a sub system reset, SUB_NRST signal on PD10 IO, to the peripherals: USB Host Hub, MFX, Ethernet, and RGB_LTDC connector.

6.4 User buttons and LEDs

The Table 7 describes the HW configuration for the user buttons and LEDs

Table 7. HW configuration for the user buttons and LEDs

IO	LED color and label	Button label
PD8	PD8 is connected to the ORANGE LD4. Active High	-
PD9	PD9 is connected to the BLUE LD5. Active High	-
PA13	PA13 is connected to RED LD2. Active Low	User PA13
PA14	MFX_IO13 is connected to ORANGE LED LD7. Active Low	User PA14

6.5 Physical input devices: buttons

The STM32MP157x-EV1 board provides a number of input devices for physical human control.

These are:

- Two Reset buttons (MB1263/B1 and MB1262/B2)
- Four-way joystick controller with select key (MB1262/B1)
- Wake-up button (MB1263/B4)

Table 8. Physical user devices: buttons

Devices	Purpose/IO
Wakeup button (MB1263/B4)	Awakes the platform from low-power modes. Connected to STPMIC1A PONKEY, which generates a wake-up signal on STM32MP1 PA0
Reset buttons (MB1263/B1 or MB1262/B2)	NRST signal
JOY_CENTER: Joystick select key (MB1262/B1 pin2)	MFX_IO0
JOY_DOWN: Joystick down direction (MB1262/B1 pin3)	MFX_IO1

Devices	Purpose/IO
JOY_LEFT: Joystick left direction (MB1262/B1 pin1)	MFX_IO2
JOY_RIGHT: Joystick right direction (MB1262/B1 pin6)	MFX_IO3
JOY_UP: Joystick up direction (MB1262/B1 pin4)	MFX_IO4

6.6 Boot options

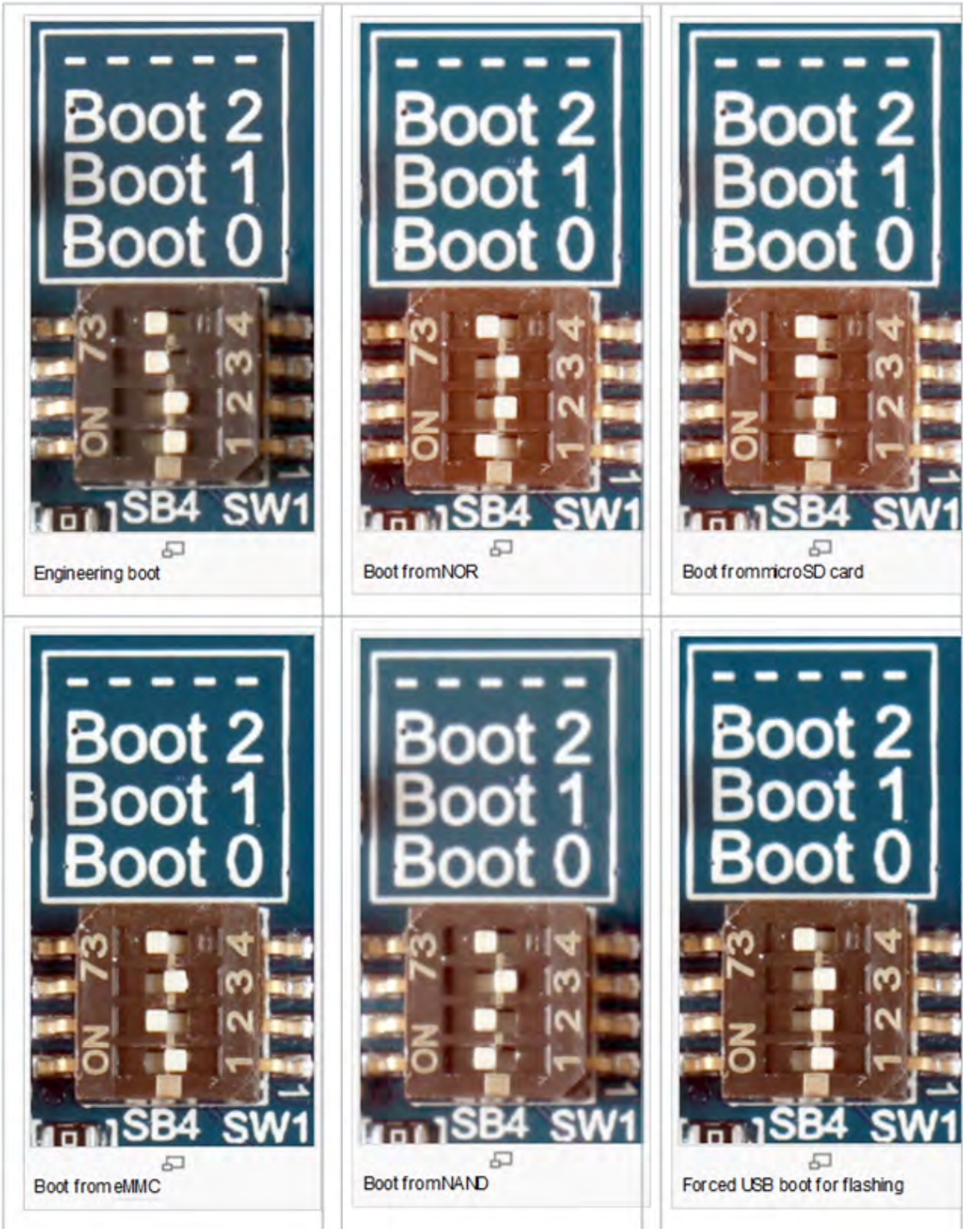
The STM32MP157x-EV1 board may boot from different sources as described in Table 9.

Table 9. HW configuration for the BOOT mode MB1263/SW1

Boot Mode	BOOT2	BOOT1	BOOT0
Serial-NOR	0	0	1
uSD card	1	0	1
eMMC	0	1	0
NAND	0	1	1
UART and USB	0	0	0
	1	1	0
Reserved	1	0	0

The boot related switches (MB1263/SW1) must be configured as illustrated by one of the following pictures:

Figure 7. **STM32MP157x-EV1 boot related switch configuration**



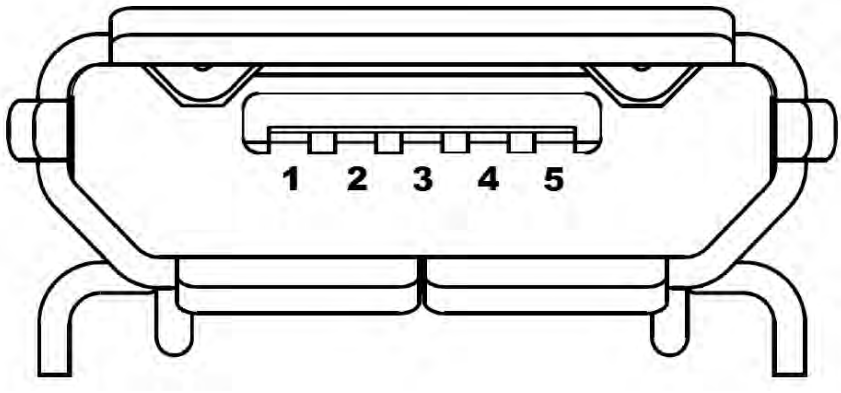
6.7 Embedded ST-LINK/V2-1

The STLINK-V2.1 programming and debugging tool is integrated in the STM32MP157x-EV1 Evaluation board. The embedded STLINK-V2.1 supports JTAG, SWD and VCP for the target STM32 MPU devices.

For information about debugging and programming features refer to STLINK-V2.1 in-circuit debugger/ programmer, User manual (UM1075) available on *www.st.com*, which describes in details all the STLINK-V2.1 features.

Figure 8 shows the STLINK USB µB connector pinout MB1263/CN4.

Figure 8. STLINK USB µB connector pinout MB1263/CN4



MSv46073V1

Table 10 describes STLINK USB µB connector pinout MB1263/CN4.

Table 10. STLINK USB µB connector pinout MB1263/CN4

Pin	Board function	STLINK STM32 pin
1	VBUS Power	-
2	DM	PA11
3	DP	PA12
4	ID	GND
5	GND	GND

As current consumption of the EVAL exceeds permissible current on USB, it is not possible to power the boards through the STLINK-V2.1 USB. To use the STLINK-V2.1 for programming and debugging, it is mandatory to power the board first using the 5V power supply, then connect the STLINK-V2.1 USB cable to the PC. Proceeding this way the USB enumeration succeed thanks to the external power source.

The user must respect the following power sequence procedure:

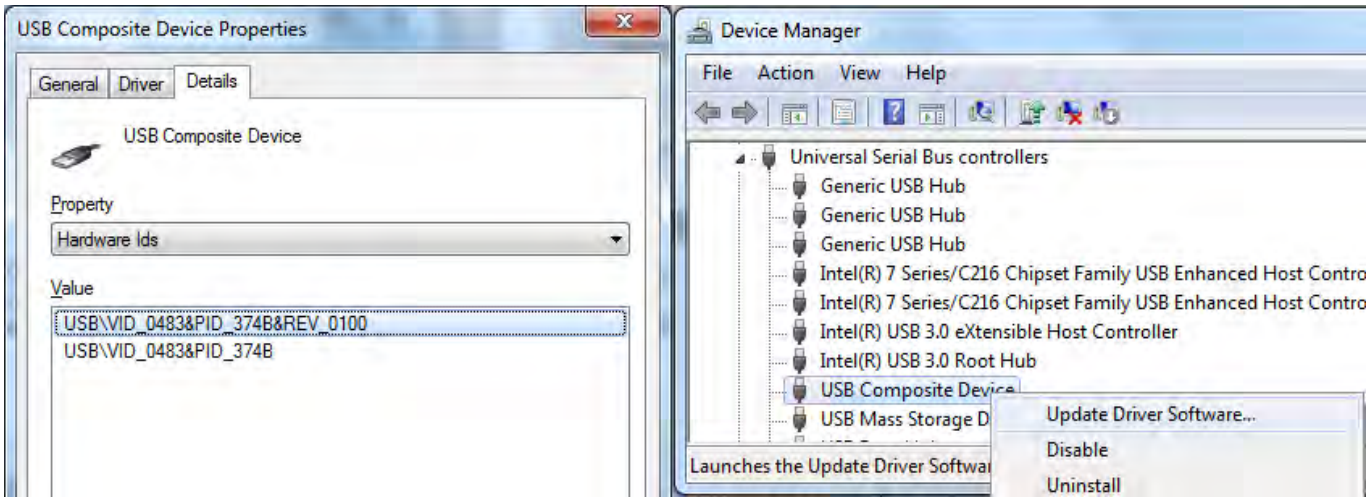
1. Check that MB1263/JP1 is OFF, MB1263/JP4 [2-3] and JP5 [2-3] are ON to connect UART4 as STLINK VCP.
2. Connect the 5 V power source, MB1263/LD1 LED turns green, MB1263/LD6 flashes red.
3. Connect the PC to USB connector MB1263/CN4, MB1263/LD6 is red and becomes green once the connection with the STLINK is established.

6.7.1 Drivers

Before connecting STM32MP157x-EV1 to a Windows (XP, 7, 8 10) PC via USB, a driver for ST-LINK/V2-1 must be installed. It may be downloaded from *www.st.com*.

In case the STM32MP157x-EV1 Evaluation board is connected to the PC before installing the driver, the Windows device manager may report some USB devices found on STM32MP157x-EV1as “Unknown”. To recover from this situation, after installing the dedicated driver downloaded from *www.st.com*, the association of “Unknown” USB devices found on STM32MP157x-EV1 to this dedicated driver must be updated in the device manager manually. It is recommended to proceed using USB Composite Device line, as shown in Figure 9.

Figure 9. **USB composite device**



6.7.2 ST-LINK/V2-1 firmware upgrade

For its own operation, ST-LINK/V2-1 employs a dedicated MCU with Flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance. The firmware may evolve during the life span of STM32MP157x-EV1 to include new functionality, fix bugs or support new target microcontroller families. It is therefore recommended to keep ST-LINK/V2-1 firmware up to date. The latest version is available from *www.st.com*.

6.8 ETM TRACE Mictor-38 connector

The Mictor-38 connector MB1262/U10 may output trace signals used for debug, as well as JTAG signals.
Table 11 describes the HW configuration for the TRACE function.

Table 11. **HW configuration for the TRACE connector MB1262/U10**

IO	Bridge	Setting(1)	Comment
PI14	SB38	**ON**	**PI14 may be used for the trace function TRACE CLK**
		OFF	PI14 is not connected to Trace PI14 may be used for LTDC CLK
PI12	SB43	**ON**	**PI12 may be used for the trace function TRACE_D0**
		OFF	PI12 is not connected to Trace PI12 may be used for LTDC HSYNC
PI13	SB42	**ON**	**PI13 may be used for the trace function TRACE_D1**
		OFF	PI13 is not connected to Trace PI13 may be used for LTDC VSYNC
PJ5	SB36	**ON**	**PJ5 may be used for the trace function TRACE_D2**
		OFF	PJ5 is not connected to Trace PJ5 may be used forLTDC_R6
PJ6	SB41	**ON**	**PJ6 be used for the trace function TRACE_D3**
		OFF	PJ6 is not connected to Trace PJ6 may be used for LTDC_R7
PK1	SB40	**ON**	**PK1 may be used for the trace function TRACE_D4**
		OFF	PK1 is not connected to Trace PK1 may be used for LTDC_G6

IO	Bridge	Setting[1]	Comment
PK2	SB39	**ON**	**PK2 may be used for the trace function TRACE_D5**
		OFF	PK2 is not connected to Trace PK2 may be used for LTDC_G7
PK5	SB49	**ON**	**PK5 may be used for the trace function TRACE_D6**
		OFF	PK5 is not connected to Trace PK5 may be used for LTDC_B6
PK6	SB35	**ON**	**PK6 may be used for the trace function TRACE_D7**
		OFF	PK6 is not connected to Trace PK6 may be used for LTDC_B7
PJ0	SB34	**ON**	**PJ0 may be used for the trace function TRACE_D8**
		OFF	PJ0 is not connected to Trace PJ0 may be used for LTDC_R1
PJ1	SB37	**ON**	**PJ1 may be used for the trace function TRACE_D9**
		OFF	PJ1 is not connected to Trace PJ1 may be used for LTDC_R2
PJ2	SB48	**ON**	**PJ2 may be used for the trace function TRACE_D10**
		OFF	PJ2 is not connected to Trace PJ2 may be used for LTDC_R3
PJ3	SB47	**ON**	**PJ3 may be used for the trace function TRACE_D11**
		OFF	PJ3 is not connected to Trace PJ3 may be used for LTDC_R4
PJ4	SB46	**ON**	**PJ4 may be used for the trace function TRACE_D12**
		OFF	PJ4 is not connected to Trace PJ4 may be used for LTDC_R5
PJ7	SB45	**ON**	**PJ7 may be used for the trace function TRACE_D13**
		OFF	PJ7 is not connected to Trace PJ7 may be used for LTDC_G0
PJ8	SB44	**ON**	**PJ8 may be used for the trace function TRACE_D14**
		OFF	PJ8 is not connected to Trace PJ8 may be used for LTDC_G1
PJ9	SB50	**ON**	**PJ9 may be used for the trace function TRACE_D15**
		OFF	PJ9 is not connected to Trace PJ9 may be used for LTDC_G2

1. *Default configuration is shown in **bold***

Figure 10 shows the TRACE Mictor-38 connector

Figure 10. **TRACE Mictor-38 connector: MB1262/U10**

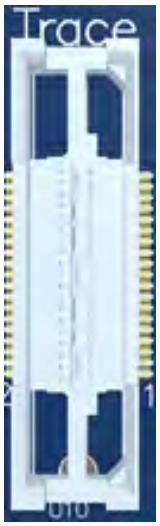


Table 12 describes the MICTOR-38 connector pinout for TRACE and JTAG signals.

Table 12. **TRACE MICTOR-38 connector pinout: MB1262/U10**

Board function	Pin	Pin	Board function
NC	1	2	NC
NC	3	4	NC
GND	5	6	TRACE_CLK
Pulldown	7	8	Pulldown
NRST	9	10	Pulldown
TDO/SWO	11	12	VDD
Pulldown	13	14	VDD
TCK/SWCLK	15	16	TRACE_D7
TMS/SWDIO	17	18	TRACE_D6
TDI	19	20	TRACE_D5
NJTRST	21	22	TRACE_D4
TRACE_D15	23	24	TRACE_D3
TRACE_D14	25	26	TRACE_D2
TRACE_D13	27	28	TRACE_D1
TRACE_D12	29	30	GND
TRACE_D11	31	32	GND
TRACE_D10	33	34	VDD
TRACE_D9	35	36	GND
TRACE_D8	37	38	TRACE_D0

6.9 JTAG connector

A JTAG/Serial Wire Debug 20 pins IDC connector (ARM JTAG 20, IDC 2.54mm) MB1262/CN14 outputs the JTAG signals. The JTAG function is a dedicated interface of STM32MP157XAA3.

Table 13 describe the JTAG connector pinout.

Table 13. **MB1262/CN14 JTAG connector pinout**

Board function	Pin	Pin	Board function
Power	**1**	**2**	Power
NJTRST	**3**	**4**	GND
JTDI	**5**	**6**	GND
JTMS/SWDIO	**7**	**8**	GND
JTCK/SWCLK	**9**	**10**	GND
Pull down	**11**	**12**	GND
JTDO/SWO	**13**	**14**	GND
NRST	**15**	**16**	GND
Pull down	**17**	**18**	GND
Pull down	**19**	**20**	GND

6.10 DDR3L

Two 16-bit DDR3L NT5CC256M16ER-EK of 4 Gbytes are implemented in flyby topology in MB1263/U6 and U7 positions. They are connected to the dedicated DDR interface of STM32MP157xAA3. For detailed information concerning the DDR HW design implementation, please refer to the application note AN5122 available on the *www.st.com* website.

6.11 eMMC

The STM32MP157xAA3 SDMMC2 in 8-bit wide bus mode drives a THGBMNG5D1LBAIL 32 Gbits eMMC in MB1263/U5 position.

6.11.1 eMMC IO interface

Table 14 HW configuration for the eMMC interface.

Table 14. **HW configuration for the Quad-SPI interface**

IO	Configuration(1)
PB14	**SDMMC2_D0 connected to MB1263/U5 DAT0**
PB15	SDMMC2_D1 connected to MB1263/U5 DAT1
PB3	SDMMC2_D2 connected to MB1263/U5 DAT2
PB4	SDMMC2_D3 connected to MB1263/U5 DAT3
PA8	SDMMC2_D4 connected to MB1263/U5 DAT4
PA9	SDMMC2_D5 connected to MB1263/U5 DAT5
PE5	SDMMC2_D6 connected to MB1263/U5 DAT6
PD3	SDMMC2_D7 connected to MB1263/U5 DAT7
PE3	**SDMMC2_CK connected to MB1263/U5 CLK**
PG6	**SDMMC2_CMD connected to MB1263/U5 CMD**

1. *Minimum set of signals required by the boot ROM during eMMC boot in **bold***

6.12 NAND Flash

The STM32MP157xAA3 FMC interface is connected to an 8 Gbits SLC NAND, 8-bit, 8-bit ECC, and 4 KBytes PS MT29F8G08ABACAH4 in MB1262/U11 position.

6.12.1 NAND IO interface

Table 15 features the HW configuration for the NAND interface.

Table 15. HW configuration for the Quad-SPI interface

IO	Configuration(1)
PD6	**NAND_NWAIT connected to MB1262/U11 R/B#**
PD11	**NAND_CLE connected to MB1262/U11 CLE**
PD12	**NAND_ALE connected to MB1262/U11 ALE**
PG9	**NAND_NCE connected to MB1262/U11 CE#**
PD5	**NAND_NWE connected to MB1262/U11 WE#**
PD4	**NAND_NOE connected to MB1262/U11 RE#**
PD14	**NAND_D0 connected to MB1262/U11 IO0**
PD15	**NAND_D1 connected to MB1262/U11 IO1**
PD0	**NAND_D2 connected to MB1262/U11 IO2**
PD1	**NAND_D3 connected to MB1262/U11 IO3**
PE7	**NAND_D4 connected to MB1262/U11 IO4**
PE8	**NAND_D5 connected to MB1262/U11 IO5**
PE9	**NAND_D6 connected to MB1262/U11 IO6**
PE10	**NAND_D7 connected to MB1262/U11 IO7**

1. *Minimum set of signals required by the boot ROM during NAND boot in **bold***

6.13 Quad-SPI NOR Flash

The STM32MP157xAA3 Quad-SPI interface is in dual-Serial mode to interface with two NOR Flash memories in parallel. Two MX25L51245G-XD, 3V3/512-Mbit each, are fitted on the STM32MP157x-EV1 MB1262, in MB1262/U14 and MB1262/U15 positions.

6.13.1 Quad-SPI IO interface

Table 16 describes the HW configuration for the Quad-SPI interface

Table 16. HW configuration for the Quad-SPI interface

IO	Configuration(1)
PF8	**QSPI_BK1_IO0 connected to MB1262/U14 SIO0**
PF9	**QSPI_BK1_IO1 connected to MB1262/U14 SIO1**
PF7	QSPI_BK1_IO2 connected to MB1262/U14 SIO2
PF6	QSPI_BK1_IO3 connected to MB1262/U14 SIO3
PB6	**QSPI_BK1_NCS connected to MB1262/U14 CS#**
PH2	**QSPI_BK2_IO0 connected to MB1262/U15 SIO0**
PH3	**QSPI_BK2_IO1 connected to MB1262/U15 SIO1**
PG10	QSPI_BK2_IO2 connected to MB1262/U15 SIO2
PG7	QSPI_BK2_IO3 connected to MB1262/U15 SIO3
PC0	QSPI_BK2_NCS connected to MB1262/U15 CS#
PF10	**QSPI_CLK connected to MB1262/U14 SCLK and MB1262/U15 SCLK**

1. *Minimum set of signals required by the boot ROM during dual-serial NOR boot in **bold***

6.14 microSD card

The MB1263/CN9 slot for microSD card is routed to STM32MP157xAA3 SDMMC1 port. This SD card interface is compliance with SD Memory Card Specification Version 3.01, UHS-I, all operation modes up to SDR104 and DDR50. The SD card interface is compatible with 1.8 V or 2.9 V signal levels.

6.14.1 SD card interface

The SD card interface, SDMMC1, is 4-bit wide with level shifter support, in order to connect to an SD 3.0-compliant bidirectional dual voltage level translator, interfacing with the memory card inserted in the SDCARD connector.

Table 17 describes the IO for the SDMMC1 interface.

Table 17. IO configuration for the SDIO interface

IO	Signal(1)
PC12	**SDMMC1_CK**
PE4	SDMMC1_CKIN
PD2	**SDMMC1_CMD**
PB9	**SDMMC1_CDIR**
PC8	**SDMMC1_D0**
PC9	SDMMC1_D1
PC10	SDMMC1_D2
PC11	SDMMC1_D3
PF2	SDMMC1_D0DIR
PC7	SDMMC1_D123DIR
PF14	uSD_LDO_SEL

1. *Minimum set of signals required by the boot ROM during SD card boot in **bold***

Figure 11 shows the SDCARD connector pinout MB1263/CN9.

Figure 11. SDCARD connector pinout MB1263/CN9

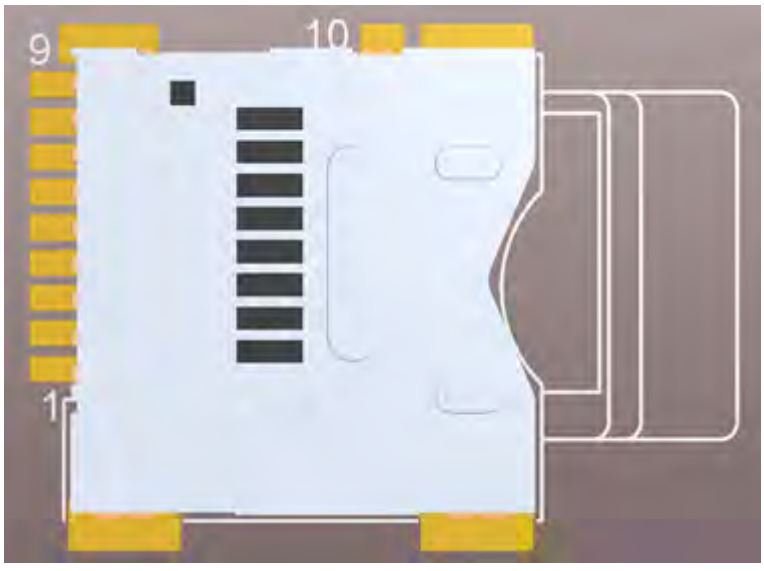


Table 18 describes the SDCARD connector pinout MB1263/CN9.

Table 18. **SDCARD connector pinout MB1263/CN9**

Pin	Board function
1	DATA2_SD
2	DATA3_SD
3	CMD_SD
4	VDD_SD
5	CLK_SD
6	GND
7	DATA0_SD
8	DATA1_SD
9	GND
10	SDCARD_DETECT active LOW

6.15 Audio

A codec WM8994ECS/R connected to an SAI of STM32MP157xAA3 supports TDM feature of the SAI port. TDM feature offers to STM32MP157xAA3 the capability to stream stereo audio channels. There are four digital microphones on STM32MP157x-EV1 board. STM32MP157x-EV1 also offers the possibility to connect a MEMS extension module.

6.15.1 Audio codec interface

The audio codec has two supplies 3V3 and 1V8 provided by STPMIC1.

The audio codec interfaces to the MPU are SAI2 and I2C2. Audio interrupt is connected to the IO-expander MFX.

SAI2A as Tx and SAI2B as Rx are connected to two different analog interfaces of the codec, to independently playback and record.

SAI2 is connected by default to the audio codec, and may be shared via solder bridge configuration with the expansion GPIO connector (refer to paragraph 6.28).

I2C2 is shared with all the peripherals: Audio codec, DSI LCD, RGB LTDC, Camera, and USB Hub. The audio codec I²C address is 0x36

Table 19. **IO configuration for the Audio Codec interface**

IO	Board function
PI5	SAI2_SCKA
PI7	SAI2_FSA
PI6	SAI2_SDA
PF11	SAI2_SDB
PE12	SAI2_SCK_B
PE13	SAI2_FS_B
PE0	SAI2_MCLKA
PE14	SAI2_MCLKB
PH5	I2C2_SDA
PH4	I2C2_SCL
MFX_IO5	AUDIO_INT

6.15.2 Digital microphones

MB1262/U1, U2, U3 and U4 are four MP34DT01TR MEMS digital omnidirectional microphones providing PDM (pulse density modulation) outputs. The implementation allows the beam forming.

Those 4 digital microphones support two stereo inputs connected either to the audio Codec or, by default, connected on two DFSDM odd channels of STM32MP157xAA3: DFSDM_DATA1 and DFSDM_DATA3 synchronized on DFSDM_CKOUT.

The STM32MP157xAA3 DFSDM interface is shared between the 4 embedded digital microphones and the extension module on connector MB1262/CN8.

Table 20 describes the HW configuration for the digital microphones.

Table 20. HW configuration for the digital microphones

Jumpers	HW	Setting	Configuration(1)
MB1262/JP1	U1/U3 stereo output selection	JP1[1-2]	Connected to codec DMICDAT2
		JP1[2-3]	Connected to STM32MP157xAA3 DFSDM_DATA3
MB1262/JP2	U2/U4 stereo output selection	JP2[1-2]	Connected to codec DMICDAT1
		JP2[2-3]	Connected to STM32MP157xAA3 DFSDM_DATA1
MB1262/JP3	U1/U2/U3/U4 CLK selection	**JP3[1-2]**	**Connected to STM32MP157xAA3 DFSDM_CKOUT**
		JP3[2-3]	Connected to codec DMICCLK
MB1262/JP4	U1/U2/U3/U4 VDD selection	**JP4[1-2]**	**3V3**
		JP1[2-3]	Codec MICBIAS1

1. *Default configuration in **bold***

6.15.3 Analog microphone and audio jack headphone

A headset including an analog microphone and a stereo headphone may be connected to the black 3.5 mm headset jack MB1262/CN5.

Figure 12. Audio jack connector MB1262/CN5

Table 21. Audio jack connector pinout MB1262/CN5

Pin	Board function
2	MIC_IN
3	GND
4	OUT_RIGHT
5	N/A
6	OUT_LEFT
7	N/A

6.15.4 Audio speaker out

The codec stereo speaker output is connected to a green 3.5 mm Speaker_out jack MB1262/CN4.

Figure 13. Audio jack connector MB1262/CN4

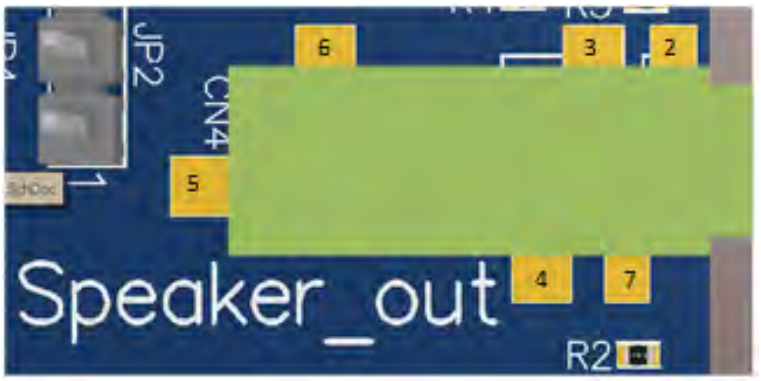


Table 22. Audio jack connector pinout MB1262/CN4

Pin	Board function
2	GND
3	GND
4	OUT_RIGHT
5	N/A
6	OUT_LEFT
7	N/A

6.15.5 SPDIF input and output

An RCA (white) connector MB1262/CN1 followed by an amplifier/filter stage is connected to the STM32MP157xAA3 SPDIF RX_IN.

The STM32MP157xAA3 SAI4_SDA port provides SPDIF_TX data to a RCA (yellow) connector MB1262/CN2.