SAMSUNG

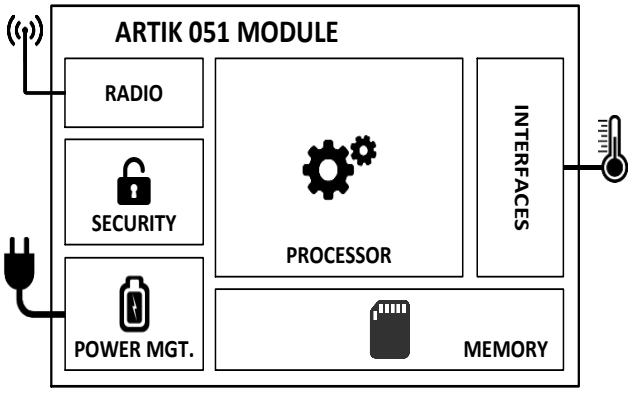
# ARTIK™ Modules

**CWAM210S**


Top View (Image is preliminary and will change)

Samsung's ARTIK™ Module is a highly integrated module for secure Internet of Things (IoT) devices that require Wi-Fi. It is based on an ARM® Cortex® R4 core with on-chip memories, an ARM® Cortex® M0+ core, a complete 2.4GHz Wi-Fi Phy, MAC layer processing, a large complement of standard digital buses including audio ($I^2S$), and power management. The module is packaged with additional external Flash memory, a hardware Secure Element and a single integrated 2.4GHz structural antenna.

The application processor is fully available for applications since the Wi-Fi stack, through the MAC layer, is handled by a co-processor. Aimed especially at power-sensitive devices needing Wi-Fi, the CWAM210S Module provides excellent performance in a variety of environments, with a feature set tailored specifically for IoT end nodes.




CWAM210S Module Block Diagram

| | |
|---|---|
| **Processor** | |
| CPU | ARM® Cortex® R4, 32-bit with 32KB I-Cache and 32KB D-Cache @ 320MHz |
| WLAN CPU | ARM Cortex M0+ @ 320MHz |
| **Memory** | |
| Embedded ROM | 64KB |
| User Embedded RAM | 1.25MB<br>128KB (Shared) |
| FLASH | 8MB SPI FLASH on Module |
| **Security** | |
| Secure Element | Secure point to point authentication and data transfer |
| **Radio** | |
| WLAN | IEEE802.11™ b/g/n 2.4GHz radio |
| **Power Management** | |
| Single Supply | Provides all power of the CWAM210S Module using on board bucks and LDO's |
| **Interfaces** | |
| Digital I/O | UART, $I^2C$, $I^2S$, SPI, PWM and GPIO |

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## Version History

| Revision | Date | Description | Maturity |
|---|---|---|---|
| V0.1 | 11/29/2016 | First Draft CWAM210S Module Datasheet | Pre Alpha |
| V0.11 | 12/14/2016 | Updated CWAM210S Module Block Diagram, Created Module Memory section. Created Power Management Unit section. | Pre Alpha |
| V0.12 | 12/27/2016 | Updated Figure 2. Updated Table 1. Created Level Shifter Table. Updated Table 4, 5, 6, 7, 8, 9, 10, 11, 12. Updated Table 13. Created Absolute Maximum Rating section. Created ESD section. Updated DC Electrical specifications section. | Pre Alpha |
| V0.13 | 12/29/2016 | Created Booting section. Updated Figure 4. Created Table 19. | Pre Alpha |
| V0.14 | 1/3/2016 | Updated Figure 3. Updated Figure 5. Updated Figure 2. | Pre Alpha |
| V0.15 | 1/5/2016 | Created ADC Dynamic behavior graph | Pre Alpha |
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# CWAM210S Module Block Diagram and Component Placement

*Figure 1* shows the functional Block Diagram of the CWAM210S Module.

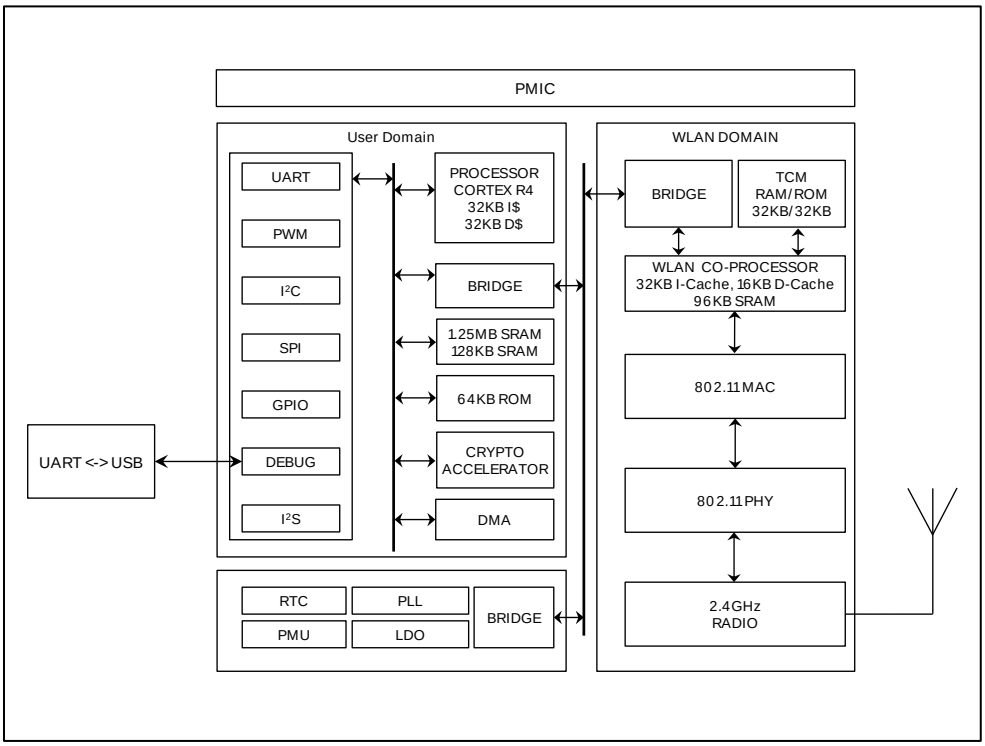


Figure 1. CWAM210S Module Block Diagram

## CWAM210S Module Wi-Fi Interface

The CWAM210S Module has an 802.11b/g/n Wi-Fi subsystem. The most important hardware features of the Wi-Fi system are:

- 802.11b/g/n support @ 2.4GHz
- 20MHz SISI (802.11n)
- UDP throughput up to 50Mbps
- WPA/WPA2/WAPI with WEP/TKIP implemented in software
- Dedicated Wi-Fi Processor Sub System
    - ARM® Cortex® R4 Processor @ 480 MHz
    - Operating frequency of 320MHz
    - 32KB I-Cache
    - 16KB D-Cache
    - Tightly Coupled Memory (32KB Code Memory/32KB Data Memory)
    - SRAM 96KB

## CWAM210S Module Memory

The CWAM210S Module has a memory subsystem with the following hardware features:

- Internal RAM for secure boot, secure OS and general purpose operations.
    - 1280KB dedicated RAM
    - 128KB shared RAM

- Internal ROM for secure boot and secure OS operations.
    - 64KB dedicated ROM

## CWAM210S Module Power Management Unit

The CWAM210S Module has one universal power management unit that controls the state of power on the CWAM210S Module. The most important features of the PMU are:

- Fine granular power control
    - Through the use of power domains
- System level power control
    - Deep stop mode
    - Sleep power mode
- Power savings techniques
    - Frequency scaling
    - Clock gating
    - Power gating

## CWAM210S Module Security Subsystem

The CWAM210S Module has a dedicated security subsystem to ensure a secure end to end operation in any IoT environment. The most important features of the CWAM210S Module security subsystem are:

- Isolated Execution Environment
    - Isolated Cortex-M0 processor
    - 8KB ROM for secure booting
    - 32KB secure SRAM
    - Dedicated secure DMA channel for secure backup/restore of SRAM content
    - Secure Mailbox (68x32b wide) for secure communication
    - Isolated key support
        - Backup encryption key 256-bits
        - SSS root private key 521-bits
        - Storage key 256-bits
- Symmetric key engines
    - Secure AES
    - Secure DES/Triple-DES
- Stream cipher engine
    - ARC4 engine
- Various Hash engines
    - SHA-1/SHA2-256/ SHA2-384/ SHA2-512/MD5 HMAC
- Asymmetric key engines
    - PKA (Public Key Accelerator) engine
- PRNG (Pseudo Random Number Generator)
- DTRNG (Digital True RNG)
- Secure timer
- Secure key manager
- DMA Support, Descriptor DMA
- Block ciphers + hashing
- Retention reset scheme

## CWAM210S Module ADC Interface

The CWAM210S Module has one 4-channel selectable analog to digital converter. The most important hardware features of the A/D interface are:

- Programmable 4-channel selection
- Main ADC clock at 6.5MHz

- Conversion clock ADC at 1.08MHz
- Support for selectable conversion mode: 1, 2, 4, 8, 16, 32, 64
- Differential non-linearity error ±2 LSB
- Integral non-linearity error ±6 LSB
- Top offset error ±10 LSB
- Bottom offset error ±10 LSB

Figure 2 depicts the dynamic behavior between input voltage on the ADC and resulted LSB value in the ADC register.

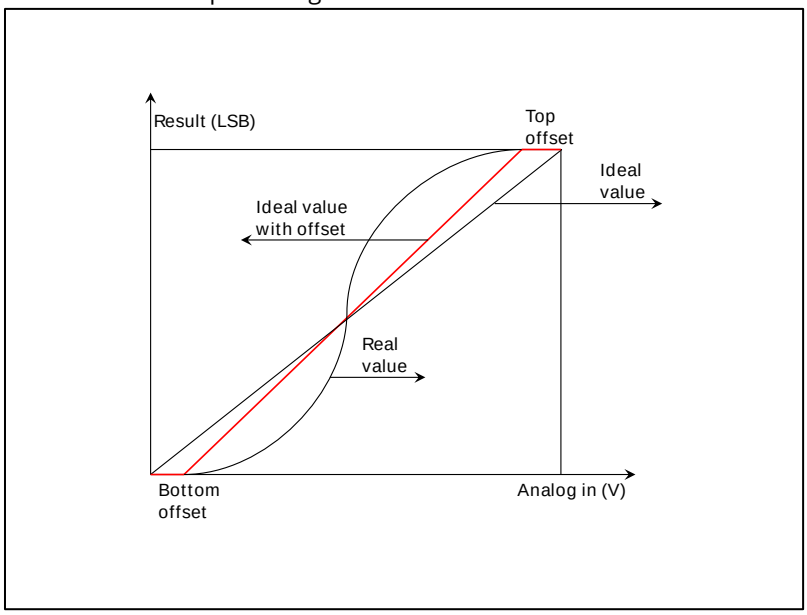


Figure 2. ADC LSB behavior

## CWAM210S Module UART Interface

By default the CWAM210S Module has three, 2-pin UART interfaces. Using GPIOs that are currently used for other functionality you can potentially create two 4-pin UART interfaces. The most important hardware features of the UART interface is:

- The UART can be operated in DMA or interrupt-based mode
- Support for 5-bit, 6-bit, 7-bit or 8-bit serial data transmit and receive
- Programmable baud rate
- One or two stop bit insertion

## CWAM210S Module GPIO Interface

The CWAM210S Module has an extensive general purpose Input/Output interface. The most important features of the CWAM210S Module GPIO interface are:

- Support for 63 multi-function input output ports.
- Support for 28 dedicated GPIO ports
- Control of 16 external interrupts

## CWAM210S INT Interface

The CWAM210S Module is equipped with an interrupt controller. The most important features of the CWAM210S Module Interrupt Interface are:

- Enable, disable and generate interrupts from peripheral sources
- Software generated interrupts
- Interrupt masking and prioritization
- Wake-up events for power management

- Control of 3 external wakeup interrupts

## CWAM210S Module I²C Interface

By default the CWAM210S Module has two high speed multi-master $I^2C$ interfaces available with speeds up to 3.4Mbps. Using GPIOs that are currently used for other functionality you can potentially create four $I^2C$ interfaces.

## CWAM210S Module SPI Interface

By default the CWAM210S Module has two dedicated SPI interfaces. Using GPIOs that are currently used for other functionality you can potentially create four SPI interfaces. The most important hardware features of the SPI interfaces are:

- Full duplex communication
- 8, 16 or 32-bit shift registers and bus interface
- Motorola SPI protocol and National Semiconductor Microwire protocol
- Master and slave mode operation
- Two independent 32-bit wide transmit/receive FIFOs
- Transmit and receive speeds up to 50MHz

## CWAM210S Module PWM Interface

By default the CWAM210S Module has seven PWM timers available. The most important features of the PWM interfaces are:

- 32-bit size timers on each PWM signal
- Two 8-bit pre-scalers (first level of division) and 5 clock-dividers/multiplexers for second level division
- Static configuration option
- Dynamic configuration option
- Auto-reload and One-shot pulse mode
- Dead zone generator
- Level interrupt generation

## CWAM210S Module I²S Interface

By default the CWAM210S Module does not have an $I^2S$ interface, however when re-using the right GPIO pins one I2S interface can be allocated. The most important features of the $I^2S$ interface are:

- Stereo channel support with external DMA based operation
- Mixes up to two sound sources
- Support for serial data transfer of 8, 16 or 32-bit per channel
- Support for slave mode

## CWAM210S Module Processor System

The ARTIK 51 Module has one dedicated Cortex®-R4 processor dedicated towards application processing. The main features of the main processor are:

- Cortex® R4 ARM® processor
- CPU speed 320MHz
- 32kB Instruction cache
- 32kB Data cache

# CWAM210S Module Edge Connector

The CWAM210S Module utilizes 76 signals and ground pins providing all the relevant signaling. *Figure 3* shows how the Edge Connector is oriented and how signal-coordinates are assigned to the edge of the CWAM210S Module. *Table 1* describes the relation between the edge coordinates and the signal names.

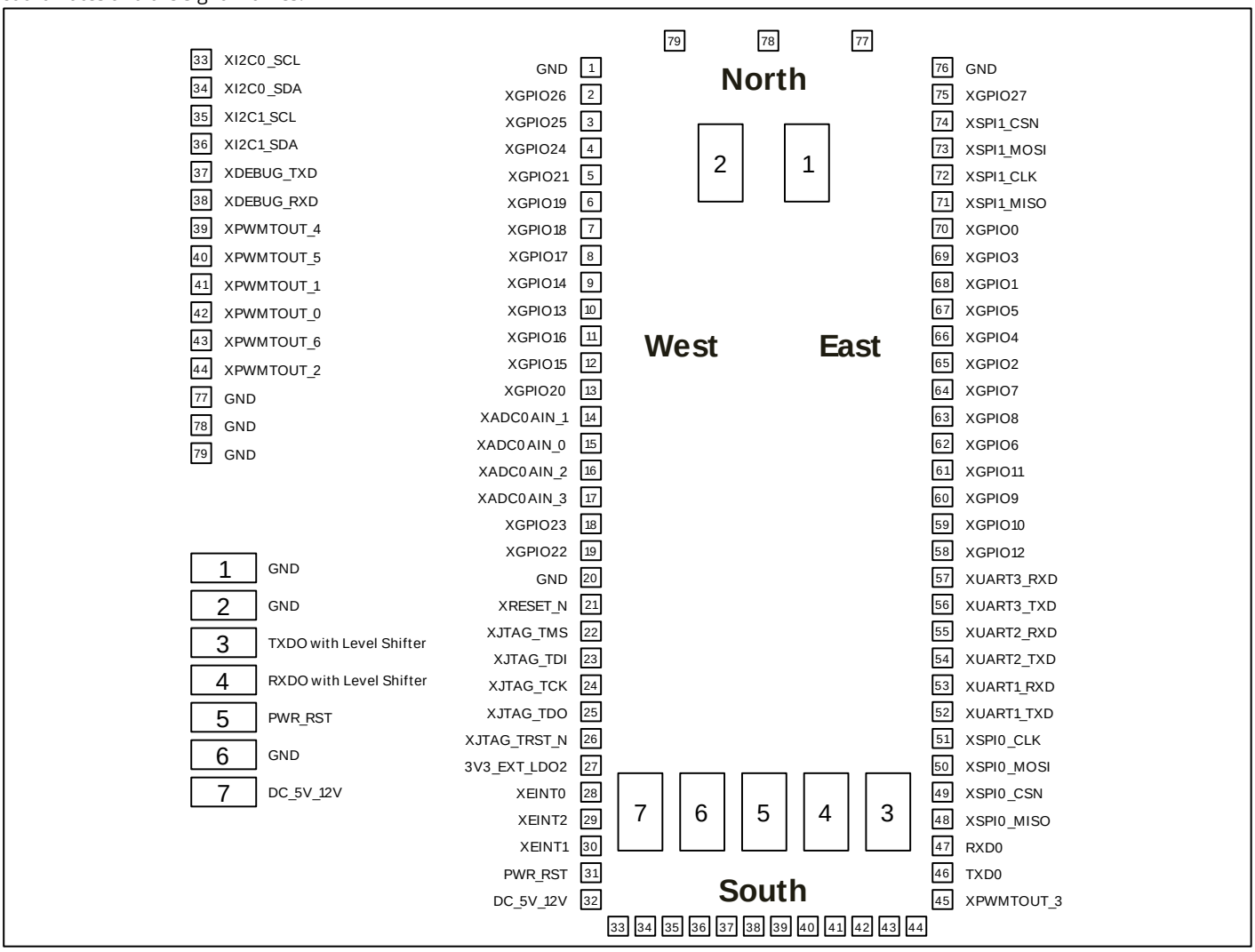


Figure 3. CWAM210S Module Edge Connector

Table 1. CWAM210S Module Edge Connector Table Signal Descriptions

| Pin Number | Pin Name | I/O* | PU/PD | Power | Default Function | Groups |
|---|---|---|---|---|---|---|
| 1 | GND | - | - | - | GND | 1 |
| 2 | XGPIO26 | I | PD | VDDQ33_EXT0 | GPIO | 2 |
| 3 | XGPIO25 | I | PD | VDDQ33_EXT0 | GPIO | 3 |
| 4 | XGPIO24 | I | PD | VDDQ33_EXT0 | GPIO | 4 |
| 5 | XGPIO21 | I | PD | VDDQ33_EXT0 | GPIO | 5 |
| 6 | XGPIO19 | I | PD | VDDQ33_EXT0 | GPIO | 6 |
| 7 | XGPIO18 | I | PD | VDDQ33_EXT0 | GPIO | 7 |
| 8 | XGPIO17 | I | PD | VDDQ33_EXT0 | GPIO | 8 |
| 9 | XGPIO14 | I | PD | VDDQ33_EXT0 | GPIO | 9 |
| 10 | XGPIO13 | I | PD | VDDQ33_EXT0 | GPIO | 10 |

| Pin Number | Pin Name | I/O* | PU/PD | Power | Default Function | Groups |
|---|---|---|---|---|---|---|
| 11 | XGPIO16 | I | PD | VDDQ33_EXT0 | GPIO | 11 |
| 12 | XGPIO15 | I | PD | VDDQ33_EXT0 | GPIO | 12 |
| 13 | XGPIO20 | I | PD | VDDQ33_EXT0 | GPIO | 13 |
| 14 | XADC0AIN_1 | – | – | AVDD18_ADC0 | ADC | 14 |
| 15 | XADC0AIN_0 | – | – | AVDD18_ADC0 | ADC | 15 |
| 16 | XADC0AIN_2 | – | – | AVDD18_ADC0 | ADC | 16 |
| 17 | XADC0AIN_3 | – | – | AVDD18_ADC0 | ADC | 17 |
| 18 | XGPIO23 | I | PD | VDDQ1833_SDIO_0 | GPIO | 18 |
| 19 | XGPIO22 | I | PD | VDDQ1833_SDIO_0 | GPIO | 19 |
| 20 | GND | - | - | - | GND | 20 |
| 21 | XRESET_N | I | – | VDDQ33_EXT1 | RESET | 21 |
| 22 | XJTAG_TMS | I | PU | VDDQ33_EXT1 | DEBUG | 22 |
| 23 | XJTAG_TDI | I | PU | VDDQ33_EXT1 | DEBUG | 23 |
| 24 | XJTAG_TCK | I | PD | VDDQ33_EXT1 | DEBUG | 24 |
| 25 | XJTAG_TDO | I | PD | VDDQ33_EXT1 | DEBUG | 25 |
| 26 | XJTAG_TRST_N | I | PD | VDDQ33_EXT1 | DEBUG | 26 |
| 27 | 3V3_EXT_LDO2 | - | - | - | POWER | 27 |
| 28 | XEINT_0 | I | PD | VDDQ33_EXT1 | INT | 28 |
| 29 | XEINT_2 | I | PD | VDDQ33_EXT1 | INT | 29 |
| 30 | XEINT_1 | I | PD | VDDQ33_EXT1 | INT | 30 |
| 31 | PWR_RST | - | - | - | RESET | 31 |
| 32 | DC_5V_12V | - | - | - | POWER | 32 |
| 33 | XI2C0_SCL | I | PD | VDDQ33_EXT1 | I2C | 33 |
| 34 | XI2C0_SDA | I | PD | VDDQ33_EXT1 | I2C | 34 |
| 35 | XI2C1_SCL | I | PD | VDDQ33_EXT1 | I2C | 35 |
| 36 | XI2C1_SDA | I | PD | VDDQ33_EXT1 | I2C | 36 |
| 37 | XDEBUG_TXD | I | PD | VDDQ33_EXT1 | DEBUG | 37 |
| 38 | XDEBUG_RXD | I | PD | VDDQ33_EXT1 | DEBUG | 38 |
| 39 | XPWMTOUT_4 | I | PD | VDDQ33_EXT0 | PWM | 39 |
| 40 | XPWMTOUT_5 | I | PD | VDDQ33_EXT0 | PWM | 40 |
| 41 | XPWMTOUT_1 | I | PD | VDDQ33_EXT0 | PWM | 41 |
| 42 | XPWMTOUT_0 | I | PD | VDDQ33_EXT0 | PWM | 42 |
| 43 | XPWMTOUT_6 | I | PD | VDDQ33_EXT0 | PWM | 43 |
| 44 | XPWMTOUT_2 | I | PD | VDDQ33_EXT0 | PWM | 44 |
| 45 | XPWMTOUT_3 | I | PD | VDDQ33_EXT0 | PWM | 45 |
| 46 | TXD0 | - | - | - | TR | 46 |
| 47 | RXD0 | - | - | - | TR | 47 |
| 48 | XSPI0_MISO | I | PD | VDDQ33_EXT0 | SPI | 48 |
| 49 | XSPI0_CSN | I | PD | VDDQ33_EXT0 | SPI | 49 |
| 50 | XSPI0_MOSI | I | PD | VDDQ33_EXT0 | SPI | 50 |
| 51 | XSPI0_CLK | I | PD | VDDQ33_EXT0 | SPI | 51 |
| 52 | XUART1_TXD | I | PD | VDDQ33_EXT0 | UART | 52 |
| 53 | XUART1_RXD | I | PD | VDDQ33_EXT0 | UART | 53 |
| 54 | XUART2_TXD | I | PD | VDDQ33_EXT0 | UART | 54 |
| 55 | XUART2_RXD | I | PD | VDDQ33_EXT0 | UART | 55 |
| 56 | XUART3_TXD | I | PD | VDDQ33_EXT0 | UART | 56 |
| 57 | XUART3_RXD | I | PD | VDDQ33_EXT0 | UART | 57 |
| 58 | XGPIO12 | I | PD | VDDQ33_EXT0 | GPIO | 58 |
| 59 | XGPIO10 | I | PD | VDDQ33_EXT0 | GPIO | 59 |
| 60 | XGPIO9 | I | PD | VDDQ33_EXT0 | GPIO | 60 |
| 61 | XGPIO11 | I | PD | VDDQ33_EXT0 | GPIO | 61 |
| 62 | XGPIO6 | I | PD | VDDQ33_EXT0 | GPIO | 62 |

| Pin Number | Pin Name | I/O* | PU/PD | Power | Default Function | Groups |
|---|---|---|---|---|---|---|
| 63 | XGPIO8 | I | PD | VDDQ33_EXT0 | GPIO | 63 |
| 64 | XGPIO7 | I | PD | VDDQ33_EXT0 | GPIO | 64 |
| 65 | XGPIO2 | I | PD | VDDQ33_EXT0 | GPIO | 65 |
| 66 | XGPIO4 | I | PD | VDDQ33_EXT0 | GPIO | 66 |
| 67 | XGPIO5 | I | PD | VDDQ33_EXT0 | GPIO | 67 |
| 68 | XGPIO1 | I | PD | VDDQ33_EXT0 | GPIO | 68 |
| 69 | XGPIO3 | I | PD | VDDQ33_EXT0 | GPIO | 69 |
| 70 | XGPIO0 | I | PD | VDDQ33_EXT0 | GPIO | 70 |
| 71 | XSPI1_MISO | I | PD | VDDQ33_EXT0 | SPI | 71 |
| 72 | XSPI1_CLK | I | PD | VDDQ33_EXT0 | SPI | 72 |
| 73 | XSPI1_MOSI | I | PD | VDDQ33_EXT0 | SPI | 73 |
| 74 | XSPI1_CSN | I | PD | VDDQ33_EXT0 | SPI | 74 |
| 75 | XGPIO27 | I | PD | VDDQ33_EXT0 | GPIO | 75 |
| 76 | GND | - | - | - | GND | 76 |

Note:

1. *Default setting after reset
2. Type definition: [S:Signal ball, P:Power ball, G:GND ball]
3. IO pad type definition: [I:Input, O:Output, I/O: Input/Output
4. Internal Pull Up/Down definition: – PU:Pull Up, PD:Pull Down, N:No Pull

# CWAM210S Functional Interfaces

## ADC Interface

Table 2. ADC Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 14 | XADC0AIN_1 | – | – | AVDD18_ADC0 | XADC0AIN_1 |
| 15 | XADC0AIN_0 | – | – | AVDD18_ADC0 | XADC0AIN_0 |
| 16 | XADC0AIN_2 | – | – | AVDD18_ADC0 | XADC0AIN_2 |
| 17 | XADC0AIN_3 | – | – | AVDD18_ADC0 | XADC0AIN_3 |

## Debug Interface

Table 3. Debug Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 22 | XJTAG_TMS | I | PU | VDDQ33_EXT1 | XJTAG_TMS |
| 23 | XJTAG_TDI | I | PU | VDDQ33_EXT1 | XJTAG_TDI |
| 24 | XJTAG_TCK | I | PD | VDDQ33_EXT1 | XJTAG_TCK |
| 25 | XJTAG_TDO | I | PD | VDDQ33_EXT1 | XJTAG_TDO |
| 26 | XJTAG_TRST_N | I | PD | VDDQ33_EXT1 | XJTAG_TRST_N |
| 37 | XDEBUG_TXD | I | PD | VDDQ33_EXT1 | XDEBUG_TXD |
| 38 | XDEBUG_RXD | I | PD | VDDQ33_EXT1 | XDEBUG_RXD |

## GPIO Interface

Table 4. GPIO Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 2 | XGPIO26 | I | PD | VDDQ33_EXT0 | XGPIO26 |
| 3 | XGPIO25 | I | PD | VDDQ33_EXT0 | XGPIO25 |
| 4 | XGPIO24 | I | PD | VDDQ33_EXT0 | XGPIO24 |
| 5 | XGPIO21 | I | PD | VDDQ33_EXT0 | XGPIO21 |
| 6 | XGPIO19 | I | PD | VDDQ33_EXT0 | XGPIO19 |
| 7 | XGPIO18 | I | PD | VDDQ33_EXT0 | XGPIO18 |
| 8 | XGPIO17 | I | PD | VDDQ33_EXT0 | XGPIO17 |
| 9 | XGPIO14 | I | PD | VDDQ33_EXT0 | XGPIO14 |
| 10 | XGPIO13 | I | PD | VDDQ33_EXT0 | XGPIO13 |
| 11 | XGPIO16 | I | PD | VDDQ33_EXT0 | XGPIO16 |
| 12 | XGPIO15 | I | PD | VDDQ33_EXT0 | XGPIO15 |
| 13 | XGPIO20 | I | PD | VDDQ33_EXT0 | XGPIO20 |
| 18 | XGPIO23 | I | PD | VDDQ1833_SDIO_0 | XGPIO23 |
| 19 | XGPIO22 | I | PD | VDDQ1833_SDIO_0 | XGPIO22 |
| 58 | XGPIO12 | I | PD | VDDQ33_EXT0 | XGPIO12 |
| 59 | XGPIO10 | I | PD | VDDQ33_EXT0 | XGPIO10 |
| 60 | XGPIO9 | I | PD | VDDQ33_EXT0 | XGPIO9 |
| 61 | XGPIO11 | I | PD | VDDQ33_EXT0 | XGPIO11 |
| 62 | XGPIO6 | I | PD | VDDQ33_EXT0 | XGPIO6 |
| 63 | XGPIO8 | I | PD | VDDQ33_EXT0 | XGPIO8 |
| 64 | XGPIO7 | I | PD | VDDQ33_EXT0 | XGPIO7 |
| 65 | XGPIO2 | I | PD | VDDQ33_EXT0 | XGPIO2 |
| 66 | XGPIO4 | I | PD | VDDQ33_EXT0 | XGPIO4 |
| 67 | XGPIO5 | I | PD | VDDQ33_EXT0 | XGPIO5 |

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 68 | XGPIO1 | I | PD | VDDQ33_EXT0 | XGPIO1 |
| 69 | XGPIO3 | I | PD | VDDQ33_EXT0 | XGPIO3 |
| 70 | XGPIO0 | I | PD | VDDQ33_EXT0 | XGPIO0 |
| 75 | XGPIO27 | I | PD | VDDQ33_EXT0 | XGPIO27 |

## I²C Interface

Table 5. I²C Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 33 | XI2C0_SCL | I | PD | VDDQ33_EXT1 | XI2C0_SCL |
| 34 | XI2C0_SDA | I | PD | VDDQ33_EXT1 | XI2C0_SDA |
| 35 | XI2C1_SCL | I | PD | VDDQ33_EXT1 | XI2C1_SCL |
| 36 | XI2C1_SDA | I | PD | VDDQ33_EXT1 | XI2C1_SDA |

## INT Interface

Table 6. Interrupt Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 28 | XEINT_0 | I | PD | VDDQ33_EXT1 | XEINT_0 |
| 29 | XEINT_2 | I | PD | VDDQ33_EXT1 | XEINT_2 |
| 30 | XEINT_1 | I | PD | VDDQ33_EXT1 | XEINT_1 |

## Power Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 1 | GND | - | - | - | - |
| 20 | GND | - | - | - | - |
| 27 | 3V3_EXT_LDO2 | - | - | - | - |
| 32 | DC_5V_12V | - | - | - | - |
| 76 | GND | - | - | - | - |

## PWM Interface

Table 7. PWM Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 39 | XPWMTOUT_4 | I | PD | VDDQ33_EXT0 | XPWMTOUT_4 |
| 40 | XPWMTOUT_5 | I | PD | VDDQ33_EXT0 | XPWMTOUT_5 |
| 41 | XPWMTOUT_1 | I | PD | VDDQ33_EXT0 | XPWMTOUT_1 |
| 42 | XPWMTOUT_0 | I | PD | VDDQ33_EXT0 | XPWMTOUT_0 |
| 43 | XPWMTOUT_6 | I | PD | VDDQ33_EXT0 | XPWMTOUT_6 |
| 44 | XPWMTOUT_2 | I | PD | VDDQ33_EXT0 | XPWMTOUT_2 |
| 45 | XPWMTOUT_3 | I | PD | VDDQ33_EXT0 | XPWMTOUT_3 |

## Reset Interface

Table 8. Reset Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 21 | XRESET_N | I | – | VDDQ33_EXT1 | XRESET_N |
| 31 | PWR_RST | - | - | - | - |

## SPI Interface

Table 9. SPI Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 48 | XSPI0_MISO | I | PD | VDDQ33_EXT0 | XSPI0_MISO |
| 49 | XSPI0_CSN | I | PD | VDDQ33_EXT0 | XSPI0_CSN |
| 50 | XSPI0_MOSI | I | PD | VDDQ33_EXT0 | XSPI0_MOSI |
| 51 | XSPI0_CLK | I | PD | VDDQ33_EXT0 | XSPI0_CLK |
| 71 | XSPI1_MISO | I | PD | VDDQ33_EXT0 | XSPI1_MISO |
| 72 | XSPI1_CLK | I | PD | VDDQ33_EXT0 | XSPI1_CLK |
| 73 | XSPI1_MOSI | I | PD | VDDQ33_EXT0 | XSPI1_MOSI |
| 74 | XSPI1_CSN | I | PD | VDDQ33_EXT0 | XSPI1_CSN |

## Level Shifter

Table 10. Level Shifter

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 46 | TXD0 | - | - | - | - |
| 47 | RXD0 | - | - | - | - |

## UART Interface

Table 11. UART Interface

| Pin Number | Pin Name | I/O | PU/PD | Power | Default Function |
|---|---|---|---|---|---|
| 52 | XUART1_TXD | I | PD | VDDQ33_EXT0 | XUART1_TXD |
| 53 | XUART1_RXD | I | PD | VDDQ33_EXT0 | XUART1_RXD |
| 54 | XUART2_TXD | I | PD | VDDQ33_EXT0 | XUART2_TXD |
| 55 | XUART2_RXD | I | PD | VDDQ33_EXT0 | XUART2_RXD |
| 56 | XUART3_TXD | I | PD | VDDQ33_EXT0 | XUART3_TXD |
| 57 | XUART3_RXD | I | PD | VDDQ33_EXT0 | XUART3_RXD |

# CWAM210S Module GPIO Alternate Functions

*Table 12* describes the alternate functions that can be accessed using GPIOs that are available on the edge of the CWAM210S Module.

Table 12. Alternate functions of the CWAM210S Module

| PIN # | Pin Name | Default Function | Alternate Function | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 2 | XGPIO26 | XGPIO26 | GPG3[2] | I2S_0_SDO | MCT1_INTlev | - | - | - | - |
| 3 | XGPIO25 | XGPIO25 | GPG3[1] | I2S_0_LRCK | MCT0_TICK | - | - | - | - |
| 4 | XGPIO24 | XGPIO24 | GPG3[0] | I2S_0_BCLK | MCT0_INTlev | WB2AP_ETM_DATA_OUT_15 | WLBT_DEBUG_15 | - | - |
| 5 | XGPIO21 | XGPIO21 | GPG2[5] | SerialFLASH_MONITOR_sf1_5 | WLBT_UART_TXD | WB2AP_ETM_DATA_OUT_12 | WLBT_DEBUG_12 | WAKE_EXT_INTG2[5] | - |
| 6 | XGPIO19 | XGPIO19 | GPG2[3] | SerialFLASH_MONITOR_sf1_3 | WB2AP_ETM_DATA_OUT_10 | WLBT_DEBUG_10 | WAKE_EXT_INTG2[3] | - | - |
| 7 | XGPIO18 | XGPIO18 | GPG2[2] | SerialFLASH_MONITOR_sf1_2 | WB2AP_ETM_DATA_OUT_09 | WLBT_DEBUG_09 | WAKE_EXT_INTG2[2] | - | - |
| 8 | XGPIO17 | XGPIO17 | GPG2[1] | SerialFLASH_MONITOR_sf1_1 | WB2AP_ETM_DATA_OUT_08 | WLBT_DEBUG_08 | WAKE_EXT_INTG2[1] | - | - |
| 9 | XGPIO14 | XGPIO14 | GPG1[6] | SerialFLASH_MONITOR_sf0_6 | ALV_DBG[14] | WB2AP_ETM_DATA_OUT_05 | WLBT_DEBUG_05 | WAKE_EXT_INTG1[6] | - |
| 10 | XGPIO13 | XGPIO13 | GPG1[5] | SerialFLASH_MONITOR_sf0_5 | ALV_DBG[13] | WB2AP_ETM_DATA_OUT_04 | WLBT_DEBUG_04 | WAKE_EXT_INTG1[5] | - |
| 11 | XGPIO16 | XGPIO16 | GPG2[0] | SerialFLASH_MONITOR_sf1_0 | WB2AP_ETM_DATA_OUT_07 | WLBT_DEBUG_07 | WAKE_EXT_INTG2[0] | - | - |
| 12 | XGPIO15 | XGPIO15 | GPG1[7] | SerialFLASH_MONITOR_sf0_7 | ALV_DBG[15] | WB2AP_ETM_DATA_OUT_06 | WLBT_DEBUG_06 | WAKE_EXT_INTG1[7] | - |
| 13 | XGPIO20 | XGPIO20 | GPG2[4] | SerialFLASH_MONITOR_sf1_4 | WLBT_UART_RXD | WB2AP_ETM_DATA_OUT_11 | WLBT_DEBUG_11 | WAKE_EXT_INTG2[4] | - |
| 18 | XGPIO23 | XGPIO23 | GPG2[7] | SerialFLASH_MONITOR_sf1_7 | WB2AP_ETM_DATA_OUT_14 | WLBT_DEBUG_14 | WAKE_EXT_INTG2[7] | - | - |
| 19 | XGPIO22 | XGPIO22 | GPG2[6] | SerialFLASH_MONITOR_sf1_6 | WB2AP_ETM_DATA_OUT_13 | WLBT_DEBUG_13 | WAKE_EXT_INTG2[6] | - | - |
| 22 | XJTAG_TMS | XJTAG_TMS | ETC0[1] | - | - | - | - | - | - |
| 23 | XJTAG_TDI | XJTAG_TDI | ETC0[3] | - | - | - | - | - | - |
| 24 | XJTAG_TCK | XJTAG_TCK | ETC0[2] | - | - | - | - | - | - |
| 25 | XJTAG_TDO | XJTAG_TDO | ETC0[4] | - | - | - | - | - | - |
| 26 | XJTAG_TRST_N | XJTAG_TRST_N | ETC0[0] | - | - | - | - | - | - |
| 28 | XEINT_0 | XEINT_0 | GPA0[0] | WAKE_EXT_INTA0[0] | - | - | - | - | - |
| 29 | XEINT_2 | XEINT_2 | GPA0[2] | WAKE_EXT_INTA0[2] | - | - | - | - | - |
| 30 | XEINT_1 | XEINT_1 | GPA0[1] | WAKE_EXT_INTA0[1] | - | - | - | - | - |
| 33 | XI2C0_SCL | XI2C0_SCL | GPA1[0] | HSI2C_0_SCL | - | - | - | - | - |
| 34 | XI2C0_SDA | XI2C0_SDA | GPA1[1] | HSI2C_0_SDA | - | - | - | - | - |
| 35 | XI2C1_SCL | XI2C1_SCL | GPA1[2] | HSI2C_1_SCL | - | - | - | - | - |
| 36 | XI2C1_SDA | XI2C1_SDA | GPA1[3] | HSI2C_1_SDA | - | - | - | - | - |
| 37 | XDEBUG_TXD | XDEBUG_TXD | GPA3[1] | Xdebug_TXD | - | - | - | - | - |
| 38 | XDEBUG_RXD | XDEBUG_RXD | GPA3[0] | Xdebug_RXD | - | - | - | - | - |
| 39 | XPWMTOUT_4 | XPWMTOUT_4 | GPP2[4] | PWM_TOUT_4 | - | - | - | - | - |
| 40 | XPWMTOUT_5 | XPWMTOUT_5 | GPP2[5] | PWM_TOUT_5 | - | - | - | - | - |
| 41 | XPWMTOUT_1 | XPWMTOUT_1 | GPP2[1] | PWM_TOUT_1 | COUNTER_0 | UART_3_RTSn | - | - | - |

| PIN # | Pin Name | Default Function | Alternate Function | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 42 | XPWMTOUT_0 | XPWMTOUT_0 | GPP2[0] | PWM_TOUT_0 | UART_3_CTSn | - | - | - | - |
| 43 | XPWMTOUT_6 | XPWMTOUT_6 | GPP2[6] | PWM_TOUT_6 | - | - | - | - | - |
| 44 | XPWMTOUT_2 | XPWMTOUT_2 | GPP2[2] | PWM_TOUT_2 | - | - | - | - | - |
| 45 | XPWMTOUT_3 | XPWMTOUT_3 | GPP2[3] | PWM_TOUT_3 | - | - | - | - | - |
| 48 | XSPI0_MISO | XSPI0_MISO | GPP0[2] | SPI_0_MISO | - | - | - | - | - |
| 49 | XSPI0_CSN | XSPI0_CSN | GPP0[1] | SPI_0_CSn | - | - | - | - | - |
| 50 | XSPI0_MOSI | XSPI0_MOSI | GPP0[3] | SPI_0_MOSI | - | - | - | - | - |
| 51 | XSPI0_CLK | XSPI0_CLK | GPP0[0] | SPI_0_CLK | - | - | - | - | - |
| 52 | XUART1_TXD | XUART1_TXD | GPP0[5] | UART_1_TXD | UART_2_RTSn | - | - | - | - |
| 53 | XUART1_RXD | XUART1_RXD | GPP0[4] | UART_1_RXD | UART_2_CTSn | - | - | - | - |
| 54 | XUART2_TXD | XUART2_TXD | GPP0[7] | UART_2_TXD | - | - | - | - | - |
| 55 | XUART2_RXD | XUART2_RXD | GPP0[6] | UART_2_RXD | - | - | - | - | - |
| 56 | XUART3_TXD | XUART3_TXD | GPP1[7] | UART_3_TXD | - | - | - | - | - |
| 57 | XUART3_RXD | XUART3_RXD | GPP1[6] | UART_3_RXD | - | - | - | - | - |
| 58 | XGPIO12 | XGPIO12 | GPG1[4] | SerialFLASH_MONITOR_sf0_4 | ALV_DBG[12] | WB2AP_ETM_DATA_OUT_03 | WLBT_DEBUG_03 | WAKE_EXT_INTG1[4] | - |
| 59 | XGPIO10 | XGPIO10 | GPG1[2] | SPI_3_MISO | SerialFLASH_MONITOR_sf0_2 | ALV_DBG[10] | WB2AP_ETM_DATA_OUT_01 | WLBT_DEBUG_01 | WAKE_EXT_INTG1[2] |
| 60 | XGPIO9 | XGPIO9 | GPG1[1] | SPI_3_CSn | SerialFLASH_MONITOR_sf0_1 | ALV_DBG[9] | WB2AP_ETM_DATA_OUT_00 | WLBT_DEBUG_00 | WAKE_EXT_INTG1[1] |
| 61 | XGPIO11 | XGPIO11 | GPG1[3] | SPI_3_MOSI | SerialFLASH_MONITOR_sf0_3 | ALV_DBG[11] | WB2AP_ETM_DATA_OUT_02 | WLBT_DEBUG_02 | WAKE_EXT_INTG1[3] |
| 62 | XGPIO6 | XGPIO6 | GPG0[6] | SPI_2_MISO | ALV_DBG[6] | - | - | - | - |
| 63 | XGPIO8 | XGPIO8 | GPG1[0] | SPI_3_CLK | SerialFLASH_MONITOR_sf0_0 | ALV_DBG[8] | WB2AP_TRACE_CLK_OUT | WAKE_EXT_INTG1[0] | - |
| 64 | XGPIO7 | XGPIO7 | GPG0[7] | SPI_2_MOSI | ALV_DBG[7] | - | - | - | - |
| 65 | XGPIO2 | XGPIO2 | GPG0[2] | HSI2C_3_SCL | ALV_DBG[2] | - | - | - | - |
| 66 | XGPIO4 | XGPIO4 | GPG0[4] | SPI_2_CLK | ALV_DBG[4] | - | - | - | - |
| 67 | XGPIO5 | XGPIO5 | GPG0[5] | SPI_2_CSn | ALV_DBG[5] | - | - | - | - |
| 68 | XGPIO1 | XGPIO1 | GPG0[1] | HSI2C_2_SDA | ALV_DBG[1] | - | - | - | - |
| 69 | XGPIO3 | XGPIO3 | GPG0[3] | HSI2C_3_SDA | ALV_DBG[3] | - | - | - | - |
| 70 | XGPIO0 | XGPIO0 | GPG0[0] | HSI2C_2_SCL | ALV_DBG[0] | - | - | - | - |
| 71 | XSPI1_MISO | XSPI1_MISO | GPP4[2] | SPI_1_MISO | - | - | - | - | - |
| 72 | XSPI1_CLK | XSPI1_CLK | GPP4[0] | SPI_1_CLK | - | - | - | - | - |
| 73 | XSPI1_MOSI | XSPI1_MOSI | GPP4[3] | SPI_1_MOSI | - | - | - | - | - |
| 74 | XSPI1_CSN | XSPI1_CSN | GPP4[1] | SPI_1_CSn | - | - | - | - | - |
| 75 | XGPIO27 | XGPIO27 | GPG3[3] | I2S_0_SDI | MCT1_TICK | - | - | - | - |

# CWAM210S Module Booting Sequence

The section describes the timing associated with powering up and resetting the CWAM210S Module. *Figure 4* depicts the various relevant external (PWR_RST and DC_5V_12V) and internal signaling relations.

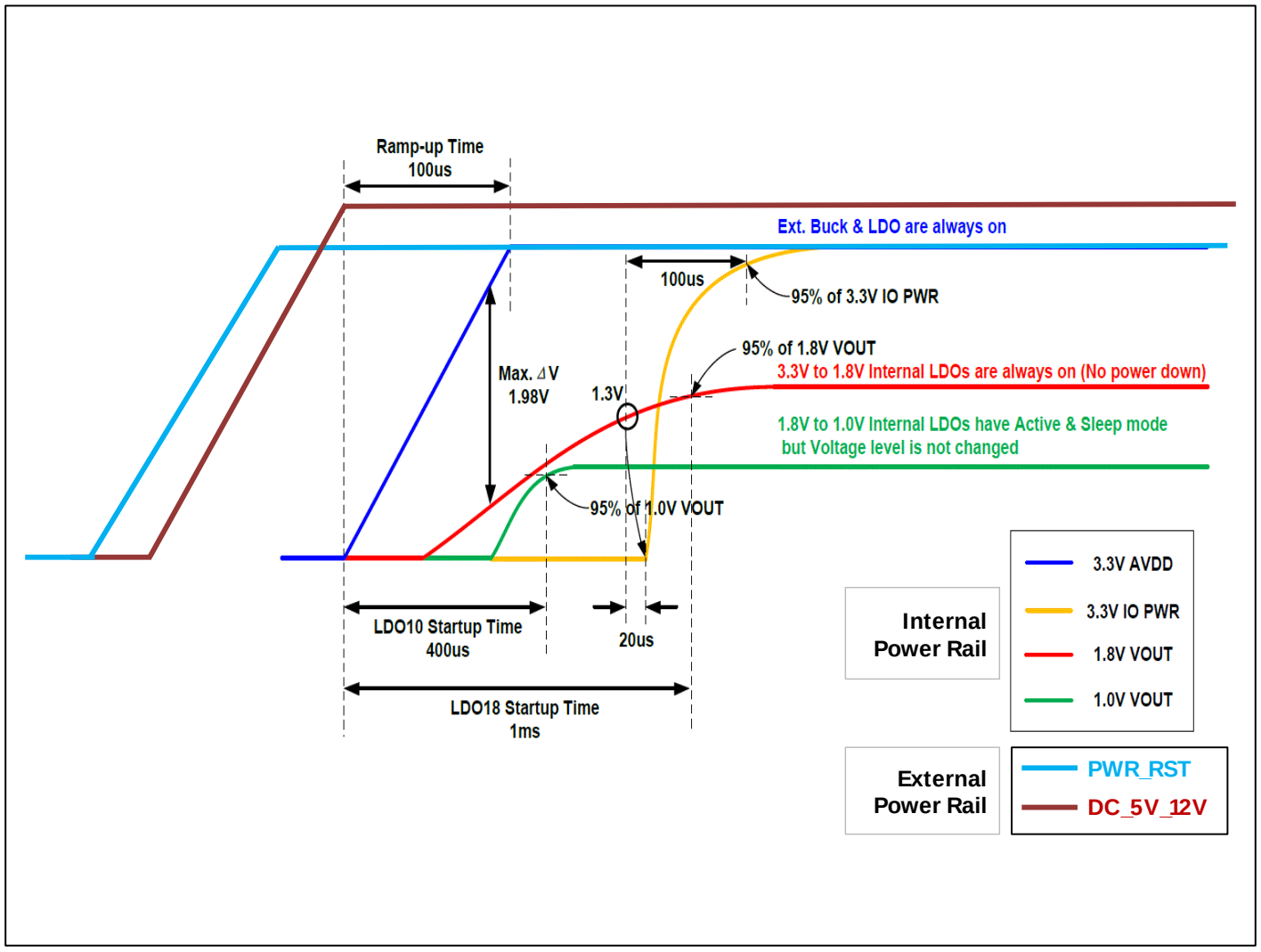


Figure 4. Booting and Reset Timing Relations

# CWAM210S Module Wi-Fi Antenna structure

The CWAM210S Module has an integrated Metal Structural Antenna that operates autonomously. In addition there is an option to attach an external Wi-Fi antenna using a conventional RF connector interface as depicted in *Figure 5*.

**Caution:** Do not apply power (enable) the radio chips before connecting the Wi-Fi antenna or damage to the CWAM210S Module may result.

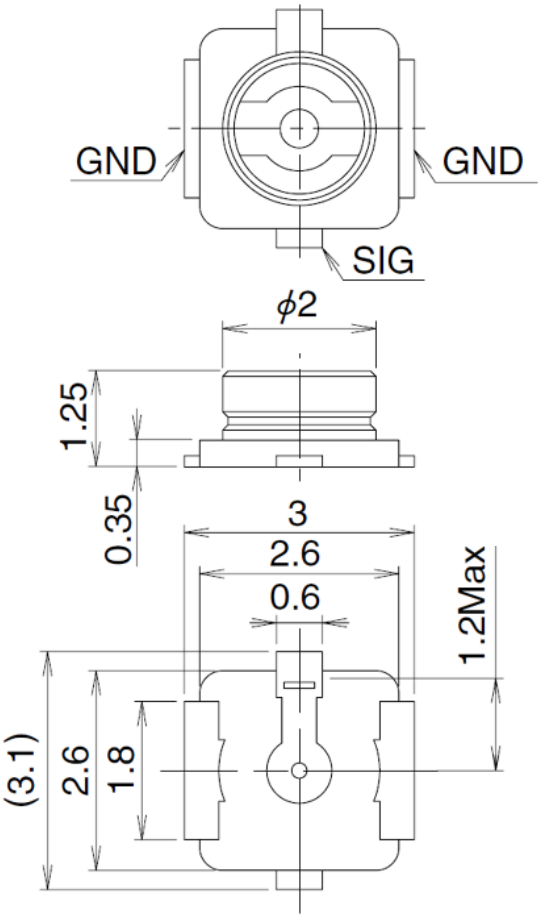


*Figure 5. RF Connector for Wi-Fi Antenna*

The U.FL-R-SMT Hirose connector is used to connect a standard Wi-Fi antenna to the CWAM210S Module. The mechanical size of the connector (receptacle) is described in *Figure 5*. For suggestions on mating plug and more details on the connector, please contact Hirose Electric Co., LTD.

# CWAM210S Module Electrical Specifications

## Absolute Maximum Rating

Table 13. Absolute Maximum Ratings

| PAD:[Pin#] | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PAD:[32] | $V_{IN}$ | Input voltage $V_{IN}$ on the high efficiency step down converter | – | – | 20 | V |
| PAD:[2~19], [21~26], [28~31], [33~45], [48~75] | $V_{undershoot}$ | Undershoot voltage for I/O | -0.3 | – | - | V |
| PAD:[31] | PWR_RST | – | -0.3 | – | 6 | V |
| PAD:[46,47] | $V_{MAX}$ | Based on 3V3 I/O signalling | – | – | 63.3 | V |
| | $I_{MAX}$ | Continuous | – | – | 305 | mA |
| | | | | | | |
| | | Pulsed | – | – | 800 | mA |

## DC Electrical Characteristics

Table 14. I/O DC Electrical Characteristics (PAD:[2-13,18,19],[21-26],[28-31],[33-45],[48-75], I/O)

| Parameter | | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Tolerant External Voltage | $V_{TOL}$ | 3.3 Power Off and On | | – | – | 3.60 | V |
| High-Level Input Voltage | | | | | | | |
| CMOS Interface | $V_{IH}$ | | | 2.31 | – | 3.60 | V |
| Low-Level Input Voltage | | | | | | | |
| CMOS Interface | $V_{IL}$ | $V_{DD}$=3.30V | | -0.30 | – | 0.70 | V |
| Hysteresis Voltage | $\Delta_V$ | | | 0.15 | – | – | V |
| High-Level Input Current | | | | | | | |
| Input Buffer | $I_{IH}$ | $V_{IN}$=3.30V | $V_{DD}$=3.30V Power On | -3.00 | – | 3.00 | µA |
| | | | $V_{DD}$=3.30V Power Off & SNS=0 | -5.00 | – | 5.00 | µA |
| Input Buffer with Pull-Down | | $V_{IN}$=3.30V | $V_{DD}$=3.30V | 13 | 40 | 90 | µA |
| Low-Level Input Current | | | | | | | |
| Input Buffer | $I_{IL}$ | $V_{IN}$=0V | $V_{DD}$=3.30V Power On and Off | -3.00 | – | 3.00 | µA |
| Input Buffer with Pull-Down | | $V_{IN}$=0V | $V_{DD}$=3.30V | -13.00 | – | -90.00 | µA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 2.0mA, 4.0mA, 8.0mA and 12.0mA | | 2.64 | – | 3.30 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = -2.0mA, -4.0mA, -8.0mA and -12.0mA | | 0 | – | 0.66 | V |
| Output Hi-Z Current | $V_{OZ}$ | | | -5 | – | 5 | µA |
| Input Capacitance | $C_{IN}$ | Any input and bi-directional buffers | | – | – | 5 | pF |

Table 15. I/O DC Electrical Characteristics (PAD:[14-17], ADC)

| Parameter | | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High Level Input Voltage | $V_{IH}$ | Guaranteed Logic High Level | 1.26 | – | 1.80 | V |
| Low Level Input Voltage | $V_{IL}$ | Guaranteed Logic Low Level | 0 | – | 0.54 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$=2mA, 4mA, 8mA and 12mA | 1.44 | – | 1.80 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$=2mA, 4mA, 8mA and 12mA | 0 | – | 0.36 | V |
| Input Pull-Up Resistor Current | $I_{RPU}$ | $V_{PAD}$=0 | 15 | – | 77 | µA |
| Input Pull-Down Resistor Current | $I_{RPD}$ | $V_{PAD}$=1.80 | 17 | – | 77 | µA |

| Parameter | | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Hysteresis | $V_H$ | – | 0.18 | – | – | V |
| Input Leakage Current for Non Tolerant Cells | $I_{PAD}$ | $D_{VDD}$=1.80, $V_{PAD}$=0 or 1.80V | -6 | – | +6 | µA |
| Off State Leakage Current | $I_{OZ}$ | $D_{VDD}$=1.80, $V_{PAD}$=0 or 1.80V | -6 | – | +6 | µA |

Table 16. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Main Power Supply: PAD:[32] | DC_5V_12V | 4.50 | – | 18.00 | V |
| Maximum Operating Temperature | $T_O$ | -20 | – | 70 | °C |
| Storage Temperature | $T_S$ | TBD | – | TBD | °C |

Table 17. I/O Drive Strength

| State | | | Currents: worst conditions $V_{DD}$=3.30V | Units |
|---|---|---|---|---|
| DS0 | DS1 | SR: 0: Fast, 1: Slow | | |
| 0 | 0 | 0/1 | 2 | mA |
| 0 | 1 | 0/1 | 4 | mA |
| 1 | 0 | 0/1 | 8 | mA |
| 1 | 1 | 0/1 | 12 | mA |

## DC Module Use Case Characteristics

TBD

## Power Supply Requirements

TBD

## ESD Ratings

Table 18. ESD Ratings

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| ESD stress voltage Human Body Model (JEDEC) | -1.0 | – | 1.0 | kV |
| ESD stress voltage Charged Device Model | – | 250 | – | V |

## AC Electrical Characteristics

Table 19.Level Shifter AC Electrical Characteristics

| PAD:[Pin#] | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PAD:[46,47] | Dynamic Characteristics | | | | | | |
| | $C_{ISS}$ | Input Capacitance | $V_{DS}$=25V, f=1.0MHz, $V_{GS}$=0V | – | – | 50 | pF |
| | $C_{OSS}$ | Output Capacitance | | – | – | 25 | pF |
| | $C_{RSS}$ | Reverse Transfer Capacitance | | – | – | 5 | pF |

## RF Electrical Characteristics

TBD

# CWAM210S Module Mechanical Specifications

In *Figure 6* the mechanical dimensions of the CWAM210S Module are provided. All dimensions are in mm.

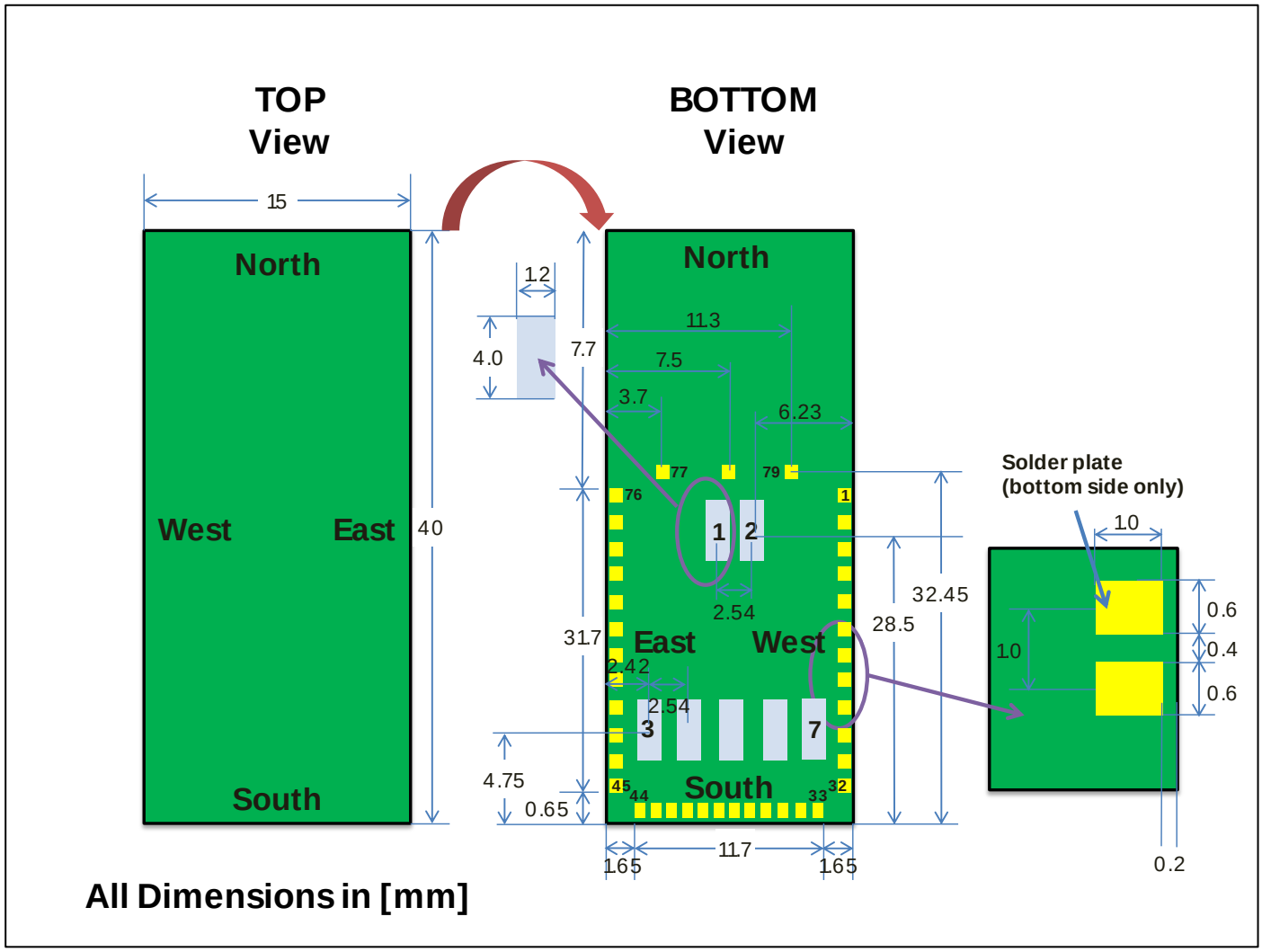


Figure 6. CWAM210S Module Mechanical Dimensions

# CWAM210S Module FCC Certification

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

Caution: Any changes or modifications to the equipment not expressly approved by the party responsible for compliance could void user's authority to operate the equipment. This appliance and its antenna must not be co-located or operation in conjunction with any other antenna or transmitter.

A minimum separation distance of 20cm must be maintained between the antenna and the person for this appliance to satisfy the RF exposure requirements.

**Instruction to OEM**

This device complies with Industry Canada's license-exempt RSSs. Operation is subject to the following two conditions:

1. This device may not cause interference and
2. This device must accept any interference, including interference that may cause

undesired operation of the device. This application and its antenna must not be co-located or operation in conjunction with any other antenna or transmitter. A minimum separation distance of 20cm must be maintained between the antenna and the person for this appliance to satisfy the RF exposure requirements. Host labeling requirement: "Contains transmitter module

FCC ID: A3LCWAM210S
IC : 649E-CWAM210S "

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

**WARNING & SAFETY INFORMATION**

*Safety Symbols*

*Warning*

- When encountering this symbol in the manual, you must follow these recommendations to avoid irreparable damage to your car, system or connected devices or to avoid accidents with injuries or death.

**IC Information**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:
(1) this device may not cause interference, and
(2) this device must accept any interference, including interference

Le present appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.
L'exploitation est autorisee aux deux conditions suivantes :
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioelectrique subi, meme si le brouillage est susceptible d'en compromettre le fonctionnement.

The antenna(s) used for this device must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

*FCC Information*

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

*FCC notification to users*

This equipment has been tested and found to comply with the limits for a CLASS B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference, the user is encouraged to try to correct the interference by consulting with a dealer or an experienced technician for technical assistance.

Any changes or modifications to the equipment not expressly approved by the party responsible for compliance could void user's authority to operate the equipment.

# CWAM210S Module Ordering Information

| Type | Order Number | Description |
|---|---|---|
| CWAM210S Module | ?? | One CWAM210S Module |
| CWAM210S Evaluation Kit | ?? | One CWAM210S Module<br>One EVK Board<br>One Wi-Fi Antenna |

For volume ordering of evaluation kits, please contact a sales representative in your area or email *sales@artik.io*.

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