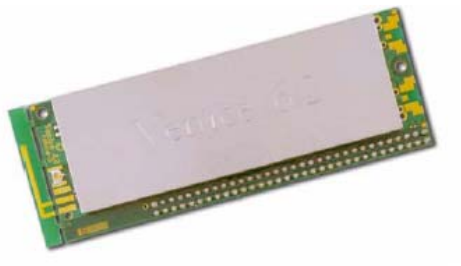
Venice6.2 Internet radio/Network streaming/DAB+/FM Module



General description

The Venice 6.2 FS2026-2 module is a complete hardware and software solution for Internet radio, network streaming, UPnP, premium content services, DAB/DAB+ and FM-RDS products. It provides the simplest and lowest-cost solution for high-quality audio streaming from live Internet radio stations or network-based music collections.

Venice 6.2 has been designed as part of a complete system including IR 2.0 software and the Jupiter 6.2 platform. Products based on these components may achieve compliance with a number of industry standards.

Several configurations are available, with different combinations of integrated RF receivers for Wi-Fi networks, DAB Band 3, L-Band and FM reception.

Based around Frontier Silicon's powerful Chorus 2 processor, Venice 6.2 streams radio stations and music files in a variety of formats and protocols including MP3, Windows® Media Audio (WMA), RealAudio, WAV and FLAC, enabling a new generation of stand-alone network-based audio products.

Applications include a wide range of audio products, from kitchen and alarm clock radios to CD micro systems, boomboxes and HiFi tuners.

Key features

- Simple registration and configuration via
  - remote control
  - front panel
  - Web portal
- DRM (digital rights management) for protected music files
- Clock/alarms
- UPnP™ support
- On-board Wi-Fi antenna for easy integration in final products
- Automatically upgradeable in the field through Internet/Wi-Fi connection or USB

Modes

- Live Internet radio broadcasts
- Podcast and "listen again" on-demand content
- Premium streaming services such as Last.fm, Pandora, Rhapsody[1] and Sirius Internet Radio
- Network streaming with playlist capability
- DAB/DAB+ Digital Audio Broadcast radio
- DMB-Audio[1]
- FM radio reception with RDS
- Audio playback from USB memory stick

Connectivity

- USB 2.0 device or host
- 802.11b/g Wi-Fi with WEP/WPA/WPA2 security
- Analogue audio output from onboard DAC
- Digital audio outputs - I^2S and S/PDIF, supporting external DACs
- LCD interface supports range of display types
- Keyboard presets, rotary encoder
- Support for infrared remote control
- Support for external SPI 10/100 Mbit/s Ethernet

Ordering information

Part		Wi-Fi Net audio	DAB		FM
			Band 3	L-Band	
FS2026-2	W	•			
	WB	•	•		•
	WD	•	•	•	•
	WF	•			•

1. Available on request

1 Introduction

Figure 1 shows a block diagram of the Venice 6.2 module. The main components are the Wi-Fi transceiver, Apollo 2 FS1112 tri-band RF front end, Chorus 2 FS1020 processor, serial boot Flash and audio DAC. For more information on the connectors (J4 - J8), see *Chapter 3: Hardware interfaces*.

The Chorus 2 processor is an extremely flexible baseband receiver covering a number of physical layer standards, particularly those utilising COFDM modulation. The baseband signal processing is achieved using a blend of hardware and software to optimise trade-offs between power, cost and flexibility.

Venice 6.2 measures 40 x 112.5 mm (with on-board PIFA Wi-Fi antenna) or 40 x 107 mm (without antenna). The underside of the module has a solid copper ground plane and all components are fitted on the top. With the exception of the connectors and screw holes, all components are fitted inside the 4-chamber screen can. This screens and isolates the broadcast RF, Wi-Fi, baseband and DAC sections from each other.

2 Applications

Venice 6.2 is designed to work in different applications in either master or slave mode. The 64-way pin connector available on the module provides a range of functionalities which can be interfaced to drive different peripherals to form a full system.

This chapter presents typical applications using Venice 6.2.

2.1 Master mode

Figure 2 shows Venice 6.2 in master mode, functioning as the main system controller in the radio.

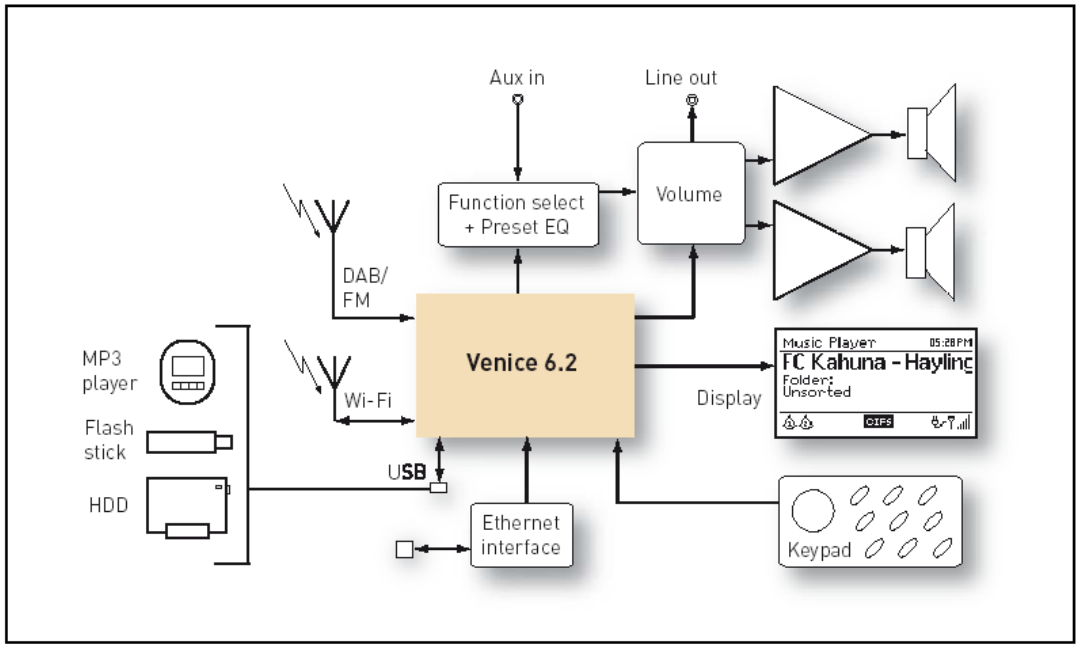


Figure 2: Master mode application

2.2 Slave mode

Figure 3 shows an example application with Venice 6.2 in slave mode.

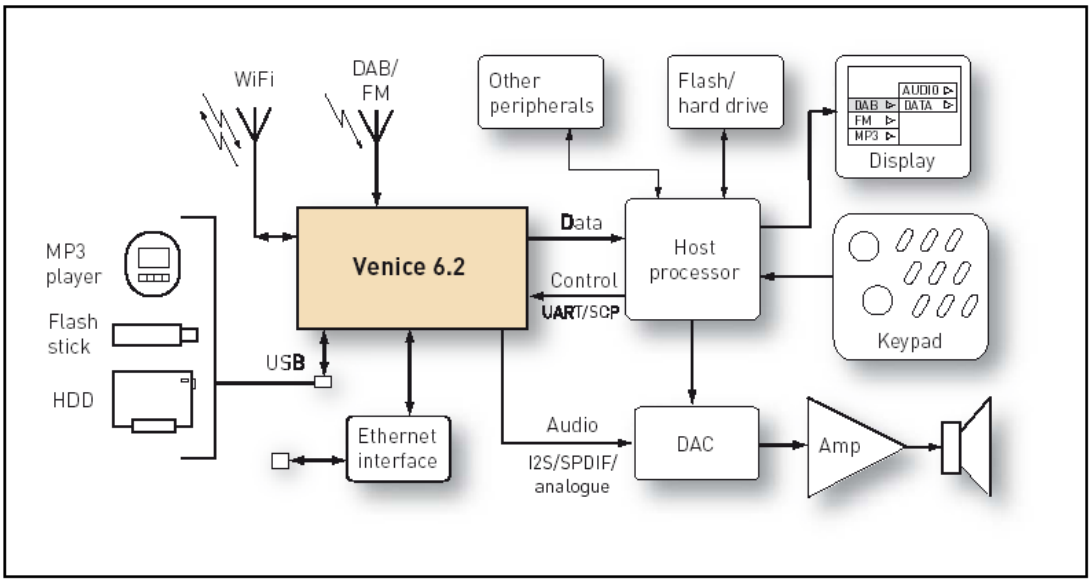


Figure 3: Slave mode application

3 Hardware interfaces

This chapter describes the various hardware interfaces of Venice 6.2.

Note: 1 Some interfaces are mutually exclusive.

2 There is no JTAG/debug connector option, in order to ensure compliance with DRM standards.

Figure 4 shows the module's connector locations, and the pin numbering scheme of the main 64-way connector, J8.

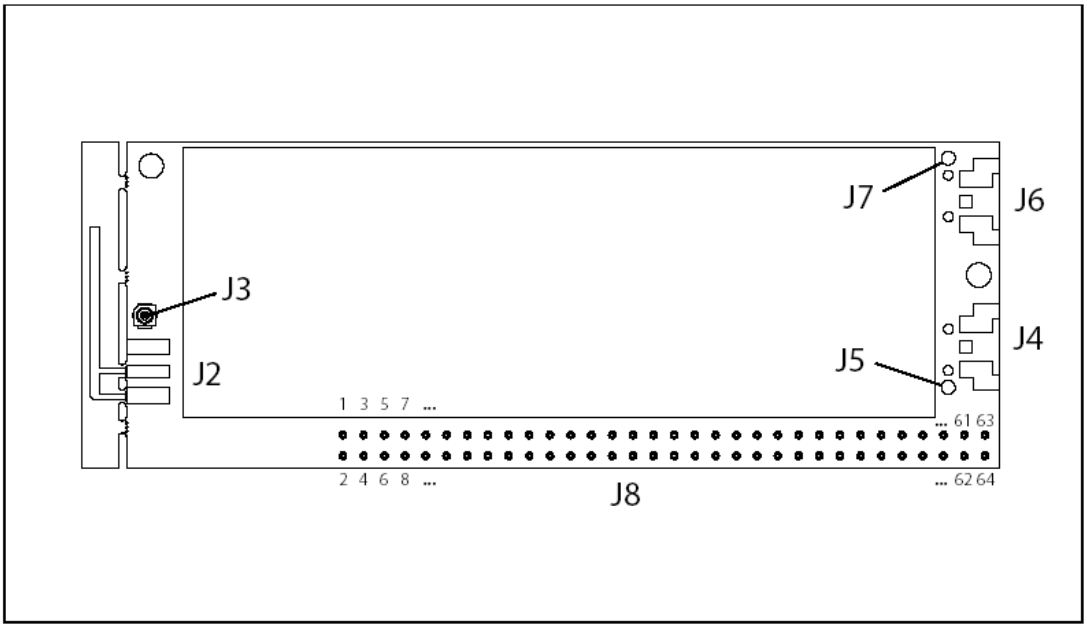


Figure 4: Connector locations and J8 pin numbering scheme

3.1 Main connector pin assignments

Table 2 shows the J8 (main connector) pin assignments.

Pin	Name	Usage
2	3V3 Supply	3.3 V supply
4	Ground	Ground
6	SCP2_CLK	SCP interface
8	GPIOE10	GPIO
10	S1_DIN	UART
12	USBDP	USB2
14	USB VBUS	USB2
16	USB_VBUS_DRIVE	USB2
18	GPIOG3	Keyboard ROW 1
20	GPIOG5	Keyboard ROW 3
22	GPIOG7	Keyboard ROW 2
24	GPIOG10	Keyboard ROW 4
26	SPI1_CSn2_SD card	SPI/SD Card
28	SPI1_MOSI	SPI/SD Card
30	Ground (SPI)	Ground (SPI)
32	SPDIFOUT	S/PDIF out
34	SD_DETECT	SD_DETECT
36	LCD_F_VSYNC	Parallel LCD control
38	LCD_PE_CLK	Parallel LCD control
40	LCD_DAT0	Parallel LCD data 0
42	LCD_DAT2	Parallel LCD data 2
44	LCD_DAT4	Parallel LCD data 4
46	LCD_DAT6	Parallel LCD data 6
48	Ground (I^2S)	Ground (I^2S)
50	AUD_SFR	I^2S serial audio frame
52	AUD_SDOUT0	I^2S serial audio data out
54	GPIOG15	Rotary encoder 2
56	GPIOH3	GPIO
58	GPIOG11	Rotary Encoder 4
60	GPIOG14	Rotary Encoder 1
62	Ground	Ground
64	AUD_L	Audio L

Pin	Name	Usage
1	1V2 Supply	1.2 V supply
3	Ground	Ground
5	SCP2_DATA	SCP interface
7	GPIOE11	GPIO
9	S1_DOUT	UART
11	USBDM	USB2
13	Ground (USB)	Ground (USB)
15	USB_VBUS_FAULT	USB2
17	GPIOB11	Keyboard COL 3
19	GPIOB12	Keyboard COL 1
21	GPIOB13	Keyboard COL 4
23	GPIOB14	Keyboard COL 2
25	GPIOB8	GPIO
27	SPI1_MISO	SPI/SD Card
29	SPI1_SCLK	SPI/SD Card
31	SYS_nRST	SYS_nRST
33	SD_PROTECT	SD_PROTECT
35	LCD_M_HSYNC	Parallel LCD control
37	LCD_LRS_EN	Parallel LCD control
39	Ground (LCD)	Ground (LCD)
41	LCD_DAT1	Parallel LCD data 1
43	LCD_DAT3	Parallel LCD data 3
45	LCD_DAT5	Parallel LCD data 5
47	LCD_DAT7	Parallel LCD data 7
49	AUD_MCLK	I^2S audio master clock
51	AUD_SCLK	I^2S serial audio data clock
53	GPIOD4	GPIO
55	GPIOH4	GPIO
57	GPIOG13	Rotary Encoder 3
59	GPIOG8	IR Remote/GPIO
61	Audio Ground	Audio Ground
63	AUD_R	Audio R

Table 2: J8 (main connector) pin assignments

3.2 DAB/DAB+/FM broadcast antenna inputs

The two RF broadcast antenna inputs support any combination of Band 2, Band 3 and L-Band. Both have an impedance of 75 Ω.

- J6/J7 is the combined antenna input for all wavebands.
- J4/J5 is an optional separate L-Band input.

Antenna connector options are described in *Chapter 5: Hardware build options*, *Section 5.2: Broadcast radio*.

3.3 Wi-Fi antenna

The module's Wi-Fi block both transmits and receives IEEE 802.11 b/g signals. Antenna/connector options are described in *Chapter 5: Hardware build options*, *Section 5.3: Wi-Fi antenna connectivity*.

3.4 Analogue audio output

The onboard audio DAC provides an analogue stereo line-level output. *Table 3* lists the specifications.

Parameter	Min	Typ	Max	Units	Comments
Load resistance	3.0			kΩ	To mid-rail or AC coupled
Signal level		0.6		V_{RMS}	into 10 kΩ
THD (full scale)		0.01	0.02	%	THD full scale
SNR	95	97	102	dB	3.3 V supply
3 dB audio bandwidth (referenced to 1 kHz level)	< 20		20000	Hz	DAB mode
			12500	Hz	FM mode

Table 3: Audio analogue output specifications

3.5 Digital audio outputs

3.5.1 I²S

The I²S bus is suitable for driving an external DAC or codec. The sample rate is 48 kHz.

Pin number	Pin name	Pin description	Notes	Alternate usage	Drive capability, mA
49	AUD_MCLK	I²S audio master clock	512 x sample rate, i.e. 24.576 MHz	GPIO	2
50	AUD_SFR	I²S serial audio frame	32/48/64 bits (2 channels)		
51	AUD_SCLK	I²S serial audio data clock	Generated with appropriate extra clocks for 16-bit data in 32-bit frame etc.		
52	AUD_SDOUT0	I²S serial audio data out	MSB first; left justified or right justified 16/18/20/24 bits		

Table 4: Digital audio output

I²S connectivity options are described in *Chapter 5: Hardware build options*, *Section 5.5: I2S connectivity*

3.5.2 S/PDIF

The S/PDIF audio output carries a stereo digital audio output on a single wire using the signal format defined in IEC60958 *[reference 16]*.

Pin number	Pin name	Pin description	Alternate usage	Drive capability, mA
32	SPDIFOUT	S/PDIF out	-	4

Table 5: S/PDIF audio output

3.6 LCD port

The Venice 6.2 parallel LCD interface uses four control and eight data lines, as shown in *Table 6*. Both parallel interface and serial SPI/SCP displays can be supported.

Pin number	Pin description	Pin usage	Alternate usage	Drive capability, mA
35	LCD_M_HSYNC	Parallel LCD control	GPIOD15	8
36	LCD_F_VSYNC	Parallel LCD control	GPIOD14	
37	LCD_LRS_EN	Parallel LCD control	GPIOD13	
38	LCD_PE_CLK	Parallel LCD control	GPIOD12	
39	LCD ground	LCD ground	-	-
40	LCD_DAT(0)	Parallel LCD data 0	GPIOF0	8
41	LCD_DAT(1)	Parallel LCD data 1	GPIOF1	
42	LCD_DAT(2)	Parallel LCD data 2	GPIOF2	
43	LCD_DAT(3)	Parallel LCD data 3	GPIOF3	
44	LCD_DAT(4)	Parallel LCD data 4	GPIOF4	
45	LCD_DAT(5)	Parallel LCD data 5	GPIOF5	
46	LCD_DAT(6)	Parallel LCD data 6	GPIOF6	
47	LCD_DAT(7)	Parallel LCD data 7	GPIOF7	

Table 6: LCD port interface

3.7 Asynchronous serial port (UART)

The UART provides a standard asynchronous serial port with a maximum speed of 115200 baud.

Pin number	Pin description	Alternate usage	Drive capability, mA
9	S1_DOUT	GPIO	2
10	S1_DIN		

Table 7: Asynchronous serial port (UART)

3.8 Serial control port (SCP)

The SCP is a bidirectional, 2-wire, open collect bus and may be used by a host to control Venice 6.2. The functionality of the SCP is master/slave transmitter/receiver in standard or fast mode (100/400 kHz). Multi-master operation is not supported. The SCP pins are 5 V-tolerant.

Pin number	Pin description	Alternate usage	Drive capability, mA
5	SCP2DATA	Display control	4
6	SCP2CLK		

Table 8: Serial control port (SCP)

3.9 SPI/SD card/Ethernet interface

The serial peripheral interface (SPI) pins can be used to interface the Venice 6.2 module to an SD card (connected in SPI mode), an SPI display or an Ethernet chip.

Table 9 shows the SPI signals.

Pin number	SPI mode	Alternate usage	Drive capability, mA
5	SPI2_CSn	SCP2_DATA	4
6	SPI2_SCLK	SCP2_CLK	
7	SPI2_SO	GPIO	2
8	SPI2_SI		
26	SPI1_CSn2_SD card	GPIO	8
27	SPI1_MISO		
28	SPI1_MOSI		
29	SPI1_SCLK		

Table 9: Serial peripheral interface (SPI)

Table 10 shows the SD card signals.

Venice 6.2 J8		SD card	
Pin number	Pin name	Pin number	Pin name
26	SPI_CSn2_SDcard	1	Card detect DAT3
28	SPI1_MOSI	2	Command/response
3/4/62	Ground	3	Ground
2	3V3 Supply	4	Supply voltage
29	SPI1_SCLK	5	Clock
3/4/62	Ground	6	Ground
27	SPI1_MISO	7	Data bit 0
-	-	8	Data bit 1
-	-	9	Data bit 2
34	SD_DETECT	-	Detect
3/4/62	Ground	-	Protect/detect
33	SD_PROTECT	-	Protect

Table 10: SD card interface

For information about Ethernet support see the Venice 6.2 *Application Note [reference 4]*.

3.10 Infrared remote

An infrared remote (IR) interface is present on the main connector, J1.The Philips RC5 IR protocol is supported.

Pin number	Pin description	Alternate usage	Drive capability, mA
59	IR remote	GPIO	8

Table 11: Infrared remote

3.11 USB 2.0 interface

The USB 2.0 interface supports both device and host operation in full speed mode (12 Mbit/s).

Pin number	Pin description	Alternate usage
11	USBDM	USB2
12	USBDP	
13	GND (USB)	
14	USB VBUS	USB2
15	USB_VBUS_FAULT	
16	USB_VBUS_DRIVE	

Table 12: USB 2.0 interface

Table 13 lists the The USB parameters.

Parameter	Min	Typ	Max	Units
High level output voltage			3.6	V
Low level output voltage	0.6			
Pin current		0.45		mA

Table 13: USB parameters

3.12 General purpose I/O and keyboard

There are 18 dedicated GPIO lines, but as described above, many of the other digital interfaces have alternative usage as additional GPIO. The default GPIO usage is:

- 8 lines are used for a 4 x 4 keyboard matrix
- 4 lines are used for 2 rotary encoders
- 6 lines are spare.

Each GPIO line may be configured by software as an input or output. The state of each GPIO input can be read by software. The logic level and tri-state drive of each GPIO output can be controlled by software.

Figure 14 shows GPIO driver capability.

Pin numbers	**Drive capability**, mA
7 -10	2
17 - 29	8
32	2
33 - 47	8
49 - 52	2
53 - 60	8

Table 14: GPIO driver capability

4 Power supplies

4.1 Requirements

Venice 6.2 requires regulated power supplies: 1.2 V ± 10% supply for the digital baseband circuits and 3.3 V ± 5% for the RF circuits, audio DAC and other blocks. Both supplies should be clean with low ripple. Any noise on these supplies will affect performance.

Table 15 shows power supply requirements for the main module variants. Power consumption however depends on several factors; see *Section 7.2.2: Power consumption*.

Product variant		Supply voltage, V	Current, mA		Power, W	
			Typ	Max	Typ	Max
FS2026-2	W (Wi-Fi only)	1.2	180	350	1.1	2.2
		3.3	260	550		
	WB WD WF (Wi-Fi/DAB/FM)	1.2	180	500	1.2	2.75
		3.3	300	650		

Table 15: Module variant power supply requirements (PRELIMINARY, TBC)

Venice 6.2 includes some internal filtering on the power supply lines. This takes the form of a Pi network with a ferrite bead inductor in the supply line with one or more capacitors to ground on either side.

The power supply needs to cope with peak power requirements in excess of those stated in *Table 15*, due to the burst requirements of the DAB receiver. Suitable bulk decoupling can help provide this and also reduce noise and ripple. The regulators and capacitors should be mounted as close as possible to J8. Use a solid ground plane if possible; otherwise use large tracks with the ground connections from each regulator joining close to the module.

4.2 Power-on/reset timing and operation

Supply line rise ordering

CAUTION: During power-up, the 3.3 V supply line must reach 1.2 V before the 1.2 V supply, otherwise a damaging latch condition may occur.

The 3.3 V supply must rise before the 1.2 V supply. This can be arranged via ordering of the linear regulators, scaling of decoupling capacitors, or by use of reset management chips (where the 1.2 V regulator has an enable).

When in slave mode, Venice 6.2 sends a 'Command Reset' message over the serial interface to indicate when boot is completed and it is ready to accept commands from the host.

Reset

Venice 6.2 can be reset either internally/automatically through its power-on reset circuitry, or externally by use of the SYS_nRST signal. Once reset, Chorus 2 optionally starts its self-test and then boots.

The reset pin, SYS_nRST, is open drain and has a 60 kΩ weak pull-up internal to Chorus 2.

Internal reset

When Venice 6.2 has powered-up, the Chorus 2 power-on reset (POR) circuit holds the module in reset for approximately 200 µs. During this time the SYS_nRST pin is driven low. After reset completes, the SYS_nRST pin releases, allowing the signal to go high

External reset

SYS_nRST can be pulsed externally to reset the module, or held low indefinitely, which keeps the module in a forced reset state. The reset pulse (T_{RST}) must be applied only after the 1.2 V supply has reached at least 0.95 V, and be of minimum duration 200 µs.

Timing diagram

Figure 5 shows the relationship between the power supplies and SYS_nRST during proper power supply sequencing and an internal POR reset. A 10 kΩ pull-up resistor is connected to SYS_nRST.

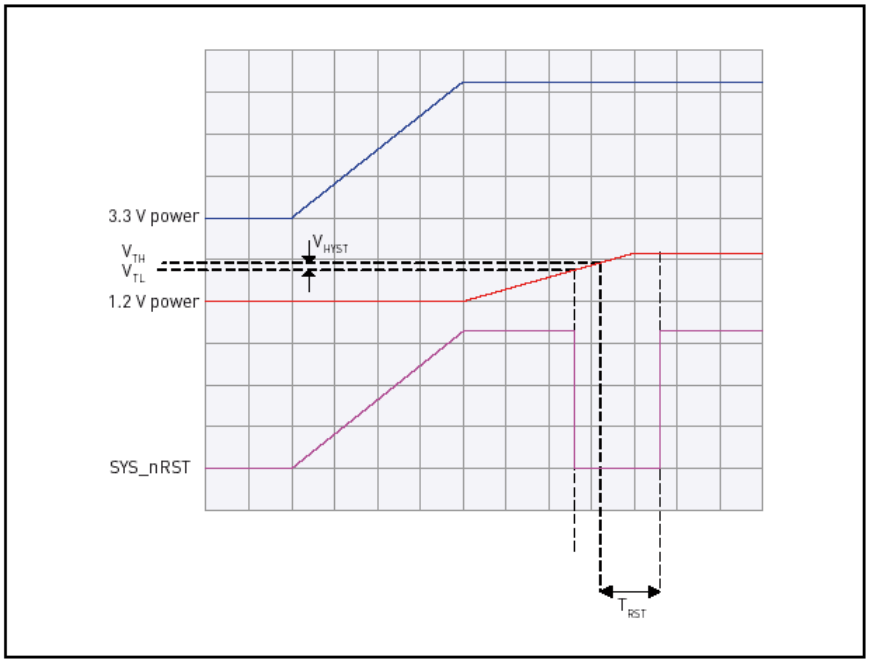


Figure 5: Ideal power up sequence/POR timing diagram

Symbol	Parameter	Min	Typ	Max	Units
V_{TH}	Reset threshold rising level	864	950	1036	mV
V_{TL}	Reset threshold falling level	819	900	981	
V_{HYST}	Reset threshold hysteresis	49	50	51	
T_{RST}	Reset pulse duration (V to SYS_nRST = 1)	116	197	316	µs

Table 16: Chorus 2 reset parameters

Note: 1 Over the temperature range from 0°C to +70°C.

2 VTH and VTL move together from a threshold point of view.

4.3 Power-off timing

Venice 6.2 is designed so that the power can be removed in any order at any time without affecting the module. However, when in slave mode, the host must allow enough time to process the last command sent before powering-down the module (400 ms).

5 Hardware build options

Venice 6.2 has been designed for flexibility in application and use. The following build options are available.

5.1 Main variants and functionality

Part		Wi-Fi Net audio	DAB		FM
			Band 3	L-Band	
FS2026-2	W	•			
	WB	•	•		•
	WD	•	•	•	•
	WF	•			•

Table 17: Venice 6.2 main variants and functionality

5.2 Broadcast radio

Reception

As shown in *Table 17*, Venice 6.2 can be supplied with or without broadcast radio reception components for DAB/DAB+/FM.

Dual- or tri-band

Venice 6.2 can be supplied in dual- or tri-band versions, for Bands 2 and 3 (WB), or Band 2, Band 3 and L-Band (WD).

The WD tri-band variant may be configured to accept all antenna inputs on J6/J7, or may alternatively use J4/J5 as a dedicated L-Band input.

Connectors

J4/J6, the DAB/FM RF antenna inputs, can be fitted with any of the following RF connectors:

- 2.6 mm UMP,
- F-Type,
- SMA,
- SMB,
- none.

Alternatively, connections can be made to J5/J7 with coaxial pig-tail flying lead(s).

5.3 Wi-Fi antenna connectivity

The standard Wi-Fi configuration is to use the integral board-mounted PIFA linked via J2 to the Wi-Fi radio block. Alternatively, the PIFA can be removed to allow an RF connector or cable to be fitted to J2/J3.

NOTE: For the present case the on board PIFA was removed and an external antenna was connected via a 50Ω flying lead.

5.4 SDRAM memory

Venice 6.2 can be supplied with 16 Mbytes or 32 Mbytes of SDRAM. This corresponds to standard and premium variants of the IR 2.0 software.

5.5 I^2S connectivity

The four I^2S digital audio output signals are connected to J8 via links. If neither the I^2S interface nor its alternate GPIO functions are required, these links may be left unfitted; this may improve EMC performance depending on implementation.

6 Performance characteristics

6.1 Introduction

Venice 6.2 supports 802.11b/g Wi-Fi connectivity.

Venice 6.2 is a Eureka 147 DAB receiver to EN61000-4-2 supporting:

- Band 3 (174.928 - 239.20 MHz) and Korean Band 3 (175.280 - 214.736 MHz)
- L-Band (1452.960 - 1490.624 MHz)

with typical performance equal to or better than EN50248:2001 *[reference 13]*.

Venice 6.2 supports Band 2 Soft FM (87.5 MHz to 108 MHz) and meets parts of the BS 5942-2:1987 Hi-Fidelity minimum performance when tested to BS 60315-4 *[reference 14]*.

The figures in the following sections are for conditions:

T_A = 25°C;
voltage supplies are 1.2 V and 3.3 V.

6.2 Wi-Fi performance

Venice 6.2 supports the mandatory modes required by 802.11b and 802.11g plus some optional modes, as listed in *Table 18*. The maximum transmit power of the Wi-Fi module is limited to 20 dBm.(output power)

Standard	Mode	Bit rate, Mbit/s	Receiver sensitivity		
			Min	Typ	Units
802.11b	DSSS	1	-79	-93	dBm @ 8%PER
	DSSS	2	-79	-93	
	HR/DSSS	5.5	-79	-92	
	HR/DSSS	11	-79	-87	
802.11g	ERP-OFDM	6	-82	-86	dBm @10% PER
		9	-81	-85	
		12	-79	-85	
		18	-77	-84	
		24	-74	-80	
		36	-70	-79	
		48	-66	-73	
		54	-65	-72	

Table 18: Wi-Fi performance

6.3 RF performance

6.3.1 DAB Band 3

Operating mode = decoding one DAB stereo audio channel at 192 kbit/s)

Parameters		Min	Typ	Max	Units
Tuning range	Band 3	175.280	-	214.736	MHz
	Korean Band 3	174.928	-	239.200	
Large signal handling capacity		-5	0		dBm
Sensitivity		-95	-97		
Far off selectivity		40			dB
Adjacent channel rejection		30	40		

Table 19: Band 3 performance

6.3.2 DAB L-Band

6.3.3 Operating mode = decoding one DAB stereo audio channel at 192 kbit/s)FM

Parameters		Min	Typ	Max	Units
Tuning range	L-Band	1452.960	-	1490.624	MHz
	Canadian L-Band	1452.816	-	1491.184	
Large signal handling capacity		-5	0		dBm
Sensitivity		-95	-97		
Far off selectivity		40			dB
Adjacent channel rejection		30	38		

Table 20: L-Band performance

Operating mode = decoding one FM stereo audio channel at ± 67.5 kHz with 1 kHz tone.

Parameters	Min	Typ	Max	Units
Tuning range	89.5	-	108	MHz
Sensitivity (S+N)/N=26dB	-106	-108	-	dBm
Large signal handling capacity	-	0	-	
(S+N)/N ultimate signal-to-noise ratio	-	50	-	dB
THD	-	0.3	-	%
Tuning step size	-	50	-	KHz
FM selectivity	30	40	-	dB
Stereo separation	25	40	-	

Table 21: FM performance

6.4 Audio specification

The audio frequency response (-3dB) is 20 Hz - 12.5 kHz (FM) and 20 Hz - 20 kHz (DAB). In DAB mode, a typical SNR of 99 dBA is achieved, worst case 97 dBA. This is dependant on the load applied.

7 Electrical specification

7.1 Absolute maximum ratings

CAUTION: Exceeding these values may damage the module.

Parameter	Min	Typ	Max	Units	Comments
3.3 V power terminal	-0.3	3.3	4.0	V	
1.2 V power terminal	-0.3	1.2	1.32		
V_{IN}	-0.3		5.5	V	Other than supply pins
Storage temperature	-40		+85	°C	
I_{OUT}			100	mA	Total for all I/O
Humidity	0		90	%	Non-condensing
RF input			+10	dBm	
Other inputs	-0.3		3.6	V	
Outputs	-20		+20	mA	

Table 22: Absolute maximum ratings

7.2 Typical values

All figures are stated for a temperature of 25 °C.

7.2.1 Power supply voltage range

Table 23 shows the power supply voltage ranges.

Parameter		Min	Max	Units
Power supply voltage range	3.3 ± 5%	3.135	3.5	V
	1.2 ± 10%	1.08	1.32	

Table 23: Power supply voltage ranges

7.2.2 Power consumption

Table 24 shows typical power consumption; this depends on the operating mode, data rates and module variant (see *Chapter 5: Hardware build options*). These figures include GPIO driving current to the display, but not the display backlight, the current for which is supplied externally to the module. Maximum power supply requirements are shown in *Chapter 4: Power supplies*.

Mode		Current consumption, mA		Total power consumption, W
		1.2 V rail	3.3 V rail	
Standby				< 1.0
Soft FM		180	160	0.75
DAB		160	160	0.72
DAB+				
Wi-Fi Internet radio/ music player	FS2026-2 W (Wi-Fi only)	180	260	1.1
	FS2026-2 WB/WD/WF (Wi-Fi/DAB/FM)	180	300	1.2

Table 24: Typical power consumption (PRELIMINARY, TBC)

7.2.3 Main signal levels

Parameter	Min	Typ	Max	Units
LOW level input voltage	-0.3	0.1	0.8	V
HIGH level input voltage	2	3.3	5.5	
Input leakage current	-10		+10	µA

Table 25: Main signal levels

Notice: The user should not modify or change this equipment without written approval form SANGEAN ELECTRONICS INC. Modification could void authority to use this equipment.

Label for end product must include “Contains FCC ID: BYG021” or “A RF transmitter inside, FCC ID: BYG021”.

FCC ID Label Graph:

FCC ID: BYG021 Model: Venice6.2

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Note:

If the product is too small to make so many text labels, only need to indicate the FCC ID number on the label, but the above text will be printed in the manual or packaging box.

IMPORTANT NOTE: To comply with the FCC RF exposure compliance requirements, the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. No change to the antenna or the device is permitted. Any change to the antenna or the device could result in the device exceeding the RF exposure requirements and void user’s authority to operate the device.

The module has been regulatory approved for integrations which meet the following conditions:

1. The radio integration is embedded
2. The antenna must be installed such that 20 cm is maintained between the antenna and users
3. The ‘Type’ and ‘Gain’ of the antenna selected for the integration of the external antenna must meet the requirements as detailed in section.

Used outside of these conditions will trigger re-approval.