Product Technical Specification

Q2686 Wireless CPU®

Reference: **WM_PRJ_Q2686_PTS_001**

Revision: **010**

Date: **June 30, 2009**

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Q2686 Wireless CPU®

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Reference: WM_PRJ_Q2686_PTS_001
Revision: 010
Date: June 30, 2009

Supports Open AT® embedded ANSI C applications

Document History

Level	Date	List of revisions	
001	01/17/2005	Creation (Preliminary version)	
002	06/01/2005	Pin-out modification (see chapter 3.1)	
003	15/09/2005	Update Functional architecture Pin-out modification (see chapter 4.1) Add RESET state of all IOs of all interfaces Update power supply range (see chapter 3.2) Update electrical information for digital IO (see chapter 3.2) Update SPI bus configuration (see chapter 3.4) Remove 3 GPIO (see chapter 3.9) Change MIC1 biasing voltage configuration (see chapter 3.11) Change SPK1 definition to only single-ended (see chapter 3.11) Update ON/ŌFF operating sequence (see chapter 3.14) Update BOOT definition (see chapter 3.15) Update ~RESET operating sequence and electrical characteristics (see chapter 3.14) Update Interrupt activation (see chapter 3.17) Update RTC electrical characteristics (see chapter 3.19) Update PCM description and add waveform (see chapter 3.21)	
004	November 22, 2005	Update Q2686 version "Overview" section Update "Cautions", "Trademarks" and "Copyright" Update "Electrical information for digital I/O" (see chapter 3.3) Update SPI max frequency (see chapter 3.4) Update available GPIO (see chapter 3.9) Add "OFF state" voltage caution (see chapter 3.2) Update "Battery charging interface" (see chapter 3.13) Update "Analog audio interface" (see chapter 3.11) Update "Environmental Specifications" (see chapter 4.2) Update "General Purpose Connector pin-out description" (see chapter 4.1)	
005	February 2006	Update "PCM interface" waveform (see chapter 3.21) Update "Electrical information for digital IO" absolute maximum rating (see chapter 3.3) Update "General purpose connector" (see chapter 3.1) Update "SPI bus" speed (see chapter 3.4.1) Update "I²C bus" (see chapter 3.4.2) Update "Main serial link UART 1" maximum speed (see chapter 3.6) Update "Auxiliary serial link UART 2" maximum speed (see chapter 3.7) Update "SIM" General description (see chapter 3.8.1) Update "USB 2.0 interface" features (see chapter 3.22) Update "Operating system upgrade" (see chapter 6.3) Update "General purpose input/output" signals description (see chapter 3.9) Update "General purpose connector pin-out description" signal description (see chapter 4.1) Update "Battery charging interface" (see chapter 3.13) Update "Analog to µDigital Converter" (see chapter 3.10) Update "FLASH-LED signal" (see chapter 3.20)	

Level	Date	List of revisions	
		Update 'Analog Audio interface" (see chapter 3.11)	
006	March 2006	Update "Power consumption" (see chapter 3.3.2) Update "ON/~OFF signal" (see chapter 3.14) Update "BAT-RTC" (see chapter 3.19) Update "Electrical information for digital IO" absolute maximum rating (see chapter 3.3) Update "Buzzer output", remove PWM features (see chapter 3.12) Update "EMC recommendation" add ESD recommendations (see chapter 6.1.1) Update "SPI bus" add waveforms (see chapter 3.4.1) Update "I²C bus" add waveforms (see chapter 3.4.2) Update "Analog to Digital Converter" sampling rate (see chapter 3.10)	
007	March 2007	Modification of the ON/ ~OFF paragraph Add ATEX 94/9/CE directive information in section 4.4 Update reference documents Update section 3.6 "Main serial link (UART1)" Other minor corrections	
008	June 2008	Software update : Open AT® Software Suite v2 Consumption modifications: (see chapter 3.22) Modification in analog audio interface (see chapter 3.11). Update of Temperature Class B (-30 °C + 85°C) (see chapter 4.3) New chapter for correspondences of labelling between Q2686 with Open AT® Software Suite v2 (see chapter 4.2) ADC modifications: (see chapter 3.10) SPI modification: (see chapter 3.4) BUZZER modifications : (see chapter 3.12) LED0 : new designation : (see chapter 3.20 and 4.2) GPIO44:new designation: (see chapter 4.2) Reset signal: modification on input impedance (see chapter 3.16) Current start up definition (see chapter 3.2.2) Charger interface updated (see chapter 3.13) RTC interface : Maximum input voltage updated (see chapter 3.19.1)	
009	May 14, 2009	Update Storage temperature in section 4.3. Updates to contents of section 7.1.	
010	June 30, 2009	Updated to antenna gain information in section 7.1.	

Overview

This document defines and specifies the Q2686 Wireless CPU®, available in a GSM/GPRS Class 10 quad-band version:

- **Q2686H**: EGSM/GPRS **900/1800/850/1900** MHz version with **32** Mb of Bursted Flash memory and **8** Mb of SRAM (**32/8**).
- **Q2686G**: EGSM/GPRS **900/1800/850/1900** MHz version with **64** Mb of Bursted Flash memory and **16** Mb of SRAM (**64/16**).

The Q2686 Wireless CPU® supports a powerful open software platform (Open AT®). Open AT® is the world's most comprehensive cellular development environment, which allows embedded standard ANSI C applications to be natively executed directly on the Wireless CPU®.

This Product Technical Specification document covers the Wireless CPU® alone and does not include the programmable capabilities provided via the use of Open AT® Software Suites.

For detailed software programming guides, refer to the documents shown in the "WM_PRJ_Q2686_PTS_001" section.

Cautions

This platform contains a modular transmitter. This device is used for wireless applications. Note that all electronics parts and elements are ESD sensitive.

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Web Site Support

General information about Wavecom and its range of products:	www.wavecom.com
Specific support about the Q2686 Wireless CPU®:	www.wavecom.com/Q2686
Carrier/Operator approvals:	www.wavecom.com/approvals
Open AT® Introduction:	www.wavecom.com/OpenAT
Developer support for software and hardware:	www.wavecom.com/forum

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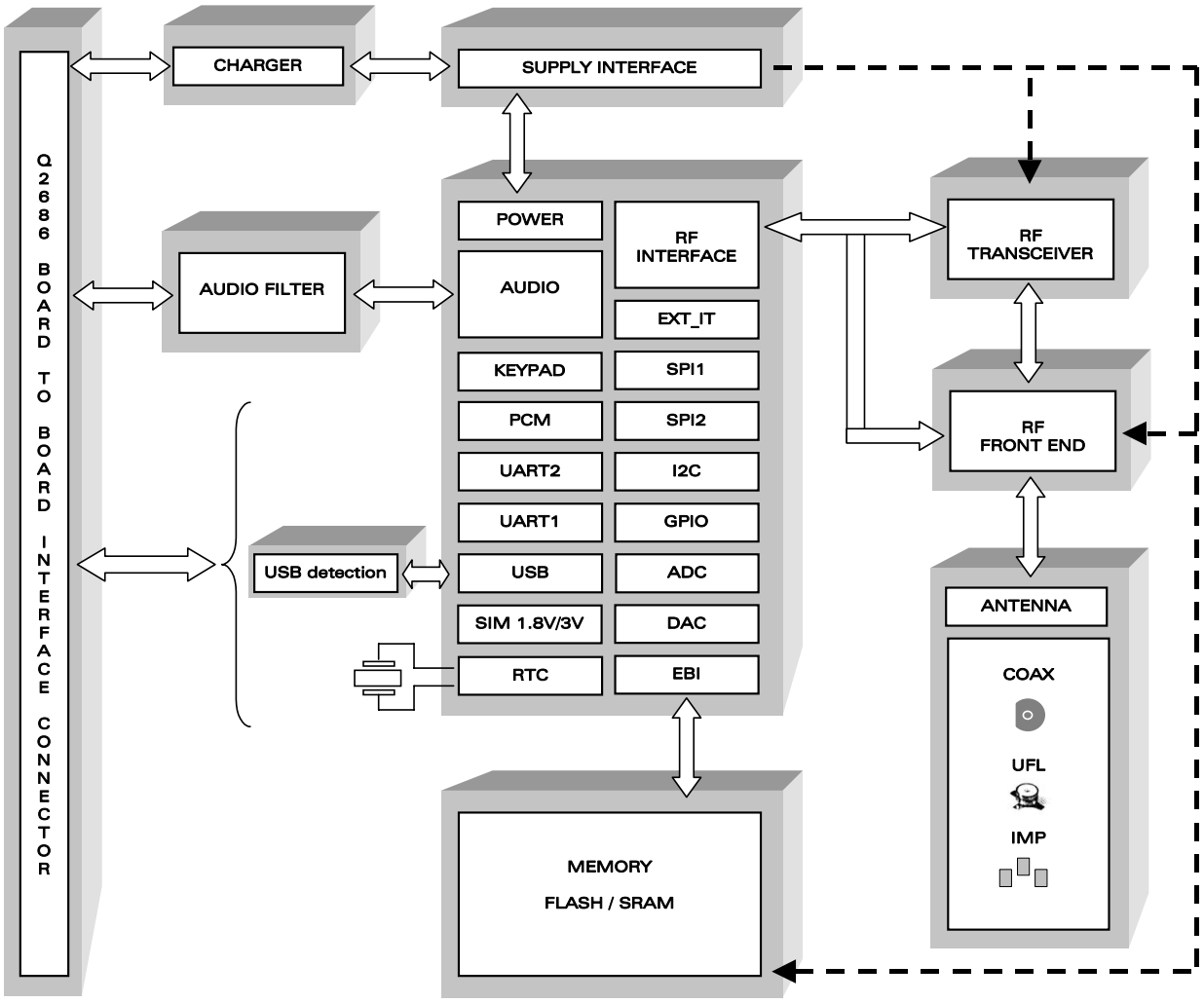


1 References

1.1 Reference Documents

For more details, several reference documents may be consulted. The Wavecom reference documents are provided in the Wavecom document package, contrary to the general reference documents which are not authored by Wavecom.

Please check the web site for the latest documentation available. Note that the last software version available for Q2686 is Open AT® Software Suite v2.0.

1.1.1 Open AT® Software Documentation

[1] Getting started with Open AT®
[2] Tutorial for Open AT®
[3] Tools Manual for Open AT®
[4] Basic Development Guide for Open AT®
[5] ADL User Guide for Open AT®
[6] Open AT® Release Note

1.1.2 AT Software Documentation

[7] AT commands interface Guide V7.1
[8] AT Commands Interface Guide (Bluetooth)
[9] Open AT® firmware Release Note

1.1.3 Hardware Documents

[10] Q2686 Wireless CPU® Customer Design Guidelines (Ref. WM_PRJ_Q2686_PTS_003)
[11] Q2686 Wireless CPU® Process Customer Guidelines (Ref.WM_PRJ_Q2686_PTS_004)

1.1.4 Other Wavecom Documents

[12] Automotive Environmental Control Plan for Q2686 Wireless CPU® (Ref. WM_T&D_Q2686_DCP_001)

1.1.5 General Reference Documents

[13] "I²C Bus Specification", Version 2.0, Philips Semiconductor 1998
[14] ISO 7816-3 Standard

1.2 List of Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate

Abbreviation	Definition
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory

Abbreviation	Definition
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio

2 General Description

2.1 General Information

The Q2686 series is a self-contained E-GSM/GPRS 900/1800 and 850/1900 quad-band Wireless CPU® with the following characteristics:

2.1.1 Overall Dimensions

- Length: 40 mm
- Width: 32.2 mm
- Thickness: 4 mm

2.1.2 Environment and Mechanics

- Green policy: RoHS compliant
- Complete shielding

The Q2686 Wireless CPU® is compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)".

The Wireless CPU®s which are compliant with this directive are identified by the RoHs logo on their label.

2.1.3 GSM/GPRS Features

- 2-Watt EGSM 900/GSM 850 radio section running under 3.6 volts
- 1-Watt GSM1800/1900 radio section running under 3.6 volts
- Hardware GPRS class 10 capable

2.1.4 Interfaces

- Digital section running under 2.8 volts and 1.8V.
- 3V/1V8 SIM interface
- Complete interfacing:
  - Power supply
  - Serial link
  - Analog audio
  - PCM digital audio
  - SIM card
  - Keyboard
  - USB 2.0 slave
  - Serial LCD (not available with AT commands)

2.1.5 Operating System

- Real Time Clock (RTC) with calendar
- Battery charger
- Echo cancellation + noise reduction (quadri codec)
- Full GSM or GSM/GPRS Operating System stack

2.1.6 Connection Interfaces

The Q2686 Wireless CPU® has four external connections:

- Three for RF circuit:
  - UFL connector
  - Soldered connection
  - IMP connection
- One for baseband signals:
  - 100 pin I/O connector.

2.2 Functional Architecture

The global architecture of the Q2686 Wireless CPU® is displayed below:

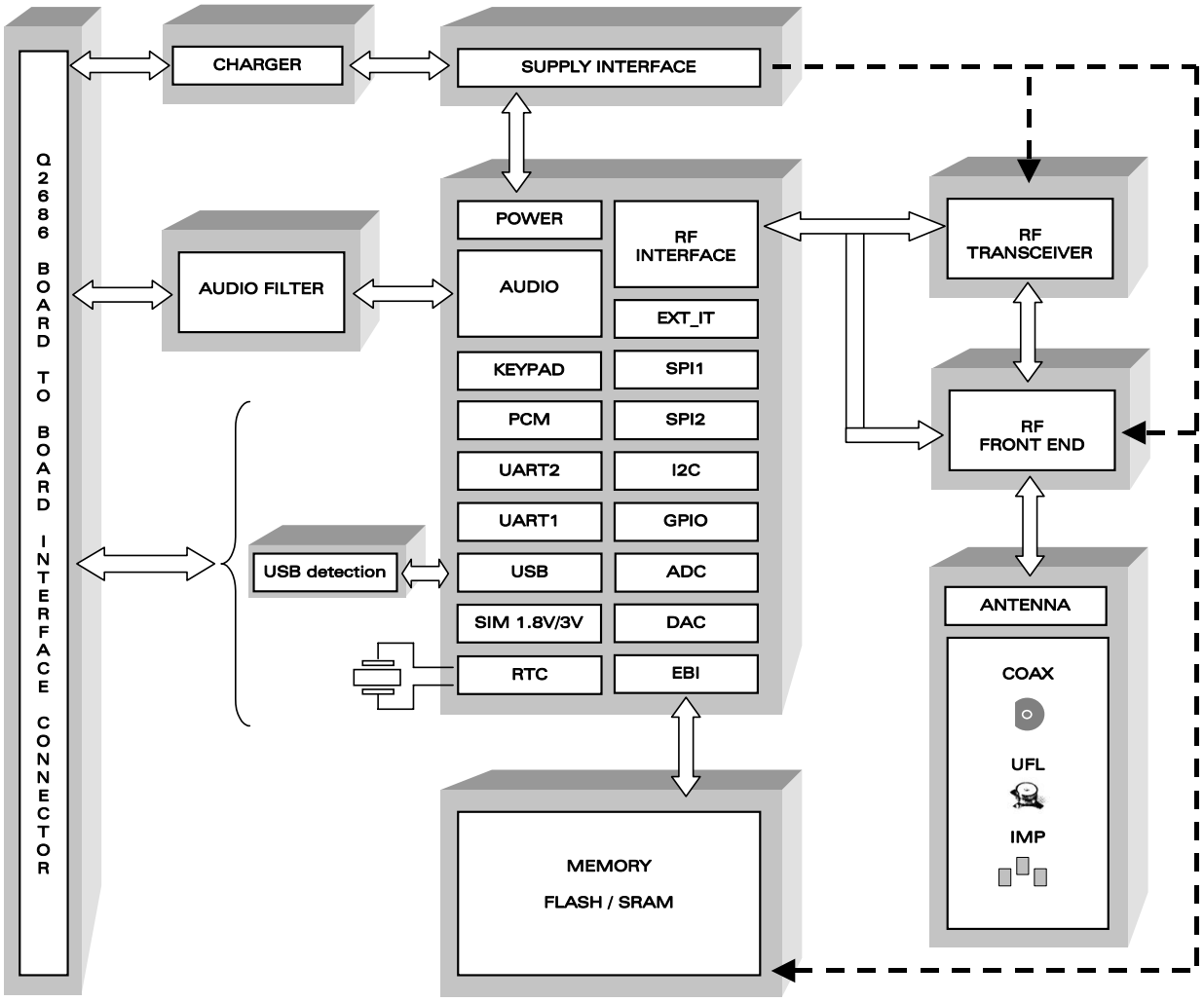


Figure 1: Functional architecture

2.2.1 RF Functionalities

The Radio Frequency (RF) range complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendations. The frequencies are:

	Transmit band (Tx)	Receive band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PCS 1900	1850 to 1910 MHz	1930 to 1990 MHz

The Radio Frequency (RF) part is based on a specific quad-band chip with a:

- Digital low-IF receiver
- Quad-band LNA (Low Noise Amplifier)
- Offset PLL (Phase Locked Loop) transmitter
- Frequency synthesizer
- Digitally controlled crystal oscillator (DCXO)
- Tx/Rx FEM (Front-End Wireless CPU®) for quad-band GSM/GPRS

2.2.2 Baseband Functionalities

The digital part of the Q2686 Wireless CPU® is composed of a PCF5212 PHILIPS chip. This chipset uses a 0.18 µm CMOS mixed technology, which allows massive integration as well as low current consumption.

2.3 Operating System

The Q2686 Wireless CPU® is designed to integrate various types of specific process applications such as vertical applications (telemetry, multimedia, automotive).

The Operating System offers a set of AT commands to control the Wireless CPU®. With this standard Operating System, some interfaces of the Wireless CPU® are not available because they are dependent on the peripheral devices connected to the Wireless CPU®.

The Operating System is Open AT® compliant.

3 Interfaces

3.1 General Purpose Connector (GPC)

A 100-pin connector is provided to interface the Q2686 Wireless CPU® with a board containing either a serial LCD Wireless CPU®, a keyboard, a SIM connector, or a battery connection.

The available interfaces on the GPC are described below:

Chapter	Name	Driven by AT commands	Driven by Open AT®
3.4	Serial Interface		X
3.5	Keyboard Interface	X	X
3.6	Main Serial Link	X	X
3.7	Auxiliary Serial Link	X	X
3.8	SIM Interface	X	X
3.9	General Purpose IO	X	X
3.10	Analog to Digital Converter	X	X
3.11	Analog Audio Interface	X	X
3.12	Buzzer Output	X	X
3.13	Battery Charging Interface	X	X
3.17	External Interruption	X	X
3.18	VCC_2V8 and VCC_1V8		
3.19	BAT-RTC (Backup Battery)		
3.20	LED0 signal	X	X
3.21	Digital Audio Interface (PCM)		X
3.22	USB 2.0 Interface	X	X

3.2 Power Supply

3.2.1 Power Supply Description

The power supply is one of the key issues in the design of a GSM terminal.

Due to the burst emission mode used in GSM/GPRS, the power supply must be able to deliver high current peaks in a short time. During the peaks, the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit (see Table 1 Power supply voltage).

- In communication mode, a GSM/GPRS class 2 terminal emits 577µs radio bursts every 4.615ms (see Figure 2).

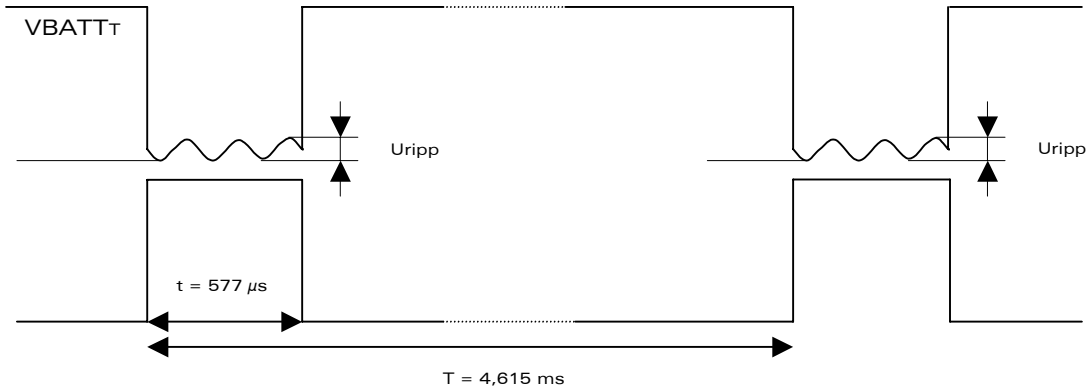


Figure 2: Power supply during burst emission

- In communication mode, a GPRS class 10 terminal emits 1154µs radio bursts every 4.615ms.

Only the VBATT input is necessary to supply the Q2686 Wireless CPU®.

VBATT:

- Directly supplies the RF components with 3.6 V. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error.

  The RF Power Amplifier current (**1.5 A** peak in GSM /GPRS mode) flows with a ratio of:

  - 1/8 of the time (around 577µs every 4.615ms for GSM /GPRS cl. 2) and
  - 2/8 of the time (around 1154µs every 4.615ms for GSM /GPRS cl. 10).

  The rising time is around 10µs.

- Is internally used to provide, via several regulators, the VCC_2V8 and VCC_1V8 power supply required for the baseband signals.

The Q2686 Wireless CPU® shielding case is the grounding. The ground must be connected to the motherboard through a complete layer on the PCB.

	V_{MIN}	V_{NOM}	V_{MAX}
VBATT[1,2]	3.2	3.6	4.8

Table 1 Power supply voltage

(1): This value must be guarantied during the burst (with **1.5A** Peak in GSM or GPRS mode)
(2): Max operating Voltage Stationary Wave Ratio (VSWR) 2:1

When the Wireless CPU® is supplied with a battery, the total impedance (battery + protections + PCB) should be < 150 mΩ.

As the radio power amplifier is directly connected to VBATT, the Wireless CPU® is sensitive to any Alternative Current on lines. When a DC/DC converter is used, Wavecom recommends setting the converter frequency in such a way that the resulting voltage does not exceed the values in following table.

Freq. (kHz)	U_{ripp} Max (mVpp)
<10	300
10 ≤ f ≤ 200	40
> 200	10

Table 2 Maximum voltage ripple (Uripp) vs Frequency

When the Wireless CPU® is in Alarm/Off mode, no voltage has to be applied on any pin of the 100-pin connector, except on Vbatt (pins 1 to 4) ,BAT-RTC (pin 7) for RTC operation or ON/~OFF (pin 19) to power-ON the Wireless CPU®.

3.2.2 Power Consumption

Power consumption is dependent on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used (AT or Open AT®).

All the following information is given assuming a 50 Ω RF output.

The following consumption values were obtained by performing measurements on the Wireless CPU® samples at a temperature of 25° C.

Three VBATT values are used to measure the consumption, $VBATT_{MIN}$ (3.2V), $VBATT_{MAX}$ (4.8V) and $VBATT_{TYP}$ (3.6V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

For a more detailed description of the operating modes, see the appendix of the AT Command User Guide [7].

For more information on the consumption measurement procedure, see Q2686 Wireless CPU® Customer Design Guidelines [10].

First let's define start-up current in view to avoid start issues.

3.2.2.1 Start-up Current

The start-up current is defined as follow:

During the first second following the Power on, a peak of current appears : This peak of current is called "$I_{startup}$ current " and has a duration of about 161 ms (Typical) .

Figure 3 shows the waveform of current and localizes the peak considered as the start-up current.

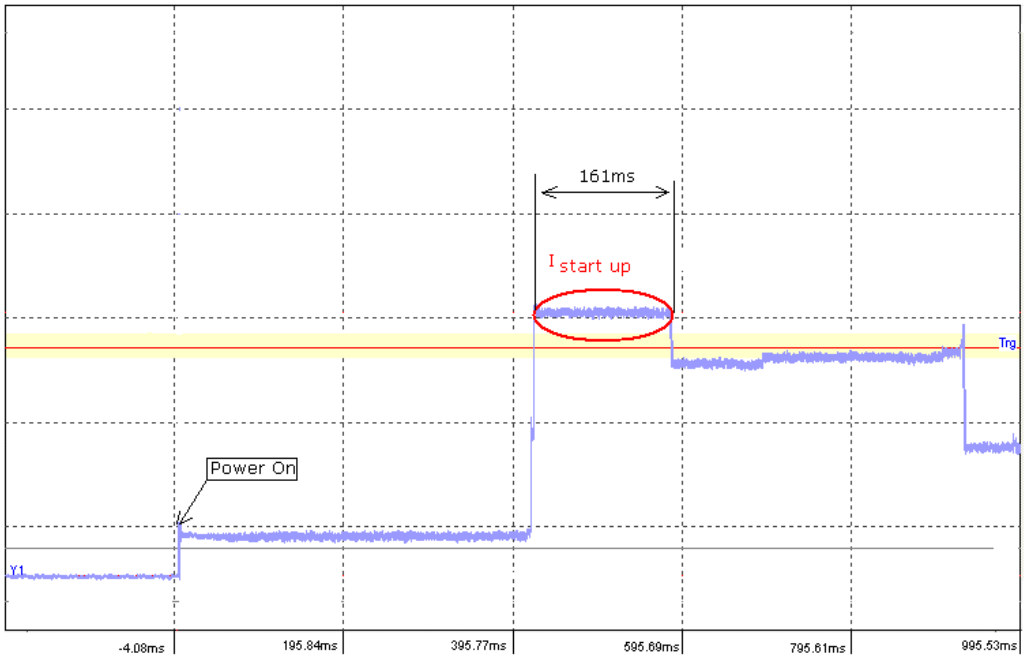


Figure 3: Start-up current waveform

In this condition, we can consider the following results:

25°C	3.2 V	3.6 V	4.8 V
$I_{Start-up}$	88 mA	80 mA	64 mA

3.2.2.2 Power Consumption without Open AT® Processing

The following measurement results are relevant when:

- there is no Open AT® application
- Open AT® application is disabled
- no processing is required by the Open AT® application

Power consumption without Open AT® processing							
Operating mode	**Parameters**		**I_{NOM} average VBATT=4,8V**	**I_{NOM} average VBATT=3,6V**	**I_{NOM} average VBATT=3,2V**	**I_{MAX} peak**	**unit**
Alarm Mode			21	16	15		µA
Fast Idle Mode	Paging 9 (Rx burst occurrence ~2s)		32.6	39.7	43.2	154 $_{RX}$	mA
	Paging 2 (Rx burst occurrence ~0,5s)		33.6	40.7	44.2	156 $_{RX}$	mA
Slow Idle Mode [1]	Paging 9 (Rx burst occurrence ~2s)		1.9	2.1	2.3	155 $_{RX}$	mA
	Paging 2 (Rx burst occurrence ~0,5s)		5	5.7	6	158 $_{RX}$	mA
Fast Standby Mode			33.5	40.8	44.1	51	mA
Slow Standby Mode			0.37	0.38	0.43	49.9	mA
Connected Mode	850/900 MHz	PCL5 (TX power 33dBm)	209	217	222	1462 $_{TX}$	mA
		PCL19 (TX power 5dBm)	85.6	93.8	98	257 $_{TX}$	mA
	1800/1900 MHz	PCL0 (TX power 30dBm)	153	162	166	894 $_{TX}$	mA
		PCL15 (TX power 0dBm)	82	89	94	225 $_{TX}$	mA
Transfer Mode **class 8 (4Rx/1Tx)**	850/900 MHz	gam. 3(TX power 33dBm)	198.2	206.5	211.5	1428 TX	mA
		gam.17(TX power 5dBm)	80	88	91	226 $_{TX}$	mA
	1800/1900 MHz	gam.3(TX power 30dBm)	145	153	158	870$_{TX}$	mA
		gam.18(TX power 0dBm)	77	85	88	206 $_{TX}$	mA
Transfer Mode **class 10 (3Rx/2Tx)**	850/900 MHz	gam.3 (TX power 33dBm)	357	366.5	373	1426 $_{TX}$	mA
		gam.17 (TX power 5dBm)	114	123	125	248 $_{TX}$	mA
	1800/1900 MHz	gam.3 (TX power 30dBm)	248	257	263	878$_{TX}$	mA
		gam.18 (TX power 0dBm)	108	117	121	229 $_{TX}$	mA

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst)

$_{RX}$ means that the current peak is the RF reception burst (Rx burst)

[1] **Slow Idle Mode** consumption is dependent on the SIM card used. Some SIM cards respond faster than others, the longer the response time, the higher the consumption. The measurements were performed with a large number of 3V SIM cards, the results in brackets are the minimum and maximum currents measured from among all the SIMs used.

3.2.2.3 Power Consumption with Open AT® Software

The Open AT™ software used is the Full CPU Load application, the following consumption results are measured during the run of the Full CPU Load application.

The two tables are respectively for the CPU clock programmed at 26 MHz and 104 MHz.

Power consumption with Full CPU load Open AT® application CPU@26MHz								
Working mode		**Parameters**		**I_{NOM} average VBATT=4,8V**	**I_{NOM} average VBATT=3,6V**	**I_{NOM} average VBATT=3,2V**	**I_{MAX} peak**	**unit**
Alarm Mode				N/A*	N/A*	N/A*	N/A*	
Fast Idle Mode		Paging 9 (Rx burst occurrence ~2s)		32	38	43	194 $_{RX}$	mA
		Paging 2 (Rx burst occurrence ~0,5s)		33	39	44	196 $_{RX}$	mA
Slow Idle Mode		Paging 9 (Rx burst occurrence ~2s)		N/A*	N/A*	N/A*	N/A*	
		Paging 2 (Rx burst occurrence ~0,5s)		N/A*	N/A*	N/A*	N/A*	
Fast Standby Mode				33	38	44	50	mA
Slow Standby Mode				N/A*	N/A*	N/A*	N/A*	
Connected Mode		850/900 MHz	PCL5 (TX power 33dBm)	210	220	223	1390 $_{TX}$	mA
			PCL19 (TX power 5dBm)	86	92	95	270 $_{TX}$	mA
		1800/1900 MHz	PCL0 (TX power 30dBm)	154	162	167	888 $_{TX}$	mA
			PCL15 (TX power 0dBm)	80	88	92	241 $_{TX}$	mA
GPRS	**Transfer Mode class 8 (4Rx/1Tx)**	850/900 MHz	Gam.3 (TX power 33dBm)	199	207	212	1450 $_{TX}$	mA
			Gam.17 (TX power 5dBm)	80	88	92	249 $_{TX}$	mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	147	152	159	860 $_{TX}$	mA
			Gam.18 (TX power 0dBm)	77	85	89	221 $_{TX}$	mA
	Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz	Gam.3 (TX power 33dBm)	357	367	374	1462 $_{TX}$	mA
			Gam.17 (TX power 5dBm)	115	123	127	275 $_{TX}$	mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	252	260	266	870 $_{TX}$	mA
			Gam.18 (TX power 0dBm)	109	117	121	249 $_{TX}$	mA

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst)
$_{RX}$ means that the current peak is the RF reception burst (Rx burst)

* N/A: That doesn't mean that no Open AT® application is possible in this specific mode. That means that the specific Full CPU load Open AT® application can't allow this specific mode. (This is a worst case for the consumption measurement).

Power consumption with Full CPU load Open AT® application CPU@104MHz								
Working mode		**Parameters**		**I_{NOM} average VBATT=4,8V**	**I_{NOM} average VBATT=3,6V**	**I_{NOM} average VBATT=3,2V**	**I_{MAX} peak**	**unit**
Alarm Mode				N/A*	N/A*	N/A*	N/A*	
Fast Idle Mode		Paging 9 (Rx burst occurrence ~2s)		51	62	68	220 $_{RX}$	mA
		Paging 2 (Rx burst occurrence ~0,5s)		52	63	69	220 $_{RX}$	mA
Slow Idle Mode		Paging 9 (Rx burst occurrence ~2s)		N/A*	N/A*	N/A*	N/A*	
		Paging 2 (Rx burst occurrence ~0,5s)		N/A*	N/A*	N/A*	N/A*	
Fast Standby Mode				49	63	69	150	mA
Slow Standby Mode				N/A*	N/A*	N/A*	N/A*	
Connected Mode		850/900 MHz	PCL5 (TX power 33dBm)	210	220	230	1385 $_{TX}$	mA
			PCL19 (TX power 5dBm)	84	94	104	290 $_{TX}$	mA
		1800/1900 MHz	PCL0 (TX power 30dBm)	155	163	169	880 $_{TX}$	mA
			PCL15 (TX power 0dBm)	89	102	109	270 $_{TX}$	mA
GPRS	**Transfer Mode class 8 (4Rx/1Tx)**	850/900 MHz	Gam.3 (TX power 33dBm)	225	243	252	1509 $_{TX}$	mA
			Gam.17 (TX power 5dBm)	107	126	133	306 $_{TX}$	mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	175	190	198	912 $_{TX}$	mA
			Gam.18 (TX power 0dBm)	104	120	129	284 $_{TX}$	mA
	Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz	Gam.3 (TX power 33dBm)	385	403	414	1532 $_{TX}$	mA
			Gam.17 (TX power 5dBm)	142	159	167	385 $_{TX}$	mA
		1800/1900 MHz	Gam.3 (TX power 30dBm)	271	288	301	949 $_{TX}$	mA
			Gam.18 (TX power 0dBm)	136	153	161	341 $_{TX}$	mA

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst)
$_{RX}$ means that the current peak is the RF reception burst (Rx burst)
* N/A: That doesn't mean that no Open AT® application is possible in this specific mode. That means that the specific Full CPU load Open AT® application can't allow this specific mode. (This is a worst case for the consumption measurement).

3.2.2.4 Consumption Waveform Samples

The consumption waveforms are given for a EGSM900 network configuration with AT software running on the Q2686 Wireless CPU®/Open AT® Software Suite v2.

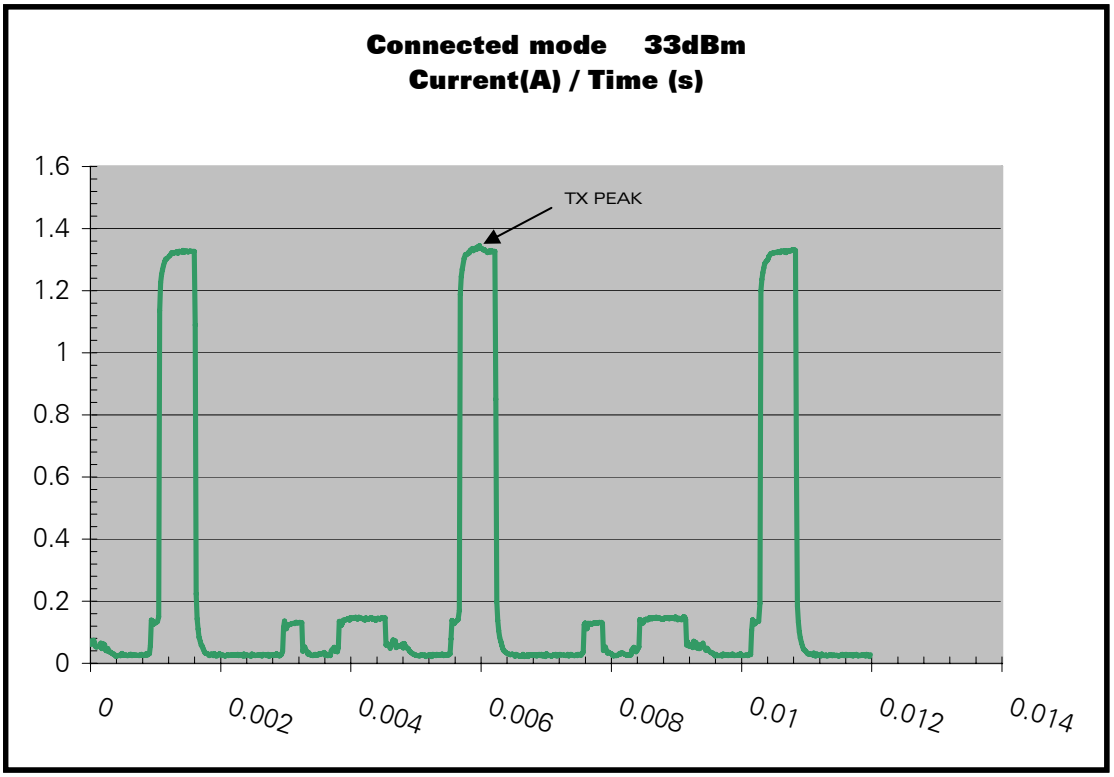
The VBATT voltage is at the typical value of 3.6V.

Four significant operating mode consumption waveforms are described:

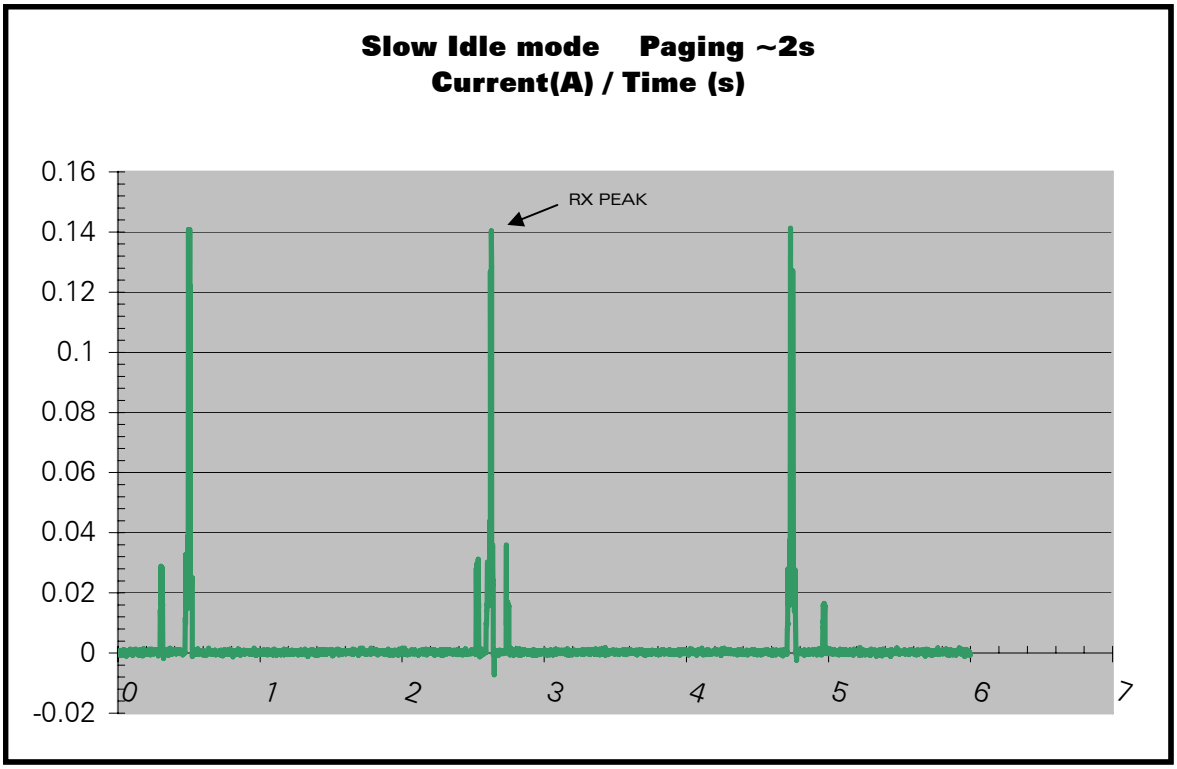
- Connected Mode (PCL5: Tx power 33dBm)
- Slow Idle mode (Paging 9)
- Fast idle mode (Paging 9)
- Transfer mode (GPRS class 10, PCL3: Tx power 33dBm)

The following waveform shows only the form of the current, for correct current values, see sections 3.2.2.2 and 3.2.2.3.

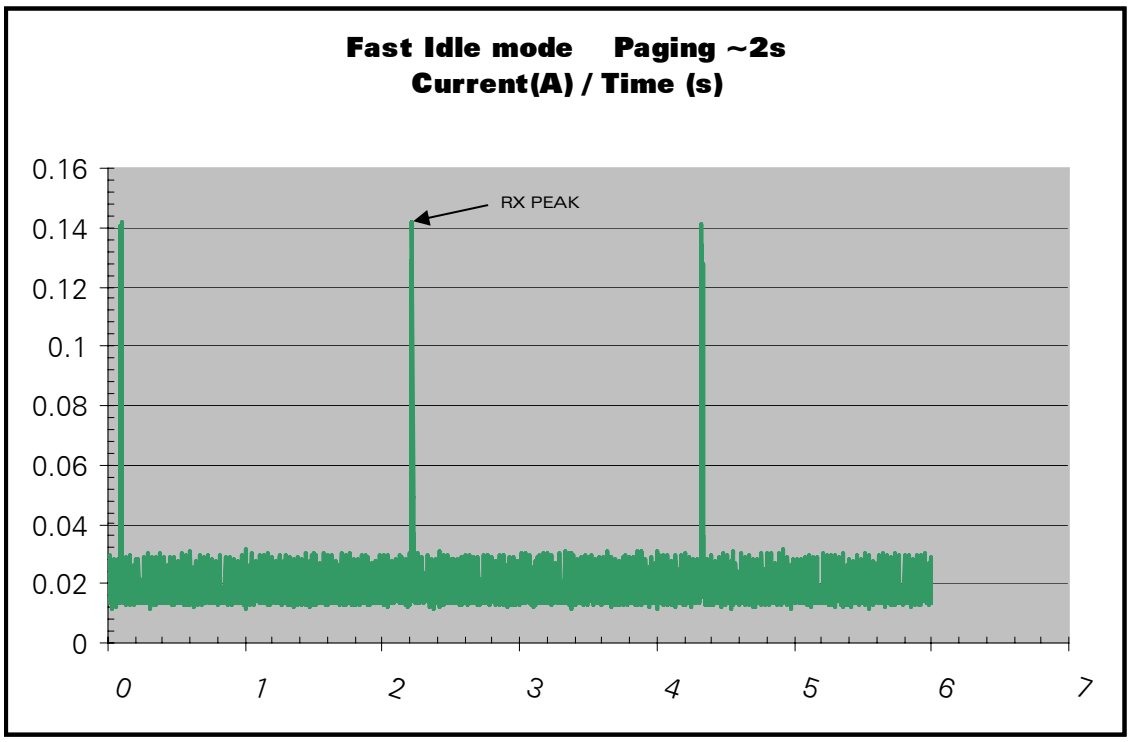
3.2.2.4.1 Connected Mode Current Waveform



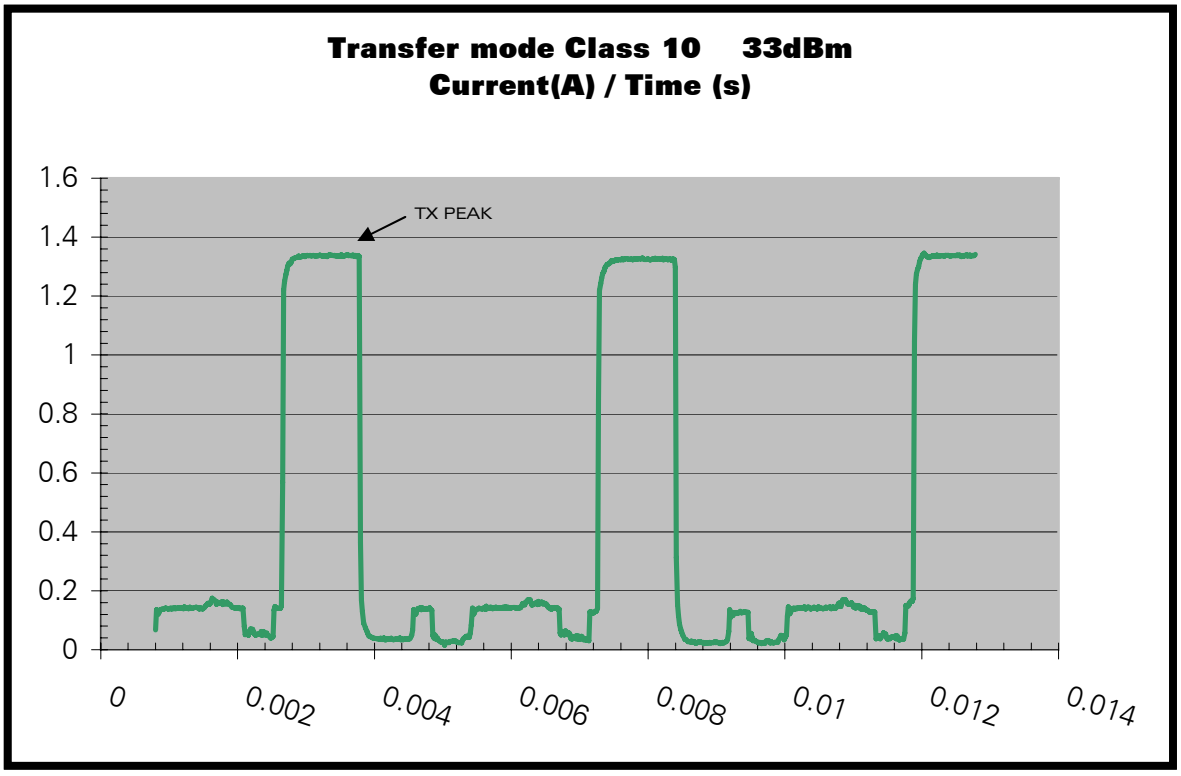
3.2.2.4.2 Slow Idle Mode Current Waveform



3.2.2.4.3 Fast Idle Mode Current Waveform



3.2.2.4.4 Transfer Mode Class 10 Current Waveform



3.2.2.5 Power Supply Pin-out

Power supply pin-out

Signal	Pin number
VBATT	1,2,3,4
GND	Shielding

The grounding connection is made through the shielding; the four leads must be soldered to the ground plane.

3.3 Electrical Information for Digital I/O

The three types of digital I/O on the Q2686 Wireless CPU® are: 2.8 volt CMOS, 1.8 volt CMOS and Open drain.

The three types are described below:

Electrical characteristics of digital I/O

2.8 volt type (2V8)						
Parameter		**I/O type**	**Minim.**	**Typ**	**Maxim.**	**Condition**
Internal 2.8V power supply		VCC_2V8	2.74V	2.8V	2.86V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.84V	
	V_{IH}	CMOS	1.96V		3.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	2.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

*Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltage above the maximum voltage specified above, **except for the UART1 interface, which is 3.3V tolerant**.

1.8 volt type (1V8)						
Parameter		**I/O type**	**Minim.**	**Typ**	**Maxim.**	**Condition**
Internal 1V8 power supply		VCC_1V8	1.76V	1.8V	1.94V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.54V	
	V_{IH}	CMOS	1.33V		2.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	1.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

*Absolute maximum ratings

Open drain output type						
Signal name	Parameter	I/O type	Minimum	Typ	Maximum	Condition
LED0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			8mA	
BUZZER0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			100mA	
SDA1 / GPIO27 and SCL1 / GPIO26	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2V			
	V_{IL}	Open Drain			0.8V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The reset states of the I/Os are given in each interface description chapter. Definitions of these states are given below:

Reset state definition	
Parameter	**Definition**
0	Set to GND
1	Set to supply 1V8 or 2V8 depending on I/O type
Pull-down	Internal pull-down with ~60kΩ resistor.
Pull-up	Internal pull-up with ~60kΩ resistor to supply 1V8 or 2V8 depending on I/O type.
Z	High impedance
Undefined	Caution: undefined must not be used in your application if a special state is required at reset. These pins may be a toggling signal during reset.

3.4 Serial interface

The Q2686 Wireless CPU® provide two SPI bus (i.e. for LCD, memories...). or an I²C 2-wire interface..

3.4.1 SPI Bus

Both SPI bus interfaces include:

- A CLK signal
- An I/O signal
- An I signal
- A CS (Chip Select) signal complying with the standard SPI bus (any GPIO).
- An optional Load signal (only the SPIx-LOAD signal)

3.4.1.1 Characteristics

- Master mode operation
- The CS signal must be any GPIO
- The LOAD signal (optional) is used for the word handling mode (only the SPIx-LOAD signal)
- SPI speed is from 102 kbit/s to 13 Mbit/s in master mode operation
- 3 or 4-wire interface(5-wire possible with the optional SPIx-LOAD signal)
- SPI-mode configuration: 0 to 3 (for more details, refer to document.
- 1 to 16 bits data length

3.4.1.2 SPI configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire type	4-wire type	5-wire type
Master	13 Mb/s	0,1,2,3	Half	SPIx-CLK; SPIx-IO; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS; SPIx-LOAD (not muxed in GPIO);

For the 3-wire configuration, SPIx-I/O is used as input and output.

For the 4-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only.

For the 5-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only. And the dedicated SPIx-LOAD signal is used. It is an additional signal in more than a Chip Select (any other GPIOx)

3.4.1.3 SPI waveforms

Waveform for SPI transfer with 4-wire configuration in master mode 0 .

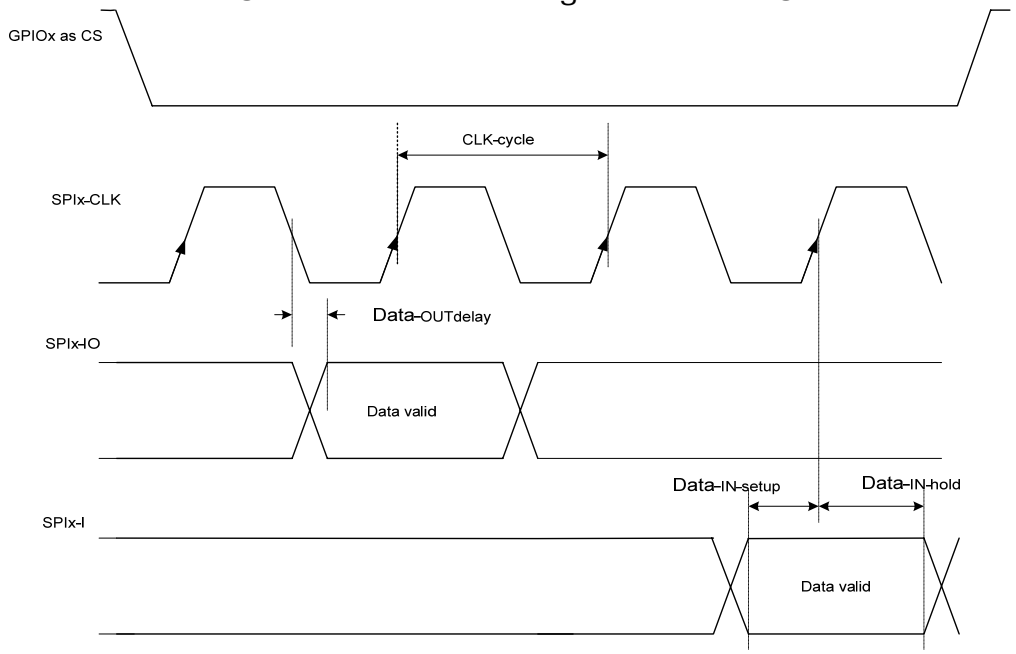


Figure 4: SPI Timing diagrams,Mode 0,Master,4 wires

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
CLK-cycle	SPI clock frequency	0.102		13	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

Waveform for SPI transfer with the LOAD signal configuration in master mode 0.(chip select is not represented)

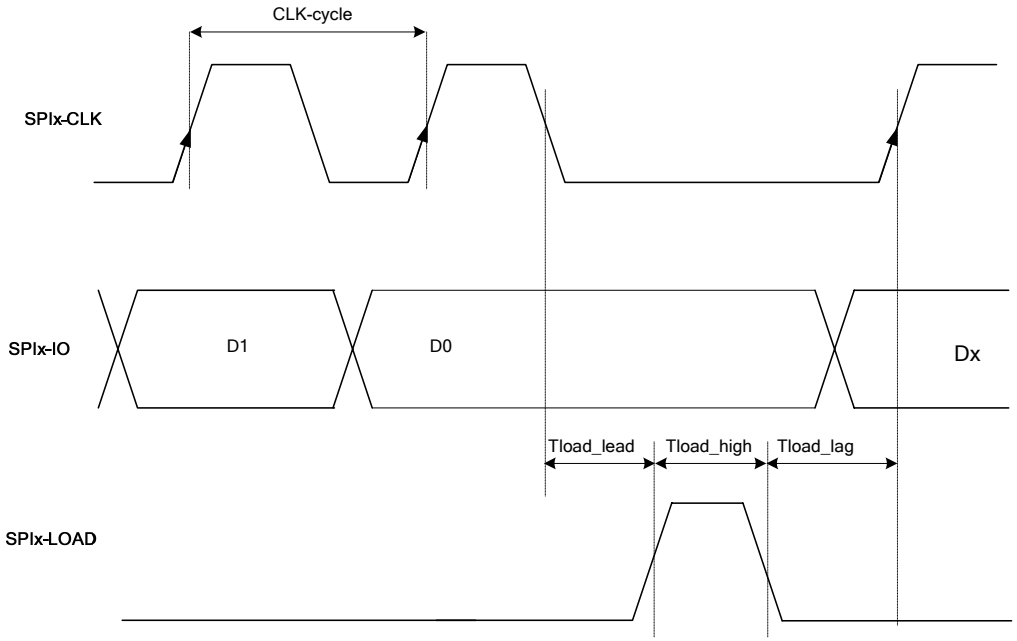


Figure 5: SPI Timing diagrams with LOAD signal, Mode 0, Master, 4 wires

3.4.1.4 SPI1 Bus: Pins description

Pins description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI1-CLK	23	O	2V8	Z	SPI Serial Clock	GPIO28
SPI1-IO	25	I/O	2V8	Z	SPI Serial input/output	GPIO29
SPI1-I	24	I	2V8	Z	SPI Serial input	GPIO30
SPI1-LOAD	22	O	2V8	Z	SPI load	GPIO31

For Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition, refer to Chapter 3.3, "Electrical information for digital I/O".

3.4.1.5 SPI2 Bus: Pins description

Pins description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI2-CLK	26	O	2V8	Z	SPI Serial Clock	GPIO32
SPI2-IO	27	I/O	2V8	Z	SPI Serial input/output	GPIO33
SP2-I	29	I	2V8	Z	SPI Serial input	GPIO34
SPI2-LOAD	28	O	2V8	Z	SPI Load	GPIO35

See Chapter 3.3 “Electrical information for digital I/O” for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.4.2 I2C Bus

The I2C interface includes a clock signal (**SCL1**) and data signal (**SDA1**) complying with a 100kbit/s-standard interface (standard mode: s-mode).

The I²C bus is always master.

The maximum speed transfer range is 400kbit/s (fast mode: f-mode).

For more information on the bus, see the "I²C Bus Specification Version 2.0" from PHILIPS [13].

3.4.2.1 I²C Waveforms

I²C bus waveform in master mode configuration:

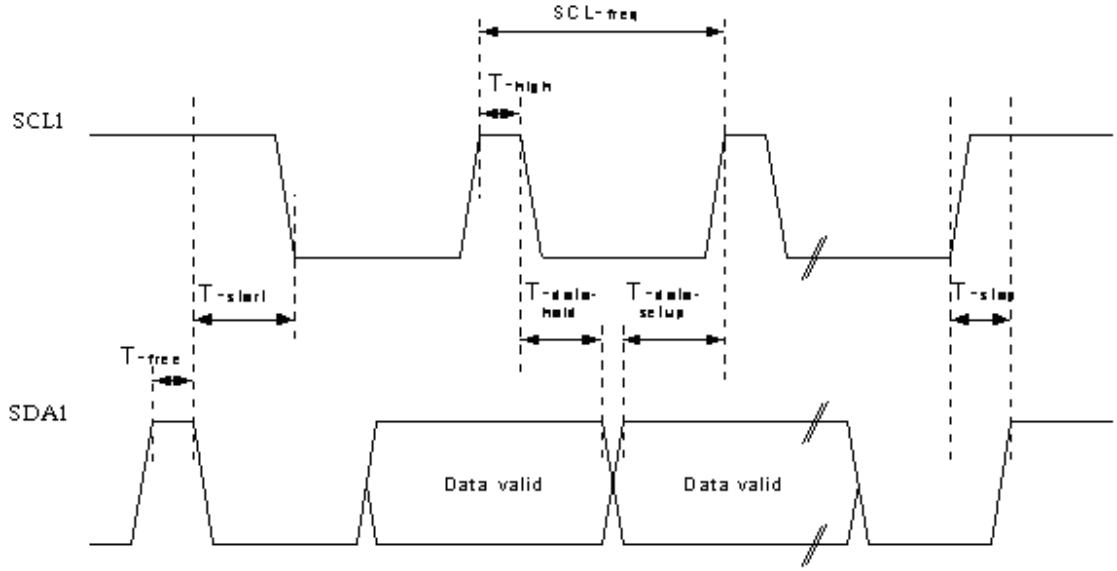


Figure 6: I²C Timing diagrams, Master

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
SCL1-freq	I²C clock frequency	100		400	kHz
T-start	Hold time START condition	0.6			µs
T-stop	Setup time STOP condition	0.6			µs
T-free	Bus free time, STOP to START	1.3			µs
T-high	High period for clock	0.6			µs
T-data-hold	Data hold time	0		0.9	µs
T-data-setup	Data setup time	100			ns

3.4.2.2 I²C Bus Pin-out

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SCL1	44	O	Open drain	Z	Serial Clock	GPIO26
SDA1	46	I/O	Open drain	Z	Serial Data	GPIO27

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.5 Keyboard Interface

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4) and
- 5 columns (COL0 to COL4).

The scanning is a digital one and debouncing is performed in the Q2686 Wireless CPU®.

No discrete components such as Rs, Cs (Resistors, Capacitors) are needed.

Keyboard interface pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
ROW0	68	I/O	1V8	0	Row scan	GPIO9
ROW1	67	I/O	1V8	0	Row scan	GPIO10
ROW2	66	I/O	1V8	0	Row scan	GPIO11
ROW3	65	I/O	1V8	0	Row scan	GPIO12
ROW4	64	I/O	1V8	0	Row scan	GPIO13
COL0	59	I/O	1V8	Pull-up	Column scan	GPIO4
COL1	60	I/O	1V8	Pull-up	Column scan	GPIO5
COL2	61	I/O	1V8	Pull-up	Column scan	GPIO6
COL3	62	I/O	1V8	Pull-up	Column scan	GPIO7
COL4	63	I/O	1V8	Pull-up	Column scan	GPIO8

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

With the Open AT® Software Suite v2 when the keyboard service is used the whole multiplexed signals become unavailable for other purposes. In the same way if one or more GPIOs (of this table) are allocated the keyboard service is unavailable.

3.6 Main Serial Link (UART1)

A flexible 8-wire serial interface is available, complying with V24 protocol signalling, but not with V28 (electrical interface) due to a 2.8 volts interface.

The signals are:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (~CT105/RTS)
- Clear To Send (~CT106/CTS)
- Data Terminal Ready (~CT108-2/DTR)
- Data Set Ready (~CT107/DSR).
- Data Carrier Detect (~CT109/DCD)
- Ring Indicator (CT125/RI).

UART1 interface pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
CT103/TXD1*	71	I	2V8	Z	Transmit serial data	GPIO36
CT104/RXD1*	73	O	2V8	1	Receive serial data	GPIO37
~CT105/RTS1*	72	I	2V8	Z	Request To Send	GPIO38
~CT106/CTS1*	75	O	2V8	Z	Clear To Send	GPIO39
~CT107/DSR1*	74	O	2V8	Z	Data Set Ready	GPIO40
~CT108-2/DTR1*	76	I	2V8	Z	Data Terminal Ready	GPIO41
~CT109/DCD1 *	70	O	2V8	Undefined	Data Carrier Detect	GPIO43
~CT125/RI1 *	69	O	2V8	Undefined	Ring Indicator	GPIO42
CT102/GND*	Shielding leads		GND		Ground	

See Chapter "3.3 Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

*According to PC view

With the Open AT® Software Suite v2, when the UART1 service is used, the whole multiplexed signals become unavailable for other purposes. In the same way if one or more GPIOs (of this table) are allocated the UART1 service is unavailable.

The **rise** and **fall time** of the reception signals (mainly CT103) must be less than **300 ns.**

The maximum baud rate of UART1 is **921** kbit/s for the firmware provided in the Open AT® Software Suite v2.

Recommendation:

The Q2686 Wireless CPU® is designed to operate using all the serial interface signals. In particular, it is recommended to use RTS and CTS for hardware flow control in order to avoid data loss during transmission.

For use with 5-wire serial interface

- Signal: CT103/TXD1*, CT104/RXD1*, ~CT105/RTS1*, ~CT106/CTS1*
- The signal ~CT108-2/DTR1* must be managed by following the V24 protocol signalling, if you want to use the slow idle mode.
- Other signals and their multiplexes are not available.
- Please refer to technical appendixes of AT commands User Guide [7] for more information.

For use with 4-wire serial interface

- CT103/TXD1*, CT104/RXD1*, ~CT105/RTS1*, ~CT106/CTS1*
- The signal ~CT108-2/DTR1* must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to technical appendixes in the AT commands User Guide [7] for more information.

For use with 2-wire serial interface

- This case is possible for connected external chip, but not recommended (and forbidden for AT command or modem use)
- The flow control mechanism has to be managed at the customer side.
- CT103/TXD1*, CT104/RXD1*
- The signal ~CT108-2/DTR1* must be configured at low level.
- The signals ~CT105/RTS1*, ~CT106/CTS1* are not used, please configure the AT command (AT+IFC=0,0 see AT command User Guide [7]).
- The signal ~CT105/RTS1* must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to technical appendixes in the AT commands User Guide [7] for more information.

3.7 Auxiliary Serial Link (UART2)

An auxiliary serial interface (UART2) is available on Q2686. This interface may be used to connect a Bluetooth or a GPS chip controlled by an Open AT® Plug-in.

UART2 interface pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
CT103 / TXD2*	31	I	1V8	Z	Transmit serial data	GPIO14
CT104 / RXD2*	30	O	1V8	Z	Receive serial data	GPIO15
~CT106 / CTS2*	32	O	1V8	Z	Clear To Send	GPIO16
~CT105 / RTS2*	33	I	1V8	Z	Request To Send	GPIO17

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

* According to PC view

The Q2686 is designed to operate using all the serial interface signals. In particular, it is recommended to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

The maximum baud rate of UART2 is **921** kbit/s for the firmware provided with Open AT® Software Suite v2.

For use with 4-wire serial interface

- CT103/TXD2*, CT104/RXD2*, ~CT105/RTS2*, ~CT106/CTS2*
- The signal ~CT108-2/DTR2* must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to technical appendixes in the AT commands User Guide [7] for more information.

For use with 2-wire serial interface

- This case is possible for connected external chip, but not recommended (and forbidden for AT command or modem use)
- The flow control mechanism has to be managed at the customer side.
- CT103/TXD2*, CT104/RXD2*
- The signals ~CT105/RTS2*, ~CT106/CTS2* are not used, you must configure the AT command (AT+IFC=0,0 see AT commands User Guide [7]).

- The signal ~CT105/RTS2* must be configured at low level.
- Other signals and their multiplexes are not available.
- Please refer to technical appendixes in the AT commands User Guide [7] for more information.

3.8 SIM Interface

The Subscriber Identification Module (SIM) may be directly connected to the Q2686 Wireless CPU® via this dedicated interface.

3.8.1 General Description

The five signals are:

- SIM-VCC: SIM power supply
- ~SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port
- SIMPRES: SIM card detect

The SIM interface controls a 3V/1V8 SIM. This interface is fully compliant with the GSM 11.11 recommendations concerning SIM functions.

SIM interface pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SIM-CLK	14	O	2V9 / 1V8	0	SIM Clock	Not mux
~SIM-RST	13	O	2V9 / 1V8	0	SIM Reset	Not mux
SIM-IO	11	I/O	2V9 / 1V8	*Pull-up	SIM Data	Not mux
SIM-VCC	9	O	2V9 / 1V8		SIM Power Supply	Not mux
SIMPRES	12	I	1V8	Z	SIM Card Detect	GPIO18

*SIM-IO pull-up is about 10 k Ω.

See Chapter 3.3 "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

SIM interface electrical characteristics

Parameter	Conditions	Minim.	Typ	Maxim.	Unit
SIM-IO V_{IH}	I_{IH} = ± 20µA	0.7xSIMVCC			V
SIM-IO V_{IL}	I_{IL} = 1mA			0.4	V
~SIM-RST, SIM-CLK V_{OH}	Source current = 20µA	0.9xSIMVCC			V
SIM-IO V_{OH}	Source current = 20µA	0.8xSIMVCC			
~SIM-RST, SIM-IO, SIM-CLK V_{OL}	Sink current = -200µA			0.4	V
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.6V			10	mA
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	µs
SIM-CLK Frequency	Loaded with 30pF			3.25	MHz

Note:

When **SIMPRES** is used, a **low to high** transition means that the SIM card is inserted and a **high to low** transition means that the SIM card is removed.

3.9 General Purpose Input/Output

The Q2686 Wireless CPU® provides up to 44 General Purpose I/Os, used to control any external device such as an LCD or a Keyboard backlight.

All I/Os highlighted in grey are 1V8, whereas the others (not highlighted in grey) are 2V8.

GPIO pin description

Signal	Pin number	I/O	I/O type*	Reset state	Multiplexed with
Reserved	42		Do not used*		
GPIO0	43	I/O	2V8	Undefined	32kHz**
GPIO1	51	I/O	1V8	0	Not mux
GPIO2	53	I/O	1V8	0	Not mux
GPIO3	50	I/O	1V8	Z	INT0
GPIO4	59	I/O	1V8	Pull-up	COL0
GPIO5	60	I/O	1V8	Pull-up	COL1
GPIO6	61	I/O	1V8	Pull-up	COL2
GPIO7	62	I/O	1V8	Pull-up	COL3
GPIO8	63	I/O	1V8	Pull-up	COL4
GPIO9	68	I/O	1V8	0	ROW0
GPIO10	67	I/O	1V8	0	ROW1
GPIO11	66	I/O	1V8	0	ROW2
GPIO12	65	I/O	1V8	0	ROW3
GPIO13	64	I/O	1V8	0	ROW4
GPIO14	31	I/O	1V8	Z	CT103 / TXD2
GPIO15	30	I/O	1V8	Z	CT104 / RXD2
GPIO16	32	I/O	1V8	Z	~CT106 / CTS2
GPIO17	33	I/O	1V8	Z	~CT105 / RTS2
GPIO18	12	I/O	1V8	Z	SIMPRES
GPIO19	45	I/O	2V8	Z	Not mux
GPIO20	48	I/O	2V8	Undefined	Not mux
GPIO21	47	I/O	2V8	Undefined	Not mux
GPIO22	57	I/O	2V8	Z	Not mux*
GPIO23	55	I/O	2V8	Z	Not mux

Signal	Pin number	I/O	I/O type*	Reset state	Multiplexed with
GPIO24	58	I/O	2V8	Z	Not mux
GPIO25	49	I/O	2V8	Z	INT1
GPIO26	44	I/O	Open drain	Z	SCL1
GPIO27	46	I/O	Open drain	Z	SDA1
GPIO28	23	I/O	2V8	Z	SPI1-CLK
GPIO29	25	I/O	2V8	Z	SPI1-IO
GPIO30	24	I/O	2V8	Z	SP1-I
GPIO31	22	I/O	2V8	Z	
GPIO32	26	I/O	2V8	Z	SPI2-CLK
GPIO33	27	I/O	2V8	Z	SPI2-IO
GPIO34	29	I/O	2V8	Z	SP2-I
GPIO35	28	I/O	2V8	Z	
GPIO36	71	I/O	2V8	Z	CT103 / TXD1
GPIO37	73	I/O	2V8	1	CT104 / RXD1
GPIO38	72	I/O	2V8	Z	~CT105 / RTS1
GPIO39	75	I/O	2V8	Z	~CT106 / CTS1
GPIO40	74	I/O	2V8	Z	~CT107 / DSR1
GPIO41	76	I/O	2V8	Z	~CT108-2 / DTR1
GPIO42	69	I/O	2V8	Undefined	~CT125 / RI1
GPIO43	70	I/O	2V8	Undefined	~CT109 / DCD1

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

* If a Bluetooth module is used with the Q2686 Wireless CPU®, these GPIOs must be reserved.

** With the Open AT® Software Suite v2: see "AT commands User Guide " [7].

3.10 Analog to Digital Converter

Two **A**nalog to **D**igital **C**onverter inputs are provided by the Q2686 Wireless CPU®. The converters are more than 10-bit resolution, ranging from 0 to 2V.

ADC1 / BAT-TEMP input can be used, typically, to monitor external temperature, useful for safety power off in case of application over heating (for Li-Ion battery).

ADC2 input can be used for customer application.

ADC pin description

Signal	Pin number	I/O	I/O type	Description
ADC1/BAT-TEMP*	20	I	Analog	A/D converter
ADC2	21	I	Analog	A/D converter

* This input can be used for a battery charging temperature sensor, see Chapter 3.13, “Battery Charging interface”.

ADC electrical characteristics

Parameter		Min	Typ	Max	Unit
Maximum output code			1635		LSB
Sampling period		0,5		3[1]	s
Input signal range		0		2	V
Input impedance	ADC1/BAT-TEMP		1M		Ω
	ADC2		1M		Ω

[1] Sampling rate only for ADC2 and Open AT® application.

3.11 Analog Audio Interface

Two different microphone inputs and two different speaker outputs are supported. The Q2686 INSIM Wireless CPU® also includes an echo cancellation feature, which allows hands-free function

In some cases, ESD protection must be added on the audio interface lines.

3.11.1 Microphone Features

The connection can be either differential or single-ended but using a differential connection in order to reject common mode noise and TDMA noise is strongly recommended. When using a single-ended connection, be sure to have a very good ground plane, a very good filtering as well as shielding in order to avoid any disturbance on the audio path.

The gain of MIC inputs is internally adjusted and can be tuned using an AT command.

Both can be configured in differential or single ended.

The MIC2 inputs already include the biasing for an electret microphone allowing an easy connection.

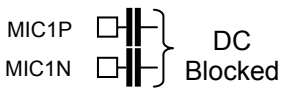
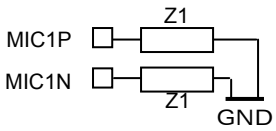
3.11.1.1 MIC1 Microphone Inputs

By default, the MIC1 inputs are single-ended but it can be configured in differential.

The MIC1 inputs do not include an internal bias . The MIC1 input needs to have an external biasing if an electret microphone is used.

AC coupling is already embedded in the Wireless Microprocessor®.

Equivalent circuits of MIC1

DC equivalent circuit	AC equivalent circuit
	

Electrical Characteristics of MIC1

Parameters		Min	Typ	Max	Unit
DC Characteristics			N/A		V
AC Characteristics 200 Hz<F<4 kHz	Z1	70	120	160	kΩ
Working voltage (MIC1P-MIC1N)	AT+VGT*=3500(4)		13.8	18.6***	mVrms
	AT+VGT*=2000(4)		77.5	104***	mVrms
	AT+VGT*=700(4)		346	465***	mVrms
Maximum rating voltage (MIC1P or MIC1N)	Positive			+7.35	V
	Negative	-0.9			

- *The input voltage depends of the input micro gain set by AT command. Please refer to the document :AT command User Guide [7]
- **Because MIC2P is internally biased, it is necessary to use a coupling capacitor to connect an audio signal provided by an active generator. Only a passive microphone can be directly connected to the MIC2P and MIC2N inputs.
- *** This value is obtained with digital gain = 0 and for frequency = 1kHz :
- (4) This value is given in dB, but it's possible to toggle to index value. Please refer to the document :AT command User Guide [7]

WARNING:

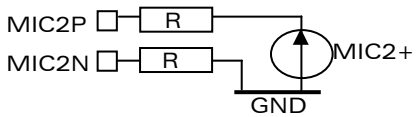
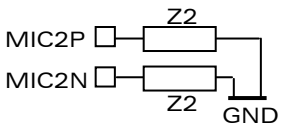
The voltage input value for MIC1 can't exceed the maximum working voltage, otherwise clipping will appear.

3.11.1.2 MIC2 Microphone Inputs

By default, the MIC2 inputs are differential ones, but it can be configured in single ended. They already include the convenient biasing for an electret microphone. The electret microphone can be directly connected on those inputs, thus allowing easy connection to a handset.

AC coupling is already embedded in the Wireless CPU®.

Equivalent circuits of MIC2

DC equivalent circuit	AC equivalent circuit
	

Electrical Characteristics of MIC2

Parameters		Min	Typ	Max	Unit
Internal biasing DC Characteristics	MIC2+	2	2.1	2.2	V
	Output current		0.5	1.5	mA
	R2	1650	1900	2150	Ω
AC Characteristics 200 Hz<F<4 kHz	Z2 MIC2P (MIC2N=Open)	1.1	1.3	1.6	kΩ
	Z2 MIC2N (MIC2P=Open)				
	Z2 MIC2P (MIC2N=GND)	0.9	1.1	1.4	
	Z2 MIC2N (MIC2P=GND)				
	Impedance between MIC2P and MIC2N	1.3	1.6	2	
Working voltage (MIC2P-MIC2N)	AT+VGT*=3500(4)		13.8	18.6 ***	mVrms
	AT+VGT*=2000(4)		77.5	104***	
	AT+VGT*=700(4)		346	466***	
Maximum rating voltage (MIC2P or MIC2N)	Positive			+7.35**	V
	Negative	-0.9			

- *The input voltage depends of the input micro gain set by AT command. Please refer to the document : AT command User Guide[7]
- **Because MIC2P is internally biased, it is necessary to use a coupling capacitor to connect an audio signal provided by an active generator. Only a passive microphone can be directly connected to the MIC2P and MIC2N inputs.
- *** This value is obtained with digital gain = 0 and for frequency = 1kHz ..
- (4) This value is given in dB, but it's possible to toggle to index value. Please refer to the document :AT command User Guide [7]

WARNING:

The voltage input value for MIC2 can't exceed the maximum working voltage, otherwise clipping will appear.

3.11.2 Speaker Features

The connection is single-ended on SPK1 and is differential or single-ended on SPK2. Using a differential connection to reject common mode noise and TDMA noise is strongly recommended. Moreover in single-ended mode, the power is divided by 4. When using a single-ended connection, be sure to have a very good ground plane, a very good filtering as well as shielding in order to avoid any disturbance on the audio path.

Parameter	Typ	Unit	Connection
Z (SPK1P, SPK1N)	16 or 32	Ω	single-ended mode
Z (SPK2P, SPK2N)	4	Ω	single-ended mode
Z (SPK2P, SPK2N)	8	Ω	Differential mode

3.11.2.1 Speakers Outputs Power

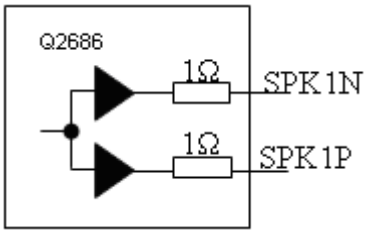
The both speakers maximum power output are not similar, that is due to the different configuration between the Speaker1 which is only single ended and the speaker2 which can be differential, so speaker2 can provides more power.

The maximal specifications given below are available with the maximum power output configuration values set by an AT command. The typical values are recommended.

3.11.2.1.1 SPK1 Speaker Outputs

With the SPK1 interface, only single ended speaker connection is allowed

Equivalent circuits of SPK1



Electrical Characteristics of SPK1

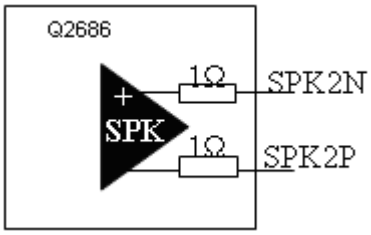
Parameters			Min	Typ	Max	Unit
Biasing voltage	-			1.30		V
Output swing voltage	RL=16Ω: AT+VGR=-1600**; single-ended		-	1.7	-	Vpp
	RL=32Ω; AT+VGR=-1600**; single-ended		-	1.9	2.75	Vpp
RL	Load resistance		14.5	32	-	Ω
IOUT	Output current; single-ended; peak value	RL=16Ω	-	40	85	mA
		RL=32Ω	-	22	-	mA
POUT	RL=16Ω; AT+VGR*=-1600**		-	25		mW
	RL=32Ω; AT+VGR*=-1600**		-	16	27	mW
RPD	Output pull-down resistance at power-down		28	40	52	kΩ

- *The output voltage depends of the output speaker gain set by AT command. Please refer to the document AT command User Guide [7].
- ** This value is given in dB, but it's possible to toggle to index value. Please refer to the document :AT command User Guide [7]

3.11.2.1.2 SPK2 Speaker Outputs

The SPK2 interface allows differential and single ended speaker connection

Equivalent circuits of SPK2



Electrical Characteristics of SPK2

Parameters		Min	Typ	Max	Unit
Biasing voltage	SPK2P and SPK2N		1.30		V
Output swing voltage	RL=8Ω: AT+VGR=-1000*; single ended	-	-	2	Vpp
	RL=8Ω: AT+VGR=-1000*; differential	-	-	4	Vpp
	RL=32Ω: AT+VGR=-1000*; single ended	-	-	2.5	Vpp
	RL=32Ω: AT+VGR=-1000*; differential	-	-	5	Vpp
RL	Load resistance	6	8	-	Ω
IOUT	Output current; peak value; RL=8Ω	-	-	180	mA
POUT	RL=8Ω; AT+VGR=-1000*;	-	-	250	mW
RPD	Output pull-down resistance at power-down	28	40	52	kΩ
VPD	Output DC voltage at power-down	-	-	100	mV

- *The output voltage depends of the output speaker gain set by AT command. Please refer to the document: AT command User Guide [7].This value is given in dB, but it's possible to toggle to index value.

If a singled ended solution is used with the speaker2 output, only one of the both SPK2 has to be chosen. The result is a maximal output power divided by 4.

3.11.3 Pin description

Signal	Pin number	I/O	I/O type	Description
MIC1P	40	I	Analog	Microphone 1 positive input
MIC1N	38	I	Analog	Microphone 1 negative input
MIC2P	36	I	Analog	Microphone 2 positive input
MIC2N	34	I	Analog	Microphone 2 negative input
SPK1P	35	O	Analog	Speaker 1 positive output
SPK1N	37	O	Analog	Speaker 1 negative output
SPK2P	39	O	Analog	Speaker 2 positive output
SPK2N	41	O	Analog	Speaker 2 negative output

3.12 Buzzer Output

This output is controlled by a pulse width modulation controller and may be used only as buzzer.

BUZZER0 is an open drain output. A buzzer can be directly connected between this output and VBATT. The maximum current is 100 mA (PEAK).

Pin description of PWM/Buzzer output

Signal	Pin number	I/O	I/O type	Reset state	Description
BUZZER0	15	O	Open drain	Z	Buzzer output

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

Electrical characteristics

Parameter	Condition	Minimum	Maximum	Unit
$V_{OL\ on}$	Iol = 100mA		0.4	V
I_{PEAK}	VBATT = VBATTmax		100	mA
Frequency		1	50000	Hz

3.13 Battery Charging Interface

The Q2686 Wireless CPU® supports one battery charging circuit, two algorithms and one hardware charging mode (pre-charging) for 3 battery technologies:

- Ni-Cd (Nickel-Cadmium) with algorithm 0
- Ni-Mh (Nickel-Métal Hydrure) with algorithm 0
- Li-Ion (Lithium-Ion) with the embedded PCM (Protection Circuit Module).algorithm 1

The two algorithms control a switch, which connects the CHG-IN signal to the VBATT signal. The algorithm controls the frequency and the connected time of the switching. During the charging procedure, battery charging level is monitored and when Li-Ion algorithm is used, battery temperature is monitored via the ADC1/BAT-TEMP input.

One more charging procedure is provided by the Q2686 Wireless CPU®. This is called "Pre-charging" mode, but is a special charging mode because it is activated only when the Wireless CPU® is OFF. Control is in this case only performed by the hardware. The purpose of this charging mode is to avoid battery damage by preventing the battery from being discharged to below the minimum battery level.

3.13.1 Ni-Cd / Ni-Mh Charging Algorithm

To charge the battery, the algorithm measures battery level when the switch is open (T2) and charges the battery by closing the switch (T3). When the battery is charged (battery voltage has reached BattLevelMax) the switch is open for time T3.

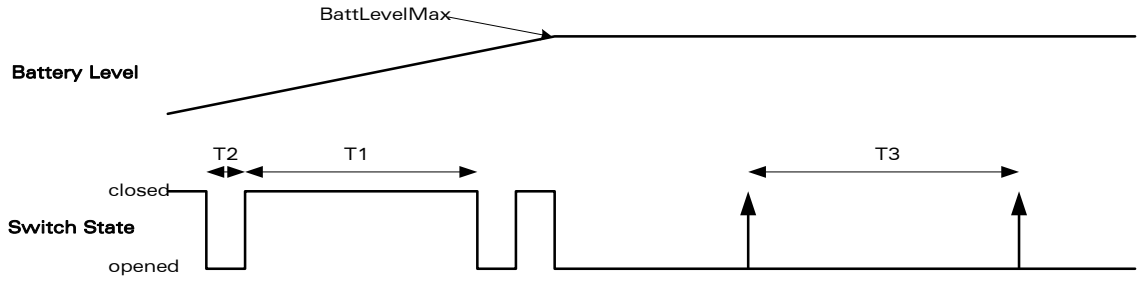


Figure 7: Ni-Cd / Ni-Mh charging waveform

Electrical characteristics of Ni-Cd / Ni-Mh battery timing charge

Parameter	Min	Typ	Max	Unit
T1		1		s
T2		0.1		s
T3		5		s

Note: T1,T2,T3 and BattLevelMax may be configured by AT command.

The battery level is monitored by the software (but not temperature)

3.13.2 Li-Ion Charging Algorithm

The Li-Ion algorithm provides battery temperature monitoring, which is highly recommended to prevent battery damage during the charging phase.

The Li-Ion charger algorithm can be broken down into three phases:

1. Constant charge
2. Beginning of pulse charge
3. End of pulse charge

The three phases can be seen on the following waveform for full charging:

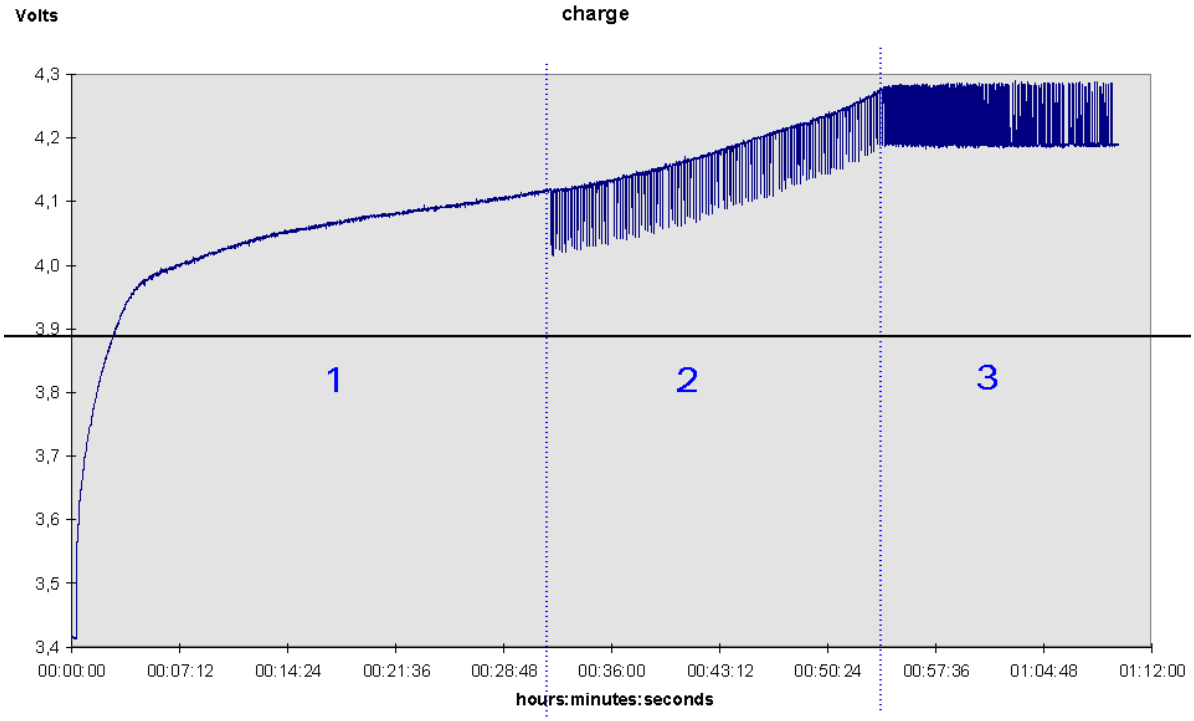


Figure 8: Li-Ion full charging waveform

Electrical characteristics of Li-Ion battery timing charge

Parameter		Min	Typ	Max	Unit
Step 1 switching	Closed		Always		s
Step 2 switching	Open		0.1		s
	Closed		1		s
Step 3 switching	Open	0.1		3	s
	Closed		1		s

3.13.3 Pre-charging

When a charger DC power supply is connected to the CHG-IN input and if the voltage battery is between 2.8V* and 3.2V, a constant current of 50mA is provided to the battery.

When the battery is able to supply the Q2686 Wireless CPU®, it is automatically powered on and the software algorithm is activated to finish the charge.

* For the Lithium-ion battery, the minimum voltage must be higher than PCM lock level.

Note: When pre-charging is launched, the LED0 output blinks automatically.

WARNING:

The Q2686 Wireless CPU® can not release the PCM protection inside Lithium battery pack. Voltage forbidden on the CHG-IN signal if no battery connected on VBATT signals.

3.13.4 Temperature Monitoring

Temperature monitoring is only available for the Li-Ion battery with algorithm 1. The ADC1/BAT-TEMP (pin 20) input must be used to sample the temperature analog signal provided by an NTC temperature sensor. The minimum and maximum temperature range may be set by AT command.

Pin description of battery charging interface

Signal	Pin number	I/O	I/O type	Description
CHG-IN	6,8	I	Analog	Current source input
ADC1/BAT-TEMP	20	I	Analog	A/D converter

Electrical characteristics of battery charging interface

Parameter		Minimum	Typ	Maximum	Unit
Charging operating temperature		0		50	°C
ADC1/BAT-TEMP (pin 20)	Maximum output code		1635		LSB
	Sampling rate		216		S/s
	Input Impedance (R)		1M		Ω
	Input signal range	0		2	V
CHG-IN (pin 6, 8)	Voltage (for I=Imax)	4.8*			V
	Voltage (for I=0)			6*	V
	DC Current	400**		800	mA

- * To be configured as specified by the battery manufacturer
- ** : Take care ; this value has to be selected in function of the power consumption mode used: please refer to the power consumption tables § 3.2.2.

WARNINGS:

- The Charger DC power supply must have an output current limited to 800mA.
- The maximum Charger output current, provided to the battery, must be accorded to the battery electrical characteristics.
- Li-Ion batteries must be used with the embedded PCM (Protection Circuit Module).
- The maximum charging voltage is up to 4,3V (Software drive)
- At the first plug, if the battery Li-ion is locked by its PCM the charger function doesn't work.

3.14 ON / ~OFF signal

This input is used to switch the Q2686 Wireless CPU® ON or OFF.

A high-level signal must be provided on the ON/~OFF pin to switch ON the Wireless CPU®. The voltage of this signal has to be maintained higher than 0.8 x VBATT during a minimum of 1500ms. This signal can be left at high level until switch-off.

To switch OFF the Wireless CPU®, the ON/OFF pin must be released. The Wireless CPU® can be switched off via the Operating System.

Pin description

Signal	Pin number	I/O	I/O type	Description
ON/~OFF	19	I	CMOS	Wireless CPU® Power-ON

Electrical characteristics of the signals

Parameter	I/O type	Minimum	Maximum	Unit
V_{IL}	CMOS		VBATT x 0.2	V
V_{IH}	CMOS	VBATT x 0.8	VBATT	V

Warning:

All external signals must be inactive when the Wireless CPU® is OFF to avoid any damage when starting and allow the Wireless CPU® to start and stop correctly.

3.14.1 Operating Sequences

3.14.1.1 Power-ON

Once the Wireless CPU® is supplied, the application must set the ON/OFF signal to high to start the Wireless CPU® power-ON sequence. The ON/OFF signal must be held high during a minimum delay of $T_{on/off\text{-}hold}$ (Minimum hold delay on the ON/~OFF signal) to power-ON. After this delay, an internal mechanism maintains the Wireless CPU® in power-ON condition.

During the power-ON sequence, an internal reset is automatically performed by the Wireless CPU® for 40ms (typical). Any external reset should be avoided during this phase.

Once initialization is completed (timing is SIM- and network-dependent), the AT interface answers "OK" to the application. For further details, please check the AT Commands User Guide [7].

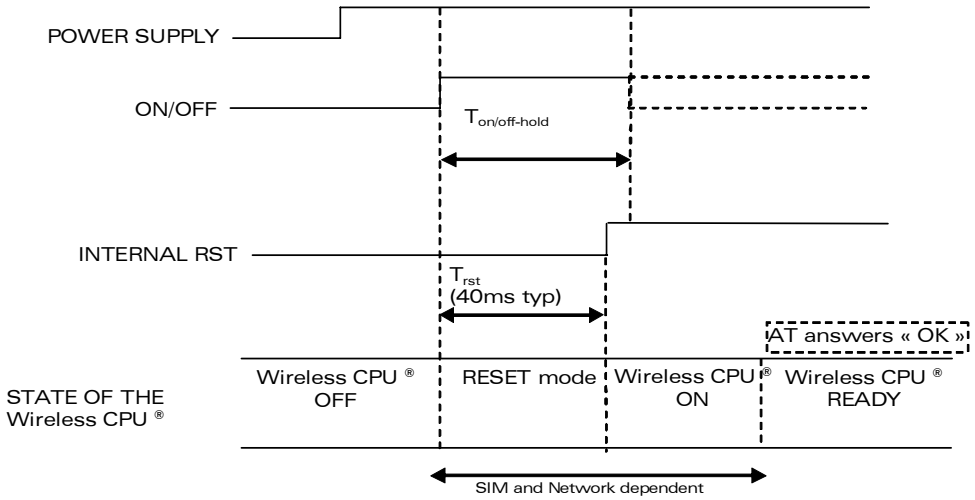


Figure 9: Power-ON sequence (no PIN code activated)

The duration of the firmware power-up sequence depends on:

- the need to perform a recovery sequence if the power has been lost during a flash memory modification.

Other factors have a minor influence

- the number of parameters stored in EEPROM by the AT commands received so far
- the ageing of the hardware components, especially the flash memory
- the temperature conditions

The *recommended* way to de-assert the ON/~OFF signal is to use either an AT command or WIND indicators: the application must detect the end of the power-up initialization and de-assert ON/~OFF afterwards.

- Send an "AT" command and wait for the "OK" answer: once the initialization is complete the AT interface answers « OK » to "AT" message[1].
- Wait for the "+WIND: 3" message: after initialization, the Wireless CPU®, if configured to do so, will return an unsolicited "+WIND: 3" message. The generation of this message is enabled or disabled via an AT command.

Note:
See also "AT Commands User Guide" [7] for more information on these commands.

[1] If the application manages hardware flow control, the AT command can be sent during the initialisation phase.

Proceeding thus – by software detection - will always prevent the application from de-asserting the ON/~OFF signal too early.

If WIND indicators are disabled or AT commands unavailable or not used, it is still possible to de-assert ON/~OFF after a delay long enough ($T_{on/off-hold}$) to ensure that the firmware has already completed its power-up initialization.

The table below gives the minimum values of $T_{on/off-hold}$:

$T_{on/off-hold}$ minimum values

Open AT® Firmware	$T_{on/off-hold}$ Safe evaluations of the firmware power-up time
Open AT® Software Suite v2	8 s (TBC)

The above figure take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But, they are safe because they are large enough to ensure that ON/~OFF is not de-asserted too early.

Additional notes:

1 Typical power-up initialization time figures for best cases conditions (no power-loss recovery, fast and new flash memory...) approximate 3.5 seconds in every firmware version. But releasing ON/~OFF after this delay does not guarantee that the application will actually start-up if for example the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command...

2 The ON/~OFF signal can be left at a high level until switch OFF. But this is not recommended as it will prevent the AT+CPOF command from performing a clean power-off. (see also Note in section 3.14.1.2 on Power-OFF for an alternate usage)

3 When using a battery as power source, it is not recommended to let this signal high:

4 If the battery voltage is too low and the ON/~OFF signal at low level, an internal mechanism switches OFF the Wireless CPU®. This automatic process prevents the battery to be over discharged and optimize its life span.

5 During the power-ON sequence, an internal reset is automatically performed by the Wireless CPU® for 40 ms (typical). Any external reset should be avoided during this phase.

6 After a reset (hardware or software), if the ON/~OFF signal is OFF (Low level) the Wireless CPU® switches OFF.

3.14.1.2 Power-OFF

To power-OFF the Wireless CPU® correctly, the application must reset the ON/OFF signal and then send the AT+CPOF command to deregister from the network and switch off the Wireless CPU®.

Once the "OK" response is issued by the Wireless CPU®, the power supply can be switched off.

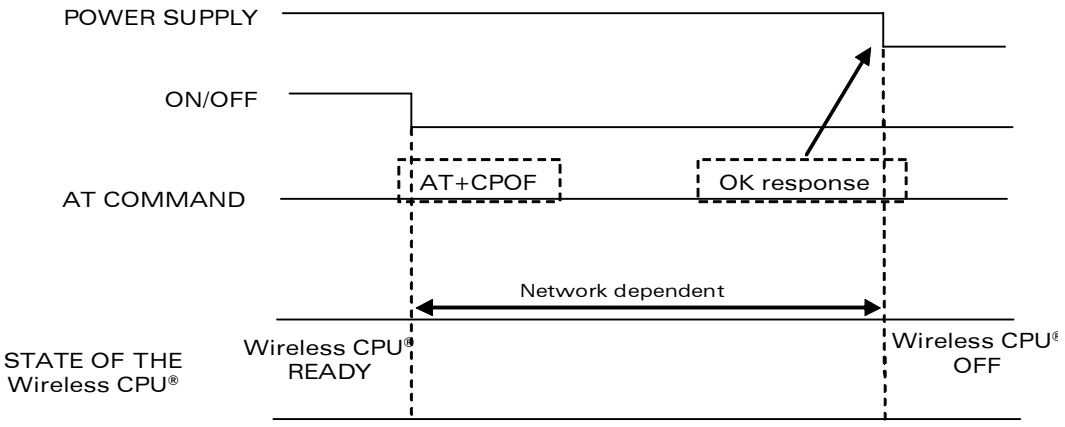


Figure 10: Power-OFF sequence

Additional notes:

1. If the ON/~OFF pin is maintained to ON (High Level), then the Wireless CPU® can't be switched OFF.
2. Connecting a charger on the Wireless CPU® as exactly the same effect than setting the ON/~OFF signal. In particular the Wireless CPU® will not POWER-OFF after the AT+CPOF command, unless the Charger is disconnected.

3.15 BOOT Signal

A specific BOOT control pin is available to download the Q2686 Wireless CPU® (only if the standard XModem download, controlled with AT command, is not possible).

A specific PC software program, provided by Wavecom, is needed to perform this specific download.

The BOOT pin must be connected to VCC_1V8 for this specific download.

Operating mode description

BOOT	Operating mode	Comment
Leave open	Normal use	No download
Leave open	Download XModem	AT command for Download AT+WDWL
1	Download specific	Need Wavecom PC software

For more information, see Q2686 / Open AT® Software Suite v2 AT Command User Guide [7].

This BOOT pin must be left open either for normal use or XModem download.

However, in order to render the development and maintenance phases easier, it is highly recommended to set a test point, either a jumper or a switch on the VCC_1V8 (pin 5) power supply.

Pin description

Signal	Pin number	I/O	I/O type	Description
BOOT	16	I	1V8	Download mode selection

3.16 Reset Signal (~RESET)

This signal is used to force a reset procedure by providing low level for at least 200µs. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-up sequence.

This signal may also be used to provide a reset to an external device (at power-up only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven by an open collector or an open drain.

The Wireless CPU® remains in reset mode as long as the ~RESET signal is held low.

CAUTION: This signal should only be used for "emergency" resets.

An Operating System reset is to be preferred to a hardware reset.

Reset sequence:

To activate the "emergency" reset sequence, the ~RESET signal must be set to low for 200µs minimum. As soon as the reset is completed, the AT interface answers "OK" to the application.

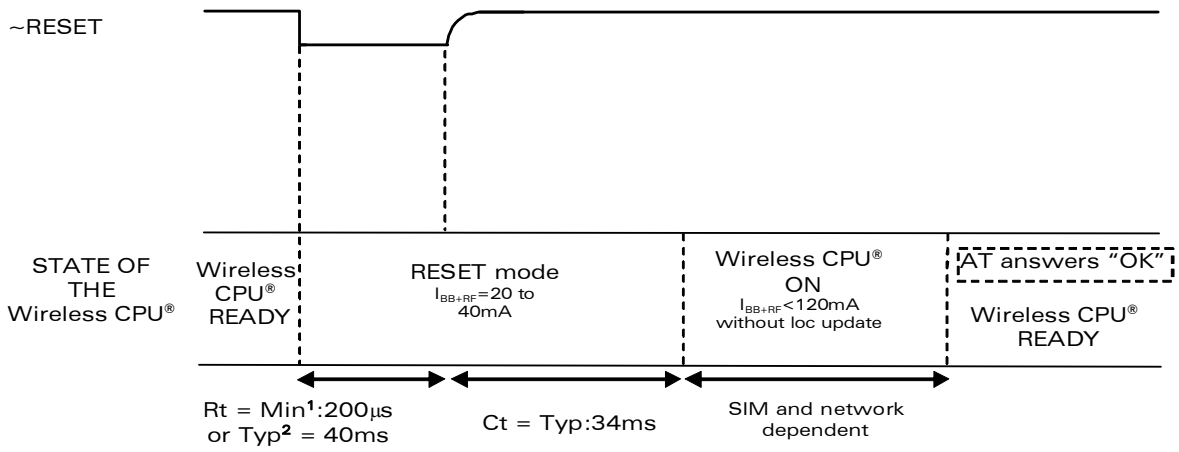


Figure 11: Reset sequence waveform

At power-up, the ~RESET time (Rt) is carried out after switching ON the Wireless CPU®. It is generated by the internal Q2686 Wireless CPU® voltage supervisor.

The ~RESET time is provided by the internal RC component. To keep the same time, it is not recommended to connect another R or C component on the ~RESET signal. Only a switch or an open drain gate is recommended.

Ct is the cancellation time required for the Wireless CPU® Q2686 initialization. Ct is automatically carried out by the Q2686 Wireless CPU® after a hardware reset.

Electrical characteristics of the signals

Parameter	Minimum	Typ	Maximum	Unit
Input Impedance (R)*		100		kΩ
Input Impedance (C)		10n		F
~RESET time (Rt) [1]	200			µs
~RESET time (Rt) [2] at power up only	20	40	100	ms
Cancellation time (Ct)		34		ms
V_H	0.57			V
V_{IL}	0		0.57	V
V_{IH}	1.33			V

* internal pull-up

* $V_{H:}$ Hysterisis Voltage

1 This reset time is the minimum to be carried out on the ~RESET signal when the power supply is already stabilized.

2 This reset time is internally carried out by the Wireless CPU® power supply supervisor only when the Wireless CPU® power supplies are powered ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
~RESET	18	I/O Open Drain	1V8	Wireless CPU® Reset

3.17 External Interrupt

The Q2686 Wireless CPU® provides two external interrupt inputs. These interrupt inputs can be activated on:

- High to low edge
- Low to high edge
- Low to high and high to low edge

When used, the interrupt inputs must not be left open.

If not used, they must be configured as GPIOs.

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
INT1	49	I	2V8	Z	External Interrupt	GPIO25
INT0	50	I	1V8	Z	External Interrupt	GPIO3

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

Electrical characteristics of the signals

Parameter		Minimum	Maximum	Unit
INT1	V_{IL}		0.84	V
	V_{IH}	1.96		V
INT0	V_{IL}		0.54	V
	V_{IH}	1.33		V

3.18 VCC_2V8 and VCC_1V8 Output

These outputs can only be used to connect pull-up resistor. **VCC_2V8** and **VCC_1V8** must be used as a reference supply. These voltages supplies are available when the Wireless CPU® is ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
VCC_2V8	10	O	Supply	Digital supply
VCC_1V8	5	O	Supply	Digital supply

Electrical characteristics of the signals

Parameter		Minimum	Typ	Maximum	Unit
VCC_2V8	Output voltage	2.74	2.8	2.86	V
	Output Current			15	mA
VCC_1V8	Output voltage	1.76	1.8	1.94	V
	Output Current			15	mA

3.19 BAT-RTC (Backup Battery)

The Q2686 Wireless CPU® provides an input/output to connect a Real Time Clock (RTC) power supply.

3.19.1 Interface Description

This pin is used as a back-up power supply for the internal **R**eal **T**ime **C**lock. The RTC is supported by the Wireless CPU® when VBATT is available, but a back-up power supply is needed to save date and time when VBATT is switched off (VBATT = 0V).

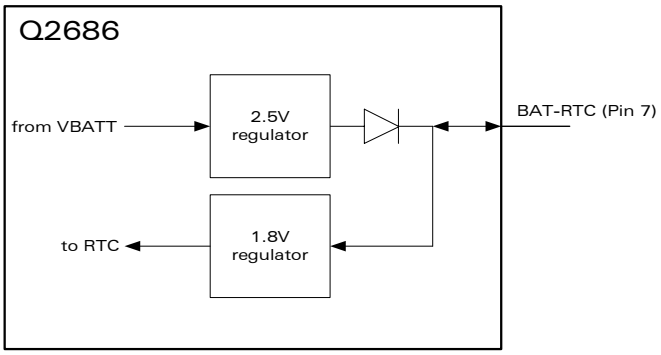


Figure 12: Real Time Clock power supply

If the RTC is not used, this pin can be left open.

If VBATT is available, the back-up battery can be charged by the internal 2.5V power supply regulator.

Pin description

Signal	Pin number	I/O	I/O type	Description
BAT-RTC	7	I/O	Supply	RTC Back-up supply

Electrical characteristics of the signals

Parameter	Minimum	Typ	Maximum	Unit
Input voltage	1.85		3.0	V
Input current consumption*		3.3		µA
Output voltage		2.45		V
Output current			2	mA

*Provided by an RTC back-up battery when Wireless CPU® power supply is off (VBATT = 0V).

3.20 LED0 Signal

LED0 is an open drain output. A LED and a resistor can be directly connected between this output and VBATT.

When the Q2686 Wireless CPU® is OFF, if 2.8V < VBATT < 3.2V and a charger is connected on CHG-IN inputs, this output flashes (100 ms ON, 900 ms OFF) to indicate the pre-charging phase of the battery.

When the Q2686 Wireless CPU® is ON, this output is used to indicate network status.

LED0 status

Q2686 state	VBATT status	LED0 status	Q2686 Wireless CPU® status
Wireless CPU® OFF	VBATT<2.8V or VBATT> 3.2V	OFF	Wireless CPU® is OFF
	2.8V < VBATT < 3.2V	Pre-charge flash LED ON for 100 ms, OFF for 900 ms	Wireless CPU® is OFF, Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
Wireless CPU® ON	VBATT > 3.2V	Permanent	Wireless CPU® switched ON, not registered on the network
		Slow flash LED ON for 200 ms, OFF for 2 s	Wireless CPU® switched ON, registered on the network
		Quick flash LED ON for 200 ms, OFF for 600 ms	Wireless CPU® switched ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	Wireless CPU® switched on, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description
LED0	17	O	Open Drain Output	1 and Undefined	LED driving

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

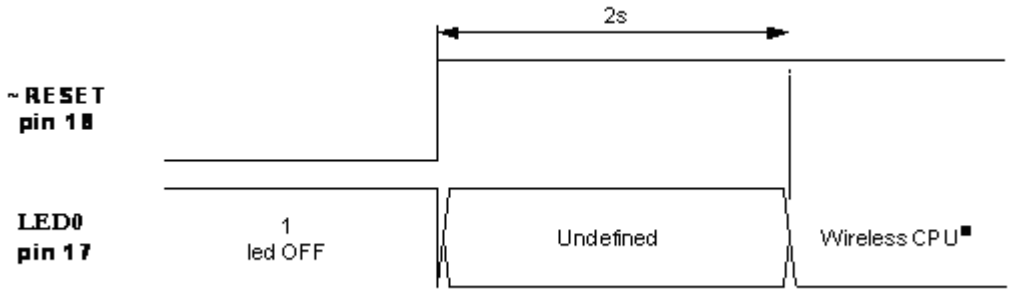


Figure 13: LED0 state during RESET and Initialization time

LED0 state is high during the RESET time and undefined during the software initialization time. During software initialization time, for 2 seconds max after RESET cancellation, the LED0 signal is toggling and does not provide Wireless CPU® status. After the 2s period, the LED0 provides the true status of the Wireless CPU®.

Electrical characteristics of the signal

Parameter	Condition	Minimum	Typ	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				8	mA

3.21 Digital Audio Interface (PCM)

Digital audio interface (PCM) interface mode allows connectivity with audio standard peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this mode allows to address a large range of audio peripherals.

PCM features:

- IOM-2 compatible device on physical level
- Master mode only with 6 slots by frame, user only on slot 0
- Bit rate single clock mode at 768kHz only
- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Long Frame Synchronization only
- Push-pull configuration on PCM-OUT and PCM-IN

The digital audio interface configuration cannot differ from that specified above.

3.21.1 Description

The PCM interface consists of 4 wires:

- PCM-SYNC (output): The frame synchronization signal delivers an 8 kHz frequency pulse that synchronizes the frame data in and the frame data out.
- PCM-CLK (output): The frame bit clock signal controls data transfer with the audio peripheral.
- PCM-OUT (output): The frame “data out” relies on the selected configuration mode.
- PCM-IN (input): The frame “data in” relies on the selected configuration mode.

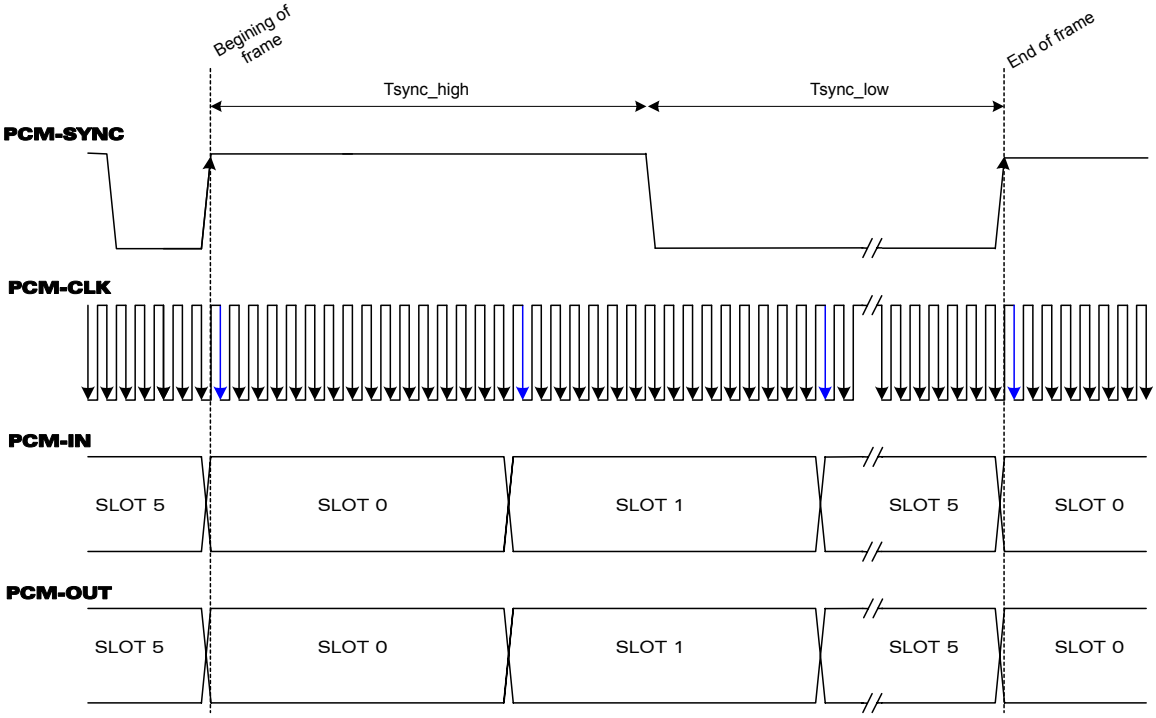


Figure 14: PCM frame waveform

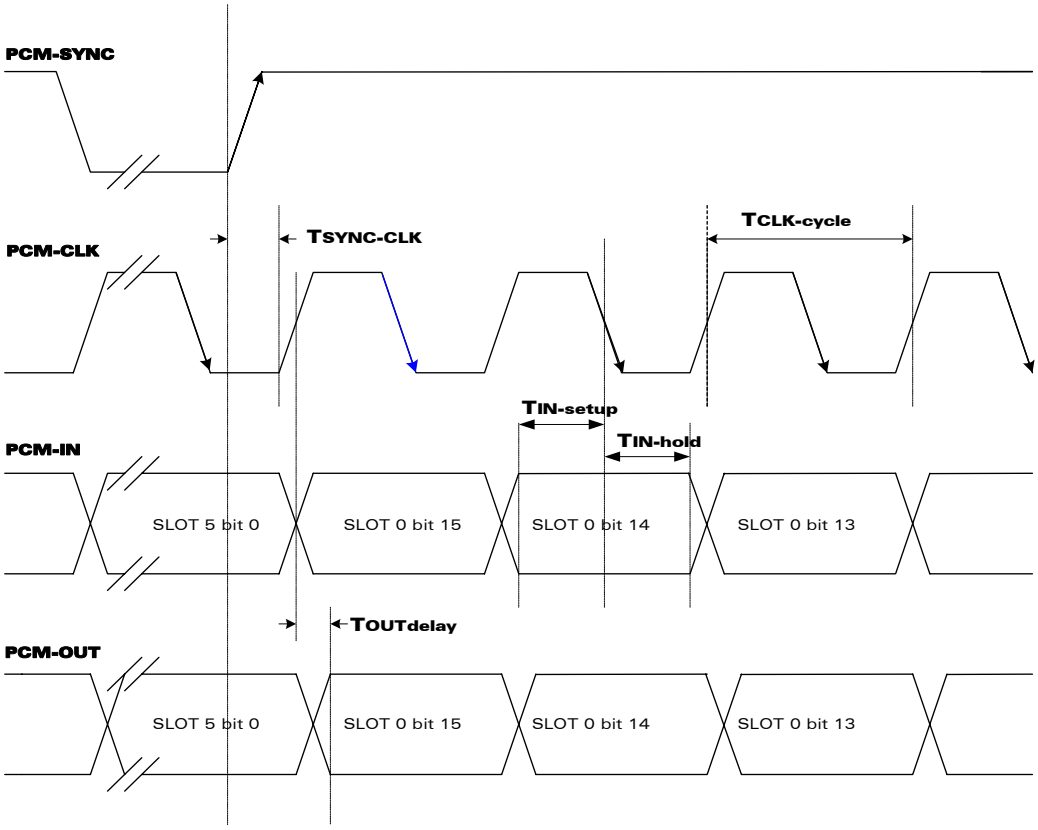


Figure 15: PCM sampling waveform

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
Tsync_low + Tsync_high	PCM-SYNC period		125		µs
Tsync_low	PCM-SYNC low time		93		µs
Tsync_high	PCM-SYNC high time		32		µs
TSYNC-CLK	PCM-SYNC to PCM-CLK time		-154		ns
TCLK-cycle	PCM-CLK period		1302		ns
TIN-setup	PCM-IN setup time	50			ns
TIN-hold	PCM-IN hold time	50			ns
TOUT-delay	PCM-OUT delay time			20	ns

Pin description of the PCM interface

Signal	Pin number	I/O	I/O type	Reset state	Description
PCM-SYNC	77	O	1V8	Pull-down	Frame synchronization 8 kHz
PCM-CLK	79	O	1V8	Pull-down	Data clock
PCM-OUT	80	O	1V8	Pull-up	Data output
PCM-IN*	78	I	1V8	Pull-up	Data input

*When using analog audio interface, the PCM_IN signal should be in HZ

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.22 USB 2.0 Interface

A 4-wire USB slave interface is available which complies with USB 2.0 protocol signaling. But it is not compliant with the electrical interface, due to the 5V of VPAD-USB.

The USB interface signals are VPAD-USB, USB-DP, USB-DM and GND.

USB interface features:

- 12Mbit/s full-speed transfer rate
- 3.3V typ compatible
- USB Softconnect feature
- Download feature is not supported by USB
- CDC 1.1 – ACM compliant

NOTE: A 5V to 3.3V typ voltage regulator is needed between the external interface power in line (+5V) and the Wireless CPU® line (VPAD-USB).

Pin description of the USB interface

Signal	Pin number	I/O	I/O type	Description
VPAD-USB	52	I	VPAD_USB	USB Power Supply
USB-DP	54	I/O	VPAD_USB	Differential data interface positive
USB-DM	56	I/O	VPAD_USB	Differential data interface negative

Electrical characteristics of the signals

Parameter	Min	Typ	Max	Unit
VPAD-USB, USB-DP, USB-DM	3	3.3	3.6	V
VPAD-USB Input current consumption		8		mA

3.23 RF Interface

The impedance is 50 Ω nominal and the DC impedance is 0 Ω.

3.23.1 RF Connections

U.FL Connector

A wide variety of cables fitted with U.FL connectors is offered by different suppliers.

Soldered solution

The soldered solution will preferably be based on an RG178 coaxial cable.

IMP connector

This connector is dedicated to board-to-board applications and must be soldered on the customer board. The supplier is Radiall (reference: R107 064 900).

Notes:

- The Q2686 Wireless CPU® does not support an antenna switch for a car kit, but this function can be implemented externally and can be driven using a GPIO.
- The antenna cable and connector should be selected in order to minimize losses in the frequency bands used for GSM 850/900MHz and 1800/1900MHz.
- 0.5dB may be considered as the maximum value of loss between the Wireless CPU® and an external connector.
- For mounting, assembly and handling of the IMP connector, please contact the supplier, Radiall, directly. Wavecom cannot provide customer support for use of this connector.

3.23.2 RF Performance

RF performance is compliant with the ETSI GSM 05.05 recommendation.

The main Receiver parameters are:

- GSM850 Reference Sensitivity = -104 dBm Static & TUHigh
- E-GSM900 Reference Sensitivity = -104 dBm Static & TUHigh
- DCS1800 Reference Sensitivity = -102 dBm Static & TUHigh
- PCS1900 Reference Sensitivity = -102 dBm Static & TUHigh
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

Transmitter parameters:

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900): 30 dBm +/- 2 dB at ambient temperature
- Minimum output power (EGSM & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature

3.23.3 Antenna Specifications

The antenna must meet the following requirements:

- The optimum operating frequency depends on the application. Either a dual-band or quad-band antenna will operate in these frequency bands and have the following characteristics:

Characteristic		Q2686			
		E-GSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50 Ω			
VSWR	Rx max	1.5:1			
	Tx max	1.5:1			
Typical radiated gain		0dBi in one direction at least			

4 Technical Specifications

4.1 General Purpose Connector Pin-out Description

Description	I/O*	Voltage	Signal Name		Pin Number		Signal Name		Voltage	I/O*	Description
			Mux	Nominal			Nominal	Mux			
Power Supply	I	VBATT		ADC0/ VBATT	1	2	ADC0/ VBATT		ADC0/ VBATT	I	Power Supply
Power Supply	I	VBATT		ADC0/ VBATT	3	4	ADC0/ VBATT		ADC0/ VBATT	I	Power Supply
1.8V Supply Output	O	VCC_1V8		VCC_1V8	5	6	CHG-IN		CHG-IN	I	Charger input
RTC Battery connection	I/O	BAT-RTC		BAT-RTC	7	8	CHG-IN		CHG-IN	I	Charger input
SIM Power Supply	O	1V8 or 3V		SIM-VCC	9	10	VCC_2V8		VCC_2V8	O	2.8V Supply Output
SIM Data	I/O	1V8 or 3V		SIM-IO	11	12	SIMPRES	GPIO18	VCC_1V8	I	SIM Detection
SIM reset Output	O	1V8 or 3V		~SIM-RST	13	14	SIM-CLK		1V8 or 3V	O	SIM Clock
Buzzer Output	O	Open Drain		BUZZER 0	15	16	BOOT		VCC_1V8	I	Not Used
LED0 Output	O	Open Drain		LED0	17	18	~RESET		VCC_1V8	I/O	RESET Input
ON / ~OFF Control	I	VBATT		ON/~OFF	19	20	BAT-TEMP		Analog	I	Analog temperature
Analog to Digital Input	I	Analog		ADC2	21	22	GPIO31		VCC_2V8	I/O	
SPI1 Clock	O	VCC_2V8	GPIO28	SPI1-CLK	23	24	SPI1-I	GPIO30	VCC_2V8	I	SPI1 Data Input
SPI1 Data Input / Output	I/O	VCC_2V8	GPIO29	SPI1-IO	25	26	SPI2-CLK	GPIO32	VCC_2V8	O	SPI2 Clock
SPI2 Data Input / Output	I/O	VCC_2V8	GPIO33	SPI2-IO	27	28	GPIO35		VCC_2V8	I/O	
SPI2 Data Input	I	VCC_2V8	GPIO34	SPI2-I	29	30	CT104-RXD2	GPIO15	VCC_1V8	O	Auxiliary RS232 Receive
Auxiliary RS232 Transmit	I	VCC_1V8	GPIO14	CT103-TXD2	31	32	~CT106-CTS2	GPIO16	VCC_1V8	O	Auxiliary RS232 Clear To Send
Auxiliary RS232 Request To Send	I	VCC_1V8	GPIO17	~CT105-RTS2	33	34	MIC2N		Analog	I	Micro 2 Input Negative
Speaker 1 Output Positive	O	Analog		SPK1P	35	36	MIC2P		Analog	I	Micro 2 Input Positive

Description	I/O*	Voltage	Signal Name		Pin Number		Signal Name		Voltage	I/O*	Description
			Mux	Nominal			Nominal	Mux			
Speaker 1 Output Negative	O	Analog		SPK1N	37	38	MIC1N		Analog	I	Micro 1 Input Negative
Speaker 2 Output Positive	O	Analog		SPK2P	39	40	MIC1P		Analog	I	Micro 1 Input Positive
Speaker 2 Output Negative	O	Analog		SPK2N	41	42	Reserved	**			
	I/O	VCC_2V8	32kHz	GPIO0	43	44	SCL1	GPIO26	Open Drain	O	I²C Clock
	I/O	VCC_2V8		GPIO19	45	46	SDA1	GPIO27	Open Drain	I/O	I²C Data
	I/O	VCC_2V8		GPIO21	47	48	GPIO20		VCC_2V8	I/O	
Interruption 1 Input	I	VCC_2V8	GPIO25	INT1	49	50	INT0	GPIO3	VCC_1V8	I	Interruption 0 Input
	I/O	VCC_1V8	**	GPIO1	51	52	VPAD-USB		VPAD-USB	I	USB Power supply input
	I/O	VCC_1V8	**	GPIO2	53	54	USB-DP		VPAD-USB	I/O	USB Data
	I/O	VCC_2V8	**	GPIO23	55	56	USB-DM		VPAD-USB	I/O	USB Data
	I/O	VCC_2V8	**	GPIO22	57	58	GPIO24		VCC_2V8	I/O	
Keypad column 0	I/O	VCC_1V8	GPIO4	COL0	59	60	COL1	GPIO5	VCC_1V8	I/O	Keypad column 1
Keypad column 2	I/O	VCC_1V8	GPIO6	COL2	61	62	COL3	GPIO7	VCC_1V8	I/O	Keypad column 3
Keypad column 4	I/O	VCC_1V8	GPIO8	COL4	63	64	ROW4	GPIO13	VCC_1V8	I/O	Keypad Row 4
Keypad Row 3	I/O	VCC_1V8	GPIO12	ROW3	65	66	ROW2	GPIO11	VCC_1V8	I/O	Keypad Row 2
Keypad Row 1	I/O	VCC_1V8	GPIO10	ROW1	67	68	ROW0	GPIO9	VCC_1V8	I/O	Keypad Row 0
Main RS232 Ring Indicator	O	VCC_2V8	GPIO42	~CT125-RI	69	70	~CT109-DCD1	GPIO43	VCC_2V8	O	Main RS232 Data Carrier Detect
Main RS232 Transmit	I	VCC_2V8	GPIO36	CT103-TXD1	71	72	~CT105-RTS1	GPIO38	VCC_2V8	I	Main RS232 Request To Send
Main RS232 Receive	O	VCC_2V8	GPIO37	CT104-RXD1	73	74	~CT107-DSR1	GPIO40	VCC_2V8	O	Main RS232 Data Set Ready
Main RS232 Clear To Send	O	VCC_2V8	GPIO39	~CT106-CTS1	75	76	~CT108-2-DTR1	GPIO41	VCC_2V8	I	Main RS232 Data Terminal Ready
PCM Frame Synchro	O	VCC_1V8		PCM-SYNC	77	78	PCM-IN		VCC_1V8	I	PCM Data Input
PCM Clock	O	VCC_1V8		PCM-CLK	79	80	PCM-OUT		VCC_1V8	O	PCM Data Output
				NC-1	81	82	Reserved				

Description	I/O*	Voltage	Signal Name		Pin Number		Signal Name		Voltage	I/O*	Description
			Mux	Nominal			Nominal	Mux			
				NC-3	83	84	NC-2				
				NC-5	85	86	NC-4				
				NC-7	87	88	NC-6				
				NC-9	89	90	NC-8				
				NC-11	91	92	NC-10				
				NC-13	93	94	NC-12				
				NC-15	95	96	NC-14				
				NC-17	97	98	NC-16				
				NC-19	99	100	NC-18				

* The I/O direction information is only for the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

** For more information about the multiplexing of these signals, see “General purpose input /output”, section 3.9

4.2 Labeling Correspondence between Q2686 and Open AT® Software Suite v2

Each signal has strictly the same characteristics: It is only a new designation in view to conform with the AT Command User Guide [7].

Signal Name Q2686 with SW preceding Open AT® Software Suite v2	Signal Name Q2686 with SW from Open AT® Software Suite v2	Description	I/O	PIN number
+VBATT	ADC0 / +VBATT	Possibility to read VBATT value using the ADC0	I	1,2,2,4
BAT-TEMP	ADC1/BAT-TEMP	Possibility to read either the Battery's temperature or something else customer specific	I	20
AUX-ADC	ADC2	Analog to Digital converter	I	21
SCL	SCL1		O	44
SDA	SDA1		I/O	46
FLASHLED	LED0		O	17
~SPI1_CS	GPIO31 / SPI1 Load		O	22
~SPI2_CS	GPIO35 / SPI2-Load		O	28
BUZZ-OUT	BUZZER0		O	15
GPIO44	GPIO0		I/O	43

4.3 Environmental Specifications

Wavecom specifies the following temperature range for the Q2686 product.

The Q2686 Wireless CPU® is compliant with the following operating class.

Conditions	Temperature range
Operating / Class A	-20 °C to +55°C
Operating / Class B	-30 °C to +85°C
Storage	-40 °C to +85°C

Function Status Classification:

Class A:

The Wireless CPU® remains fully functional, meeting GSM performance criteria in accordance with ETSI requirements, across the specified temperature range.

Class B:

The Wireless CPU® remains fully functional, across the specified temperature range. Some GSM parameters may occasionally deviate from the ETSI specified requirements and this deviation does not affect the ability of the Wireless CPU® to connect to the cellular network and function fully, as it does within the Class A range.

Q2686		ENVIRONNEMENTAL CLASSES		
TYPE OF TEST	STANDARDS	STORAGE Class 1.2	TRANSPORTATION Class 2.3	OPERATING (PORT USE) Class 7.3
Cold	IEC 68-2.1 Ab test	-25° C 72 h	-40° C 72 h	-20° C (GSM900) 16 h -10° C (GSM1800/1900) 16h
Dry heat	IEC 68-2.2 Bb test	+70° C 72 h	+70° C 72 h	+55° C 16 h
Change of temperature	IEC 68-2.14 Na/Nb test		-40° / +30° C 5 cycles t1 = 3 h	-20° / +30° C (GSM900) 3 cycles -10° / +30° C (GSM1800/1900): 3 cycles t1 = 3 h
Damp heat cyclic	IEC 68-2.30 Db test	+30° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1
Damp heat	IEC 68-2.56 Cb test	+30° C 4 days	+40° C 4 days	+40° C 4 days
Sinusoidal vibration	IEC 68-2.6 Fc test	5 - 62 Hz : 5 mm / s 62 - 200Hz : 2 m / s2 3 x 5 sweep cycles		
Random vibration wide band	IEC 68-3.36 Fdb test		5 - 20 Hz : 0.96 m2 / s3 20 - 500Hz : - 3 dB / oct 3 x 10 min	10 -12 Hz : 0.96 m2 / s3 12 - 150Hz : - 3 dB / oct 3 x 30 min

Figure 16: Environmental classes

4.4 Conformance with ATEX 94/9/CE directive

To evaluate the conformity of the final product with ATEX 94/9/CE directive the following datas must be taken into account:

- Sum of all capacitors : 84µF
- Sum of all inductances : 12µH

4.5 Mechanical Specifications

4.5.1 Physical Characteristics

The Q2686 Wireless CPU® has a complete self-contained shield.

- Overall dimensions : 32.2x40x4 mm (except shielding pins)
- Weight : <10 g

4.5.2 Mechanical Drawings

The mechanical specifications of the Q2686 Wireless CPU® are shown in the following page.

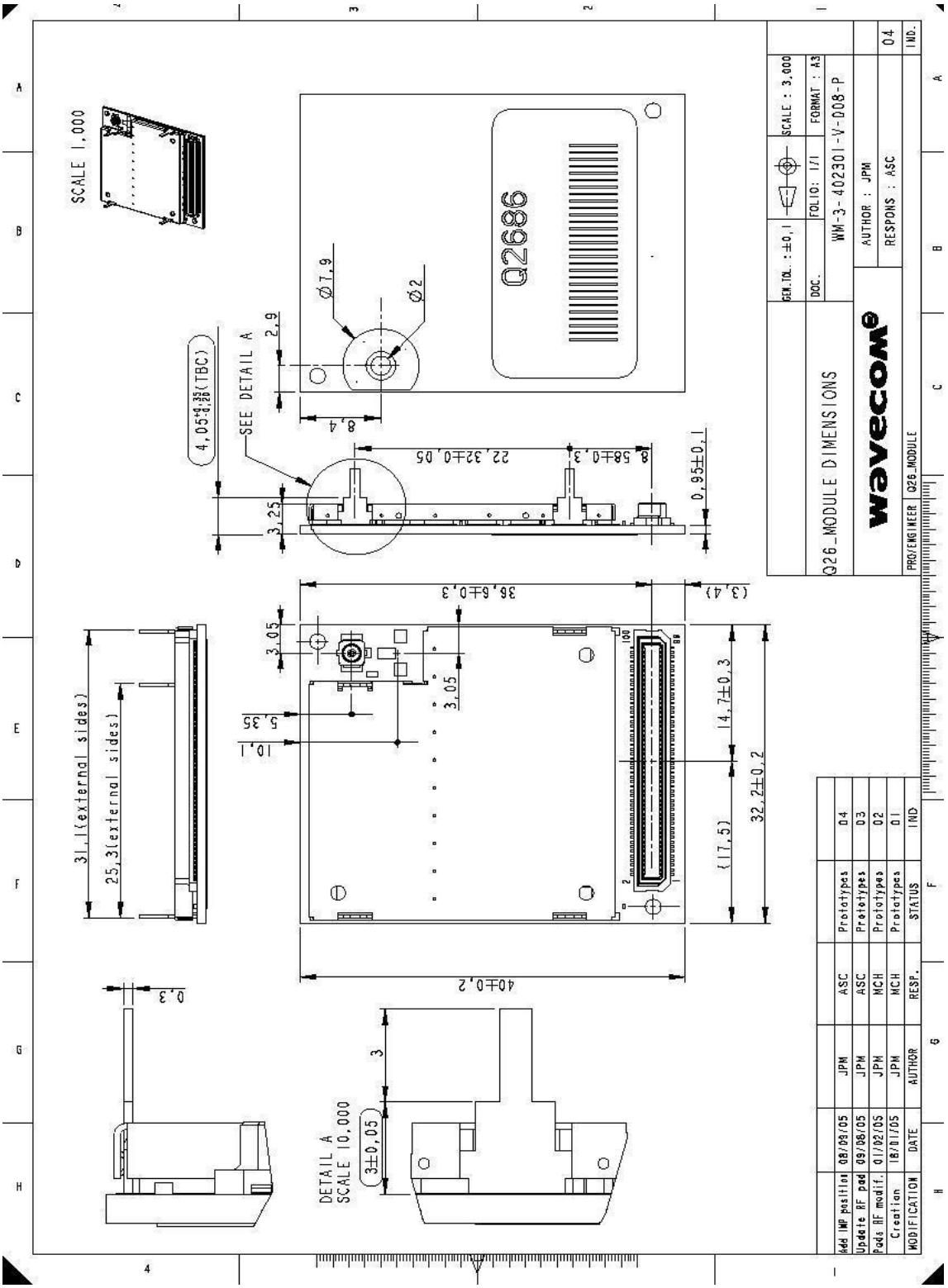


Figure 17: Mechanical drawing

5 Connector and Peripheral Device References

5.1 General Purpose Connector

The GPC is a 100-pin connector with 0.5mm pitch from the from PANASONIC Group's P5K series, with the following reference:

AXK600347BN1

The matting connector has the following reference:

AXK500147BN1J

The stacking height is 3.0 mm.

Wavecom recommends that you use the AXK500147BN1J connector for your application to benefit from Wavecom's prices. For more information, contact Wavecom, specifying the Wavecom connector reference: WM18868.

For further details see the GPC data sheets in the appendix. More information is also available from http://www.panasonic.com/host/industrl.html

5.2 SIM Card Reader

- ITT CANNON CCM03 series (see http://www.ittcannon.com)
- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.com)
- MOLEX 99228-0002 (connector) / MOLEX 91236-0002 (holder) (see http://www.molex.com)

5.3 Microphone

Possible suppliers:

- HOSIDEN
- PANASONIC
- PEIKER

5.4 Speaker

Possible suppliers:

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

5.5 Antenna Cable

A wide variety of cables fitted with UF-L connectors is offered by HIROSE:

- UF-L pigtails, Ex: Ref = **U.FL-2LP(V)-04-A-(100)**
- UF-L Ref = **U.FL-R-SMT**
- UF-L cable assemblies,
- Between series cable assemblies.

More information is also available from http://www.hirose-connectors.com/.

A coaxial cable can also be soldered on the RF pad. The following references have been certified for mounting on the Q2686 Wireless CPU®:

- RG178
- RG316

5.6 RF Board-to-board Connector

The supplier for the IMP connector is Radiall (http://www.radiall.com), with the following reference:

- R107 064 900.

5.7 GSM Antenna

GSM antennas and support for antenna adaptation can be obtained from manufacturers such as:

- ALLGON (http://www.allgon.com)
- IRSCHMANN (http://www.hirschmann.com/)

6 Design Guidelines

The purpose of the following paragraphs is to give design guidelines.

6.1 HARDWARE and RF

6.1.1 EMC Recommendations

The EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band
- ESD protection is mandatory on all signals which have external accessibility (typically human accessibility). See Q2686 Wireless CPU® Customer Design Guidelines WM_PRJ_Q2686_PTS_003 [10] for ESD protection samples.
    - Typically, ESD protection is mandatory for the:
        - SIM (if accessible from outside)
        - Serial link
- EMC protection on audio input/output (filters against 900MHz emissions)
- Biasing of the microphone inputs
- Length of the SIM interface lines (preferably <10cm)
- Ground plane: Wavecom recommends a common ground plane for analog/digital/RF grounds.
- A metallic case or plastic casing with conductive paint are recommended

Note:

The Wireless CPU® does not include any protection against over-voltage.

6.1.2 Power Supply

The power supply is one of the key issues in the design of a GSM terminal.

A weak power supply design could, in particular, affect:

- EMC performance
- The emission spectrum
- The phase error and frequency error

WARNING:

Careful attention should be paid to:

- The quality of the power supply: low ripple, PFM or PSM systems should be avoided (PWM converter preferred).
- Capacity to deliver high current peaks in a short time (pulsed radio emission).

6.1.3 Layout Requirement

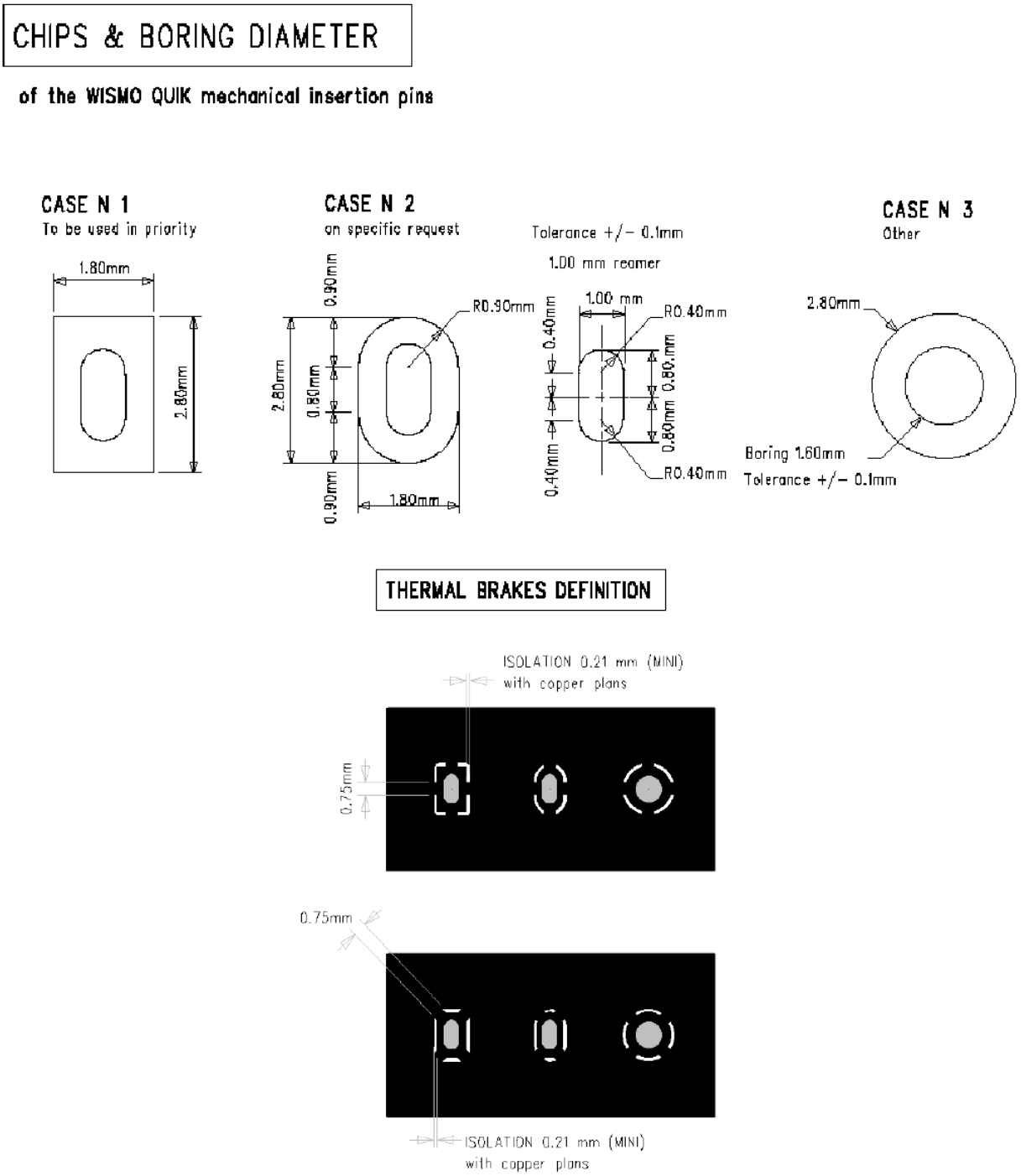


Figure 18: Layout requirement

6.1.4 Antenna

WARNING:

Wavecom strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.

Both the mechanical and electrical antenna adaptation is one of the key issues in the design of the GSM terminal.

6.2 Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Leads of the Wireless CPU® to be soldered to the Ground plane

6.3 Operating System Upgrade

The Q2686 Wireless CPU® Operating System is stored in flash memory and can easily be upgraded.

IMPORTANT:

In order to follow regular changes in the GPRS standard and to offer a state-of-the-art Operating System, Wavecom recommends that the application designed around a Wireless CPU® (or Wireless CPU® based product) allow easy Operating System upgrades on the Wireless CPU® via the standard X-modem protocol. Therefore, the application shall either allow a direct access to the Wireless CPU® serial link through an external connector or implement any mechanism allowing the Wireless CPU® Operating System to be downloaded via X-modem.

The Operating System file can be downloaded to the modem using the X-modem protocol. The AT+WDWL command allows the download process to be launched (see the description in the AT Command User Guide [7]).

The serial signals required to proceed with X-modem downloading are:

Rx, Tx, RTS, CTS and GND.

The Operating System file can also be downloaded to the modem using the DOTA (download over the air) feature. This feature is available with the Open AT® interface. For more details, please, refer to the Open AT® documentation listed in section 1.1.1.

7 Appendix

7.1 Standards and Recommendations

GSM ETSI, 3GPP, GCF and NAPRD03 recommendations for Phase II & FCC.

Specification Reference	Title
3GPP TS 45.005 v5.5.0 (2002-08) Release 5	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception
GSM 02.07 V8.0.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); Mobile Stations (MS) features (GSM 02.07 version 8.0.0 Release 1999)
GSM 02.60 V8.1.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description, Stage 1 (GSM 02.60 version 8.1.0 Release 1999)
GSM 03.60 V7.9.0 (2002-09)	Technical Specification Group Services and System Aspects; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description; Stage 2 (Release 1998)
3GPP TS 43.064 V5.0.0 (2002-04)	Technical Specification Group GERAN; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Overall description of the GPRS radio interface; Stage 2 (Release 5)
3GPP TS 03.22 V8.7.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Functions related to Mobile Station (MS) in idle mode and group receive mode; (Release 1999)
3GPP TS 03.40 V7.5.0 (2001-12)	Technical Specification Group Terminals; Technical realization of the Short Message Service (SMS) (Release 1998)
3GPP TS 03.41 V7.4.0 (2000-09)	Technical Specification Group Terminals; Technical realization of Cell Broadcast Service (CBS) (Release 1998)
ETSI EN 300 903 V8.1.1 (2000-11)	Digital cellular telecommunications system (Phase 2+); Transmission planning aspects of the speech service in the GSM Public Land Mobile Network (PLMN) system (GSM 03.50 version 8.1.1 Release 1999)

Specification Reference	Title
3GPP TS 04.06 V8.2.1 (2002-05)	Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station - Base Station System (MS - BSS) interface; Data Link (DL) layer specification (Release 1999)
3GPP TS 04.08 V7.18.0 (2002-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Mobile radio interface layer 3 specification (Release 1998)
3GPP TS 04.10 V7.1.0 (2001-12)	Technical Specification Group Core Networks; Mobile radio interface layer 3 Supplementary services specification; General aspects (Release 1998)
3GPP TS 04.11 V7.1.0 (2000-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Point-to-Point (PP) Short Message Service (SMS) support on mobile radio interface (Release 1998)
3GPP TS 45.005 v5.5.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception (Release 5)
3GPP TS 45.008 V5.8.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem link control (Release 5)
3GPP TS 45.010 V5.1.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem synchronization (Release 5)
3GPP TS 46.010 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Transcoding (Release 5)
3GPP TS 46.011 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Substitution and muting of lost frames for full rate speech channels (Release 5)
3GPP TS 46.012 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Comfort noise aspect for full rate speech traffic channels (Release 5)

Specification Reference	Title
3GPP TS 46.031 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Discontinuous Transmission (DTX) for full rate speech traffic channels (Release 5)
3GPP TS 46.032 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Voice Activity Detector (VAD) for full rate speech traffic channels (Release 5)
TS 100 913V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General on Terminal Adaptation Functions (TAF) for Mobile Stations (MS) (GSM 07.01 version 8.0.0 Release 1999)
GSM 09.07 V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General requirements on interworking between the Public Land Mobile Network (PLMN) and the Integrated Services Digital Network (ISDN) or Public Switched Telephone Network (PSTN) (GSM 09.07 version 8.0.0 Release 1999)
3GPP TS 51.010-1 v5.0.0 (2002-09)	Technical Specification Group GSM/EDGE ; Radio Access Network ;Digital cellular telecommunications system (Phase 2+);Mobile Station (MS) conformance specification; Part 1: Conformance specification (Release 5)
3GPP TS 51.011 V5.0.0 (2001-12)	Technical Specification Group Terminals; Specification of the Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (Release 5)
ETS 300 641 (1998-03)	Digital cellular telecommunications system (Phase 2); Specification of the 3 volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)
GCF-CC V3.7.1 (2002-08)	Global Certification Forum – Certification criteria
NAPRD03 V2.6.0 (2002-06)	North America Permanent Reference Document for PTCRB tests

The Q2686 Wireless CPU® connected on a development kit board application is certified to be in accordance with the following Rules and Regulations of the Federal Communications Commission (FCC).

Power listed on the Gant is conducted for Part 22 and conducted for Part 24

This device contains GSM, GPRS Class 10 functions in the 900 and 1800MHz Band, which are not operational in U.S. Territories.

This device is to be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Antennas used for this OEM module must not exceed 3.0dBi gain for PCS 1900 MHz and 7.4dBi GSM 850 MHz for mobile and fixed operating configurations. This device is approved as a module to be installed in other devices.

Installed in other portable devices, the exposure conditions require a separate equipment authorization.

The license module had a FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.

If not, a second label must be placed on the outside of the device that contains the following text:
Contains FCC ID: **O9E-Q2686**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference,
(2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT: Manufacturers of mobile or fixed devices incorporating Q2686 Wireless CPU® are advised to

- clarify any regulatory questions,
- have their completed product tested,
- have product approved for FCC compliance, and
- include instructions according to above mentioned RF exposure statements in end product user manual.

Please note that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

7.2 Safety Recommendations (for information only)

IMPORTANT
FOR THE EFFICIENT AND SAFE OPERATION OF YOUR GSM APPLICATION BASED ON Q2686 Wireless CPU®
PLEASE READ THIS INFORMATION CAREFULLY

7.2.1 RF Safety

7.2.1.1 General

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

7.2.1.2 Exposure to RF Energy

There has been some public concern on possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

7.2.1.3 Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

7.2.1.4 Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using of unauthorized antennas, modifications or attachments could damage the terminal and may violate local RF emission regulations or invalidate type approval.

7.2.2 General Safety

7.2.2.1 Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off from the road and park before making or answering a call if driving conditions so require.

7.2.2.2 Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

7.2.2.3 Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

7.2.2.4 Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

7.2.2.5 Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. In order to prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

7.2.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

7.2.2.7 Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

7.2.2.8 Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.

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