Product Technical Specification &
Customer Design Guidelines

Q52 Omni Wireless CPU®

Reference: **WI_DEV_ASSM_PTS_001**

Revision: **004**

Date: **December 01, 2008**

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Powered by the Wavecom Operating System and Open AT®

Document History

Level	Date	List of revisions	
001	March 5, 2008	Creation	Wavecom
002	August 26, 2008	Update	Wavecom
003	November 14, 2008	Addition of the "Declaration of Conformity"	Wavecom
004	December 1, 2008	Update	Wavecom

Overview

This document defines and specifies the Q52 Omni GSM/Orbcomm dual mode transceiver.

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Cautions

This platform contains a modular transmitter. This device is used for wireless applications. Note that all electronics parts and elements are ESD sensitive.

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1 References

1.1 Reference Documents

For more details, several reference documents may be consulted. The Wavecom reference documents are provided in the Wavecom document package, contrary to the general reference documents which are not authored by Wavecom.

1.1.1 Wavecom Reference Documentation

[1] Wireless Microprocessor® WMP100 Technical Specification

Reference: WM_DEV_WUP_PTS_004

[2] WMP100 Development Kit User Guide

Reference: WM_DEV_WUP_UGD_001

[3] AT Command Interface Guide for Open AT® Firmware v7.0

Reference: WM_DEV_OAT_UGD_059

1.1.2 General Reference Documents

[4] "I^{2}C Bus Specification", Version 2.0, Philips Semiconductor 1998

[5] ISO 7816-3 Standard

1.2 List of Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate

Abbreviation	Definition
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency

Abbreviation	Definition
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Wireless CPU
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio

2 General Description

2.1 General Information

The Q52 Omni is a dual mode GSM/Orbcomm transceiver consisting of an E-GSM/GPRS 900/1800 and 850/1900 quad-band GSM transceiver combined with a full function Orbcomm transceiver. The operating mode of the dual mode transceiver is managed by an internal communication controller that employs an always best connected strategy with priority given to the GSM mode of operation

2.1.1 Overall Dimensions

Length: 114.55 mm

Width: 47.5 mm

Thickness: 16.2 mm

2.1.2 Environment and Mechanics

- Green policy: RoHS compliant
- Complete shielding

The Q52 Omni is compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE)".

Transceivers which are compliant with this directive are identified by the RoHs logo on their label.

2.1.3 Transceiver Features

- 2-Watt EGSM 900/GSM 850 radio
- 1-Watt GSM1800/1900 radio
- Hardware GPRS class 10 capable
- Internal GSM SIM card
- 5-Watt Orbcomm radio

2.1.4 Primary Interfaces

- Power supply
- 2[*] UARTs Serial links
- GSM Analog audio
- Serial Protocol Interface (SPI)
- I^2C Interface
- 2 A/D inputs and 1 D/A output
- Digital I/Os
- GSM , GPS[†] and Orbcomm antenna ports

2.1.5 Operating System

- Real Time Clock with calendar
- Echo Cancellation + noise reduction (quadri codec)
- Full GSM or GSM/GPRS Operating System stack
- Full Orbcomm Operating System stack
- Full GPS Operating System Stack[‡]

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[*] *One on Version with GPS functionnality*
[†] *According to version*
[‡] *According to version*

2.2 Functional Description

The top level architecture of the Q52 Omni is described below:

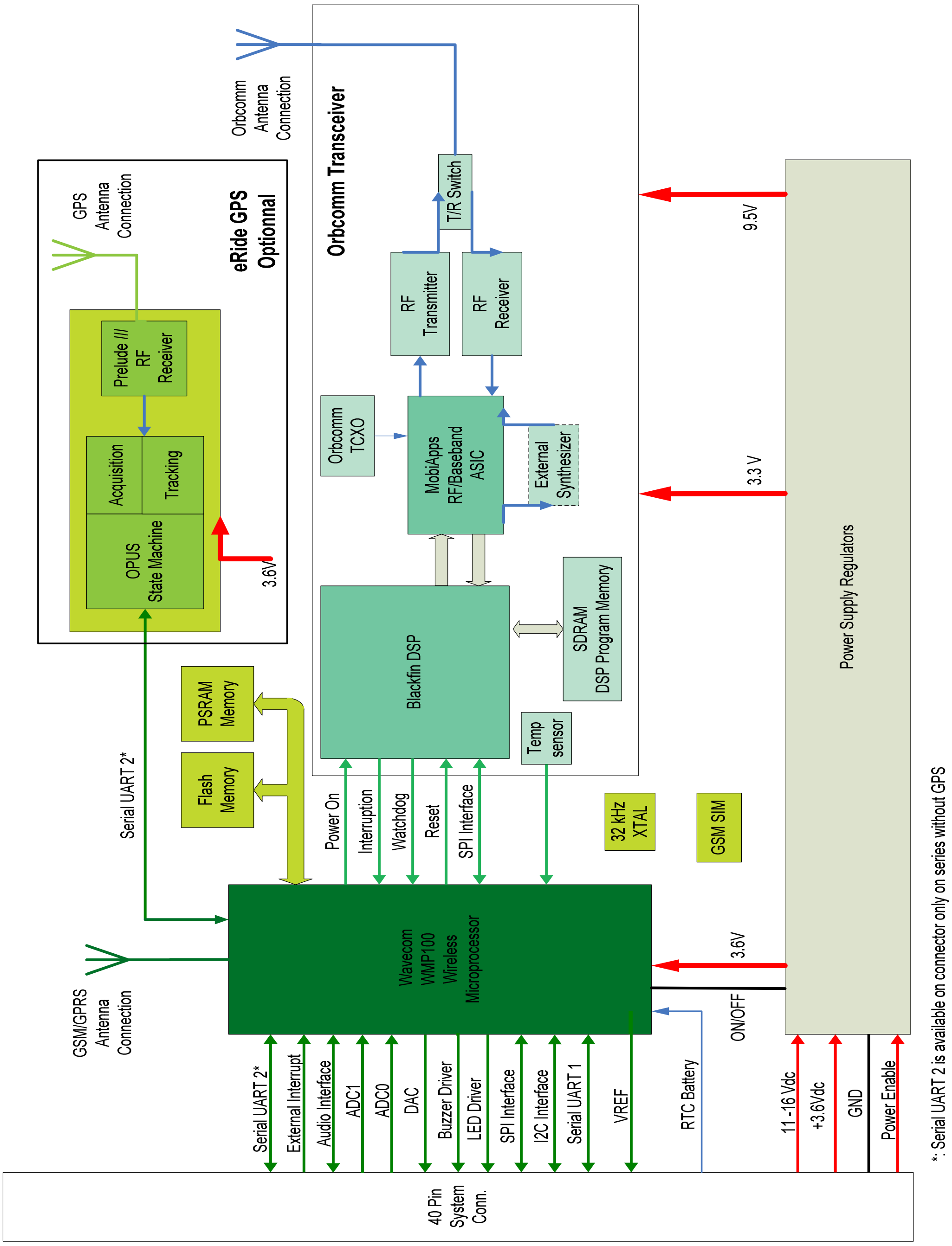


Figure 1: Top Level Architecture

2.2.1 GSM Functionalities

The Radio Frequency (RF) range of the GSM transceiver complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendations. The frequencies are:

	Transmit band (Tx)	Receive band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PCS 1900	1850 to 1910 MHz	1930 to 1990 MHz

Table 1: GSM /GPRS Frequency

2.2.2 Orbcomm Functionality

TBD

2.3 Operating System

The Operating System offers an extensive set of AT commands to control both the GSM and Orbcomm functionality of the module.

The Operating System in the module is Open AT® compliant. This enables the application developer to optionally integrate various types of specific process applications such as vertical applications (telemetry, multimedia, automotive...) into the internal ARM9 microprocessor.

3 Interfaces

3.1 System Connector

Pin	Signal	Description	Dir	Pin Type	Alternate Function
1	*BUZZ-OUT*	Buzzer Output	O	Open Drain	
2	*VREF_2V8*	Logic Voltage Reference	O	V-Ref	
3	*FLASH-LED*	Flash LED Driver	O	Open Drain	
4	*BAT-RTC*	Battery for RTC	I/O	Power	
5	*GND*	Chassis Ground		Ground	
6	*GND*	Chassis Ground		Ground	
7	*SPK2*	Speaker Audio from module	O	Audio	
8	*GND*	Chassis Ground		Ground	
9	*AGND*	Analog Reference		Ground	
10	*MIC2*	Microphone Audio to module	I	Audio	
11	*DAC0*	8 bit D/A Converter Output	O	0 - 2 volts	
12	*PWR_EN*	Switches the module on/off	I		
13	*ADC0*	10 bit A/D Converter Input	I	0 - 2 volts	
14	*ADC1*	10 bit A/D Converter Input	I	0 - 2 volts	
15	*HW_SD*	Hardware Shutdown	I/O	CMOS_2V8	
16	*EXT-INT0*	External Interrupt Signal	I	CMOS_1V8	GPIO3
17	*SPI-I*	SPI Input (four wire interface)	I	CMOS_2V8	GPIO30
18	*SPI1-IO*	SPI1 Out (four wire interface) SPI1 IO (three wire interface)	O I/O	CMOS_2V8	GPIO29
19	*SPI-CLK*	SPI1 Clock	I/O	CMOS_2V8	GPIO28
20	*SPI-CS*	SPI1 Chip Select	O	CMOS_2V8	GPIO31
21	*GND*	Chassis Ground		Ground	
22	*GND*	Chassis Ground		Ground	
23	*DCD1*	Data Carrier Detect_UART1	O	CMOS_2V8	GPIO43
24	*RI1*	Ring Indicator_UART1	O	CMOS_2V8	GPIO42
25	*CTS1*	Clear to Send_UART1	O	CMOS_2V8	GPIO39

Pin	Signal	Description	Dir	Pin Type	Alternate Function
26	*DTR1*	Data Terminal Ready_UART1	I	CMOS_2V8	GPIO41
27	*TXD1*	Transmit Data_UART1	I	CMOS_2V8	GPIO36
28	*RTS1*	Request to Send_UART1	I	CMOS_2V8	GPIO38
29	*VCC_12V*	12 VDC supply input	I	Power	
30	*RXD1*	Receive Data_UART1	O	CMOS_2V8	GPIO37
31	*VCC_12V*	12 VDC supply input	I	Power	
32	*VCC_12V*	12 VDC supply input	I	Power	
33	*VCC_3V6*	3.6 VDC regulated supply	I	Power	
34	*VCC_3V6*	3.6 VDC regulated supply	I	Power	
35	*SDA_I2C*	I^2C Data	I/O	Open Drain	GPIO27
36	*SCL_I2C*	I^2C Clock	O	Open Drain	GPIO26
37	*TXD2*	Transmit Data_UART2	I	CMOS_1V8	GPIO14
38	*CTS2*	Clear to Send_UART2	O	CMOS_1V8	GPIO16
39	*RXD2*	Receive Data_UART2	O	CMOS_1V8	GPIO15
40	*RTS2*	Request to Send_UART2	I	CMOS_1V8	GPIO17

Table 2: System connector pinout

3.2 Power Supply

3.2.1 Power Supply Description

The power supply required for the Q52Omni is a dual rail supply; VCC_3V6 and VCC_12V. VCC_12V is only required to support Satellite mode operation. VCC_3V6 is used for GSM/GPRS, Satellite and GPS operation.

The power supply is one of the key issues in the design of a dual mode terminal. Operation in GSM mode requires particularly careful attention to the ability of the power supply to provide clean DC power.

Due to the burst emission mode used in GSM/GPRS, the VCC_3V6 power supply must be able to deliver high current peaks in a short time. During the peaks, the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit (see Table 3: Power Supply Voltage).

- In communication mode, a GSM/GPRS class 2 terminal emits 577µs radio bursts every 4.615ms (see Figure 2).

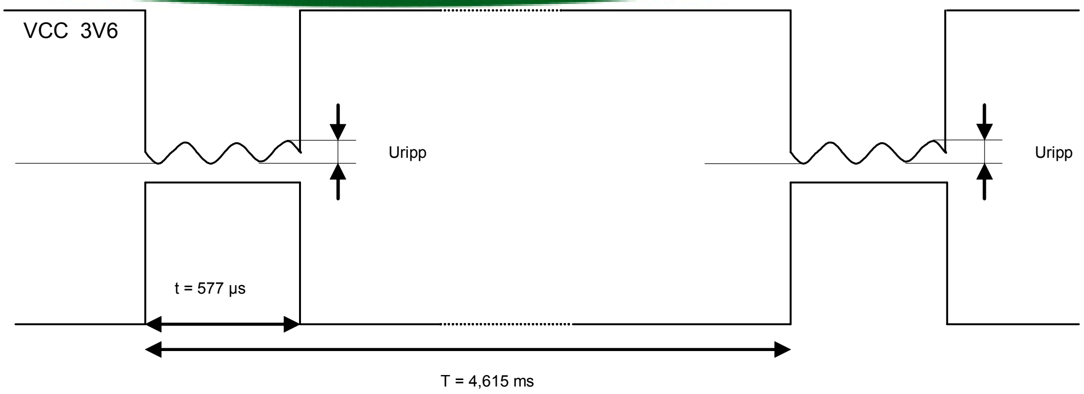


Figure 2: Power supply during burst emission

- In communication mode, a GPRS class 10 terminal emits 1154µs radio bursts every 4.615ms.

Only the VCC_3V6 (+3.6 VDC) power supply input is necessary during GSM mode of operation

VCC_3V6:

- Supplies the GSM RF components. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error.

The RF Power Amplifier current (**2.0 A** peak in GSM /GPRS mode) flows with a ratio of:

- 1/8 of the time (around 577µs every 4.615ms for GSM /GPRS cl. 2) and
- 2/8 of the time (around 1154µs every 4.615ms for GSM /GPRS cl. 10).

The rise time is around 10µs.

- Supplies the GSM baseband components

	V_{min}	V_{nom}	V_{max}	Ripple max (U_{ripp})
VCC_12V	11.0	13.6	16.0	TBD mVpp
VCC_3V6[1, 2]	3.6	3.8	4.0	200mVrms

Table 3: Power Supply Voltage

(1): This value has to be guarantied during the burst (with **2.0A** Peak in GSM or GPRS mode)
(2): Max operating Voltage Stationary Wave Ratio (VSWR) 2:1

When the Wireless CPU® is in Alarm mode, no voltage must be applied on any pin of the 40-pin connector except on VRTC (pin 4) for RTC operation or PWR_EN (pin 12) to power ON the dual mode Transceiver.

When supplying the Q52 OMNI with a battery, the total impedance (battery+protections+PCB) on 3V6 should be <150 mOhms.

3.2.2 Power Consumption

GSM power consumption is dependent on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used (AT or Open AT™).

All the following information is given assuming a 50 Ω RF output.

The following consumption values were obtained by performing measurements on Wireless Microprocessor samples at a temperature of 25° C.

Three VCC_3V6 values are used to measure the consumption, VCC_3V6_{MIN} (3.2V), VCC_3V6_{MAX} (4.8V) and VCC_3V6_{TYP} (3.6V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VCC_3V6 voltages.

For a more detailed description of the operating modes, see the appendix of the AT Command Interface Guide for Open AT® Firmware v7.0.

All following consumption measurement values have to be confirmed.

3.2.2.1 Power Consumption without Open AT® Processing

The following measurement results are relevant when:

- There is no Open AT® application
- The Open AT® application is disabled
- No processing is required by the Open AT® application

Operating mode	Parameters		I_{MIN} average VCC_3V6 =4.8V	I_{NOM} average VCC_3V6 =3.6V	I_{MAX} average VCC_3V6 =3.2V	I_{MAX} peak	unit
Alarm Mode			21	**16**	15		µA
Fast Idle Mode	Paging 9 (Rx burst occurrence ~2s)		15	**17**	18	160_{RX}	mA
	Paging 2 (Rx burst occurrence ~0,5s)		17	**18**	19	160_{RX}	mA
Slow Idle Mode [1]	Paging 9 (Rx burst occurrence ~2s)		1.5 **(1.5 to 1.75)**	**1.6** **(1.6 to 1.9)**	1.7 **(1.7 to 2.05)**	160_{RX}	mA
	Paging 2 (Rx burst occurrence ~0,5s)		4 **(4 to 4.3)**	**4.4** **(4.4 to 4.75)**	4.6 **(4.6 to 4.95)**	160_{RX}	mA
Fast Standby Mode			30	**36**	39		mA
Slow Standby Mode			1.4	**1.4**	1.5		mA
Connected Mode	850/900 MHz	PCL5 (TX power 33dBm)	210	**218**	222	1450_{TX}	mA
		PCL19 (TX power 6dBm)	81	**89**	92	270_{TX}	mA
	1800/1900 MHz	PCL0 (TX power 33dBm)	145	**153**	157	850_{TX}	mA
		PCL19 (TX power 6dBm)	77	**85**	88	250_{TX}	mA
Transfer Mode **class 8 (4Rx/1Tx)**	850/900 MHz	PCL3 (TX power 33dBm)	201	**209**	213	1450_{TX}	mA
		PCL17 (TX power 5dBm)	78	**85**	88	270_{TX}	mA
	1800/1900 MHz	PCL3 (TX power 30dBm)	138	**146**	149	850_{TX}	mA
		PCL18 (TX power 0dBm)	74	**81**	84	250_{TX}	mA
Transfer Mode **class 10 (3Rx/2Tx)**	850/900 MHz	PCL3 (TX power 33dBm)	364	**372**	378	1450_{TX}	mA
		PCL17 (TX power 5dBm)	112	**120**	123	270_{TX}	mA
	1800/1900 MHz	PCL3 (TX power 30dBm)	237	**245**	248	850_{TX}	mA
		PCL18 (TX power 0dBm)	104	**111**	115	250_{TX}	mA

Table 4: GSM power consumption without Open AT® processing

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst)

$_{RX}$ means that the current peak is the RF reception burst (Rx burst)

[1] **Slow Idle Mode** consumption is depends on the SIM card used. Some SIM cards respond faster than others, the longer the response time, the higher the consumption. The measurements were performed with a large number of 3V SIM cards, the results in brackets are the minimum and maximum currents measured from among all the SIMs used.

3.2.2.2 Power consumption with Open AT® software

The Open AT™ software used is the Dhrystone application, the following consumption results are measured during the run of the Dhrystone application.

Operating mode	**Parameters**		**I_{MIN} average VBATT=4,8 V**	**I_{NOM} average VBATT=3,6 V**	**I_{MAX} average VBATT=3,2 V**	**I_{MAX} peak**	**unit**
Alarm Mode			N/A	**N/A**	N/A		µA
Fast Idle Mode	Paging 9 (Rx burst occurrence ~2s)		31	**38**	41	160 RX	mA
	Paging 2 (Rx burst occurrence ~0,5s)		32	**39**	42	160 RX	mA
Slow Idle Mode	Paging 9 (Rx burst occurrence ~2s)		N/A	**N/A**	N/A	160 RX	mA
	Paging 2 (Rx burst occurrence ~0,5s)		N/A	**N/A**	N/A	160 RX	mA
Fast Standby Mode			31	**38**	41		mA
Slow Standby Mode			N/A	**N/A**	N/A		mA
Connected Mode	850/900 MHz	PCL5 (TX power 33dBm)	211	**219**	223	1450 TX	mA
		PCL19 (TX power 6dBm)	82	**90**	93	270 TX	mA
	1800/1900 MHz	PCL0 (TX power 33dBm)	146	**154**	159	850 TX	mA
		PCL19 (TX power 6dBm)	78	**85**	89	250 TX	mA
Transfer Mode **class 8 (4Rx/1Tx)**	850/900 MHz	PCL3 (TX power 33dBm)	202	**210**	214	1450 TX	mA
		PCL17 (TX power 5dBm)	78	**86**	89	270 TX	mA
	1800/1900 MHz	PCL3 (TX power 30dBm)	140	**148**	151	850 TX	mA
		PCL18 (TX power 0dBm)	75	**82**	85	250 TX	mA
Transfer Mode **class 10 (3Rx/2Tx)**	850/900 MHz	PCL3 (TX power 33dBm)	365	**373**	379	1450 TX	mA
		PCL17 (TX power 5dBm)	113	**121**	125	270 TX	mA
	1800/1900 MHz	PCL3 (TX power 30dBm)	239	**247**	250	850 TX	mA
		PCL18 (TX power 0dBm)	105	**113**	117	250 TX	mA

Table 5: Power consumption with Dhrystone Open AT® application

TX **means that the current peak is the RF transmission burst (Tx burst)**

RX **means that the current peak is the RF reception burst (Rx burst)**

3.2.2.3 Consumption Waveform Samples

The consumption waveforms are given for EGSM900 network configuration with AT software running on the internal ARM9 CPU.

The VCC_3V6 voltage is at the typical value of 3.6V.

Four significant operating mode consumption waveforms are described:

- Connected Mode (PCL5: Tx power 33dBm)
- Slow Idle mode (Paging 9)
- Fast idle mode (Paging 9)
- Transfer mode (GPRS class 10, PCL3: Tx power 33dBm)

The following waveform shows only the form of the current, for correct current values, see sections 3.2.2.1 and 3.2.2.2.

3.2.2.3.1 Connected Mode Current Waveform

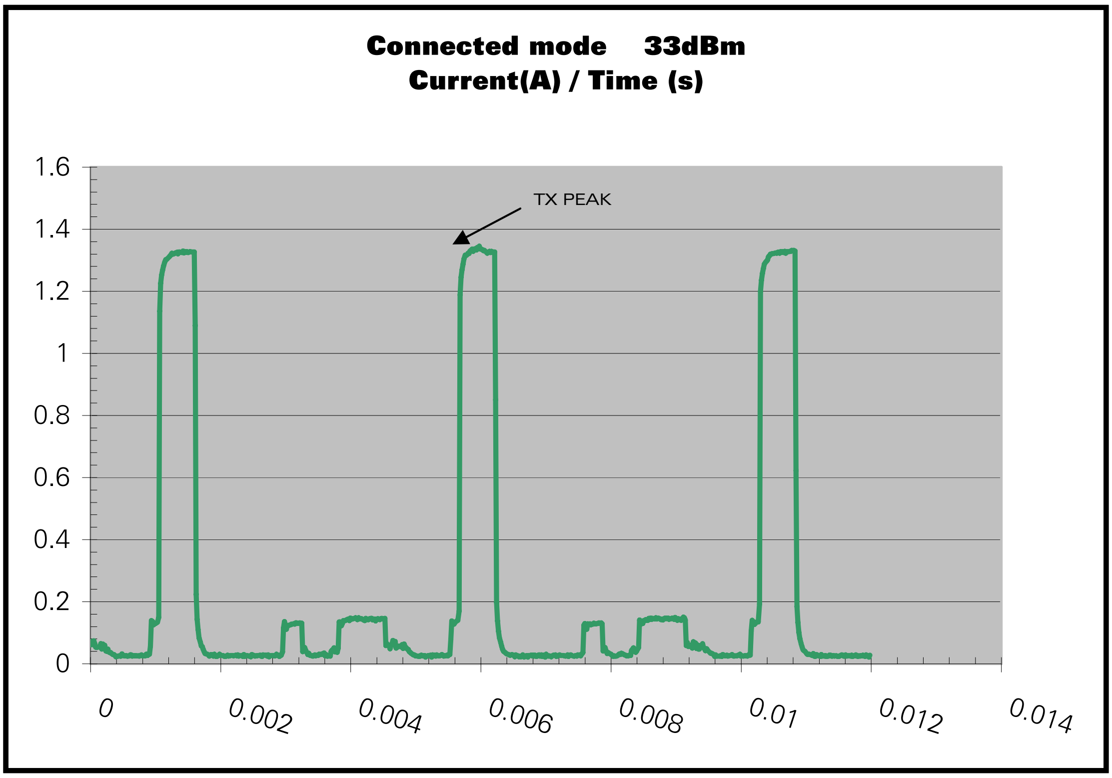


Figure 3: Connected Mode Current Waveform

3.2.2.3.2 Slow Idle Mode Current Waveform

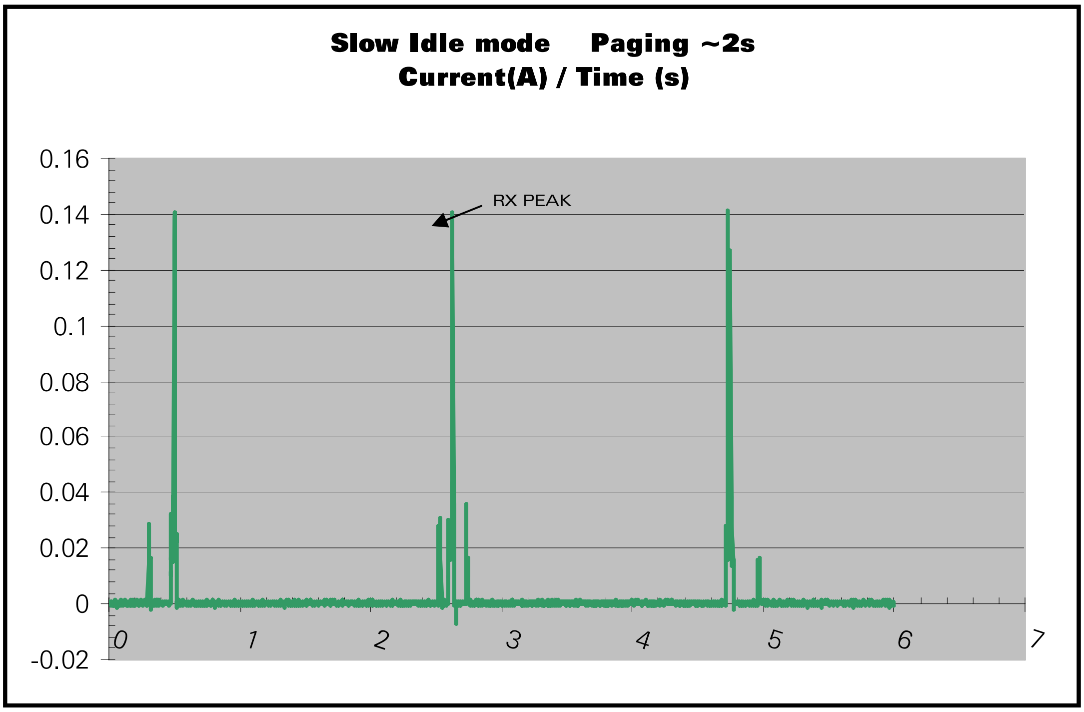


Figure 4: Slow Idle Mode Current Waveform

3.2.2.3.3 Fast Idle Mode Current Waveform

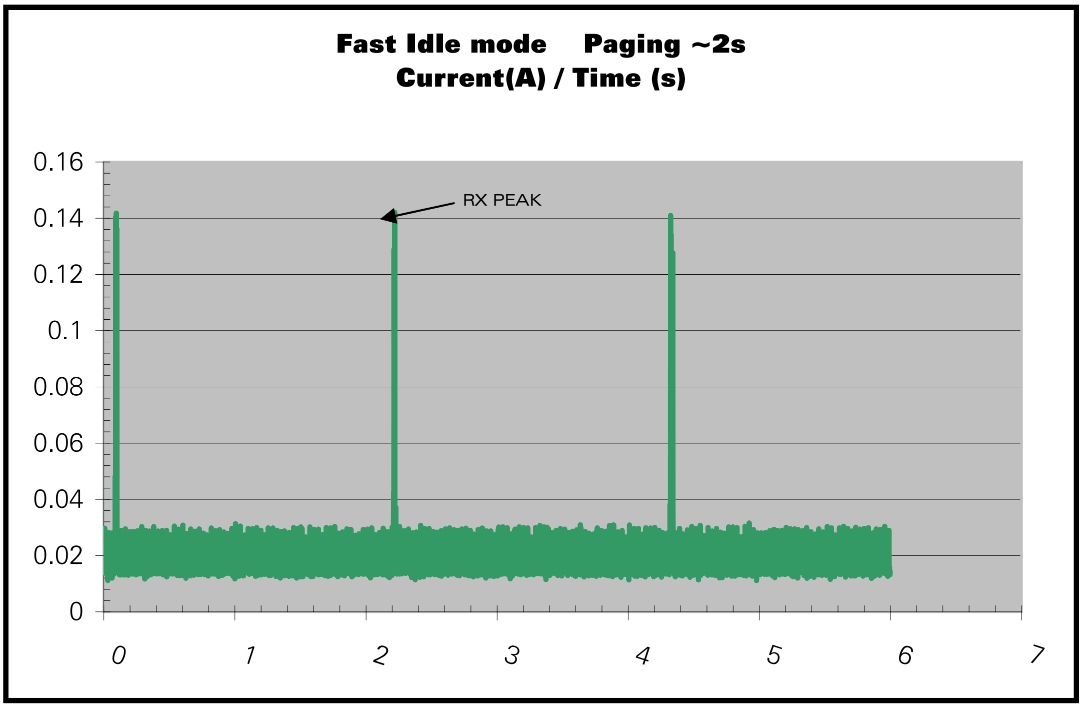


Figure 5: Fast Idle Mode Current Waveform

3.2.2.3.4 Transfer Mode Class 10 Current Waveform

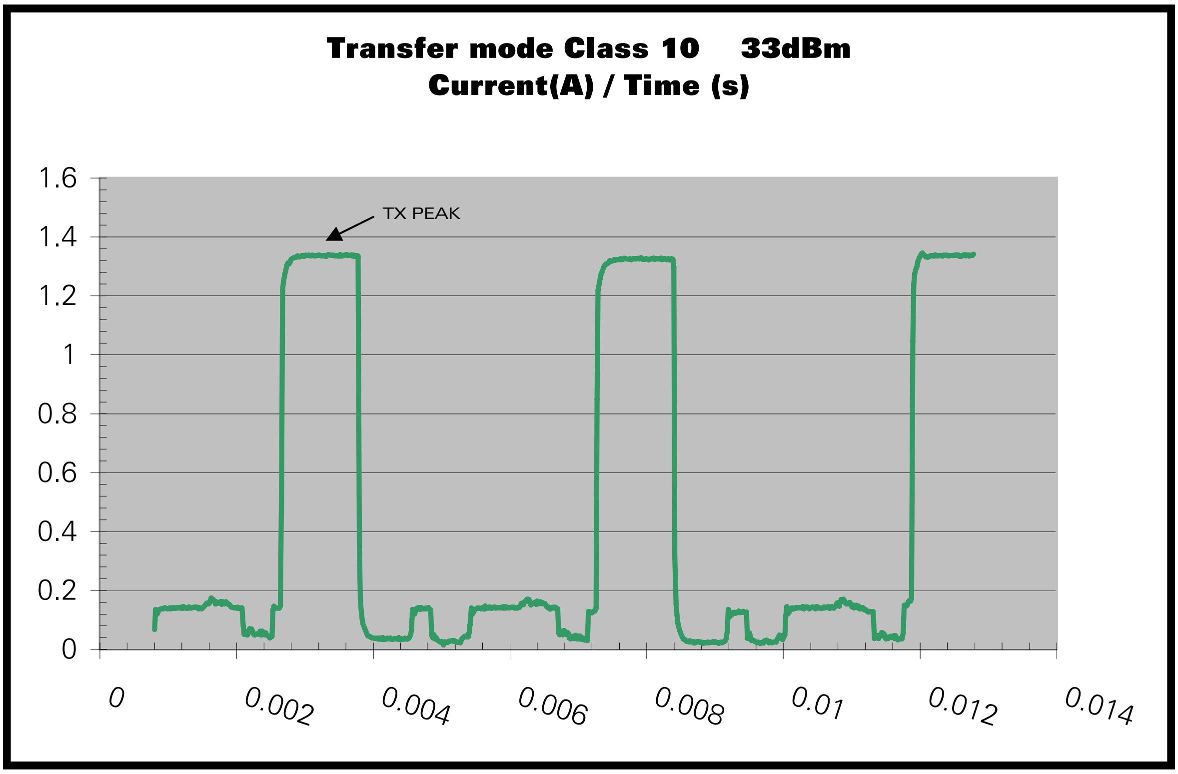


Figure 6: Transfer Mode Class 10 Current Waveform

3.2.2.4 Satellite Mode Power Consumption

The satellite portion of Q52Omni draws current from both the VCC_3V6 and VCC_12V power supply rails. In order to eliminate the GSM/GPRS radio from the values below it was placed in the Fast Standby Mode.

Operating mode	Power Supply Rail	I_{MAX}	unit
Satellite TX Mode	VCC_3V6 (nominal voltage)	250	mA
	VCC_12V (nominal voltage)	1500	mA
Satellite non TX Mode	VCC_12V (nominal voltage)	20	mA

These values in the above table are only applicable to the Satellite in TX Mode operation. The VCC_3V6 power supply rail is also used by the GSM/GPRS radio and the GPS, so there power consumption needs must also be taken into account for the power supply design.

3.2.2.5 Power Supply Pin-Out

Signal	Pin number
VCC_3V6	33,34
VCC_12V	29, 31,32
GND	5,6,8,21,22,

Table 6: Power Supply Pin-out

3.2.3 Recommendations for Less Consumption

For a better consumption, in particular for the quiescent current, it is recommended to drive the GPIOs like show in the table below.

Signal	Muxed with	I/O	I/O type	Reset state	SW driver recommended (output state)
GPIO14*	TXD2	I/O	1V8	Z	0 logic level
GPIO15*	RXD2	I/O	1V8	Z	0 logic level
GPIO16*	CTS2	I/O	1V8	Z	0 logic level
GPIO17*	RTS2	I/O	1V8	Z	0 logic level
GPIO24	HW-SD	I/O	2V8	Z	0 logic level
GPIO26	SCL	I/O	Open drain	Z	0 logic level
GPIO27	SDA	I/O	Open drain	Z	0 logic level
GPIO28	SPI1-CLK	I/O	2V8	Z	0 logic level
GPIO29	SPI1-IO	I/O	2V8	Z	0 logic level
GPIO30	SPI1-I	I/O	2V8	Z	0 logic level
GPIO31	SPI1-CS	I/O	2V8	Z	0 logic level
GPIO46	EXT-INT	I/O	2V8	Z	0 logic level

* If available

If the FLASH-LED are not necessary it is possible to disable them.

For further details refer to document [3] AT Command Interface Guide for Open AT® Firmware v7.0).

3.3 Electrical Information for Digital I/O

The CMOS signals of the Q52 OMNI shall only be considered valid when the level of the VREF_2V8 signal is above 2.4V.

Parameters for CMOS_2V8 Signals (Nominal voltage level is 2.8V)	Test Conditions	Limits		Units
		Min	Max	
High level output voltage (I_{OH} = 4mA)	V_{OH}	2.4		Volts
Low level output voltage (I_{OL} = -4mA)	V_{OL}		0.4	Volts
High level input voltage (I_{IH} = 60 µA)	V_{IH}	1.96	3.2*	Volts
Low level input voltage (I_{IL} = 60 µA)	V_{IL}	-0.5*	0.84	Volts

Table 7: CMOS Output / Input Electrical Characteristics for 2.8 volt signals

Parameters for CMOS_1V8 Signals (Nominal voltage level is 1.8V)	Test Conditions	Limits		Units
		Min	Max	
High level output voltage (I_{OH}= 4mA)	V_{OH}	1.4		Volts
Low level output voltage (I_{OL} = -4mA)	V_{OL}		0.4	Volts
High level input voltage (I_{IH} = 60 µA)	V_{IH}	1.33	2.2*	Volts
Low level input voltage (I_{IL} = 60 µA)	V_{IL}	-0.5*	0.54	Volts

Table 8: CMOS Output / Input Electrical Characteristics for 1.8 volt signals

Parameters for Open Drain Signals	Parameter	Limits	
		Min	Max
FLASH-LED	V_{OH}		0.4V
	I_{OL}		8mA
BUZZ_OUT	V_{OL}		0.4V
	I_{OL}		100mA
SDA/GPIO27 and SCL/GPIO26	$V_{TOLERATED}$		3.3V
	V_{IH}	2.0V	
	V_{IL}		0.8V
	V_{OL}		0.4V
	I_{OL}		3mA

Table 9: Open Drain Electrical Characteristics

* Absolute Maximum Ratings

3.4 Serial Interface

3.4.1 SPI Bus

The SPI bus interface includes:

- A Clock signal
- A SPI Data output or SPI Data Input/Output signal depending on whether 4 or 3 wires SPI interface is selected
- A SPI Data Input signal for applications using 4 wires interface
- A SPI Chip Select signal

SPI bus characteristics:

- Master mode operation
- SPI speed is from 101.5 Kbit/s to 13 Mbit/s in master mode operation
- 3 or 4-wire interface
- SPI-mode configuration: 0 to 3
- 1 to 16 bits data length

3.4.1.1 SPI Waveforms

Waveform for SPI transfer with 4-wire configuration in master mode 0 (slave select signal is not represented).

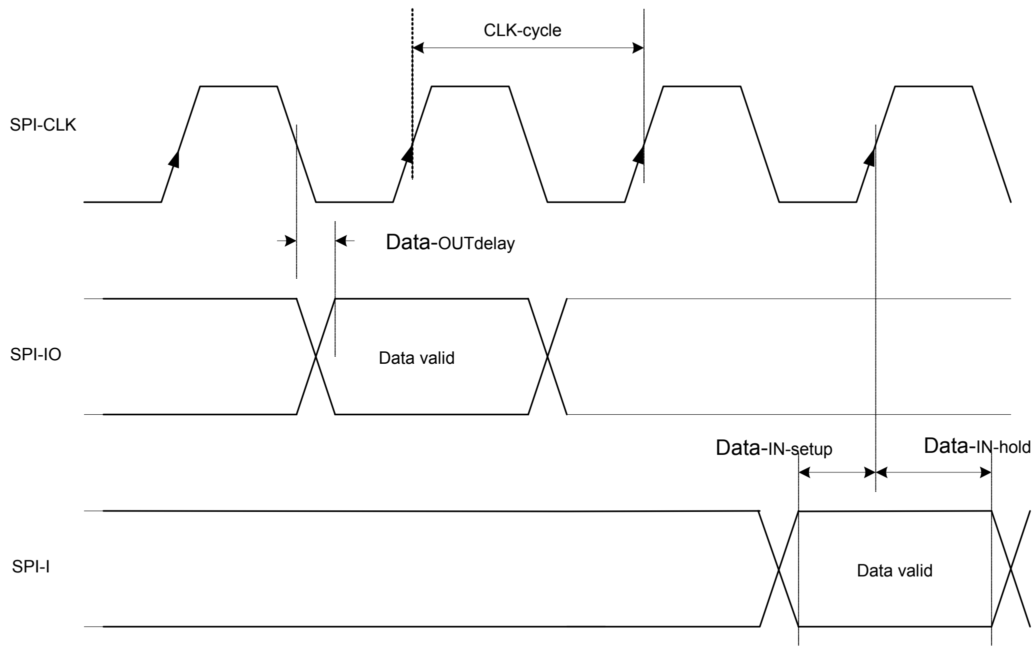


Figure 7: SPI Timing diagrams, Mode 0, Master, 4 wires

Signal	Description	Minimum	Typ	Maximum	Unit
CLK-cycle	**SPI clock frequency**	0.1015		13	MHz
Data-OUT delay	**Data out ready delay time**			10	ns
Data-IN-setup	**Data in setup time**	2			ns
Data-OUT-hold	**Data out hold time**	2			ns

Table 10: SPI Bus AC characteristics

3.4.1.2 SPI Configuration

For a 4-wire SPI interface; SPI-IO is used as output only of data from the master and SPI-I is used as input only.

For a three wire SPI interface; SPI-IO is used for both input and output of data to/from the master.

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire type	4-wire type
Master	13 Mb/s	0,1,2,3	Half	SPI-CLK SPI-IO SPI-CS	SPI-CLK SPI-I SPI-IO SPI-CS

Table 11: SPI Bus Configuration

3.4.1.3 SPI Bus Pin Description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI1-CLK	15	O	2V8	Z	SPI Serial Clock	GPIO28
SPI1-IO	14	I/O	2V8	Z	SPI Serial input/output	GPIO29
SPI1-I	13	I	2V8	Z	SPI Serial input	GPIO30
SPI1-CS	16	O	2V8	Z	SPI Slave Enable	GPIO31

Table 12: SPI Bus Pin description

See Chapter 3.2.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

3.4.2 I2C Bus

3.4.2.1 Features

The I2C interface includes a clock signal (SCL) and data signal (SDA) complying with a 100Kbit/s-standard interface (standard mode: s-mode).

3.4.2.2 Characteristics

The I²C bus is always master.

The maximum speed transfer range is 400Kbit/s (fast mode: f-mode).

For more information on the bus, see the [4]"I²C Bus Specification", Version 2.0, Philips Semiconductor 1998

3.4.2.3 I²C Waveforms

I²C bus waveform in master mode configuration:

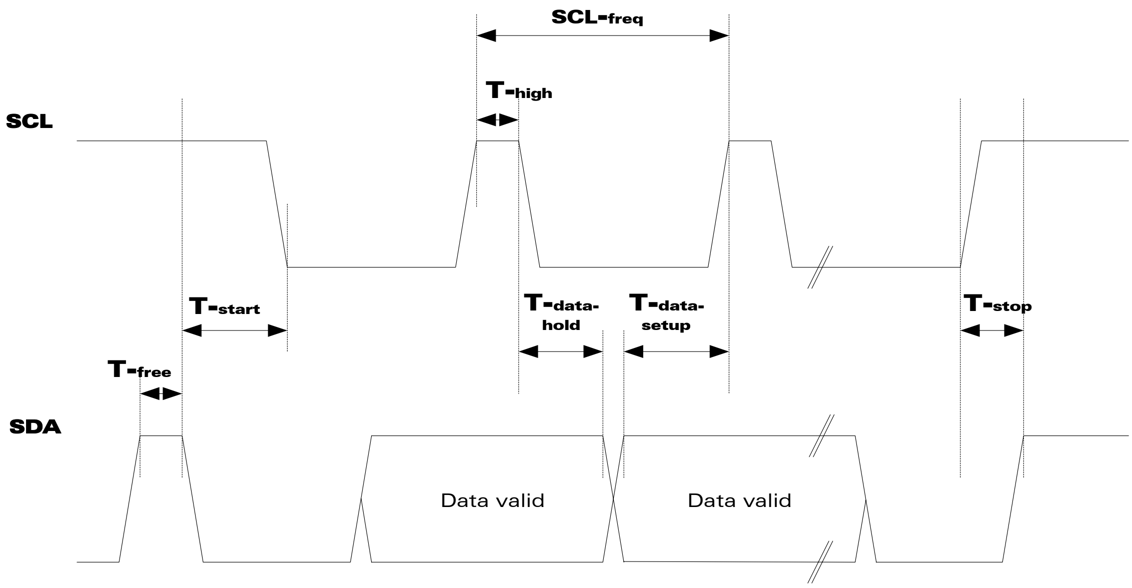


Figure 8: I²C Timing diagrams, Master

Signal	Description	Minimum	Typ	Maximum	Unit
SCL-freq	I²C clock frequency	100		400	KHz
T-start	Hold time START condition	0.6			µs
T-stop	Setup time STOP condition	0.6			µs
T-free	Bus free time, STOP to START	1.3			µs
T-high	High period for clock	0.6			µs
T-data-hold	Data hold time	0		0.9	µs
T-data-setup	Data setup time	100			ns

Table 13: I²C Bus AC characteristics

3.4.2.4 I²C Bus Pin-Out

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SCL	36	O	Open drain	Z	Serial Clock	GPIO26
SDA	35	I/O	Open drain	Z	Serial Data	GPIO27

Table 14: IC Bus Pin Description

See Chapter 3.2.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

3.5 Main Serial Link (UART1)

The UART interface functions as a DCE serial device. A flexible 7-wire serial interface is available, complying with V24 protocol signaling but not with V28 (electrical interface) due to a 2.8-Volt interface.

The signals are as follows:

3.5.1 Features

The maximum baud rate of the UART1 is 921 Kbit/s.

The signals are the follows:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (~CT105/RTS)
- Clear To Send (~CT106/CTS)
- Data Terminal Ready (~CT108-2/DTR)

- Data Carrier Detect (~CT109/DCD)
- Ring Indicator (~CT125/RI).

3.5.2 Pin Description of UART1 Interface

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
CT103/TXD1*	27	I	2V8	Z	Transmit serial data	GPIO36
CT104/RXD1*	30	O	2V8	1	Receive serial data	GPIO37
~CT105/RTS1*	28	I	2V8	Z	Request To Send	GPIO38
~CT106/CTS1*	25	O	2V8	Z	Clear To Send	GPIO39
~CT108-2/DTR1*	26	I	2V8	Z	Data Terminal Ready	GPIO41
~CT109/DCD1*	23	O	2V8	Undefined	Data Carrier Detect	GPIO43
~CT125/RI1*	24	O	2V8	Undefined	Ring Indicator	GPIO42
CT102/GND*	Chassis GND		GND		Ground	

Table 15: UART1 Pin Description

* According to PC view

See Wireless Microprocessor® WMP100 Technical Specification for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

The **rise** and **fall time** of the reception signals (mainly TXD_UART1) must be less than **300 ns**.

The Q52 Omni is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

<u>For the use case with 5-wire serial interface</u>

- Signal: CT103/TXD1*, CT104/RXD1*, ~CT105/RTS1*, ~CT106/CTS1*
- The signal ~CT108-2/DTR1* must be managed following the V24 protocol signalling if we want to use the slow idle mode
- The other signals and their multiplexed are not available
- Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0 for more information.

For the use case with 4-wire serial interface

- CT103/TXD1*, CT104/RXD1*, ~CT105/RTS1*, ~CT106/CTS1*
- The signal ~CT108-2/DTR1* must be configured at the low level
- The other signals and their multiplexed are not available
- Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0 for more information.

For the use case with 2-wire serial interface

- This case is possible for connected external chip but not recommended (and forbidden for AT command or modem use)
- The external chip must be a flow control
- CT103/TXD1*, CT104/RXD1*
- The signal ~CT108-2/DTR1* must be configured at the low level
- The signals ~CT105/RTS1*, ~CT106/CTS1* are not used, please configure the AT command (AT+IFC=0,0 see document [3] AT Command Interface Guide for Open AT® Firmware v7.0).
- The signal ~CT105/RTS1* must be configured at the low level
- The other signals and their multiplexed are not available
- Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0 for more information.

V24/CMOS possible design:

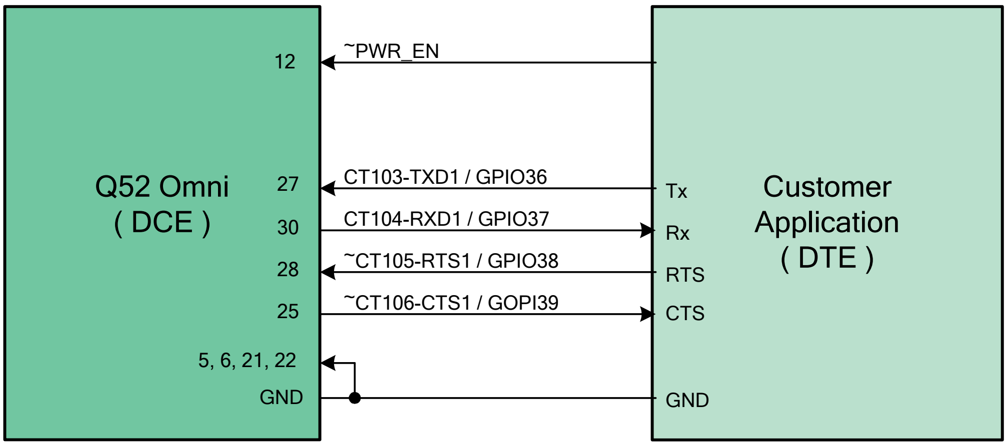


Figure 9: Example of V24/CMOS serial link implementation for UART1

The design shown in the above figure is a basic design.

However, a more flexible design to access this serial link with all modem signals is shown below

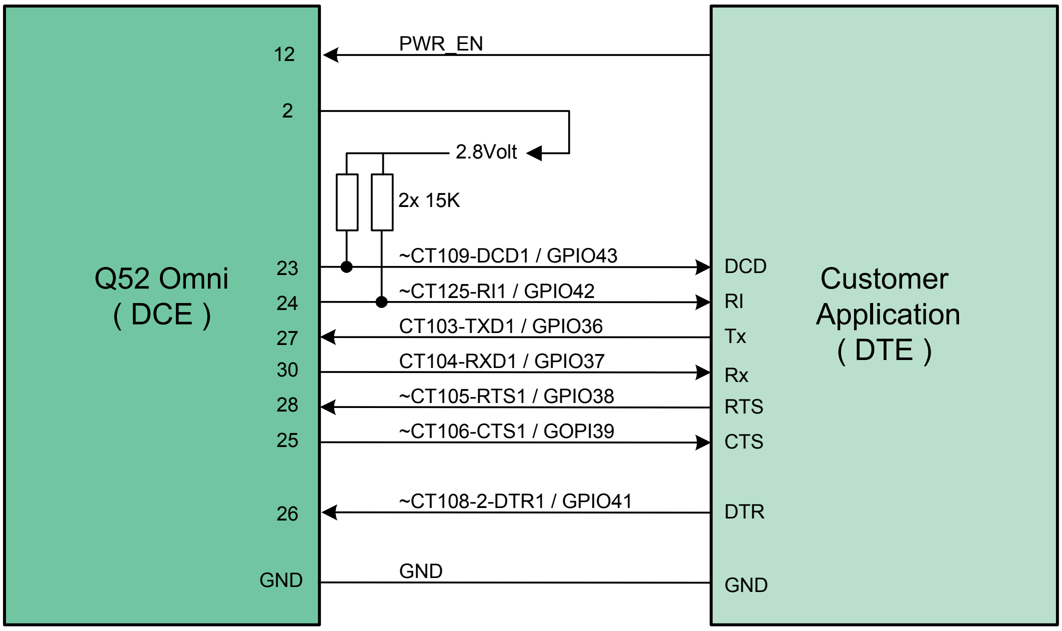


Figure 10: Example of full modem V24/CMOS serial link implementation for UART1

It is recommended to add a 15K-ohm pull-up resistor on ~CT125-RI1 and ~CT109-DCD1 to set high level during reset state.

The UART1 interface is 2.8 Volt type, but is 3 Volt tolerant.

The Q52 Omni UART1 is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

Warning: If you want to activate Power Down mode (Wavecom 32K mode) in your Open AT® application, you need to wire the DTR pin to a GPIO. Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0 (see the "Appendixes") for more information on Wavecom 32K mode activation using the Open AT® Software Suite.

3.6 Auxiliary Serial Link (UART2)

3.6.1 Features

The maximum baud rate of UART2 is **921** kbit/s.

For peripheral connectivity an auxiliary serial interface (UART2) is available on the system connector only on series without GPS functionality. On Q52 Omni series with GPS functionality GPIO16 and GPIO17 are available.

The signals are the follows:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (~CT105/RTS)
- Clear To Send (~CT106/CTS)

The Q52 Omni is designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

<u>For the use case with 2-wire serial interface</u>

- This case is possible for connected external chip but not recommended (and forbidden for AT command or modem use)
- The external chip must be a flow control
- CT103/TXD2*, CT104/RXD2*
- The signals ~CT105/RTS2*, ~CT106/CTS2* are not used, please configure the AT command (AT+IFC=0,0. Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0.
- The signal ~CT105/RTS2* must be configured at the low level
- The other signal and their multiplexed are not available
- Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0 (see the “Appendixes”).

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
TXD2	37	I	1V8	Z	Transmit serial data	GPIO14
RXD2	39	O	1V8	Z	Receive serial data	GPIO15
CTS2	38	O	1V8	Z	Clear To Send	GPIO16
RTS2	40	I	1V8	Z	Request To Send	GPIO17

Table 16: UART2 Pin Description

See Chapter 3.2.3, “Electrical information for digital I/O” for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

3.7 General Purpose Input/Output

The Q52 Omni provides up to 18 General Purpose I/Os. These pins are multiplexed with other IO functions, so the number of pins programmed as GPIOs will depend on the functionality required for a specific application

Signal	Pin number	I/O	I/O type*	Reset state	Multiplexed with
GPIO14/INT6	37	I/O	1V8**	Z	TXD2
GPIO15	39	I/O	1V8**	Z	RXD2
GPIO16	38	I/O	1V8	Z	CTS2
GPIO17/INT17	40	I/O	1V8	Z	RTS2
GPIO3/A26	49	I/O	2V8	Z	INT0
GPIO26	44	I/O	Open drain	Z	SCL
GPIO27	46	I/O	Open drain	Z	SDA
GPIO28	23	I/O	2V8	Z	SPI1-CLK
GPIO29	25	I/O	2V8	Z	SPI1-IO
GPIO30	30	I/O	2V8	Z	SPI1-I
GPIO31	31	I/O	2V8	Z	SPI1-CS
GPIO36	71	I/O	2V8	Z	TXD1
GPIO37	73	I/O	2V8	1	RXD1
GPIO38	72	I/O	2V8	Z	RTS1
GPIO39	75	I/O	2V8	Z	CTS1
GPIO41	76	I/O	2V8	Z	DTR1
GPIO42	69	I/O	2V8	Undefined	RI1
GPIO43	70	O	2V8	Undefined	DCD1

Table 17: GPIOs Pin Description

See Chapter 3.2.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

** If GPS functionality is available on Q52 Omni, these GPIOs are not available.

3.8 Analog to Digital Converters

3.8.1 Features

Two Analog to Digital Converter inputs are provided by the Q52 Omni. The converters are 10-bit resolution, ranging from 0 to 2V.

Parameter		Min	Typ	Max	Unit
Resolution			10		bits
Sampling rate			216		S/s
Integral Accuracy			15		mV
Differential Accuracy			2.5		mV
Input signal range		0		2	V
Input impedance	**ADC0**		1M		Ω
	ADC1		1M		Ω

Table 18: ADCs Electrical Characteristics

3.8.2 Pins Description

Signal	Pin number	I/O	I/O type	Description
ADC0	18	I	Analog	A/D converter
ADC1	19	I	Analog	A/D converter

Table 19: ADCs Pin Description

3.9 Digital to Analog Converter

One Digital to Analog Converter (DAC) input is provided by the Q52 Omni.

3.9.1 Features

The converter is 8-bit resolution, guaranteed monotonic with a range from 0V to 2.3V.

This output assumes a typical external load of 2kΩ and 50pF in parallel to GND.

Parameter	Min	Typ	Max	Unit
Resolution	-	8	-	bits
Maximum Output voltage	2.1	2.2	2.3	V
Minimum Output voltage	0	-	40	mV
Output voltage after reset	-	1.147	-	V
Integral Accuracy	-5	-	+5	LSB
Differential Accuracy	-1	-	+1	LSB
Full scale settling time (load: 50pF // 2kΩ to GND)	-	40	-	µs
One LSB settling time (load: 50pF // 2kΩ to GND)	-	8	-	µs

Table 20: DAC Electrical Characteristics

3.9.2 Pin Description

Signal	Pin number	I/O	I/O type	Description
AUX-DAC0	11	O	Analog	D/A converter

Table 21: DAC Pin Description

3.10 Analog Audio Interface

The Q52 OMNI provides a single ended microphone input and single ended speaker output for GSM audio I/O. An echo cancellation feature allows hands free functionality in GSM voice mode.

3.10.1 Microphone Input

3.10.1.1 Features

The MIC input includes the biasing for an electret microphone, thus allowing easy connection. The gain of the MIC input is internally adjusted and may be tuned using an AT command. AC coupling is already embedded in the Q52 Omni.

When you design the audio analog interface be sure to have a very good ground plane, a very good filtering as well as shielding in order to avoid any disturbance on the audio path.

Signal	Pin number	I/O	I/O type	Description
MIC2	10	I	Analog	Microphone input

Table 22: MIC2 Pin Description

3.10.1.2 Electrical Characteristics

Parameter		Min.	Typ	Max.	Unit
Internal Biasing	Voltage	2	2.1	2.2	V
	Output Current		0.5	1.5	mA
Impedance single-ended	Internal AC coupling		100		nF
	MIC to AGND	0.9	1.1	1.4	kΩ
Input voltage*	Positive*			7.35	V
	Negative	-0.9			V

Table 23: MIC2 Electrical Characteristics

- * The input voltage depends on the input microphone gain set by AT command.
- ** Because MIC2 is internally biased, a coupling capacitor must be used to connect an audio signal provided by an active generator. Only a passive microphone may be directly connected to the MIC2 input.

3.10.1.3 Application Example

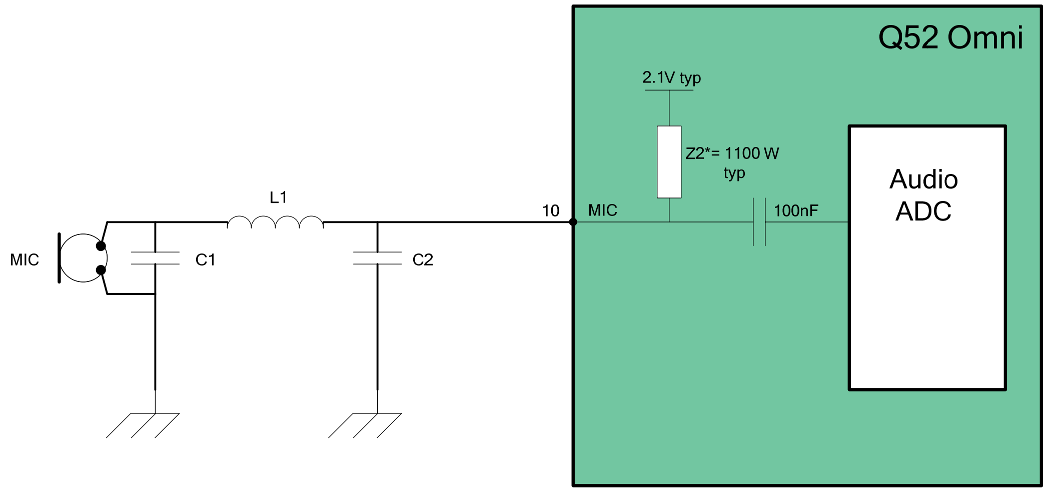


Figure 11: Example of MIC input connection with LC filter

*:Z2 is from 200Hz to 4kHz. For more characteristics refer to the chapter 3.14.1.1.2.

Internal input impedance value becomes 1100 ohms.

It is recommended to add L1 and C2 footprint to add a LC filter to try to eliminate the TDMA noise.

When not used, the filter can be removed by replacing L1 by a 0 Ohm resistor and by disconnecting C2, as the following schematic.

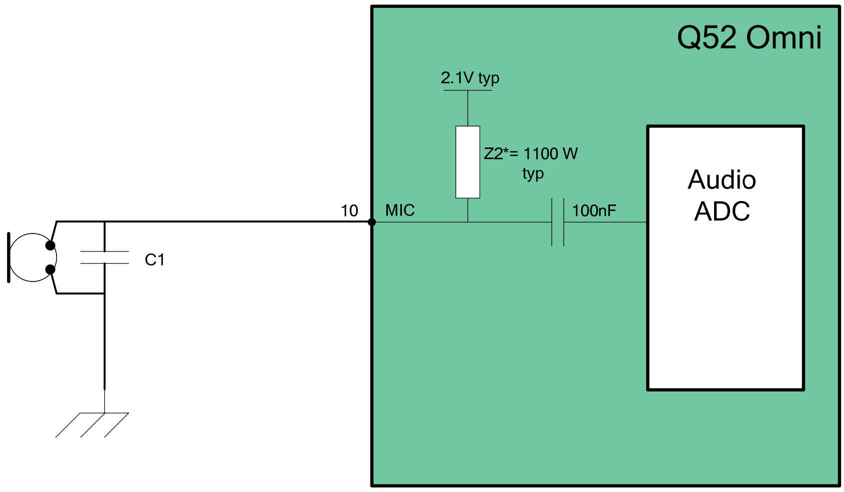


Figure 12: Example of MIC input connection without LC filter

***:Z2 is from 200Hz to 4kHz. For more characteristics refer to the chapter 3.14.1.1.2.**

The capacitor C1 is highly recommended to eliminate the TDMA noise. C1 must be close to the microphone.

Recommended components:

- C1: 12pF to 33pF (depending of the design ,needs to be tuned)
- C2: Must be tuned depending of the design.
- L1: Must be tuned depending of the design.

3.10.2 Speaker Output Characteristics

3.10.2.1 Features

The connection is single-ended on SPK. Be sure to have a good ground plane, good filtering and adequate shielding in order to avoid any disturbance on the audio path.

Signal	Pin number	I/O	I/O type	Description
SPK2	7	O	Analog	Speaker Output

Table 24: SPK Pin Description

3.10.2.2 Electrical Characteristics

Parameters		Min	Typ	Max	Unit
Biasing voltage	SPK2		1.30		V
Output swing voltage	RL=8Ω: AT+VGR=6*	-	-	2	Vpp
	RL=32Ω: AT+VGR=6*	-	-	2.5	Vpp
RL	Load resistance	6	8	-	Ω
IOUT	Output current; peak value; RL=8Ω	-	-	90	mA
POUT	RL=8Ω; AT+VGR=6*;	-	-	125	mW
RPD	Output pull-down resistance at power-down	28	40	52	KΩ
VPD	Output DC voltage at power-down	-	-	100	mV

Table 25: SPK Electrical Characteristics

*The output voltage depends of the output speaker gain set by AT command. Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.0.

3.10.2.3 Application Example

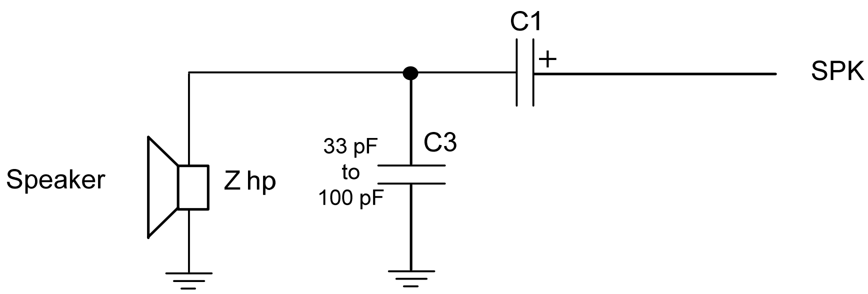


Figure 13: Example of Speaker connection

4.7 µF < C1 < 47 µF (depending on speaker characteristics and output power).

The connection between the Q52 Omni pin and the speaker must be designed to keep the serial impedance lower than 1.5 Ω in single ended mode.

3.10.3 Design Recommendation

3.10.3.1 General

When speakers and microphones are exposed to the external environment, it is recommended to add ESD protection as closed as possible to the speaker or microphone, connected between the audio lines and a good ground.

You ensure to have a good ground plane, a good filtering as well as shielding, in order to avoid any disturbance on the audio path.

It is important to select an appropriate microphone, speaker and filtering components to avoid TDMA noise

3.10.3.2 Recommended Microphone Characteristics

- The impedance of the microphone has to be around 2 kΩ.
- Sensitivity from -40dB to –50 dB.
- SNR > 50 dB.
- Frequency response compatible with the GSM specifications.

To suppress TDMA noise, it is highly recommended to use microphones with two internal decoupling capacitors:

-CM1=56pF (0402 package) for the TDMA noise coming from the demodulation of the GSM 850 and GSM900 frequency signal.

-CM2=15pF (0402 package) for the TDMA noise coming from the demodulation of the DCS/PCS frequency signal.

The capacitors have to be soldered in parallel of the microphone

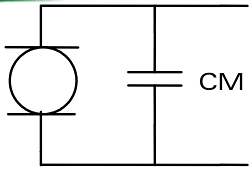


Figure 14: Capacitor near Microphone

3.10.3.3 Recommended Speaker Characteristics

- Type of speakers: Electro-magnetic /10mW
- Impedance: 8Ω for hands-free (SPK2)
- Sensitivity: 110dB SPL min
- Receiver frequency response compatible with the GSM specifications.

3.10.3.4 Recommended Filtering Components

When designing a GSM application, it is important to select the right audio filtering components.

The strongest noise, called TDMA, is mainly due to the demodulation of the GSM850/GSM900/DCS1800 and PCS1900 signal: A burst being produced every 4.615ms; the frequency of the TDMA signal is equal to 216.7Hz plus harmonics.

The TDMA noise can be suppress by filtering the RF signal using the right decoupling components.

The types of filtering components are:

-RF decoupling inductors

-RF decoupling capacitors

A good "Chip S-Parameter" simulator is proposed by Murata, the following link help to find it:

http://www.murata.com/designlib/mcsil.html

Using different Murata components, we could see that the value, the package and the current rating can have different decoupling effects.

The table below shows some examples with different Murata components:

Package	0402		
Filtered band	GSM900	GSM 850/900	DCS/PCS
Value	100nH	56pF	15pF
Types	Inductor	Capacitor	Capacitor
Position	Serial	Shunt	Shunt
Manufacturer	Murata	Murata	Murata
Rated	150mA	50V	50V
Reference	LQG15HSR10J02 or LQG15HNR10J02	GRM1555C1H560JZ01	GRM1555C1H150JZ01 or GRM1555C1H150JB01
Package	**0603**		
Filtered band	GSM900	GSM 850/900	DCS/PCS
Value	100nH	47pF	10pF
Types	Inductor	Capacitor	Capacitor
Position	Serial	Shunt	Shunt
Manufacturer	Murata	Murata	Murata
Rated	300mA	50V	50V
Reference	LQG18HNR10J00	GRM1885C1H470JA01 or GRM1885C1H470JB01	GRM1885C1H150JA01 or GQM1885C1H150JB01

Table 26: Audio filtering Examples with Murata Components

3.10.3.5 Audio Track and PCB Layout Recommendation

To avoid TDMA noise, it is recommended to surround the audio tracks by ground:

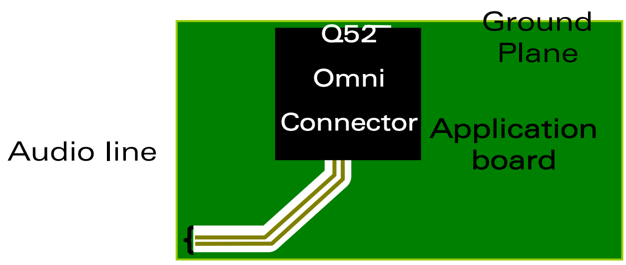


Figure 15: Audio track design

Note: Avoid digital tracks crossing under and over the audio tracks.

3.10.4 Buzzer Output

3.10.4.1 Features

This output is controlled by a PWM controller and can be used as buzzer or as PWM.

BUZZ-OUT is an open drain output. A buzzer can be directly connected between this output and VCC_MAIN. The maximum current is 100 mA (PEAK).

Parameter	Condition	Minimum	Maximum	Unit
$V_{OL\ on}$	Iol = 100mA		0.4	V
I_{PEAK}	VCC_MAIN (max)		100	mA
Frequency		TBD	TBD	Hz
Duty Cycle		TBD	TBD	

Table 27: PWM/Buzzer Output Electrical Characteristics

3.10.4.2 Pinout

Signal	Pin number	I/O	I/O type	Reset state	Description
BUZZ-OUT	1	O	Open drain	Z	PWM/Buzzer output

Table 28: PWM/Buzzer Output Pin Description

See Chapter 3.2.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

3.10.4.3 Application Example

The maximum peak current is 100 mA and the maximum average current is 40 mA. A diode against transient peak voltage must be added as described below.

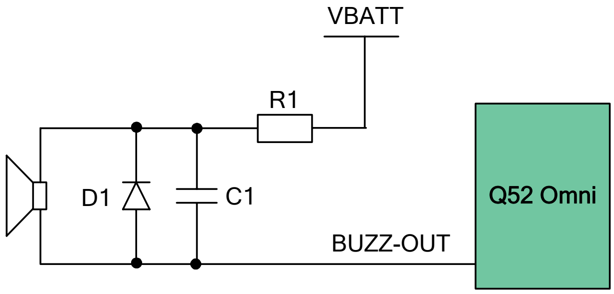


Figure 16: Example of buzzer implementation

Where:

- R1 must be chosen in order to limit the current at I_{PEAK} max
- C1 = 0 to 100 nF (depending on the buzzer type)
- D1 = BAS16 (for example)

<u>Recommended characteristics for the buzzer:</u>

- electro-magnetic type
- Impedance: 7 to 30 Ω
- Sensitivity: 90 dB SPL min @ 10 cm
- Current: 60 to 90 mA

The BUZZ-OUT output can also be used to drive a LED as shown in the Figure below:

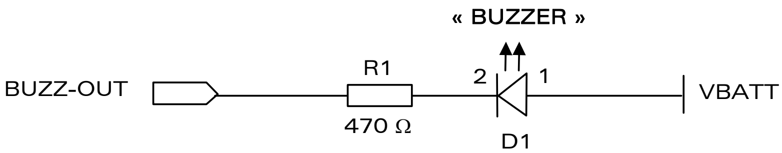


Figure 17: Example of LED driven by the BUZZ-OUT output

R1 value can be accorded depending of the LED (D1) characteristics.

3.11 ~ON / OFF Signal

This input is used to switch ON or OFF the Wireless Microprocessor.

A low level signal has to be provided on the pin ON/~OFF to switch ON the Wireless Microprocessor.. The voltage of this signal has to be maintained at 0.2 x VBATT during a minimum of 1500ms. This signal can be left at low level until switch off.

To switch OFF the Q52 OMNI the pin ~ON/OFF has to be released. The Wireless Microprocessor can be switched off through the Operating System.

☞ **Warning:**

All external signals must be inactive when the Wireless Microprocessor is OFF to avoid any damage when starting and allow Wireless Microprocessor to start and stop correctly.

3.11.1 Features

Electrical Characteristics of the signal

Parameter	I/O type	Minimum	Maximum	Unit
V_{IL}	CMOS		VBATT x 0.2	V
V_{IH}	CMOS	VBATT x 0.8	VBATT	V

3.11.2 Pin Description

Signal	Pin number	I/O	I/O type	Description
~ON/OFF	U5	I	CMOS	Q52 Omni Power ON

3.11.3 Application

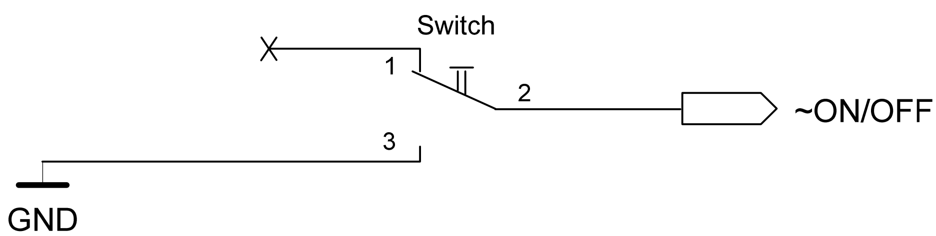


Figure 18 : Example of ON/~OFF pin connection

3.11.3.1 Power ON

Once Q52 Omni/Open AT® Software Suite v2.0 is powered, the application must set the ON/OFF signal to low to start the Q52 Omni/Open AT® Software Suite v2.0 power ON sequence. The ~ON/OFF signal must be held low during a minimum delay of $T_{on/off-hold}$ (Minimum hold delay on the ~ON/OFF signal) to power-ON. After this delay, an internal mechanism maintains the Q52 OMNI /Open AT® Software Suite v2.0 in power ON condition.

During the power ON sequence, an internal reset is automatically performed by the Q52 OMNI /Open AT® Software Suite v2.0 for 40ms (typically). During this phase, any external reset should be avoided during this phase.

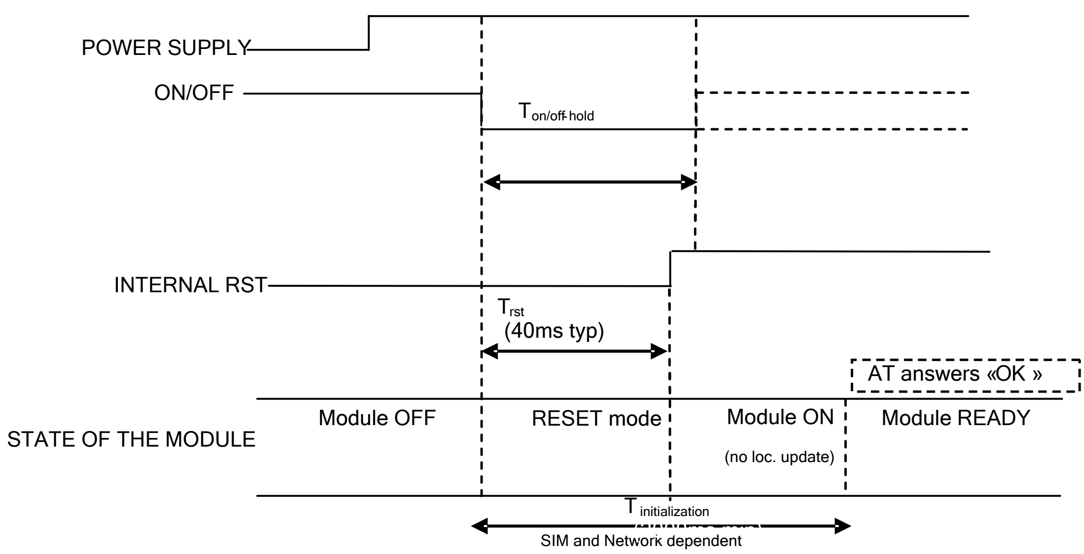


Figure 19 : Power-ON sequence (no PIN code activated)

The duration of the firmware power-up sequence depends on:

- The need to perform a recovery sequence if the power has been lost during a flash memory modification.

Other factors have a minor influence

- the number of parameters stored in EEPROM by the AT commands received so far
- the ageing of the hardware components, especially the flash memory
- the temperature conditions

The *recommended* way to de-assert the ~ON/OFF signal is to use either an AT command or WIND indicators: the application has to detect the end of the power-up initialization and de-assert ~ON/OFF afterwards.

- Send an "AT" command and wait for the "OK" answer: once the initialization is complete the AT interface answers « OK » to "AT" message*.
- Wait for the "+WIND: 3" message: after initialization, the Q52 OMNI /Open AT® Software Suite v2.0, if configured to do so, will return an unsolicited "+WIND: 3" message. The generation of this message is enabled or disabled via an AT command.

Note:

- Please refer to the document [3] AT Command Interface Guide for Open AT® Firmware v7.00 for more information on these commands.

Proceeding thus – by software detection - will always prevent the application from de-asserting the ~ON/OFF signal too early.

If WIND indicators are disabled or AT commands unavailable or not used, it is still possible to de-assert ~ON/OFF after a delay long enough ($T_{on/off-hold}$) to ensure that the firmware has already completed its power-up initialization.

The table below gives the minimum values of $T_{on/off-hold}$:

$T_{initialization}$ minimum values

Open AT® Firmware	$T_{initialization}$ Safe evaluations of the firmware power-up time
6.65 & above	8 s

The above figure take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But they are safe because they are large enough to ensure that ~ON/OFF is not de-asserted too early.

Additional notes:

* If the application manages hardware flow control, the AT command can be sent during the initialisation phase.

1. Typical power-up initialization time figures for best cases conditions (no power-loss recovery, fast and new flash memory...) approximate 3.5 seconds in every firmware version. But releasing ~ON/OFF after this delay does not guarantee that the application will actually start-up if for example the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command...
2. The ~ON/OFF signal can be left at a low level until switch OFF. But this is not recommended as it will prevent the AT+CPOF command from performing a clean power-off. (See also the note in the Power OFF chapter for an alternate usage.)
3. When using a battery as power source, it is not recommended to let this signal high:

   If the battery voltage is too low and the ~ON/OFF signal at high level, an internal mechanism switches OFF the Q52 OMNI /Open AT® Software Suite v1.0. This automatic process prevents the battery to be over discharged and optimize its life span.
4. During the power-ON sequence, an internal reset is automatically performed by the Q52 OMNI /Open AT® Software Suite v2.0 for 40 ms (typically). Any external reset should be avoided during this phase.
5. After a reset (hardware or software), if the ~ON/OFF signal is OFF (High level) the Q52 OMNI switches OFF.

3.11.3.2 Power OFF

To properly power OFF the Q52 OMNI/Open AT® Software Suite v2.0 the application must set the ~ON/OFF signal and then send the AT+CPOF command to deregister from the network and switch off the Q52 OMNI /Open AT® Software Suite v2.0.

Once the « OK » response is issued by the Q52 OMNI /Open AT® Software Suite v2.0, the power supply can be switched off.

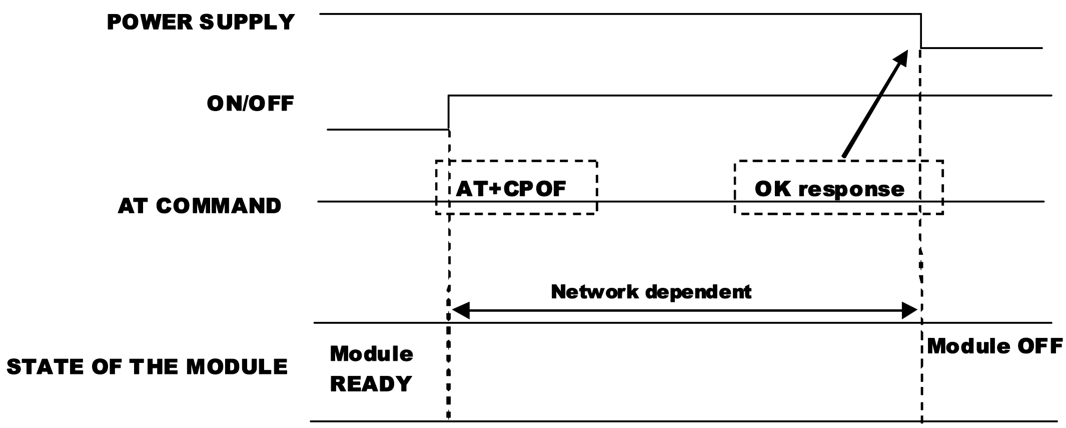


Figure 20 : Power-OFF sequence

Note:

- If the ~ON/OFF pin is maintained to ON (Low Level) then the module can't be switched OFF.

3.12 External Interrupt

The Q52 OMNI provides one external interrupt input. The interrupt input can be activated on:

- High to low edge
- Low to high edge
- Low to high and high to low edge
- Low level
- High level

When used, the interrupt input must not be left open.

If not used, it must be configured as a GPIO.

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
INT1	17	I	2V8	Z	External Interrupt	GPIO3

Table 29: External Interrupt Pin description

See Chapter 3.2.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

Parameter		Minimum	Maximum	Unit
INT1	V_{IL}		0.84	V
	V_{IH}	1.96		V

Table 30: External Interrupt Electrical Characteristics

3.13 BOOT Signal

A specific control signal BOOT is available to download the Q52 Omni only if the standard XMODEM download, controlled with AT command, is not possible.

Specific PC software, provided by WAVECOM, is needed to perform this download, specifically for the first download of the Flash memory.

3.13.1 Features

The BOOT signal is muxed with DCD1 pin.

The BOOT signal must be connected to the VCC_1V8 for this specific download.

BOOT	Operating mode	Comment
Leave open	Normal use DCD function	No download
Leave open	Download XMODEM DCD function	AT command for Download AT+WDWL
1	Download specific	Need WAVECOM PC software

Table 31: Boot Signal Mode

For more information, see chapter 3.8.3.

This BOOT signal must be left open for normal use or XMODEM download.

3.13.2 Pin Description

Signal	Pin number	I/O	I/O type	Description
BOOT (DCD pin)	23	I	1V8	Download mode selection

Table 32: Boot Pin description

3.13.3 Application

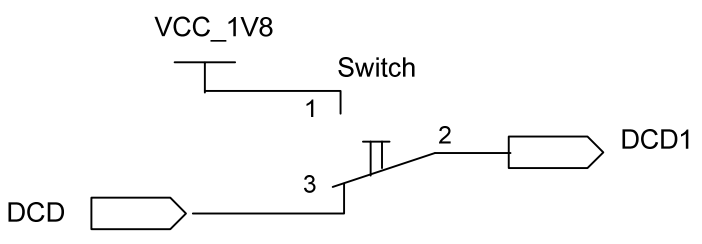


Figure 21: Boot Selection Application Example

3.14 VREF_2V8 Output

This output can only be used to connect pull-up resistor. VCC_2V8 must be used as a reference supply. The voltage supply is available when the Q52 OMNI is on.

Signal	Pin number	I/O	I/O type	Description
VREF_2V8	2	O	Supply	Digital supply

Table 33: VREF_2V8 Pin Description

Parameter		Minimum	Typ	Maximum	Unit
VCC_2V8	Output voltage	2.74	2.8	2.86	V
	Output Current			15	mA

Table 34: VREF_2V8 Electrical Characteristics

3.15 BAT-RTC (Backup Battery)

The Q52 Omni provides an input/output to connect a Real Time Clock power supply.

3.15.1 Interface Description

This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported by the Q52 Omni when VCC_3V6 is available, but a back-up power supply is needed to save date and time when the VCC_3V6 is switched off (VCC_3V6 = 0V).

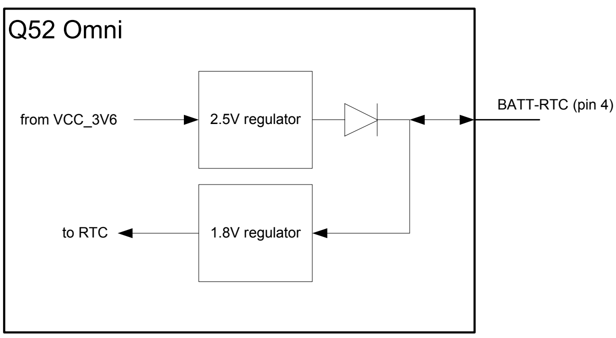


Figure 22: Real Time Clock power supply

If the RTC is not used, this pin can be left open.

If VCC_MAIN is available, the back-up battery can be charged by the internal 2.5V power supply regulator.

Signal	Pin number	I/O	I/O type	Description
BATT-RTC	4	I/O	Supply	RTC Back-up supply

Table 35: Bat-RTC Pin Description

Parameter	Minimum	Typ	Maximum	Unit
Input voltage	1.85		2.5	V
Input current consumption*		3.3		µA
Output voltage		2.45		V
Output current			2	mA

Table 36: Bat-RTC Electrical Characteristics

*Provided by an RTC back-up battery when Q52 OMNI VCC_MAIN power supply is off (VCC_MAIN = 0V).

3.16 FLASH-LED Signal

FLASH LED is an open drain output. A LED and a resistor can be directly connected between this output and VCC_MAIN.

When the Q52 Omni CPU is ON, this output is used to indicate network status.

GSM status	VCC_3V6 status	FLASH-LED status	Q52 OMNI GSM status
ON	**VCC_3V6 = 3.6V**	Permanent	Q52 Omni switched ON, not registered on the network
		Slow flash LED ON for 200 ms, OFF for 2 s	Q52 Omni switched ON, registered on the network
		Quick flash LED ON for 200 ms, OFF for 600 ms	Q52 Omni switched ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	Q52 Omni switched on, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

Table 37: Flash-LED Status

Signal	Pin number	I/O	I/O type	Reset state	Description
FLASH-LED	3	O	Open Drain Output	1 and Undefined	LED driving

Table 38: Flash-LED Pin Description

See Chapter 3.2.3, “Electrical information for digital I/O” for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definitions.

FLASH-LED state is undefined during the software initialization time. During software initialization time, for 2 seconds max after POWER_EN is pulled active low, the FLASH-LED signal is toggling and does not provide Q52 Omni GSM status. After the 2s period, the FLASH-LED provides the true status of the Q52 Omni GSM connection.

Parameter	Condition	Minimum	Typ	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				8	mA

Table 39: Flash-LED Electrical Characteristics

3.17 GPS Functionality

The Q52 Omni provides in option GPS functionality. The GPS is assumed by e-Ride solution based on Opus /// ® Chipsets. This part is controlled by a Q52 Omni’s CPU.

For list of command available refer to AT command list...

3.17.1 Features (eRide Documentation Extract: For Information Only)

- Supports GPS L-band C/A code channels and 2 additional dedicated WAAS channels for enhanced accuracy
- High indoor sensitivity of -161dBm achieved utilizing 44,000 effective correlators (both in acquisition & tracking mode)
- Fast TTFF of typically < 1s when in hot and 34s in cold start conditions
- Accuracy of 2.5m outdoors (CEP 50%) and 10m indoors
- User interface via a serial port, 1Hz update rate

3.17.2 Performances (eRide Documentation Extract: For Information Only)

Parameter	Conditions	Min	Typ	Max	Unit
Hot Start @-135 dBm			1		s
Hot Start @-155 dBm	All SV’s same level		13		s

Parameter	Conditions	Min	Typ	Max	Unit
Warm Start @-135 dBm			33		s
Warm Start @-145 dBm	All SV's same level		67		s
Cold Start @-135 dBm			34		s
Cold Start @-145 dBm	All SV's same level		83		s
Acquisition sensitivity, hot start			-161		dBm
Acquisition sensitivity, warm start			-146.5		dBm
Tracking sensitivity			-161		dBm
Position accuracy, outdoors	Open sky, CEP 50%		2.5		m
Position accuracy, indoors	CEP 50%		10		m

Table 40: GPS Functionality Performances

3.17.2.1 Time-to-First-Fix Charts

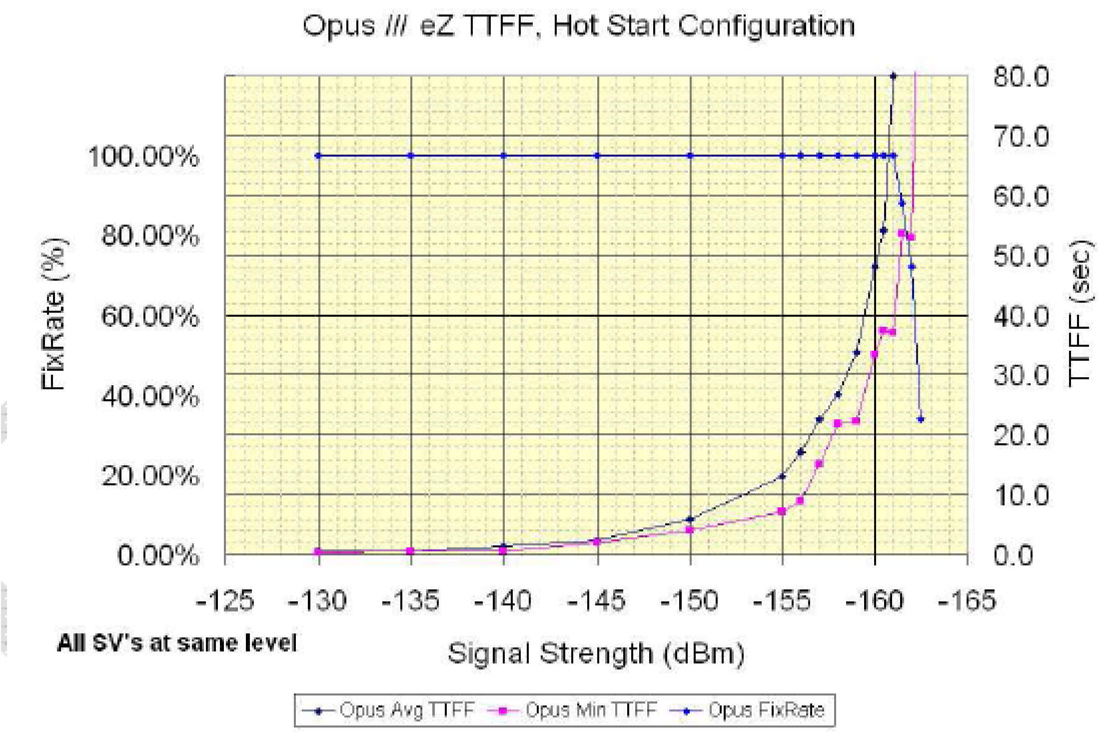


Figure 23: GPS TTFF, Hot Start Configuration

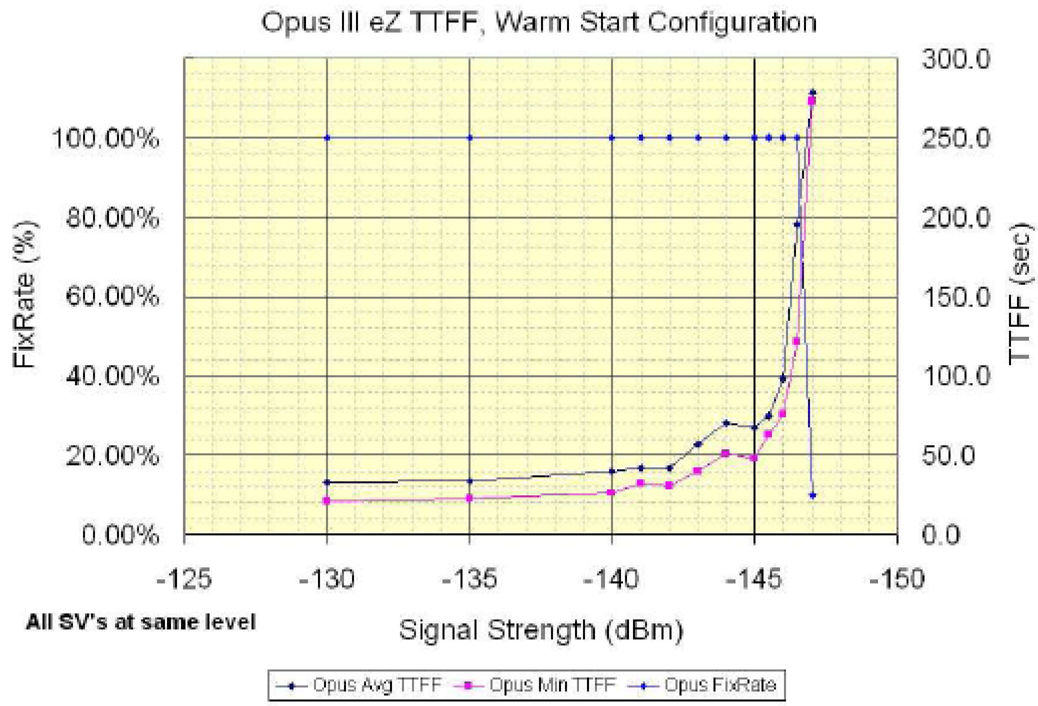


Figure 24: GPS TTFF, Warm Start Configuration

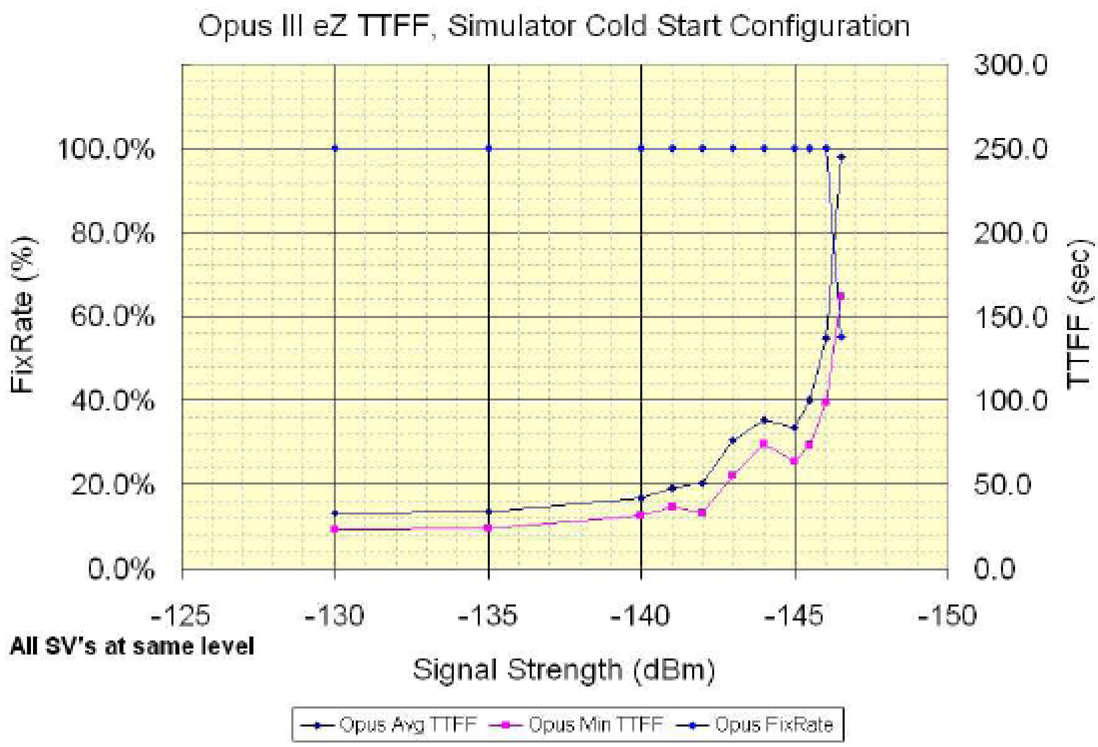


Figure 25: GPS TTFF, Simulator Cold Start Configuration

3.17.2.2 First Position Fix Accuracy Charts

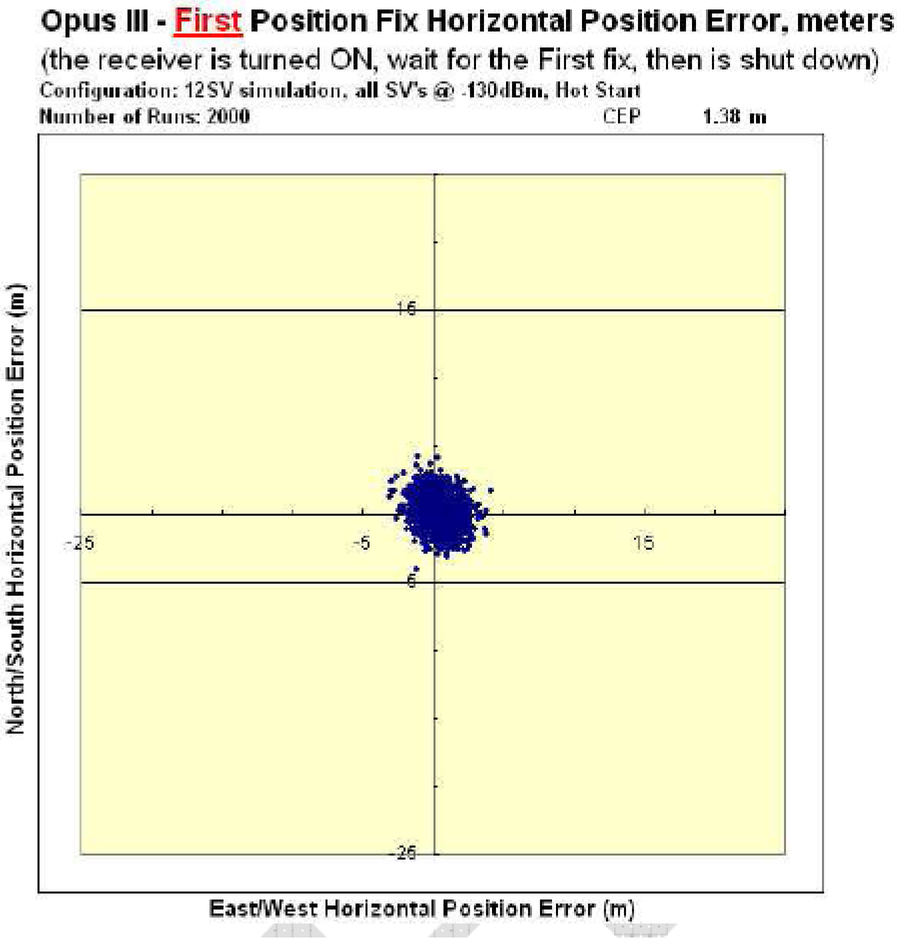


Figure 26: First Position Fix Accuracy Chart 01

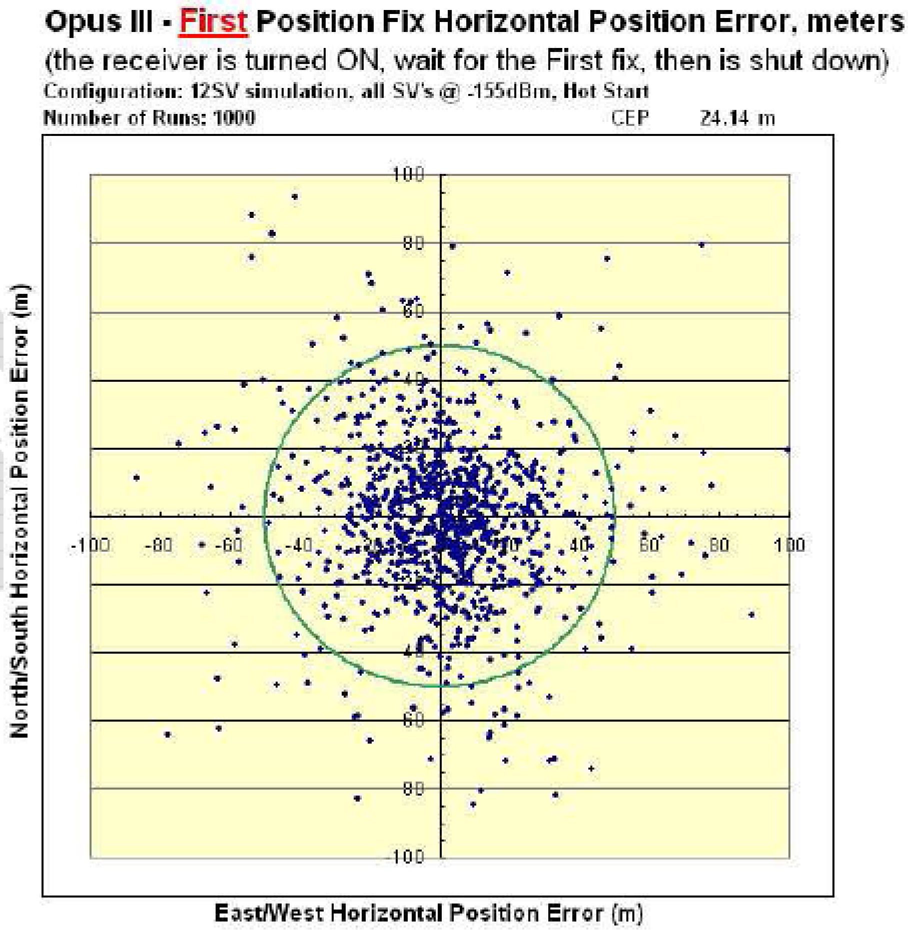


Figure 27: First Position Fix Accuracy Chart 02

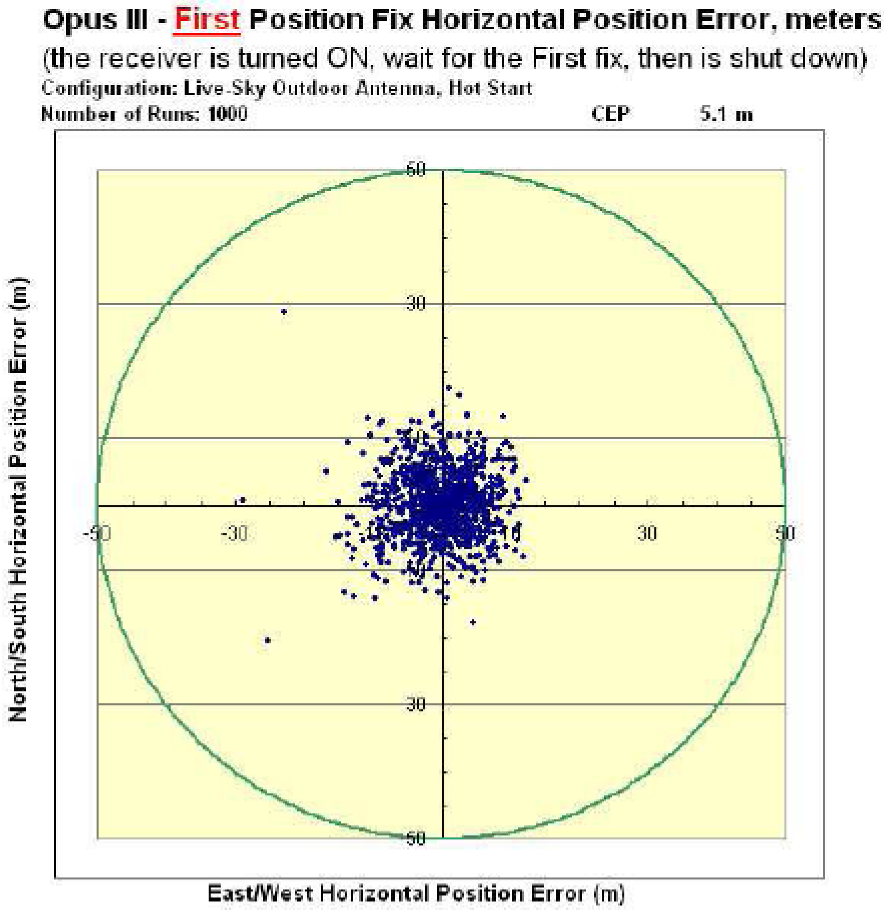


Figure 28: First Position Fix Accuracy Chart 03

3.18 RF Interface

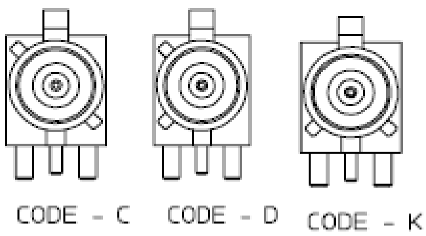
The RF impedance GSM, Orbcomm and GPS* antenna outputs is 50 Ohms nominal and the DC impedance is 0 Ohm.

The GPS* antenna provides 3V biasing for active antenna.

3.18.1 RF Connections

The Q52 OMNI RF connections are assumed by FAKRA Type connectors:

RF Type	Fakra Type	Color
GSM/GPRS	Type D	Bordeaux Violet
Satellite	Type K	Curry Yellow
GPS*	Type C	Blue

- *if available
-
-
- 

3.18.2 RF Performance

GSM mode RF performance is compliant with the ETSI GSM 05.05 recommendation.

The GSM Receiver parameters are:

- GSM850 Reference Sensitivity = -108 dBm Static & TUHigh
- E-GSM900 Reference Sensitivity = -108 dBm Static & TUHigh
- DCS1800 Reference Sensitivity = -107 dBm Static & TUHigh
- PCS1900 Reference Sensitivity = -107 dBm Static & TUHigh
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

3.18.3 Transmitter Parameters

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900): 30 dBm +/- 2 dB at bient temperature
- Minimum output power (EGSM & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature

3.18.4 Antenna Specifications

The antenna must meet the following requirements:

- The optimum operating frequency depends on the application. A dual band or quad band antenna shall operate in these frequency bands and have the following characteristics:

Characteristic		Q52 Omni GSM Mode of Operation			
		E-GSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50 Ohms			
VSWR	Rx max	1.5:1			
	Tx max	1.5:1			
Typical radiated gain		0dBi in one direction at least			

Table 41: GSM Antenna Specifications

4 Technical Specifications

4.1 Environmental Specifications

Wavecom specifies the following temperature range for the Q52 OMNI dual mode product.

The dual mode transceiver is compliant with the following operating class.

Conditions	Temperature range
Operating / Class A	-20 °C to +55°C
Operating / Storage / Class B	-40 °C to +85°C

Function Status Classification:

Class A:

The Wireless CPU® remains fully functional, meeting GSM performance criteria in accordance with ETSI requirements, across the specified temperature range.

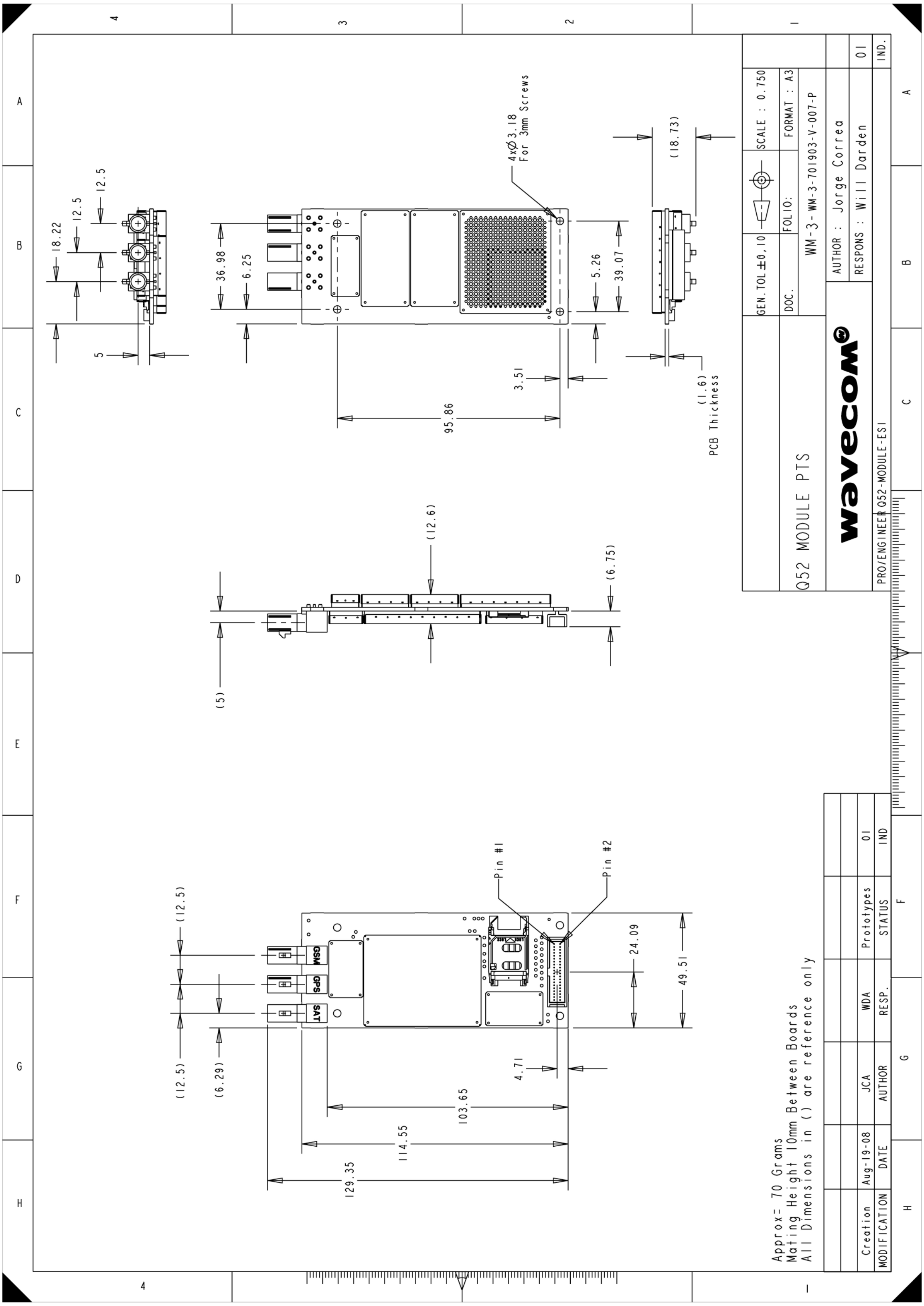
Class B:

The Wireless CPU® remains fully functional, across the specified temperature range. Some GSM parameters may occasionally deviate from the ETSI specified requirements and this deviation does not affect the ability of the Wireless CPU® to connect to the cellular network and function fully.

Q52 Omni Transceiver		ENVIRONNEMENTAL CLASSES		
TYPE OF TEST	STANDARDS	STORAGE Class 1.2	TRANSPORTATION Class 2.3	OPERATING (PORT USE) Class 7.3
Cold	IEC 68-2.1 Ab test	-25° C 72 h	-40° C 72 h	-20° C (GSM900) 16 h -10° C (GSM1800/1900) 16h
Dry heat	IEC 68-2.2 Bb test	+70° C 72 h	+70° C 72 h	+55° C 16 h
Change of temperature	IEC 68-2.14 Na/Nb test		-40° / +30° C 5 cycles t1 = 3 h	-20° / +30° C (GSM900) 3 cycles -10° / +30° C (GSM1800/1900): 3 cycles t1 = 3 h
Damp heat cyclic	IEC 68-2.30 Db test	+30° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1
Damp heat	IEC 68-2.56 Cb test	+30° C 4 days	+40° C 4 days	+40° C 4 days
Sinusoidal vibration	IEC 68-2.6 Fc test	5 - 62 Hz : 5 mm / s 62 - 200Hz : 2 m / s2 3 x 5 sweep cycles		
Random vibration wide band	IEC 68-3.36 Fdb test		5 - 20 Hz : 0.96 m2 / s3 20 - 500Hz : - 3 dB / oct 3 x 10 min	10 -12 Hz : 0.96 m2 / s3 12 - 150Hz : - 3 dB / oct 3 x 30 min

Figure 29: Environmental classes

4.2 Mechanical Specifications



4.3 Antenna Cable

TBD

4.4 GSM Antenna

GSM antennas and support for antenna adaptation can be obtained from manufacturers such as:

- ALLGON (**http://www.allgon.com**)
- IRSCHMANN (**http://www.hirschmann.com/**)

5 Appendix

5.1 Standards and Recommendations

GSM ETSI, 3GPP, GCF and NAPRD03 recommendations for Phase II & FCC.

Specification Reference	Title
3GPP TS 45.005 v5.5.0 (2002-08) Release 5	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception
GSM 02.07 V8.0.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); Mobile Stations (MS) features (GSM 02.07 version 8.0.0 Release 1999)
GSM 02.60 V8.1.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description, Stage 1 (GSM 02.60 version 8.1.0 Release 1999)
GSM 03.60 V7.9.0 (2002-09)	Technical Specification Group Services and System Aspects; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description; Stage 2 (Release 1998)
3GPP TS 43.064 V5.0.0 (2002-04)	Technical Specification Group GERAN; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Overall description of the GPRS radio interface; Stage 2 (Release 5)
3GPP TS 03.22 V8.7.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Functions related to Mobile Station (MS) in idle mode and group receive mode; (Release 1999)
3GPP TS 03.40 V7.5.0 (2001-12)	Technical Specification Group Terminals; Technical realization of the Short Message Service (SMS) (Release 1998)
3GPP TS 03.41 V7.4.0 (2000-09)	Technical Specification Group Terminals; Technical realization of Cell Broadcast Service (CBS) (Release 1998)
ETSI EN 300 903 V8.1.1 (2000-11)	Digital cellular telecommunications system (Phase 2+); Transmission planning aspects of the speech service in the GSM Public Land Mobile Network (PLMN) system (GSM 03.50 version 8.1.1 Release 1999)

Specification Reference	Title
3GPP TS 04.06 V8.2.1 (2002-05)	Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station - Base Station System (MS - BSS) interface; Data Link (DL) layer specification (Release 1999)
3GPP TS 04.08 V7.18.0 (2002-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Mobile radio interface layer 3 specification (Release 1998)
3GPP TS 04.10 V7.1.0 (2001-12)	Technical Specification Group Core Networks; Mobile radio interface layer 3 Supplementary services specification; General aspects (Release 1998)
3GPP TS 04.11 V7.1.0 (2000-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Point-to-Point (PP) Short Message Service (SMS) support on mobile radio interface (Release 1998)
3GPP TS 45.005 v5.5.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception (Release 5)
3GPP TS 45.008 V5.8.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem link control (Release 5)
3GPP TS 45.010 V5.1.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem synchronization (Release 5)
3GPP TS 46.010 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Transcoding (Release 5)
3GPP TS 46.011 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Substitution and muting of lost frames for full rate speech channels (Release 5)
3GPP TS 46.012 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Comfort noise aspect for full rate speech traffic channels (Release 5)

Specification Reference	Title
3GPP TS 46.031 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Discontinuous Transmission (DTX) for full rate speech traffic channels (Release 5)
3GPP TS 46.032 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Voice Activity Detector (VAD) for full rate speech traffic channels (Release 5)
TS 100 913V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General on Terminal Adaptation Functions (TAF) for Mobile Stations (MS) (GSM 07.01 version 8.0.0 Release 1999)
GSM 09.07 V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General requirements on interworking between the Public Land Mobile Network (PLMN) and the Integrated Services Digital Network (ISDN) or Public Switched Telephone Network (PSTN) (GSM 09.07 version 8.0.0 Release 1999)
3GPP TS 51.010-1 v5.0.0 (2002-09)	Technical Specification Group GSM/EDGE ; Radio Access Network ;Digital cellular telecommunications system (Phase 2+);Mobile Station (MS) conformance specification; Part 1: Conformance specification (Release 5)
3GPP TS 51.011 V5.0.0 (2001-12)	Technical Specification Group Terminals; Specification of the Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (Release 5)
ETS 300 641 (1998-03)	Digital cellular telecommunications system (Phase 2); Specification of the 3 Volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)
GCF-CC V3.7.1 (2002-08)	Global Certification Forum – Certification criteria
NAPRD03 V2.6.0 (2002-06)	North America Permanent Reference Document for PTCRB tests

The Q52 Omni connected on a development kit board application is certified to be in accordance with the following Rules and Regulations of the Federal Communications Commission (FCC).

Power listed on the Gant is conducted for Part 22 and conducted for Part 24

This device contains GSM, GPRS Class 10 functions in the 900 and 1800MHz Band which are not operational in U.S. Territories.

This device is to be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Antennas used for this OEM module must not exceed 3.1dBi gain for PCS 1900 MHz and 0.9dBi for GSM 850 MHz for mobile and fixed operating configurations. This device is approved as a module to be installed in other devices.

Installed in other portable devices, the exposure conditions require a separate equipment authorization.

The license module had a FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.
If not, a second label must be placed on the outside of the device that contains the following text:

Contains FCC ID: O9EQ52OMNI

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference,
(2) this device must accept any interference received, including interference that may cause undesired operation.

IIMPORTANT: Manufacturers of mobile or fixed devices incorporating the Q52 Omni device are advised to:

• clarify any regulatory questions,
• have their completed product tested,
• have product approved for FCC compliance, and
• include instructions according to above mentioned RF exposure statements in end product user manual.

Please note that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

5.2 Declaration of Conformity

To Whom it May Concern:

We, Wavecom

430 Davis Drive Suite 300

PO Box 13920

Research Triangle Park

NC 27709 USA

declare under our sole responsibility that the Product

Q52 OMNI

to which this declaration relates is in conformity with the following standards or other normative documents

EN 301 721

EN 301-489-20

as they apply to the above referenced Product.

Research Triangle Park — Peter Cotterill

November 12, 2008 — Certification Manager

5.3 Safety Recommendations (for Information Only)

IMPORTANT
FOR THE EFFICIENT AND SAFE OPERATION OF YOUR GSM APPLICATION
PLEASE READ THIS INFORMATION CAREFULLY

5.3.1 RF Safety

5.3.1.1 General

Your GSM terminal* is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out and receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

5.3.1.2 Exposure to RF Energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

5.3.1.3 Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

* based on WISMO2D

5.3.1.4 Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. Consult your manual to see if you may change the antenna yourself. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Use only the supplied or approved antenna. Unauthorized antennas, modifications or attachments could damage the terminal and may contravene local RF emission regulations or invalidate type approval.

5.3.2 General Safety

5.3.2.1 Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull off the road and park before making or answering a call if driving conditions so require.

5.3.2.2 Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However RF energy may affect some improperly shielded electronic equipment.

5.3.2.3 Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

5.3.2.4 Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

5.3.2.5 Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you to have permission from a crew member to use your terminal while the aircraft is on the ground. To prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

5.3.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

5.3.2.7 Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

5.3.2.8 Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. It is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fueling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is to be used.

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