BGM113 Blue Gecko *Bluetooth*® Smart Module Data Sheet

The Blue Gecko BGM113 is a Bluetooth® Smart Module targeted for Bluetooth Smart applications where small size, reliable RF, low-power consumption, and easy application development are key requirements. At +3 dBm TX power, BGM113 is ideal for applications requiring short and medium range Bluetooth Smart connectivity.

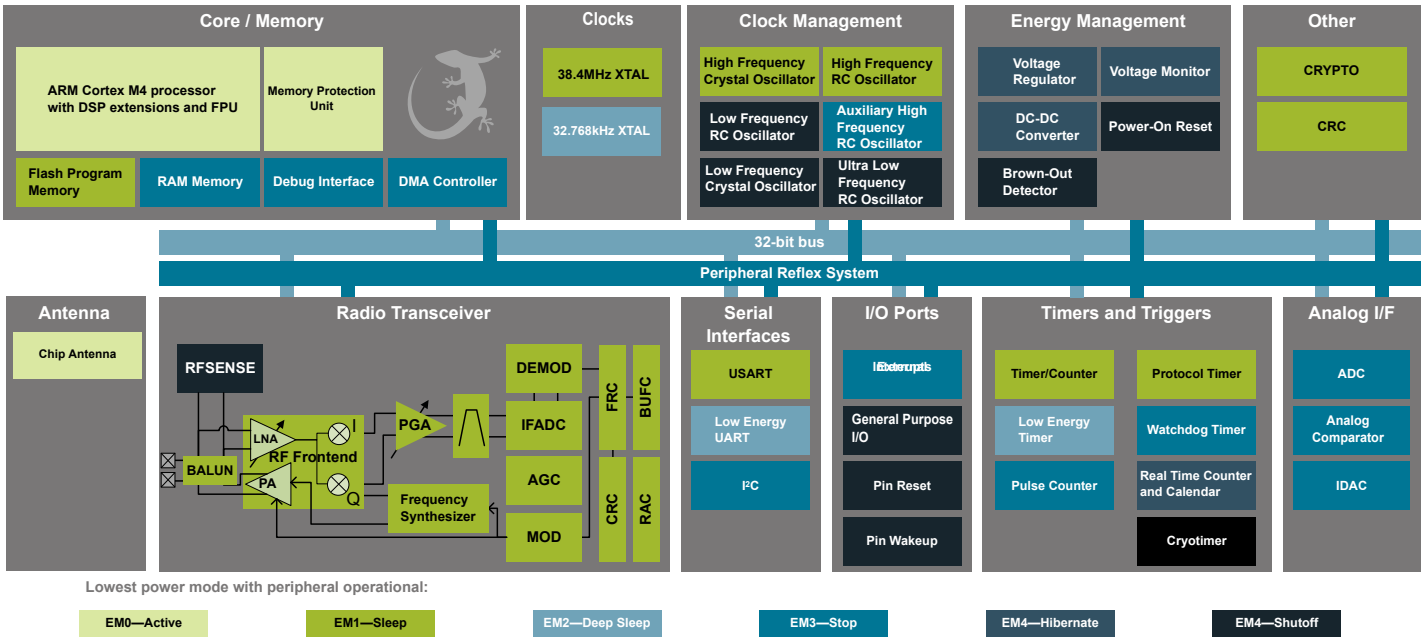
The BGM113 integrates all of the necessary elements required for a Bluetooth Smart application: Bluetooth radio, software stack, and GATT-based profiles, and it can also host end user applications, which means no external microcontroller is required in size, price or power constrained devices. The BGM113 Bluetooth Smart Module also has highly flexible hardware interfaces to connect to different peripherals or sensors.

BGM113 can be used in a wide variety of applications:

- IoT Sensors and End Devices
- Commercial and Retail
- Health and Wellness
- Industrial, Home and Building Automation
- Smart Phone, Tablet and PC Accessories

KEY FEATURES

- Bluetooth 4.1 Compliant (Bluetooth Smart)
- Software upgradable to Bluetooth 4.2
- Integrated antenna
- TX power: up to +3 dBm
- RX sensitivity: down to -93 dBm
- Range: up to 50 meters
- 32-bit ARM® Cortex®-M4 core at 38.4 MHz
- Flash memory: 256kB
- RAM: 32 kB
- Autonomous Hardware Crypto Accelerator and True Random Number Generator
- Integrated DC-DC Converter
- Onboard Bluetooth Smart stack



1. Feature List

The BGM113 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit 38.4 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - 256 kB flash program memory
  - 32 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to +3 dBm
- **Low Energy Consumption**
  - 8.7 mA RX current at 2.4 GHz
  - 8.8 mA TX current @ 0 dBm output power at 2.4 GHz
  - 63 µA/MHz in Active Mode (EM0)
  - 1.4 µA EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 1.1 µA EM3 Stop current (State/RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -93 dBm sensitivity @ 1 Mbit/s GFSK (2.4GHz)
- **Supported Protocol**
  - Bluetooth® Smart
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2× Analog Comparator (ACMP)
  - Digital to Analog Current Converter (IDAC)
  - 14 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
  - 14 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator @ 50nA
  - 2×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - Low Energy UART (LEUART™)
  - I^2C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.85 V to 3.8 V single power supply
  - Integrated DC-DC
  - -40 °C to 85 °C
- **Dimensions**
  - 9.15 x 15.73 x 1.9 mm

2. Ordering Information

Ordering Code	Protocol Stack	Frequency Band	Max TX Power (dBm)	Encryption	Flash (KB)	RAM (KB)	GPIO	Package
BGM113A256V1[1]	Bluetooth Smart	2.4 GHz	3	Full	256	32	14	100 pcs cut reel
BGM113A256V1R[1]	Bluetooth Smart	2.4 GHz	3	Full	256	32	14	1000 pcs tape and reel
BGM113A256V2	Bluetooth Smart	2.4 GHz	3	Full	256	32	14	100 pcs cut reel
BGM113A256V2R	Bluetooth Smart	2.4 GHz	3	Full	256	32	14	1000 pcs tape and reel
SLWSTK6101B[2]								

Note:

1. Initial production. This (V1) product code is updated to production version (V2) when the logos of the official CE and FCC certifications are marked into the RF shield. The only visual difference between initial production (V1) and production (V2) versions will be the certification codes printed on the RF shield. Silicon Labs reserves the right to deliver V2 (production version) for customers ordering V1.
2. Blue Gecko Bluetooth Smart Module Wireless Development Kit (WSTK) with BGM113 and BGM111 radio boards, expansion board and accessories.

3. System Overview

3.1 Introduction

The BGM113 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application, as well as other system requiring high performance and low-energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the *EFR32 Reference Manual*.

A detailed block diagram of the EFR32BG SoC is shown in the figure below which is used in the BGM113 Bluetooth Smart module.

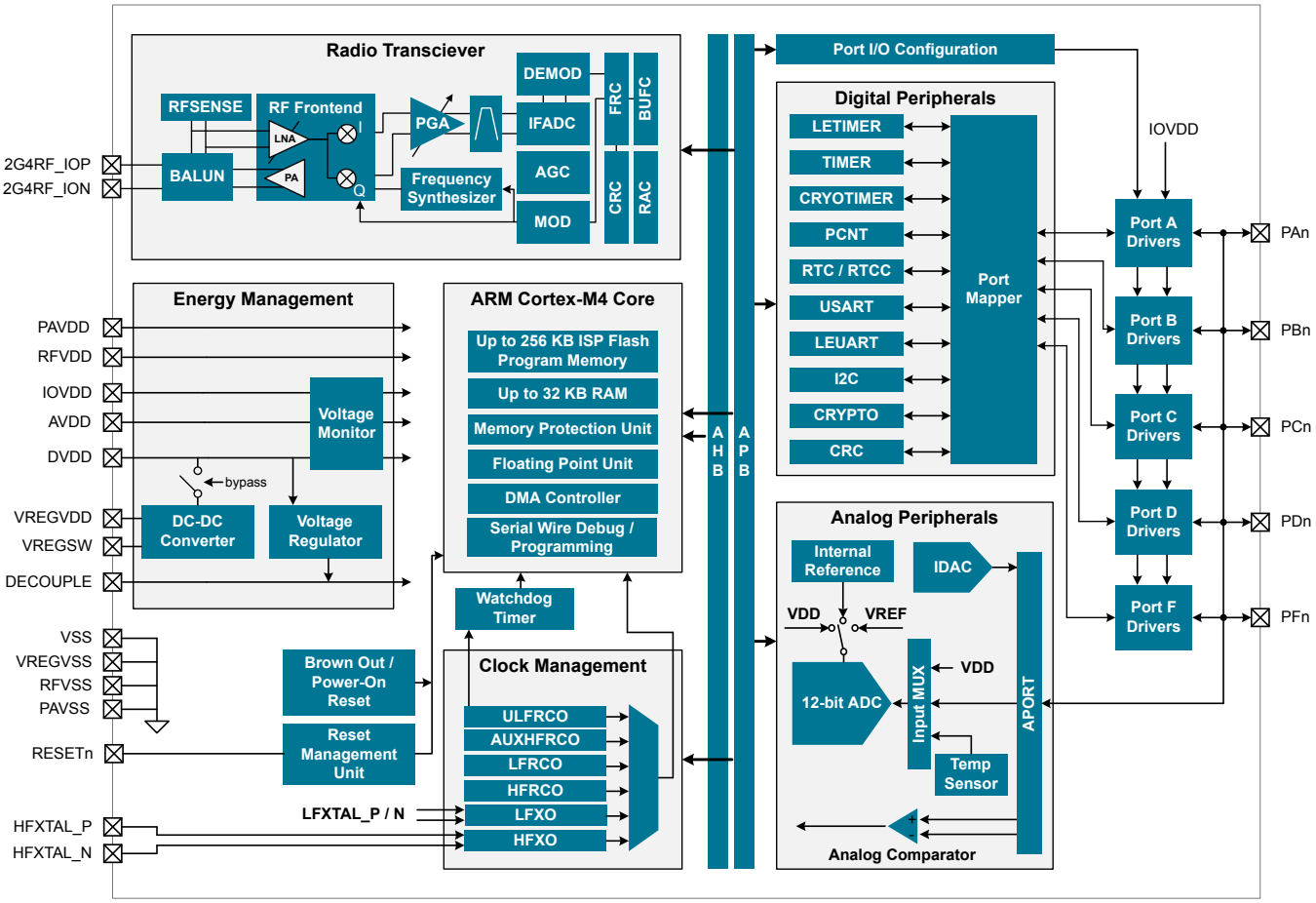


Figure 3.1. Detailed EFR32BG1 Block Diagram

3.2 Radio

The BGM113 features a radio transceiver supporting Bluetooth Smart® protocol.

3.2.1 Antenna Interface

The BGM113 has a built in 2.4GHz ceramic chip antenna.

Table 3.1. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	30%	Efficiency and peak gain depend on the application PCB layout and mechanical design
Peak gain	0.5 dBi	

3.2.2 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the BGM113 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.3 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.4 Packet and State Trace

The BGM113 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.5 Data Buffering

The BGM113 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.6 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the BGM113. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.7 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The BGM113 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An integrated DC-DC buck regulator is utilized to further reduce the current consumption.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

BGM113 has up to 14 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the BGM113. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal Oscillators

The BGM113 fully integrates two crystal oscillators and four RC oscillators, listed below.

- A 38.4MHz high frequency crystal oscillator (HFXO) provides a precise timing reference for the MCU and radio.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. It supports AES encryption and decryption with 128- or 256-bit keys and ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05 µA and 64 µA with several ranges with various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the BGM113. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M4F processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4F RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- 256 KB flash program memory
- 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The BGM113 memory map is shown in the figures below.

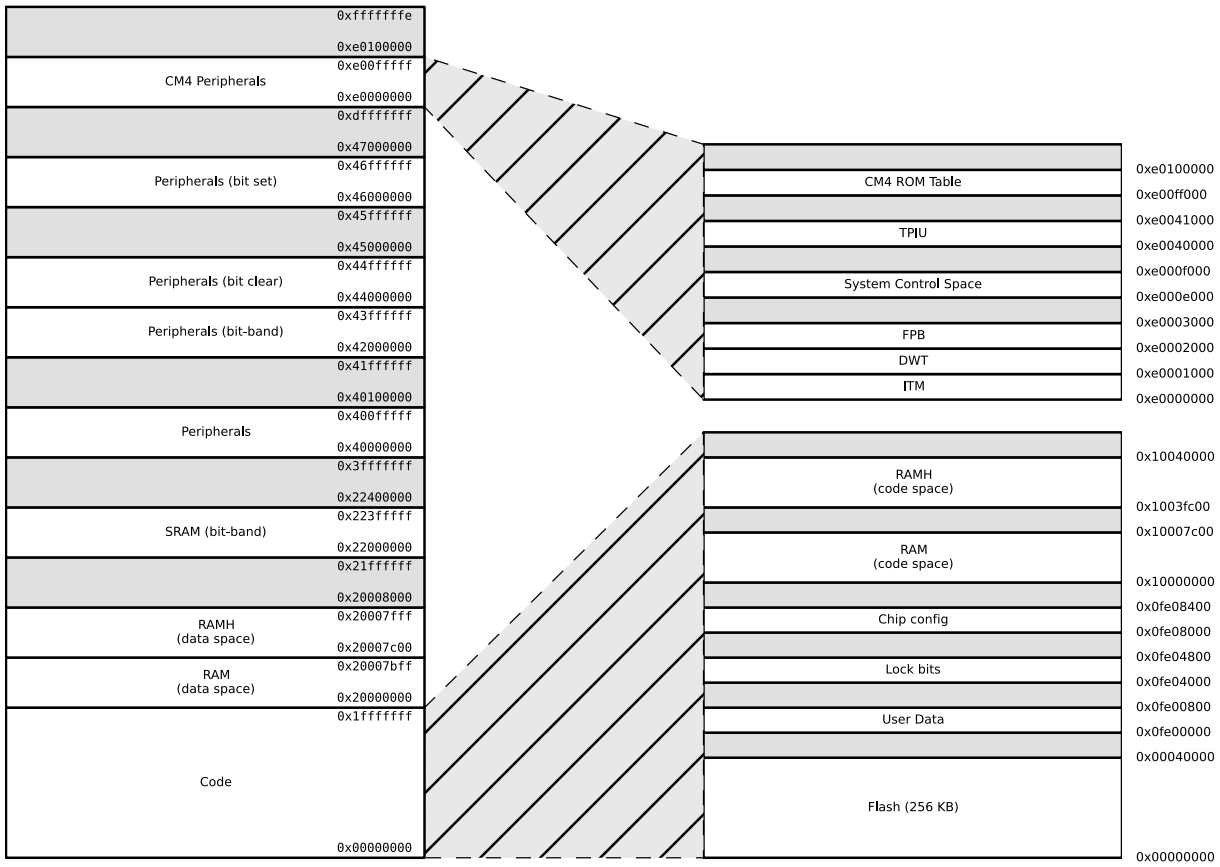


Figure 3.2. BGM113 Memory Map — Core Peripherals and Code Space

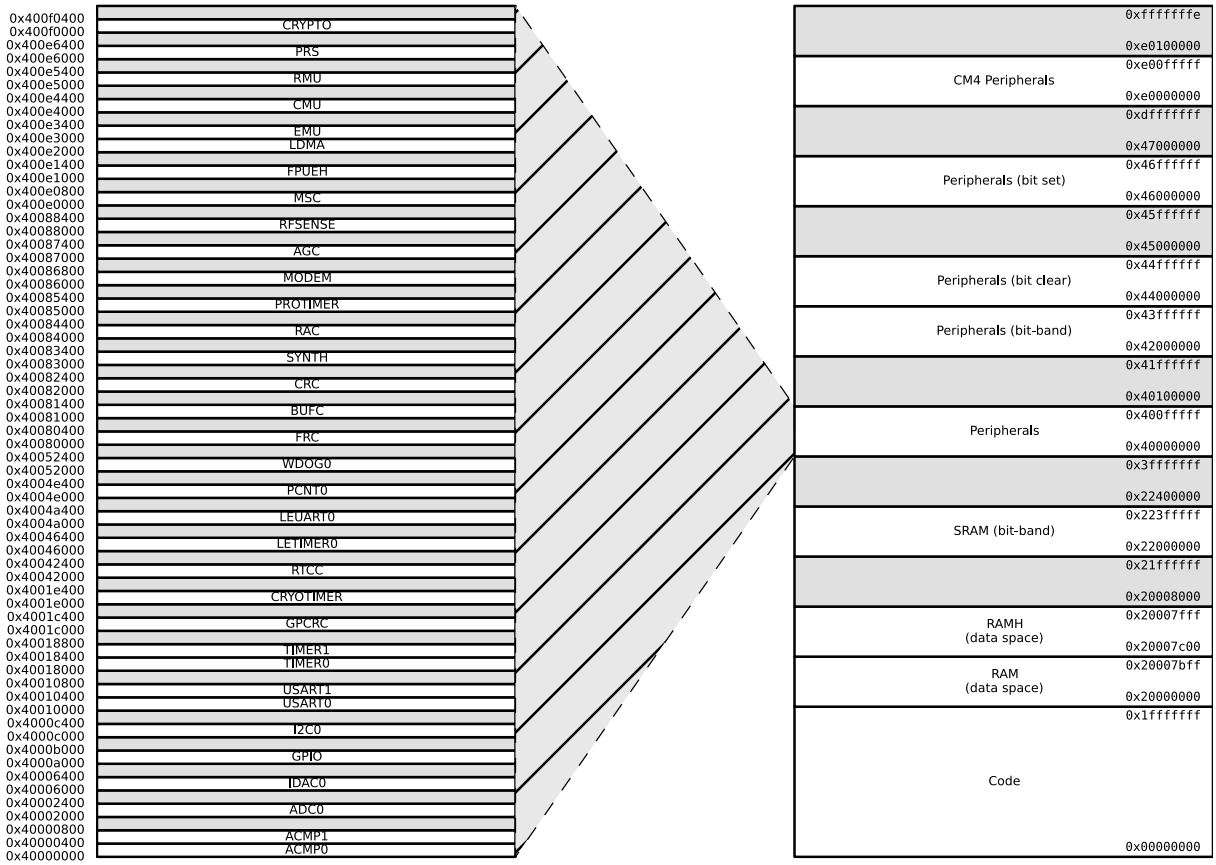


Figure 3.3. BGM113 Memory Map — Peripherals

3.13 Configuration Summary

The features of the BGM113 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and an operating temperature of -40 to +85 °C, unless stated otherwise.

Refer to Table 4.2 General Operating Conditions on page 12 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Total current into V_{SS} ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	-G temperature grade	-40	25	85	°C
VDD Operating supply voltage	V_{DD}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass 50mA load	TBD	3.3	3.8	V
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0)	—	—	26	MHz
		1 wait-states (MODE = WS1)	—	38.4	38.4	MHz

4.1.3 Current Consumption

4.1.3.1 Current Consumption 1.85 V without DC-DC Converter

EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. See 5.1 Power, Ground, Debug and UART.

Table 4.3. Current Consumption 1.85V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled, All peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash	—	128	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	103	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	105	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	235	—	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled	I_{EM1}	38.4 MHz crystal	—	61	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	167	—	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.36	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	3.13	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.84	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.08	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.64	—	µA
		128 byte RAM retention, no RTCC	—	0.63	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	No RAM retention, no RTCC	—	0.02	—	µA

4.1.3.2 Current Consumption 3.3 V without DC-DC Converter

EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. See 5.1 Power, Ground, Debug and UART.

Table 4.4. Current Consumption 3.3V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled, All peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash	—	129	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	103	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	105	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	237	—	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled	I_{EM1}	38.4 MHz crystal	—	61	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	170	—	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.47	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	3.35	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.92	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.13	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.67	—	µA
		128 byte RAM retention, no RTCC	—	0.66	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

4.1.3.3 Current Consumption 3.3 V using DC-DC Converter

Table 4.5. Current Consumption 3.3V with DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled. All peripherals disabled, DCDC in LowNoise mode	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash.	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	79	—	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled, DCDC in LowPower mode.	I_{EM1}	38.4 MHz crystal	—	39	—	µA/MHz
		38 MHz HFRCO	—	23	—	µA/MHz
		26 MHz HFRCO	—	25	—	µA/MHz
		1 MHz HFRCO	—	142	—	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	1.4	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	1.4	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	1.1	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	0.9	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.6	—	µA
		128 byte RAM retention, no RTCC	—	0.6	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.03	—	µA

4.1.3.4 Current Consumption Using Radio

Table 4.6. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{RX}	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	8.7	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{TX}	CW, 0 dBm, F = 2.4 GHz, Radio clock prescaled by 3	—	8.8	—	mA
		CW, 3 dBm, F = 2.4 GHz	—	17.6	—	mA
RFSENSE current consumption	$I_{RFSENSE}$		—	51	—	nA

4.1.4 Wake up times

Table 4.7. Wake up times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep Sleep	t_{EM2_WU}	Code execution from flash	—	10.7	—	µs
		Code execution from RAM	—	3	—	µs
Wakeup time from EM1 Sleep	t_{EM1_WU}	Executing from flash	—	3	—	AHB Clocks
		Executing from RAM	—	3	—	AHB Clocks
Wake up from EM3 Stop	t_{EM3_WU}	Executing from flash	—	10.7	—	µs
		Executing from RAM	—	3	—	µs
Wake up from EM4H Hibernate [1]	t_{EM4H_WU}	Executing from flash	—	60	—	µs
Wake up from EM4S Shutoff[1]	t_{EM4S_WU}		—	290	—	µs

Note:
1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

4.1.5 Brown Out Detector

Table 4.8. Brown Out Detector

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDDBOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	TBD	V
		DVDD falling	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	24	—	mV
DVDD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.85	V
		AVDD falling	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	21	—	mV
AVDD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	46	—	mV
EM4 response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.6 Frequency Synthesizer Characteristics

Table 4.9. Frequency Synthesizer Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F_{RANGE_2400}	2.4 GHz frequency range	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	F_{RES_2400}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	ΔF_{MAX_2400}		—	—	1677	kHz

4.1.7 2.4 GHz RF Transceiver Characteristics

4.1.7.1 RF Transmitter Characteristics for Bluetooth Smart in the 2.4 GHz Band

Table 4.10. RF Transmitter Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6dB bandwidth	TXBW		—	740	—	kHz
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247	—	-6.5	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	10	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	At ±2 MHz	—	-39.8	—	dBm
		At ±3 MHz	—	-42.1	—	dBm
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM\_FCC}$	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	—	-47.3	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$. Restricted Bands	$SPUR_{OOB\_FCC}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier[2]	—	-47	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$. Non Restricted Bands		Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328	$SPUR_{ETSI328}$	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz	—	-42	—	dBm
		1-12 GHz	—	-36	—	dBm

Note:

1. Per Bluetooth Core_4.2, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2480 Mhz, a maximum duty cycle of 20% is used to achieve this value.

4.1.7.2 RF Receiver Characteristics for Bluetooth Smart in the 2.4 GHz Band

Table 4.11. RF Receiver Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	With dirty transmitter as defined in Core_4.1	—	-91.8	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity	—	8.3	—	dB
N+1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-3	—	dB
N-1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-0.5	—	dB
Alternate (2 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-43	—	dB
Alternate (3 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_3	Interferer is reference signal at ±3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-46.7	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-38.7	—	dB
Selectivity to image frequency +1 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision	—	-48.2	—	dB
Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range.	$BLOCK_{OOB}$	Interferer frequency 30 MHz ≤ f ≤ 2000 MHz	—	-27	—	dBm
		Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz	—	-32	—	dBm
		Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz	—	-32	—	dBm
		Interferer frequency 3 GHz ≤ f ≤ 12.75 GHz	—	-27	—	dBm
Intermodulation performance per Core_4.1, Vol 6 Section 4.4 (n = 3 alternative), 0.1% BER.	IM	Desired is reference signal at 6dB above reference sensitivity level. Interferer 1 is CW at level IM_{BLE}. Interferer 2 is reference signal at IM_{BLE}.	—	-33	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		4	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		—	—	-101	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	—	0.5	dB

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm

4.1.8 Oscillators

4.1.8.1 LFXO

Table 4.12. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Current consumption after startup	I_{LFXO}	GAIN[1], AGC[1]	—	273	—	nA
Start- up time	t_{LFXO}	GAIN[1]	—	308	—	ms

Note:
1. In CMU_LFXOCTRL register

4.1.8.2 HFXO

Table 4.13. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}			38.4		MHz
Startup time	t_{HFXO}	38.4 MHz: BOOST[1] = 2	—	300	—	µs
Frequency Tolerance for the crystal	FT_{HFXO}	38.4 MHz	-25	—	25	ppm

Note:
1. In CMU_HFXOCTRL register

4.1.8.3 LFRCO

Table 4.14. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	TBD	32.768	TBD	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register

4.1.8.4 HFRCO and AUXHFRCO

Table 4.15. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{HFRCO}	38 MHz frequency band	TBD	38	TBD	MHz
		32 MHz frequency band	TBD	32	TBD	MHz
		26 MHz frequency band	TBD	26	TBD	MHz
		19 MHz frequency band	TBD	19	TBD	MHz
		16 MHz frequency band	TBD	16	TBD	MHz
		13 MHz frequency band	TBD	13	TBD	MHz
		7 MHz frequency band	TBD	7	TBD	MHz
		4 MHz frequency band	TBD	4	TBD	MHz
		2 MHz frequency band	TBD	2	TBD	MHz
		1 MHz frequency band	TBD	1	TBD	MHz
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on DVDD	$I_{HFRCODIG}$	$f_{HFRCO} = 38$ MHz	—	43	—	µA
		$f_{HFRCO} = 32$ MHz	—	37	—	µA
		$f_{HFRCO} = 26$ MHz	—	31	—	µA
		$f_{HFRCO} = 19$ MHz	—	25	TBD	µA
		$f_{HFRCO} = 16$ MHz	—	22	—	µA
		$f_{HFRCO} = 13$ MHz	—	19	—	µA
		$f_{HFRCO} = 7$ MHz	—	12	—	µA
		$f_{HFRCO} = 4$ MHz	—	10	—	µA
		$f_{HFRCO} = 2$ MHz	—	8	—	µA
		$f_{HFRCO} = 1$ MHz	—	7	—	µA
Current consumption on AVDD [1]	$I_{HFRCOANA}$	$f_{HFRCO} = 38$ MHz	—	161	—	µA
		$f_{HFRCO} = 32$ MHz	—	134	—	µA
		$f_{HFRCO} = 26$ MHz	—	116	—	µA
		$f_{HFRCO} = 19$ MHz	—	101	TBD	µA
		$f_{HFRCO} = 16$ MHz	—	88	—	µA
		$f_{HFRCO} = 13$ MHz	—	81	—	µA
		$f_{HFRCO} = 7$ MHz	—	69	—	µA
		$f_{HFRCO} = 4$ MHz	—	23	—	µA
		$f_{HFRCO} = 2$ MHz	—	23	—	µA
		$f_{HFRCO} = 1$ MHz	—	23	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Note:
1. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register

4.1.8.5 ULFRCO

Table 4.16. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

4.1.9 Flash Memory Characteristics

Table 4.17. Flash Memory Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<85°C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	26	40	µs
Page erase time	t_{PERASE}		20	27	40	ms
Mass erase time	t_{MERASE}		20	27	40	ms
Device erase time[2]	t_{DERASE}		—	60	TBD	ms
Page erase current[3]	I_{ERASE}		—	—	3	mA
Mass or Device erase current[3]			—	—	5	mA
Write current[3]	I_{WRITE}		—	—	3	mA

Note:
1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
3. Measured at 25°C

4.1.10 GPIO

Table 4.18. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	IOVDD*0.3	V
Input high voltage	V_{IOIH}		IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{IOOH}	Sourcing 3 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{IOOL}	Sinking 3 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	GPIO ≤ IOVDD	—	0.1	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up resistor	R_{PU}		TBD	43	TBD	kΩ
I/O pin pull-down resistor	R_{PD}		TBD	43	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register

4.1.11 VMON

Table 4.19. VMON

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VMON Supply Current	I_{VMON}	In EM0 or EM1, 1 supply monitored	—	5.8	—	µA
		In EM0 or EM1, 4 supplies monitored	—	11.8	—	µA
		In EM2, EM3 or EM4, 1 supply monitored	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored	—	99	—	nA
VMON Loading of Monitored Supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		TBD	—	TBD	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.12 ADC

Table 4.20. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range	V_{ADCIN}	Single ended	0	—	2*V_{REF}	V
		Differential	-V_{REF}	—	V_{REF}	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[1]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current on DVDD, using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADCDIG\_CONTINOUS}$	1 Msps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	40	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG[3] = 6	—	15	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG[3] = 15	—	9	—	µA
Current on DVDD, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	I_{ADCDIG_NORMAL}	35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	40	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG[3] = 0	—	5	—	µA
Current on DVDD, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADCDIG\_STANDBY}$	125 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	12	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	6	—	µA
Current on AVDD[4], using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADCANA\_CONTINOUS}$	1 Msps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	286	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG[3] = 6	—	155	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG[3] = 15	—	102	—	µA
Current on AVDD[4] , using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	I_{ADCANA_NORMAL}	35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	35	—	µA
		5 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	5	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current on AVDD[4], using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADCANA\_STANDBY}$	125 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	110	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	80	—	µA
ADC Clock Frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[5]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core in NORMAL mode	$t_{ADCSTART}$	WARMUPMODE[2] = NORMAL	—	—	5	µs
From standby mode		WARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	—	—	1	µs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	TBD	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	—	380	—	µV
Offset Error	$V_{ADCOFFSETERR}$		TBD	1	TBD	LSB
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution	-1	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Temperature Sensor Slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL
2. In ADCn_CNTL register
3. In ADCn_BIASPROG register
4. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register
5. Derived from ADCCLK

4.1.13 IDAC

Table 4.21. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N_{IDAC_RANGES}		—	4	—	-
Output Current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total Accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	TBD	—	TBD	%
		EM0 or EM1	TBD	—	TBD	%
		EM2 or EM3	TBD	—	TBD	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption in EM0 or EM1 [2]	I_{IDAC}	Source mode, excluding output current	—	8.9	—	µA
		Sink mode, excluding output current	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.16	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.08	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.03	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.82	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.65	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.4	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.25	—	%

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.14 Analog Comparator (ACMP)

Table 4.22. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	CMPVDD = ACMPn_CTRL_PWRSEL [1]	0	—	CMPVDD	V
Active current not including voltage reference	I_{ACMP}	BIASPROG[2] = 1, FULLBIAS[2] = 0	—	50	—	nA
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	306	—	nA
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	74	TBD	µA
Current consumption of internal voltage reference,	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA
Hysteresis	$V_{ACMPHYST}$	HYSTSEL[3] = HYST0	—	0	TBD	mV
		HYSTSEL[3] = HYST1	—	12	—	mV
		HYSTSEL[3] = HYST2	—	22	—	mV
		HYSTSEL[3] = HYST3	—	30	—	mV
		HYSTSEL[3] = HYST4	—	36	—	mV
		HYSTSEL[3] = HYST5	—	41	—	mV
		HYSTSEL[3] = HYST6	—	47	—	mV
		HYSTSEL[3] = HYST7	—	52	—	mV
Comparator delay	$t_{ACMPDELAY}$	BIASPROG[2] = 1, FULLBIAS[2] = 0 [4]	—	30	—	µs
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0 [4]	—	3.7	—	µs
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1 [4]	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[2] =0x20, FULLBIAS[2] = 1 [4]	—	—	TBD	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Capacitive Sense Internal Resistance	R_{CSRES}	CSRESSEL[5] = 0	—	inf	—	kΩ
		CSRESSEL[5] = 1	—	15	—	kΩ
		CSRESSEL[5] = 2	—	27	—	kΩ
		CSRESSEL[5] = 3	—	39	—	kΩ
		CSRESSEL[5] = 4	—	51	—	kΩ
		CSRESSEL[5] = 5	—	102	—	kΩ
		CSRESSEL[5] = 6	—	164	—	kΩ
		CSRESSEL[5] = 7	—	239	—	kΩ

Note:

1. CMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD
2. In ACMPn_CTRL register
3. In ACMPn_HYSTERESIS register
4. ± 100 mV differential
5. In ACMPn_INPUTSEL register

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

$I_{ACMPREF}$ is zero if an external voltage reference is used.

4.1.15 I2C

I2C Standard-mode (Sm)

Table 4.23. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	$t_{SU,DAT}$		250	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	3450	ns
Repeated START condition set-up time	$t_{SU,STA}$		4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		4	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode (Fm)

Table 4.24. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$		100	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	900	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:
1. For CLHR set to 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode Plus (Fm+)

Table 4.25. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$		50	—	—	ns
SDA hold time	$t_{HD,DAT}$		100	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.16 USART SPI

SPI Master Timing

Table 4.26. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1, 2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1, 2]	t_{CS_MO}		0	—	8	ns
SCLK to MOSI [1, 2]	t_{SCLK_MO}		3	—	20	ns
MISO setup time [1, 2]	t_{SU_MI}	IOVDD = 1.98 V	56	—	—	ns
		IOVDD = 3.0 V	37	—	—	ns
MISO hold time [1, 2]	t_{H_MI}		6	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

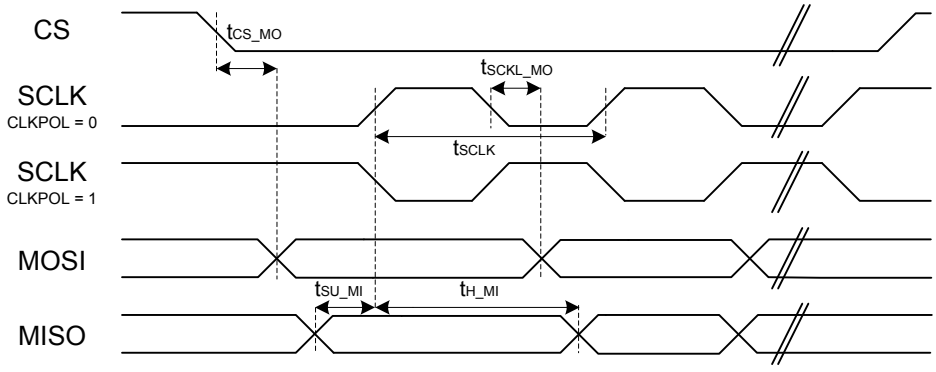


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.27. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCKL period [1, 2]	t_{SCLK_sl}		2 * $t_{HFPERCLK}$	—	—	ns
SCLK high period[1, 2]	t_{SCLK_hi}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low period [1, 2]	t_{SCLK_lo}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1, 2]	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO [1, 2]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1, 2]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1, 2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1, 2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

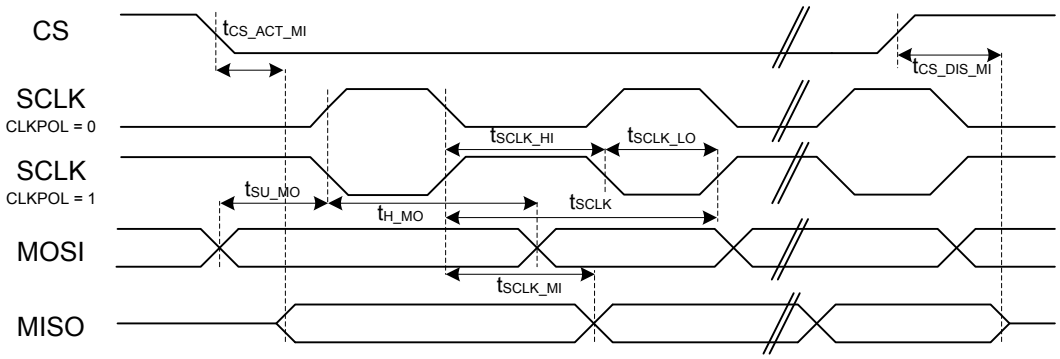


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 1.0 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 8 MHz

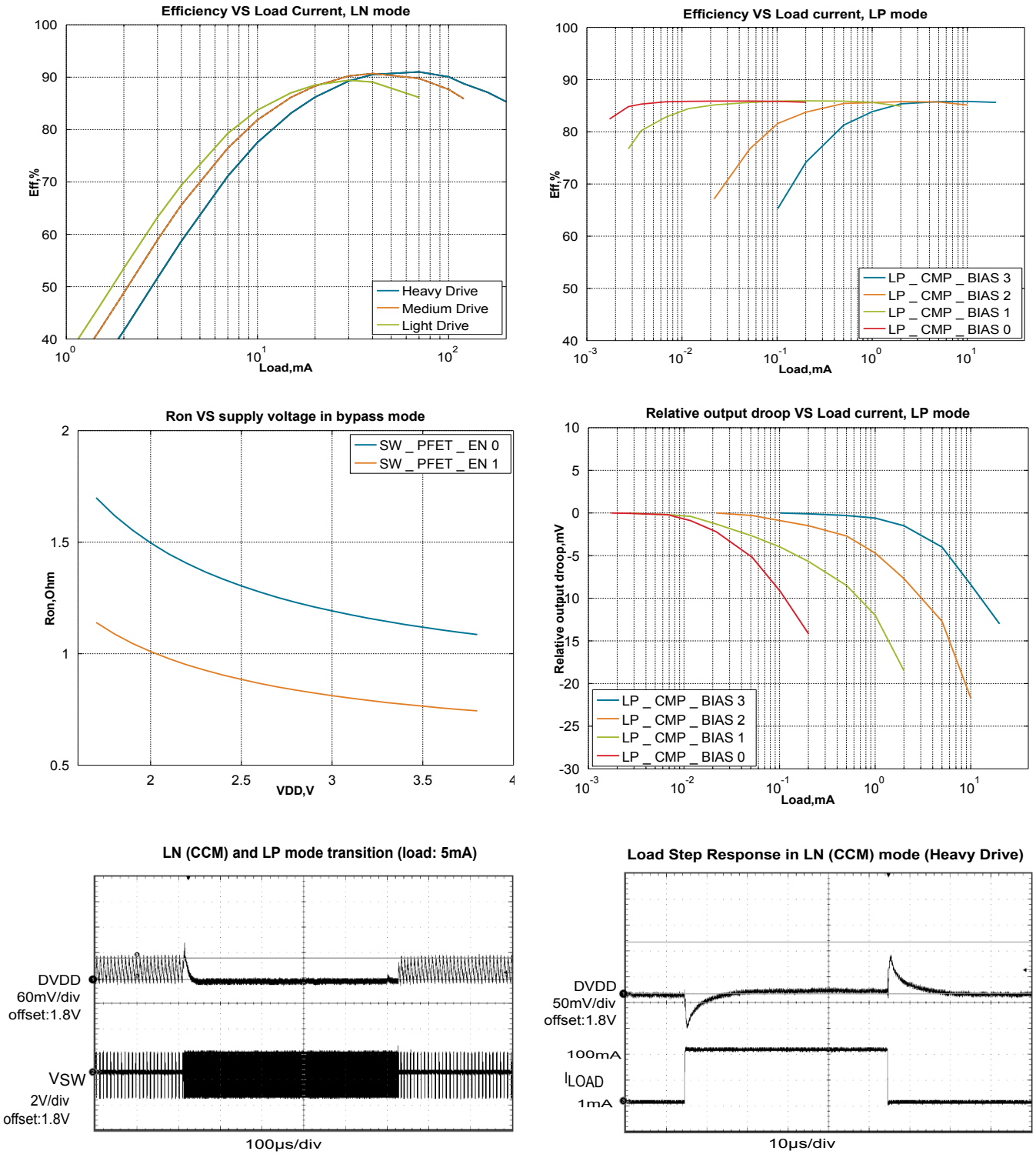
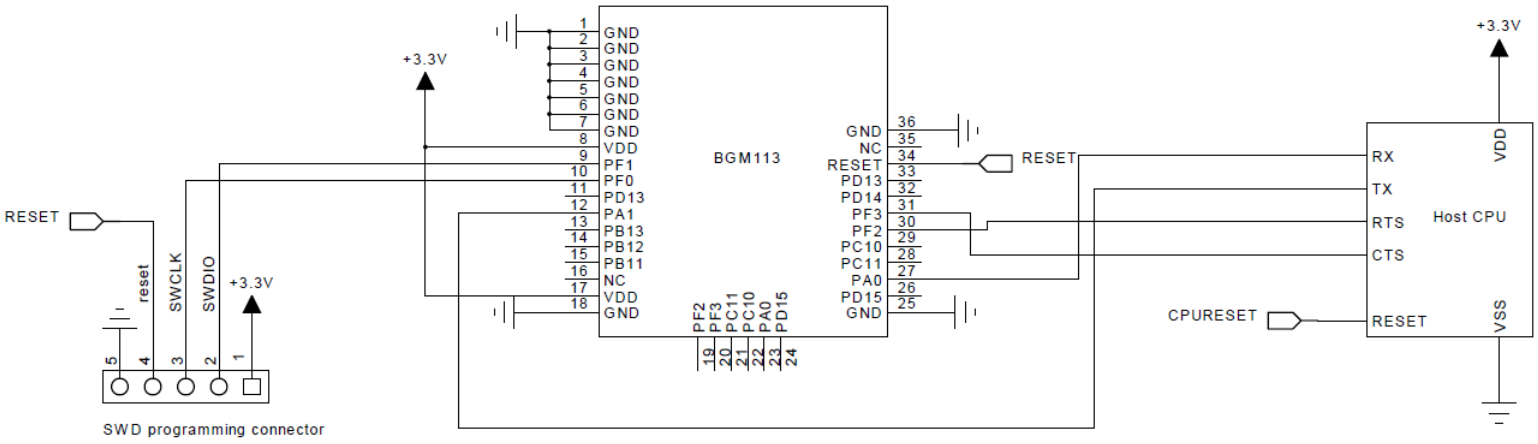


Figure 4.3. DC-DC Converter Typical Performance Characteristics

5. Typical Connection Diagrams

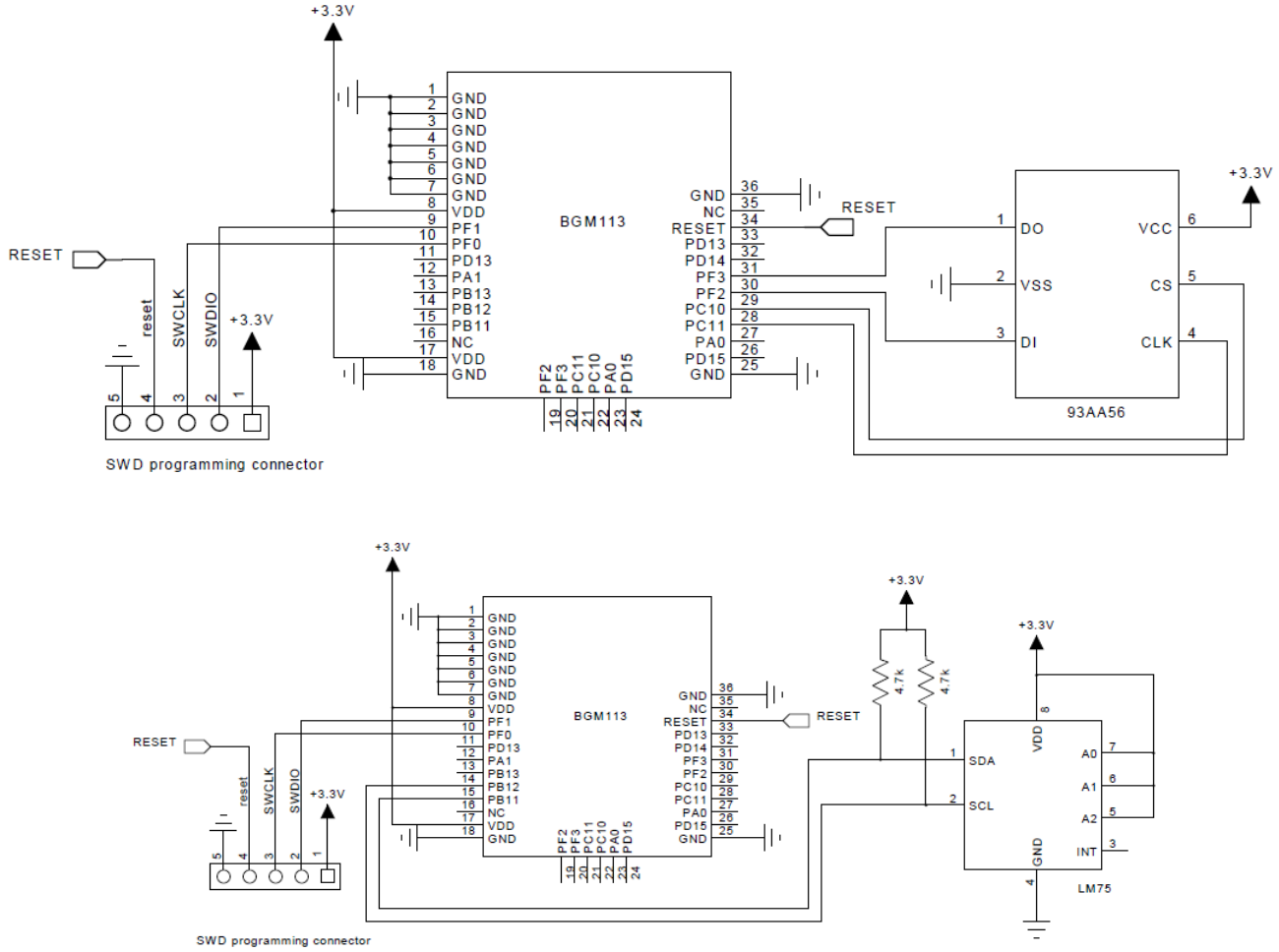
5.1 Power, Ground, Debug and UART

Typical power supply, ground and MCU debug and UART connections are shown in the figure below.



5.2 SPI and I2C Peripheral Connections

The figure below shows how to connect a SPI or I2C peripherals.



6. Layout Guidelines

6.1 Layout Guidelines

For optimal performance of the BGM113 Module, please follow these guidelines:

- Place the module at the edge of the PCB, as shown in the figure below.
- Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna (shown in the figure below as a white rectangle between the pad rows).
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Do not place plastic or any other dielectric material in touch with the antenna.

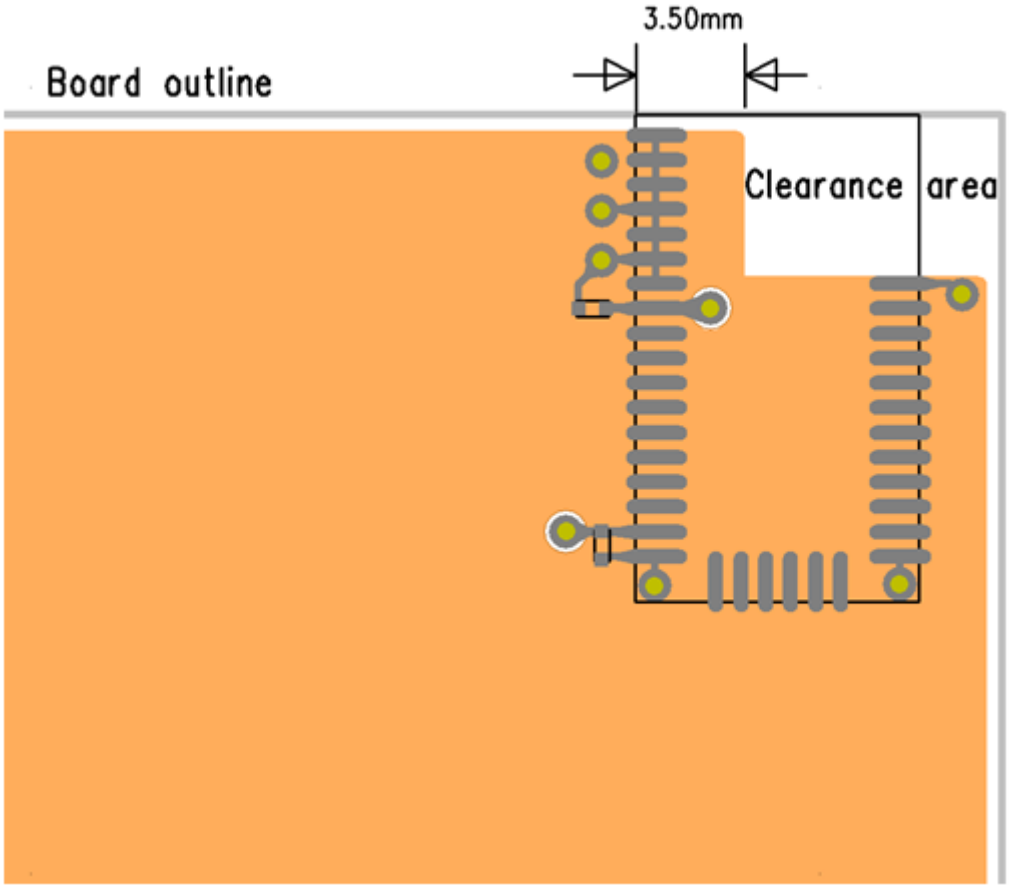


Figure 6.1. Recommended Layout for BGM113 Module

The layouts shown in the figure below will result in severely degraded RF-performance.

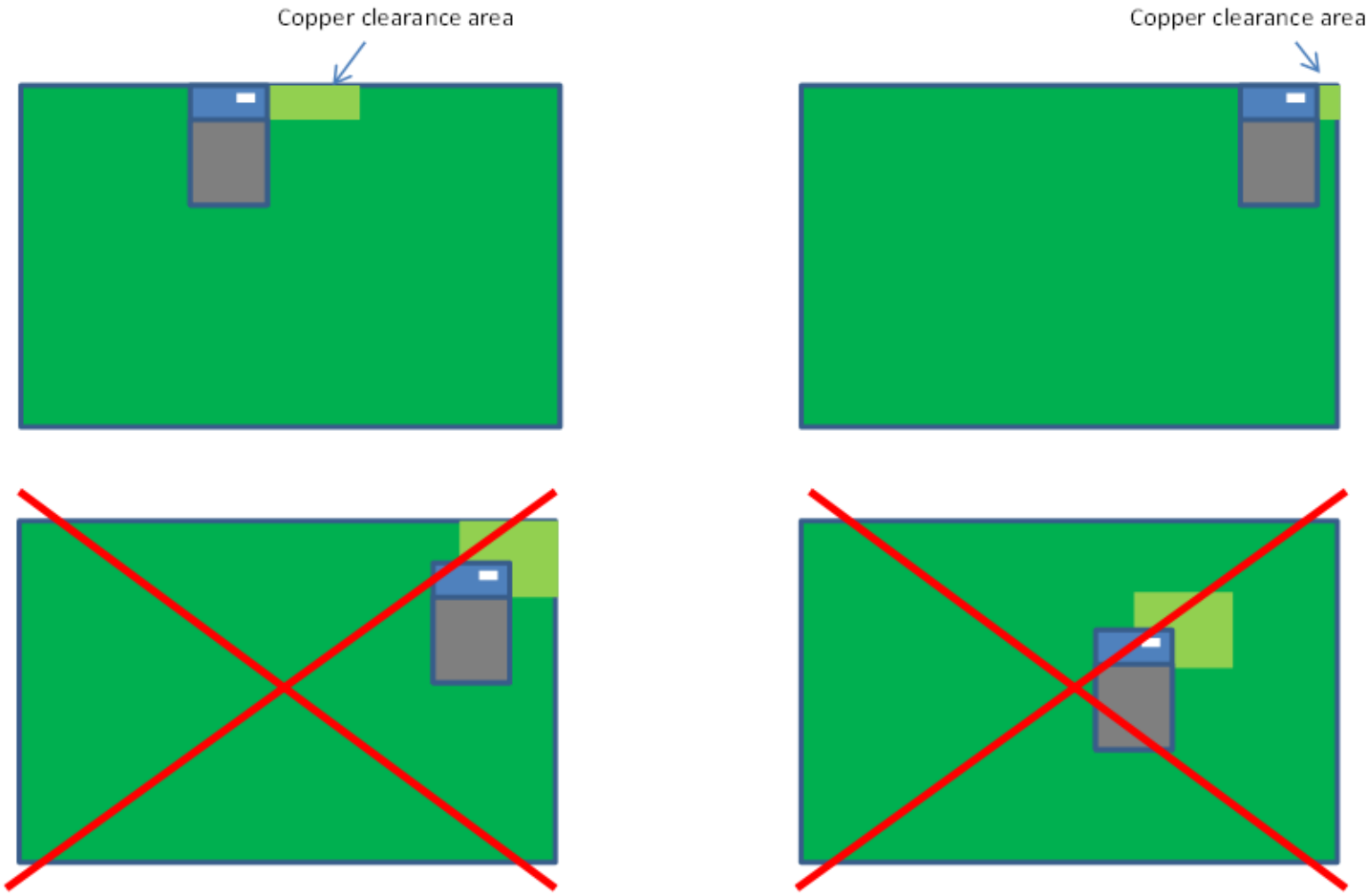


Figure 6.2. Non-optimal PCB Layouts for BGM113 Module

6.2 Effect of Plastic and Metal Materials

The antenna on BGM113 is fairly robust to the proximity of plastic and other low dielectric constant materials, but placing plastic or any other dielectric material in direct contact with the antenna should be avoided. A minimum separation of 5 mm should be maintained between a plastic material and the antenna on the top side and end of the module to prevent dielectric loading of the antenna, but materials can be placed against the bottom of the application PCB. The PCB thickness should be 1 - 2 mm.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7. Pin Definitions

7.1 BGM113 Definition

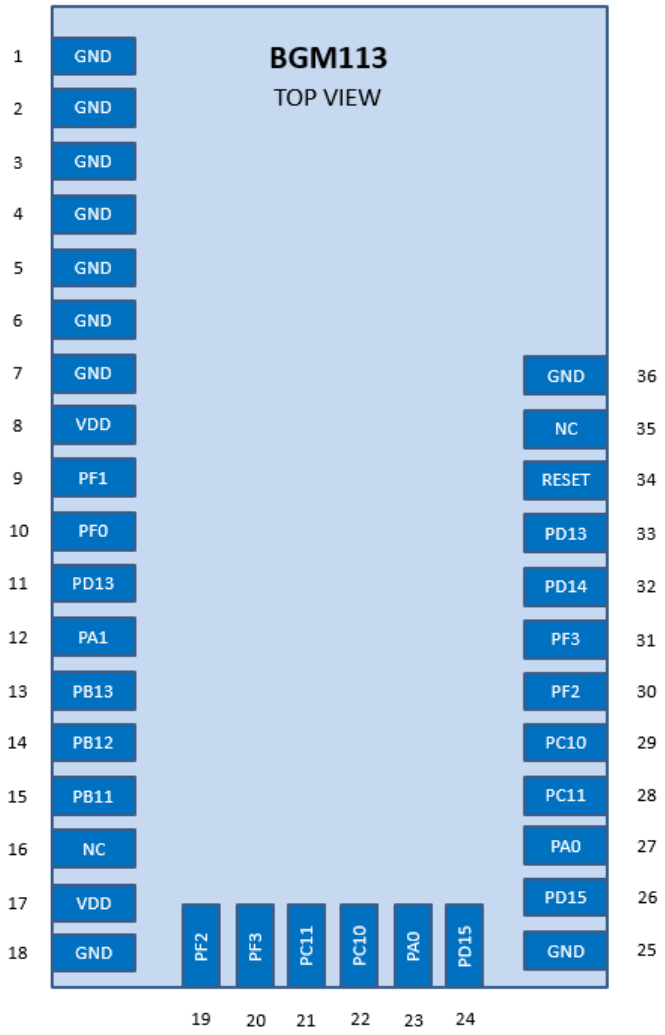


Figure 7.1. BGM113 Pinout

Table 7.1. Device Pinout

Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
1-7, 18, 25, 36	GND	Ground				
10	PF0	BUSAX [ADC0: APORT1XCH16 ACMP0: APORT1XCH16 ACMP1: APORT1XCH16] BUSBY [ADC0: APORT2YCH16 ACMP0: APORT2YCH16 ACMP1: APORT2YCH16]	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE-TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0
9	PF1	BUSAY [ADC0: APORT1YCH17 ACMP0: APORT1YCH17 ACMP1: APORT1YCH17] BUSBX [ADC0: APORT2XCH17 ACMP0: APORT2XCH17 ACMP1: APORT2XCH17]	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE-TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23 MODEM_ANT0 #22 MODEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0
19, 30	PF2	BUSAX [ADC0: APORT1XCH18 ACMP0: APORT1XCH18 ACMP1: APORT1XCH18] BUSBY [ADC0: APORT2YCH18 ACMP0: APORT2YCH18 ACMP1: APORT2YCH18]	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE-TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24 MODEM_ANT0 #23 MODEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
20, 31	PF3	BUSAY [ADC0: APORT1YCH19 ACMP0: APORT1YCH19 ACMP1: APORT1YCH19] BUSBX [ADC0: APORT2XCH19 ACMP0: APORT2XCH19 ACMP1: APORT2XCH19]	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE-TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
8, 17	VDD	Radio power supply				
34	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
11, 33	PD13	BUSCY [ADC0: APORT3YCH5 ACMP0: APORT3YCH5 ACMP1: APORT3YCH5 IDAC0: APORT1YCH5] BUSDX [ADC0: APORT4XCH5 ACMP0: APORT4XCH5 ACMP1: APORT4XCH5]	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE-TIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19 MODEM_ANT0 #18 MODEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
32	PD14	BUSCX [ADC0: APORT3XCH6 ACMP0: APORT3XCH6 ACMP1: APORT3XCH6 IDAC0: APORT1XCH6] BUSDY [ADC0: APORT4YCH6 ACMP0: APORT4YCH6 ACMP1: APORT4YCH6]	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE-TIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20 MODEM_ANT0 #19 MODEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4

Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
24, 26	PD15	BUSCY [ADC0: APORT3YCH7 ACMP0: APORT3YCH7 ACMP1: APORT3YCH7 IDAC0: APORT1YCH7] BUSDX [ADC0: APORT4XCH7 ACMP0: APORT4XCH7 ACMP1: APORT4XCH7]	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE-TIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21 MODEM_ANT0 #20 MODEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2
23, 27	PA0	ADC0_EXTN BUSCX [ADC0: APORT3XCH8 ACMP0: APORT3XCH8 ACMP1: APORT3XCH8 IDAC0: APORT1XCH8] BUSDY [ADC0: APORT4YCH8 ACMP0: APORT4YCH8 ACMP1: APORT4YCH8]	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
12	PA1	ADC0_EXTP BUSCY [ADC0: APORT3YCH9 ACMP0: APORT3YCH9 ACMP1: APORT3YCH9 IDAC0: APORT1YCH9] BUSDX [ADC0: APORT4XCH9 ACMP0: APORT4XCH9 ACMP1: APORT4XCH9]	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1

Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
15	PB11	BUSCY [ADC0: APORT3YCH27 ACMP0: APORT3YCH27 ACMP1: APORT3YCH27 IDAC0: APORT1YCH27] BUSDX [ADC0: APORT4XCH27 ACMP0: APORT4XCH27 ACMP1: APORT4XCH27]	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
14	PB12	BUSCX [ADC0: APORT3XCH28 ACMP0: APORT3XCH28 ACMP1: APORT3XCH28 IDAC0: APORT1XCH28] BUSDY [ADC0: APORT4YCH28 ACMP0: APORT4YCH28 ACMP1: APORT4YCH28]	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
13	PB13	BUSCY [ADC0: APORT3YCH29 ACMP0: APORT3YCH29 ACMP1: APORT3YCH29 IDAC0: APORT1YCH29] BUSDX [ADC0: APORT4XCH29 ACMP0: APORT4XCH29 ACMP1: APORT4XCH29]	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9

Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
22, 29	PC10	BUSAX [ADC0: APORT1XCH10 ACMP0: APORT1XCH10 ACMP1: APORT1XCH10] BUSBY [ADC0: APORT2YCH10 ACMP0: APORT2YCH10 ACMP1: APORT2YCH10]	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE-TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13 MODEM_ANT0 #12 MODEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
21, 28	PC11	BUSAY [ADC0: APORT1YCH11 ACMP0: APORT1YCH11 ACMP1: APORT1YCH11] BUSBX [ADC0: APORT2XCH11 ACMP0: APORT2XCH11 ACMP1: APORT2XCH11]	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE-TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14 MODEM_ANT0 #13 MODEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3
16, 35	NC					

7.1.1 BGM113 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

Table 7.2. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	-	-	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	-	-	-	-	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	-	-	-	-	-	-	-	-	-	-	-	-	-
Port E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.
Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 7.3. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
CMU_CLK0	0: PA1 3: PC11	5: PD14 6: PF2							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 3: PC10	5: PD15 6: PF3							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function is enabled to pin out of reset.
FRC_DCLK	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Frame Controller, Data Sniffer Clock.
FRC_DFRAME		4: PB11 5: PB12 6: PB13		13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3	30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1									Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8									Pin can be used to wake the system up from EM4

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N									Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P									Low Frequency Crystal (typically 32.768 kHz) positive pin.
MODEM_ANT0	3: PB11	4: PB12 5: PB13		12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3	29: PA0 30: PA1	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	2: PB11 3: PB12	4: PB13	11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3		28: PA0 29: PA1	MODEM antenna control output 1, used for antenna diversity.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
MODEM_DCLK	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		MODEM data clock out.
MODEM_DIN	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	MODEM data in.
MODEM_DOUT		4: PB11 5: PB12 6: PB13		13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3	30: PA0 31: PA1	MODEM data out.
PCNT0_S0IN	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	2 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3			12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3	7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3	6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3	5: PF0 6: PF1 7: PF2		12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4		4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.
PRS_CH5	3: PD13	4: PD14 5: PD15							Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1	5: PB11 6: PB12 7: PB13	10: PA0						Peripheral Reflex System PRS, channel 7.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH8		4: PB11 5: PB12 6: PB13	9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	3: PB11	4: PB12 5: PB13	8: PA0 9: PA1	15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10		4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	3: PC10	4: PC11							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2		4: PB11 5: PB12 6: PB13		13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3	30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	3: PB11	4: PB12 5: PB13		12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3	29: PA0 30: PA1	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	2: PB11 3: PB12	4: PB13	11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3		28: PA0 29: PA1	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	1: PB11 2: PB12 3: PB13		10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 2	27: PA0	28: PA1	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	2 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		4: PB11 5: PB12 6: PB13		13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3	30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC3	3: PB11	4: PB12 5: PB13		12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3	29: PA0 30: PA1	Timer 1 Capture Compare input / output channel 3.
US0_CLK		4: PB11 5: PB12 6: PB13		13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3	30: PA0 31: PA1	USART0 clock input / output.
US0_CS	3: PB11	4: PB12 5: PB13		12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3	29: PA0 30: PA1	USART0 chip select input / output.
US0_CTS	2: PB11 3: PB12	4: PB13	11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3		28: PA0 29: PA1	USART0 Clear To Send hardware flow control input.
US0_RTS	1: PB11 2: PB12 3: PB13		10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 2	27: PA0	28: PA1	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK		4: PB11 5: PB12 6: PB13		13: PC10 14: PC11	19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3	30: PA0 31: PA1	USART1 clock input / output.
US1_CS	3: PB11	4: PB12 5: PB13		12: PC10 13: PC11	18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3	29: PA0 30: PA1	USART1 chip select input / output.
US1_CTS	2: PB11 3: PB12	4: PB13	11: PC10	12: PC11	17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3		28: PA0 29: PA1	USART1 Clear To Send hardware flow control input.
US1_RTS	1: PB11 2: PB12 3: PB13		10: PC10 11: PC11		16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3	27: PA0	28: PA1	USART1 Request To Send hardware flow control output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_RX	0: PA1	5: PB11 6: PB12 7: PB13		14: PC10 15: PC11		20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3	31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1	6: PB11 7: PB12	8: PB13	15: PC10	16: PC11	21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3		USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

7.3 Analog Port (APORT)

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, and DACs. The APORT consists of wires, switches, and control needed to configurably implement the routes. Please see the device Reference Manual for a complete description.

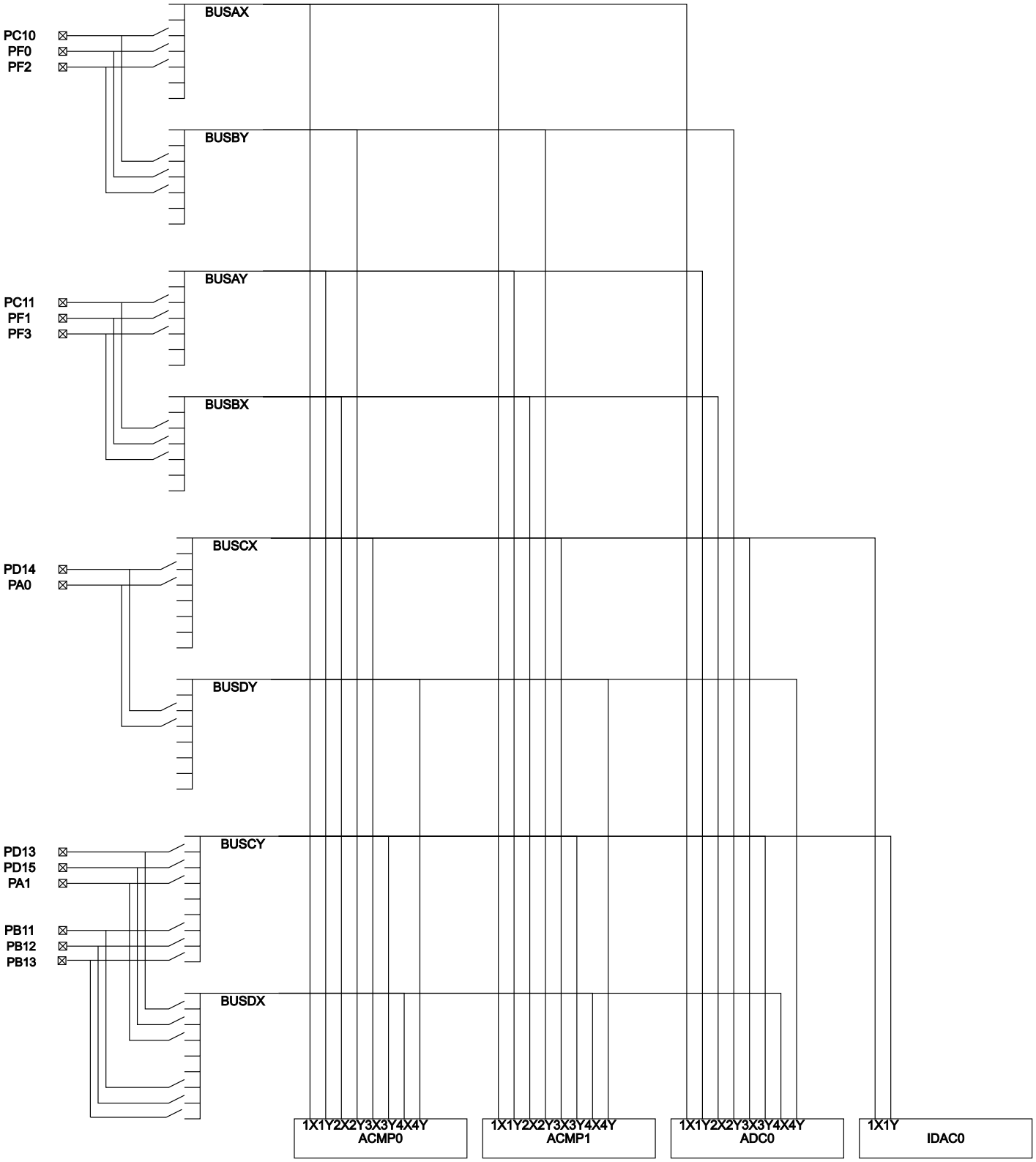


Figure 7.2. BGM113 APORT

Table 7.4. APORT Client Map

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT1XCH6	BUSAX	
	APORT1XCH8		
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		
	APORT1XCH22		
ACMP0	APORT1YCH7	BUSAY	
	APORT1YCH9		
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		
	APORT1YCH23		
ACMP0	APORT2XCH7	BUSBX	
	APORT2XCH9		
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		
	APORT2XCH23		
ACMP0	APORT2YCH6	BUSBY	
	APORT2YCH8		
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		
	APORT2YCH22		

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT3XCH2	BUSCX	
	APORT3XCH4		
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		
	APORT3XCH12		
	APORT3XCH28		PB12
	APORT3XCH30		
ACMP0	APORT3YCH3	BUSCY	
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		
	APORT3YCH13		
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		
ACMP0	APORT4XCH3	BUSDX	
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		
	APORT4XCH13		
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		
ACMP0	APORT4YCH2	BUSDY	
	APORT4YCH4		
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		
	APORT4YCH12		PA4
	APORT4YCH28		PB12
	APORT4YCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT1XCH6	BUSAX	
	APORT1XCH8		
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		
	APORT1XCH22		
ACMP1	APORT1YCH7	BUSAY	
	APORT1YCH9		
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		
	APORT1YCH23		
ACMP1	APORT2XCH7	BUSBX	
	APORT2XCH9		
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		
	APORT2XCH23		
ACMP1	APORT2YCH6	BUSBY	
	APORT2YCH8		
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		
	APORT2YCH22		
ACMP1	APORT3XCH2	BUSCX	
	APORT3XCH4		
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		
	APORT3XCH12		
	APORT3XCH28		PB12
	APORT3XCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT3YCH3	BUSCY	
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		
	APORT3YCH13		
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		
ACMP1	APORT4XCH3	BUSDX	
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		
	APORT4XCH13		
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		
ACMP1	APORT4YCH2	BUSDY	
	APORT4YCH4		
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		
	APORT4YCH12		
	APORT4YCH28		PB12
	APORT4YCH30		
ADC0	APORT1XCH6	BUSAX	
	APORT1XCH8		
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		
	APORT1XCH22		

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT1YCH7	BUSAY	
	APORT1YCH9		
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		
	APORT1YCH23		
ADC0	APORT2XCH7	BUSBX	
	APORT2XCH9		
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		
	APORT2XCH23		
ADC0	APORT2YCH6	BUSBY	
	APORT2YCH8		
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		
	APORT2YCH22		
ADC0	APORT3XCH2	BUSCX	
	APORT3XCH4		
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		
	APORT3XCH12		
	APORT3XCH28		PB12
	APORT3XCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT3YCH3	BUSCY	
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		
	APORT3YCH13		
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		
ADC0	APORT4XCH3	BUSDX	
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		
	APORT4XCH13		
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		
ADC0	APORT4YCH2	BUSDY	
	APORT4YCH4		
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		
	APORT4YCH12		
	APORT4YCH28		PB12
	APORT4YCH30		
IDAC0	APORT1XCH2	BUSCX	
	APORT1XCH4		
	APORT1XCH6		PD14
	APORT1XCH8		PA0
	APORT1XCH10		
	APORT1XCH12		
	APORT1XCH28		PB12
	APORT1XCH30		

Analog Module	Analog Module Channel	Shared Bus	Pin
IDAC0	APORT1YCH3	BUSCY	
	APORT1YCH5		PD13
	APORT1YCH7		PD15
	APORT1YCH9		PA1
	APORT1YCH11		
	APORT1YCH13		
	APORT1YCH27		PB11
	APORT1YCH29		PB13
	APORT1YCH31		

8. BGM113 Package Specifications

8.1 BGM113 Dimensions

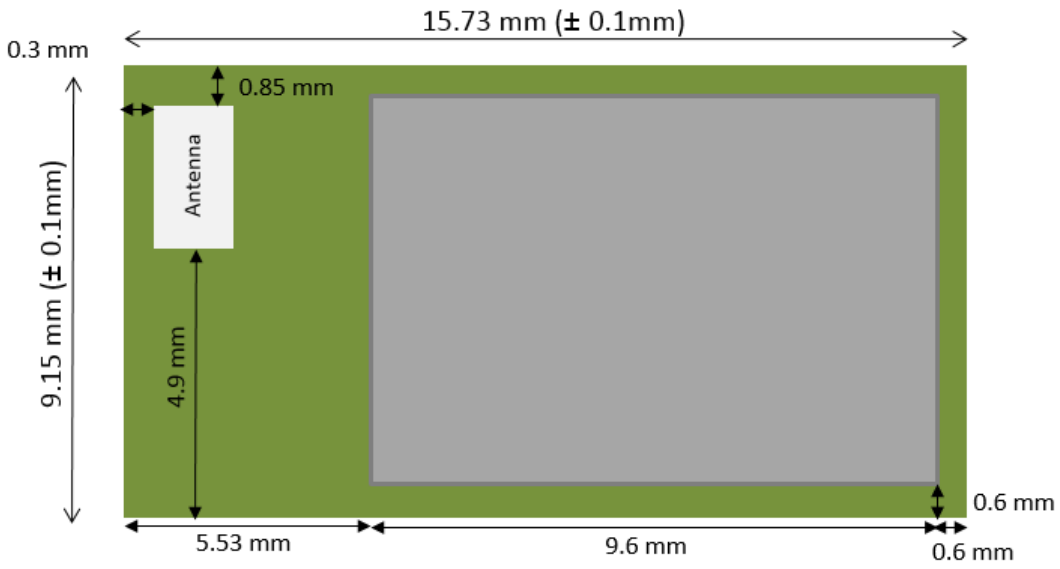
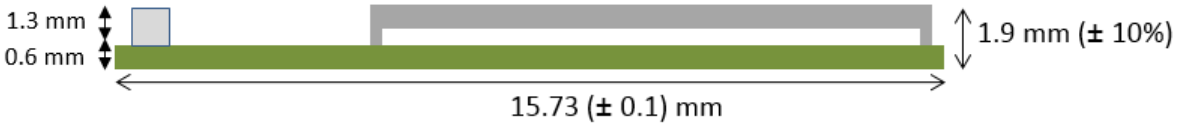


Figure 8.1. BGM113 Dimensions



8.2 BGM113 PCB Land Pattern

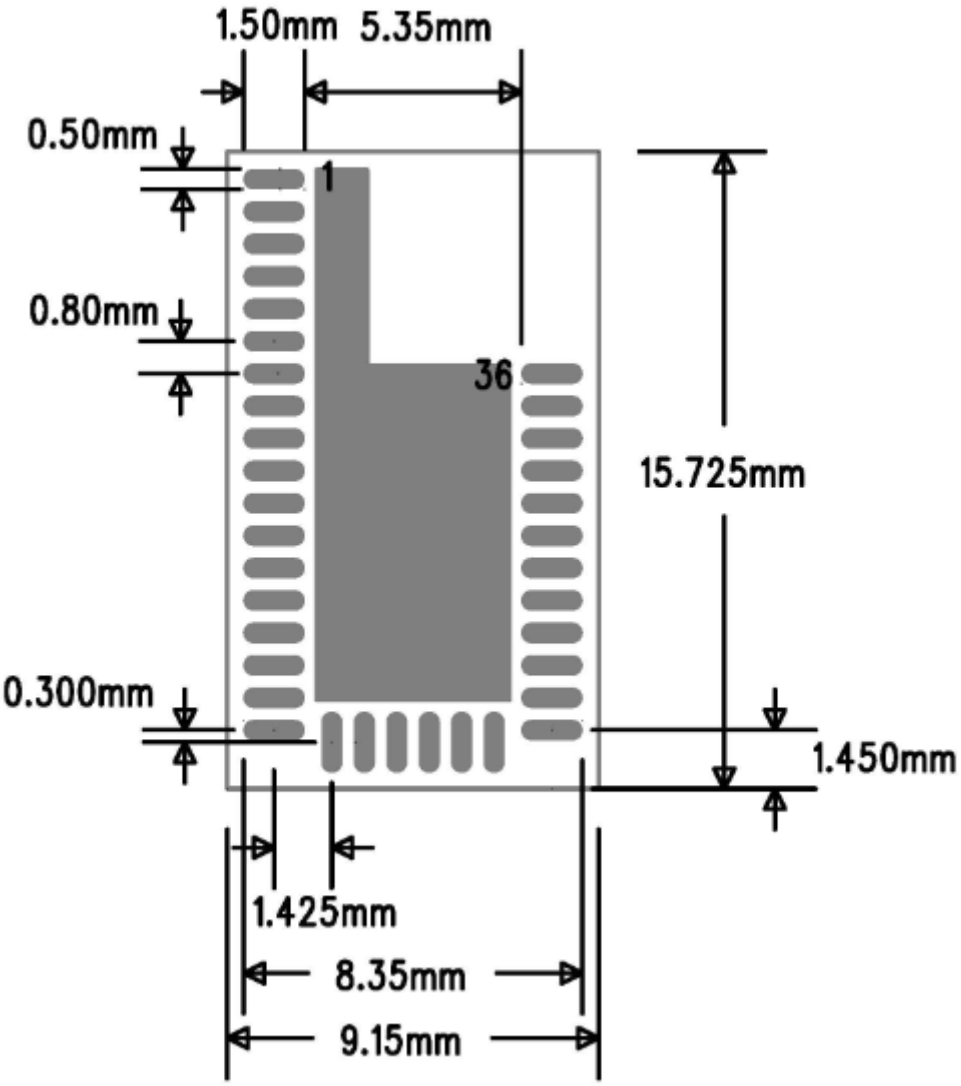


Figure 8.2. BGM113 Land Pattern Drawing

8.3 BGM113 Package Marking

Figure 8.3. BGM113 Initial Production Version Package Marking

The package marking consists of:

- TBD

9. Certifications

9.1 Bluetooth

The Bluetooth certification for the BGM113 is pending.

QDID: TBD

9.2 CE

The BGM113 module is in conformity with the essential requirements and other relevant requirements of the R&TTE Directive (1999/5/EC). This device is compliant with the following standards:

- **Safety**: EN 60950
- **EMC**: EN 301 489
- **Spectrum**: EN 300 328

A formal DoC is available from *www.silabs.com*.

9.3 FCC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmittermeets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures. As long as the condition above is met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

OEM Responsibilities to comply with FCC Regulations

The BGM113 Module has been certified for integration into products only by OEM integrators under the following condition:

- The antenna(s) must be installed such that a minimum separation distance of 0 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

As long as the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).
Note: In the event that this condition cannot be met (for certain configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The BGM113 Module is labeled with its own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ-BGM113"

or

"Contains FCC ID: QOQ-BGM113"

The OEM integrator must not provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

To comply with FCC RF radiation exposure limits for general population, the antenna(s) used for this transmitter must be installed such that a minimum separation distance of 0 mm is maintained between the radiator (antenna) and all persons at all times and must not be co-located or operating in conjunction with any other antenna or transmitter.

9.4 IC

IC (English)

This radio transmitter has been approved by Industry Canada to operate with the embedded chip antenna. Other antenna types are strictly prohibited for use with this device.

This device complies with Industry Canada's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5. BGM113 meets the given requirements when the minimum separation distance to human body 0 mm. RF exposure or SAR evaluation is not required when the separation distance is 0 mm or more. If the separation distance is less than 0 mm the OEM integrator is responsible for evaluating the SAR.

OEM Responsibilities to comply with IC Regulations

The BGM113 Module has been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance of 0 mm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Note: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the IC authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate IC authorization.

End Product Labeling

The BGM113 module is labeled with its own IC ID. If the IC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module IC: 5123A-BGM113"

or

"Contains IC: 5123A-BGM113"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

IC (Francais)

Cet émetteur radio (IC : QOQ-BGM113) a reçu l'approbation d'Industrie Canada pour une exploitation avec l'antenne puce incorporée. Il est strictement interdit d'utiliser d'autres types d'antenne avec cet appareil.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Déclaration relative à l'exposition aux radiofréquences (RF)

Les limites applicables à l'exemption de l'évaluation courante du DAS sont énoncées dans le CNR 102, 5e édition. L'appareil BGM113 répond aux exigences données quand la distance de séparation minimum par rapport au corps humain est inférieure ou égale à 0 mm. L'évaluation de l'exposition aux RF ou du DAS n'est pas requise quand la distance de séparation est de 0 mm ou plus. Si la distance de séparation est inférieure à 0 mm, il incombe à l'intégrateur FEO d'évaluer le DAS.

Responsabilités du FEO ayant trait à la conformité avec les règlements IC

Le Module BGM113 a été certifié pour une intégration dans des produits uniquement par les intégrateurs FEO dans les conditions suivantes:

- La ou les antennes doivent être installées de telle façon qu'une distance de séparation minimum de 0 mm soit maintenue entre le radiateur (antenne) et toute personne à tout moment.
- Le module émetteur ne doit pas être installé au même endroit ou fonctionner conjointement avec toute autre antenne ou émetteur.

Dès lors que les deux conditions ci-dessus sont respectées, d'autres tests de l'émetteur ne sont pas obligatoires. Cependant, il incombe toujours à l'intégrateur FEO de tester la conformité de son produit final vis-à-vis de toute exigence supplémentaire avec ce module installé (par exemple, émissions de dispositifs numériques, exigences relatives aux matériels périphériques PC, etc).

Note: S'il s'avère que ces conditions ne peuvent être respectées (pour certaines configurations ou la colocation avec un autre émetteur), alors l'autorisation IC n'est plus considérée comme valide et l'identifiant IC ne peut plus être employé sur le produit final. Dans ces circonstances, l'intégrateur FEO aura la responsabilité de réévaluer le produit final (y compris l'émetteur) et d'obtenir une autorisation IC distincte.

Étiquetage du produit final

L'étiquette du Module BGM113 porte son propre identifiant IC. Si l'identifiant IC n'est pas visible quand le module est installé à l'intérieur d'un autre appareil, l'extérieur de l'appareil dans lequel le module est installé doit aussi porter une étiquette faisant référence au module qu'il contient. Dans ce cas, une étiquette comportant les informations suivantes doit être collée sur une partie visible du produit final.

"Contient le module émetteur IC: 5123A-BGM113"

or

"Contient IC : 5123A-BGM113"

L'intégrateur FEO doit être conscient de ne pas fournir d'informations à l'utilisateur final permettant d'installer ou de retirer ce module RF ou de changer les paramètres liés aux RF dans le mode d'emploi du produit final.

9.5 Japan

The certification of BGM113 Module in Japan is pending.

Certification number: TBD

Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment can place the certification mark and certification number (the same marking/number as depicted on the label of the radio module) on the outside of the host equipment. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Figure 9.1. Text to be Placed on the Housing of the End-user Device

Translation of the text in the figure above:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

9.6 KC (South-Korea)

The certification of BGM113 in South-Korea is pending.

Certification number: TBD

10. Revision History

10.1 Revision 0.93

2016-03-16
Minor changes.

10.2 Revision 0.92

2016-03-15
Ordering information updated.

10.3 Revision 0.91

2016-03-15

Pinout update. Antenna characteristics and layout guidelines added.

10.4 Revision 0.9

2016-03-14

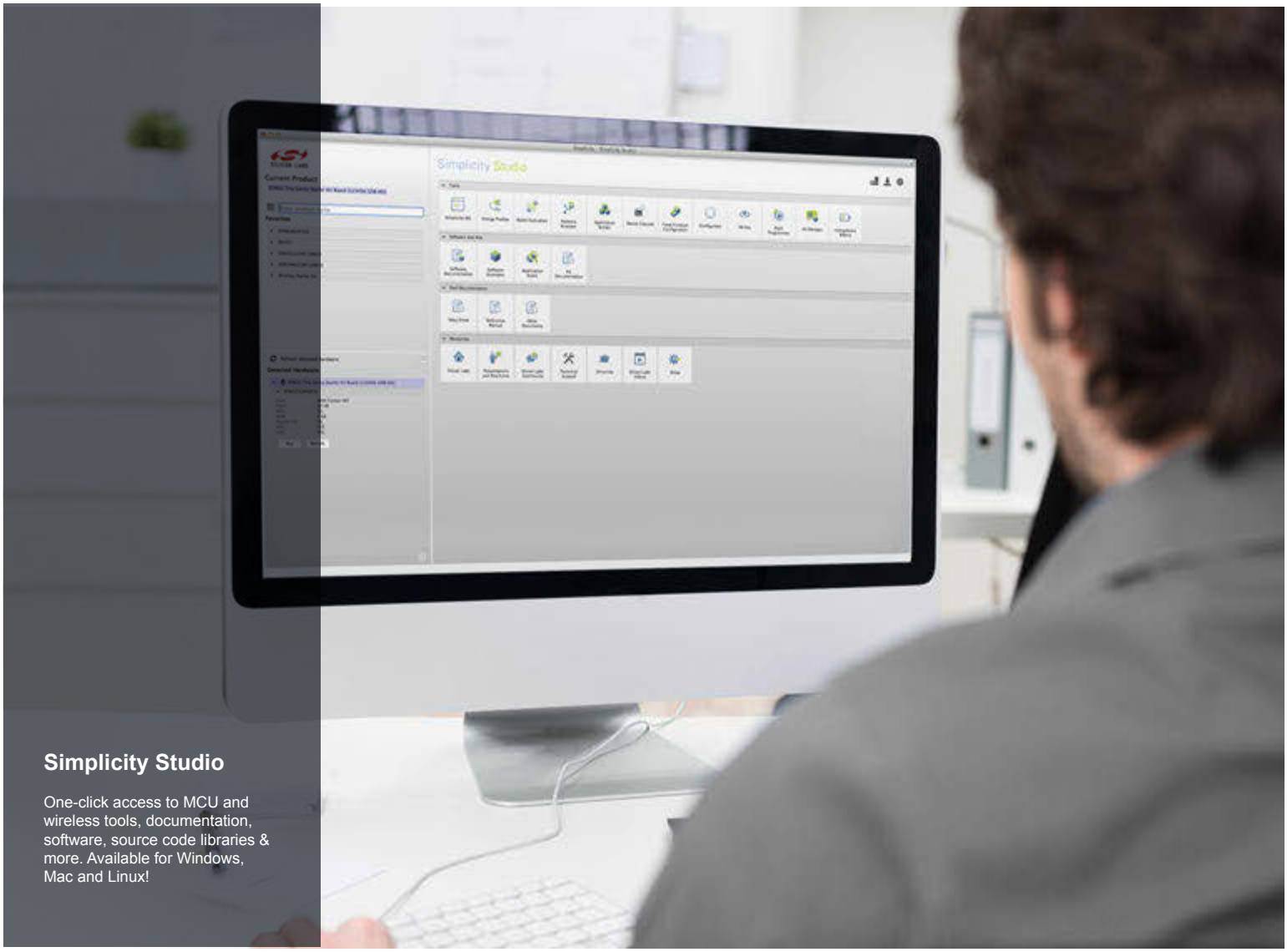
Updated version for initial product release.

10.5 Revision 0.8

2016-03-04
Ready for initial product release.

10.6 Revision 0.7

2016-03-02
Initial version



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