UG395: WFM200 Hardware Design User's Guide

This document provides information to help users design Wi-Fi applications using the WFM200.

KEY FEATURES

- Schematics guidelines
- BOM selection guideline
- Antenna matching guideline
- Layout guideline
- Package information
- Certification guideline

Table of Contents

1. WFM200 Pinout

WFM200 is a 6.5 x 6.5 mm LGA module. The diagram below describes the pinout (top view).

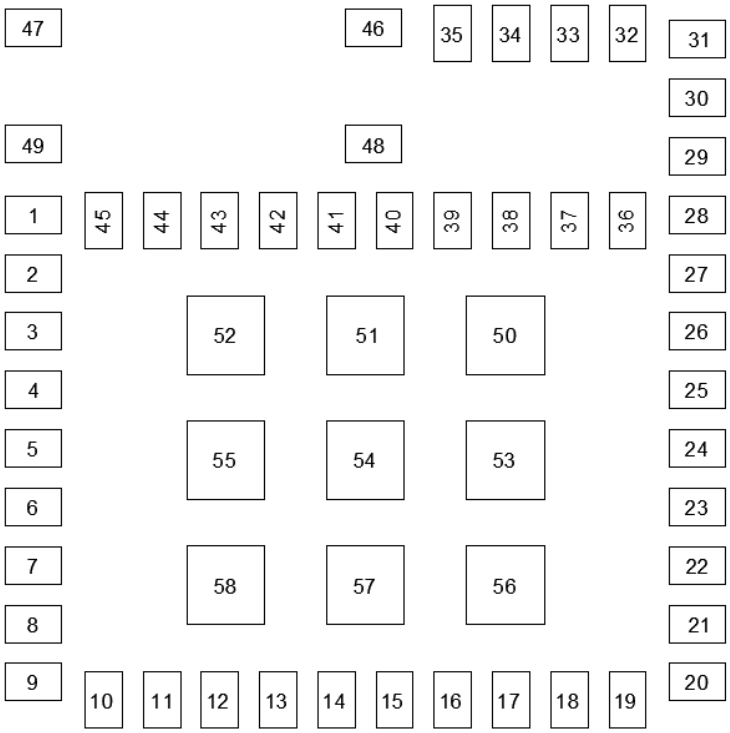


Figure 1.1. WFM200 Pinout

Table 1.1. WFM200 Pin Description

Pin #	WFM200 Pin Name	Description
1	GND	
2	2G4ANT_IN, or No Connect on OPN with no integral antenna	Embedded 2.4 GHz antenna port. To use the antenna, connect this pin to RF_1.
3	RF_1	50 Ω RF_1 input/output port. If not used, this pin should be connected to GND through a 50 Ω resistor.
4, 5, 6, 7, 8	GND	
9	RF_2	50 Ω RF_2 input/output port. If not used, this pin should be connected to GND through a 50 Ω resistor.
10	VDD_PA	Power supply for the power amplifier.
11	GND	
12	RESETn	RESET pin, active Low.
13	GPIO/WUP	This pin can be used to wake-up the device from sleep mode or as a GPIO.
14	GPIO/PTA_TX_CONF	As part of PTA interface, these pins can be used to manage co-existence with another 2.4 GHz radio or can be used as a GPIO.
15	GPIO/PTA_RF_ACT	
16	GPIO/PTA_STATUS	
17	GPIO/PTA_FREQ	

Pin #	WFM200 Pin Name	Description
18	LP_CLK	Low Power clock input. This pin is typically connected to the 32 kHz clock. If not used, the pin should be connected to GND.
19	GPIO/WIRQ	This pin can be used as an IRQ from WFM200 to host to indicate that a message or data should be read or can be used as a GPIO if the WIRQ is done using SDIO_DAT1/SPI_WIRQ.
20	VDD	Power supply for the digital and RF parts.
21	GND	
22	SDIO_CLK/SPI_CLK	Host interface: SDIO_CLK or SPI_CLK.
23	SDIO_CMD/SPI_MOSI	Host interface: SDIO_CMD or SPI_MOSI.
24	SDIO_DAT0/SPI_MISO	Host interface: SDIO_DAT0 or SPI_MISO.
25	SDIO_DAT1/SPI_WIRQ	Host interface: SDIO_DAT1 or WIRQ.
26	SDIO_DAT2/HIF_SEL	Host interface selection: Used to select the host interface during reset rising edge. If Low, selects SPI interface. When High, selects SDIO interface and this pin becomes SDIO_DAT2.
27	SDIO_DAT3/SPI_CSn	Host interface: SDIO_DAT3 or SPI_CSn.
28	VDD_IO	Power supply for I/Os.
29	GPIO/FEM_1	These pins can be used for dynamic control of an external front-end module (FEM); otherwise, they can be used as a GPIO.
30	GPIO/FEM_2	
31	GPIO/FEM_3	
32	GPIO/FEM_4	This pin can be used for dynamic control of an external Power Amplifier; otherwise, this pin can be used as a GPIO.
33	GND	
34	GPIO/FEM_PDET(2)	This pin can be used as an analog input to be connected to a Power Amplifier Vdet output whenever an external Power amplifier or a FEM is used. Otherwise, it can be used as a GPIO.
35, 36	GND	
37	GPIO/FEM_6	These pins can be used for dynamic control of an external front-end module (FEM); otherwise, this can be used as a GPIO.
38	GPIO/FEM_5	
39	RESERVE_1	Reserved. For normal operation, this pin must be grounded.
40	RESERVE_2	Reserved. Leave this pin unconnected.
41, 42, 43, 44, 45, 46,	GND	
47	ANT_LOOP, or No Connect on OPN with no integral antenna	To use the embedded antenna, connect this pin to GND through the antenna loop capacitor.
48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58	GND	

Note:

1. All digital pins (GPIO/xx, host interface pins, RESETn, LP_CLK) are referred to VDD_IO voltage.
2. GPIO/FEM_PDET requires special care because it refers to VDD_IO voltage when configured as a GPIO. However,when configured as FEM_PDET, this pin is an analog input pin with a 0 to 1.2 V range.

2. Device Configuration

The configuration linked to the hardware platform (RF pins, configurable pins, etc.) is achieved through firmware by downloading a dedicated binary file (a PDS file, which stands for "Platform Data Set") just after firmware download and before operation.

More details on device configuration will be provided in an upcoming application note.

Table 2.1. WFM200 Pin Status and Impedance

Pin #	Pin Name	I/O	Configuration	
			Reset[1]	After Boot
3	RF_1	I/O	50 Ω at 2442 MHz	
9	RF_2	I/O	50 Ω at 2442 MHz	
12	RESETn	I	43 kΩ pull-up resistor	
13	GPIO/WUP	I/O	tristate	according to PDS
14	PTA_TX_CONF	I/O	tristate	according to PDS
15	PTA_RF_ACT	I/O	tristate	according to PDS
16	PTA_STATUS	I/O	tristate	according to PDS
17	PTA_FREQ	I/O	tristate	according to PDS
18	LP_CLK	I	no pull resistor	
19	GPIO_WIRQ	I/O	tristate	according to PDS
29	GPIO/FEM_1	I/O	tristate	according to PDS
30	GPIO/FEM_2	I/O	tristate	according to PDS
31	GPIO/FEM_3	I/O	tristate	according to PDS
32	GPIO/FEM_4	I/O	tristate	according to PDS
34	GPIO/FEM_DET	I/O	tristate	according to PDS
37	GPIO/FEM_6	I/O	tristate	according to PDS
38	GPIO/FEM_5	I/O	tristate	according to PDS

Note:

1. All digital I/Os are in tristate except pin LP_CLK, which is configured as input.

3. Features Description

3.1 WFM200 RF Ports

WFM200 has two Tx/Rx RF ports named RF_1 (pin 3) and RF_2 (pin 9). RF_1 and RF_2 have internal low-pass filtering and RF impedance matching components to 50 Ω in the 2.4 GHz band of operation. Any of the RF ports can be used in a similar way. However, note that RF_2 output power is around 1 dB lower than that of RF_1. Several configurations for the RF part are possible, as described below:

- **Single antenna:** For this use case, any RF pin can be used.
- **Antenna diversity without external FEM:** In this case, both RF_1 and RF_2 ports are connected to their respective antennas and, over time, the WFM200 selects the antenna that provides the best budget link to optimize performance, range, and throughput.
- **Use of an external Front-End Module (FEM):** In this case, one port is used for Tx and the other for Rx.

This RF configuration is set with the PDS file.

3.2 Host Interface

The host interface allows control of the WFM200 by an MCU or SoC using either SPI or SDIO. Selection between SPI and SDIO is done upon the logic state on the SDIO_DAT2/HIF_SEL pin during the rising edge of the RESETn signal. If this signal is HIGH, the host interface is configured as SDIO; otherwise, it is configured as SPI. These configurations are summarized in the table below:

Table 3.1. WFM200 Host Interface Configuration

WFM200 Pin Name	SPI Mode		SDIO Mode	
RESETn	0 → 1	1	0 → 1	1
SDIO_DAT2/HIF_SEL	0	x	1	SDIO_DAT2
SDIO_CLK/SPI_CLK	x	SPI_CLK	x	SDIO_CLK
SDIO_CMD/SPI_MOSI	x	SPI_MOSI	x	SDIO_CMD
SDIO_DAT0/SPI_MISO	x	SPI_MISO	x	SDIO_DAT0
SDIO_DAT1/SPI_WIRQ	x	WIRQ	x	SDIO_DAT1
SDIO_DAT3/SPI_CSn	x	SPI_CSn	x	SDIO_DAT3

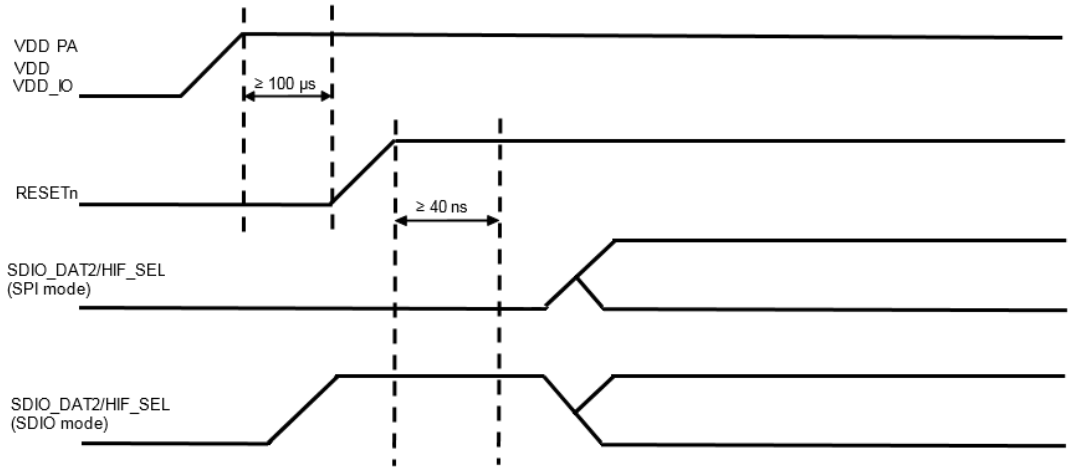


Figure 3.1. WFM200 Power Up and Host Interface Timing Parameters

Besides the host interface main signals, a couple of pins also complement the host interface.

The GPIO/WIRQ pin is programmable and optionally can be used in SDIO mode to provide the interrupt request to the host if a given host does not support in-band IRQ. In SPI mode, the pin can be configured as a copy of SDIO_DAT1/SPI_WIRQ IRQ. The pin can also be used to wake up the host if it is in a power saving mode with the host interface inactive. If this is not required, the pin can be configured as GPIO.

The GPIO/WUP pin should be used by the host to wake up the WFM200 when in power-save mode. This pin is programmable and if power save mode is not enabled on the WFM200, this pin can be configured as a GPIO. Note that this pin should be LOW to enable the WFM200 to reach sleep or shutdown modes.

3.3 Programmable Pins

3.3.1 Multi-Protocol Coexistence

If an RF transceiver using the same 2.4 GHz band (e.g., Bluetooth, Zigbee, or Thread) is located next to the WFM200 Wi-Fi transceiver, a Packet Transfer Arbitration (PTA) interface can be used to minimize mutual interference. In this case, PTA pins are connected to the other transceiver. The PTA interface is highly programmable and can use 1, 2, 3, or 4 pins upon configuration. Because PTA signal names can vary by manufacturer, the table below shows some alternative names.

Table 3.2. PTA Pins

Pin #	WFM200 Pin Name	Potential Alternative Naming
14	PTA_TX_CONF	GRANT, WL_ACTIVE, WL_DENY
15	PTA_RF_ACT	REQUEST, BT_ACTIVE
16	PTA_STATUS	PRIORITY, BT_STATUS
17	PTA_FREQ	FREQ, BT_FREQ

Details on PTA operation will be provided in an upcoming application note.

3.3.2 FEM

FEM pins can be used to control a potential Front-End Module (FEM). The FEM interface is composed of seven pins as described below:

- FEM_PDET is an analog input that is connected to the Tx Power Amplifier detector output for Tx power control. The voltage range on this input is 0 to 1.2 V, which matches most of the power amplifier's detector output.
- FEM_4 is the signal to be used as the power amplifier enable.
- FEM_1 to FEM_3, FEM_5, and FEM_6 are used to dynamically control the FEM during Tx and Rx. All other FEM_x signals are configurable beause of an embedded LookUp Table. This configurability facilitates PCB layout because a given FEM control signal can be generated by any of these pins. The LUT also enables adapting to any FEM control logic. FEM signals can be configured by using the downloaded PDS file.

Available pins can also be configured to monitor the WLAN activity, that is, to drive an LED during Tx and another one during Rx, or a single one during Tx/Rx.

Details regarding FEM control and signals configurations will be provided in an upcoming application note.

3.3.3 Common Features for Programmable Pins

In this section, programmable pins refer to GPIO/FEM_xx pins (7 pins), GPIO/PTA_xx pins (4 pins), GPIO/WUP and GPIO/WIRQ.

Each of these pins has the following features:

- Configurable slew rate to optimize power consumption.
- Programmable pull-up or pull-down. Resistance value for such pull-up or pull-down is 43 kΩ typical.

These features are available whether the pin is used as a GPIO or in “functional” mode and are configured through the PDS file.

3.4 Clocks

The master clock oscillator is embedded in WFM200. It is calibrated in production and temperature compensated in firmware.

Additionally, WFM200 has a provision for a 32 kHz clock input (LP_CLK pin) that allows the lowest power consumption (sleep state) while in power save mode. This clock can be used during sleep mode and should be a square wave with I/O levels complying with I/O pin requirements.

Minimizing battery current between Rx beacons requires frequency drift of LP_CLK within 1 second to be lower than ±100 ppm. Most hosts have 32 kHz that can be shared with WFM200.

If there is no 32 kHz clock provided, this pin should be connected to ground.

4. Power Supplies

WFM200 has three power supply pins.

- VDD_PA supplies the Power amplifier. Recommended to have VDD_PA as the highest supply voltage of WFM200.
- VDD supplies the core, i.e., both RF and digital parts.
- VDD_IO supplies the pins and determines the voltage levels on pins, so this voltage should be compatible with WFM200 peripherals.

Bypass capacitors and filtering are included internally. If DC regulators are not placed sufficiently close to the supply pins to minimize trace inductance and voltage drop, then additional external bypass caps (ceramics) may be required depending on application. Similarly, it is recommended to use external bypass caps and series ferrite beads for supply pins fed by the same supply.

The requirements for these supplies are summarized in the table below:

Table 4.1. Power Supply Requirements

Pin #	WFM200 Pin Name	Min Voltage	Max Voltage	Typical Supply Current
10	VDD_PA	3.0 V	3.6 V	~100 mA
20	VDD	1.62 V	VDD_PA	~40 mA
28	VDD_IO	1.62 V	3.6 V	Upon SPI/SDIO frequency and load

Note: Although VDD_PA is variable, the maximum TX power can be achieved only when VDD_PA is set to 3.3 V minimum. For example, the TX power may be slightly lower if VDD_PA is set to 3.0 V.

There are no specific pin requirements on supplies sequencing except that all supply voltages should be settled at the rising edge of the RESETn pin, as shown in Figure 3.1 WFM200 Power Up and Host Interface Timing Parameters on page 7.

5. Application Schematic Recommendations

5.1 Power Supplies – Schematics

Care should be taken that the VDD_PA supply source is capable of supplying enough current for the load peaks of the power amplifier (which can go momentarily up to 200 mA), so it is recommended to select a regulator capable of supplying 300 mA. The peaks can be very fast, and the power supply for the module should be capable of reacting to load changes within 5 µs.

External high-frequency bypass capacitors are not needed because the module contains the required supply filter capacitors. However, care should be taken to prevent strong switching noise from being superimposed on the supply lines. Such noise can be generated, for example, by the onboard charge pump converters used in RS232 level shifters, in which case it is recommended to place series ferrite and decoupling capacitors with proper SRF at the switching noise frequencies on the supply lines connected. Silicon Labs reference expansion board design with the WFM200 SiP module utilizes a series ferrite with a 10 µF decoupling capacitor between the external power regulator and SiP.

Note that there is a total of about 2.3 µF of low ESR ceramic capacitors inside the module connected directly on the supply input. When using external regulators to generate regulated supplies for the module, the stability of the regulator with the low ESR provided by these capacitors should be checked. Some low-drop linear regulators and some older switched mode regulators are not stable when ceramic output capacitors are used. The data sheet of the regulator typically lists recommendations concerning suitable capacitors, including data on ESR range and/or stability curves. A regulator should include the statement “stable with ceramic capacitors”.

5.2 RF Ports – Schematics

When using the module with the integrated antenna or an antenna external to the module, whether they are connectorized off-the-shelf antennas or PCB trace antennas, antenna impedance must be well matched to 50 Ω to reduce distortion in the module power amplifier because of the impedance mismatch. The matching should be verified in the final enclosure, and it is recommended to reserve SMD placeholders for external antenna tuning.

The suggested external antenna matching structure is a 3-element PI network. The optimum load impedance for each RF port is 50 Ω, so externally, only the antenna matching components may be required.

When using the integrated module antenna (with its required external GND loop trace on the top layer and copper clearance area applied on each layer), the RF_1 port needs to be connected to the 2G4ANT_IN port while externally only a capacitor is required on the antenna loop trace (C_ANT) to the GND.

Unused RF port must be terminated to ground with a resistor between 47 and 51 Ω.

- External antennas used with the Single Modular Transmitter are required to meet these specifications. For reference impedance of 50 Ω, the VSWR must be less than or equal to 2:1 (which is the same as Return Loss higher than 9.5 dB), over the allowed operating frequency range for all operating conditions and production variations.
- The integral antenna on the reference board nominally achieves 18 dB return loss from 2412 MHz to 2462 MHz with reference impedance of 50 Ω. Production tolerance and variations over operating conditions of the main board can degrade this to 12 dB return loss. Production tolerance and variations over operating conditions of WFM200 module can further degrade up to VSWR = 2:1.
- If the hardware design guide is not properly followed, the resulting VSWR may be higher than 2:1 over operating conditions, which would require Tx Output Power to be reduced using PDS file Back Off, and possibly agency approval.

6. Typical Application Schematics

The following diagrams show simple applications using SDIO and SPI interfaces.

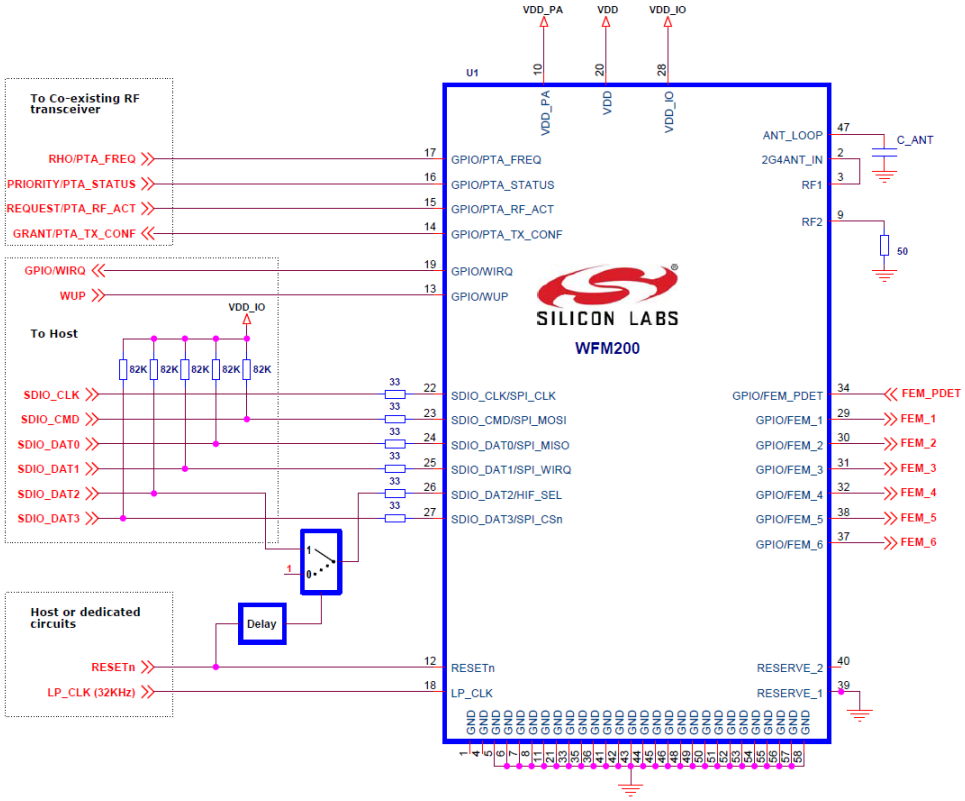


Figure 6.1. Application Using SDIO Interface

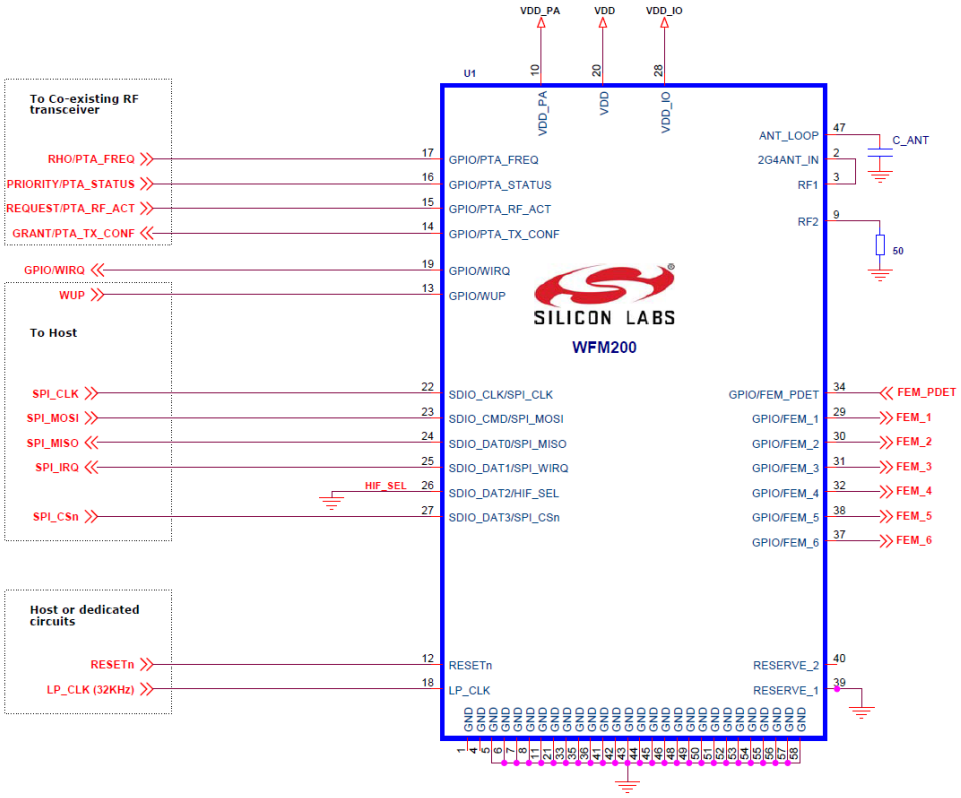


Figure 6.2. Application Using SPI Interface

7. Layout Recommendations

The figure below shows the WFM200 section of Silicon Labs' reference board layout with some feature highlights.

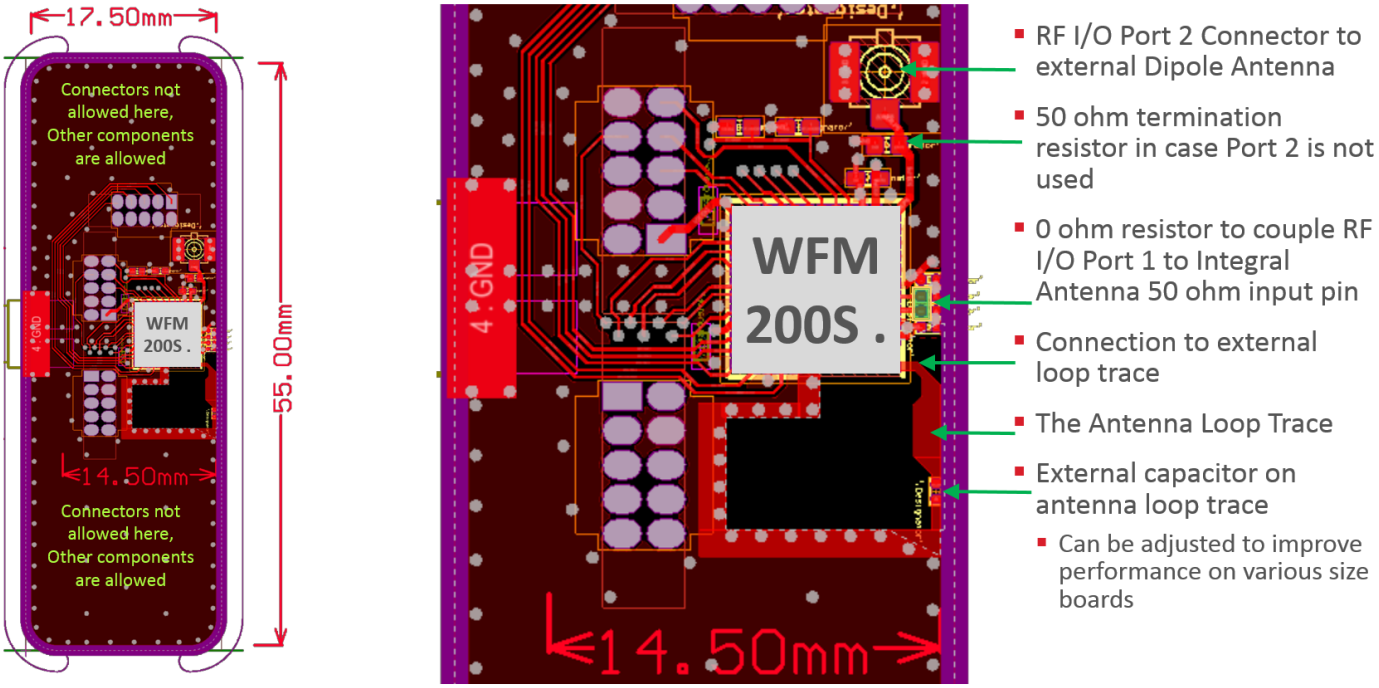


Figure 7.1. WFM200 Portion of Reference Design Board Layout

7.1 Generic RF Layout Considerations

For custom designs, use the same number of PCB layers as are present in the reference design. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the antenna matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required. The Silicon Labs development kit uses a 1.6 mm thick FR-4 PCB with the board stack-up detailed in the figure below.

For best performance, use the following guidelines for custom layout designs:

- Use as much continuous and unified ground plane metallization as possible, especially on the top and bottom layers.
- Use as many ground stitching vias as possible, especially near the GND pins, to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.
- Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10th harmonic (the typical distance between vias on a reference design is 1 mm). This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.
- For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers, while keeping the GND pour metallization unbroken beneath the RF areas (between the antenna, matching network, and module). To benefit from parasitic decoupling capacitance, the inner layer can be used to route the power supply with a wide VDD_PA sub-plane and traces to increase parasitic capacitance with nearby ground layers.
- Avoid using long and/or thin transmission lines to connect the RF-related components. Otherwise, because of their distributed parasitic inductance, some detuning effects can occur. Also, shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discrete components may increase in this way.
- Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.
- To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good supply filtering. Any gap on each PCB layer should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. Because of the layout restrictions, such as traces routed on other layers or components on the bottom side, vias are not used on the entire GND section.
- Use tapered lines between transmission lines with different widths (i.e., different impedances) to reduce internal reflections.
- Avoid using loops and long wires to obviate their resonances. They also result in unwanted radiation, especially at the harmonics.
- Avoid routing GPIO lines close or beneath the RF lines, antenna, or crystal, or in parallel with a crystal signal. Use the lowest slew rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.
- Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the supply traces, to reduce their harmonic radiation caused by the fringing field.

```
BOARD THICKNESS    : 1.6 mm +/-10%
NO OF LAYERS       : 4
MATERIAL(S)        : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C
                     Materials in compliance with the RoHS and WEEE directives
MARKINGS           : Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))
                     (Avoid areas reserved for DataMatrix, Barcodes or Lables)
                     All PCB manufacturerÆs markings (Logo, Week/Year, UL)
                     shall be put in the PCB frame. No marking on the boards
                     is allowed
QUALITY REQ.       : IPC-A-600 (current revisions) Class 2, and IPC specifications
                     refered to by IPC-A-600
GENERAL REQ.       : - Copper must not be added or removed from inside the board
                       outline(s), without written consent/approval.
                     Use the balancing of the panel that comes with the
                     Gerber files (without alterations)
                     If applicable, the following requirements are valid:
                     - If Build-Up (Stack-Up) is specified, follow Build-Up,
                       otherwise use (board manufacturer) standard Build-Up.
                     - Break-away areas may be used for patterns, holes etc.
                       by manufacturer for QA purposes.
                     - If V-CUT, use angle 30 +/- 5 degrees.
                       V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
                       Use of V-CUT test pads is allowed.
                     - Inner radius (contour/outline) 1.2 mm, unless stated
                       otherwise.
COPPER THK.        : SEE BUILD-UP
COPPER PASSIV.     : ENIG to meet IPC-4552 requirements (current revision)
                     (Electroless Nickel/Immersion Gold)
RESIST MASK        : Solder Mask Color: BLACK (NBI NON-STANDARD)
                     Photo Polymer Wet film
                     to IPC-SM-840 Class T requirements (current revision)
                     Thickness minimum 8 um, maximum 20 um
VIA HOLES          : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
                     Plugged and Covered Both Sides, Low CTE Plugging Paste
                     If Type IV-b is not available as a process, then Type IV-a
                     for the Top Side, and Overprinted (Tented) Bot Side is OK
LEGEND/SILKSCR.    : WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP     : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!
                     Unless explicitly stated otherwise, controlled impedance
                     has been designed into the board. Use of test strip is
                     hence normally not required.
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE)    : Minimum conductor width      : 0.125 mm (5 mils)
Cu TRACK(TRACE)    : Minimum conductor spacing    : 0.125 mm (5 mils)
MINIMUM VIA        : Minimum via pad diameter     : 0.5 mm ( 20 mils)
                     Minimum via hole diameter    : 0.25 mm (10 mils)
                     Min via hole may have more than one pad diameter.

BUILD UP           :
                     L1  ==== | |========================== 38 um Cu (ca) After plating
                        ///// | |/////// PREPREG //////// 300 um *)
                     L2 ===== | |========================== 18 um Cu (0.5 Oz)
                        - - - | | - - - - - CORE - - - - -  **)
                     L3 ===== | |========================== 18 um Cu (0.5 Oz)
                        ///// | |/////// PREPREG ////////
                     L4 ====  | |========================== 38 um Cu (ca) After plating

                     *)
                     The distance from bottom of L1 to top of L2 should be
                     as close to 300 um as possible!

                     **)
                     Select Core and Prepreg thickness in order to reach specified
                     board thickness


TEST               : 100% Electrical Test
                       Optical test, AOI (with automatic scanner)
                       Visual inspection
                       (Generate netlist from Gerber and Drill files)

                       Avoid use of 2125 Prepreg

                       If NBI is used in this specification, it means:
                       abbreviation for nota bene!, a Latin expression meaning
                       note well!


-------------------------------------------------------------------------------
NC DRILL - HOLE INFORMATION:
WARNING    : Drill dimensions must be taken from the Excellon (.DRL) file(s), and
             the drill report file(s) (.DRR).
             NON-PLATED holes may have a small center marker in the Gerber files.
             Under no circumstance must these Gerber flashes be mistaken for the
             hole drill dimensions!
The drill data may contain slots (in a separate file).
Dimensions for the finished board (after plating).
Tolerances +/- 0.1 mm, unless specified differently.
Via Holes +0.05 mm/-Via Size, unless specified differently.
```

Figure 7.2. Reference Design PCB Specification

7.2 GND and RF Pads Including the Diversity Port and External Antennas

WFM200 ground pads need to be well connected to the PCB ground plane to optimize thermal conductivity and prevent unwanted emissions that result from ground currents.

The RF pads and RF traces conducting the RF signal should be dimensioned to have a characteristic impedance of 50 Ω. It is vital that proper RF design principles be used when designing an application using the RF pads.

Antennas external to the module, be they connectorized, off-the-shelf antennas or PCB trace antennas, must be well-matched to 50 Ω. PCB size and layout recommendations from the antenna manufacturer must be followed. Board size, ground plane size, plastic enclosures, metal shielding, and components in close proximity to the antenna can affect the antenna impedance and radiation pattern. Therefore, antenna matching should be verified in the final enclosure. See Section 5.2 for antenna specifications.

Ensuring proper antenna impedance matching is also recommended to prevent distortion in the module power amplifier because of the impedance mismatch. PA distortion can cause significant packet loss and poor overall performance.

7.3 Module Antenna

To minimize impedance detuning and degradation of the radiation pattern, reduce as much shielding of the selected antenna as possible.

The ground plane usually forms an important part of the antenna as there is significant current running along the ground plane (i.e., the GND plane is also part of any monopole-type antenna, in general). For optimal performance when using an integral antenna, ensure that the PCB size is at least 55 mm (± 3mm) in width and follow the layout recommendations for the different host PCB sizes as detailed in this section. These layout drawing solutions are patented by Silicon Labs.

For optimal performance of the WFM200 module antenna, follow these generic guidelines:

- Place the module at the edge of the carrier PCB where the centers of pins 1, 47, and 49 are 1.8 mm away from the metal edge of the PCB.
- Do not place any metal (traces, components, etc.) in the antenna clearance area. This keep-out applies on each layer. The form and dimensions of the antenna clearance area are shown in Section 10 of this document.
- Connect all ground pads directly to a solid ground plane and place the ground stitching vias close to the ground pads. The recommended GND via stitching placement for WFM200 is shown in Figure 7.3 Grounding and Via Stitching of WFM200 Part on page 17.
- Using size, thickness, or permittivity for the main board other than optimum requires tuning and testing to re-optimize antenna loop trace capacitor value (C_ANT). The default capacitor value is C_ANT = 0.9 pF in an SMD0201 package.
- Additionally, a series-matching capacitor/inductor between the 2G4ANT_IN and RF_1 ports can also be utilized for fine impedance tuning (C_SER). The default configuration of C_SER is a 0 Ω jumper as shown in Figure 7.1 WFM200 Portion of Reference Design Board Layout on page 13 above.
- The area occupied by WFM200, its required loop trace, and keep-out is 8.5 mm x 13.5 mm = 115 mm^2. The rest of the required area can have components and traces which are surrounded by GND fill, especially 1 mm wide around the perimeter of the placement areas, which amounts to 120 mm^2.
- There can be no cable connections within the required area during TX operation except for the UFL connector for the second RF I/O port in the location shown just north of WFM200 and away from the edge (refer to the figure below). The co-ax cable must exit the northern placement area over the allowed GND bridge or routing area between the WFM200 required board portion and the rest of the main board portion.
- Any digital component added to the loop side and supply side could degrade WFM200 sensitivity because of signal harmonics falling into Wi-Fi band. To get lower than 0.5 dB desensitization, the radiated level of CW interference measured at pin 2G4ANT_IN should be less than -108 dBm. To get lower than 3 dB desensitization, the level of AWGN-like interference measured at pin 2G4ANT_IN in channel bandwidth should be less than -94 dBm.

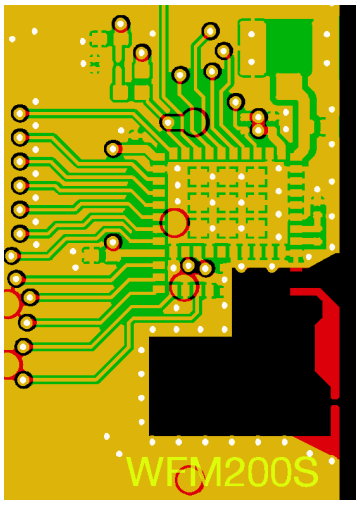


Figure 7.3. Grounding and Via Stitching of WFM200 Part

7.3.1 Small Board Size Recommendations for Good RF Performance

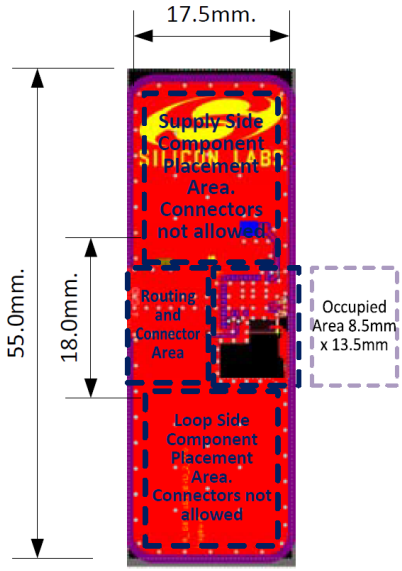


Figure 7.4. Reference Design for Small PCB Sizes

Note: Spaces filled in black represent metal keep-outs on the PCB in the figure above.

- Required WFM200 Board size in X = 17.5 mm ± 3 mm of metal.
- Required WFM200 Board size in Y = 55 mm ± 3 mm of metal.
- PCB may be slightly larger to account for PCB edge routing.
- Area for optimum performance is 55 mm z 17.5 mm = 963 mm^2
- The recommended board width is Y= 55 mm. Board widths up to Y= 65 mm still meet regulatory certifications but will result slightly degraded RF performance.
- Board size smaller than 17.5 mm x 55 mm will have lower antenna efficiency, more variation in return loss, and may require TX power to be reduced to meet RF performance specifications.
- If the carrier board width Y < 45 mm, then better RF performance can be achieved if the WFM200 module is shifted to the north, i.e., ensure larger (close to 22.5 mm) PCB metal width on the antenna clearance area side of WFM200. Otherwise, center pins 49 and 48 vertically.
- The center of pin 49 is 1.8 mm from the metal edge.
- Connectors are only allowed in the middle 18 mm adjacent to the occupied area.
- Components may be placed north and south of occupied area.
- The PCB must have continuous GND fill around the edge inboard to at least 1.8 mm with the exception of the occupied area as shown.
- Cables must exit from the connector area directly away from the designated occupied area.

7.3.2 Extended X Dimension Recommendation for Good RF Performance

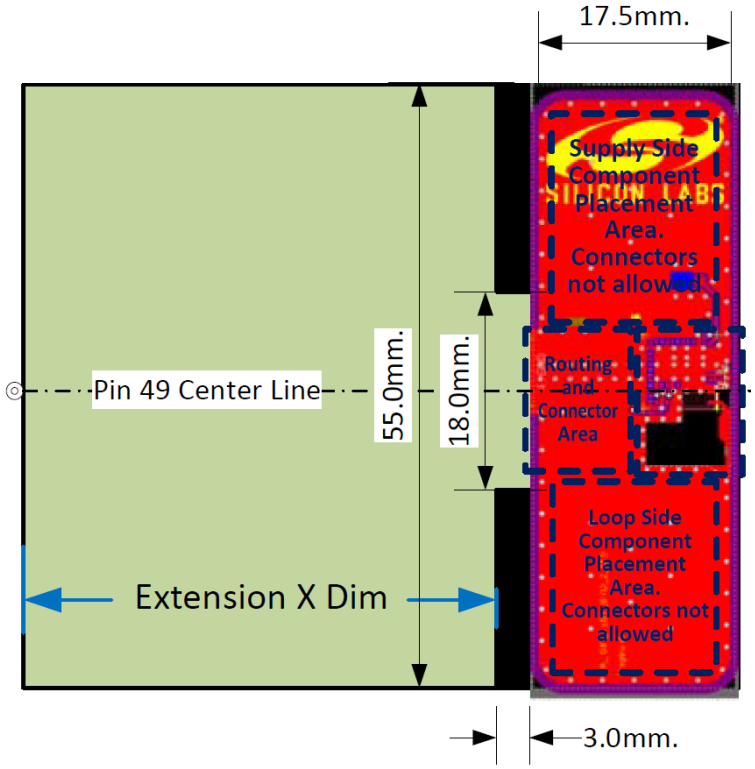


Figure 7.5. Reference Design for Extended X-dimensioned PCB Sizes*

Note: Spaces filled in black represent metal keep-outs on the PCB in the figure above.*

- Required WFM200 portion size is X = 17.5 mm of metal.
- Required board size is Y = 55mm ± 3 mm of metal.
- PCB may be slightly larger to account for PCB edge routing.
- The recommended board width is Y = 55 mm. Board widths up to Y = 65 mm still meet regulatory certifications but will result in slightly degraded RF performance.
- Board width (Y) smaller than 55 mm will have lower antenna efficiency, more variation in return loss, and may require TX power to be reduced to meet RF performance specifications.
- If the carrier board width Y < 45 mm, then better RF performance can be achieved if the WFM200 module is shifted to north, i.e., ensure larger (close to 22.5 mm) PCB metal width on the antenna clearance area side of WFM200. Otherwise, center pins 49 and 48 vertically.
- Add 3 mm wide keep-outs adjacent to the designated component placement areas near WFM200, which allows only an 18 mm wide bridge of GND and signal routing area between the two PCB portions.
- The extension in X dimension can be any length.
- The center of pin 49 is 1.8 mm from the metal edge.
- Connectors are only allowed in the X dimension extension portion.
- Components may be placed north and south of the occupied area, but these must be surrounded by GND to the edge of the placement areas.

7.3.3 Y Dimension (65 to 80 mm) Recommendation for Good RF Performance

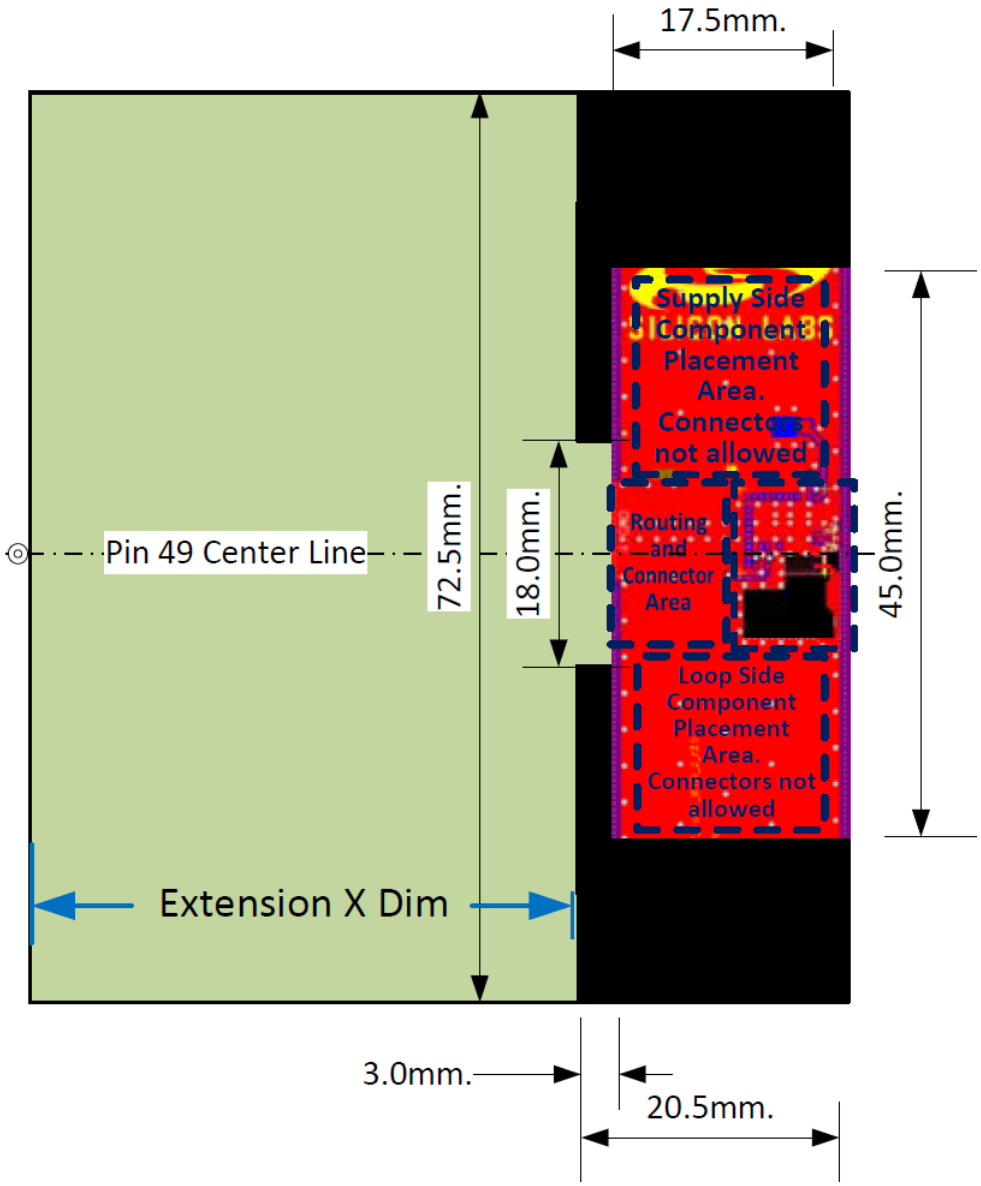


Figure 7.6. Reference Design for Extended X- and Slightly Extended Y-dimensioned PCB Sizes*

Note: Spaces filled in black represent metal keep-outs on the PCB in the figure above.*

- Add 3 mm wide keep-outs adjacent to the designated Component Placement Areas near the WFM200, which allows only an 18 mm wide bridge of GND and signal routing area between the two PCB portions.
- The 20.5 mm corners beyond the placement areas must be metal keep-outs.
- PCB may be slightly larger to account for PCB edge routing.
- Main portion of the PCB X dimension can be any length.
- Main portion of PCB Y dimension can be any length over 65 mm.
- WF(M)200S portion of board X dimension is 17.5 mm +/-3 mm.
- WF(M)200S portion of board Y dimension is 45 mm to 55 mm.
- Pins 49 and 48 are to be centered vertically, and center of Pin 49 is 1.8 mm from metal edge.
- Connectors are only allowed in the Extension X dimension portion away from WFM200.
- Components may be placed north and south of the occupied area, but only within the designated component placement areas. Also, these must be surrounded by GND to the edge of the placement areas.

7.3.4 Y Dimension (80 mm or Larger) Recommendation for Good RF Performance

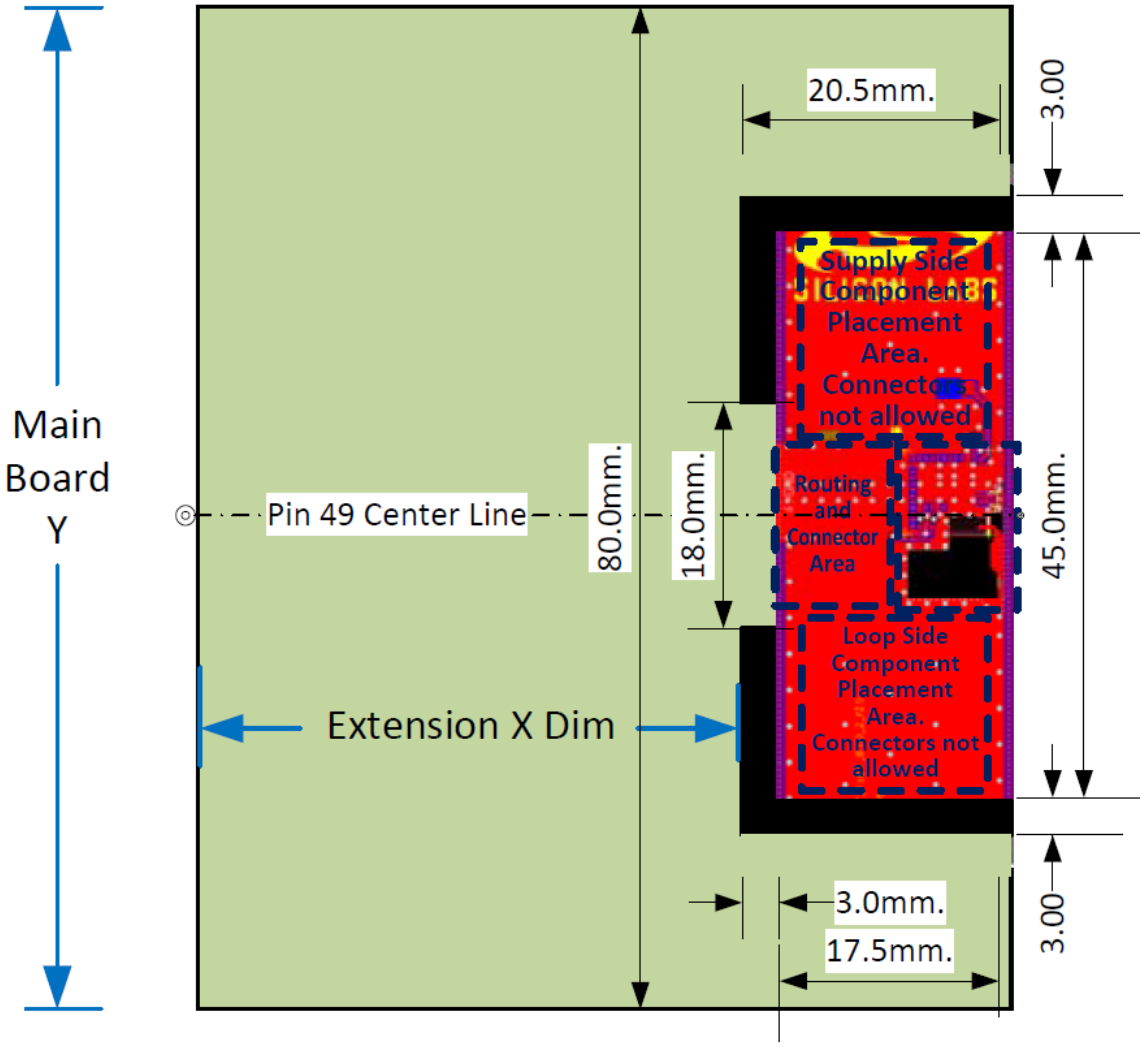


Figure 7.7. Reference Design for Extended X- and Y-dimensioned PCB Sizes*

Note: Spaces filled in black represent metal keep-outs on the PCB in the figure above.*

- WFM200 PCB portion size is X = 17.5 mm and Y= 45 mm of metal.
- PCB may be slightly larger to account for PCB edge routing.
- Main portion of PCB X dimension can be any length.
- The Y dimension of PCB may be of any length, however, 3 mm metal keep-outs must be placed as shown. There must only be an 18 mm x 3 mm area where traces and GND fill can bridge between the two portions of the PCB.
- Pins 49 and 48 are to be centered vertically, and the center of pin 49 is 1.8 mm from metal edge.
- Connectors are allowed in the extension X dimension portion away from WFM200.
- If connectors are placed in the 17.5 mm corners north or south of the designated component placement areas, testing must be performed with cables in place to assure good RF performance.
- Components may be placed in the component placement areas, and north and south of these areas beyond the 3 mm metal keep-out gap.
- Component placement areas must have GND surrounding them to the edge of the placement areas.

7.3.5 WFM200 Portion One Corner Bias with 3 mm Metal Keep-Outs

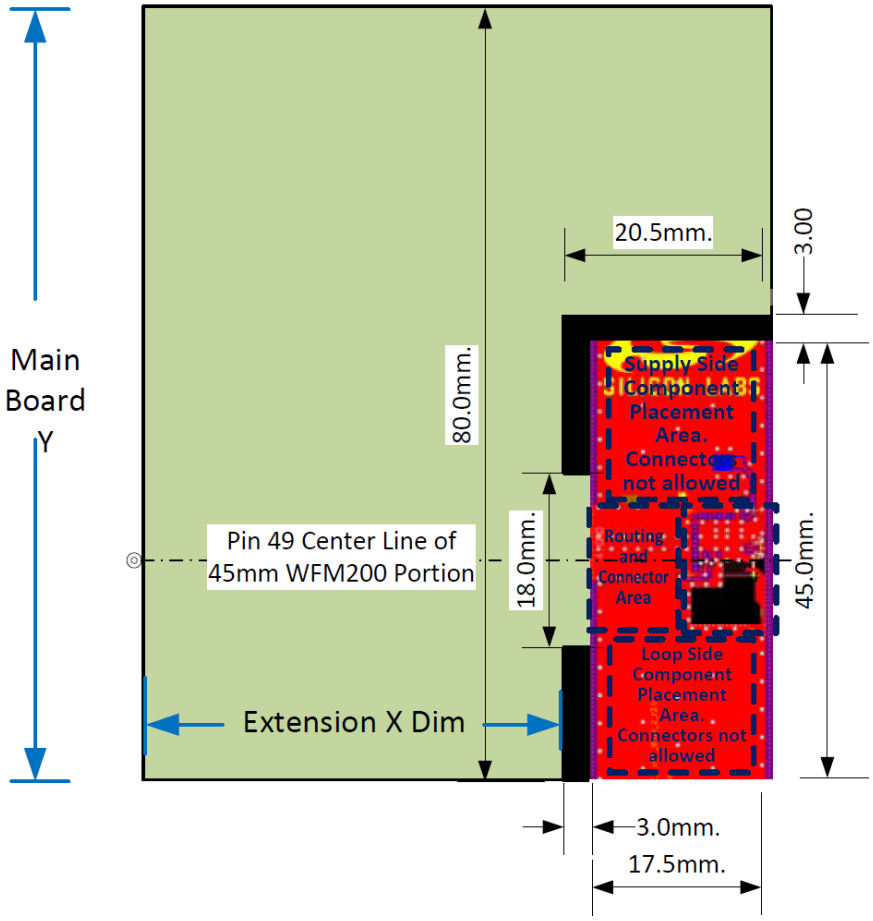


Figure 7.8. Reference Design for Extended X- and Y-dimensioned PCB Sizes with WFM200 Portion in Corner*

Note: Spaces filled in black represent metal keep-outs on the PCB in the figure above.*

If the available metallization size of WFM200 section is equal to or smaller than 15 mm x 35 mm on a space-restricted design, then better performance can be achieved when the metal keep-out gap is set to 1 mm. Also, shift the WFM200 module to north to ensure close to 22.5 mm PCB metal width on the antenna loop side of the WFM200. The center of pin 49 is 1.8 mm from the metal edge.

7.3.6 Recommended Antenna Loop Trace Capacitor Values

This sections provides guidelines for antenna matching component values for various board sizes. System integrators should verify the antenna impedance in their full application with all housings and connections attached and mounted. The antenna matching component values can be adjusted to achieve Max VSWR of 2:1 in the actual application. As the board size is reduced, the antenna gain also reduces, and it becomes more important to adjust these component values to meet 2:1 max VSWR.

Table 7.1. Recommended BOM vs. PCB Size

Carrier PCB Dimensions		Size of WFM200 Section		C_ANT [pF]	C_SER	Antenna Realized Gain Typ. [dBi]	Notes
X [mm]	Y [mm]	X [mm]	Y [mm]				
17.5	55	17.5	55	0.9	0 Ω	+2.5	Small PCB size as shown in Figure 7.4 on page 18
14.5	55	14.5	55	0.9	0 Ω	+2.4	
20.5	55	20.5	55	0.8	0 Ω	+2.2	
17.5	45	17.5	45	0.7	0 Ω	+2.2	
27	45	27	45	0.7	0 Ω	+2.0	
17.5	65	17.5	65	0.8	0 Ω	+2.0	
14	42	14	42	0.8	4.3 nH	+1.0	
100	55	28	55	0.8	0 Ω	+2.8	Extended X-dimension PCB size as shown in Figure 7.5 on page 19
100	45	17.5	45	0.6	0 Ω	+1.2	
100	65	17.5	65	0.9	0 Ω	+3.3	
85	55	17.5	55	0.8	0 Ω	+2.8	
100	65	21.5	55	0.7	1.8 pF	+4.0	Maximum gain is +4.7 dBi. Configured as shown in Figure 7.5 on page 19
75	75	17.5	45	0.6	0 Ω	+2.1	Extended PCB size as shown in Figure 7.6 on page 20
35	100	17.5	45	0.8	0 Ω	+2.4	Extended PCB size as shown in Figure 7.7 on page 21
75	100	17.5	45	0.8	0 Ω	+3.7	
100	100	17.5	45	0.8	0 Ω	+2.2	
200	100	17.5	45	0.8	0 Ω	+3.7	
75	80	17.5	45	0.8	0 Ω	+3.6	
75	120	17.5	45	0.8	0 Ω	+3.7	
75	150	17.5	45	0.8	0 Ω	+2.0	
75	200	17.5	45	0.8	0 Ω	+2.5	
200	200	17.5	45	0.8	0 Ω	+2.8	
110	140	15	30	0.6	1.0 pF	+0.3	Ext. PCB size, in corner, as shown in Figure 7.8 on page 22

Note:

1. C_SER can be a series tuning capacitor [pF] / inductor [nH] option mounted between the 2G4ANT_IN and RF_1 ports for carrier boards with small GND metallization size. C_ANT is the antenna loop trace capacitor.
2. Using FR-4 Carrier PCB with a relative permittivity of $\varepsilon_r = 4.4 \pm 10\%$
3. The recommended component values provided in this table might need to be optimized on a custom design within its final enclosure by measuring S11 at pin 2G4ANT_IN to ensure VSWR antenna requirements are met.

7.4 WFM200 Reference Evaluation Board

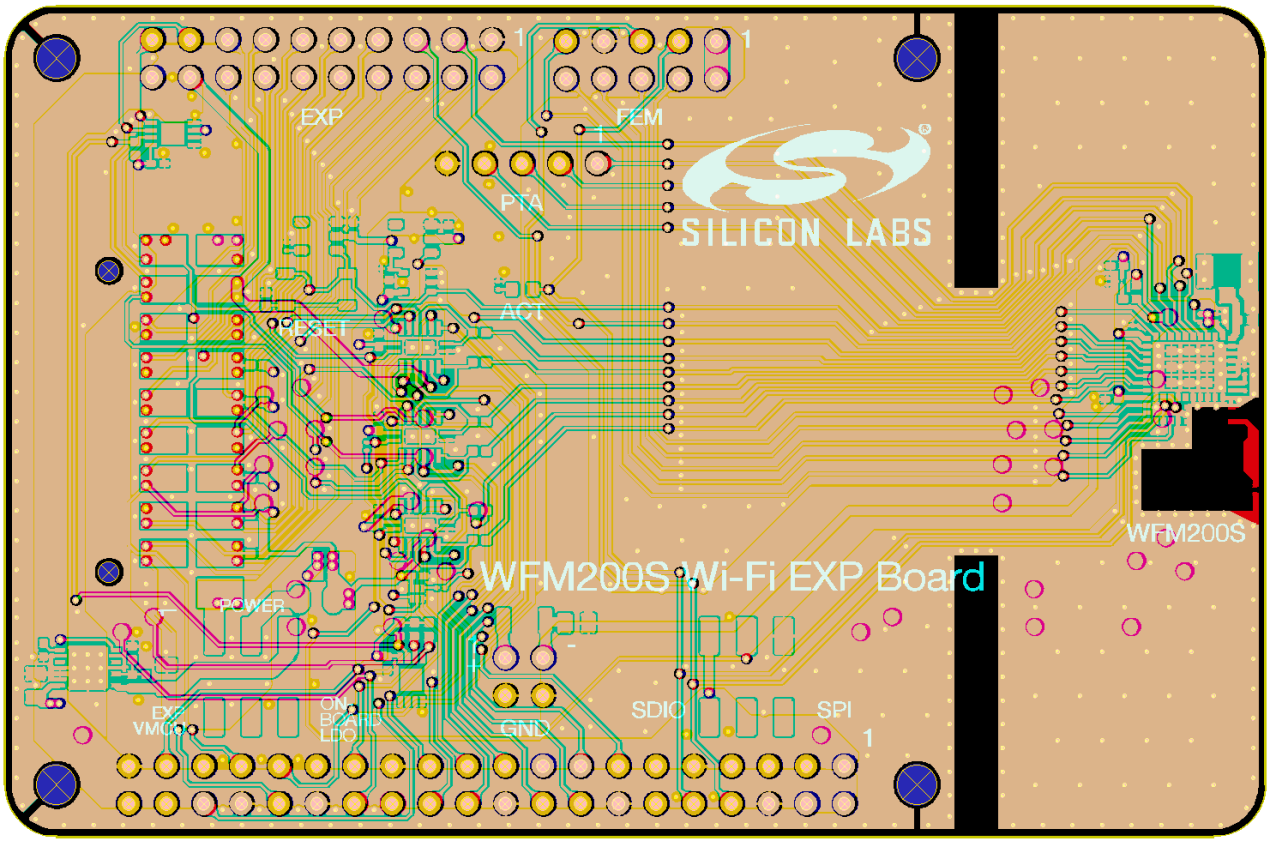


Figure 7.9. WFM200 Evaluation Board Design with Expansion Header

The carrier board size is 84 mm x 55 mm. The WFM200 section has a metallization of 17.5 mm x 55 mm.

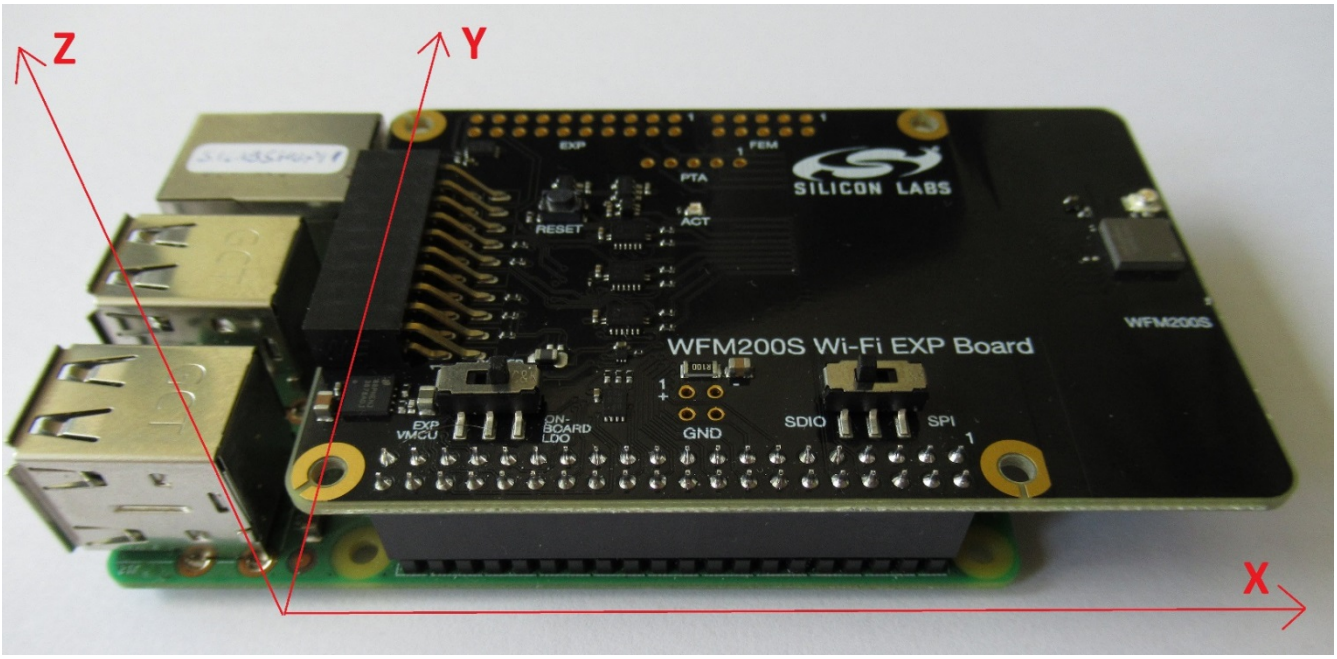


Figure 7.10. WFM200 Evaluation Board with Raspberry PI Connected and Reference Coordinates

The following two-dimensional radiation pattern plots have been measured on the BRD8023A evaluation board using the integrated module antenna and being connected together with the Raspberry Pi:

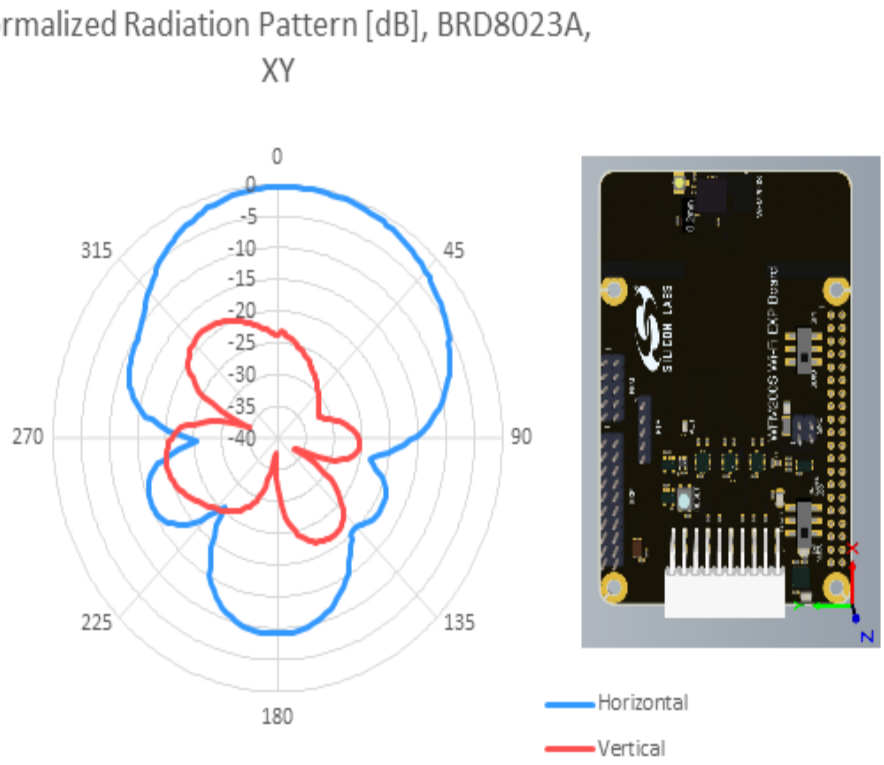


Figure 7.11. 2D Radiation Pattern of WFM200 Evaluation Board – Top View

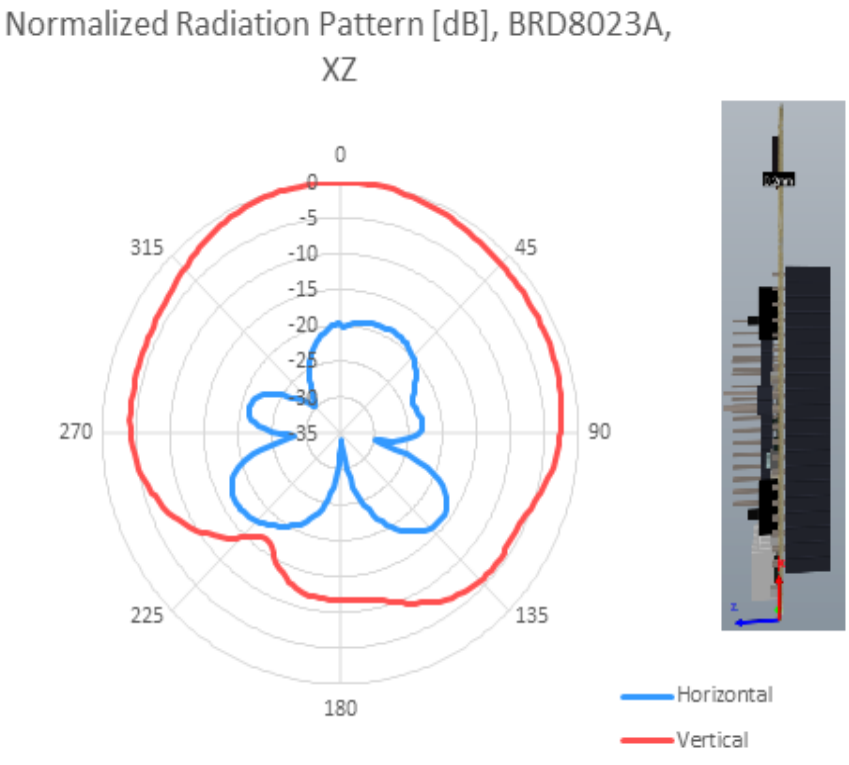


Figure 7.12. 2D Radiation Pattern of WFM200 Evaluation Board – Side View

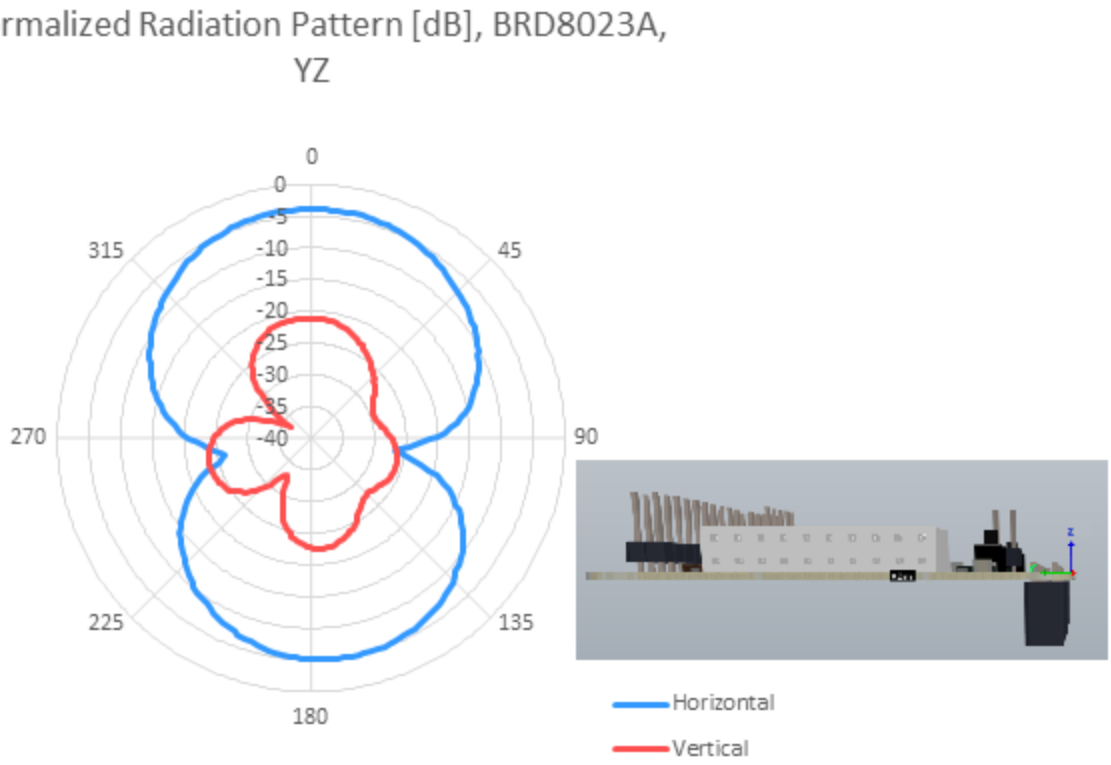


Figure 7.13. 2D Radiation Pattern of WFM200 Evaluation Board – Rear View

Note: The X and Y axis are in the PCB plane cut as shown in the previous section, while the Z axis is orthogonal to the PCB. The typical antenna gain is +3.0 dBi and the antenna efficiency is -1 dB (= ~80%).

8. Recommendations for Certification

This section provides additional information on the certification details already provided in the WFM200 data sheet.

WFM200 embeds TX power backoffs for 2:1 VSWR on its RF ports and is certified with an external connectorized coaxial dipole antenna and an integrated module antenna.

Except for minor cosmetic changes, most changes to an FCC certified equipment require testing to determine whether the change is a Class I or Class II permissive change.

For more details about using the Single Modular Transmitter, such as WFM200, refer to the following FCC documents:

- KDB 996369 D01 Transmitter Module Equipment Authorization Guide
- KDB 996369 D02 Frequently Asked Questions and Answers about Modules
- KDB 178919 D01 Permissive Change Policy
- KDB 178919 D02 Permissive Change Frequently-Asked Questions

Certification was performed with:

- Linux driver 2.2.4
- WLAN firmware FW3.0.1

8.1 Qualified External Antenna Type

The WFM200 SiP module has been certified in multiple regions and is designed to operate with a connectorized whip dipole antenna type with a reference impedance of 50 Ω. FCC certification is restricted to external antennas of this type. The maximum antenna gain is +4.7 dBi. System integrators must comply with all regulatory agency requirements for the applicable regions including FCC, IC, and CE, especially those governing antennas used with this module.

Table 8.1. Certified and Approved External Antennas and Board Sizes

External Antenna Type	Specification for max. VSWR	Specified Max. Gain [dBi]	Notes
Connectorized Whip Dipole	2:1	+4.7	Straight or 90 degrees bent W1038 antenna, or similar type

8.2 Certified Module Antenna

The WFM200 SiP module has also been certified and designed to operate with the integrated module antenna. When using the module antenna, customer designs should ensure that the layout recommendations are carefully being followed as described in the previous sections in this document. The maximum module antenna gain with an appropriate carrier board size and proper layout design is +4.7 dBi with a maximum VSWR of 2:1 across frequency band 2412-2462 MHz. The antenna total radiation efficiency is about -1 dB (= ~80%).

Customer designs which do not follow this hardware guideline may not meet Max VSWR over production part-to-part variation and/or across the Wi-Fi frequency band of interest. The customer should configure additional backoffs within the PDS for the worst-case VSWR achievable by the design. To reduce the probability of needing to configure such additional backoffs, use the BOM and PCB ground antenna area sizes as discussed in Section 7.3. Module Antenna.

Certified and approved board sizes and BOM are provided in the table below.

Table 8.2. Certification Board Dimensions and BOM with Integral on-Module Antenna

Carrier PCB Dimensions		Size of WFM200 Section		C_ANT [pF]	C_SER [pF]	Antenna Realized Gain Max. [dBi]
X [mm]	Y [mm]	X [mm]	Y [mm]			
100 ± 3	65 ± 3	21.5	55	0.7	1.8	+4.7

Note:

1. Using an FR-4 host board PCB with a relative permittivity of ε_r = 4.4 ± 10%.

This device is certified based on the board size with the maximum antenna gain (100 mm x 65 mm overall, and 55 mm x 21.5 mm WFM200S portion) and the two external components for the loop antenna, which have values optimized to minimize mismatch loss. Although this board size is valid to use, the recommended board size (55 mm x 17.5 mm) with the recommend nominal component values results in a smaller overall solution size and allows for a wider range of board size and production variations.

8.3 CE Certification Requirements

The Certification in CE Regions requires lower TX Power for the 1 Mbps and 2 Mbps 802.11b modulations. The amount of power reduction is based on the actual Max Gain specification of the Antenna used in the application. When the antenna gain reduces by 0.25 dB, the application may use 0.25 dB higher power settings for these two modulations. Use the PDS file for this purpose. The two affected modulations are in Mod_Group_0. This section provides the minimum amount of TX Power Back Off necessary in the PDS file for Mod_Group_0 for specific channels, for a given Antenna Max Gain Specification. As stated in previous sections, the highest gain antenna allowed is 4.7 dBi. The first column in the table below shows the Specified Max Antenna Gain for the application in CE Regions. If the exact value is not found, use the next higher gain specification provided in the table. The values to the right of the antenna gain are the minimum values for TX Power Back Off in quarter dB steps, which are required to go into the PDS file for the given operating Wi-Fi Channels. More back off than given here may be applied for other concerns.

CE Certified and Approved PDS File Minimum TX Power Back Off based on Antenna Max Gain Specification

Table 8.3. Required Minimum TX Power Back Off to Apply in PDS according to Maximum Antenna Gain

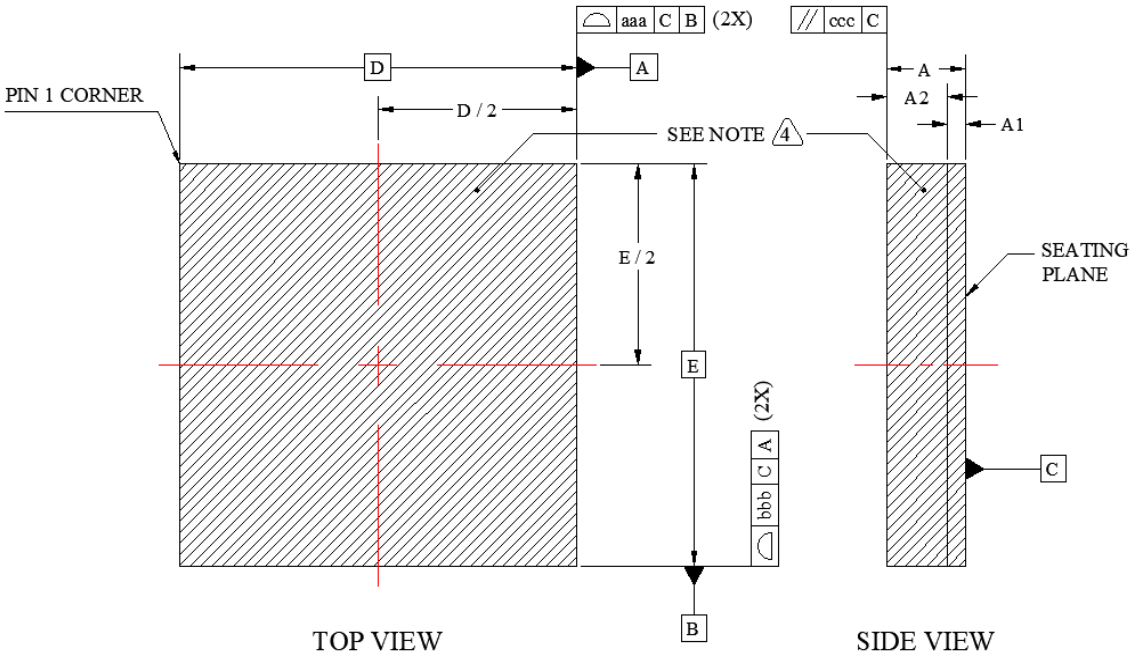
Antenna	CE Minimum PDS File TX Power Back Off in quarter dB steps			
Max Gain dBi	CH1, CH2, 2412-2417 MHz	CH3-CH9, 2422-2452 MHz	CH10, CH11, 2457-2462 MHz	CH12, CH13, 2467-2472 MHz
4.7	8	11	9	5
4.45	7	10	8	4
4.2	6	9	7	3
3.95	5	8	6	2
3.7	4	7	5	1
3.45	3	6	4	0
3.2	2	5	3	0
2.95	1	4	2	0
2.7	0	3	1	0
2.45	0	2	0	0
2.2	0	1	0	0
1.95	0	0	0	0

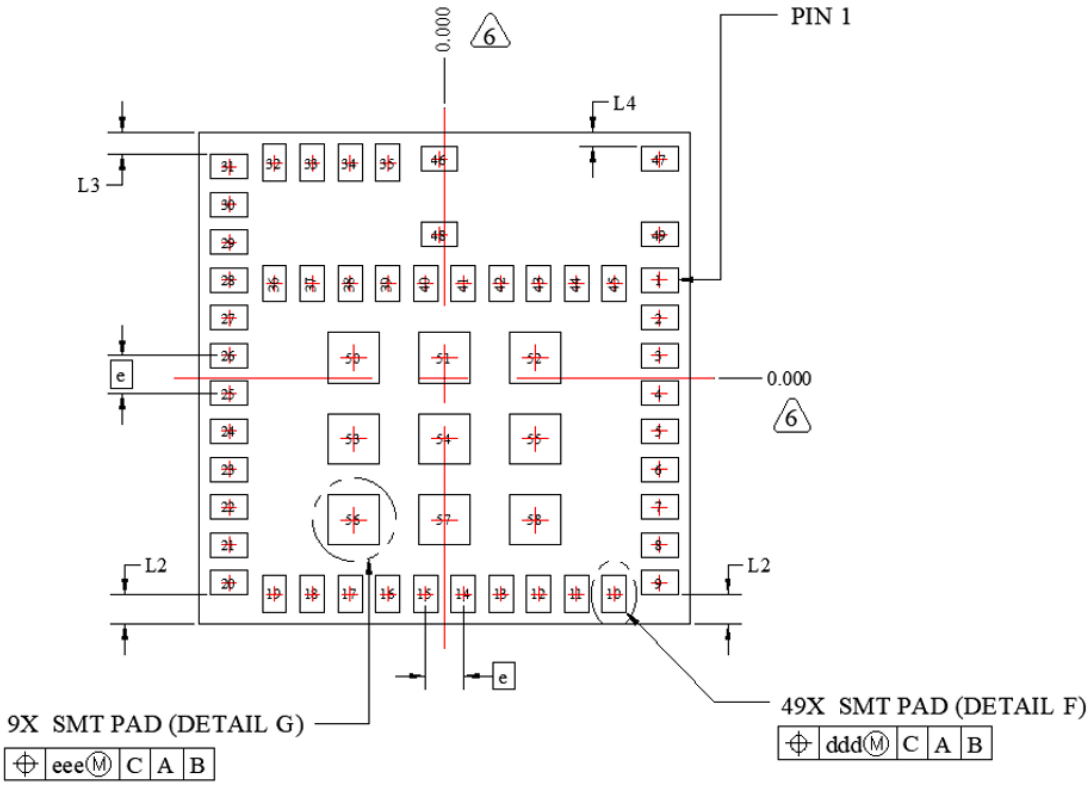
Clear Channel Assessment must be configured in absolute mode to meet CE requirements.

This is achievable with Linux driver 2.2.4 by sending the following command to WFM200 after firmware download and before connecting the the Access Point:

```
  "sudo su" + "echo -en "\x0c\x00\x06\x04\x03\x20\x04\x00\x01\x00\x00\x00" > /sys/kernel/debug/ieee80211/
phy*/wfx/send_hif_msg"
```

9. Package Outline





BOTTOM VIEW

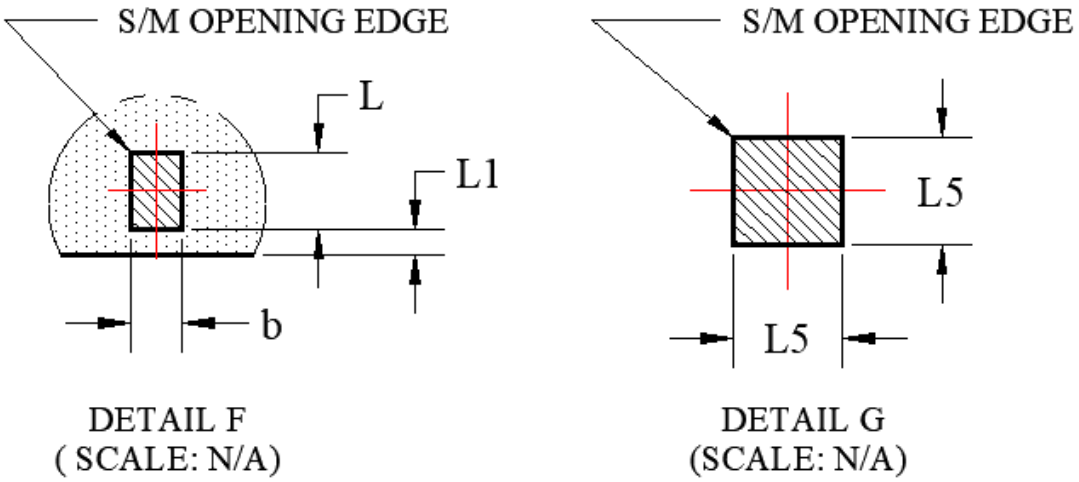


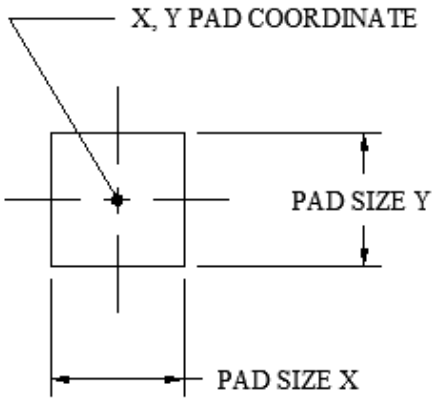
Table 9.1. Top Marking Description

Dimension	MIN	NOM	MAX
A	1.20	1.30	1.40
A1	0.26	0.30	0.34
A2	0.95	1.00	1.05
b	0.27	0.32	0.37
D		6.50 BSC	
e		0.50 BSC	
E		6.50 BSC	
L	0.43	0.48	0.53
L1	0.11	0.16	0.21
L2	0.34	0.39	0.44
L3	0.24	0.29	0.34
L4	0.14	0.19	0.24
L5	0.62	0.67	0.72
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.10	
eee		0.10	

Dimension	MIN	NOM	MAX

Note:

1. All dimensions in millimeters (mms).
2. Unless otherwise specified tolerances are:
   a. Decimal:
      - X.X = ±0.1
      - X.XX = ±0.05
      - X.XXX = ±0.03
   b. Angular: ±0.1 (In Deg)
3. Hatching lines means package shielding area.
4. Dimensioning and Tolerance per ANSI Y14.5M-1994.



10. Integral Antenna Loop and Keep-Out Required Dimensions

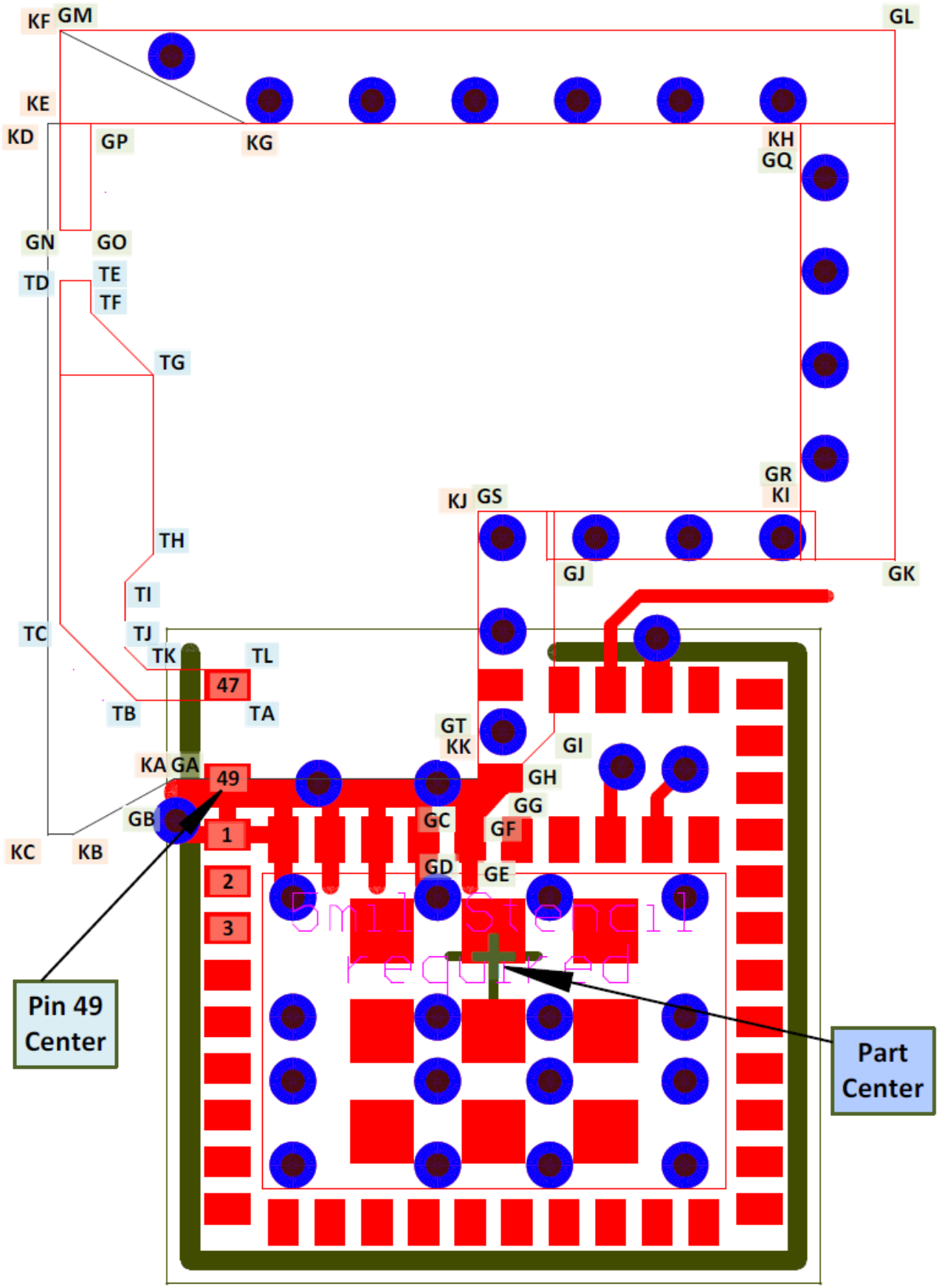


Figure 10.1. Integral Antenna Loop and Keep-Out Required Dimensions

	Pin 49 and 47 Lower Right like Figure 7.1				Pin 49 and 47 Upper Left like Figure 11.1			
Vertex	Origin at Pin 49		Origin at Part Center		Origin at Pin 49		Origin at Part Center	
Trace	X	Y	X	Y	X	Y	X	Y
TA	-0,240	-0,840	2,610	-2,740	0,240	0,840	-2,610	2,740
TB	0,980	-0,840	3,830	-2,740	-0,980	0,840	-3,830	2,740
TC	1,800	-1,660	4,650	-3,560	-1,800	1,660	-4,650	3,560
TD	1,800	-5,320	4,650	-7,220	-1,800	5,320	-4,650	7,220
TE	1,460	-5,320	4,310	-7,220	-1,460	5,320	-4,310	7,220
TF	1,460	-4,980	4,310	-6,880	-1,460	4,980	-4,310	6,880
TG	0,800	-4,320	3,650	-6,220	-0,800	4,320	-3,650	6,220
TH	0,800	-2,400	3,650	-4,300	-0,800	2,400	-3,650	4,300
TI	1,100	-2,100	3,950	-4,000	-1,100	2,100	-3,950	4,000
TJ	1,100	-1,400	3,950	-3,300	-1,100	1,400	-3,950	3,300
TK	0,860	-1,160	3,710	-3,060	-0,860	1,160	-3,710	3,060
TL	-0,240	-1,160	2,610	-3,060	0,240	1,160	-2,610	3,060
GND FILL	X	Y	X	Y	X	Y	X	Y
GA	0,570	0,000	3,420	-1,900	-0,570	0,000	-3,420	1,900
GB	0,570	0,300	3,420	-1,600	-0,570	-0,300	-3,420	1,600
GC	-2,440	0,300	0,410	-1,600	2,440	-0,300	-0,410	1,600
GD	-2,440	0,890	0,410	-1,010	2,440	-0,890	-0,410	1,010
GE	-2,760	0,890	0,090	-1,010	2,760	-0,890	-0,090	1,010
GF	-2,760	0,410	0,090	-1,490	2,760	-0,410	-0,090	1,490
GG	-2,990	0,160	-0,140	-1,740	2,990	-0,160	0,140	1,740
GH	-3,160	-0,160	-0,310	-2,060	3,160	0,160	0,310	2,060
GI	-3,500	-0,500	-0,650	-2,400	3,500	0,500	0,650	2,400
GJ	-3,500	-2,280	-0,650	-4,180	3,500	2,280	0,650	4,180
GK	-7,140	-2,280	-4,290	-4,180	7,140	2,280	4,290	4,180
GL	-7,140	-8,000	-4,290	-9,900	7,140	8,000	4,290	9,900
GM	1,800	-8,000	4,650	-9,900	-1,800	8,000	-4,650	9,900
GN	1,800	-5,860	4,650	-7,760	-1,800	5,860	-4,650	7,760
GO	1,460	-5,860	4,310	-7,760	-1,460	5,860	-4,310	7,760
GP	1,460	-7,000	4,310	-8,900	-1,460	7,000	-4,310	8,900
GQ	-6,140	-7,000	-3,290	-8,900	6,140	7,000	3,290	8,900
GR	-6,140	-2,860	-3,290	-4,760	6,140	2,860	3,290	4,760
GS	-2,680	-2,860	0,170	-4,760	2,680	2,860	-0,170	4,760
GT	-2,680	0,000	0,170	-1,900	2,680	0,000	-0,170	1,900
Keep Out	X	Y	X	Y	X	Y	X	Y
KA	0,570	0,000	3,420	-1,900	-0,570	0,000	-3,420	1,900
KB	1,660	0,600	4,510	-1,300	-1,660	-0,600	-4,510	1,300
KC	1,920	0,600	4,770	-1,300	-1,920	-0,600	-4,770	1,300
KD	1,920	-7,000	4,770	-8,900	-1,920	7,000	-4,770	8,900
KE	1,800	-7,000	4,650	-8,900	-1,800	7,000	-4,650	8,900
KF	1,800	-8,000	4,650	-9,900	-1,800	8,000	-4,650	9,900
KG	-0,200	-7,000	2,650	-8,900	0,200	7,000	-2,650	8,900
KH	-6,140	-7,000	-3,290	-8,900	6,140	7,000	3,290	8,900
KI	-6,140	-2,860	-3,290	-4,760	6,140	2,860	3,290	4,760
KJ	-2,680	-2,860	0,170	-4,760	2,680	2,860	-0,170	4,760
KK	-2,680	0,000	0,170	-1,900	2,680	0,000	-0,170	1,900

Figure 10.2. Dimensions and Coordinates for Integral Antenna Loop and Keep-Out Areas of WFM200

11. Recommended PCB Land Pattern

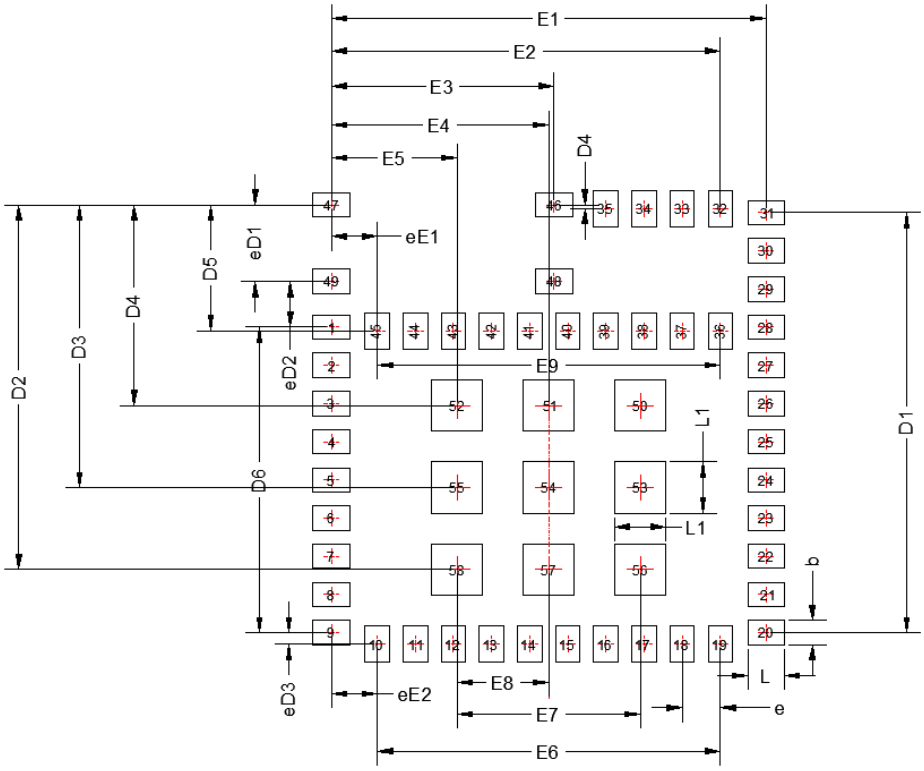


Table 11.1. PCB Land Pattern Dimensions

Dim	mm
b	0.32
D1	5.50
D2	4.77
D3	3.70
D4	2.63
D5	1.65
D6	4.00
D7	0.05
eD1	1.00
eD2	0.60
eD3	0.15
e	0.50
E1	5.70
E2	5.10
E3	2.92
E4	2.85

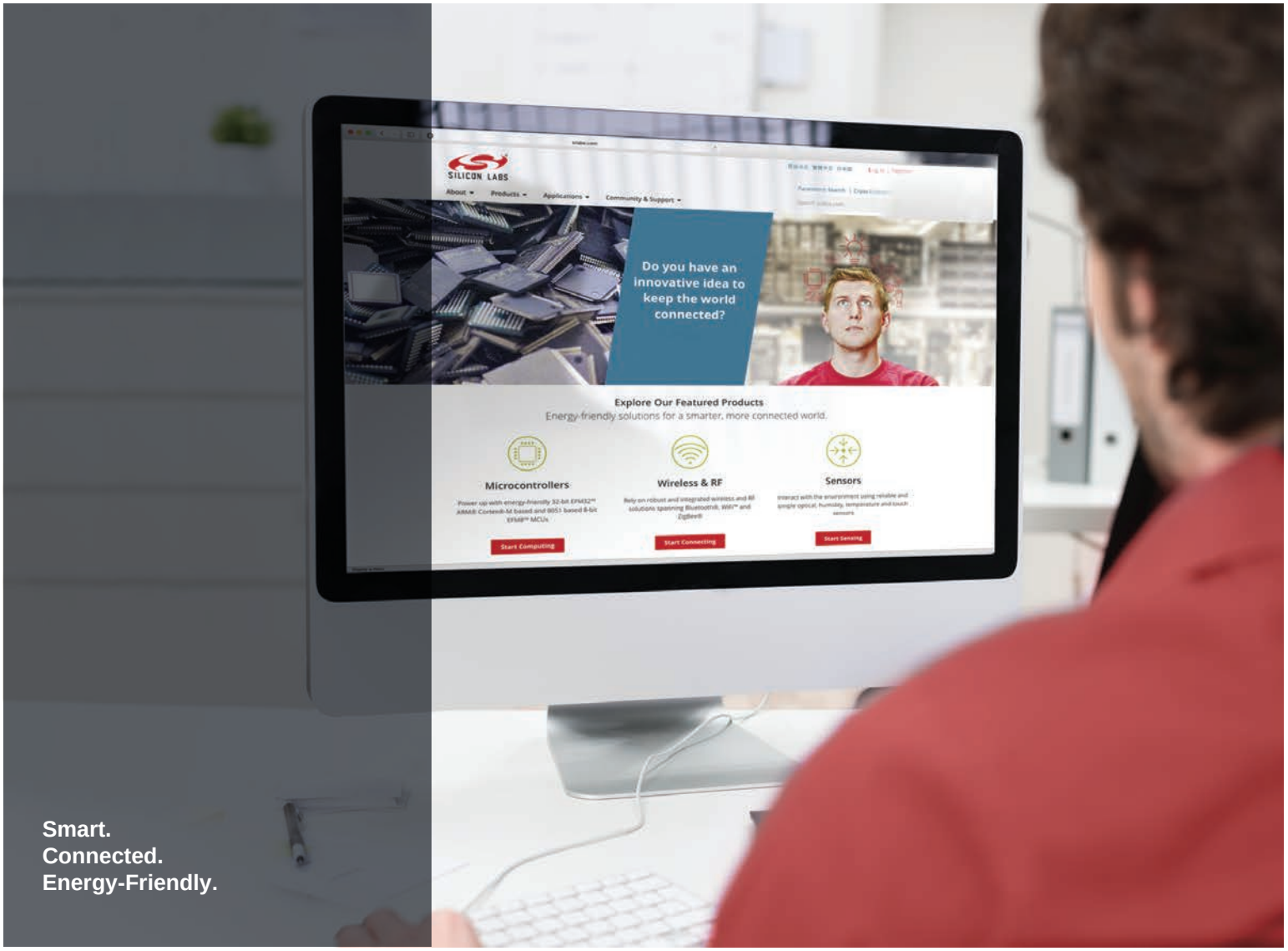
Dim	mm
E5	1.65
E6	4.50
E7	2.40
E8	1.20
E9	4.50
L	0.48
L1	0.67
eE1	0.60
eE2	0.60

Note:
1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. Dimensioning and Tolerance is per the ANSI Y14.5M-1994 specification.

Table 11.2. Stencil Design

Pad No.	Pad Size (mm)	Pad Coordinates (X, Y)
47	0.32 x 0.48	Pad Center Origin (0,0)
1	0.32 x 0.48	(0.00, -1.60)
2	0.32 x 0.48	(0.00, -2.10)
9	0.32 x 0.48	(0.00, -5.60)
10	0.32 x 0.48	(0.60, -5.75)
19	0.32 x 0.48	(5.10, -5.75)
20	0.32 x 0.48	(5.70, -5.60)
31	0.32 x 0.48	(5.70, -0.10)
32	0.32 x 0.48	(5.10, -0.05)
36	0.32 x 0.48	(5.10, -1.65)
45	0.32 x 0.48	(0.60, -1.65)
49	0.32 x 0.48	(0.00, -1.00)
46	0.32 x 0.48	(2.92, 0.00)
50	0.67 x 0.67	(4.05, -2.63)
51	0.67 x 0.67	(2.85, -2.63)
52	0.67 x 0.67	(1.65, -2.63)
55	0.67 x 0.67	(1.65, -3.70)
58	0.67 x 0.67	(1.65, -4.77)

Note:
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.100 mm (4 mils).
3. The stencil aperture to land pad size recommendation is 70% paste coverage.



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