SONY

Sony 2.4G RF Receiver VGP-WRC9

Features

- Fully integrated 2.4-GHz radio on a chip
- 1-Mbps over-the-air data rate
- Transmit power typical: 0 dBm
- Receive sensitivity typical: –87 dBm
- Below 1 µA typical current consumption in sleep state
- Closed-loop frequency synthesis
- Supports frequency-hopping spread spectrum
- On-chip packet framer with 64-byte first in first out (FIFO) data buffer
- Built-in auto-retry-acknowledge protocol simplifies usage
- Built-in cyclic redundancy check (CRC), forward error correction (FEC), data whitening
- Supports DC ~ 12-MHz SPI bus interface
- Additional outputs for interrupt request (IRQ) generation
- Digital readout of received signal strength indication (RSSI)
- 4 × 4 mm quad flat no-leads (QFN) package, bare die, or wafer sales

Product Description

The RF Receiver, optimized to operate in the 2.4-GHz ISM band, is Sony using Cypress 8935 of 2.4-GHz low-power RF technology, bringing the next level of low-power performance into a small 4-mm × 4-mm footprint. WirelessUSB NL implements a Gaussian frequency-shift keying (GFSK) radio using a differentiated single-mixer, closed-loop modulation design that optimizes power efficiency and interference immunity. Closed-loop modulation effectively eliminates the problem of frequency drift, enabling WirelessUSB NL to transmit up to 255-byte payloads without repeatedly having to pay power penalties for re-locking the phase locked loop (PLL) as in open-loop designs.

Among the advantages of RF Receiver are its fast lock times and channel switching, along with the ability to transmit large payloads. Use of longer payload packets, compared to multipl short payload packets, can reduce overhead, improve overa power efficiency, and help alleviate spectrum crowding.

Combined with Cypress's enCoRe™ family of USB and wireles microcontrollers, the RF Receiver also provides the lowest bil of materials (BOM) cost solution for PC peripheral application such as wireless keyboards and mice, as well as best-in-clas wireless performance in other demanding applications such a toys, remote controls, fitness, automation, presenter tools, an gaming.

Applications

- Wireless keyboards and mice
- Handheld remote controls
- Wireless game controllers
- Hobby craft control links
- Home automation
- Industrial wireless links and networks
- Cordless audio and low-rate video

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Functional Description

The RF Receiver was applied with CYRF8935 RF transceiver for variety of applications.

The module is a low-cost, fully-integrated CMOS RF transceiver, GFSK data modem, and packet framer, optimized for use in the 2.4-GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver uses extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

The product transmits GFSK data at approximately 0-dBm output power. Sigma-Delta PLL delivers high-quality DC-coupled transmit data path.

The low-IF receiver architecture produces good selectivity and image rejection, with typical sensitivity of –87 dBm or better on most channels. Sensitivity on channels that are integer multiples of the crystal reference oscillator frequency (12 MHz) may show approximately 5 dB degradation. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

Power-on and Register Initialization Sequence

For proper initialization at power up, V_{IN} must ramp up at the minimum overall ramp rate no slower than shown by T_{VIN} specification in the following figure. During this time, the RST_n line must track the V_{IN} voltage ramp-up profile to within approximately 0.2 V. Since most MCU GPIO pins automatically default to a high-Z condition at power up, it only requires a pull-up resistor, as shown in Figure 11 on page 15. When power is stable and the MCU POR releases, and MCU begins to execute instructions, RST_n must then be pulsed low as shown in Figure 2, followed by writing Reg[27 = 0x4200. During or after this SPI transaction, the State Machine status can be read to confirm FRAMER_ST= 1, indicating a proper initialization.

Figure 2. Power-on and Register Programming Sequence

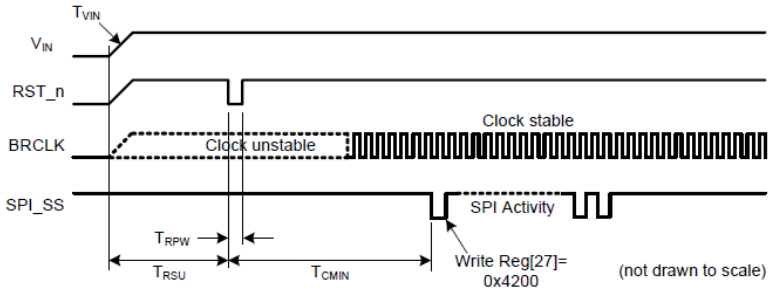


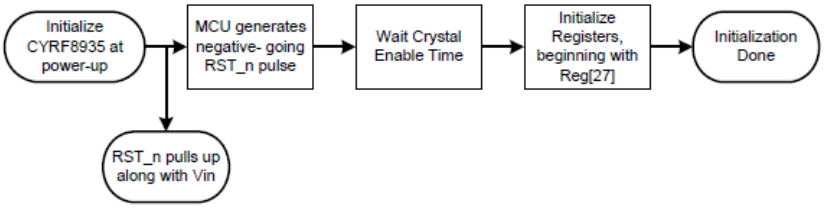
Table 2. Initialization Timing Requirements

Timing Parameter	Min	Max	Unit	Notes
T_{RSU}	–	20	ms	Reset setup time necessary to ensure complete reset
T_{RPW}	1	10	µs	Reset pulse width necessary to ensure complete reset
T_{CMIN}	3	–	ms	Minimum recommended crystal oscillator and APLL settling time
T_{VIN}	–	6.5	ms/V	Maximum ramp time for V_{IN}, measured from 0 to 100% of final voltage. For example, if V_{IN}= 3.3 V, the max ramp time is 6.5 × 3.3 = 21.45 ms. If V_{IN}= 1.9 V, the max ramp time = 6.5 × 1.9 = 12.35 ms.

■ After RST_n transitions from 0 to 1, BRCLK begins running at 12-MHz clock.

■ After register initialization, CYRF8935 is ready to transmit or receive.

Figure 3. Initialization Flowchart



Enter Sleep and Wakeup

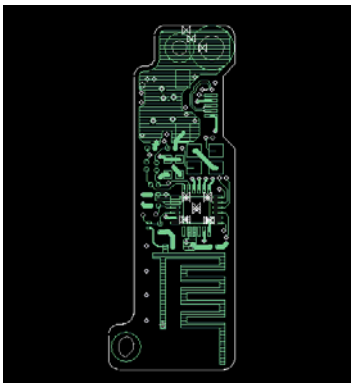
When the MCU or application writes to the CYRF8935 register 35[14] to enter sleep mode and deasserts SPI_SS, CYRF8935 enters the sleep state where current consumption is extremely low.

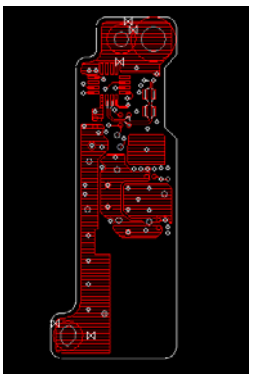
Later, when SPI_SS is reasserted, CYRF8935 automatically wakes up from the sleep state. At this time the crystal oscillator is reactivated. The crystal oscillator takes 1 to 3 ms to become fully stable. During wakeup, there is no requirement to clear register 35[14] and no requirement to hold SPI_SS asserted.

There are two sleep current choices available, selectable by Reg[27] setting: 1 µA and 8 µA. If you use the 1 µA setting, Vin must be greater than or equal to 3.0 VDC. If Vin is ever expected to be < 3.0 VDC during Sleep, use the 8 µA setting.

To achieve the lowest sleep current, a special sleep state firmware patch is required. The patch is as follows:

SLEEP PATCH: Before writing register 35 to enter sleep, write Reg[10]= 0x8FFD, wait 30 µs or more, then write Reg[10] back to the default value of 0x7FFD. Next, write Reg[35] to enter sleep, as usual.





Setting the Radio Frequency

Programming by channel number is the easiest way to set frequency. In the CYRF8935, RF carrier frequency and RF channel number are always related by the expression:

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Freq. = 2402 + Ch. #
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Channel number is loaded into bits [6:0] of Register 7. Bits 7 and 8 initiate the desired Rx or Tx operation, respectively.

Some sample Register 7 examples are as shown in Table 4.

During Regulatory Compliance testing, you can jump directly to another frequency any time without going through IDLE state. If you change between Tx and Rx, however, you must pass through IDLE state. For IDLE state, write Register 7 to clear bits 8 and 7. Tx or Rx operation is initiated when Register 7 bit 8 or 7 is set. Radio frequency is also determined at that time.

Table 4. Sample Register 7 Settings

Carrier Frequency, MHz	DUT Channel Number (decimal)	DUT Channel Number (hex)	Tx setting: Reg. 7 value for TX_EN= 1	Rx setting: Reg. 7 value for RX_EN= 1
2402	0	00	0100	0080
2403	1	01	0101	0081
2404	2	02	0102	0082
|	|	|	|	|
2434	32	20	0120	00A0
|	|	|	|	|
2441	39	27	0127	00A7
|	|	|	|	|
2480	78	4E	014E	00CE

Crystal Oscillator

The RF Receiver contains the CYRF8935 gain block for the quartz crystal frequency standard.

Quartz Crystal Application

As shown in Figure 10 on page 15, the series resistor Rs limits power to the crystal and contributes to the phase-shift necessary for oscillation. The ideal Rs value may need to be determined empirically, adjusted for certain crystal manufacturer part numbers and designs. The series equivalent combinations of C1 and C2 largely determine the capacitive load seen by the crystal, which should match the crystal vendor's specification. These capacitor values are chosen to center the crystal oscillator frequency at the correct value, 12 MHz. The feedback resistor Rf from the buffer output to input serves to self-bias the on-chip buffer to the center of the linear region for maximum gain.

Verifying correct crystal oscillator frequency may require special test methods. Because connecting a frequency counter probe to either XTALi or XTALo adds capacitive loading and alters the crystal oscillation frequency, other methods must be used. For bare die applications involving COB packaging, use the BRCLK test point to verify correct frequency of oscillation. This requires register 32[3:1] set accordingly (see Register Definitions on page 23). For 24-QFN packaged parts, the correct crystal frequency is determined by transmitting a continuous carrier frequency (see Register Settings for Test Purposes on page 20) and using a RF frequency counter to ensure correct frequency. Irrespective of which method is used, initial tolerance should be within budget as recommended in Table 5, such that the total frequency error stays within budget.

Table 5. Crystal Specifications

Crystal Parameter	Specification
Frequency	12.000 MHz
Initial frequency tolerance	±15 ppm
Frequency tolerance over temperature	±15 ppm
Frequency tolerance after aging	±5 ppm
Frequency drift due to load cap. drift	±5 ppm
Total	**±40 ppm**
Equivalent series resistance	80 Ω max
Resonance mode	Fundamental, parallel resonant
Load capacitance	In accordance with external load capacitors (see C1 and C2 in Figure 10)

Note For proper operation, the total frequency error must not exceed what is shown in Table 5. Individual error contributions can be adjusted; for example 10+20+5+5=40, or 5+30+2+3=40.

Note: For Model VGP-WKB16, will use Firmware to lock some frequency. So its frequency range is from 2402MHz to 2478MHz only. Total channel number is 77.

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: AK8VGPWRC9".

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

End Product Labeling
The final end product must be labeled in a visible area with the following: “Contains transmitter module IC: 409B-VGPWRC9”.

CAN ICES-3 (B)/NMB-3(B)