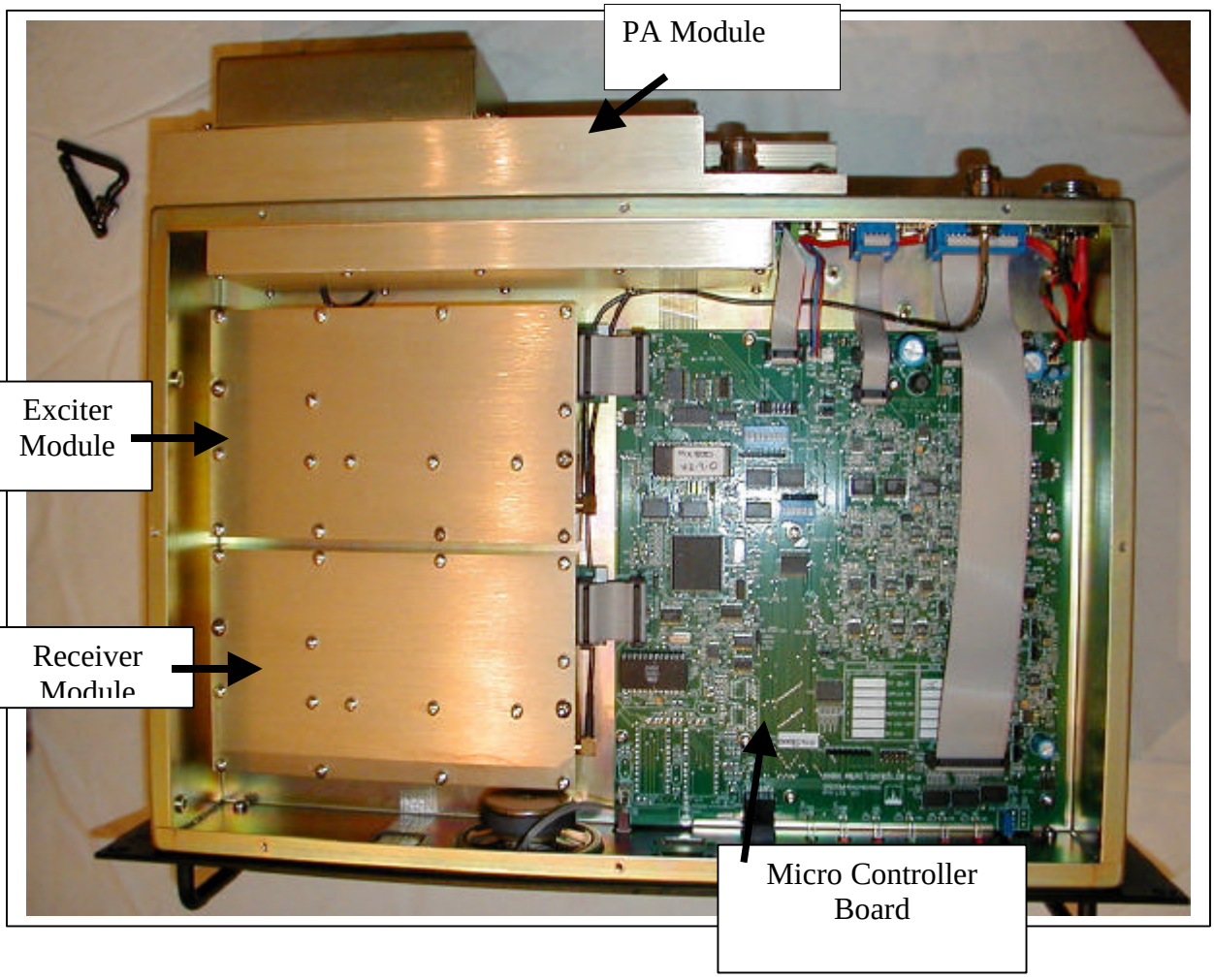
4. Technical Description

The internal design of the MX800 is of a modular nature allowing for simple configuration and maintenance while ensuring minimal downtime. For reference purposes, the top view of a typical MX800 with top cover removed is shown below. The standard unit without speaker and microphone is illustrated.



MX800 top view.

4.1. Exciter Module

Refer.

Exciter Block Diagram:	BD002
Exciter Circuit Diagram:	CS002-1
TX VCO Circuit Diagram:	CS004-1 (Bands A to Q)

RF from the VCO on SKU-1 at a nominal level of+3dBm is applied to the fractional-N synthesizer ICI0 main divider input. This signal is compared with the reference oscillator frequency and the correction voltage from the synthesizers charge pump output is filtered then amplified by the non inverting low noise op amp IC9A. This correction voltage is fed back to the VCO to maintain loop lock as well as being fed to the Micro Controller via SKD-14. A lock detect signal from IC10 is also fed to the Micro Controller via SKD-16.

The op amp uses a 25 volt power supply (generated on the Micro Controller) so as to provide a wide tuning range voltage to the frequency control varicaps located on the VCO
board. Frequency programming data for the exciter is sent to the synthesizer chip from the Micro Controller via a serial data line on SKD-18 under the control of the Clock (SKD-15) and Strobe (SKD-17) lines.

Provision is made for the optional injection of an external reference frequency. If this option is selected CN3 is fitted and X1 is not fitted. Components R30 and TR7 are also omitted.

A second RF output from the VCO on SKT-6 also at +3dBm is used as the main transmit RF amplifier signal source. This main signal is first buffered by a very high isolation circuit consisting ofa 10dB pad and a MMIC amplifier (IC1). The signal is further amplified by IC2 and a variable gain wide band amplifier with 40dB control range and power output of 300mW. The drive power of this stage is used to set the output power to the main power amplifier under the control of the DC voltage on SKD-4 from the Micro Controller board.

The VCO boards and synthesizer circuits are the same for the exciter and receiver modules. The VCO consists ofa 10mm ceramic coaxial resonator with common base oscillator for low phase noise for bands 805-960 MHz. Frequencies below 520 MHz use an LC tank circuit. The power supply to the VCO consists of an 8 volt regulator and active filter for maximum noise rejection. It is controlled by the Micro Controller through SKD-7 which connects to switch TR6. For standard modulation, transmit audio is fed on SKD-8 to the conventional point of the VCO varactor. For 2 point modulation, audio is also fed via SKD-19 to the voltage control pin of the VC-TXCO, this in effect cancels out the PLL error that would otherwise have occurred for low audio frequencies, hence

resulting in a flat VF response.

4.2. Receiver Module

Refer:

Receiver Block Diagram:	BD001
Receiver Front End Circuit Diagram:	CS003-2
Receiver IF Circuit Diagram:	CS003-1
RX VCO Circuit Diagram:	CS005-1 (Band A to Q) CS012-1 (Band R to X)

The receive signal from the antenna enters on CN1 a 3 section Bandpass filter which provides the initial filtering for the front end amplifier. The front end amplifier IC12 is a broad band high performance MMIC with a gain of 18dB, noise figure of 4dB and 3rd order intermodulation intercept of+36dB. This is followed by a 4dB pad and a second 3 section BPF, and a high level double balanced mixer M1.

The receiver uses high side local oscillator injection for bands A to I and low side injection for all other bands. RF from the VCO main output on SKT-6 is buffered and amplified to + 17dBm by IC4 and injected in the high level mixer which down converts the signal to the first IF frequency of 90 MHz (45MHz for bands A to D3). This IF signal from the mixer is terminated by a bi-directional constant impedance network and is then amplified by a hipolar amplifier TR2 with a gain of 15dB and 3rd order intermodulation intercept +35dB. This provides a high degree of intermodulation rejection for the receiver. This stage is followed by a 4 pole 90 MHz crystal filter FL3A/B with its associated matching networks. The signal is further amplified and filtered by a transistor amplifier TR3 and its associated 2 pole crystal filter FL4 before being fed into the main IF demodulator chip IC 1 with a second IF frequency of 455kHz. The resulting audio is passed out to the Micro Controller board on SKD-3. The Received Signal Strength Indication (RSSI) from IC1 is buffered by IC5A and connected to the Micro Controller board via SKD-4.

RF from the VCO on SKU-1 at a nominal level of+3dBm, is applied to the fractional-N synthesizer (IC10) main divider input. This signal is compared with the reference oscillator frequency and the correction voltage from the synthesizer's charge pump output is filtered then amplified by the non inverting low noise op amp (ICI 1A). This correction voltage is fed back to the VCO to maintain loop lock as well as being fed to the Micro Controller via SKD44. A lock detect signal from IC10 is also fed to the Micro Controller via SKD-I6. The op amp uses a 25 volt power supply (generated on the Micro Controller)

so as to provide a wide tuning range voltage to the frequency control varicaps located on the VCO board. Frequency programming data for the receiver is sent to the synthesizer chip from the Micro Controller via the a serial data line on SKD-18 under the control of the Clock (SKD- 15) and Strobe (SKD- 17) lines

The local oscillator signal to the mixer is controlled by the Micro Controller through an enable signal on SKD-8. This signal switches the supply to the local oscillator amplifier and is used to enable or disable the receiver.

Provision is made for the optional injection of an external reference frequency. If this option is selected CN3 is fitted.

4.3. Power Amplifier Module

Refer:

PA Block Diagram	BD004
PA Circuit Diagram:	CSO16-1 (Band A to B)
	CS006-1 (Band C to D3)
	CS007-1 (Band E to F)
	CS013-1 (Band G to I)
	CS008-1 (Band J to M)
	CS009-1 (Band N to Q)
	CS0010-1 (Band R to X)
	CS014-1 (Band Nto Q 5W)

RF from the Exciter on CN1 is first attenuated by a 50 ohm pad which is used to provide a good 50 ohm source impedance for the high power hybrid amplifier IC1. The RF is amplified to between 5 and 13 watts at the hybrid 50 ohm output. The signal from the hybrid is then matched by a broad band network to drive the low input impedance associated with the final transmit power amplifier transistor TR1. The transistors low collector impedance is then also matched back to 50 ohms by a broadband matching network. Trimmer capacitors enable adjustment of the power amplifier over a wide bandwidth so as to maintain good conversion efficiency. Prior to transmission a low loss 13 element elliptical low pass filter, filters out the unwanted harmonics to less than -90dBc.

A dual directional coupler consists of coupled microstrip transmission lines S5, S6 **and** S7 fabricated on the PCB artwork. The sampled RF energy is rectified to provide a proportional DC voltage output on CN4-8 (FWD) and CN4-5 (REFL).

TR2 serves to switch the DC supply to the Hybrid under control of the PTT line from the Micro Controller on CN4-2. A thermistor TS1 physically located on the PA heatsink is connected to the Micro Controller via CN4-4/6

4.4. Micro Controller Board

Refer:

Block Diagram	BD003 (Rev A to I-D BD005 (Rev I upwards)
Circuit Diagram	CS001-1/6

The MX800 Micro Controller Board has 4 main functions
Overall radio management
TX and RX signal processing
RF power control
User interface

4.4.1. Overall Radio Management

In addition to analogue signal processing circuitry the Micro Controller board accommodates an 80C552 microprocessor IC1, a 64kbyte EPROM IC3, 32kbyte RAM IC4, a 16kbyte EEPROM as well as address decoding, I/O latches and other miscellaneous circuitry. The Micro Controller is responsible for ensuring that the radio acts as programmed by the user. It stores the user-entered parameters for each channel in EEPROM. This information includes RX and TX RF frequencies, RX and TX CTCSS frequencies as weIl as RF output power and operating mode. An 8 channel analog to digital converter allows the microprocessor to read 8 analogue values internal to the radio which in conjunction with the digital inputs to the microprocessor allow the operating status of the radio to be monitored and controlled. The following analogue items are read

Port	**Parameter**
ADC0	Received Signal Strength Indication(RSSl)
ADC 1	Detected Discriminator output level
ADC2	DC operating voitage
ADC3	RX VCO tuning Voltage
ADC4	TX VCO tuning Voltage
ADC5	PA temperature
ADC6	PA forward power
ADC7	PA reflected power

The Micro Controller sends programming data to the synthesizer ICs on the Receiver **and** Exciter modules each time the channel is changed as well as on PTT. This information is

communicated to the Receiver and Exciter modules by way of bussed data and clock lines on SKC/D-18 and SKC/D-15 (Exciter/Receiver) and an individual module strobe on SKC/D-17. A lock detect signal from each module on SKC/D-16 is read by the micro controller.

In addition to the synthesizer programming bus an I2C bus goes to each of the modules. This bus is currently unused.

IC25 is a non predictive, full duplex CTCSS encoder/decoder which is under the control of the microprocessor.

4.4.2. TX Signal Processing

TX audio may be sourced from a number of different paths. These include VF from line, Talk through audio, the microphone, DC FM/Wideband input, Tone generator from microcontroller, Test TX VF inject from the Monitor port, CTCSS generator and the internal RF modem.

The TX VF path is readily user configurable with most major functional blocks being possible to either select or bypass by means of links (refer to 2.2.2.1 for details of link settings). The VF from line enters the board on SKH-14 and RV4 (TX VF gain) provides gain adjustment to accommodate different line levels. This is followed by a selectable compressor (IC34A) with 30rib dynamic range. The output of the compressor apart from being fed to the main TX audio path is also connected to the input side of the 'Line' FFSK modem and via a gain control pot the speaker amp (IC60). Following the main TX audio path, IC36B serves to switch the VF further on the TX audio path or, under the control of the external input on SKH- 13, to loop it back to the line output via RV7 which provides level adjustment for the looped back signal. From this switch the VF passes though a second switch IC32B under the control of the Micro Controller and the external TX talk line on SKH-10. This switch is used to disable the line TX VF path. From here the VF passes through a pre-emphasis stage C66, R67 and a 300Hz high pass filter (IC30B and IC29A) each of which is selectable through links. The output of this filter is fed to IC30A a summer/limiter amp.

The summing point of this amp also serves to combine the audio from the talkthrough path which is level adjusted by RV3, the microphone which is processed through a similar compression, pre-emphasis and filtering chain as the line VF, the tone (Morse code) signal from the microprocessor, the DC FM input which enters the board on SKH-6 and the Test TX VF injection from SKE-2. The latter three inputs are all at fixed levels. RV2 on IC30A provides overall gain adjustment. Following the limiter amp is the TX VF low pass filter. The standard Bessel filter has a 3.4kHz cut off frequency but may optionally be ordered as a 3kHz Chebychev filter. A second summing amplifier iC24B follows which combines the CTCSS, optional modem (IC52 and IC54) and Wideband audio inputs with the TX VF. Level adjustment of the CTCSS signal is in three 0.85dB steps either above or below the nominal level (10% of max dev). These level steps are

set up using the Configure screen of MXTOOLS. The output of this final stage is fed to two microprocessor controlled digipots which serve to adjust the modulating signal level to the VCO and the reference oscillator. A third digipot is used to provide an offset null for the reference oscillator center frequency. Adjustment of these levels is also by way of MXTOOLS using the Channel Edit screen.

4.4.3. RX Signal Processing.

In a similar fashion to the TX audio path the major functional elements of the RX audio path are capable of being selected or bypassed by means of links.

Discriminator audio enters the board on SKD-3 and is fed to a selectable 300Hz highpass filter comprising IC37 and IC38B. This output or an unfiltered version of the discriminator audio is fed via a switch IC32A to the TTR path. The switch is used to disable talk through audio under the control of the microprocessor and the external TX

talk line on SKH-10. Following the HPF a selectable 3.4kHz cutoff low pass filter IC38A and IC39B connects to the de-emphasis circuit IC39A. From here the audio passes through the mute switch IC32C which is under control of the microprocessor and on to the RX talk switch ICIC36C which is controlled externally from SKH-3. This second switch is used to disable RX audio to line. A final switch IC36A selects between RX audio and TX looped back audio for output to line via amplifiers IC40A and IC40B. Secondary inputs to these amplifiers are the TX audio from the line modem and microphone audio to line. The output on SKH-2 forms an unbalanced 600• VF output to line and, alternatively, outputs SKH-2 and SKH-11 form a differential output.

Discriminator audio is also fed via a low pass filter IC31 to the CTCSS decoder as well as to a level detector D9 the output of which is connected to ADC 1 on the microprocessor.

Discriminator audio is also fed to the mute detection circuit. This comprises a high pass filter IC41 followed by RV4 which sets the mute threshold. Following amplification by IC42A and rectification by IC42B and IC43A a comparator, IC43B, determines when the detected signal passes a fixed threshold. The output of the comparator is fed to the microprocessor and via a selectable inverter to SKH-4.

Discriminator audio is also fed to RX port of the RF modem IC54.

4.4.4. RF Power Control

Forward power is controlled by the microprocessor through two mechanisms. Based on preprogrammed per channel adjustments the microprocessor sets the digipot IC 10 to a reference setting. IC23A serves as a comparator and, with the non-inverting input

connected to the wiper of the digipot, is set up with a reference voltage. The detected actual PA forward power is fed to the inverting input oflC23A. The error voltage at the output of IC23A is fed to the exciter output power control circuit via SKC-4 and the action
of the control loop is to set the RF power such that the actual detected volts equals the reference volts. The digipot setting is static for each channel unless the required forward power is changed.

The voltage to the top of the digipot is set up by the microprocessor through the Pulse Width Modulator output PWM1. On PTT the ON duty cycle of the PWMI output is progressively increased and the filtered result of this forms a ramp to the top of the power control digipot. Once 100% duty cycle is reached full power is produced. This results in a fast but controlled RF power rise characteristic.

4.4.5. User Interface

All user interface to the MX800 except the RF connections is made by way of the Micro Controller board.

- Output latch IC18 drives the six LED indicators on the front panel. The function is described in section 1.1.1.

- Input latch IC14 serves to accept the programmed status of the 8 bit binary channel select DIP switch SW1. Refer section 6.3 for programming instructions.

- Input latch IC 13 serves to accept the programmed status of the 6 bit binary mode select DIP switch SW2. Refer section 2.2.2.2 for mode selection instructions.

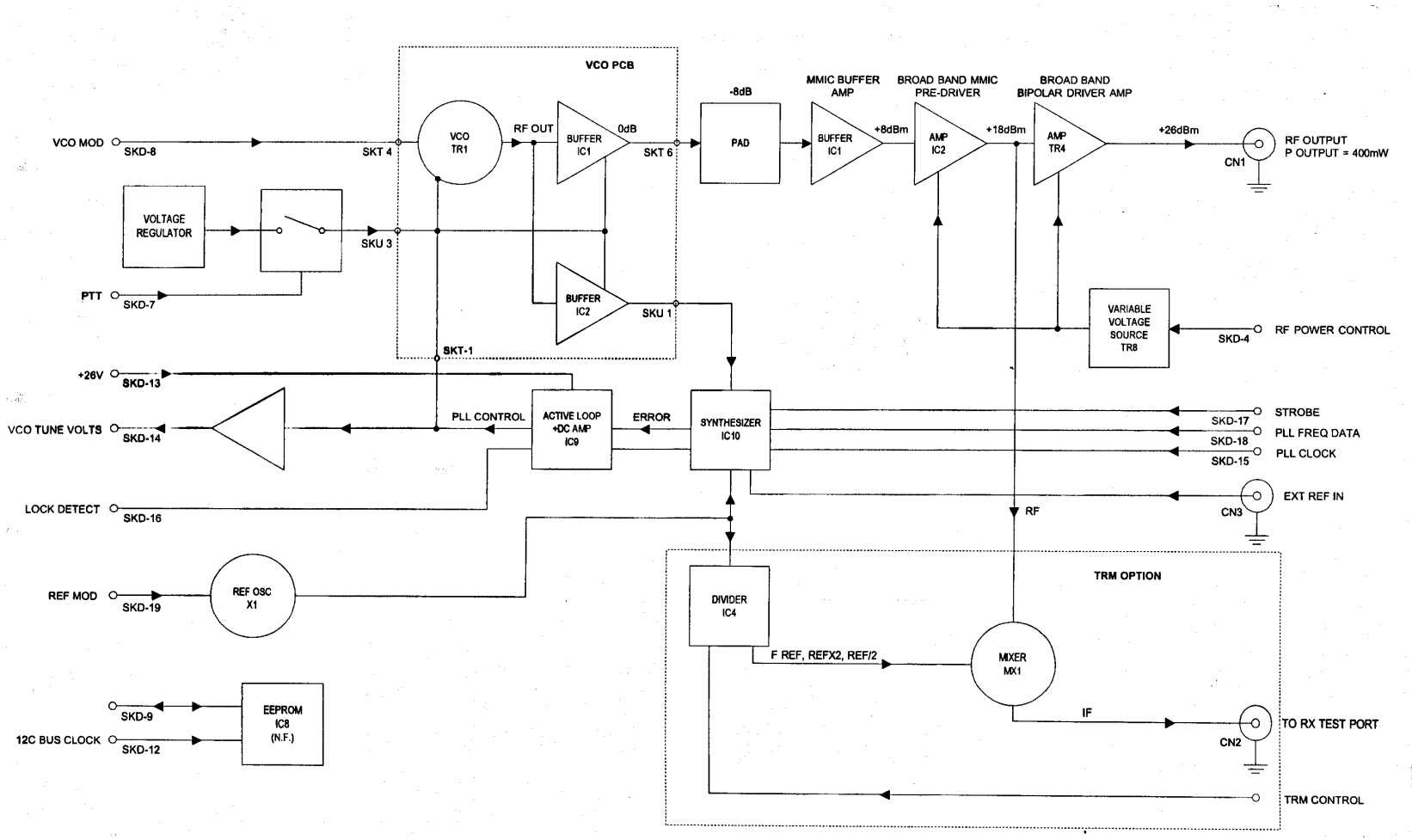
- Input latches IC48 and IC47 provide two eight bit +5V CMOS compatible digital input ports (ports A and B respectively). The inputs may be either internally pulled high and active low or internally pulled low and active high. Port B inputs are configured as external channel select inputs. The inputs are buffered by 10k.Q

- Output latch IC46 provides 8 uncommitted +5V CMOS compatible digital outputs. Each output is buffered by a 1kohm resistor.

- IC60 is a 1 watt speaker amplifier, which drives the internal speaker. This IC includes the volume control function connection to the front panel toggle switch.

- Microphone audio is fed via amplifier IC61A to a compressor (IC34B). This VF is pre-emphasized and filtered before being fed to the main TX voice path.

- IC22 provides CMOS to RS-232 conversion for the serial port.



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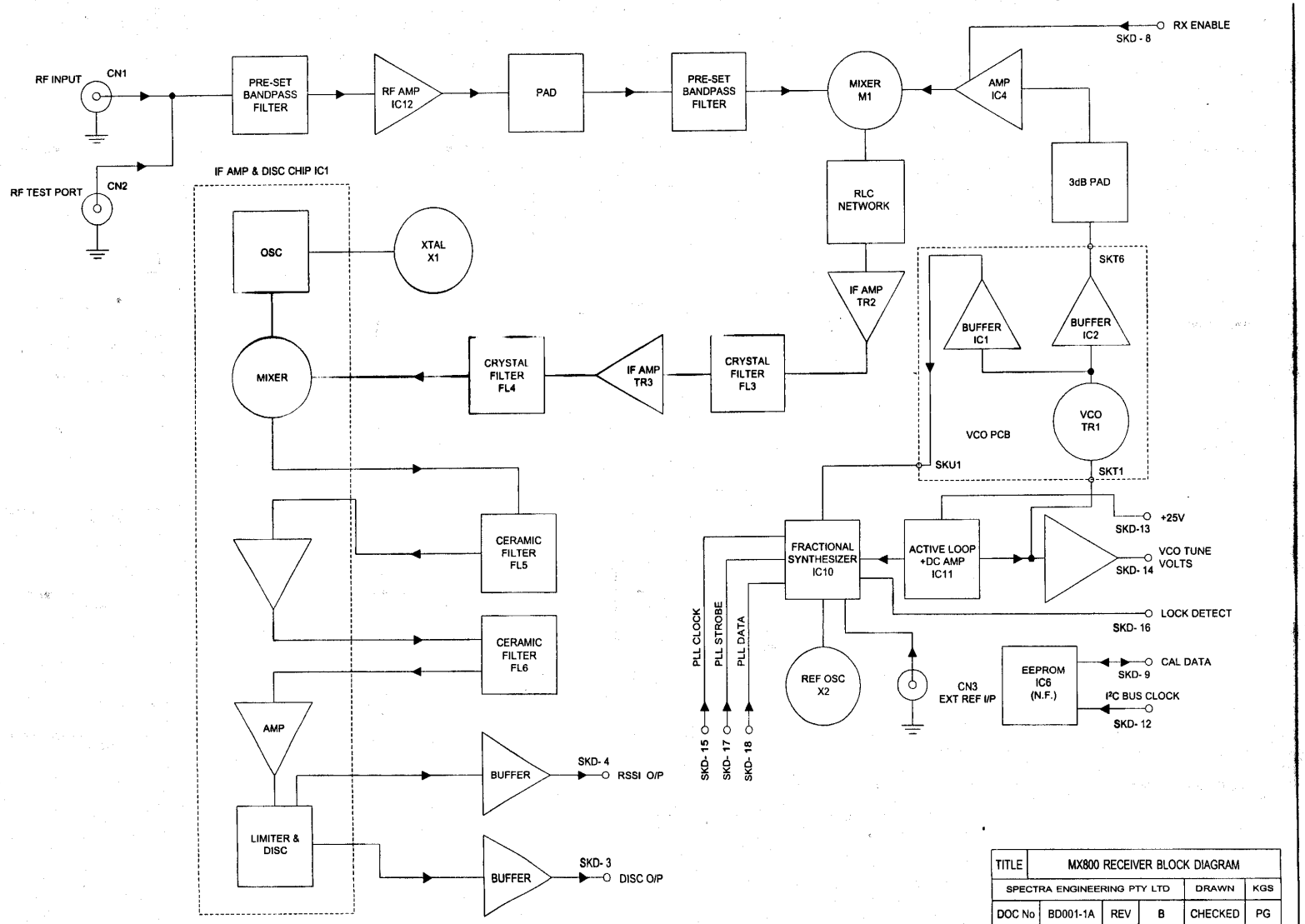

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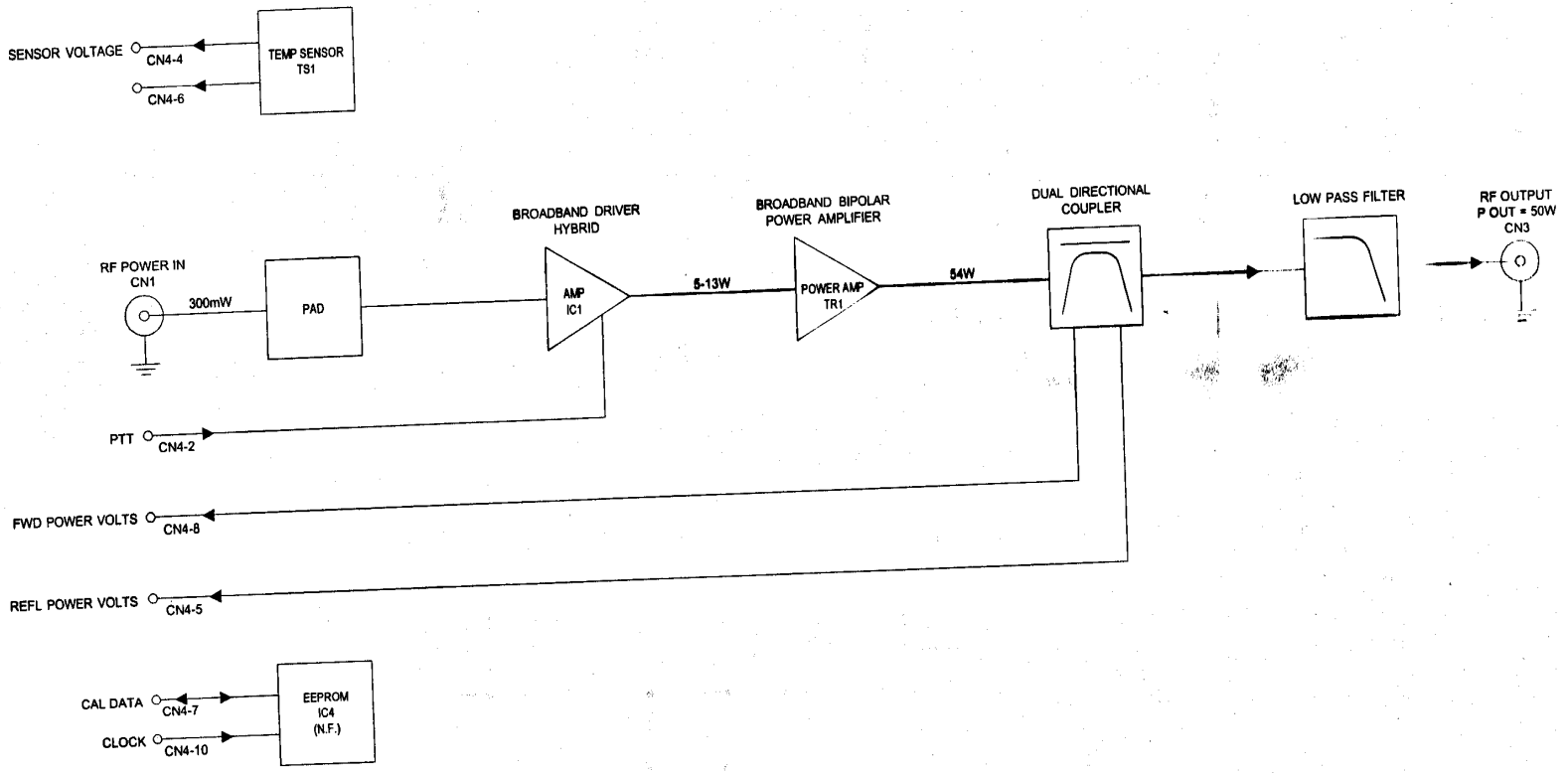

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DOC No	BD004-1A	REV	B	CHECKED	
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