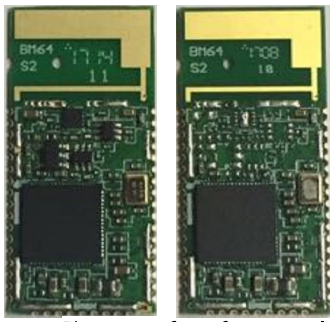
BM64C1 BT4.2 Stereo Audio Module

IS2064GM



(This Photos are for reference only)

Features

• Qualified for Bluetooth v4.2 specifications
• Supports HFP 1.6, HSP 1.2, A2DP 1.3, SPP 1.2 and AVRCP 1.6
• Supports Bluetooth 4.2 dual-mode (BDR/EDR/ BLE) specifications (FW dependent)
• Stand-alone module with on-board PCB antenna and Bluetooth stack
• Supports high resolution up to 24-bit, 96 kHz audio data format
• Supports to connect two hosts with HFP/A2DP profiles simultaneously
• Transparent UART mode for seamless serial data over UART interface
• Supports virtual UART communication between host MCU and smartphone applications by Bluetooth SPP or BLE link
• Easy to configure with Windows® GUI or directly by external MCU
• Supports firmware field upgrade
• Supports one microphone
• Compact surface mount module:32 x 15 x 2.7 mm
• Castellated surface mount pads for easy and reliable host PCB mounting
• RoHS compliant
• Ideal for portable battery operated devices
• Internal battery regulator circuitry DSP Audio Processing
• Supports 64 kbps A-Law, -Law PCM format/ Continuous Variable Slope Delta (CVSD) modulation for SCO channel operation
• Supports 8/16 kHz noise suppression
• Supports 8/16 kHz echo cancellation
• Supports Modified Sub-Band Coding (MSBC) for wide band speech
• Built-in High Definition Clean Audio (HCA) algorithms for both narrow band and wide band speech processing
• Packet loss concealment (PLC)
• Built-in audio effect algorithms to enhance audio streaming

Peripherals

• Built-in lithium-ion and lithium-polymer battery charger (up to 350 mA)
• Integrated 1.8V and 3V configurable switching regulator and low-dropout (LDO) regulator
• Built-in ADC for battery monitoring and voltage sense
• Built-in ADC for charger thermal protection
• Built-in undervoltage protection (UVP)
• An AUX-In port for external audio input
• Two LED drivers
• Multiple I/O pins for control and status

HCI Interface

• High-speed HCI-UART interface (supports up to 921,600 bps)

RF/Analog

• Frequency spectrum: 2.402 GHz to 2.480 GHz
• Receive sensitivity: -90 dBm (2 Mbps EDR)
• Output Power
- BM64 Class 1: +15 dBm typical
- BM64 Class 2: +2 dBm typical

Audio Codec

• Sub-band Coding (SBC) and optional Advanced Audio Coding (AAC) decoding
• 20-bit digital-to-analog converter (DAC) with 98 dB SNR
• 16-bit analog-to-digital converter (ADC) with 92 dB SNR
• Supports up to 24-bit, 96 kHz I2S digital audio

MAC/Baseband Processor

• Supports Bluetooth 4.2 dual-mode (FW dependent)
- BDR/EDR transport for audio, voice, and SPP data exchange
- BLE transport for proprietary transparent service and Apple Notification Center Service (ANCS) data exchange

Operating Condition

• Operating voltage: 3.2V to 4.2V
• Operating temperature: -20°C to +70°C

Description

The BM64 Stereo Audio module is a fully qualified Bluetooth 4.2 dual-mode (BDR/EDR/BLE) module for designers to add wireless audio and voice applications to their products. The BM64 module is a Bluetooth Special Interest Group (SIG) certified module that provides a complete wireless solution with Bluetooth stack, integrated PCB antenna, and worldwide radio certifications in a compact surface-mount package.
The BM64 module has several SKUs. The BM64 module is available in both Class 1 and Class 2 versions.

Applications

• Soundbar and Subwoofer (FW dependent)
• Bluetooth portable speaker phone
• Multi-speaker (FW dependent)

1.0 DEVICE OVERVIEW

The BM BM64 Stereo Audio modules are built around Microchip Technology IS2064 SoCs respectively.
The IS2064 SoC integrates the Bluetooth 4.2 dual mode radio transceiver, Power Management Unit (PMU), a crystal and DSP. Users can configure the BM64 module by using the UI tool and DSP tool, a Windows-based utility.

> **Note:** The UI and DSP tools are available for download from the Microchip web site at: www.microchip.com/BM64.

Figure 1-1 illustrates a typical example of the Class 1 BM64 module which is connected to an external MCU and a DSP/codec.

FIGURE 1-1: APPLICATION USING BM64 MODULE

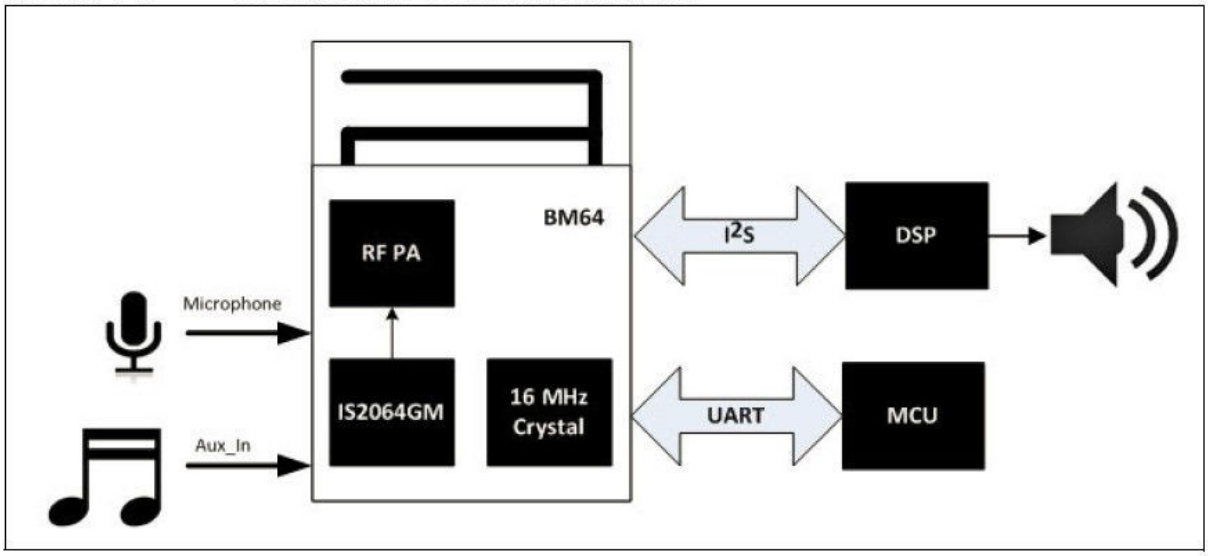


Figure 1-2 illustrates the Soundbar and Subwoofer applications using the BM64 module.

FIGURE 1-2: SOUNDBAR AND SUBWOOFER APPLICATIONS USING BM64 MODULE

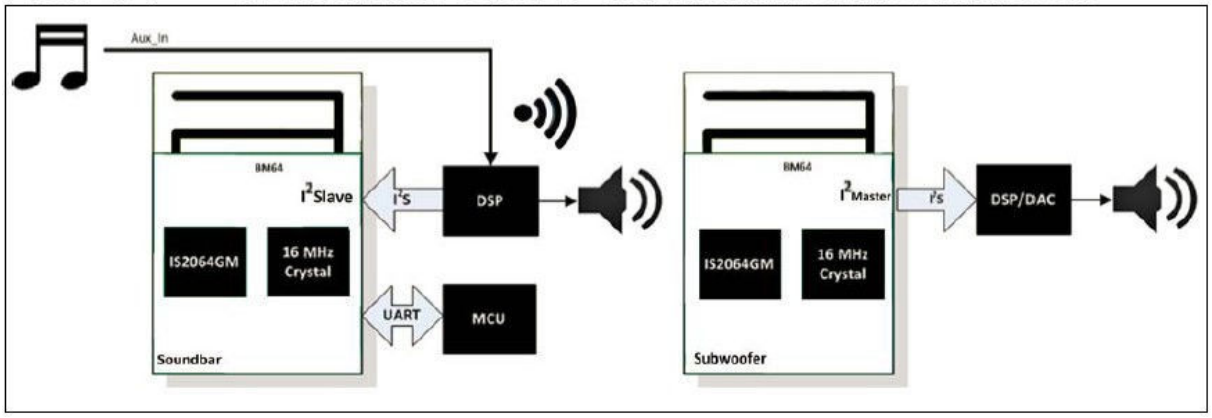


Figure 1-3 illustrates the Soundbar and Subwoofer applications using the BM64 module and smartphone.

FIGURE 1-3: SOUNDBAR AND SUBWOOFER APPLICATIONS USING BM64 MODULE AND SMARTPHONE

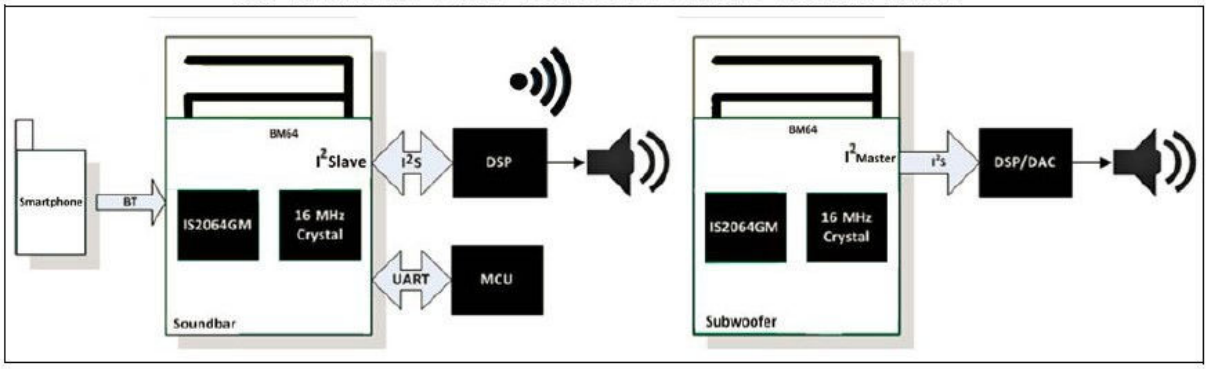


Figure 1-4 illustrates the Multi-speaker application using the BM64 module.

FIGURE 1-4: SOUNDBAR AND SUBWOOFER APPLICATIONS USING BM64 MODULE AND SMARTPHONE

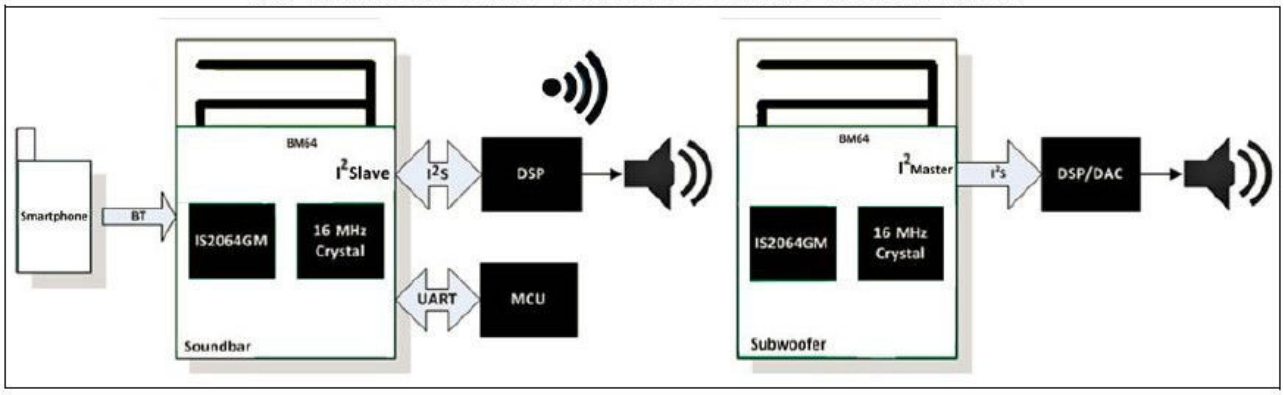


Table 1-1 provides the key features of the BM64 module.

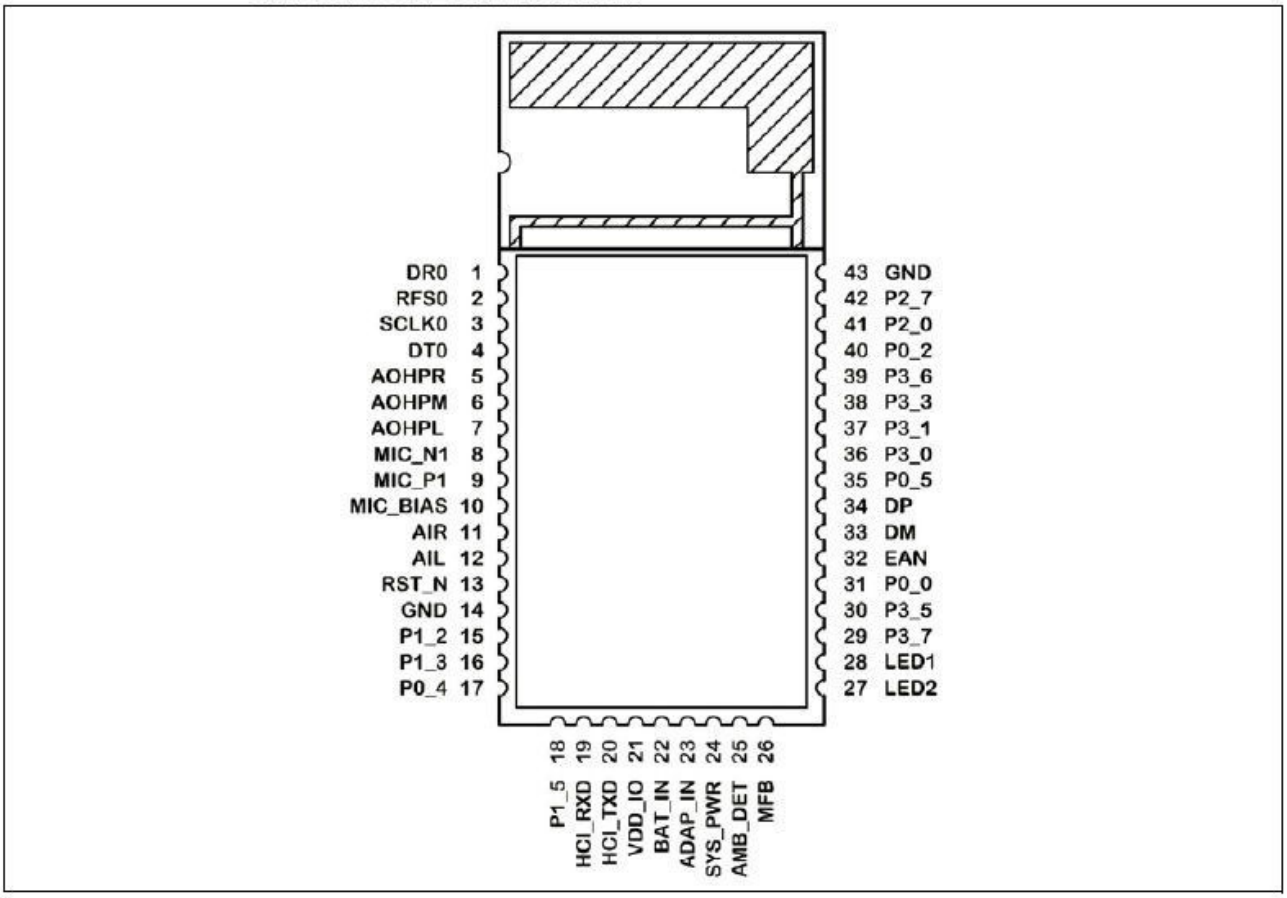
TABLE 1-1: BM62/64 KEY FEATURES

Feature	BM64 CLASS 2	BM64 CLASS 1
Application	Multi-speaker/Soundbar/Subwoofer	
Stereo/mono	Stereo	Stereo
Pin count	43	43
Dimensions (mm^2)	15 x 32	15 x 32
PCB antenna	Yes	Yes
Tx power (typical)	2 dBm	15 dBm
Audio DAC output	2 Channel	2 Channel
DAC (single-ended) SNR at 2.8V (dB)	-98	-98
DAC (capless) SNR at 2.8V (dB)	-98	-98
ADC SNR at 2.8V (dB)	-92	-92
I^2S digital interface	Yes	Yes
Analog AUX-In	Yes	Yes
Mono MIC	1	1
External audio amplifier interface	Yes	Yes
UART	Yes	Yes
USB	Yes	Yes
LED driver	2	2
Internal DC-DC step down regulator	Yes	Yes
DC 5V adapter input	Yes	Yes
Battery charger (350 mA max)	Yes	Yes
ADC for thermal charger protection	Yes	Yes
Undervoltage protection (UVP)	Yes	Yes
GPIO	12	12
Button support	6	6
NFC (triggered by external NFC)	Yes	Yes
EEPROM	Yes	Yes

Feature	BM64 CLASS 2	BM64 CLASS 1
Customized voice prompt	8K Sampling Rate, Stored in EEPROM with approximately 800 bytes/second	
Multi-tone	Yes	Yes
DSP sound effect	Yes	Yes
BLE	Yes	Yes
Bluetooth profiles		
HFP	1.6	1.6
AVRCP	1.6	1.6
A2DP	1.3	1.3
HSP	1.2	1.2
SPP	1.2	1.2

Figure 1-5 illustrates the pin diagram of the BM64 module.

FIGURE 1-5: BM64 MODULE PIN DIAGRAM



BM64 MODULE PIN DESCRIPTION

Pin No	Pin Type	Pin Name	Description
1	I/O	DR0	I^2S interface: digital left/right data
2	I/O	RFS0	I^2S interface: left/right clock
3	I/O	SCLK0	I^2S interface: bit clock
4	I/O	DT0	I^2S interface: digital left/right data
5	O	AOHPR	Right-channel, analog headphone output
6	O	AOHPM	Headphone common mode output/sense input
7	O	AOHPL	Left-channel, analog headphone output
22	P	BAT_IN	Battery input. Voltage range: 3.2V to 4.2V. When an external power supply is connected to the ADAP_IN pin, the BAT_IN pin can be left open if battery is not connected
23	P	ADAP_IN	5V power adapter input
24	P	SYS_PWR	System power output derived from ADAP_IN or BAT_IN
25	P	AMB_DET	Analog input for ambient temperature detection
26	I	MFB	• Multi-Function Button and power-on key • UART RX_IND, active-high (used by host MCU to wakeup the Bluetooth system)
27	I	LED2	LED driver 2
28	I	LED1	LED driver 1

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin
Note: All I/O pins can be configured using the UI tool, a Windows utility.

BM64 MODULE PIN DESCRIPTION (CONTINUED)

Pin No	Pin Type	Pin Name	Description
29	I/O	P3_7	Configurable control or indication pin (Internally pulled-up, if configured as an input) UART TX_IND, active-low (used by Bluetooth system to wakeup the host MCU)
30	I/O	P3_5	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Slide switch detector, active-high
31	I/O	P0_0	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Slide switch detector, active-high, Out_Ind_0
32	I	EAN	External address bus negative System configuration pin along with the P2_0 and P2_4 pins used to set the module in any one of these modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the module) refer to Table 5-1 Flash: must be pulled-down with 4.7 kOhm to GND
33	I/O	DM	Differential data-minus USB
34	I/O	DP	Differential data-plus USB
35	I/O	P0_5	Configurable control or indication pin (Internally pulled-up, if configured as an input) Volume-down key (default), active-low
36	I/O	P3_0	Configurable control or indication pin (Internally pulled-up, if configured as an input) AUX-In detector, active-low
37	I/O	P3_1	Configurable control or indication pin (Internally pulled-up, if configured as an input) REV key (default), active-low
38	I/O	P3_3	Configurable control or indication pin (Internally pulled-up, if configured as an input) FWD key (default), active-low
39	I/O	P3_6	Configurable control or indication pin (Internally pulled-up, if configured as an input) Multi-SPK Master/Slave mode control (FW dependent)
40	I/O	P0_2	Configurable control or indication pin (Internally pulled-up, if configured as an input) Play/Pause key (default)
41	I/O	P2_0	System configuration pin along with P2_4 and EAN pins used to set the module in any one of the following modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the module), refer to Table 5-1
42	I/O	P2_7	Configurable control or indication pin (Internally pulled-up, if configured as an input) Volume-up key (default), active-low
43	P	GND	Ground reference

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin
Note: All I/O pins can be configured using the UI tool, a Windows utility.

2.0 AUDIO

The input and output audios have different stages and each stage can be programmed to vary the gain response characteristics. For microphone, both single ended inputs and differential inputs are supported.
To maintain a high quality signal, a stable bias voltage source to the condenser microphone's FET is provided.
The DC blocking capacitors can be used at both positive and negative sides of a input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

2.1 Digital Signal Processor

A Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction are inbuilt. To reduce nonlinear distortion and to help echo cancellation, an outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. Adaptive filtering is also applied to track the echo path impulse in response to provide echo free and full-duplex user experience.
The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by the microphones and improves mutual understanding in communication.
The advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are inbuilt. The audio effect algorithms are to improve the user's audio listening experience in terms of better audio quality after audio signal processing.
Figure 2-1 and Figure 2-2 illustrate the processing flow of speakerphone applications for speech and audio signal processing.

FIGURE 2-1: SPEECH SIGNAL PROCESSING

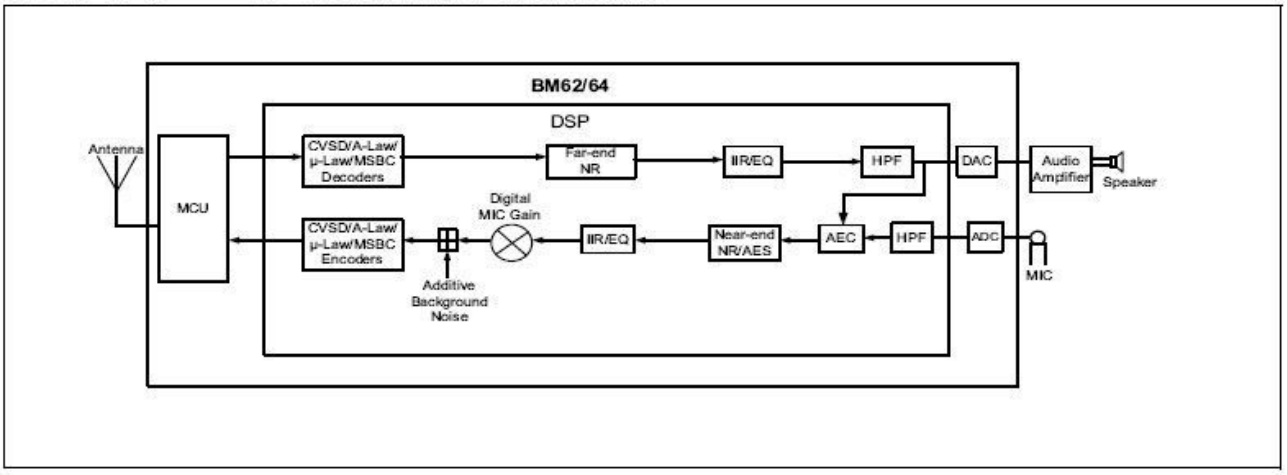
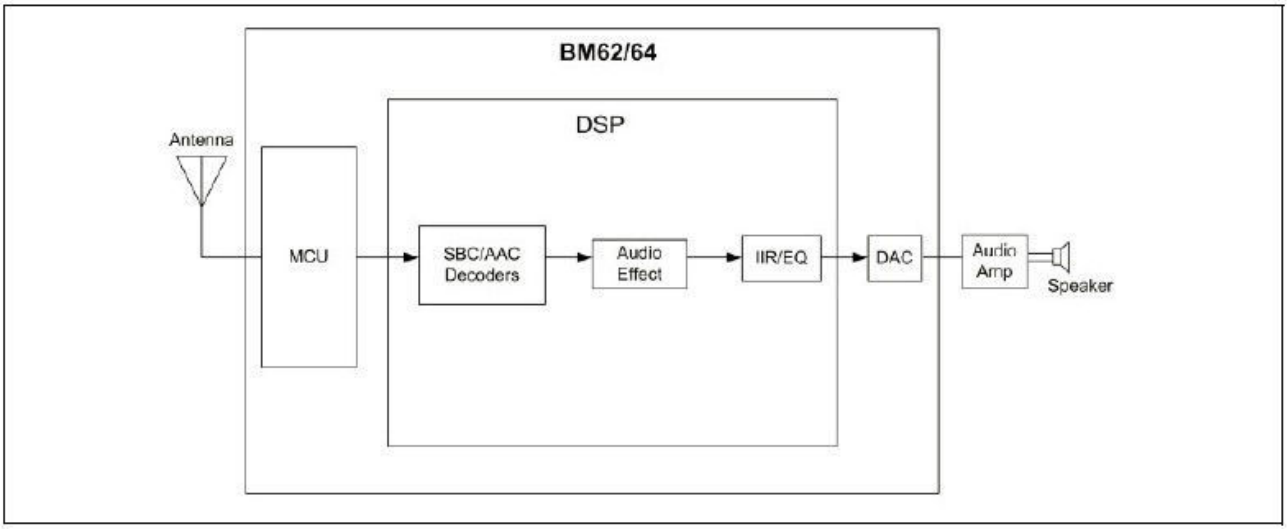


FIGURE 2-2: AUDIO SIGNAL PROCESSING



The DSP parameters can be configured using the DSP tool. For additional information on the DSP tool, refer to the "IS206X DSP Application Note".

Note:	The DSP tool and *"IS206X DSP Application Note"* document, are available for download from the Microchip web site at: www.microchip.com/BM64.

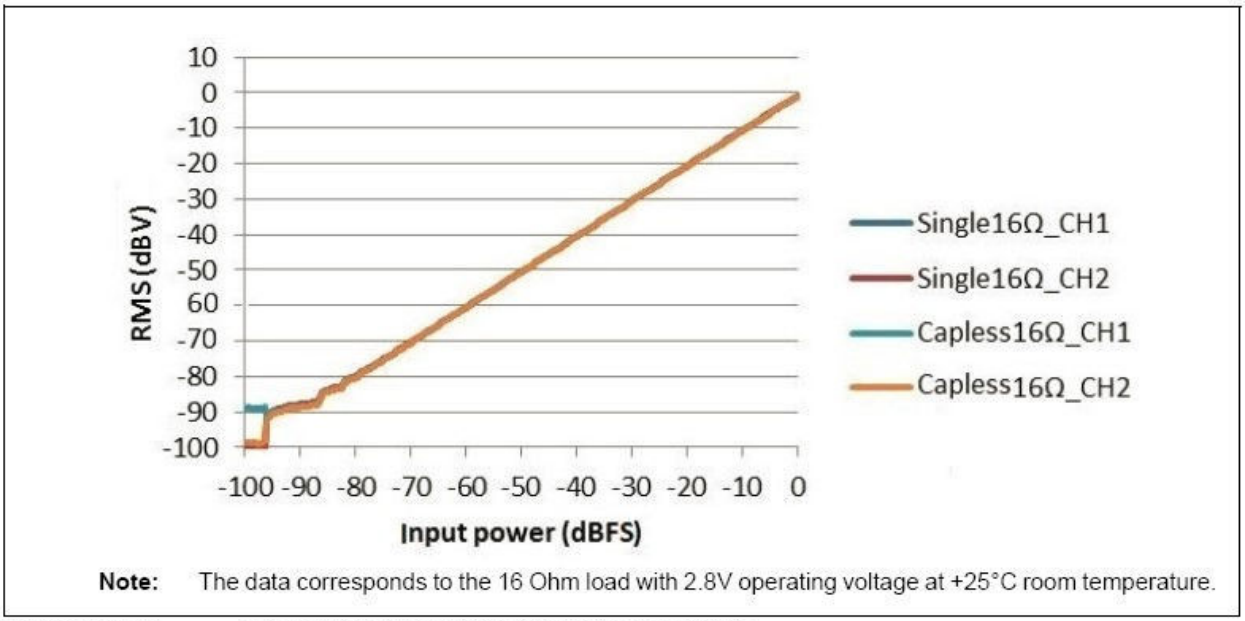
2.2 Codec

The built-in codec has a high signal-to-noise ratio (SNR) performance and it consists of an ADC, a DAC and an additional analog circuitry.

Note:	The internal codec supports 16-bit resolution, by adding trailing zeros in LSBs 24-bit I^2S port requirements can be met.

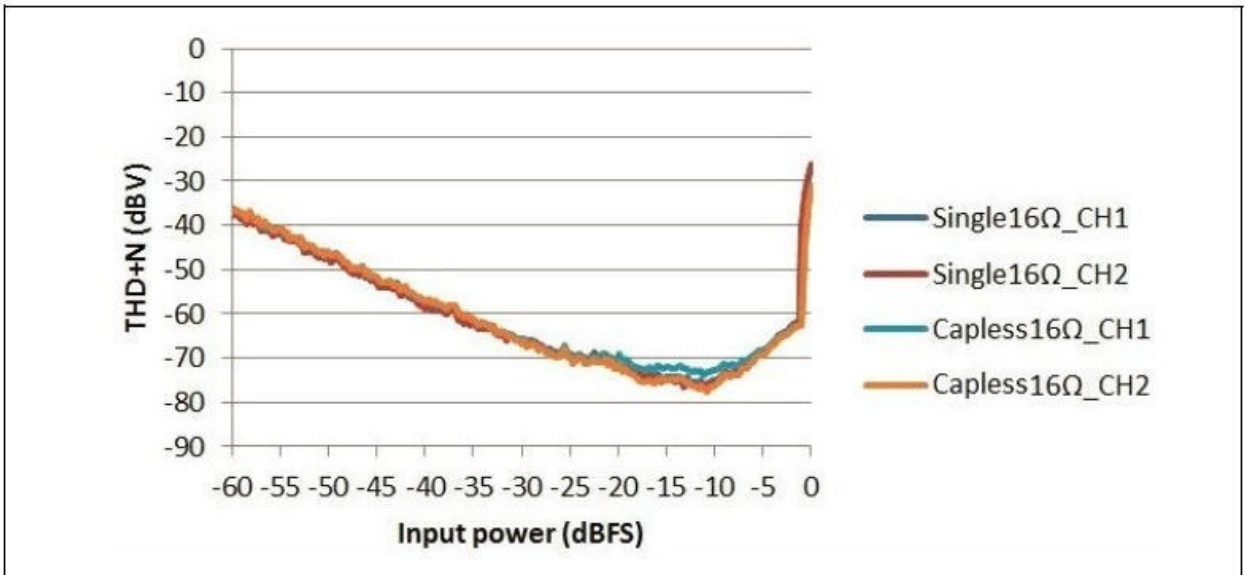
Figure 2-3 through Figure 2-6 illustrate the dynamic range and frequency response of the codec.

FIGURE 2-3: CODEC DAC DYNAMIC RANGE



Note: The data corresponds to the 16 Ohm load with 2.8V operating voltage at +25°C room temperature.

FIGURE 2-4: CODEC DAC THD+N VERSUS INPUT POWER



Note: The data corresponds to the 16 Ohm load with 2.8V operating voltage at +25°C room temperature.

FIGURE 2-5: CODEC DAC FREQUENCY RESPONSE (CAPLESS MODE)

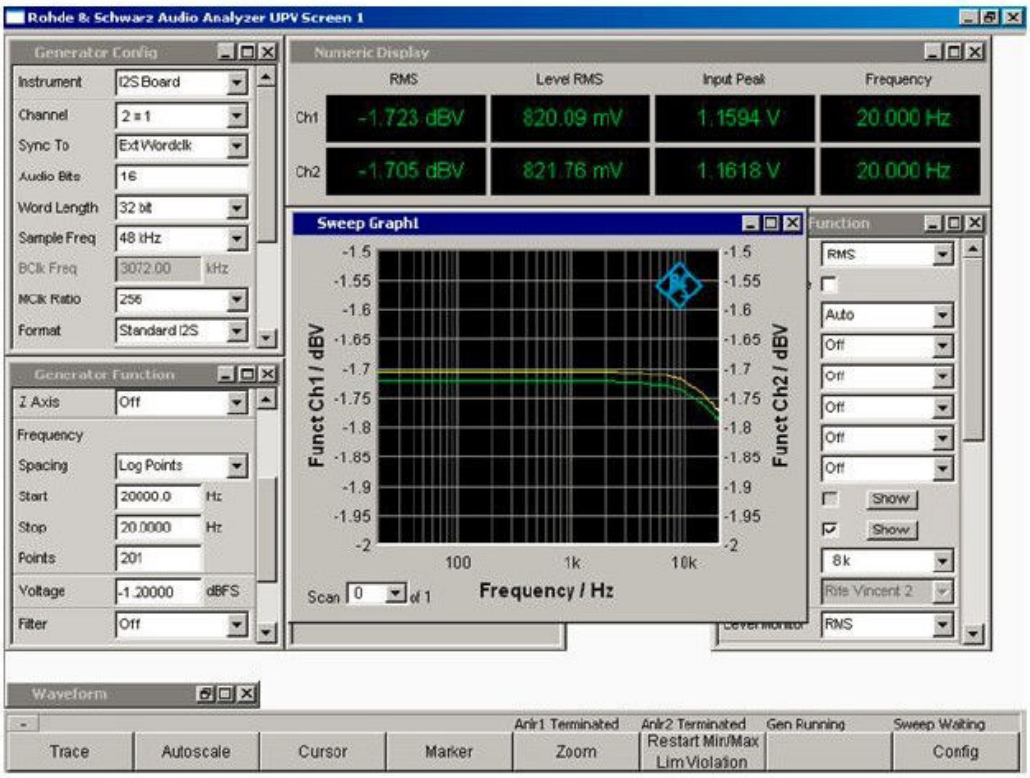
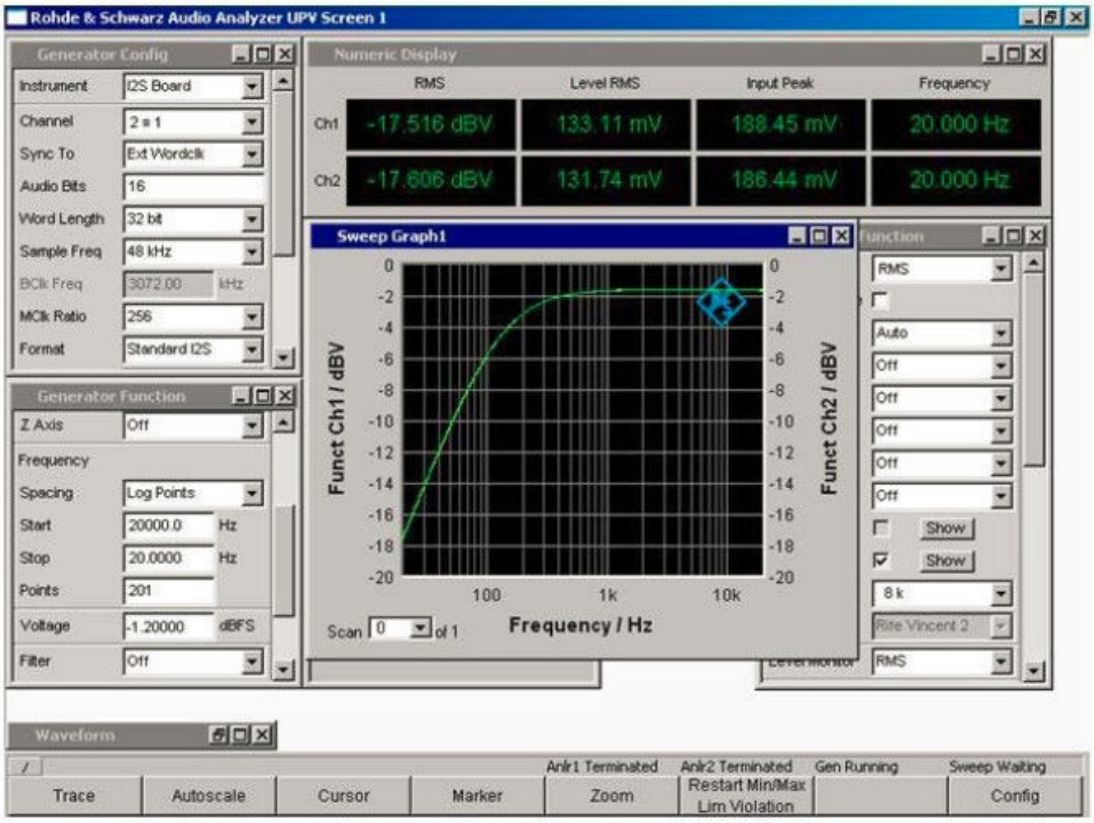


FIGURE 2-6: CODEC DAC FREQUENCY RESPONSE (SINGLE-ENDED MODE)



Note: The DAC frequency response corresponds to single-ended mode with a 47 µF DC block capacitor.

2.3 Auxiliary Port

The BM64 module supports one analog (line-in) signal from the external audio source. The analog (line-in) signal can be processed by the DSP to generate different sound effects (Multi-band dynamic range compression and audio widening), which can be configured by using the DSP tool.

2.4 Analog Speaker Output

The BM62/64 module supports the following analog speaker output modes:

• Capless mode — Recommended for headphone applications in which capless output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. Figure 2-7 illustrates the analog speaker output capless mode

• Single-ended mode — Used for driving an external audio amplifier where a DC blocking capacitor is required. Figure 2-8 illustrates the analog speaker output single-ended mode

FIGURE 2-7: ANALOG SPEAKER OUTPUT CAPLESS MODE

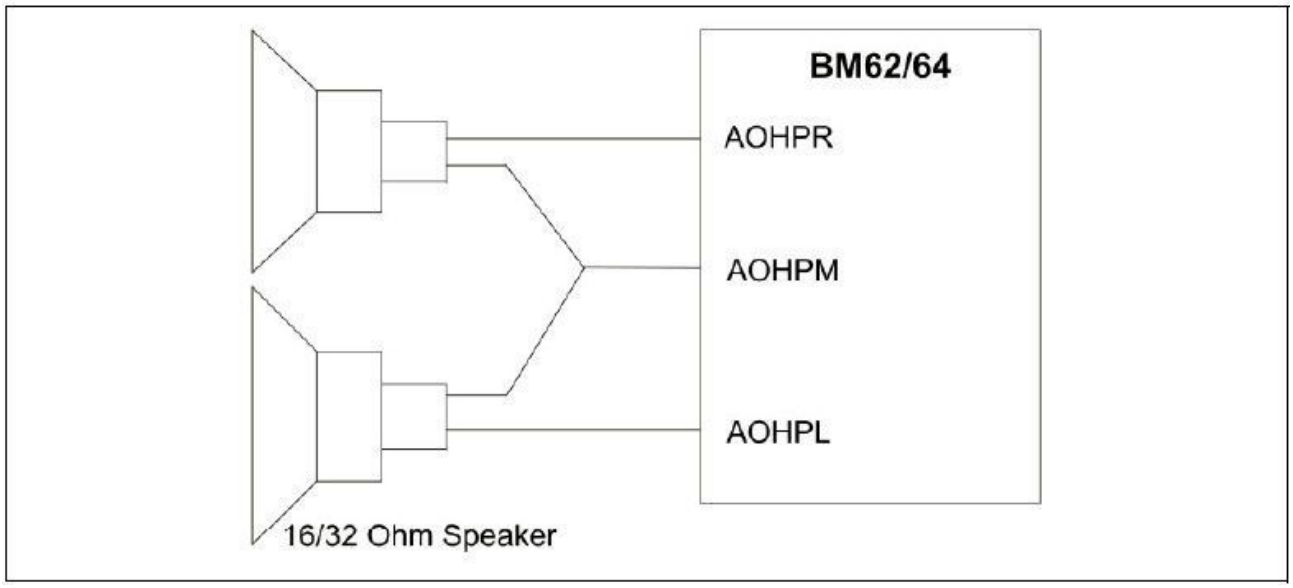
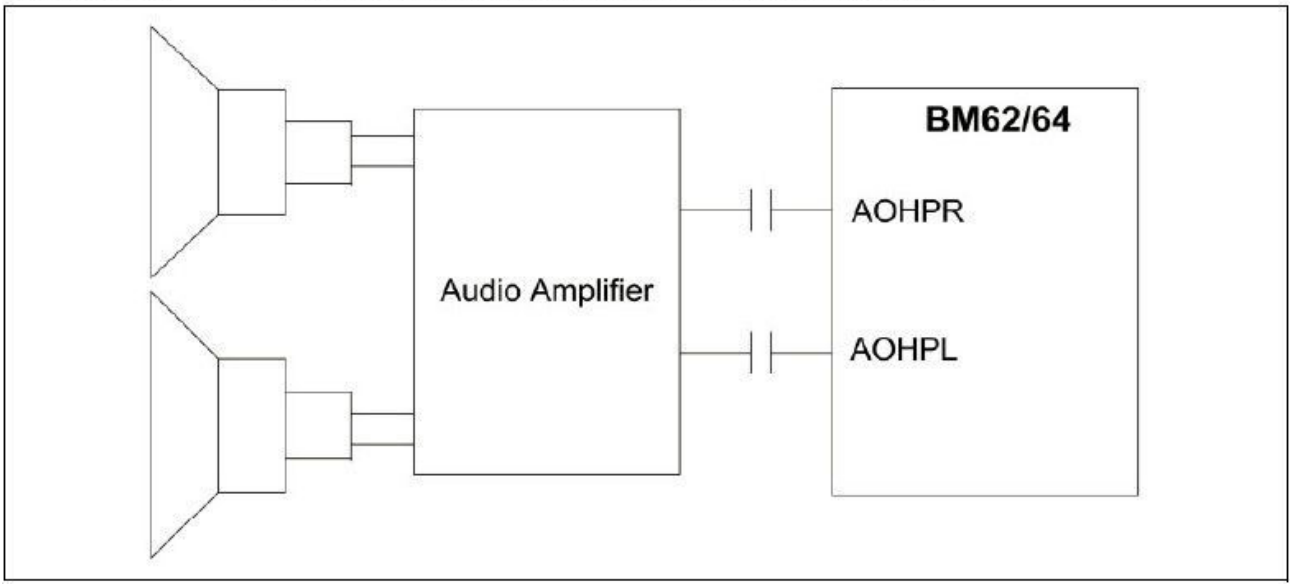


FIGURE 2-8: ANALOG SPEAKER OUTPUT SINGLE-ENDED MODE



3.0 TRANSCEIVER

The BM64 module is designed and optimized for Bluetooth 2.4 GHz system. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronizing with another device.

3.1 Transmitter

The internal power amplifier (PA) has a maximum output power of +4 dBm. This is applied for Class 2 or Class 3 radios without an external RF PA. The transmitter performs the IQ conversion to minimize the frequency drift.

3.2 Receiver

The low-noise amplifier (LNA) operates with TR-combined mode for single port application. It can save a pin on the package without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into a digital signal for demodulator analysis.
A channel filter has been integrated into the receiver channel before the ADC, which is used to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject the image frequency for low-IF architecture. This filter for low-IF architecture is intented to reduce external Band Pass Filter (BPF) component for a super heterodyne architecture.

The Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

3.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside with a tunable internal LC tank that can reduce variation for components. Acrystal oscillator with an internal digital trimming circuitprovides a stable clock for the synthesizer.

3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps was the standard data rate based on the Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with Enhanced Data Rate (EDR) specifications.

For Bluetooth 2.0 and above specifications, EDR has been introduced to provide the data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packet represents 2/3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8 DPSK.

3.5 Adaptive Frequency Hopping(AFH)

The BM62/64 module has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose clear channel for transceiver Bluetooth signal.

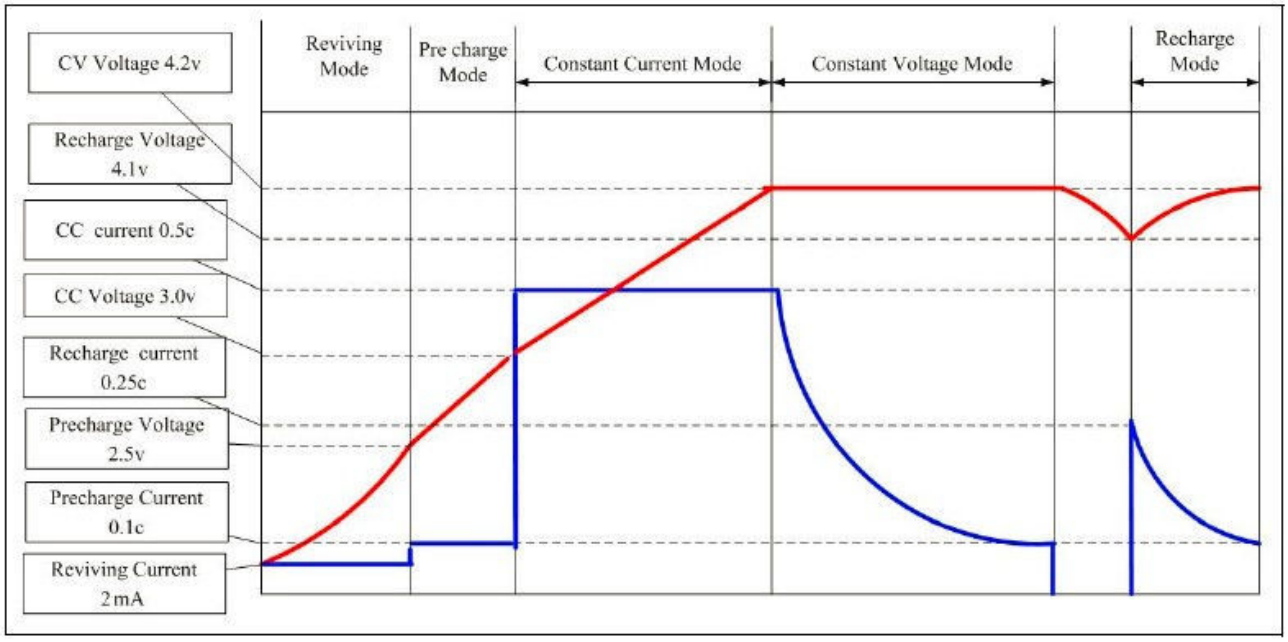
4.0 POWER MANAGEMENT UNIT

The on-chip Power Management Unit (PMU) has two main features: lithium-ion and lithium-polymer battery charger, and voltage regulator A power switch is used to switch over the power source between the battery and an adapter. Also, the PMU provides current to drive two LEDs.

4.1 Charging a Battery

The BM62/64 module has a built-in battery charger which is optimized for lithium-ion and lithium-polymer batteries. The battery charger includes a current sensor for charging control, user programmable current regulation, and high accuracy voltage regulation. The charging current parameters are configured by the UI tool. Reviving, pre-charging, constant current and constant voltage modes, and re-charging functions are included. The maximum charging current is 350 mA.
Figure 4-1 illustrates the charging curve of a battery.

FIGURE 4-1: BATTERY CHARGING CURVE



4.2 Voltage Monitoring

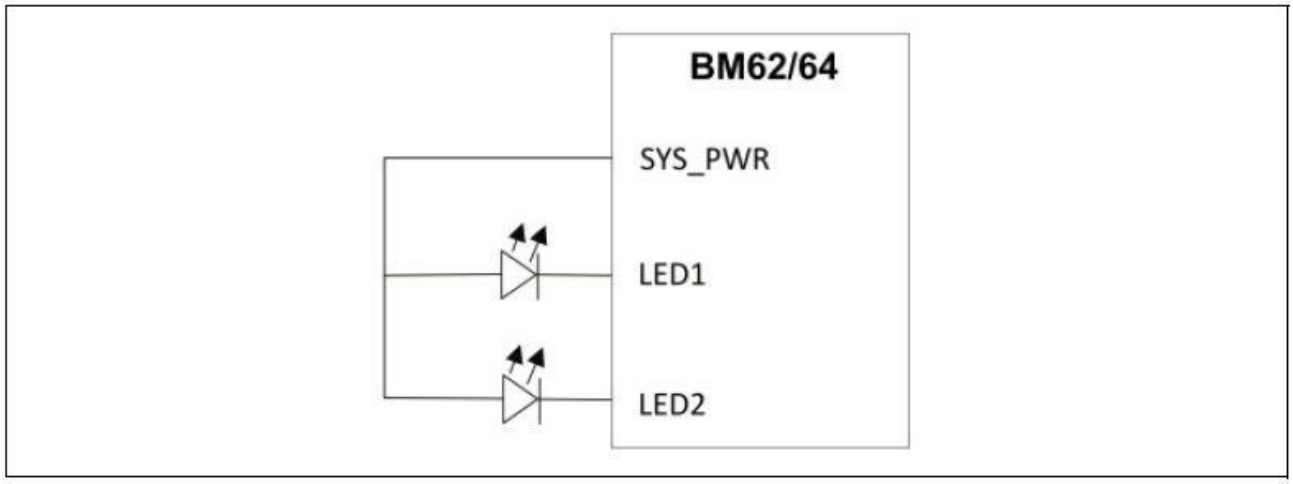
A 10-bit, successive approximation register ADC (SAR ADC) provides a dedicated channel for battery voltage level detection. The warning level can be programmed by using the UI tool. The ADC provides a granular resolution to enable the external MCU to take control over the charging process.

4.3 LED Driver

Two dedicated LED drivers control the LEDs. They provide enough sink current (16 step control and 0.35 mA for each step), thus LEDs can be connected directly with the BM62/64 module. The LED settings can be configured using the UI tool.

Figure 4-2 illustrates the LED drivers in the BM62/64 module.

FIGURE 4-2: LED DRIVER



4.4 Under Voltage Protection

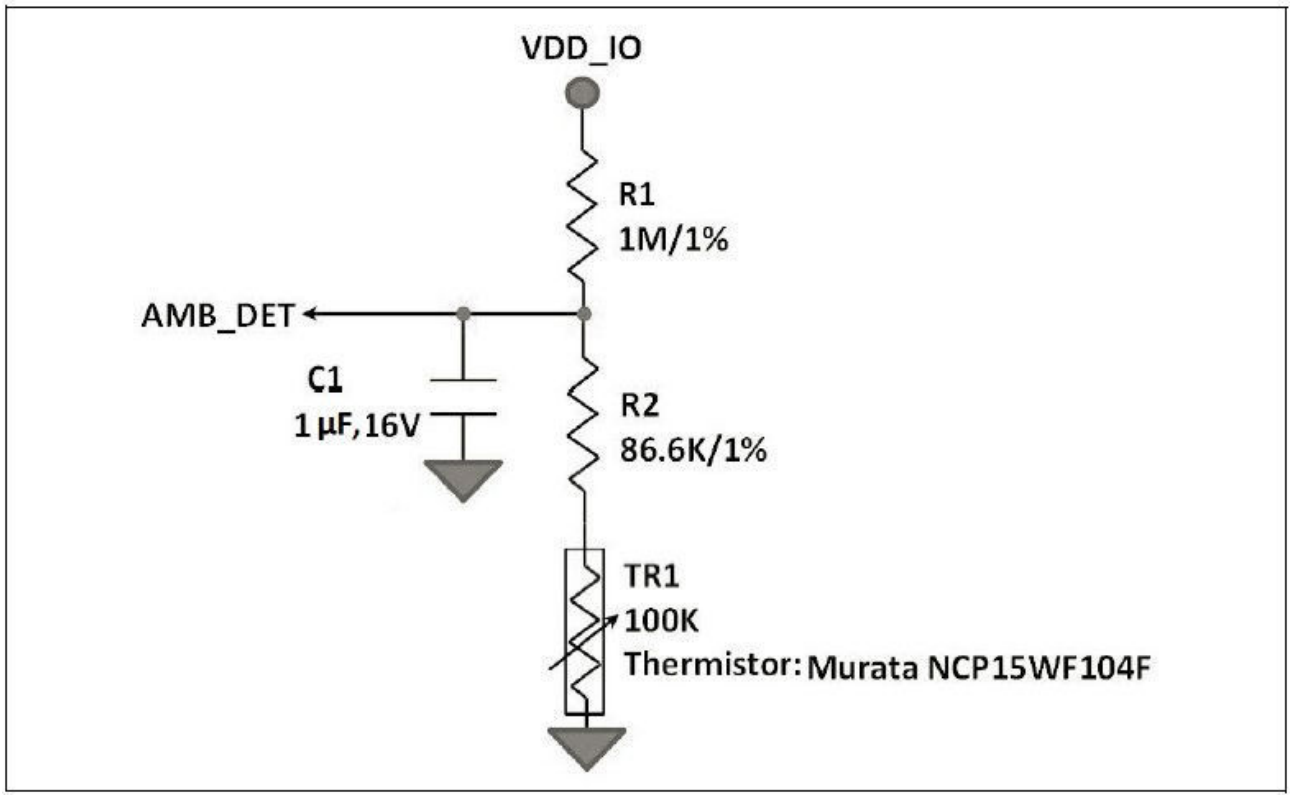
When the voltage of the SYS_PWR pin drops below the voltage level of 2.9V, the system will shutdown automatically.

4.5 Ambient Detection

The BM64 module has a built-in ADC for charger thermal protection. Figure 4-3 illustrates the suggested circuit and thermistor, Murata NCP15WF104F. The charger thermal protection can avoid battery charge in restricted temperature range. The upper and lower limits for temperature values can be configured by using the UI tool.

Note:	Thermistor must be placed close to the battery in the user application for accurate temperature measurements and to enable thermal shutdown feature.

FIGURE 4-3: AMBIENT DETECTION

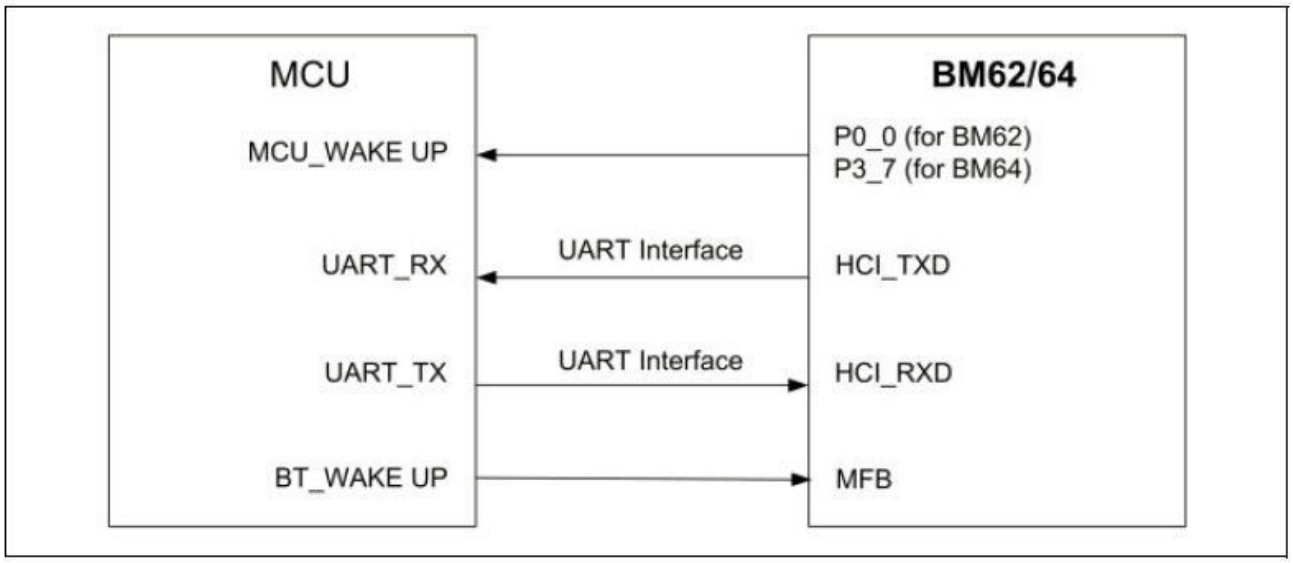


5.0 APPLICATION INFORMATION

5.1 Host MCU Interface

The BM64 module supports UART commands. The UART commands enable an external MCU to control the BM64 module. Figure 5-1 illustrates the UART interface between the BM64 module and an external MCU.

FIGURE 5-1: HOST MCU INTERFACE OVER UART



An external MCU can control the BM64 module over the UART interface and wakeup the module with the MFB, P3_7

pins.
Refer to the "UART_CommandSet" document for a list of functions the BM64 module supports and how to use the UI tool to configure the UART and UART Command Set tool.

Note: The UART Command set tool (SPKCommandSetTool v160.xx) and "*UART_CommandSet*" document are available for download from the Microchip web site at: www.microchip.com/BM64.

Figure 5-2 through Figure 5-7 illustrate the timing sequences of various UART control signals.

FIGURE 5-2: POWER-ON/OFF SEQUENCE

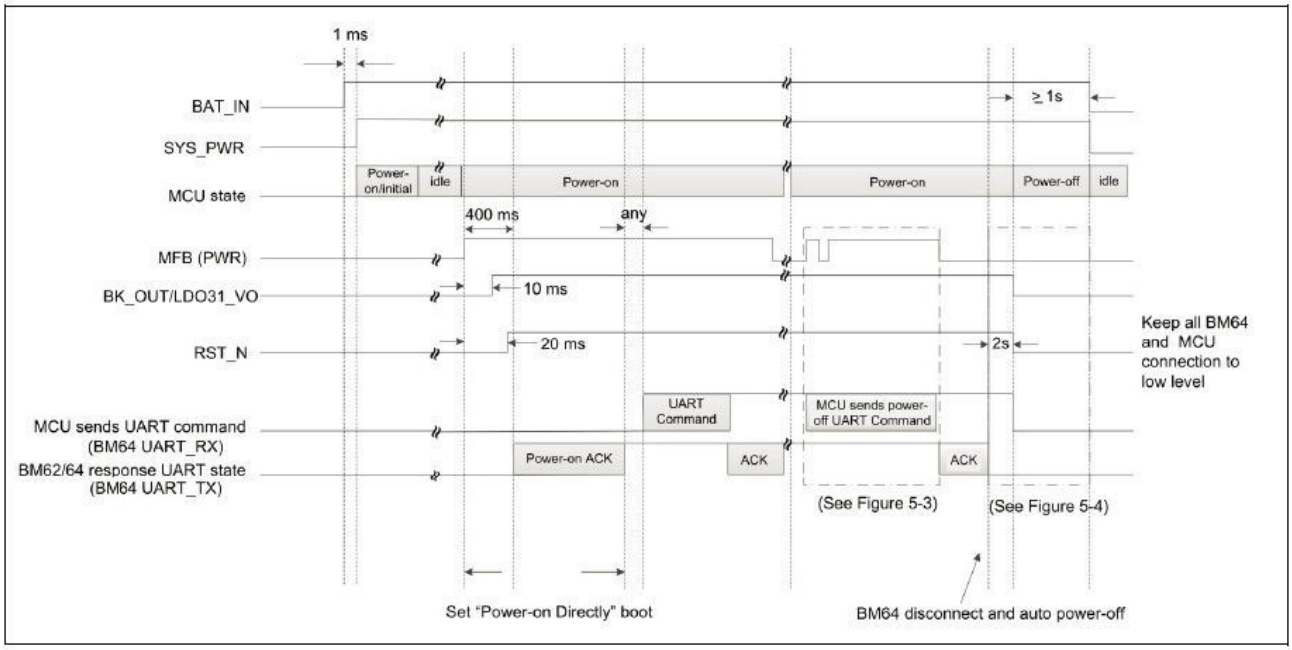


FIGURE 5-3: TIMING SEQUENCE OF RX INDICATION AFTER POWER-ON STATE

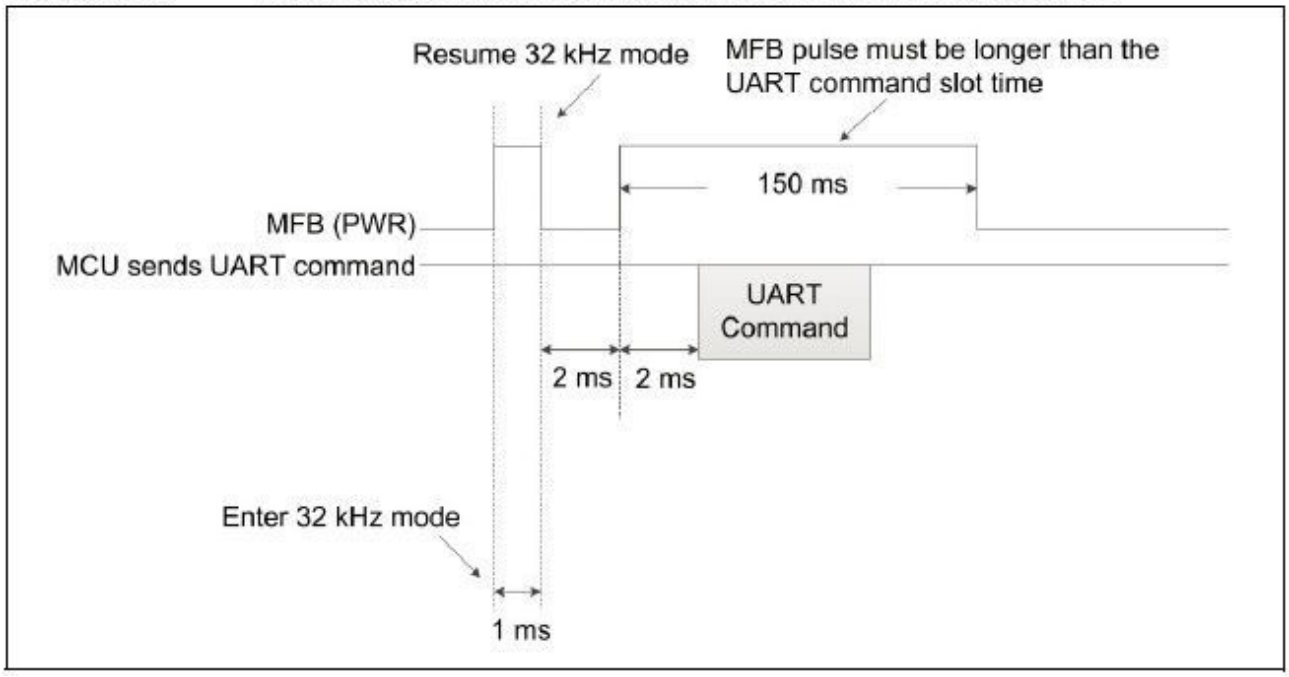
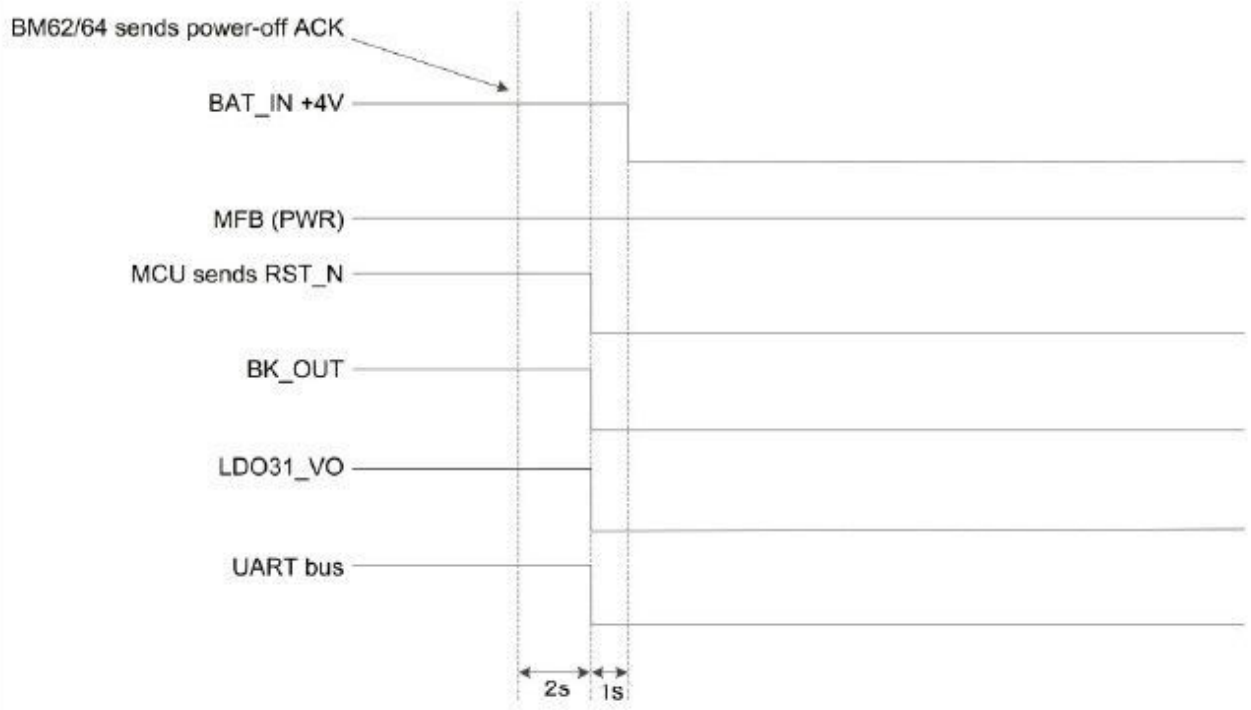


FIGURE 5-4: TIMING SEQUENCE OF POWER-OFF STATE



Note 1: EEPROM clock = 100 kHz.

2: For a byte write: 0.01 ms x 32 clock x 2 = 640 µs.

3: It is recommended to have ramp-down time more than 640 µs during the power-off sequence to ensure safe operation of the device.

FIGURE 5-5: TIMING SEQUENCE OF POWER-ON (NACK)

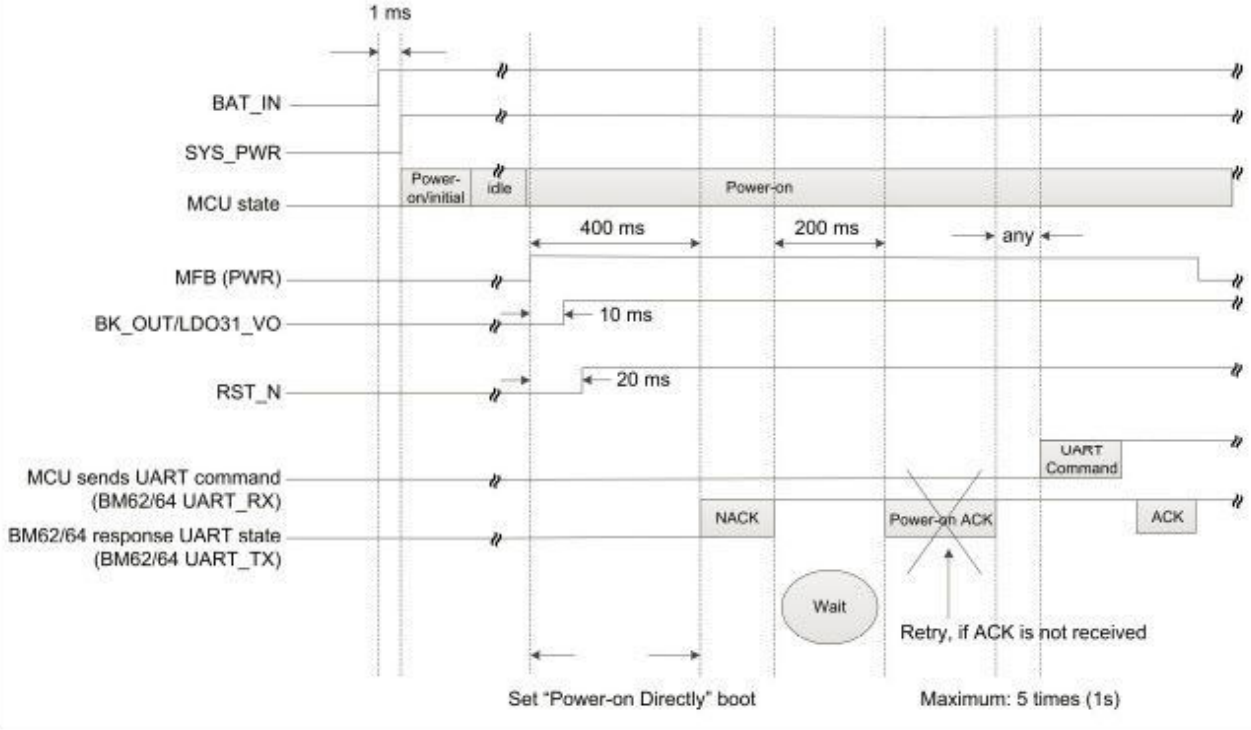
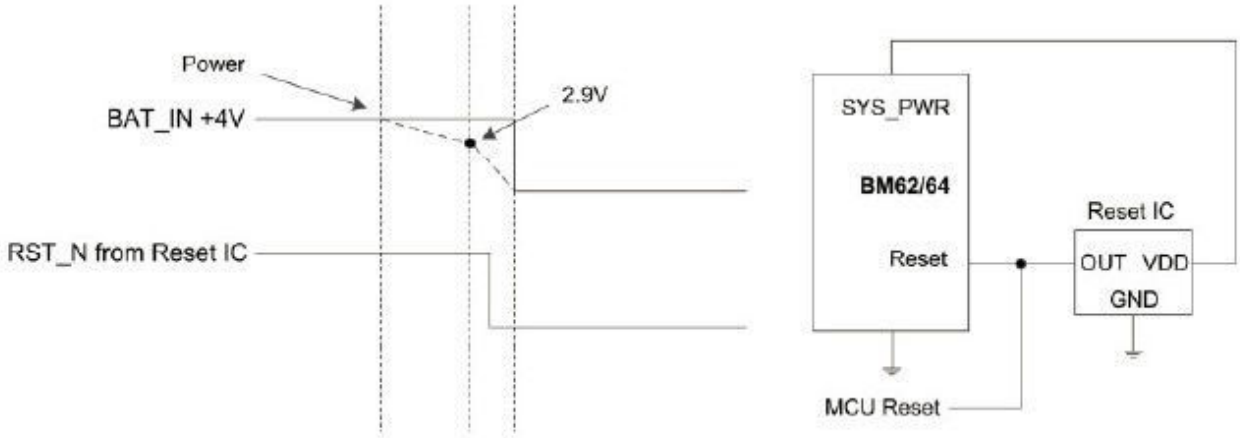


FIGURE 5-7: TIMING SEQUENCE OF POWER DROP PROTECTION



Note 1: It is recommended to use the battery to provide the power supply at BAT_IN in to the module.

2: If an external power source or a power adapter is utilized to provide power to the module (ADAP_IN), it is recommended to use a voltage supervisor IC.

3: The Reset IC output pin, RST_N, must be "Open drain" with delay time ≦ 10 ms and the recommended part is G691L293T73.

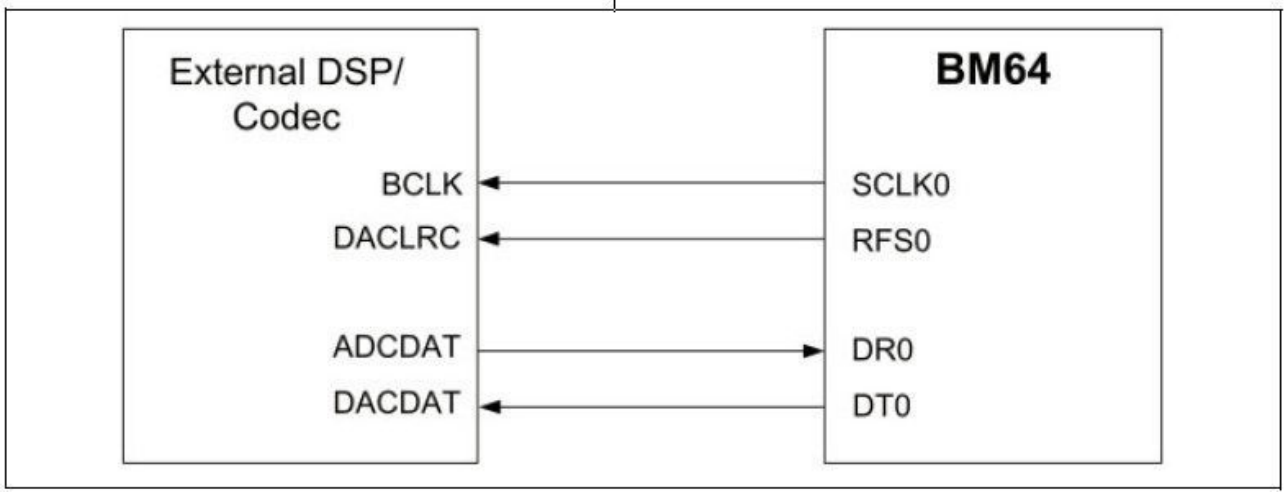
5.2 I2S Mode Application

The BM64 module provides an I2S digital audio output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2, and 96 kHz sampling rates for 16-bit and 24-bit data formats. The I2S setting can be configured by using the UI and DSP tools.

Figure 5-8 and Figure 5-9 illustrate the I2S signal connectionbetween the BM64 module and an external DSP. Use the DSP tool to configure the BM64 module as a Master/Slave. For additional information on timing specifications, refer to

8.2 “Timing specifications”.

FIGURE 5-8: BM64 MODULE IN I²S MASTER MODE



5.3 Reset

The BM64 module provides a watchdog timer (WDT) to reset the chip. It has an integrated Power-on Reset (POR) circuit that will reset all circuits to a known Power-on state. This action can also be driven by an external Reset signal which is used to control the device externally by forcing it into a POR state. The RST_N signal input is active-low and no connection is required in most applications.

5.4 External Configuration and Programming

The BM64 module can be configured by using an external configuration tool (EEPROM tool) and the firmware is programmed by using a programming tool (Flash tool).

Note:	The EEPROM and Flash tools are available for download from the Microchip web www.microchip.com/BM64.

Figure 5-15 through Figure 5-18 illustrate the BM64 reference circuit for a stereo headset application.

FIGURE 5-15: BM64 REFERENCE CIRCUIT FOR STEREO HEADSET APPLICATION

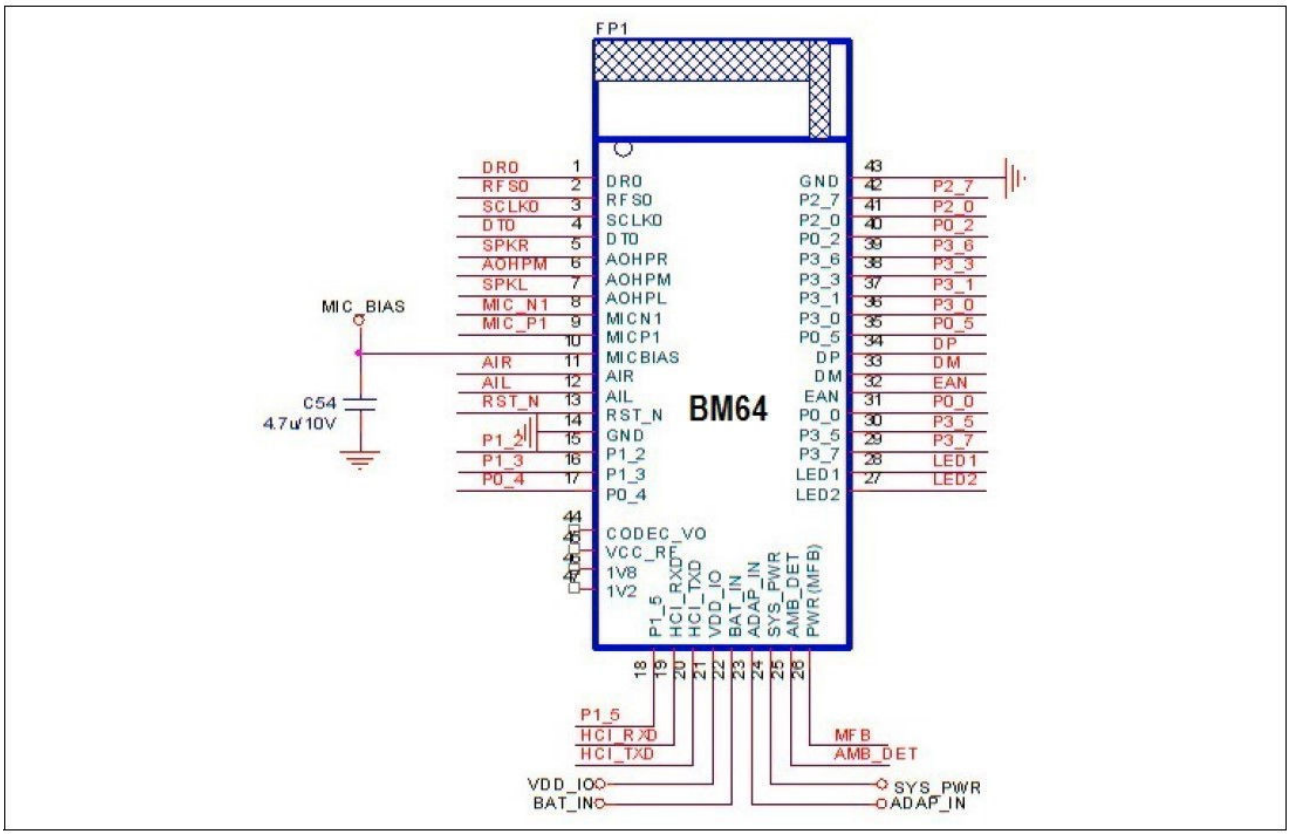
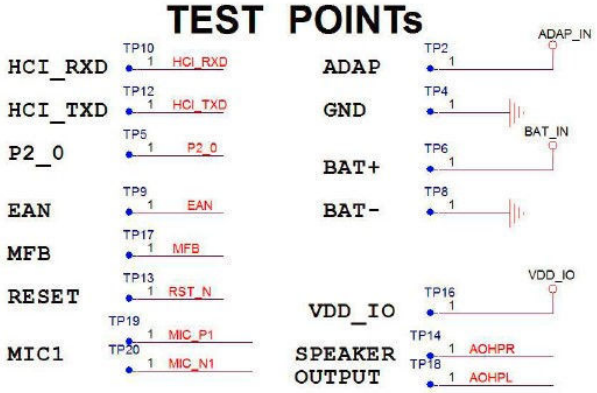


FIGURE 5-16: BM64 REFERENCE CIRCUIT FOR STEREO HEADSET APPLICATION



GPIO	Description
MFB	UART_RX_IND; MFB
P0_2	PLAY / PAUSE
P2_7	VOL+
P0_5	VOL-
P0_0	SLIDE SWITCH
P0_4	AMP_EN; NFC
P3_0	AUX IN Detection
P3_1	REV
P3_3	FWD
P3_7	UART_TX_IND
P1_5	AMP_EN; SLIDE SWITCH
	Single / Double setting
P3_6	Single / Double setting
P2_0	System Configuration
EAN	System Configuration

FIGURE 5-17: BM64 REFERENCE CIRCUIT FOR STEREO HEADSET APPLICATION

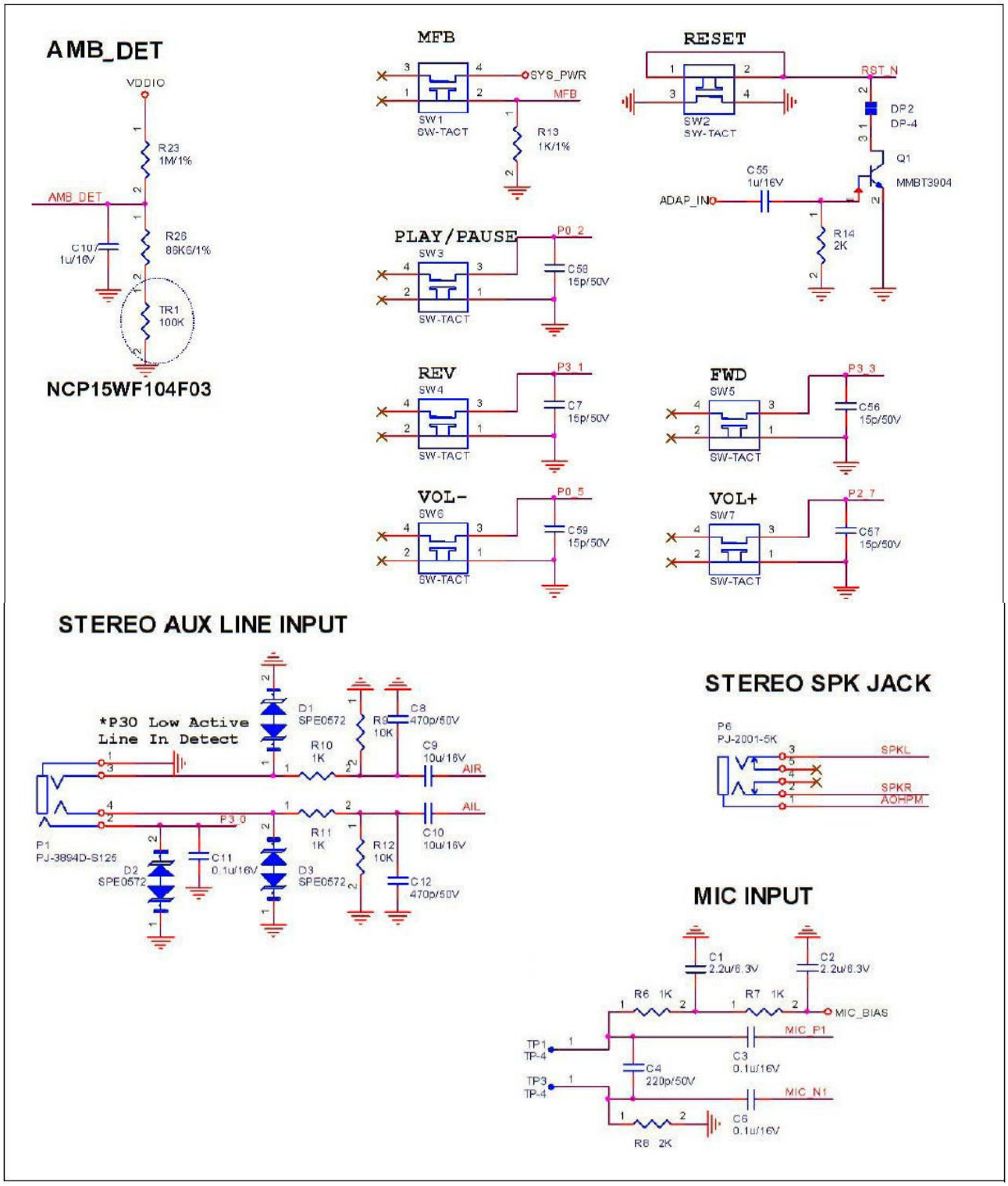
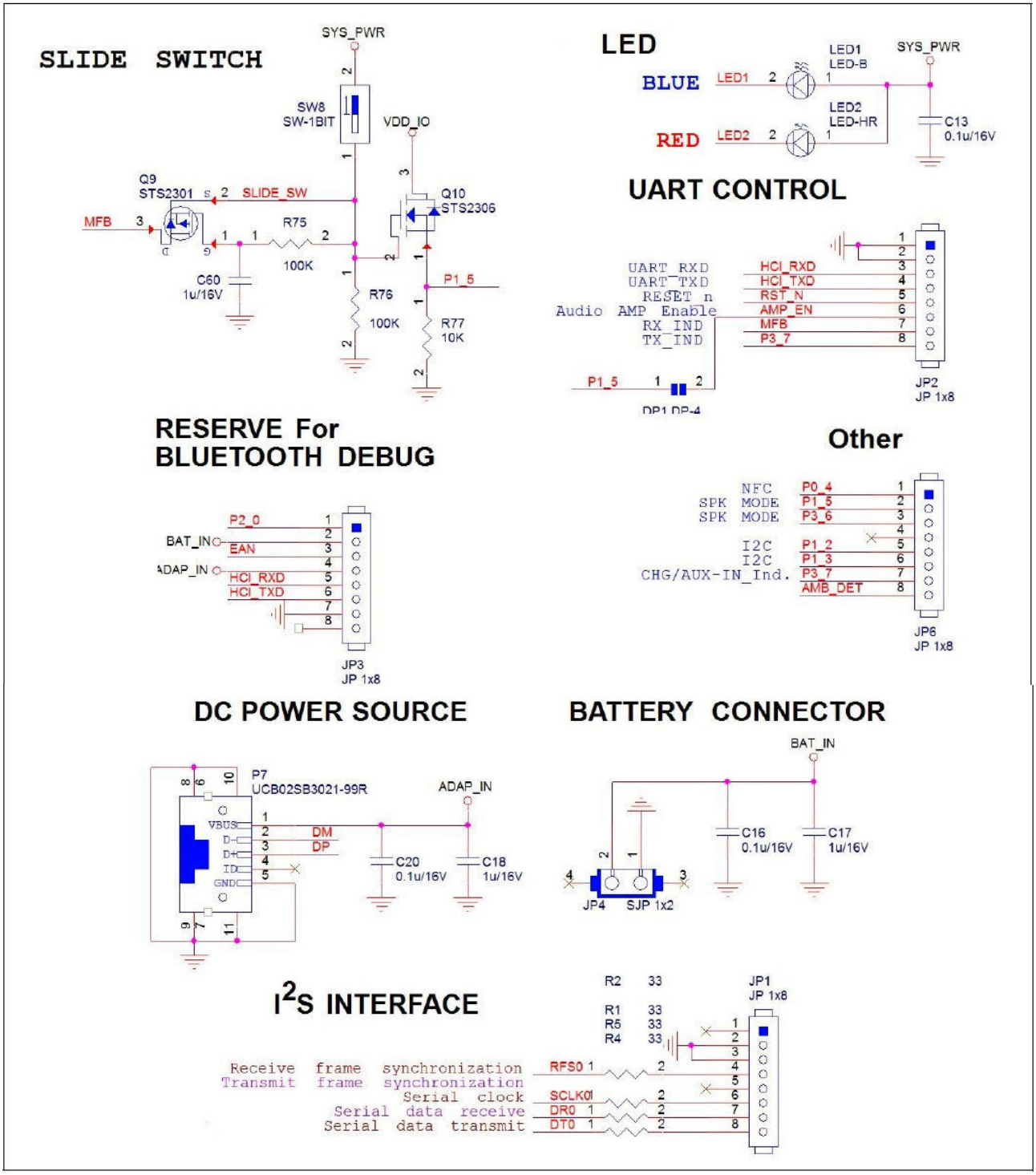


FIGURE 5-18: BM64 REFERENCE CIRCUIT FOR STEREO HEADSET APPLICATION



6.0 PRINTED ANTENNA INFORMATION

6.1 Antenna Radiation Pattern

The BM64 module is integrated with one PCB printed antenna, see Figure 6-1.