

H8DMT/H8DMT-F H8DMT-IBX/H8DMT-IBXF Serverboards



H8DMT/H8DMT-IBX



H8DMT-F/H8DMT-IBXF

User's Manual

Revison 1.0a

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Manual Revison 1.0a

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Preface

About this Manual

This manual is written for system integrators, PC technicians and knowledgeable PC users. It provides information for the installation and use of the H8DMT/H8DMT-IBX/H8DMT-F/H8DMT-IBXF serverboards. All these serverboards are based on the nVidia MCP55 Pro chipset and support AMD Opteron™ processors with up to 64 GB of DDR2-800/667/533/400 registered ECC SDRAM.

The differences between these serverboards is that some have full IPMI capability, some have InfiniBand components and some have both or neither capability. Refer to the chart below for details on which boards have which capabilities.

| Serverboard | Full IPMI Capability | InfiniBand Components |
|-------------|-------------------------|--------------------------|
| H8DMT | - | - |
| H8DMT-F | X | - |
| H8DMT-IBX | - | X |
| H8DMT-IBXF | X | X |

Please refer to the motherboard specifications pages on our web site for updates on supported processors (http://www.supermicro.com/aplus/). This product is intended to be professionally installed.

Manual Organization

Chapter 1 – This chapter includes a checklist of what should be included in your Serverboard box. It also describes the features, specifications and performance of the Serverboard along with detailed information about the chipset.

Chapter 2 – This chapter begins with instructions on handling static-sensitive devices. Read this chapter when installing the processor(s) and memory modules and when installing the motherboard in a chassis. Also refer to this chapter to connect the hard disk drives, the various ports, power and reset buttons and system LEDs. Sections on enabling SATA RAID and system drivers are also included.

Chapter 3 – If you encounter any problems, see this chapter, which describes troubleshooting procedures for the video, memory and the setup configuration stored in CMOS. For quick reference, a general FAQ (Frequently Asked Questions) section is provided. Instructions are also included for contacting technical support.

Chapter 4 – This chapter includes an introduction to the motherboard's BIOS and provides detailed information on running the CMOS Setup utility.

Appendix A – This appendix provides BIOS Error Beep Code Messages.

Appendix B – This appendix lists BIOS POST Checkpoint Codes.

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Notes

Chapter 1 Introduction

1-1 Overview

Congratulations on purchasing your computer Serverboard from an acknowledged leader in the industry. Supermicro boards are designed with the utmost attention to detail to provide you with the highest standards in quality and performance.

Checklist

Please check that the following items have all been included with your motherboard. If anything listed here is damaged or missing, contact your retailer.

Included with retail box only:

- One (1) H8DMT/H8DMT-IBX/H8DMT-F/H8DMT-IBXF Serverboard
- Two (2) SATA cables (CBL-0288L)
- One (1) CD containing drivers and utilities

1-2 Images and Layouts



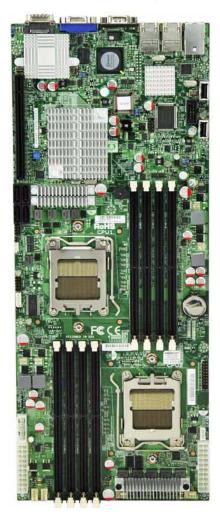




Figure 1-2. H8DMT-F/H8DMT-IBXF Family Serverboard Image



NOTE: The H8DMT/H8DMT-F serverboards shares the same layout as the H8DMT-IBX/H8DMT-IBXF serverboards, but do not include InfiniBand components. The H8DMT-F/ H8DMT-IBXF serverboards have full IPMI capability and a dedicated LAN port above the two USB ports, whereas the H8DMT/H8DMT-IBX serverboards do not.

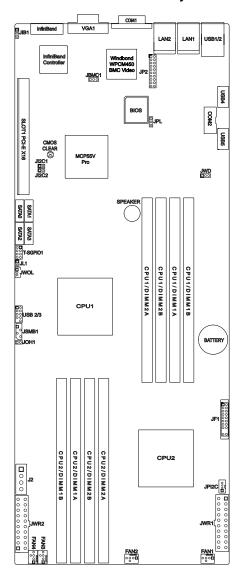


Figure 1-3. H8DMT-IBX/H8DMT-IBXF Family Serverboard Layout



NOTE: Jumpers used for test or debug purposes only are not indicated.

1-3 Quick Reference

Table 1-1. Jumpers

| Jumper | Description | Default Setting |
|---------------------------------------|--|-----------------------|
| JBT1 | CMOS Clear | (see Section 2-7) |
| JBMC1 | BMC and Video Enable Header | Pins 1-2 (Enabled) |
| JI ² C1/JI ² C2 | I ² C to PCI-E Slot | Both Closed (Enabled) |
| JIB1 | InfiniBand Enable/Disable (H8DMT/H8DMT-IBX only) | Pins 1-2 (Enabled) |
| JPL | LAN Controller | Pins 1-2 (Enabled) |
| JWD | Watch Dog | Pins 1-2 (Reset) |

Table 1-2. Connectors

| Connector | Description |
|---------------------|--|
| COM1/COM2 | COM1 Serial Port/Header |
| FAN 1-4 | Chassis/CPU Fan Headers |
| J2 | Auxiliary Power Connector (for IDE drives) |
| JF1 | Front Panel Connector |
| JL1 | Chassis Intrusion Header |
| JOH1 | Overheat Warning Header |
| JWOL | Wake-On-LAN Header |
| JWR1 | 20-Pin Proprietary Power Connector |
| JWR2 | 20-Pin Proprietary Power Connector |
| LAN 1/2 | Gigabit Ethernet (RJ45) Ports |
| Dedicated LAN | Gigabit Ethernet (RJ45) Port (H8DMT-F/H8DMT-IBXFonly) |
| PWRI ² C | Power I ² C Header |
| SATA0 ~ SATA3 | SATA Ports |
| SMBus | System Management Bus Header (H8DMT-F/H8DMT-IBXF only) |
| T-SGPIO-1 | Serial General Purpose Input/Output Header |
| USB0/1, USB2/3/4/5 | Universal Serial Bus (USB) Ports, Headers |

Table 1-3. LEDs

| LED | Description |
|-----|--------------------------------------|
| DP4 | Onboard Power LED |
| LE2 | InfiniBand Physical Link LED (Red) |
| LE3 | InfiniBand Logical Link LED (Yellow) |

1-4 Serverboard Features

CPU Dual AMD Opteron 2000 series processors (Socket F type)

NOTE: Refer to our web site for details on supported processors.

Memory Eight dual channel DIMM slots supporting up to 64 GB of DDR2-800/667/533

registered ECC SDRAM

NOTE: Refer to Section 2-4 before installing memory.

NOTE: Please refer to the latest updated tested memory lists on the

motherboard web site.

Chipset nVidia MCP55 Pro Chipset

Expansion Slots One (1) PCI-Express x16 slot

BIOS features include: APM 1.2, DMI 2.3, PCI 2.2, ACPI 1.0 (ACPI 2.0 is BIOS

supported), BIOS rescue hot keys, Hardware BIOS virus protection,

SMBIOS 2.3, Plug and Play (PnP)

PC Health Monitoring

BIOS

· Onboard voltage monitors

8 Mb AMI® LPC Flash ROM

Fan status monitor with firmware/software on/off and speed control

Watch Dog

· Environmental temperature monitoring via BIOS

Power-up mode control for recovery from AC po wer loss
 System resource alert (via included utility program)
 Auto-switching voltage regulator for the CPU core

CPU thermal trip support
I2C temperature sensing logic

ACPI Features

· Microsoft OnNow

· Slow blinking LED for suspend state indicator

· BIOS support for USB keyboard

Wake-On-LAN (WOL)

· Internal/external modem ring-on

Onboard I/O

• On-chip SATA controller supporting four (4) SATA ports (RAID 0, 1, 0+1, 5

and JBOD supported)

One (1) Fast UART 16550 compatible serial port

On-chip (MCP55 Pro) Ethernet controller supports two Gigabit LAN ports

2+2 Internal USB (Universal Serial Bus 2.0) ports/headers

• Two (2) rear USB ports

Onboard Windbond WPCM450 BMC graphics controller
 Mellanox Connect-X MT25408 20Gb/s Infiniband

Other

Onboard +3.3V standby power LED

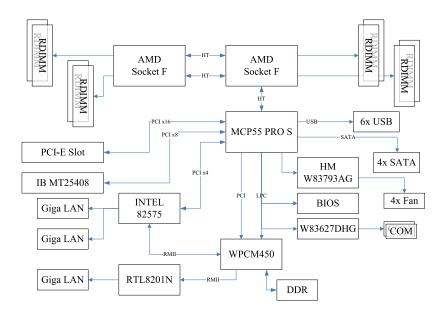
· Chassis intrusion detection

CD Utilities BIOS flash upgrade utility

Dimensions Proprietary form factor: 16.4" x 6.5" (417 x 165 mm)

1-5 Chipset Overview

Figure 1-4. nVidia MCP55 Pro Chipset System Block Diagram





NOTE: This is a general block diagram and may not exactly represent the features on your motherboard. See the previous pages for the actual specifications of your motherboard.

The H8DMT/H8DMT-IBX/H8DMT-F/H8DMT-IBXF Serverboard is based on the nVidia MCP55 Pro Chipset, which functions as a Media and Communications Processor (MCP). Controllers for the system memory are integrated directly into Opteron processors.

nVidia MCP55 Pro Chipset Media and Communications Processor

The nVidia MCP55 Pro Chipset is a single-chip, high-performance HyperTransport peripheral controller. It includes a 28-lane PCI Express interface, an AMD Opteron 16-bit Hyper Transport interface link, a four-port Serial ATA interface, a dual-port Gb Ethernet interface, a dual ATA133 bus master interface and a USB 2.0 interface. This hub connects directly to the CPU.

HyperTransport Technology

HyperTransport technology is a high-speed, low latency point to point link that was designed to increase the communication speed by a factor of up to 48x between integrated circuits. This is done partly by reducing the number of buses in the chipset to reduce bottlenecks and by enabling a more efficient use of memory in multi-processor systems. The end result is a significant increase in bandwidth within the chipset.

1-6 PC Health Monitoring

This section describes the PC health monitoring features of the H8DMT/H8DMT-IBX/H8DMT-F/H8DMT-IBXF serverboard. The serverboard has an onboard System Hardware Monitor chip that supports PC health monitoring.

Onboard Voltage Monitors

The onboard voltage monitor will continuously scan crucial voltage levels. Once a voltage becomes unstable, it will give a warning or send an error message to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor. Real time readings of these voltage levels are all displayed in BIOS.

Fan Status Monitor with Firmware/Software Speed Control

The PC health monitor can check the RPM status of the cooling fans. The onboard fans are controlled by thermal management via BIOS.

CPU Overheat/Fan Fail LED and Control

This feature is available when the user enables the CPU overheat/Fan Fail warning function in the BIOS. This allows the user to define an overheat temperature. When this temperature is exceeded or when a fan failure occurs, the Overheat/Fan Fail warning LED is triggered.

Auto-Switching Voltage Regulator for the CPU Core

The 3-phase-switching voltage regulator for the CPU core can support up to 80A and auto-sense voltage IDs ranging from 0.8 V to 1.55V. This will allow the regulator to run cooler and thus make the system more stable.

1-7 Power Configuration Settings

This section describes the features of your motherboard that deal with power and power settings.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-State Indicator

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

BIOS Support for USB Keyboard

If a USB keyboard is the only keyboard in the system, it will function like a normal keyboard during system boot-up.

Main Switch Override Mechanism

When an ATX power supply is used, the power button can function as a system suspend button. When the user depresses the power button, the system will enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. The power will turn off and no power will be provided to the motherboard.

Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, up-dates and access tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboard has a 3-pin header (WOL) to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Wake-On-LAN must be enabled in BIOS. Note that Wake-On-LAN can only be used with an ATX 2.01 (or above) compliant power supply.

1-8 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates.

The H8DMT accommodates 12V proprietary power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. A 2 amp current supply on a 5V Standby rail is strongly recommended.

It is strongly recommended that you use a high quality power supply that meets 12V ATX power supply Specification 1.1 or above. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.



WARNING: To prevent the possibility of explosion, do not use the wrong type of onboard CMOS battery or install it upside down.

1-9 Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives.

The Super I/O provides two high-speed, 16550 compatible serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250K, 500K, or 1 Mb/s, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP), Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP).

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through a SMI or SCI function pin. It also features auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can be flexibly adjusted to meet ISA PnP requirements, which support ACPI and APM (Advanced Power Management).

1-10 Contacting Supermicro

Headquarters

Address: Super Micro Computer, Inc.

980 Rock Ave.

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Email: marketing@supermicro.com (General Information)

support@supermicro.com (Technical Support)

Web Site: www.supermicro.com

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Tel: +886-(2) 8226-3990 Fax: +886-(2) 8226-3991

Web Site: www.supermicro.com.tw

Technical Support:

Email: support@supermicro.com.tw

Tel: +886-2-8228-1366, ext. 132 or 139

1-11 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

For faster service, RMA authorizations may be requested online at

http://www.supermicro.com/support/rma/

Whenever possible, repack the add-on card in the original Supermicro box, using the original packaging materials. If these are no longer available, be sure to pack the add-on card in an anti-static bag and inside the box. Make sure that there is enough packaging material surrounding the add-on card so that it does not become damaged during shipping.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alteration, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Chapter 2 Installation

2-1 Static-Sensitive Devices

Electrostatic Discharge (ESD) can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from ESD.

Precautions

- Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before removing the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the motherboard and peripherals back into their antistatic bags when not in use.
- For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.
- Use only the correct type of CMOS onboard battery as specified by the manufacturer. Do not install the CMOS onboard battery upside down, which may result in a possible explosion.

Unpacking

The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

Installation Procedure

Follow the procedures as listed below to install the motherboard into a chassis.

- 1. Install the processor(s) and the heatsink(s).
- 2. Install the motherboard in the chassis.
- Install the memory and add-on cards.
- 4. Finally, connect the cables and install the drivers.

2-2 Processor and Heatsink Installation

Follow the procedures in this section for installing the processor and heatsink into the H8DMT Serverboard.



WARNING: Exercise extreme caution when handling and installing the processor. Always connect the power cord last and always remove it before adding, removing or changing any hardware components.

Installing the Processors

 Begin by removing the cover plate that protects the CPU. Lift the lever on the CPU socket until it points straight up. With the lever raised, lift open the silver CPU retention plate.



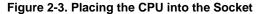
Figure 2-1. Removing the CPU Cover Plate

 Use your thumb and your index finger to hold the CPU. Locate and align pin 1 of the CPU socket with pin 1 of the CPU. Both are marked with a triangle. Align pin 1 of the CPU with pin 1 of the socket.



Figure 2-2. Aligning the CPU with Socket

Once aligned, carefully place the CPU into the socket. Do not drop the CPU on the socket, move the CPU horizontally or vertically or rub the CPU against the socket or against any pins of the socket, which may damage the CPU and/or the socket.





4. With the CPU inserted into the socket, inspect the four corners of the CPU to make sure that it is properly installed and flush with the socket. Then, gently lower the silver CPU retention plate into place.

Figure 2-4. Inspecting the CPU Installation



Carefully press the CPU socket lever down until it locks into its retention tab. For a
dual-CPU system, repeat these steps to install another CPU into the CPU#2 socket
(and into CPU#2, #3 and #4 sockets for a quad-CPU configuration).



NOTE: In single and dual-CPU configurations, memory must be installed in the DIMM slots associated with the installed CPU(s). Memory is limited to a maximum of 32 for single CPU and 64 GB for dual CPU configurations.



Figure 2-5. Secure the CPU with Socket Lever

Installing the Heatsinks

We recommend the use of active type heatsinks (except for 1U systems). Use any onboard fan header for the CPU's heatsink fan. To install the heatsink, please follow the installation instructions included with your heatsink package (not included).

2-3 Mounting the Mainboard into a Chassis

All Serverboards have standard mounting holes to fit different types of chassis. Make sure that the locations of all the mounting holes for both the Serverboard and the chassis match. Although a chassis may have both plastic and metal mounting fasteners, metal ones are highly recommended because they ground the Serverboard to the chassis. Make sure that the metal standoffs click in or are screwed in tightly.

Checking the Compatibility of the Mainboard Ports and the I/O Shield

- The H8DMT Serverboard requires a chassis that can support a board of 16.4" x 6.5" in size. It was designed to be used in a Supermicro 1U Twin system.
- 2. Make sure that the I/O ports on the Serverboard align with their respective holes in the I/O shield at the rear of the chassis.

Mounting the Mainboard onto the Tray in the Chassis

- Carefully mount the Serverboard onto the motherboard tray by aligning the motherboard mounting holes with the raised metal standoffs in the tray.
- Insert screws into all the mounting holes in the Serverboard that line up with the standoffs.
- Then use a screwdriver to secure the Serverboard to the mainboard tray tighten until just snug (if too tight you might strip the threads). Metal screws provide an electrical contact to the Serverboard ground to provide a continuous ground for the system.



WARNING: Exercise extreme caution when installing or removing memory modules to prevent any possible damage.

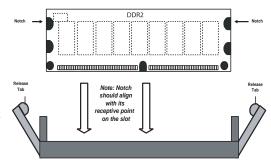
2-4 Installing Memory

Installing Memory

 Insert each memory module vertically into its slot, paying attention to the notch along the bottom of the module to prevent inserting the module incorrectly (see Figure 2-6).

Figure 2-6. Side and Top Views of DDR Installation

To Install: Insert module vertically and press down until it snaps into place. The release tabs should close – if they do not you should close them yourself. Pay attention to the bottom notch.



Note the notch in the slot and on the bottom of the DIMM. These prevent the DIMM from being installed incorrectly.

To Remove: Use your thumbs to gently push each release tab outward to free the DIMM from the slot.



- Install to slots CPU1/DIMM1B and CPU1/DIMM1A first, then to CPU1/DIMM2B and CPU1/DIMM2A, etc. Always install in pairs and in the numerical order of the DIMM slots. See "Support" information below.
- 3. Gently press down on the memory module until it snaps into place.
- 4. With two CPUs installed, repeat step 2 to populate the CPU2 DIMM slots.



NOTE: For the latest memory information on the H8DMT serverboard, please visit the http://www.supermicro.com web site.

Support

The H8DMT/H8DMT-IBX/H8DMT-F/H8DMT-IBXF Serverboards support single or dual-channel, DDR2-800/667/533 registered ECC SDRAM.

Only interleaved memory is supported, so you must populate two DIMM slots at a time.

Populating two adjacent slots at a time with memory modules of the same size and type will result in interleaved (128-bit) memory, which is faster than non-interleaved (64-bit) memory.

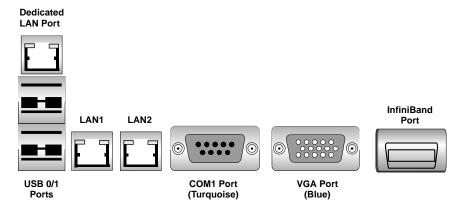
Maximum Memory

For the latest information on the maximum memory for the H8DMT serverboard, please visit the http://www.supermicro.com web site.

2-5 I/O Port and Control Panel Connections

The I/O ports are color coded in conformance with the PC99 specification to make setting up your system easier. See Figure 2-7 below for the colors and locations of the various I/O ports.

Figure 2-7. I/O Port Locations and Definitions





NOTE: The InfiniBand port is only available for the H8DMT-IBX/H8DMT-IBXF serverboards.



NOTE: The dedicated LAN port above the USB ports is only present for H8DMT-F/H8DMT-IBXFserverboards.

Front Control Panel

JF1 contains header pins for various front control panel connectors. See Figure 2-8 for the pin definitions of the various connectors. Refer to Section 2-6 for details.

Power Button Ground Reset Ground Power Fail LED OH Fan Fail LED Vcc NIC 2 Vcc NIC 1 Vcc HDD LED Vcc Power LED Vcc X (Key) X (Key) NM 1 Ground

Figure 2-8. JF1 Header Pin Connectors

2-6 Connector Definitions

Power Connector

The proprietary power supply connector (JWR1 and JWR2) meets the SSI (Superset ATX) 20-pin specification. Refer to the table below for the pin definitions of the ATX 20-pin power connector. This connection supplies power to the chipset, fans and memory.

| Pin# | Definition | Pin# | Definition |
|------|------------|------|------------|
| 1 | GND | 11 | PS_ON_N |
| 2 | GND | 12 | 5V_STBY |
| 3 | GND | 13 | GND |
| 4 | GND | 14 | GND |
| 5 | GND | 15 | GND |
| 6 | NC | 16 | NC |
| 7 | 12V | 17 | 12V |
| 8 | 12V | 18 | 12V |
| 9 | 12V | 19 | 12V |
| 10 | 12V | 20 | 12V |

Auxiliary Power Connector

A 4-pin 12V auxiliary power connector is included to provide power to hard drive disks. See the table below for pin definitions.

| Pin# | Definition |
|------|------------|
| 1 | +12V |
| 2 | Ground |
| 3 | Ground |
| 4 | +5V |

PW ON Connector

The PW_ON connector is on pins 1 and 2 of JF1. This header should be connected to the chassis power button. See the table below for pin definitions.

| Pin# | Definition |
|------|------------|
| 1 | PW_ON |
| 2 | Ground |

Reset Connector

The reset connector is located on pins 3 and 4 of JF1 and attaches to the reset switch on the computer chassis. See the table below for pin definitions.

| Pin# | Definition | |
|------|------------|--|
| 3 | Reset | |
| 4 | Ground | |

Overheat/Fan Fail LED (OH)

Connect an LED to the OH connection on pins 7 and 8 of JF1 to provide advanced warning of chassis overheating or fan failure. Refer to the tables below for pin definitions and for LED status indicators.

| Pin# | Definition | |
|------|------------|--|
| 7 | Vcc | |
| 8 | Control | |

| State | Indication | |
|----------|------------|--|
| Solid | Overheat | |
| Blinking | Fan Fail | |

NIC2 (LAN2) LED

The LED connections for LAN2 are on pins 9 and 10 of JF1. Attach LAN LED cables to display network activity. See the table below for pin definitions.

| Pin# | Definition | |
|------|------------|--|
| 9 | Vcc | |
| 10 | NIC2 | |

NIC1 (LAN1) LED

The LED connections for LAN1 are on pins 11 and 12 of JF1. Attach LAN LED cables to display network activity. See the table below for pin definitions.

| Pin# | Definition | |
|------|------------|--|
| 11 | Vcc | |
| 12 | NIC1 | |

HDD LED

The HDD LED connection is located on pins 13 and 14 of JF1. Attach the hard drive LED cable here to display disk activity (for any hard drives on the system, including SAS, Serial ATA and IDE). See the table below for pin definitions

| Pin# | Definition | |
|------|------------|--|
| 13 | Vcc | |
| 14 | HD Active | |

Power On LED

The Power On LED connector is located on pins 15 and 16 of JF1. This connection is used to provide LED indication of power being supplied to the system. See the table below for pin definitions.

| Pin# | Definition | |
|------|------------|--|
| 15 | 5V Stby | |
| 16 | Control | |

NMI Button

The non-maskable interrupt button header is located on pins 19 and 20 of JF1. Refer to the table below for pin definitions.

| Pin# | Definition | |
|------|------------|--|
| 19 | Control | |
| 20 | Ground | |

Universal Serial Bus Ports

Two Universal Serial Bus ports (USB 2.0) are located beside the LAN1/2 ports. Two additional ports (USB4/5) are included on the motherboard near the SIMSO slot. See the table below for pin definitions.

| USB0 | | USB1 | |
|------|------------|------|------------|
| Pin# | Definition | Pin# | Definition |
| 1 | +5V | 1 | +5V |
| 2 | PO- | 2 | PO- |
| 3 | PO+ | 3 | PO+ |
| 4 | Ground | 4 | Ground |

USB Headers

Two USB 2.0 headers (USB2/3) are also included on the motherboard. These may be connected to provide front side access. A USB cable (not included) is needed for the connection. See the table below for pin definitions.

| USB2 | | USB3/4 | |
|------|------------|--------|---------------|
| Pin# | Definition | Pin# | Definition |
| 1 | +5V | 1 | +5V |
| 2 | PO- | 2 | PO- |
| 3 | PO+ | 3 | PO+ |
| 4 | Ground | 4 | Ground |
| 5 | Key | 5 | No connection |

Serial Ports

The COM1 serial port is located beside the VGA port. Refer to the motherboard layout for the location of the COM2 header. See the table below for pin definitions.

| Pin# | Definition | Pin# | Definition |
|------|------------|------|-----------------|
| 1 | DCD | 6 | DSR |
| 2 | RXD | 7 | RTS |
| 3 | TXD | 8 | CTS |
| 4 | DTR | 9 | RI |
| 5 | Ground | 10 | NC ¹ |

1. Note: NC indicates no connection.

Fan Headers

The H8DMT has four 4-pin proprietary fan headers. Each fan header supports one 4-pin fans with PWM mode. See the table below for pin definitions.



NOTE: The onboard fan speed is controlled by the CPU die temperature.

| Pin# | Definition | Pin# | Definition |
|------|------------------------|------|------------------------------|
| 1 | Ground | 3 | Tachometer for Fan |
| 2 | PWR (DC Speed CTRL) | 4 | PWM (Pulse Width Modulation) |

LAN1/2 (Ethernet Ports)

Two Gigabit Ethernet ports (designated LAN1 and LAN2) are located beside the COM 1port. These Ethernet ports accept RJ45 type cables.

Dedicated LAN (Ethernet Port)

One Gigabit Ethernet (RJ45) port is located above the USB ports on the H8DMT-F/H8DMT-IBXF serverboards as a Dedicated LAN port for IPMI use. This port is not present on the H8DMT/H8DMT-IBX serverboards.

Overheat LED

Connect an LED to the JOH1 header to provide warning of chassis overheating. See the table below for pin definitions.

| Pin# | Definition |
|------|------------|
| 1 | 3.3V |
| 2 | OH Active |

Chassis Intrusion

A Chassis Intrusion header is located at JL1. Attach the appropriate cable to inform you of a chassis intrusion. See the table below for pin definitions.

| Pin# | Definition | |
|------|------------------|--|
| 1 | Intrusion signal | |
| 2 | Battery voltage | |

Wake-On-LAN

The Wake-On-LAN header is designated JWOL. You must have a LAN card with a Wake-On-LAN connector and cable to use the Wake-On-LAN feature. See the table below for pin definitions.

| Pin# | Definition |
|------|-------------|
| 1 | +5V Standby |
| 2 | Ground |
| 3 | Wake-up |

SMBus Header

The header at SMBus is for the System Management Bus for the H8DMT-F/H8DMT-IBXF Serverboards. Connect the appropriate cable here to utilize SMB on the system. See the table below for pin definitions.

| Pin# | Definition |
|------|---------------|
| 1 | Data |
| 2 | Ground |
| 3 | Clock |
| 4 | No Connection |

SGPIO

The T-SGPIO1 (Serial General Purpose Input/Output) header provides a bus between the SATA controller and the SATA drive backplane to provide SATA enclosure management functions. Connect the appropriate cables from the backplane to the T-SGPIO1 header to utilize SATA management functions on your system. See the table below for pin definitions.

| Pin# | Definition | Pin# | Definition |
|------|------------|------|-----------------|
| 1 | NC | 2 | NC |
| 3 | DataIn | 4 | DataOut |
| 5 | Load | 6 | Ground |
| 7 | Clock | 8 | NC ¹ |

1. Note: NC indicates no connection.

Power I2C

The JPI2C header is for power I2C, which may be used to monitor the status of the power supply, fan and system temperature. See the table below for pin definitions.

| Pin# | Definition |
|------|------------|
| 1 | Clock |
| 2 | Data |
| 3 | Power Fail |
| 4 | Ground |

2-7 Jumper Settings

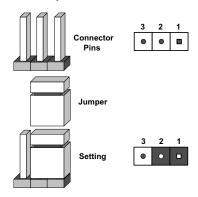
Explanation of Jumpers

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the diagram at right for an example of jumping pins 1 and 2. Refer to the motherboard layout page for jumper locations.



NOTE: On two-pin jumpers, "Closed" means the jumper is on and "Open" means the jumper is off the pins.

Figure 2-9. Jumper Connector Pins and Setting



CMOS Clear

JBT1 is used to clear CMOS, which will also clear any passwords. Instead of pins, this jumper consists of contact pads to prevent accidentally clearing the contents of CMOS.

To Clear CMOS

- 1. First power down the system and unplug the power cord(s).
- With the power disconnected, short the CMOS pads with a metal object such as a small screwdriver.
- 3. Remove the screwdriver (or shorting device).
- 4. Reconnect the power cord(s) and power on the system.



NOTE: Do not use the PW_ON connector to clear CMOS.

LAN Controller Enable/Disable

The JPL jumper allows you to enable or diable the serverboard's LAN controller. The default position is on for both pins 1 and pin 2 to enable the LAN Controller. See the table below for jumper settings.

| Jumper Setting | Definition |
|----------------|----------------------------------|
| Pins 1-2 | LAN Controller Enabled (Default) |
| Pins 2-3 | LAN Controller Disabled |

BMC/Video Enable/Disable

JBMC1 connector allows you to enable or disable the IPMI and Video. The default position is on for both pin 1 and pin 2 to enable both IPMI and VGA. See the table below for jumper settings.

| Jumper Setting | Definition |
|----------------|------------------------|
| Pins 1-2 | BMC and Video Enabled |
| Pins 2-3 | BMC and Video Disabled |

I2C to PCI-Express Slot

JI2C1/JI2C2 allows you to enable the I2C bus to communicate with the PCI-Express slot. For the jumpers to work properly, please set both jumpers to the same setting. If enabled, both jumpers must be enabled. If disabled, both jumpers must be disabled. See the table below for jumper settings.

| Jumper Setting | Definition |
|----------------|------------|
| Closed | Enabled |
| Open | Disabled |

Watch Dog Enable/Disable

JWD enables the Watch Dog function, a system monitor that takes action when a software application freezes the system. Jumping pins 1-2 will have WD reboot the system if a program freezes. Jumping pins 2-3 will generate a non-maskable interrupt for the program that has frozen. **Watch Dog must also be enabled in BIOS.** See the table below for jumper settings.



NOTE: When Watch Dog is enabled, the user must write their own application software to disable the Watch Dog Timer.

| Jumper Setting | Definition |
|----------------|------------|
| Pins 1-2 | Reset |
| Pins 2-3 | NMI |
| Open | Disabled |

InfiniBand Port Enable/Disable

JIB1 enables or disables the InfiniBand port on the H8DMT/H8DMT-IBX Serverboards. The default position is on pins 1 and 2 to enable the port. See the table below for jumper settings.

| Jumper Setting | Definition |
|----------------|------------|
| Pins 1-2 | Enabled |
| Pins 2-3 | Disabled |

2-8 Onboard Indicators

LAN1/LAN2 LEDs

The Ethernet ports (located beside the VGA port) have two LEDs. On each Gb LAN port, one LED blinks to indicate activity while the other may be green, amber or off to indicate the speed of the connection. See the table below for the functions associated with the connection speed LED.

| LED Color | Definition |
|-----------|------------|
| Off | 10 MHz |
| Green | 100 MHz |
| Amber | 1 GHz |

Power LED

DP4 is an Onboard Power LED. When this LED is lit, it means power is present on the serverboard. Be sure to turn off the system and unplug the power cord(s) before removing or installing components. See the table below for Power LED state status information.

| State | State Status |
|-------|--------------------------------------|
| | Standby power present on motherboard |
| Off | No power connected |

InfiniBand LED Indicators

Two InfiniBand LED indicators (LE2/LE3) are located near the InfiniBand port of the H8DMT/H8DMT-IBX Serverboards. The green LED (LE2) is the InfiniBand link LED while the yellow LED (LE3) indicates activity. Refer to the tables below for details.

| Color | Status | Definition |
|-------|--------|----------------------|
| Green | Solid | InfiniBand Connected |
| Off | Off | No Connection |

| Color | Status | Definition |
|--------|--------|-------------------------------------|
| Yellow | Solid | InfiniBand Active |
| Yellow | Dim | InfiniBand Connected, Activity Idle |
| Off | Off | No Connection |

2-9 Drive Connections

There are no IDE or floppy drive connectors on the motherboard. Use the following information to connect the SATA drive cables.

SATA Ports

There are no jumpers to configure the SATA ports, which are designated SATA0 through SATA3. See the table below for pin definitions.

| Pin# | Description |
|------|-------------|
| 1 | Ground |
| 2 | TXP |
| 3 | TXN |
| 4 | Ground |
| 5 | RXN |
| 6 | RXP |
| 7 | Ground |

2-10 Enabling SATA RAID

Now that the hardware is set up, you must install the operating system and the SATA RAID drivers, if you wish to use RAID with your SATA drives. The installation procedure differs depending on whether you wish to have the operating system installed on a RAID Serial ATA (SATA)

Serial ATA (SATA) is a physical storage interface that employs a single cable with a minimum of four wires to create a point-to-point connection between devices. This connection is a serial link that supports a SATA transfer rate from 150 MBps. The serial cables used in SATA are thinner than the traditional cables used in Parallel ATA (PATA) and can extend up to one meter in length, compared to only 40 cm for PATA cables. Overall, SATA provides better functionality than PATA.

Installing the OS/SATA Driver

Before installing the OS (operating system) and SATA RAID driver, you must decide if you wish to have the operating system installed as part of a bootable RAID array or installed to a separate non-RAID hard drive. If on a separate drive, you may install the driver either during or after the OS installation. If you wish to have the OS on a SATA RAID array, you must follow the procedure below and install the driver during the OS installation.

Building a Driver Diskette

You must first build a driver diskette from the Supermicro CD-ROM that was included with the system. (You will have to create this disk on a computer that is already running and with the OS installed.)

- Insert the CD into your CD-ROM drive and start the system. A display as shown in Figure 2-10 will appear.
- Click on the icon labeled BUILD DRIVER DISKETTES AND MANUALS and follow the instructions to create a floppy disk with the driver on it.
- Once it's been created, remove the floppy and insert the installation CD for the Windows Operating System you wish to install into the CD-ROM drive of the new system you are about to configure.

Enabling SATA RAID in the BIOS

Before installing the Windows Operating System, you must change some settings in the BIOS. Boot up the system and hit the key to enter the BIOS Setup Utility. After the Setup Utility loads, do the following:

- Use the arrow keys to move to the EXIT menu. Scroll down with the arrow keys to the LOAD OPTIMAL DEFAULTS setting and press <ENTER>. Select OK to confirm, then <ENTER> to load the default settings.
- Use the arrow keys to move to the ADVANCED menu, then scroll down to NVIDIA RAID SETUP and press the <ENTER> key.
- Once in the submenu, scroll down to NVIDIA RAID FUNCTION and enable the setting, which will cause the SATA0/1/2 PRIMARY/SECONDARY settings to appear. Enable the SATA devices and channels you will be using.
- Hit the <ESC> key twice and scroll to the EXIT menu. Select SAVE CHANGES AND EXIT, then hit <ENTER>, then hit <ENTER> again to verify.
- After exiting the BIOS Setup Utility, the system will reboot. When prompted during the startup, press the <F10> key when prompted to run the nVidia RAID Utility program.

Using the nVidia RAID Utility

The nVidia RAID Utility program is where you can define the drives you want to include in the RAID array and the mode and type of RAID. Two main windows are shown in the utility.

- The FREE DISKS window on the left will list all available drives. Use the arrow keys to select and move drives to the window on the right, which lists all drives that are to become part of the RAID array.
- Once you have finished selecting the drives and type of RAID you wish to use for your RAID array, press the <F7> key. You will be prompted to verify your choice; if you want to continue with your choices, select YES.



WARNING: Selecting **Yes** clears all previous data from the drives you selected to be a part of the array.

 You are then given the choice of making the RAID array bootable by pressing the the key. After you have finished, press the <CTRL> and <X> keys simultaneously.

Installing the OS and Drivers

To install the OS and drivers, do the following:

- 1. With the Windows OS installation CD in the CD-ROM drive, restart the system.
- When you see the prompt, hit the <F6> key to enter Windows setup. Eventually a
 blue screen will appear with a message that begins WINDOWS COULD NOT DETERMINE
 THE TYPE OF ONE OR MORE STORAGE DEVICES. . .
- 3. When you see the screen, hit the <S> key to SPECIFY ADDITIONAL DEVICE, then insert the driver diskette you just created into the floppy drive.
- Highlight Manufacturer Supplied Hardware Support Disk and hit the <Enter> key.
- 5. Highlight the first NVIDIA RAID driver shown and press the <ENTER> key to install it.
- Soon a similar blue screen will appear again. Again hit the <S> key, then highlight the second item, NFORCE STORAGE CONTROLLER and press the <ENTER> key, then <ENTER> again to continue with the Windows setup.

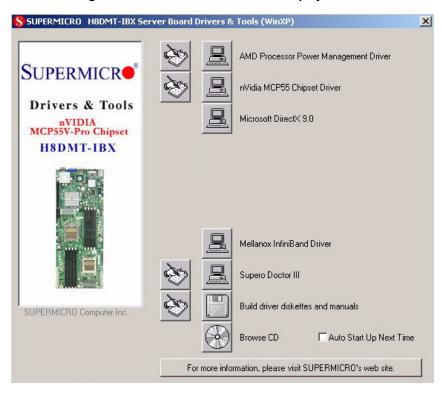
2-11 Installing Drivers

The CD that came bundled with the Serverboard contains drivers, some of which must be installed, such as the chipset driver.

 After inserting this CD into your CD-ROM drive, the display shown in Figure 2-10 should appear. If this display does not appear, click on the MY COMPUTER icon and

- then on the icon representing your CD-ROM drive. Finally, double click on the S SETUP icon.
- 2. Click the icons showing a hand writing on paper to view the readme files for each item.
- 3. Click the computer icons to the right of these items to install each item (from top to the bottom) one at a time.
- After installing each item, you should reboot the system before moving on to the next item on the list. The bottom icon with a CD on it allows you to view the entire contents of the CD.

Figure 2-10. Driver/Tool Installation Display Screen



Chapter 3 Troubleshooting

3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your Serverboard. If you have followed all of the procedures below and still need assistance, refer to Section 3-2: "Technical Support Procedures" on page 3-2 and/or Section 3-4: "Returning Merchandise for Service" on page 3-4 in this chapter. Always disconnect the AC power cord before adding, changing or installing any hardware components.

Before Power On

- 1. Check that the onboard power LED is lit (DP4 on the motherboard).
- 2. Make sure that the ATX power connector is connected to your power supply.
- 3. Make sure that no short circuits exist between the Serverboard and chassis.
- Disconnect all cables from the Serverboard, including those for the keyboard and mouse.
- Remove all add-on cards.
- Install a CPU and heatsink (making sure it is fully seated) and connect the internal (chassis) speaker and the power LED to the Serverboard. Check all jumper settings as well
- Use the correct type of onboard CMOS battery as recommended by the manufacturer. To avoid possible explosion, do not install the CMOS battery upside down.

No Power

- 1. Make sure that no short circuits exist between the Serverboard and the chassis.
- 2. Verify that all jumpers are set to their default positions.
- 3. Check that the 115V/230V switch on the power supply is properly set.
- 4. Turn the power switch on and off to test the system.
- The battery on your Serverboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.

No Video

- 1. If the power is on but you have no video, remove all the add-on cards and cables.
- Use the speaker to determine if any beep codes exist. Refer to Appendix A for details on beep codes.



NOTE: If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For I/O port 80h codes, refer to Appendix B.

Memory Errors

- 1. Make sure that the DIMM modules are properly and fully installed.
- You should be using registered ECC DDR-2 memory (see next page). Also, it is
 recommended that you use the same memory type and speed for all DIMMs in the
 system. See Section 2-4: "Installing Memory" on page 2-5 for memory details.
- Check for bad DIMM modules or slots by swapping modules between slots and noting the results.
- 4. Check the power supply voltage 115V/230V switch.

Losing the System's Setup Configuration

- Make sure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup information. Refer to Section 1-8 for details on recommended power supplies.
- 2. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.
- If the above steps do not fix the setup configuration problem, contact your vendor for repairs.

3-2 Technical Support Procedures

Before contacting Technical Support, please take the following steps. Also, note that as a motherboard manufacturer, we do not sell directly to end-users, so it is best to first check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.

- Please review the Section 3-1: "Troubleshooting Procedures" on page 3-1 and Section 3-3: "Frequently Asked Questions" on page 3-3 in this chapter or see the FAQs on our web site before contacting Technical Support.
- 2. BIOS upgrades can be downloaded from our web site.



NOTE: Not all BIOS can be flashed depending on the modifications to the boot block code.

- 3. If you still cannot resolve the problem, include the following information when contacting us for technical support:
 - Serverboard model and PCB revision number

- BIOS release date/version (this can be seen on the initial display when your system first boots up)
- System configuration

An example of a Technical Support form is posted on our web site.

Distributors: For immediate assistance, please have your account number ready when contacting our technical support department by e-mail.

3-3 Frequently Asked Questions

Question: What type of memory does my motherboard support?

Answer: The H8DMT supports up to 32 GB of DDR2-800/667/533 registered ECC SDRAM (or 16 GB with a single CPU installed). Memory must be installed in an interleaved configuration only. See Section 2-4 for details on installing memory. Refer to the http://www.supermicro.com web site for more details.

Question: How do I update my BIOS?

Answer: It is recommended that you not upgrade your BIOS if you are not experiencing problems with your system. Updated BIOS files are located on our web site. Please check our BIOS warning message and the information on how to update your BIOS on our web site. Also, check the current BIOS revision and make sure it is newer than your current BIOS before downloading.

Select your motherboard model on the web page and download the corresponding BIOS file to your computer. Unzip the BIOS update file, in which you will find the readme.txt (flash instructions), the afudos.exe (BIOS flash utility) and the BIOS image (xxx.rom) files. Copy these files to a bootable floppy disk, insert the disk into drive A and reboot the system. At the DOS prompt after rebooting, enter the command "flash" (without quotation marks) then type in the BIOS file that you want to update with (xxxx.rom).

Question: What's on the CD that came with my motherboard?

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications on the CD include chipset drivers for Windows and security and audio drivers.

Question: Why can't I turn off the power using the momentary power on/off switch?

Answer: The instant power off function is controlled in BIOS by the Power Button Mode setting. When the On/Off feature is enabled, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When the Standby or Suspend feature is enabled or when the BIOS is not in control such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down the system. This feature is required to implement the ACPI features on the Serverboard.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

For faster service, RMA authorizations may be requested online (http://www.supermicro.com/support/rma/).

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alteration, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Chapter 4 BIOS

4-1 Introduction

This chapter describes the AMIBIOS™ Setup utility for the H8DMT/H8DMT-IBX/ H8DMT-F/H8DMT-IBXF Serverboards. The AMI ROM BIOS is stored in a flash chip and can be easily upgraded using a floppy disk-based program.



NOTE: Due to periodic changes to the BIOS, some settings may have been added or deleted and might not yet be recorded in this manual. Please refer to the Manual Download area of our web site for any changes to BIOS that may not be reflected in this manual.

4-2 Starting the Setup Utility

To enter the BIOS Setup Utility, hit the <Delete> key while the system is booting-up. (In most cases, the <DELETE> key is used to invoke the BIOS setup screen. There are a few cases when other keys are used, such as <F1>, <F2>, etc.) Each main BIOS menu option is described in this manual.

The Main BIOS screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it. (Note that BIOS has default text messages built in. We retain the option to include, omit, or change any of these text messages.) Settings printed in **Bold** are the default values.

A ▶ indicates a submenu. Highlighting such an item and pressing the <ENTER> key will open the list of settings within that submenu.

The BIOS setup utility uses a key-based navigation system called hot keys. Most of these hot keys (<F1>, <F10>, <ENTER>, <ESC>, <ARROW> keys, etc.) can be used at any time during the setup navigation process.

4-3 Main Menu

When you first enter AMI BIOS Setup Utility, you will see the MAIN MENU screen. You can always return to the Main Menu by selecting the *Main* tab on the top of the screen with the arrow keys.

The MAIN MENU screen provides you with a system overview, which includes the version, built date and ID of the AMIBIOS, the type, speed and number of the processors in the system and the amount of memory installed in the system.

System Time/System Date

You can edit this field to change the system time and date. Highlight *System Time* or *System Date* using the <ARROW> keys. Enter new values through the keyboard. Press the <TAB> key or the <ARROW> keys to move between fields. The date must be entered in **DAY/MM/DD/YYYY** format. The time is entered in **HH:MM:SS** format. Please note that time is in a 24-hour format. For example, 5:30 A.M. appears as 05:30:00 and 5:30 P.M. as 17:30:00.

4-4 Advanced Settings Menu

The submenus in the ADVANCED SETTINGS menu are listed in Table 4-1 through Table 4-12 below.

Table 4-1. BIOS Features Submenu

| Menu Item | Description | |
|------------------------------------|---|--|
| Quick Boot | If Enabled, this option will skip certain tests during POST to reduce the time needed for the system to boot up. The options are Enabled and DISABLED. | |
| Quiet Boot | If Disabled, normal POST messages will be displayed on boot-up. If Enabled , this display the OEM logo instead of POST messages. | |
| OS Installation | Change this setting if using a 64-bit Linux operating system. The available options are Other and LINUX. | |
| Interrupt 19 Capture | Select Enabled to allow ROMs to trap Interrupt 19. The options are ENABLED and Disabled. | |
| Wait for F1 if Error | This setting controls the system response when an error is detected during the boot sequence. When enabled, BIOS will stop the boot sequence when an error is detected, at which point you will need to press the F1 button to re-enter the BIOS setup menu. The options are Enabled and DISABLED. | |
| ACPI Mode | Use this setting to determine whether ACPI mode will be used. The options are Yes and No. | |
| ►Advanced ACPI Con | figuration Submenu | |
| MCP55 ACPI HPET Table | Determines whether to enable or disable the MCP55 ACPI HPET table. Options are Enabled or DISABLED. | |
| ACPI Version Features | Use this setting the determine which ACPI version to use. Options are ACPI v1.0, ACPI v2.0 and ACPI v3.0. | |
| ACPI APIC Support | Determines whether to include the ACPI APIC table pointer in the RSDT pointer list. The available options are Enabled and DISABLED. | |
| AMI OEMB Table | Determines whether to include the AMI OEMB table pointer in the RSDT pointer list. The available options are Enabled and DISABLED. | |
| Headless Mode | Use this setting to ENABLE or Disable headless operation mode through ACPI. This setting is used to update the ACPI FACP table to indicate headless operations without a monitor. | |
| General WHEA Configuration Submenu | | |

Table 4-1. BIOS Features Submenu (Continued)

| Menu Item | Description |
|-----------------------------|---|
| WHEA Support | Use this setting to Enable or DISABLE WHEA (Windows Hardware Error Architecture) support. WHEA provides a common infrastructure for reporting hardware errors on Windows platforms and was designed to improve recovery following fatal hardware errors. |
| Power Button Mode | Allows the user to change the function of the power button. Options are On/Off and SUSPEND. |
| Watch Dog Timer Select | This setting is used to ENABLE or Disable the Watch Dog Timer function. It must be used in conjunction with the Watch Dog jumper (see Chapter 2 for details). To enable, choose from 1, 2, 3, 4, 8, 15 or 30 \pm MIN. |
| Restore on AC Power Loss | This setting allows you to choose how the system will react when power returns after an unexpected loss of power. The options are POWER OFF, POWER ON and Last State. |
| MPS Revision | This setting allows the user to select the MPS (MultiProcessor Specification) revision level. The options are 1.1 and 1.4. |

Table 4-2. SATA Configuration Submenu

| Menu Item | Description |
|--|---|
| Serial ATA Devices | This setting is used to determine if SATA drives will be used and how many. Options are DISABLED, DEVICE 0 and Device 0/1 . |
| nVidia RAID Function | This setting is used to ENABLE or Disable the nVidia ROM. If enabled, the setting below will appear. |
| ►SerialATA 0/1 Primary/Secondary Channel | This setting is used to ENABLE or Disable the SATA0 Primary, SATA0 Secondary, SATA1 Primary and SATA1 Secondary, channels (four settings total). If enabled, the following settings will appear: |
| LBA/Large Mode | LBA (Logical Block Addressing) is a method of addressing data on a disk drive. The options are DISABLED and Auto . |
| Block (Multi-Sector Transfer) | Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt. Select DISABLED to allow the data to be transferred from and to the device one sector at a time. Select Auto to allows the data transfer from and to the device occur multiple sectors at a time if the device supports it. The options are Auto and DISABLED. |

Table 4-2. SATA Configuration Submenu (Continued)

| Menu Item | Description |
|-------------------------|---|
| PIO Mode | PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The options are Auto , 0, 1, 2, 3, and 4. Select Auto to allow BIOS to auto detect the PIO mode. Use this value if the IDE disk drive support cannot be determined. • Select 0 to allow BIOS to use PIO mode 0, which has a data transfer rate of 3.3 MBs. • Select 1 to allow BIOS to use PIO mode 1, which has a data transfer rate of 5.2 MBs. • Select 2 to allow BIOS to use PIO mode 2, which has a data transfer rate of 8.3 MBs. • Select 3 to allow BIOS to use PIO mode 3, which has a data transfer rate of 11.1 MBs. • Select 4 to allow BIOS to use PIO mode 4, which has a data transfer rate of 16.6 MBs. This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive. |
| DMA Mode | Selects the DMA Mode. Options are Auto , SWDMA0, SWDMA1, SWDMA2, MWDMA0. MDWDMA1, MWDMA2, UDMA0. UDMA1, UDMA2, UDMA3, UDMA4 and UDMA5. (SWDMA=Single Word DMA, MWDMA=Multi Word DMA, UDMA=UltraDMA. |
| S.M.A.R.T. | Self-Monitoring Analysis and Reporting Technology (SMART) can help predict impending drive failures. Select Auto to allow BIOS to auto detect hard disk drive support. Select "Disabled" to prevent AMI BIOS from using the S.M.A.R.T. Select ENABLED to allow AMI BIOS to use the S.M.A.R.T. to support hard drive disk. The options are DISABLED, ENABLED, and Auto . |
| 32-Bit Data Transfer | Select Enabled to activate the 32-Bit Data Transfer function. Select DISABLED to deactivate the function. The options are Enabled and DISABLED. |

Table 4-3. PCI/PnP Configuration Submenu

| Menu Item | Description |
|--------------------------------|---|
| Slot 1 OPROM | Use this setting to enable or disable the OPROM (Option ROM firmware) for slot 1. The options are Yes and No. |
| Load Onboard LAN Option ROM | Use this setting to ENABLE or Disable the onboard option ROM. This setting must be enabled to view the BOOT MENU settings. |
| Clear NVRAM | Select YEs to clear NVRAM (Non-Volatile Random Access Memory) during boot-up. The options are YEs and No . |
| Plug & Play OS | Select YEs to allow the OS to configure Plug & Play devices. (This is not required for system boot if your system has an OS that supports Plug & Play.) Select No to allow AMIBIOS to configure all devices in the system. |
| PCI Latency Timer | This option sets the latency of all PCI devices on the PCI bus. Select a value to set the PCI latency in PCI clock cycles. Options are 32, 64 , 96, 128, 160, 192, 224 and 248. |

Table 4-4. Advanced Chipset Control Submenu

| Menu Item | Description |
|-------------------------------------|---|
| ► NorthBridge Configuration submenu | See Table 4-5 for further details and submenus. |
| ►SouthBridge Configuration submenu | See Table 4-6 for further details and submenus. |

Table 4-5. NorthBridge Configuration Submenu

| Menu Item | Description |
|-------------------------------|---|
| ►Memory Configuration | on |
| Bank Interleaving | Select Auto to automatically enable a bank-interleaving memory scheme when this function is supported by the processor. The options are Auto and DISABLED. |
| Channel Interleaving | Selects the channel-interleaving memory scheme when this function is supported by the processor. The options are DISABLED, ADDRESS BITS 6, ADDRESS BITS 12, XOR of Address Bits [20:16, 6] and XOR OF ADDRESS BITS [20:16, 9]. |
| Enable Clock to All Dimms | Use this setting to enable unused clocks to all DIMMSs, even if some DIMM slots are unpopulated. Options are ENABLED and Disabled . |
| Mem Clk Tristate C3/ALTVID | Use this setting to ENABLE or Disable memory clock tristate during C3 and ALT VID. |
| Memory Hole Remapping | When Enabled , this feature enables hardware memory remapping around the memory hole. Options are Enabled and DISABLED. |
| CS Sparing | This setting will reserve a spare memory rank in each node when enabled. Options are ENABLE and Disable . |
| DCT Unganged Mode | This setting enables unganged DRAM mode (64-bit). Options are AUTO (ganged mode) and Always (unganged mode). |
| Power Down Enable | This setting enables or disables the DDR power down mode. Options are Enabled and DISABLED. |
| Power Down Mode | This sets the power down mode. Options are Channel and CHIP SELECT. |
| ▶ECC Configuration | |
| ECC Mode | This setting affects the DRAM scrub rate based on its setting. Options are DISABLED, Basic , GOOD, SUPER, MAX and USER. Depending upon the setting chosen, some or all of the following settings will become active: |
| DRAM ECC Enable | DRAM ECC allows hardware to report and correct memory errors automatically. Options are Enabled and DISABLED. |
| DRAM SCRUB REDIRECT | Allows system to correct DRAM ECC errors immediately, even with background scrubbing on. Options are Enabled and DISABLED. |
| 4-Bit ECC Mode | Allows the user to enabled 4-bit ECC mode (also known as ECC Chipkill). Options are ENABLED and Disabled . |
| DRAM BG Scrub | Corrects memory errors so later reads are correct. Options are Disabled and various times in nanoseconds and microseconds. |
| Data Cache BG Scrub | Allows L1 cache RAM to be corrected when idle. Options are Disabled and various times in nanoseconds and microseconds. |

Table 4-5. NorthBridge Configuration Submenu (Continued)

| Menu Item | Description | | |
|----------------------|--|--|--|
| L2 Cache BG Scrub | Allows L2 cache RAM to be corrected when idle. Options are Disabled and various times in nanoseconds and microseconds. | | |
| L3 Cache BG Scrub | Allows L3 cache RAM to be corrected when idle. Options are Disabled and various times in nanoseconds and microseconds. | | |
| ► DRAM Timing Confi | ▶ DRAM Timing Configuration | | |
| Memory Clock Mode | This setting specifies the memory clock mode. Options are Auto , LIMIT and MANUAL. | | |
| DRAM Timing Mode | This setting specifies the DRAM timing mode. Options are Auto and DCT. | | |
| ▶ IOMMU Option Menu | | | |
| IOMMU Mode | Used to disable or set the GART size in systems without AGP. Options are AGP Present , DISABLED, 32 MB, 64 MB, 128 MB, 256 MB, 512 MB and 1 GB. | | |

Table 4-6. SouthBridge/MCP55 Configuration Submenu

| Menu Item | Description |
|----------------------------|--|
| CPU/LDT Spread Spectrum | Enables spread spectrum for the CPU/LDT. Options are Center Spread , DOWN SPREAD or DISABLED. |
| PCIE Spread Spectrum | Allows you to Enable or DISABLE spread spectrum for PCI-Express. |
| SATA Spread Spectrum | Enables spread spectrum for the SATA. Options are Enabled and DISABLED. |
| USB 1.1 Controller | Allows you to Enable or DISABLE the USB 1.1 controller. |
| USB 2.0 Controller | Setting to either Enable or DISABLE the USB 2.0 controller. |
| Legacy USB Support | Select Enabled to enable support for USB Legacy devices.Use DISABLE to disable Legacy support if there are no USB devices installed in the system. AUTO disables Legacy support if no USB devices are connected. The options are DISABLED, Enabled and AUTO. |

Table 4-7. Processor & Clock Options Submenu

| Menu Item | Description | | |
|--------------------------------|---|--|--|
| MTRR Mapping | This determines the method used for programming CPU MTRRs when 4 GB or more memory is present. The options are Continuous , which makes the PCI hole non-cacheable, and DISCRETE, which places the PCI hole below the 4 GB boundary. | | |
| Thermal Throttling | Used to ENABLE or Disable thermal to generate a power management event. | | |
| Power Now | This setting is used to ENABLE or Disable the AMD Power Now feature. | | |
| Secure Virtual Machine Mode | This setting is used to Enable or DISABLE SVM (Secure Virtual Machine). | | |
| CPU Page Translation Table | This setting is used to Enable or DISABLE the CPU Page Translation Table. | | |

Table 4-8. I/O Device Configuration Submenu

| Menu Item | Description | | |
|----------------------|--|--|--|
| Serial Port1 Address | This option specifies the base I/O port address and Interrupt Request address of serial port 1. The options are DISABLED, 3F8/IRQ4 , 3E8/IRQ4 and 2E8/IRQ3. | | |
| | Select DISABLED to prevent the serial port from accessing any system resources. When this option is set to DISABLED, the serial port physically becomes unavailable. | | |
| | Select 3F8/IRQ4 to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. | | |
| Serial Port2 Address | This option specifies the base I/O port address and Interrupt Request address of serial port 2. The options are DISABLED, 2F8/IRQ3 , 3E8/IRQ4 and 2E8/IRQ3. | | |
| | Select DISABLED to prevent the serial port from accessing any system resources. When this option is set to DISABLED, the serial port physically becomes unavailable. | | |
| | Select 2F8/IRQ3 to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. | | |

Table 4-9. DMI Event Logging Submenu

| Menu Item | Description | |
|----------------------------|---|--|
| View Event Log | Highlight this item and press <enter> to view the contents of the event log.</enter> | |
| Mark All Events as Read | Highlight this item and press <enter> to mark all events as read.</enter> | |
| Clear Event Log | Select Yes and press <enter> to clear all event logs. The options are YEs and No to verify.</enter> | |

Table 4-10. Console Redirection Submenu

| Menu Item | Description | |
|--------------------------------|---|--|
| Remote Access | Allows you to ENABLE or Disable remote access. If enabled, the settings below will appear: | |
| Serial Port Number | Selects the serial port to use for console redirection. Options are COM1 and COM2. | |
| Serial Port Mode | Selects the serial port settings to use. Options are (115200 8, n, 1) , (57600 8, N, 1), (38400 8, N, 1), (19200 8, N, 1) and (09600 8, N, 1). | |
| Flow Control | Selects the flow control to be used for console redirection. Options are None , HARDWARE and SOFTWARE. | |
| Redirection After BIOS POST | Options are DISABLE (no redirection after BIOS POST), BOOT LOADER (redirection during POST and during boot loader) and Always (redirection always active). Note that some OS's may not work with this set to ALWAYS. | |
| Terminal Type | Selects the type of the target terminal. Options are ANSI , VT100 and VT-UTF8. | |
| VT-UTF8 Combo Key Support | Allows you to Enable or DISABLE VT-UTF8 combination key support for ANSI/VT100 terminals. | |
| Sredir Memory Display Delay | Use this setting to set the delay in seconds to display memory information. Options are No Delay , 1 SEC, 2 SECS and 4 SECS. | |

Table 4-11. Hardware Health Monitor Submenu

| Menu Item | Description | | |
|---|---|--|--|
| CPU Overheat Alarm | Use the "+" and "-" keys to set the CPU temperature threshold to between 65° and 90° C. When this threshold is exceeded, the overheat LED on the chassis will light up and an alarm will sound. The LED and alarm will turn off once the CPU temperature has dropped to 5 degrees below the threshold set. The default setting is 72° C. | | |
| ►System Fan Monitor | Submenu | | |
| Fan Speed Control | This feature allows you to determine how the system will control the speed of the onboard fans. Select WORKSTATION if your system is used as a Workstation. Select SERVER if your system is used as a server. Select Disable to disable the fan speed control function to allow the onboard fans to continuously run at full speed (12V). The options are 1) Disable (Full Speed) 2) 3-PIN (SERVER) and 3) 3-PIN (WORKSTATION). | | |
| FAN1 Speed through FAN4 Reading | The speeds of the onboard fans (in rpm) are displayed here. | | |
| Other items in the submenu are systems monitor displays for the followin information: Other Information CPU1 TEMPERATURE, CPU2 TEMPERATURE (for 2U systems), SYSTEM TEMPERATURE, VCOREA, VCOREB (for 2U systems), HT VOLTAGE, CPU1 NVTT, CPU2 MEM VTT, CPU1 MEM, CPU2 MEM, 12V, 3.3V, VDD, 5V VSB, MCP55VCORE, 1.5V and VBAT. | | | |

Table 4-12. IPMI Configuration

| Menu Item | Description | | |
|--------------------------------|---|--|--|
| ► View BMC System Event Log | Use the "+" and "-" keys to navigate through the system event log. Pressing the Enter key will open the following setting: | | |
| Clear BMC System Event Log | Selecting this and pressing the Enter key will clear the BMC system event log. | | |
| Set LAN Configuration | Use the "+" and "-" keys to choose the desired channel number. | | |
| ▶ IP Address | Use the "+" and "-" keys to select the parameter. The IP address and current IP address in the BMC are shown. | | |
| ► MAC Address | Use the "+" and "-" keys to select the parameter. The MAC address and curren MAC address in the BMC are shown. | | |
| ► Subnet Mask | Use the "+" and "-" keys to select the parameter. The subnet address and curren subnet address in the BMC are shown. | | |
| ► Set PEF Configurati | ▶ Set PEF Configuration Submenu | | |
| PEF Support | Use this setting to ENABLE or Disable PEF support. When enabled, the following settings will appear: | | |
| BMC Watch Dog Timer Action | This setting is used to set the Watch Dog function. The options are Disabled , RESET SYSTEM, POWER DOWN and POWER CYCLE. | | |

4-5 Boot Menu

The BOOT menu is accessible only when the LOAD ONBOARD LAN OPTION ROM setting (in the PCI/PNP CONFIGURATION menu) is enabled. Menu items in the BOOT menu are shown below in Table 4-13.

Table 4-13. Boot Menu

| Menu Item | Description | |
|---------------------------|--|--|
| ► Boot Device Priority | This feature allows the user to prioritize the boot sequence from the available devices. | |
| ► Hard Disk Drives | This feature allows the user to specify the boot sequence from available hard disk drives. | |

4-6 Security Menu

AMI BIOS provides a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first in the SECURITY menu. Menu items for the security menu are shown below in Table 4-14.

Table 4-14. Security Menu

| Menu Item | Description | | | |
|---------------------------------|--|--|--|--|
| Change Supervisor Password | Select this option and press <enter> to access the sub menu, and then type in the password.</enter> | | | |
| Change User Password | Select this option and press <enter> to access the sub menu, and then type in the password.</enter> | | | |
| Boot Sector Virus Protection | This option is near the bottom of the SECURITY SETUP screen. Select Disabled to deactivate the Boot Sector Virus Protection. Select ENABLED to enable boot sector protection. | | | |
| | When ENABLED, the AMI BIOS displays a warning when any program (or virus) issues a DISK FORMAT command or attempts to write to the boot sector of the hard disk drive. The options are ENABLED and Disabled . | | | |

4-7 Exit Menu

Select the EXIT tab from AMI BIOS SETUP UTILITY screen to enter the EXIT BIOS SETUP screen. Then Exit menu items are described in Table 4-15 below.

Table 4-15. Exit Menu

| Menu Item | Description | | |
|----------------------------|---|--|--|
| Save Changes and Exit | When you have completed the system configuration changes, select this option to leave BIOS Setup and reboot the computer, so the new system configuration parameters can take effect. Select SAVE CHANGES AND EXIT from the EXIT menu and press <enter>.</enter> | | |
| Discard Changes and Exit | Select this option to quit BIOS Setup without making any permanent changes to the system configuration and reboot the computer. Select DISCARD CHANGES AND EXIT from the EXIT menu and press <enter>.</enter> | | |
| Discard Changes | Select this option and press <enter> to discard all the changes and return to AMI BIOS Utility Program.</enter> | | |
| Load Optimal Defaults | To set this feature, select LOAD OPTIMAL DEFAULTS from the EXIT menu and pres <enter>. Then select "OK" to allow BIOS to automatically load the OPTIMAL DEFAULTS as the BIOS Settings. The OPTIMAL settings are designed for maximum system performance, but may not work best for all computer applications.</enter> | | |
| Load Fail-Safe Defaults | To set this feature, select LOAD FAIL-SAFE DEFAULTS from the EXIT menu and press <enter>. The FAIL-SAFE settings are designed for maximum system stability, but not maximum performance.</enter> | | |

Appendix A BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list (on the following page) correspond to the number of beeps for the corresponding error. All errors listed, with the exception of Beep Code 8, are fatal errors.

Table A-1. AMIBIOS Error Beep Codes

| Beep Code | Error Message | Description |
|-----------------|---------------|---|
| 1 beep | Refresh | Circuits have been reset (Ready to power up.) |
| 5 short, 1 long | Memory error | No memory detected in system |
| 1 long, 8 short | Video error | Video adapter disabled or missing |

| HADI | MT/H8DMT | -IBX/H8DM | T-F/H8DMT-IR | KF User's Manu | ıal |
|------|----------|-----------|--------------|----------------|-----|
| | | | | | |

Notes

Appendix B BIOS POST Checkpoint Codes

B-1 Uncompressed Initialization Codes

The uncompressed initialization checkpoint codes are listed in order of execution:

| Checkpoint | Code Description | |
|------------|--|--|
| D0h | The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified. | |
| D1h | Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh and entering 4 GB flat mode next. | |
| D3h | Starting memory sizing next. | |
| D4h | Returning to real mode. Executing any OEM patches and setting the Stack next. | |
| D5h | Passing control to the uncompressed code in shadow RAM at E000:0000h. T initialization code is copied to segment 0 and control will be transferred to segment 0. | |

B-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

| Checkpoint | Code Description |
|------------|--|
| E0h | The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test. |
| E1h | Initializing the interrupt vector table next. |
| E2h | Initializing the DMA and Interrupt controllers next. |
| E6h | Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory. |
| Edh | Initializing the floppy drive. |
| Efh | A read error occurred while reading the floppy drive in drive A:. |
| F0h | Next, searching for the AMIBOOT.ROM file in the root directory. |
| F1h | The AMIBOOT.ROM file is not in the root directory. |
| F2h | Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file. |
| F3h | Next, reading the AMIBOOT.ROM file, cluster by cluster. |
| F4h | The AMIBOOT.ROM file is not the correct size. |
| F5h | Next, disabling internal cache memory. |
| FBh | Next, detecting the type of flash ROM. |

| Checkpoint | Code Description |
|------------|---|
| FCh | Next, erasing the flash ROM. |
| FDh | Next, programming the flash ROM. |
| FFh | Flash ROM programming was successful. Next, restarting the system BIOS. |

B-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution.

These codes are uncompressed in F0000h shadow RAM.

| Checkpoint | Code Description |
|------------|---|
| 03h | The NMI is disabled. Next, checking for a soft reset or a power on condition. |
| 05h | The BIOS stack has been built. Next, disabling cache memory. |
| 06h | Uncompressing the POST code next. |
| 07h | Next, initializing the CPU and the CPU data area. |
| 08h | The CMOS checksum calculation is done next. |
| 0Ah | The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next. |
| 0Bh | The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued. |
| 0Ch | The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller. |
| 0Eh | The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test. |
| 0Fh | The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next. |
| 10h | The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command. |
| 11h | Next, checking if <end <ins="" or=""> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <end> key was pressed.</end></end> |
| 12h | Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2. |
| 13h | The video display has been disabled. Port B has been initialized. Next, initializing the chipset. |
| 14h | The 8254 timer test will begin next. |
| 19h | Next, programming the flash ROM. |
| 1Ah | The memory refresh line is toggling. Checking the 15 second on/off time next. |
| 2Bh | Passing control to the video ROM to perform any required configuration before the video ROM test. |
| 2Ch | All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it. |

| The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control Reading the 8042 input port and disabling the MEGAKEY Green PC feature |
|---|
| Reading the 8042 input port and disabling the MEGAKEY Green PC feature |
| next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors. |
| The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin. |
| Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on. |
| Any initialization before setting video mode will be done next. |
| Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next. |
| Bus initialization system, static, output devices will be done next, if present. See the last page for additional information. |
| Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next. |
| The EGA/VGA controller was not found. The display memory read/write test is about to begin. |
| The display memory read/write test passed. Look for retrace checking next. |
| The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next. |
| The alternate display memory read/write test passed. Looking for alternate display retrace checking next. |
| Video display checking is over. Setting the display mode next. |
| The display mode is set. Displaying the power on message next. |
| Initializing the bus input, IPL, general devices next, if present. See the last page of this chapter for additional information. |
| Displaying bus initialization error messages. See the last page of this chapter for additional information. |
| The new cursor position has been read and saved. Displaying the Hit message next. |
| The Hit message is displayed. The protected mode memory test is about to start. |
| Preparing the descriptor tables next. |
| The descriptor tables are prepared. Entering protected mode for the memory test next. |
| Entered protected mode. Enabling interrupts for diagnostics mode next. |
| Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. |
| Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next. |
| The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next. |
| |

| Checkpoint | Code Description |
|------------|--|
| 47h | The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next. |
| 48h | Patterns written in base memory. Determining the amount of memory below 1 MB next. |
| 49h | The amount of memory below 1 MB has been found and verified. |
| 4Ch | The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next. |
| 4Dh | The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next. |
| 4Eh | The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next. |
| 4Fh | The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next. |
| 50h | The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next. |
| 51h | The memory size display was adjusted for relocation and shadowing. |
| 52h | The memory above 1 MB has been tested and initialized. Saving the memory size information next. |
| 53h | The memory size information and the CPU registers are saved. Entering real mode next. |
| 54h | Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. |
| 57h | The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. |
| 58h | The memory size was adjusted for relocation and shadowing. Clearing the Hit message next. |
| 59h | The Hit message is cleared. The <wait> message is displayed. Starting the DMA and interrupt controller test next.</wait> |
| 60h | The DMA page register test passed. Performing the DMA Controller 1 base register test next. |
| 62h | The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next. |
| 65h | The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next. |
| 66h | Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next. |
| 67h | Completed 8259 interrupt controller initialization. |
| 7Fh | Extended NMI source enabling is in progress. |
| 80h | The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next. |
| 81h | A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next. |

| The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next. The command byte was written and global data initialization has completed. Checking for a locked key next. Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next. The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next. The password was checked. Performing any required programming before WINBIOS Setup next. The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup with windity next. Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup has completed. Displaying the power on screen message next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The floppy drive controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. Performing any required processing after the option ROM returned control. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Part adaptor ROM check is next. Set the timer and printer base addresses. Setting the RS-232 base address next. Pha Set the timer and printer base addresses. Setting the RS-232 base address next. Pohn Required initialization before t | Checkpoint | Code Description |
|--|------------|---|
| Checking for a locked key next. Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next. The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next. The password was checked. Performing any required programming before WINBIOS Setup next. The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next. Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. Programming the WINBIOS Setup potions next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initializing before passing control to the adaptor ROM at C800. In ladaptor ROM check is next. Preforming any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address. Setting the RS-232 base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. PCh Required initialization before the Coprocessor test is over. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command ne | 82h | |
| RAM data next. The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next. The password was checked. Performing any required programming before WINBIOS Setup next. The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next. Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. BCh Programming the WINBIOS Setup options next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initializing before passing control to the adaptor ROM at C800. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. BCh Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 83h | |
| password or bypassing WINBIOS Setup next. The password was checked. Performing any required programming before WINBIOS Setup next. The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next. Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. The Programming the WINBIOS Setup options next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Coprocessor initialization before the Coprocessor test is over. Initializing the Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 84h | |
| WINBIOS Setup next. The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next. Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. Programming the WINBIOS Setup options next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initialization before the C800 adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base addresses. Setting the RS-232 base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 85h | |
| WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next. Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. Programming the WINBIOS Setup options next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The Hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. Phe adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base address. Performing any required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialization. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 86h | |
| necessary programming after WINBIOS Setup next. The programming after WINBIOS Setup has completed. Displaying the power on screen message next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Required initialization before the Coprocessor test is over. Initialization after the Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 87h | WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup |
| screen message next. 8Ch Programming the WINBIOS Setup options next. 8Dh The WINBIOS Setup options are programmed. Resetting the hard disk controller next. 8Fh The hard disk controller has been reset. Configuring the floppy drive controller next. 91h The floppy drive controller has been configured. Configuring the hard disk drive controller next. 95h Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. 96h Initialization before passing control to the adaptor ROM at C800. 97h Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. 98h The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. 99h Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. 98h Set the timer and printer base addresses. Setting the RS-232 base address next. 98h Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. 99h Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. 90h Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 88h | |
| The WINBIOS Setup options are programmed. Resetting the hard disk controller next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 89h | |
| next. The hard disk controller has been reset. Configuring the floppy drive controller next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 8Ch | Programming the WINBIOS Setup options next. |
| next. The floppy drive controller has been configured. Configuring the hard disk drive controller next. Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 8Dh | , , , , , , |
| psh linitializing the bus option ROMs from C800 next. See the last page of this chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 8Fh | 9 9 117 |
| chapter for additional information. Initializing before passing control to the adaptor ROM at C800. Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 91h | |
| Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 95h | |
| adaptor ROM check is next. The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 96h | Initializing before passing control to the adaptor ROM at C800. |
| Performing any required processing after the option ROM returned control. Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next. Set the timer and printer base addresses. Setting the RS-232 base address next. Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 97h | |
| the timer data area and printer base address next. 9Ah Set the timer and printer base addresses. Setting the RS-232 base address next. 9Bh Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. 9Ch Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. 9Dh Coprocessor initialized. Performing any required initialization after the Coprocessor test next. 9Eh Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 98h | |
| 9Bh Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next. 9Ch Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. 9Dh Coprocessor initialized. Performing any required initialization after the Coprocessor test next. 9Eh Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 99h | |
| initialization before the Coprocessor test next. Required initialization before the Coprocessor test is over. Initializing the Coprocessor next. Coprocessor initialized. Performing any required initialization after the Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 9Ah | Set the timer and printer base addresses. Setting the RS-232 base address next. |
| Coprocessor next. 9Dh Coprocessor initialized. Performing any required initialization after the Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 9Bh | |
| 9Eh Coprocessor test next. Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 9Ch | |
| 9Eh keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next. | 9Dh | |
| A2h Displaying any soft errors next. | 9Eh | keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID |
| | A2h | Displaying any soft errors next. |

| Checkpoint | Code Description |
|------------|--|
| A3h | The soft error display has completed. Setting the keyboard typematic rate next. |
| A4h | The keyboard typematic rate is set. Programming the memory wait states next. |
| A5h | Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next. |
| A7h | NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next. |
| A8h | Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next. |
| A9h | Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next. |
| Aah | Initialization after E000 option ROM control has completed. Displaying the system configuration next. |
| Abh | Uncompressing the DMI data and executing DMI POST initialization next. |
| B0h | The system configuration is displayed. |
| B1h | Copying any code to specific areas. |
| 00h | Code copying to specific areas is done. Passing control to INT 19h boot loader next. |

Disclaimer

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| H8DMT/H8DMT-IBX/H8DMT-F/H8DMT-IBXF User's Manual |
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