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CW6631B

Bluetooth Audio Player Microcontroller

User Manual

[CW6631B-UM-EN]

Versions: 1.0.0

Release Date: 2015-12-4

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Table of content

1 Product Overview

1.1 Outline

CW6631B is an MCS-51™ Compatible high performance mixed signal microcontroller. It integrates advanced digital and analog peripherals to suit for BT audio playback and BT Communicate applications.

1.2 Features

- CPU Compatible with MCS-51TM instruction set;
- Compliant to Bluetooth 3.0 + EDR, backward-compatible with BT1.2, 2.0 and 2.1
- Support SCMS-T content protection method;
- Support HFP v1.6, HSP v1.2, A2DP 1.3, AVCTP 1.4, AVDTP 1.3 and AVRCP 1.5
- Class 2 power level, RF Performance: Tx:0dBm, Rx: -80dBm;
- Support simple pairing and auto reconnection function;
- Support MP3/SBC decoder;
- Support two pairs of AUX;
- Six Channels 10-bit SARADC;
- CW6631B support 16bit Stereo DAC with >90dB SNR, embedded with four class A/B headphone amplifier
- 16bit Mono ADC with >90dB DR
- Support Audio record function to MIC ADPCM;
- Support Audio playback from SD/USB
- Keypad tone mixer;
- Two 8-bit timers, support Capture and PWM mode;
- Two 16-bit timers, support Capture and PWM mode;
- Watchdog Timer with on-chip RC oscillator;
- Support full-duplex IIS, UART, SPI, SD interface;
- Support IIC interface for FM function;
- 2 channels 16 levels Low Voltage Detector;
- Power on Reset
- Support Full speed USB 2.0 PHY;
- Full speed USB 2.0 HOST/DEVICE controller;
- IR controller;
- Independent powered Real-Time Clock supporting 32.768kHz crystal
- Internal crystal oscillator support 26M crystal
- Internal LDO regulator:1.35V to 1.2V;4.2V to 3.3V
- Built-in buck converter,DC-DC:4.2V to 1.35V

2 Pin Definitions

2.1 CW6631B

2.1.1 Package

SSOP28

2.1.2 Pin Assignment

Figure 2-1 shows the pin assignment of CW6631B.

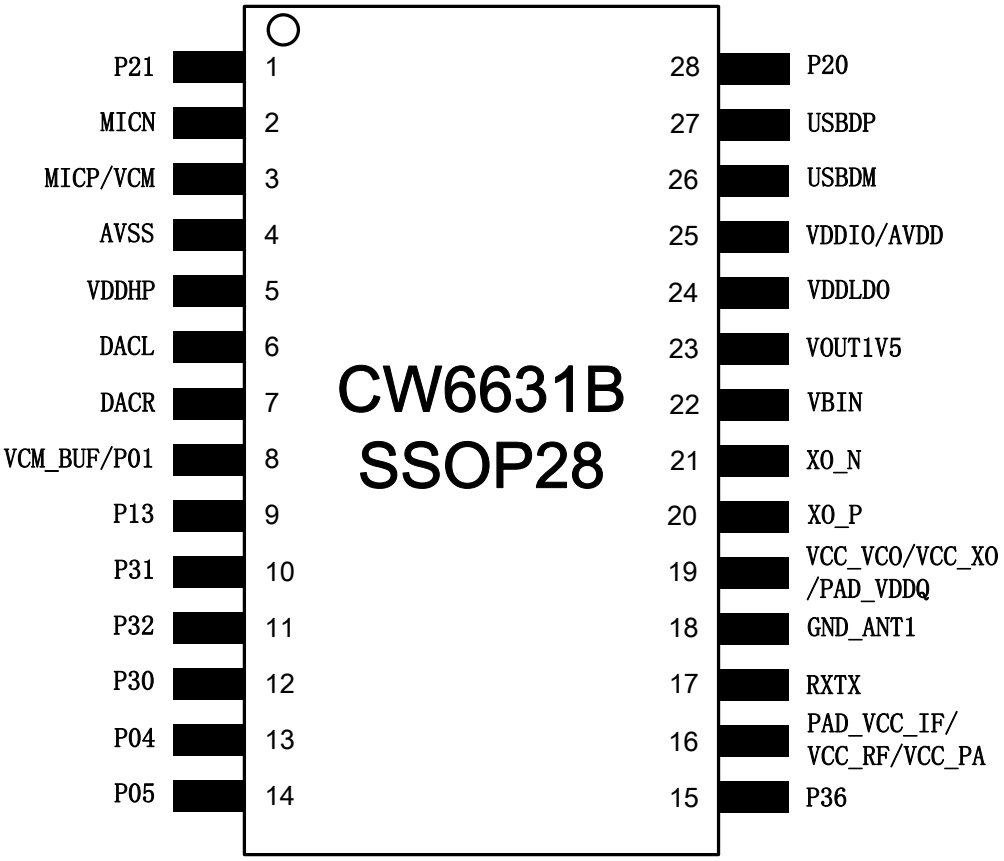


Figure 2-1 Pin Assignment of CW6631B

2.1.3 Pin Description

Table 2-1 shows the pin description of CW6631B.

Table 2-1 Pin Description of CW6631B

Pin No.SSOP28	Name	Type	Function
1	P21	I/O	GPIO AUXR2 ADC1

Pin No.SSOP28	Name	Type	Function
			SDCLK EMIDAT1 LCD_D1
2	MICN	A	MIC Negative input
3	MICP/VCM	A	MIC Positive input DAC VCM output
4	AVSS	GND	Analog GND
5	VDDHP	PWR	Headphone power
6	DACR	A	DAC right output GPIO input
7	P01/VCM_BUF	I/O	GPIO AUXR0 UARTTX1 PORT INT/WKUP0 SDDAT2 DAC VCM buffer
8	P00	I/O	GPIO AUXL0 UARTRX1 SDDAT1 SPI0DIN2
9	P13	I/O	GPIO ADC5 IISBCLK0
10	P31	I/O	GPIO SDCMD SPI0DIN3
11	P32	I/O	GPIO SDDAT0 SPI0DOUT3/DIN3
12	P30	I/O	GPIO ADC4 SDCLK SPI0CLK3
13	P04	I/O	GPIO SPI1DOUT/DIN1
14	P05	I/O	GPIO SPI1CLK
15	P36	I/O	GPIO
16	VCC_RF/VCC_PA/ PAD_VCC_IF	PWR	RF/PA Power VCC Power VCC
17	RXTX	A	RF Rx and Tx pin

Pin No.SSOP28	Name	Type	Function
18	GND_ANT1	GND	RF GND
19	VCC_XO/ PAD_VDDQ/ VCC_VCO	PWR	Power VCC/VDDQ
20	XO_P	A	BT 26MHz XOSC Positive Pin
21	XO_N	A	BT 26MHz XOSC Negative Pin
22	BVIN	PWR	PMU Power input Pin 4.2V(typ)
23	VOUT1V5	PWR	VOUT 1.5V
24	VDDLDO	PWR	LDO power input 4.2V(typ)
25	VDDIO/AVDD	PWR	Power output VDDIO 3.3V
26	USBDM	I/O	USB Negative Input/output
27	USBDP	I/O	USB Positive Input/output
28	P20	I/O	GPIO AUXL2 SDCMD EMIDAT0 LCD_D0

3 CPU Core Information

3.1 Architecture

The AXC51-CORE of CW6631B is fully compatible with the MCS-51™ instruction set.

The AXC51-CORE employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12MHz. By contrast, the AXC51-CORE executes most of its instructions in 1 system clock cycle. With system clock running at 48 MHz, it has a peak throughput of 48 MIPS running in on-chip SRAM area.

3.2 Instruction Set

The instruction set of the AXC51-CORE is fully compatible with the standard MCS-51™ instruction set; standard 8051 development tools can be used to develop software for the AXC51-CORE. All instructions of AXC51-CORE are the binary and functional equivalent of their MCS-51™ counterparts, including op-codes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051. *Table 3-1* shows AXC51-CORE Instruction Set Summary

Table 3-1 AXC51-CORE Instruction Set Summary

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in IRAM)
1	NOP		1
2	AJMP	code addr	3
3	LJMP	code addr	3
1	RR	A	1
1	INC	A	1
1	INC	data addr	1
1	INC	@Ri	1
1	INC	Rn	1
3	JBC	bit addr, code addr	1 or 3
2	ACALL	code addr	3
3	LCALL	code addr	3
1	RRC	A	1
1	DEC	A	1
2	DEC	data addr	1
1	DEC	@Ri	1
1	DEC	Rn	1
3	JB	bit addr, code addr	1 or 3
1	RET		4
1	RL	A	1
2	ADD	A, #data	1

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in IRAM)
2	ADD	A, data addr	1
1	ADD	A, @Ri	1
1	ADD	A, Rn	1
3	JNB	bit addr, code addr	1 or 3
1	RETI		4
1	RLC	A	1
2	ADDC	A, #data	1
2	ADDC	A, data addr	1
1	ADDC	A, @Ri	1
1	ADDC	A, Rn	1
2	JC	code addr	1 or 3
2	ORL	data addr, A	1
3	ORL	data addr, #data	1
2	ORL	A, #data	1
2	ORL	A, data addr	1
1	ORL	A, @Ri	1
1	ORL	A, Rn	1
2	JNC	code addr	1 or 3
2	ANL	data addr, A	1
2	ANL	data addr, #data	1
1	ANL	A, @Ri	1
1	ANL	A, Rn	1
2	JZ	code addr	1 or 3
2	XRL	data addr, A	1
3	XRL	data addr, #data	1
2	XRL	A, #data	1
2	XRL	A, data addr	1
1	XRL	A, @Ri	1
1	XRL	A, Rn	1
2	JNZ	code addr	1 or 3
2	ORL	C, bit addr	1
1	JMP	@A+DPTR	3
2	MOV	A, #data	1
3	MOV	data addr, #data	1
2	MOV	@Ri, #data	1
2	MOV	Rn, #data	1
2	SJMP	code addr	3
2	ANL	C, bit addr	1
1	MOVC*	A, @A+PC	1
1	DIV	AB	1
3	MOV	data addr, data addr	1

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in IRAM)
2	MOV	data addr, @Ri	1
2	MOV	data addr, Rn	1
3	MOV	DPTR, #data	1
2	MOV	bit addr, C	1
1	MOVC*	A, @A+DPTR	2
2	SUBB	A, #data	1
2	SUBB	A, data addr	1
1	SUBB	A, @Ri	1
1	SUBB	A, Rn	1
2	ORL	C, bit addr	1
2	MOV	C, bit addr	1
1	INC	DPTR	1
1	MUL	AB	1
2	MOV	@Ri, data addr	1
2	MOV	Rn, data addr	1
2	ANL	C, bit addr	1
2	CPL	bit addr	1
2	CPL	C	1
3	CJNE	A, #data, code addr	1 or 3
3	CJNE	A, data addr, code addr	1 or 3
3	CJNE	@Ri, #data, code addr	1 or 3
3	CJNE	Rn, #data, code addr	1 or 3
2	PUSH	data addr	1
2	CLR	bit addr	1
1	CLR	C	1
1	SWAP	A	1
2	XCH	A, data addr	1
1	XCH	A, @Ri	1
1	XCH	A, Rn	1
2	POP	data addr	1
2	SETB	bit addr	1
1	SETB	C	1
1	DA	A	1
3	DJNZ	data addr, code addr	1 or 3
1	XCHD	A, @Ri	1
2	DJNZ	Rn, code addr	1 or 3
1	MOVX	A, @DPTR	2
1	MOVX	A, @Ri	2
1	CLR	A	1
2	MOV	A, data addr	1
1	MOV	A, @Ri	1

18 Characteristics

18.1 PMU Parameters

Table 18-1 PMU Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
BVIN	Buck input voltage	2.8	4.2	4.8	V	
VDDLDO	VDDLDO input voltage	2.8	4.2	4.8	V	
VOUT1V5	Buck output voltage	1.15	1.35	1.6	V	
VDDCORE	1.2V output voltage	-	1.2	-	V	
VDDRTC	input voltage	2.2	4.2	4.8	V	
VDDHP	3.0V output voltage	2.8	3.0	3.3	V	
VCM	1.5V output voltage	-	1.35	-	V	
RVDD	output voltage	1.1	1.2	1.3	V	
VDDIO	3.3V output voltage	2.8	3.3	-	V	

18.2 CORE PLL Parameters

Table 18-2 PLL Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
F_{I1}	Frequency input	-	32.768	-	KHz	Low frequency OSC
F_{I2}	Frequency input	1	12	15	MHz	High frequency OSC
F_{OUT1}	Frequency output	-	48	-	MHz	
T_{LOCK1}	PLL locked time	-	2	-	ms	Use low frequency OSC as input reference
T_{LOCK2}	PLL locked time	-	0.1	-	ms	Use high frequency OSC as input reference

18.3 General purpose I/O Parameters

Table 18-3 I/O Parameters

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Low-Level input voltage	-	-	30% * VDDIO	V	VDDIO = 3.3V
V_{IH}	High-level input voltage	70% * VDDIO	-	-	V	VDDIO = 3.3V
R_{PUP0}	Internal pull-up resister 0	-	10	-	KΩ	
R_{PUP1}	Internal pull-up resister 1	-	200	-	KΩ	
R_{PUP2}	Internal pull-up resister 2	-	0.5	-	KΩ	
R_{PDN0}	Internal pull-down resister 0	-	10	-	KΩ	
R_{PDN1}	Internal pull-down resister 1	-	0.33	-	KΩ	
R_{PDN2}	Internal pull-down resister 2	-	0.5	-	KΩ	
I_{LEVEL1}	Level1 current driving	8	-	-	mA	For PORT1

Symbol	Description	Min	Typ	Max	Units	Conditions
I_{LEVEL2}	Level2 current driving	24	-	-	mA	For Port1.1

18.4 Audio ADDA Parameters

Table 18-4 Audio DAC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
DAC SNR&DR		-	90	-	dB	48PIN
DAC SNR&DR		-	90	-	dB	28PIN & 20 PIN
DAC THD+N		-	-80	-	dB	10Kohm loading
PWR_{AB}	ClassAB AMP power output	-	-	16	mW	32ohm loading
V_{PP}	Maximum output voltage	-	-	2.6	V	10Kohm loading
ADC SNR/DR			93		dB	In Voice Band
ADC THD+N			89		dB	In Voice Band

18.5 RF Analog Blocks

Table 18-5 Frequency Synthesizer Parameters

Parameter	Condition		MIN	typ	max	Unit
Synthesizer						
Synthesizer settling time	Within +/- 25 KHz accuracy		-	70	-	us
Phase Noise	Fc=2.4GHz	ΔF=1 MHz	-	-110	-	dBc/Hz
		ΔF=2 MHz	-	-118	-	dBc/Hz
		ΔF≥3 MHz	-	-123	-	dBc/Hz
XTAL Oscillator						
Frequency range			-	26	-	MHz
Frequency Trimming Range	6 bits		-1	-	+1	kHz

Table 18-6 Receive path Parameters

Parameter	Condition		MIN	typ	max	Unit
Receiver Channel						
Minimum Usable Signal	RX sensitivity		-	-80	-	dBm
LNA						
Gain		High Gain	-	25	-	dB
		Mid Gain	-	15	-	dB
		Low Gain	-	5	-	dB
Mixer						
Conversion Gain			-	0	-	dB
Ifamp						

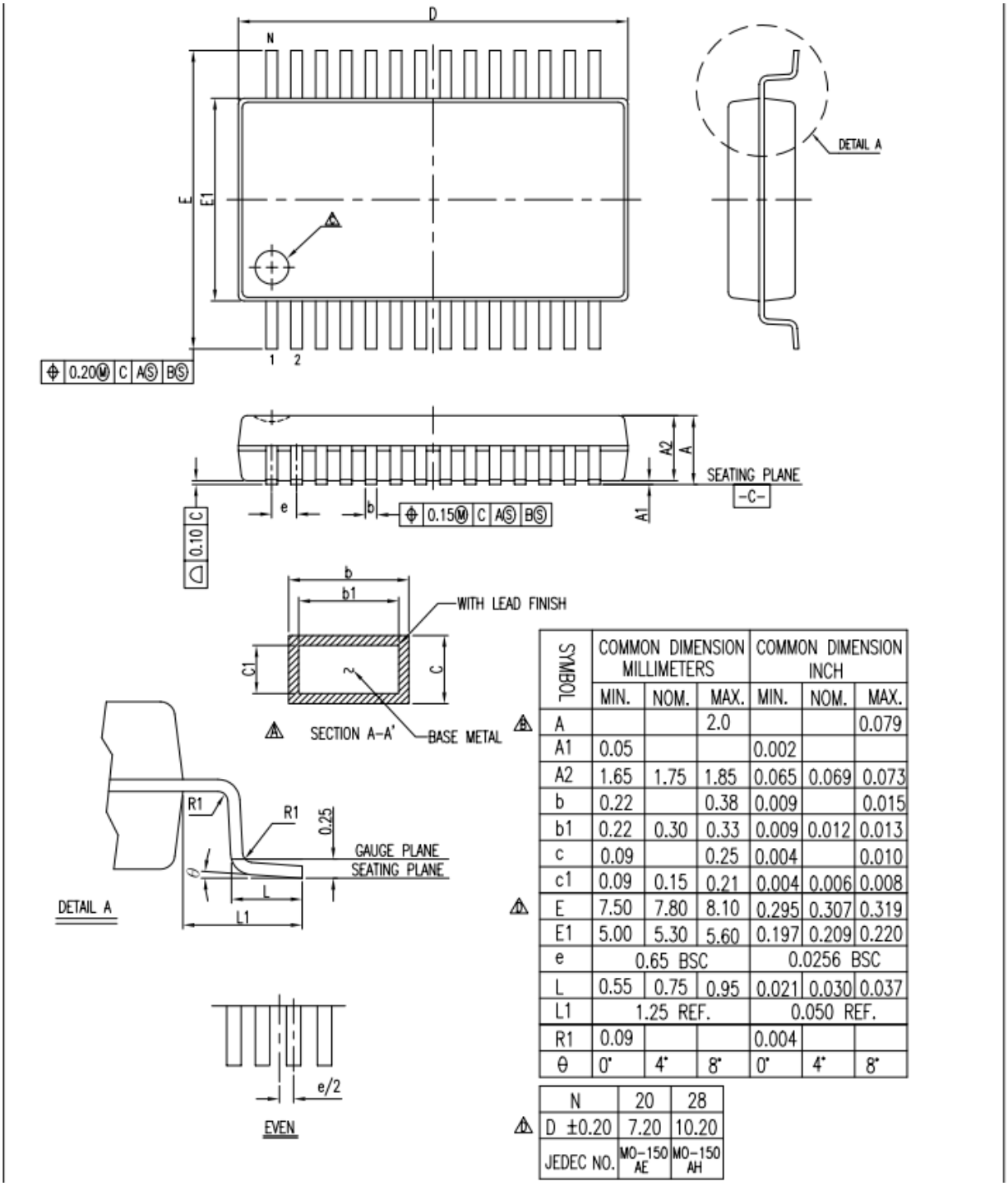
Parameter	Condition	MIN	typ	max	Unit
Gain	5/9/12/15/18 dB	-	12	-	
Complex BPF					
Band pass -3 dB BW	Figure 1.	-	2	-	MHz
Image Rejection		-	30	-	dB
VGA					
Gain Range		-6	-	+68	dB
Gain Step		-	+1/+6	-	dB
ADMOD					
SNDR	Freq = +- BW	-	>50	-	dB

Table 18-7 Transmit path Parameters

Parameter	Condition		MIN	typ	max	Unit
Transmit Channel						
Available output power			-2	0	1.5	dBm
Side Band Suppression			-	-30	-	dBm
LPF						
Low pass -3 dB BW	Figure 2.		-	1	-	MHz
TXVGA						
Gain Step			-7	-	7	dB
PA						
Gain Range	Set paPWR[2:0] of Control Register #16	GFSK	-12	-	4	dBm
		DPSK	-15	-	1	dBm

19 Package Outline Dimensions

19.1 SSOP28



SYMBOL	COMMON DIMENSION MILLIMETERS			COMMON DIMENSION INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			2.0			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
b1	0.22	0.30	0.33	0.009	0.012	0.013
c	0.09		0.25	0.004		0.010
c1	0.09	0.15	0.21	0.004	0.006	0.008
E	7.50	7.80	8.10	0.295	0.307	0.319
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BSC			0.0256 BSC		
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	1.25 REF.			0.050 REF.		
R1	0.09			0.004		
θ	0°	4°	8°	0°	4°	8°

N	20	28
D ±0.20	7.20	10.20
JEDEC NO.	MO-150 AE	MO-150 AH

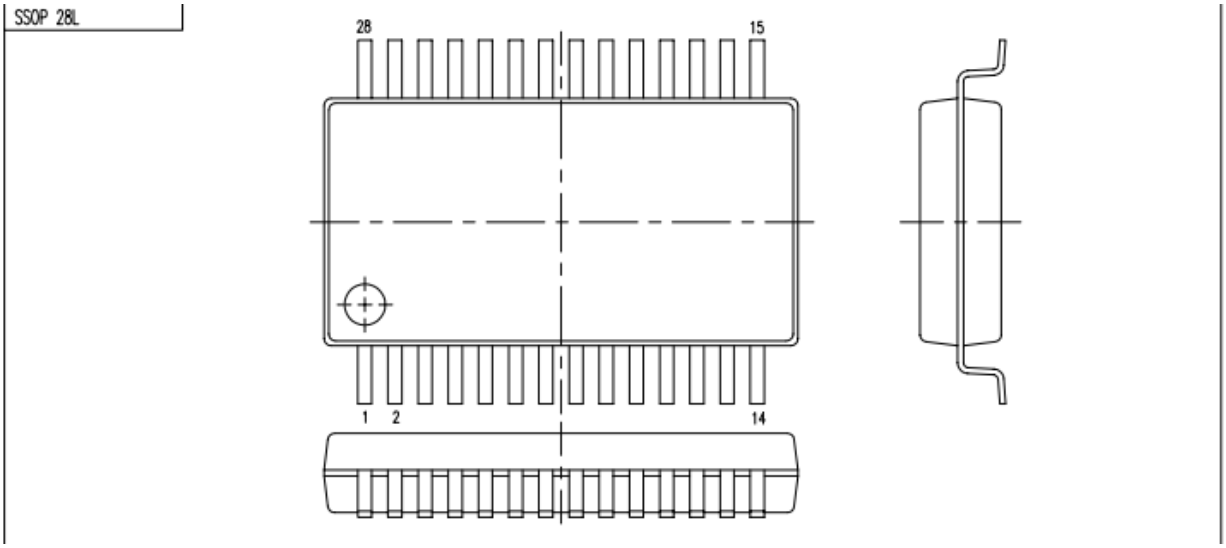


Figure 19-1 SSOP28 Package Outline Dimension

Revision History

Date	Version	Comments	Revised by
2015-7-22	0.0.1	Initial version	YX
2015-12-4	0.0.2	Checked	GAO
2015-12-4	1.0.0	Release	YX