UL865-N3G V2 Hardware User Guide

1VV0301177 Rev 2- 2015-04-20

Making machines talk.

APPLICABILITY TABLE

PRODUCT
UL865-N3G V2

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Contents

1. Introduction

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UL865-N3G V2 module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UL865-N3G V2 modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "UL865-N3G V2 Mechanical Dimensions"

Chapter 4: "UL865-N3G V2 Module Connections" deals with the pin out configuration and layout.

Chapter 5: "Hardware Commands" How to operate on the module via hardware.

Chapter 6: "Power supply" Power supply requirements and general design rules.

Chapter 7: "GSM/WCDMA Radio Section" The antenna connection and board layout design are the most important parts in the full product design.

Chapter 8: "Logic Level specifications" Specific values adopted in the implementation of logic levels for this module.

Chapter 9: "USB ports" The serial port on the Telit UL865-N3G V2 is the core of the interface between the module and OEM hardware

Chapter 10: "Serial ports" The serial port on the Telit UL865-N3G V2 is the core of the interface between the module and OEM hardware

Chapter 11: "Audio Section overview"

Chapter 12: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 13 "DAC and ADC Section" Deals with these two kind of converters.

Chapter 14: "Mounting the UL865-N3G V2 on the application board" Recommendations and specifics on how to mount the module on the user's board.

Chapter 15: "Packaging system" Recommendations and specifics on how the system is packaged.

Chapter 16: "Conformity Assessment Issues"

Chapter 17: "Safety Recommendations"

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- Digital Voice Interface Application Note 80000NT10050A
- SPI Port Application Note 80000NT10053A
- SIM Holder Design Guides 80000NT10001a
- AT Commands Reference Guide 80378ST10091A
- Telit EVK2 User Guide 1vv0300704

1.7. Document History

Revision	Date	Changes
Rev 0	2014-10-13	Preliminary Version
Rev.1	2015-04-01	Added par. 17/18
Rev.2	2015-04-20	Updated chapter 12

2. Overview

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UL865-N3G V2 module.

In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace all hardware solutions and products that may be designed. Avoiding the wrong solutions shall be considered as mandatory. While the suggested hardware configurations shall not be considered mandatory, the information given shall be used as a guide and a starting point for properly developing your product with the Telit UL865-N3G V2 module. For further hardware details that may not be explained in this document refer to the Telit UL865-N3G V2 Product Description document where all the hardware information is reported.

NOTICE:
(EN) The integration of the GSM/GPRS/WCDMA **UL865-N3G V2** cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare GSM/GPRS/WCDMA **UL865-N3G V2** all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des **UL865-N3G V2** GSM/GPRS/WCDMA Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija GSM/GPRS/WCDMA **UL865-N3G V2** modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo GSM/GPRS/WCDMA **UL865-N3G V2** debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire GSM/GPRS/WCDMA **UL865-N3G V2** dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי **UL865-N3G V2** עם המוצר.

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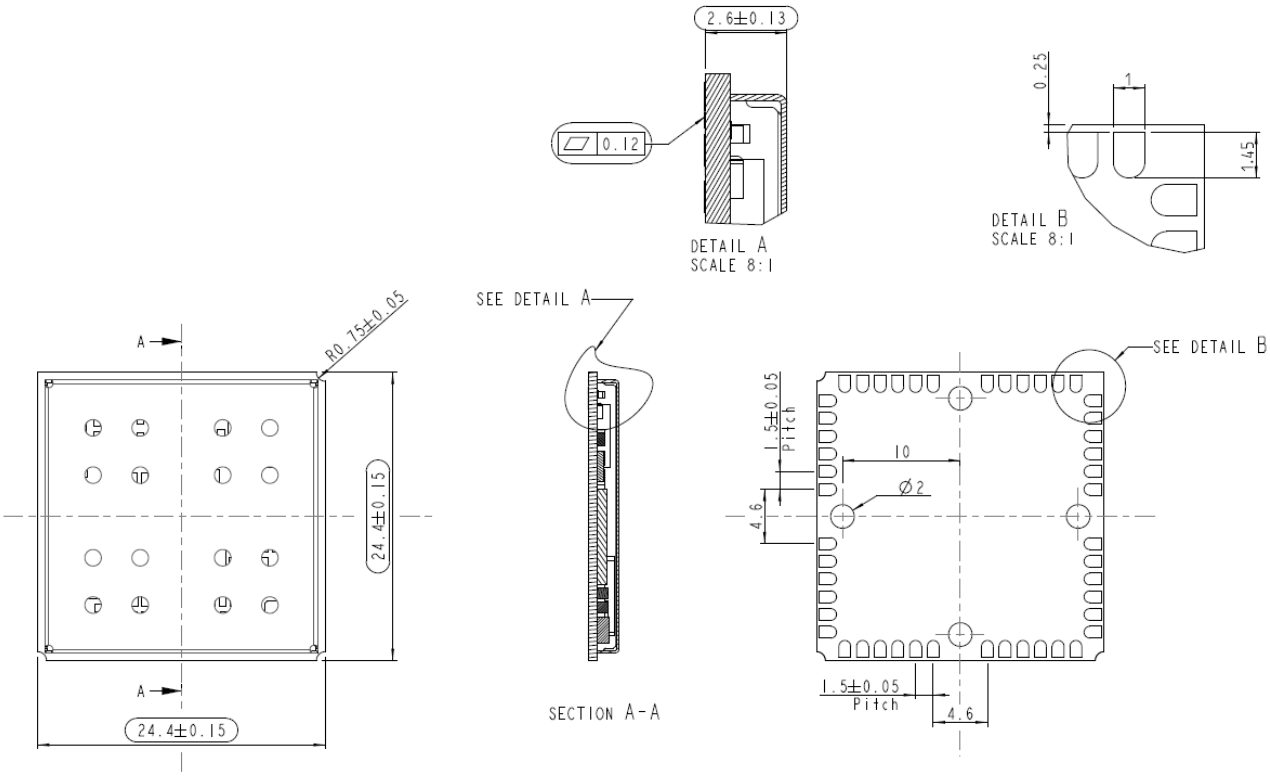
3. UL865-N3G V2 Mechanical Dimensions

The UL865-N3G V2 overall dimensions are:

Length:	24.4 mm
Width:	24.4 mm
Thickness:	2.6 mm
Weight	4 g



4. UL865-N3G V2 module connections

4.1. PIN-OUT

Pad	Signal	I/O	Function	Note	Type
Audio					
18	USB_D+	I/O	USB differential Data (+)		
17	USB_D-	I/O	USB differential Data (-)		
16	USB_VBUS	AI	Power sense for the internal USB transceiver.		
SIM card interface					
9	SIMVCC	-	External SIM signal – Power supply for the SIM		1,8 / 3V
10	SIMRST	O	External SIM signal – Reset		1,8 / 3V
11	SIMCLK	O	External SIM signal – Clock		1,8 / 3V
12	SIMIO	I/O	External SIM signal – Data I/O	4.7k Pull up	1,8 / 3V
X All GPI0 can be program med	SIMIN	I	Presence SIM input		CMOS 1.8V
Auxiliary					
44	RXD_AUX /SPI_MISO	I O	Auxiliary UART (RX Data) SPI_MISO		CMOS 1.8V
45	TXD_AUX / SPI_MOSI	O I	Auxiliary UART (TX Data) SPI_MOSI		CMOS 1.8V
Prog. / Data + HW Flow Control					
1	C109/DCD/GPO	O	Output for Data carrier detect signal (DCD) to DTE / GP output		CMOS 1.8V
2	C125/RING/GPO	O	Output for Ring indicator signal (RI) to DTE / GP output		CMOS 1.8V
3	C107/DSR/GPO	O	Output for Data set ready signal (DSR) to DTE / GP output		CMOS 1.8V
4	C108/DTR/GPI	I	Input for Data terminal ready signal (DTR) from DTE / GP input		CMOS 1.8V
5	C105/RTS/GPI	I	Input for Request to send signal (RTS) from DTE / GP input		CMOS 1.8V
6	C106/CTS/GPO	O	Output for Clear to send signal (CTS) to DTE / GP output		CMOS 1.8V
7	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 1.8V
8	C104/RXD	O	Serial data output to DTE		CMOS 1.8V
DAC and ADC					
13	ADC_IN1	AI	Analog/Digital converter input	Accepted values 0 to 1.2V DC	A/D
14	ADC_IN2	AI	Analog/Digital converter input	Accepted values 0 to 1.2V DC	A/D
15	DAC_OUT	AO	Digital/Analog converter output		D/A
Miscellaneous Functions					
30	VRTC	AO	backup for the embedded RTC supply (1.8V)		Power
47	RESET*	I	Reset Input		CMOS 1.8V
43	V_AUX / PWRMON	O	1.8V stabilized output Imax=100mA / Power ON monitor		Power Out 1.8V

Pad	Signal	I/O	Function	Note	Type
34	Antenna	I/O	Antenna pad – 50 Ω		RF
GPIO					
42	GPIO_01 / DVI_WA0	I/O	GPIO01 Configurable GPIO / Digital Audio Interface (WA0)		CMOS 1.8V
41	GPIO_02 / JDR / DVI_RX	I/O	GPIO02 I/O pin / Jammer Detect Report / Digital Audio Interface (RX)		CMOS 1.8V
40	GPIO_03 / DVI_TX	I/O	GPIO03 GPIO I/O pin / Digital Audio Interface (TX)		CMOS 1.8V
39	GPIO_04 / DVI_CLK	I/O	GPIO04 Configurable GPIO Digital Audio Interface (CLK)		CMOS 1.8V
29	GPIO_05	I/O	GPIO05 Configurable GPIO		CMOS 1.8V
28	GPIO_06 / SPI_SRDY	I/O	GPIO06 Configurable GPIO / ALARM / SPI_SRDY		CMOS 1.8V
27	GPIO_07 / SPI_MRDY	I/O	GPIO07 Configurable GPIO / Buzzer / SPI_MRDY		CMOS 1.8V
26	GPIO_08 / STAT_LED	I/O	GPIO08 Configurable GPIO / Digital Audio Interface (CLK)		CMOS 1.8V
25	SPI_CLK	I/O	SPI_CLK		CMOS 1.8V
Power Supply					
38	VBATT	-	Main power supply (Baseband)		Power
37	VBATT_PA	-	Main power supply (Radio PA)		Power
23	AGND	-	AF Signal Ground (see audio section)		AF Signal
32	GND	-	Ground		Power
33	GND	-	Ground		Power
35	GND	-	Ground		Power
36	GND	-	Ground		Power
46	GND	-	Ground		Power
23	GND	-	Ground		-
RESERVED					
19		-			
20		-			
21		-			
22		-			
24		-			
31		-			
48		-			

WARNING:

Reserved pins must not be connected.

NOTE:

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

Pin	signal	
38, 37	VBATT & VBATT_PA	
32, 33, 35, 36, 46	GND	
23	AGND	
7	C103/TXD	If not used should be connected to a Test Point
8	C104/RXD	If not used should be connected to a Test Point
5	C105/RTS	If not used should be connected to a Test Point
6	C106/CTS	If not used should be connected to a Test Point
43	V_AUX / PWRMON	
47	RESET*	
45	TXD_AUX	If not used should be connected to a Test Point
44	RXD_AUX	If not used should be connected to a Test Point
18	USB D+	If not used should be connected to a Test Point or an USB connector
17	USB D-	If not used should be connected to a Test Point or an USB connector
16	USB_VBUS	If not used should be connected to a Test Point or an USB connector

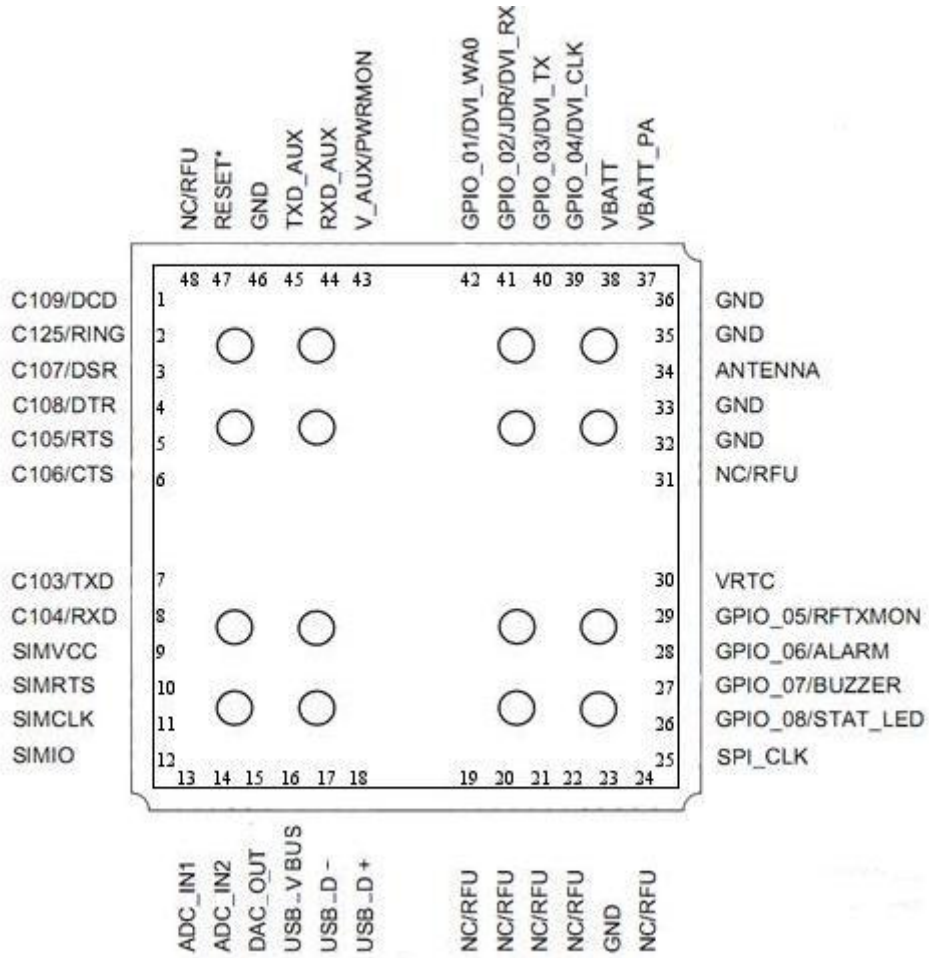
4.2. Debug in Production

To test and debug the assembled UL865-N3G V2, we strongly recommend foreseeing test pads on the host PCB, in order to check the connection between the UL865-N3G V2 itself and the application and to test the performance of the module connecting it with an external computer. Depending by the customer application, these pads include, but are not limited to the following signals:

TXD
RXD
RESET*
GND
VBATT
VBATT_PA
TX_AUX
RX_AUX
PWRMON

4.3. Pin Layout

TOP VIEW



NOTE:

The pins defined as NC/RFU shall be considered RESERVED and must not be connected to any pin in the application.

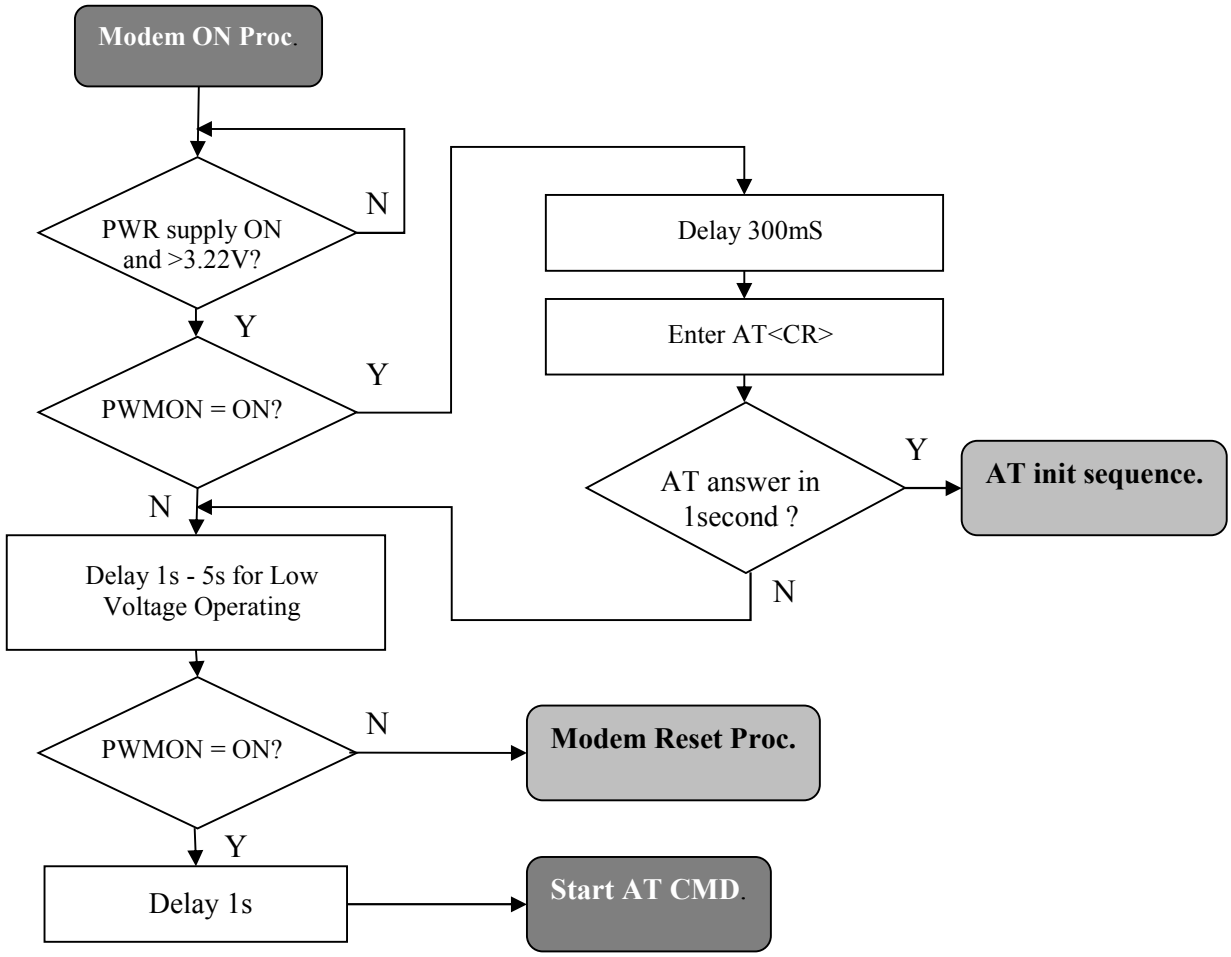
5. Hardware Commands

5.1. Auto-Turning ON the UL865-N3G V2

The UL865-N3G V2 will automatically power on itself when VBATT & VBATT_PA are applied to the module.

V_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating after 5 seconds.

The following flow chart shows the proper turn on procedure:



NOTE:

The power supply must be applied either at the same time on pins VBATT and VBATT_PA.

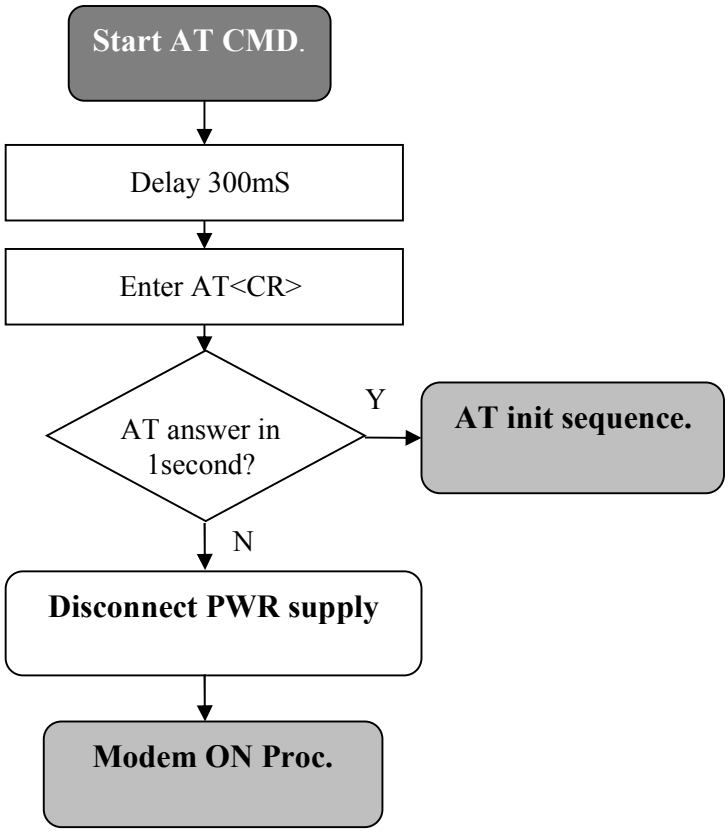
NOTE:

To guarantee a correct module's start-up please check that the Power Supply is with a level >3.22V within 21mS.

NOTE:

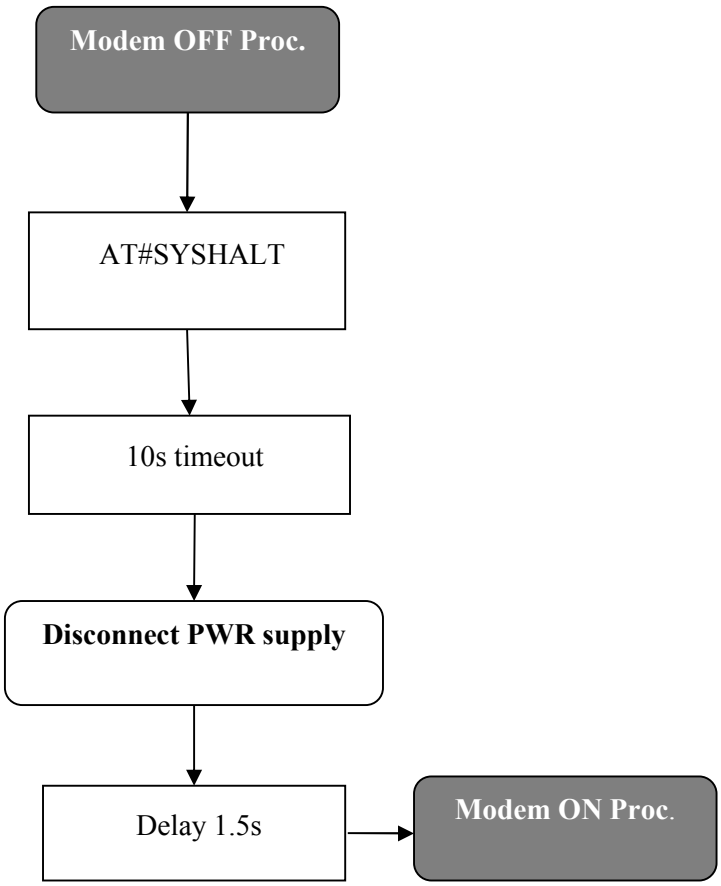
In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UL865-N3G V2 when the module is powered OFF or during an ON/OFF transition.

A flow chart showing the AT commands managing procedure is displayed below:



5.2. Turning OFF the UL865-N3G V2

The following flow chart shows the proper turnoff procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UL865-N3G V2 when the module is powered off or during an ON/OFF transition.

5.3. Resetting the UL865-N3G V2

5.3.1. Hardware Unconditional restart

To unconditionally reboot the UL865-N3G V2, the pad RESET* must be tied low for at least 200 milliseconds and then released.

The maximum current that can be drained from the ON* pad is 0,15 mA.

WARNING:

The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.

NOTE:

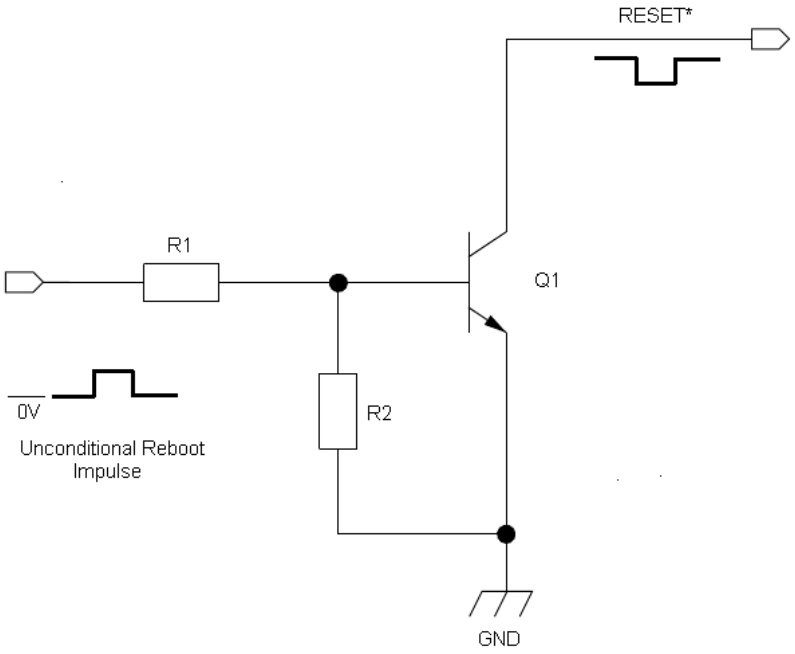
Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the UL865-N3G V2 power regulator and improper functioning of the module.

The line RESET* must be connected only in open collector configuration; the transistor must be connected as close as possible to the RESET* pin.

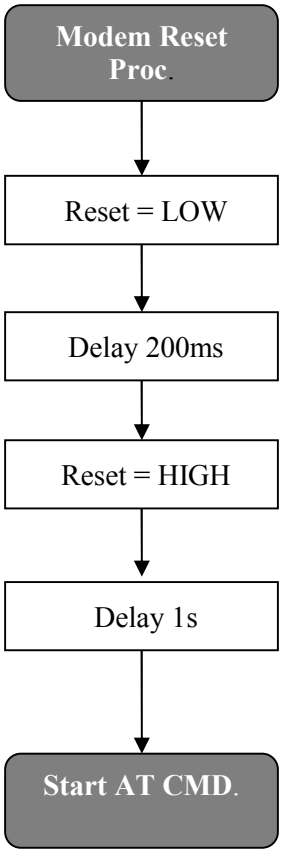
TIP:

The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

A simple circuit to do it is:



In the following flow chart is detailed the proper restart procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UL865-N3G V2 when the module is powered OFF or during an ON/OFF transition.

6. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performance, hence read the requirements carefully and the guidelines that will follow for a proper design.

6.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfill the following requirements:

POWER SUPPLY	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.40 V÷ 4.20 V
Extended Operating Voltage Range	3.1 V÷ 4.50 V

NOTE:

The Operating Voltage Range MUST never be exceeded; care must be taken in order to fulfil min/max voltage requirement.

NOTE:

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;

The “Extended Operating Voltage Range” can be used only with complete assumption and application of the HW User guide suggestions.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

The Power supply must be higher than 3.22 V to power on the module.

6.2. Power Consumption

UL865-N3G V2		
Mode	**Average (mA)**	**Mode description**
SWITCHED OFF		Module supplied but Switched Off
Switched Off	180 uA	
IDLE mode (WCDMA)		
AT+CFUN=5	1.8	Disabled TX and RX; DRX7
Operative mode (WCDMA)		
WCDMA Voice	152	WCDMA voice call (TX = 10dBm)
WCDMA HSDPA (0dBm)	187	WCDMA data call (Cat 8, TX = 0dBm)
WCDMA HSDPA (22dBm)	494	WCDMA data call (Cat 8, TX = 24dBm)

NOTE:

The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.

6.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

6.3.1. Electrical Design Guidelines

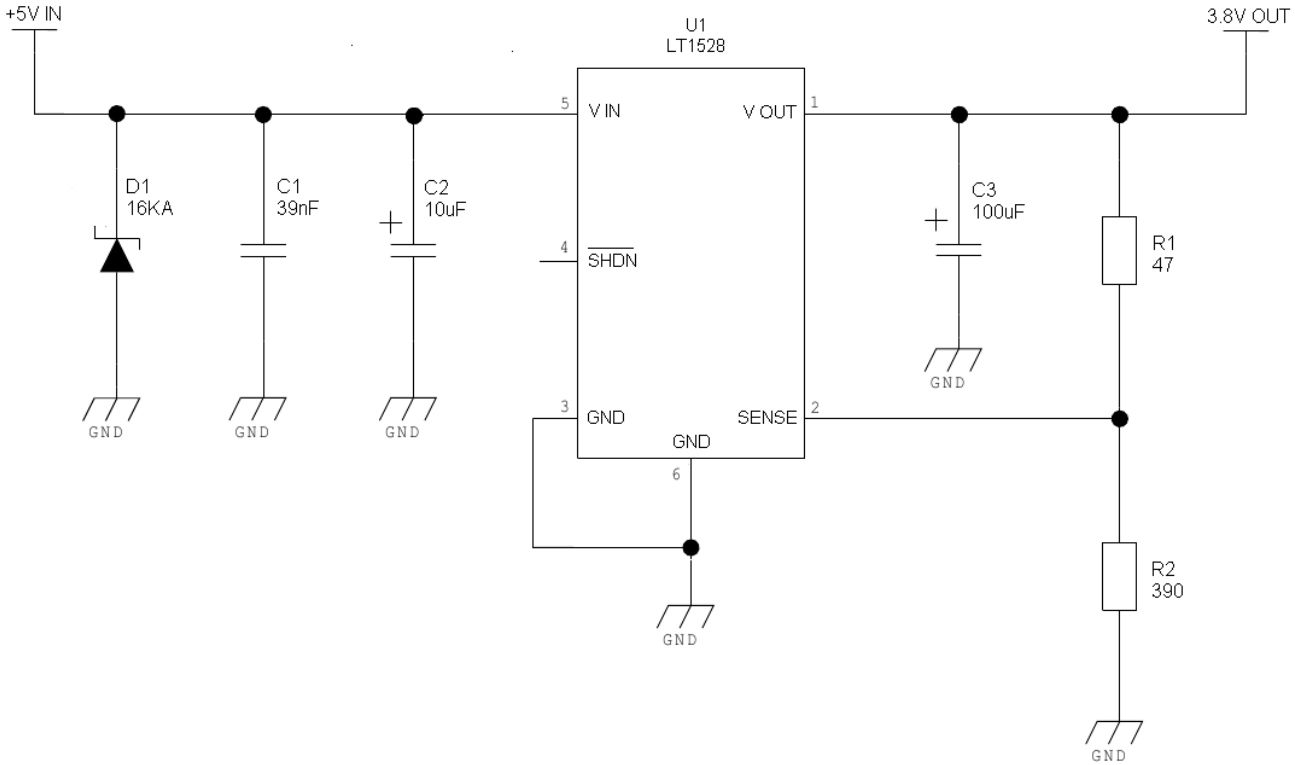
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

6.3.1.1. + 5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the UL865-N3G V2, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UL865-N3G V2 from power polarity inversion.

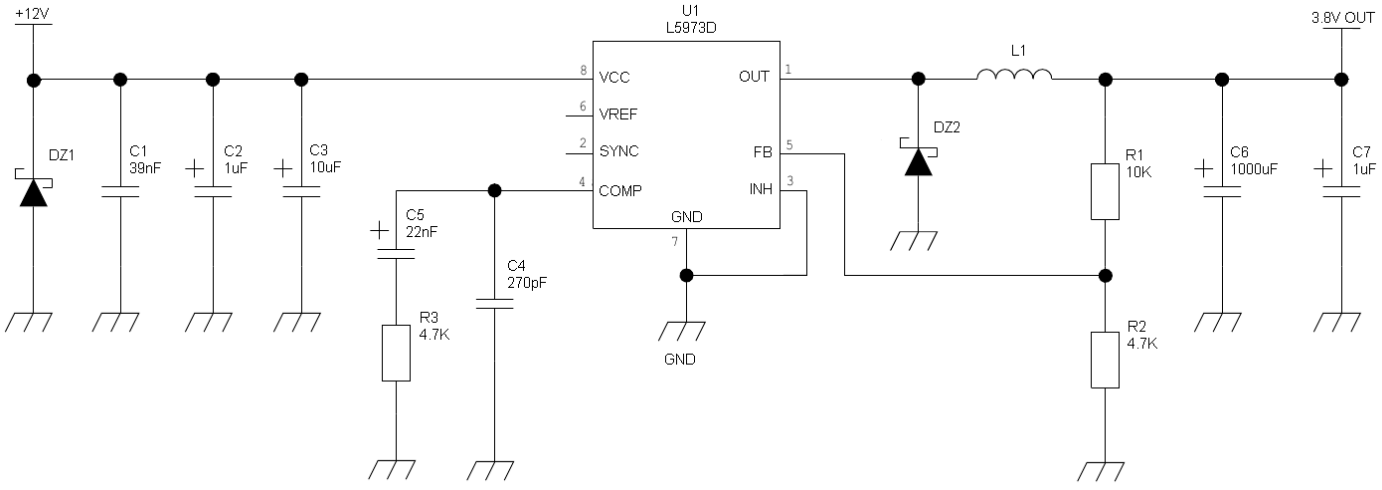
An example of linear regulator with 5V input is:



6.3.1.1. + 12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the UL865-N3G V2.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the UL865-N3G V2 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic:



6.3.1.1. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit UL865-N3G V2 module.

WARNING:

The three cells Ni/Cd or Ni/MH 3,6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for the UL865-N3G V2 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with UL865-N3G V2. Their use can lead to overvoltage on the UL865-N3G V2 and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UL865-N3G V2 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

6.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- Average current consumption during HSDPA transmission @PWR level max :

  600 mA

- *Average current during idle:*
  1.5 *mA*

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.
If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 600mA maximum RMS current, or even could be the simple chip package (no heat sink).
Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 600mA, being usually around 150mA.
For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.
For the heat generated by the UL865-N3G V2, you can consider it to be during transmission 1W max during CSD/VOICE calls.
This generated heat will be mostly conducted to the ground plane under the UL865-N3G V2; you must ensure that your application can dissipate it.

6.3.3. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit UL865-N3G V2 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the UL865-N3G V2 is wide enough to ensure a dropless connection even during the 2A current peaks.

- The protection diode must be placed close to the input connector where the power source is drained.

- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application doesn't have audio interface but only uses the data feature of the Telit UL865-N3G V2, then this noise is not so disturbing and power supply layout design can be more forgiving.

- The PCB traces to the UL865-N3G V2 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.

- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).

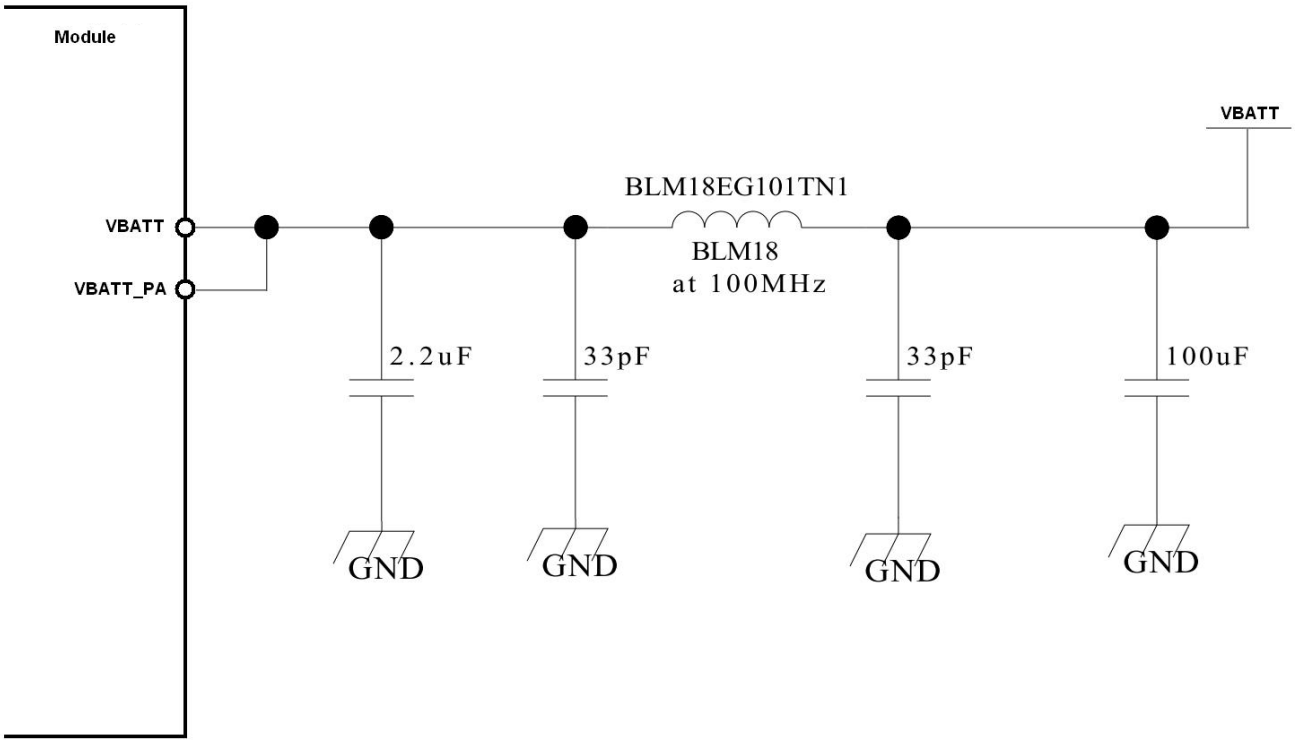
- The use of a good common ground plane is suggested.

- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.

- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.
  A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

  The below figure shows the recommended circuit:



7. Radio Section

7.5. TX Output Power

Band	Power Class
WCDMA FDD B2, B5	Class 3 (0.25W)

7.6. Sensitivity

Band	Typical	Note
WCDMA FDD B2	-110 dBm	BER <0.1%
WCDMA FDD B5	-111 dBm	BER <0.1%

7.7. Antenna Requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.
The antenna and antenna transmission line on PCB for a Telit UL865-N3G V2 device shall fulfill the following requirements:

UL865-N3G V2	
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth (WCDMA)	70 MHz in WCDMA Band V 140 MHz in WCDMA Band II
Impedance	50 ohm
Input power	> 24dBm Average power in WCDMA
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

7.7.1. UL865-N3G V2 Antenna – PCB line Guidelines

When using the Telit UL865-N3G V2 module, since there's no antenna connector on the module, the antenna must be connected to the UL865-N3G V2 through the PCB with the antenna pad (**pin 34**).

In the case that the antenna is not directly developed on the same PCB, hence directly connected at the antenna pad of the UL865-N3G V2, then a PCB line is needed in order to connect with it or with its connector.
This transmission line shall fulfill the following requirements:

ANTENNA LINE ON PCB REQUIREMENTS	
Impedance	50 ohm
Max Attenuation	0,3 dB
No coupling with other signals allowed	
Cold End (Ground Plane) of antenna shall be equipotential to the UL865-N3G V2 ground pins	

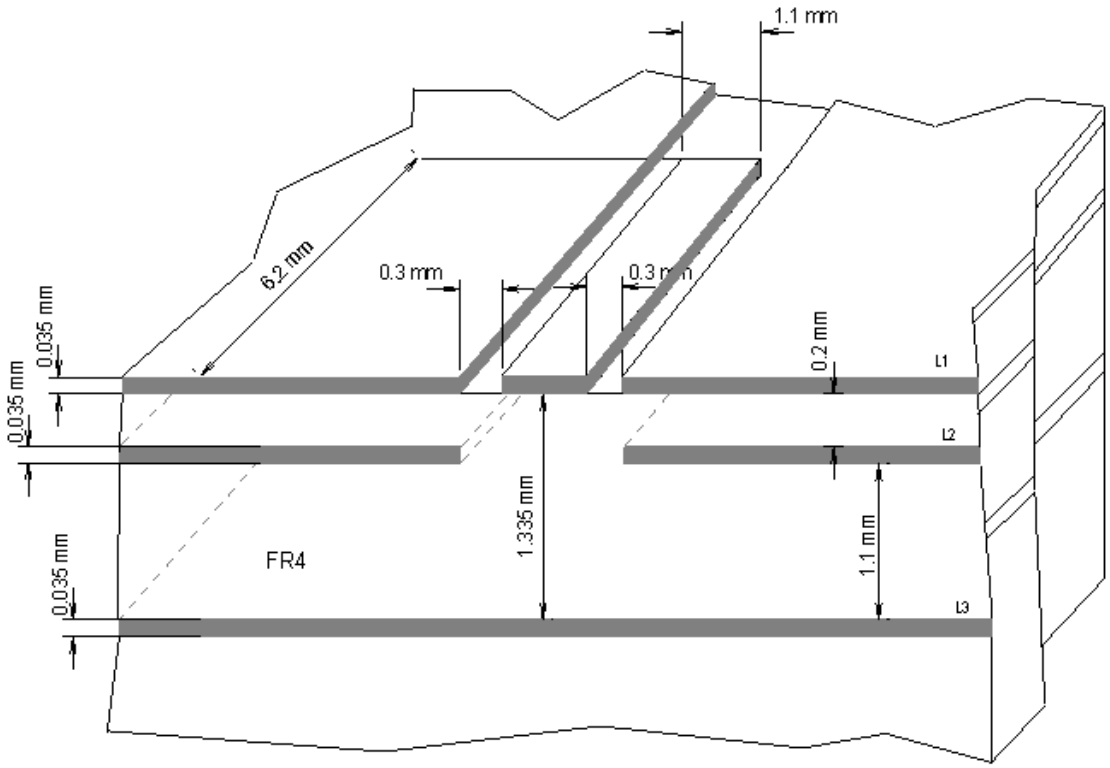
This transmission line should be designed according to the following guidelines:
Ensure that the antenna line impedance is 50 ohm;
Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
Keep, if possible, one layer of the PCB used only for the Ground plane;
Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
Place EM noisy devices as far as possible from UL865-N3G V2 antenna line;
Keep the antenna line far away from the UL865-N3G V2 power supply lines;
If you have EM noisy devices around the PCB hosting the UL865-N3G V2, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
If you don't have EM noisy devices around the PCB of UL865-N3G V2, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

7.8. PCB Guidelines in case of FCC certification

In the case FCC certification is required for an application using UL865-N3G V2, according to FCC KDB 996369 for modular approval requirements, the transmission line has to be similar to that implemented on UL865-N3G V2 interface board and described in the following chapter.

7.8.1. Transmission line design

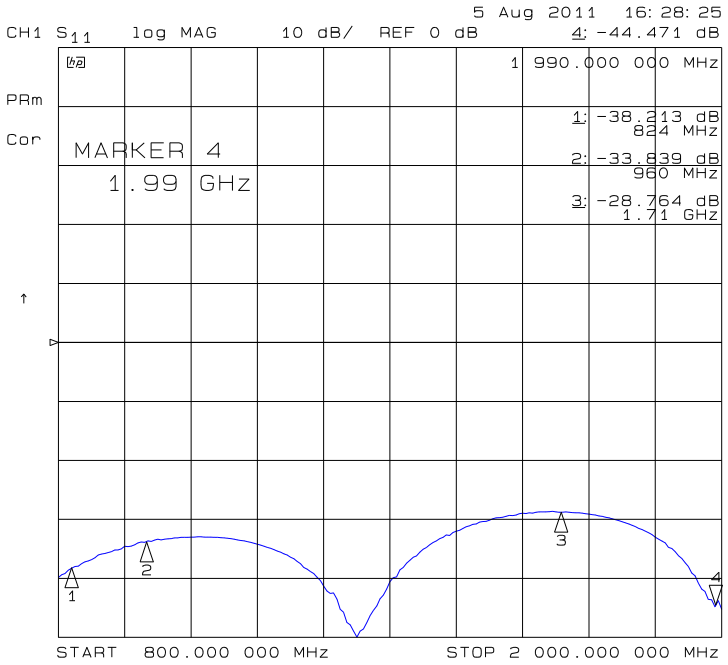
During the design of the UL865-N3G V2 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.
The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity $\varepsilon_r = 4.6 \pm 0.4$ @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



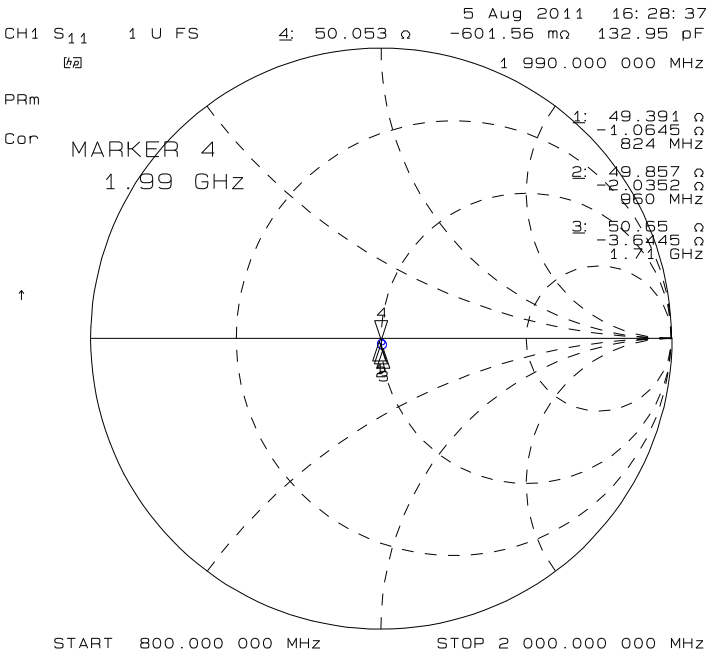
7.8.2. Transmission line measurements

HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

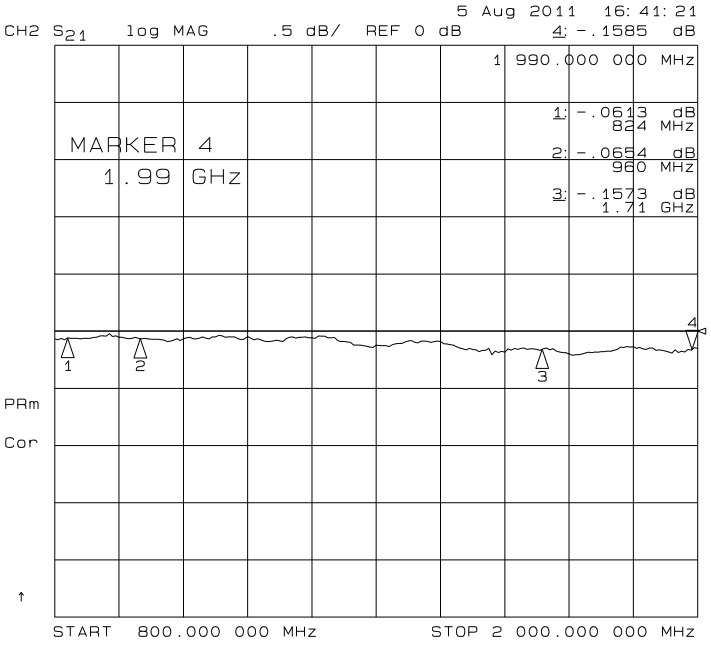
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



Insertion Loss of G-CPW line plus SMA connector is shown below:



7.9. Antenna - Installation Guidelines

Install the antenna in a place covered by the GSM / WCDMA signal.
If the device antenna is located farther than 20cm from the human body and there are no co-located transmitter then the Telit FCC/IC approvals can be re-used by the end product.
If the device antenna is located closer than 20cm from the human body or there are co-located transmitter then the additional FCC/IC testing may be required for the end product (Telit FCC/IC approvals cannot be reused).
Antenna shall not be installed inside metal cases.
Antenna shall be installed also according to antenna manufacturer instructions.

8. Logic level specifications

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels. The following table shows the logic level specifications used in the UL865-N3G V2 interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.1V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.5V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

Current characteristics

Level	Typical
Output Current	1mA
Input Current	1uA

8.5. Reset signal

Signal	Function	I/O	pin
RESET*	Phone reset	I	47

RESET* is used to reset the UL865-N3G V2. Whenever this signal is pulled low, the UL865-N3G V2 is reset. When the device is reset it stops any operation. After the release of the reset UL865-N3G V2 is unconditionally shut down, without doing any detach operation from the network where it is registered. This behavior is not a proper shut down because any GSM device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.

The RESET* is internally controlled on start-up to achieve a proper power-on reset sequence, so there's no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.

NOTE:

Do not use this signal to power OFF the UL865-N3G V2. Use the ON/OFF procedure to perform this function.

Reset Signal Operating levels:

Signal	Min	Max
RESET* Input high	1.5V(NOTE1)	1.9V
RESET* Input low	0V	0.35V

(NOTE1) this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it must always be connected with an open collector transistor, to permit to the internal circuitry the power on reset and under voltage lockout functions.

9. USB Port

The UL865-N3G V2 includes one integrated universal serial bus (USB) transceiver.

9.1. USB 2.0 HS

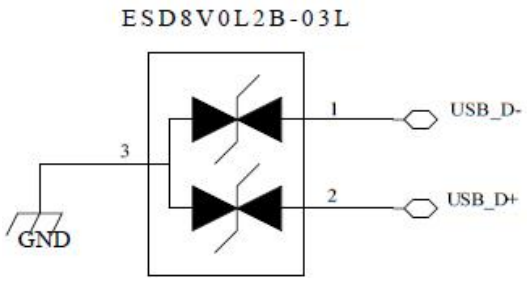
This port is compliant with the USB 2.0 HS only.
The following table is listing the available signals:

PAD	Signal	I/O	Function	Type	NOTE
18	USB_D+	I/O	USB differential Data (+)	3.3V	
17	USB_D-	I/O	USB differential Data (-)	3.3V	
6	VUSB	AI	Power sense for the internal USB transceiver.	5V	Accepted range: 4.4V to 5.25V

The USB_DPLUS and USB_DMINUS signals have a clock rate of 480 MHz.

The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The characteristic impedance value should be as close as possible to 90 Ohms differential.

In case there is a need to add an ESD protection the suggested connection is the following:



NOTE:

VUSB pin should be disconnected before activating the Power Saving Mode.

The USB FS mode could be used to provide AT Commands / Data communication but not for a SW upgrade.

The USB FS mode is supported only when the module is fully operative.

10. SPI Port

The UL865-N3G V2 Module is provided by one SPI interface.
The SPI interface defines two handshake lines for flow control and mutual wake-up of the modem and the Application Processor: SRDY (slave ready) and MRDY (master ready).
The AP has the master role, that is, it supplies the clock.

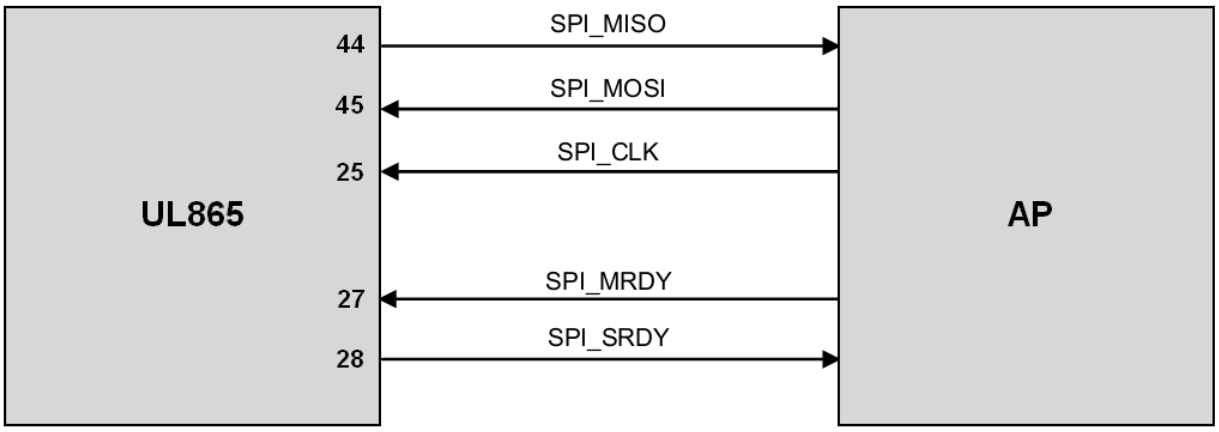
The following table is listing the available signals:

PAD	Signal	I/O	Function	Type	Comment
44	SPI_MISO	O	SPI_MISO	CMOS 1.8V	Shared with RX_AUX
45	SPI_MOSI	I	SPI_MOSI	CMOS 1.8V	
28	SPI_SRDY	I/O	SPI_SRDY	CMOS 1.8V	Shared with GPIO_06 / ALARM /
27	SPI_MRDY	I/O	SPI_MRDY	CMOS 1.8V	Shared with GPIO_07 / BUZZER /
25	SPI_CLK	I/O	SPI_CLK	CMOS 1.8V	CMOS 1.8V

NOTE:

Due to the shared functions, when the SPI port is used, it is not possible to use the Auxiliary UART, GPIO_06, GPIO_07 and related alternate functions.

10.5. SPI Connections



11. Serial Ports

The serial port on the UL865-N3G V2 is the core of the interface between the module and OEM hardware.
2 serial ports are available on the module:

- MODEM SERIAL PORT 1 (Main, ASC0)
- MODEM SERIAL PORT 2 (Auxiliary, ASC1)

11.1. MODEM SERIAL PORT 1

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 3V or other voltages different from 1.8V
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that doesn't need a level translation is the 1.8V UART.
The serial port on the UL865-N3G V2 is a +1.8V UART with all the 8 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for the UL865-N3G V2 UART are the CMOS levels:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pad when on	-0.3V	+2.1V

Operating Range - Interface levels (1.8V CMOS)

Level		Min	Max
Input high level	V_{IH}	1.5V	1.9V
Input low level	V_{IL}	0V	0.35V
Output high level	V_{OH}	1.6V	1.9V
Output low level	V_{OL}	0V	0.2V

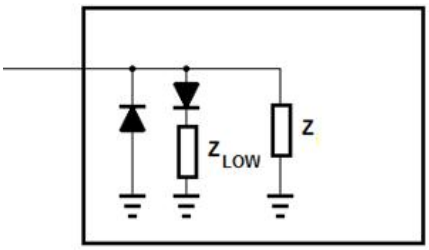
The signals of the UL865-N3G V2 serial port are:

RS232 Pin Number	Signal	UL865-N3G V2 Pad Number	Name	Usage
1	DCD - dcd_uart	1	Data Carrier Detect	Output from the UL865-N3G V2 that indicates the carrier presence
2	RXD - tx_uart	8	Transmit line *see Note	Output transmit line of UL865-N3G V2 UART
3	TXD - rx_uart	7	Receive line *see Note	Input receive of the UL865-N3G V2 UART
4	DTR - dtr_uart	4	Data Terminal Ready	Input to the UL865-N3G V2 that controls the DTE READY condition
5	GND	32, 33, 35, 36, 46	Ground	Ground
6	DSR - dsr_uart	3	Data Set Ready	Output from the UL865-N3G V2 that indicates the module is ready
7	RTS -rts_uart	5	Request to Send	Input to the UL865-N3G V2 that controls the Hardware flow control
8	CTS - cts_uart	6	Clear to Send	Output from the UL865-N3G V2 that controls the Hardware flow control
9	RI - ri_uart	2	Ring Indicator	Output from the UL865-N3G V2 that indicates the incoming call condition

The following table shows the typical input value of internal pull-up resistors for RTS DTR and TXD input lines and in all module states:

STATE	RTS DTR TXD	
		Pull up tied to
ON	5K to 12K	1V8
OFF	Schottky diode	
RESET	Schottky diode	
POWER SAVING	5K to 12K	1V8

The input line ON_OFF and RESET state can be treated as in picture below



NOTE:

According to V.24, RX/TX signal names are referred to the application side, therefore on the UL865-N3G V2 side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the UL865-N3G V2 serial port and vice versa for RX.

NOTE:

For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UL865-N3G V2 when the module is powered off or during an ON/OFF transition.

11.2. MODEM SERIAL PORT 2

The secondary serial port on the UL865-N3G V2 is a CMOS1.8V with only the RX and TX signals. The signals of the UL865-N3G V2 serial port are:

PAD	Signal	I/O	Function	Type	Comment
44	RXD_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 1.8V	Shared with SPI_MISO
45	TXD_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	Shared with SPI_MOSI

NOTE:

Due to the shared functions, when the SPI port is used, it is not possible to use the SPI port.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UL865-N3G V2 when the module is powered off or during an ON_OFF transition.

11.3. RS232 level translation

In order to interface the UL865-N3G V2 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

invert the electrical signal in both directions;

change the level from 0/1.8V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

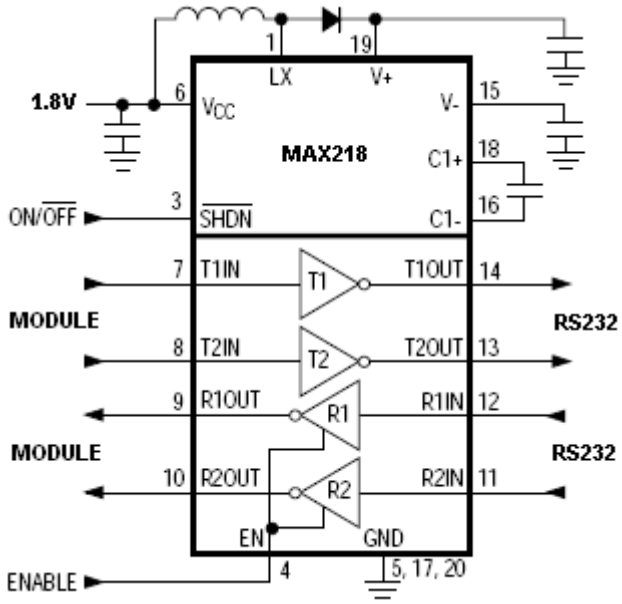
- 5 drivers
- 3 receivers

NOTE:

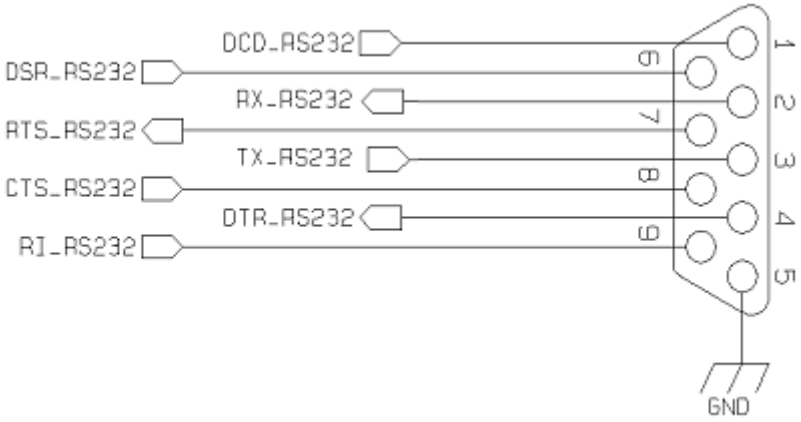
The digital input lines working at 1.8V CMOS have an absolute maximum input voltage of 2.1V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead, it must be powered from a +1.8V (dedicated) power supply.

An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218).

In this case the chipset is capable to translate directly from 0/1.8V to the RS232 levels (Example done on 4 signals only).



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



12. Audio Section Overview

The Base Band Chip of the UL865-N3G V2 provides one Digital Audio Interface.
Please refer to the UL865-N3G V2 DVI Application Note for additional details on this function.

13. General Purpose I/O

The general purpose I/O pads can be configured to act in three different ways:

- input
- output
- alternate function (*internally controlled*)

Input pads can be read; they report the digital value (*high or low*) present on the pad at the read time.
Output pads can only be written or queried and set the value of the pad output.
An *alternate function pad* is internally controlled by the UL865-N3G V2 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the UL865-N3G V2 and their state.

Pin	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
42	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function DVI_WA0
41	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function JDR and DVI_RX
40	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function DVI_TX
39	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function TX Disable and DVI_CLK
29	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	
28	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function /SPI_SRDY
27	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function /SPI_MRDY
26	GPIO_08	I/O	Configurable GPIO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function STAT_LED

NOTE:

The internal GPIO's pull up/pull down could be set to the preferred status for the application using the AT#GPIO command.

Please refer for the AT Commands User Guide for the detailed command Syntax.

WARNING:

During power up the GPIOs may be subject to transient glitches.

Also the UART‘s control flow pins can be usable as GPI/O.

Pin	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
1	GPO_A	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C109/DCD
2	GPO_B	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C125/RING
3	GPO_C	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C107/DSR
4	GPI_E	I	Configurable GPI	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C108/DTR
5	GPI_F	I	Configurable GPI	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C105/RTS
6	GPO_D	O	Configurable GPO	CMOS 1.8V	1uA/1mA	INPUT	0	0	Alternate function C106/CTS

13.1. GPIO Logic levels

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.
The following table shows the logic level specifications used in the UL865-N3G V2 interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.1V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.5V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

Current characteristics

Level	Typical
Output Current	1mA
Input Current	1uA

13.2. Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.
If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UL865-N3G V2 when the module is powered OFF or during an ON/OFF transition.

TIP:

The V_AUX / PWRMON pin can be used for input pull up reference or/and for ON monitoring.

13.3. Using a GPIO Pad as OUTPUT

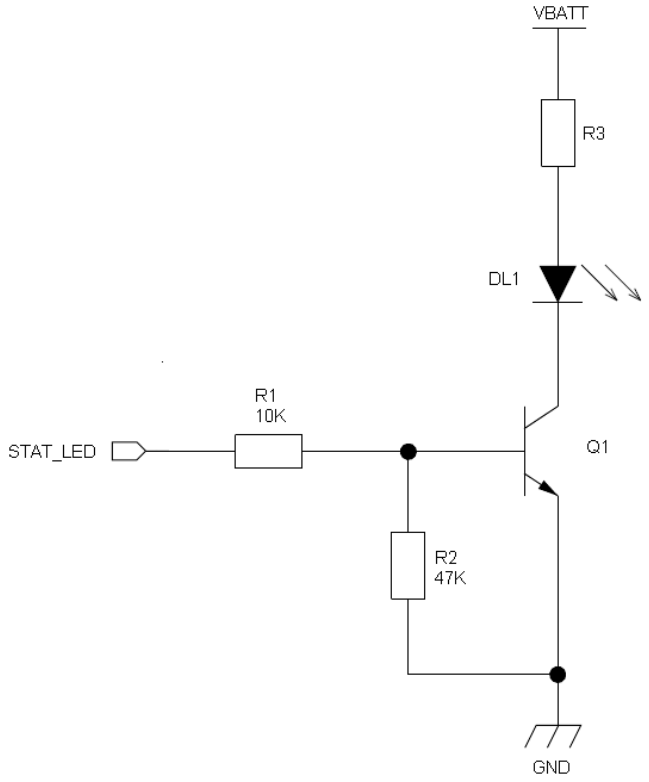
The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

13.4. Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status. The function is available as alternate function of GPIO_08 (to be enabled using the AT#GPIO=8,0,2 command).
In the UL865-N3G V2 modules, the STAT_LED needs an external transistor to drive an external LED.
Therefore, the status indicated in the following table is reversed with respect to the pin status.

Device Status	LED status
Device off	Permanently off
Not Registered	Permanently on
Registered in idle	Blinking 1sec on + 2 sec off
Registered in idle + power saving	It depends on the event that triggers the wakeup (In sync with network paging)
Voice Call Active	Permanently on
Dial-Up	Blinking 1 sec on + 2 sec off

A schematic example could be:



13.5.

13.5. SIMIN detect function

All the GPIO pins can be used as SIM DETECT input. The AT Command used to enable the function is:

AT#SIMINCFG

Use the AT command **AT#SIMDET=2** to enable the SIMIN detection
Use the AT command **AT&W0** and **AT&P0** to store the SIMIN detection **in the common profile.**

For full details see AT Commands Reference Guide, 80000ST10025a.

NOTE:

Don't use the SIM IN function on the same pin where the GPIO function is enabled and vice versa!

13.6. RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off. To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

In order to keep the RTC active when VBATT is not supplied it is possible to back up the RTC section connecting a **backup circuit** to the related VRTC signal (pad 30 on module's Pinout).

For additional details on the Backup solutions please refer to the related application note (RTC Backup Application Note)

13.7. SIM Holder Implementation

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

14. DAC and ADC section

14.1. DAC Converter

14.1.1. Description

The UL865-N3G V2 provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin **15** of the UL865-N3G V2.
The on board DAC is a 10 bit converter, able to generate an analogue value based on a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

	Min	Max	Units
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = (2 *value) / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

14.1.2. Enabling DAC

An *AT command* is available to use the DAC function.
The command is: **AT#DAC= [**<*enable*> **[,** <*value*>**]]**

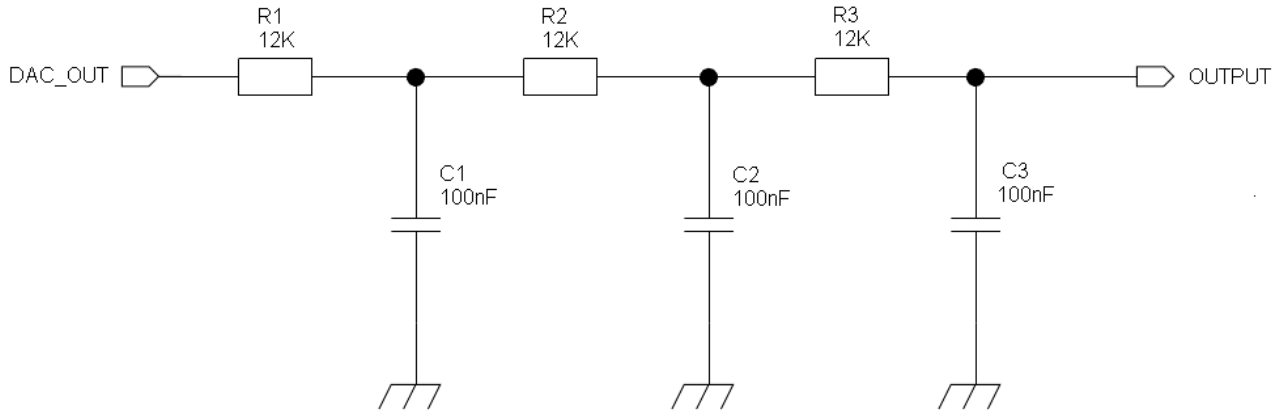
<value> - scale factor of the integrated output voltage (0..1023 - 10 bit precision)
it must be present if ***<enable>=1***

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

14.1.3. Low Pass Filter Example



14.2. ADC Converter

14.2.1. Description

The UL865-N3G V2 is provided by two A/D converters. They are able to read a voltage level in the range of 0÷1.2 volts applied on the ADC pin input, store and convert it into 10 bit word. The following table is showing the ADC characteristics:

	Min	Typical	Max	Units
Input Voltage range	0	-	1.2	Volt
AD conversion	-	-	10	bits
Input Resistance	1	-	-	Mohm
Input Capacitance	-	1	-	pF

The signal is available on the following pads:

PAD	Name	I/O	Description	Notes
13	ADC_IN1	AI	Analog/Digital converter input	Accepted values 0 to 1.2V DC
14	ADC_IN2	AI	Analog/Digital converter input	Accepted values 0 to 1.2V DC

14.2.2. Using ADC Converter

An AT command is available to use the ADC function.

The command is ***AT#ADC=1,2***

The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

14.3. VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. The signal is present on Pad 43 and it is in common with the PWRMON (module powered ON indication) function.
This output is always active when the module is powered ON.

The operating range characteristics of the supply are:

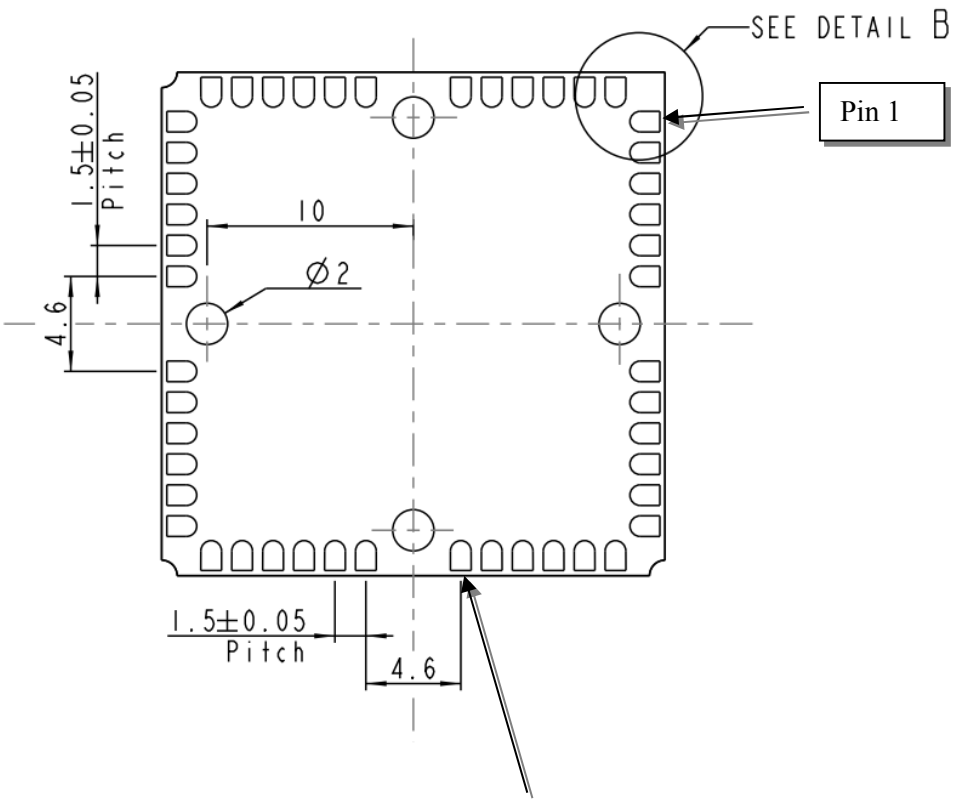
Level	Min	Typical	Max
Output voltage	1.78V	1.80V	1.82V
Output current	-	-	60mA
Output bypass capacitor (inside the module)		1uF	

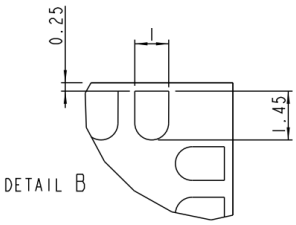
15. Mounting the UL865-N3G V2 on your Board

15.1. General

The UL865-N3G V2 modules have been designed to be compliant with a standard lead-free SMT process.

15.2. Module finishing & dimensions



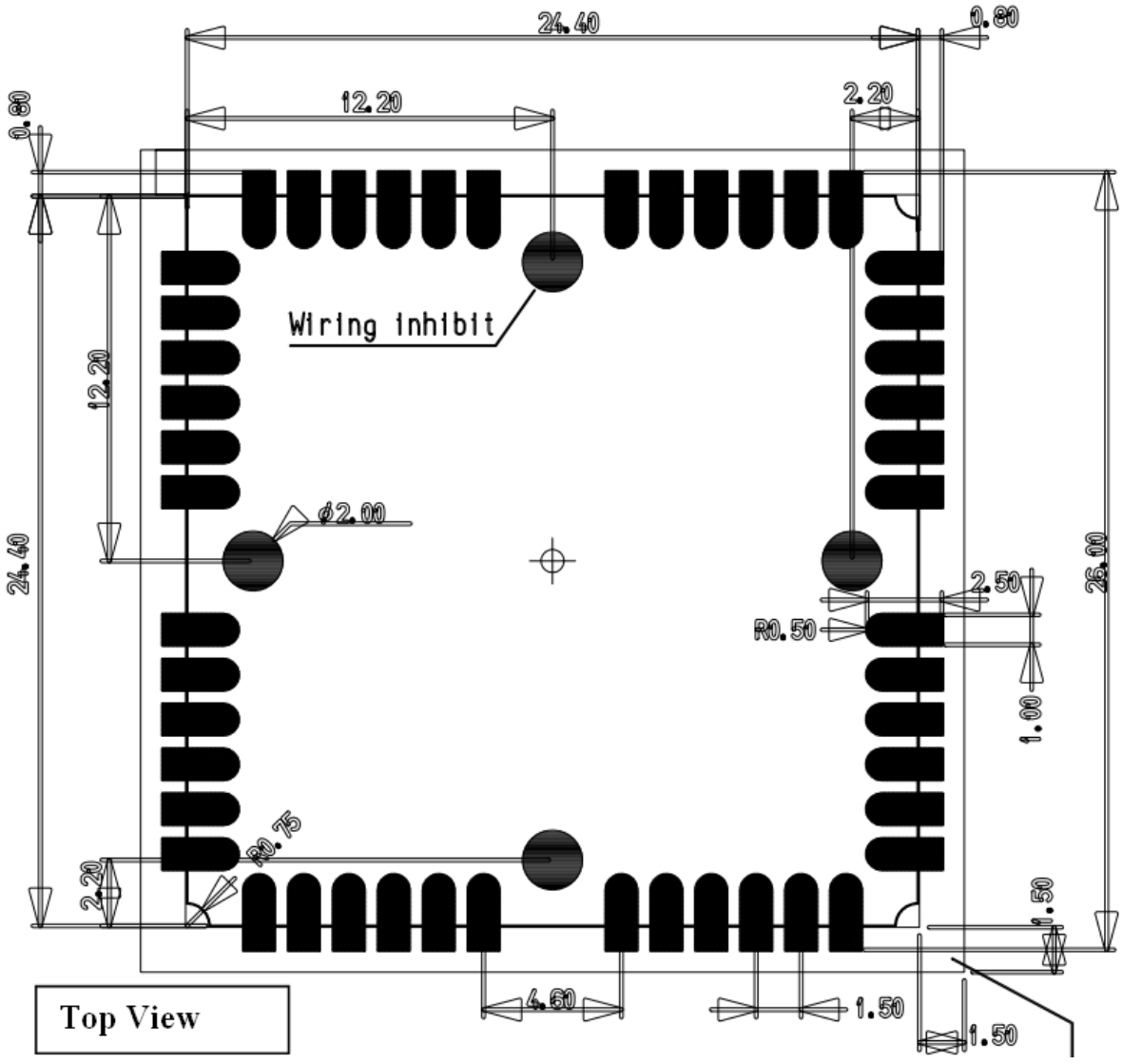


Lead-free Alloy:
Surface finishing Ni/Au for all solder pads

Bottom View

Dimensions in mm

15.3. Recommended foot print for the application



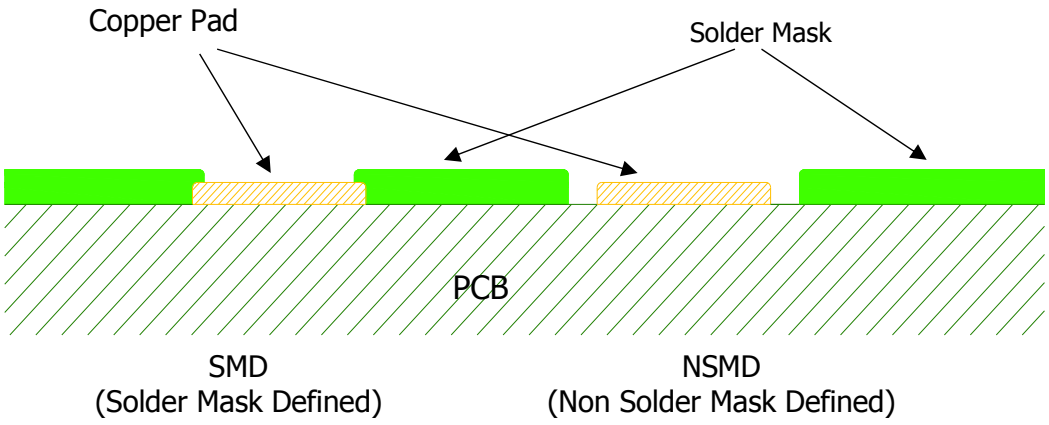
In order to easily rework the UL865-N3G V2 is suggested to consider on the application a 1.5 mm placement inhibited area around the module.
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

15.4. Stencil

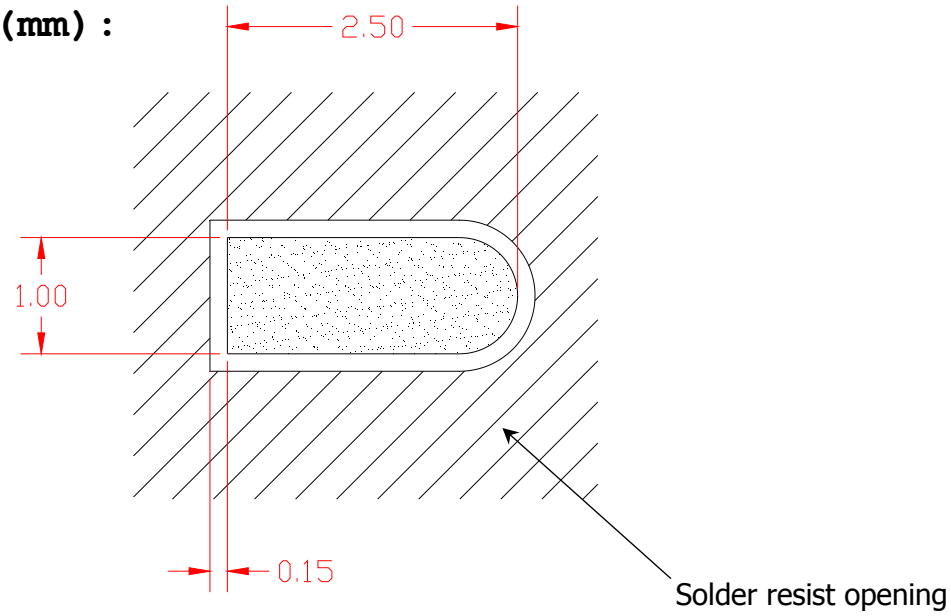
Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120µm.

15.5. PCB pad design

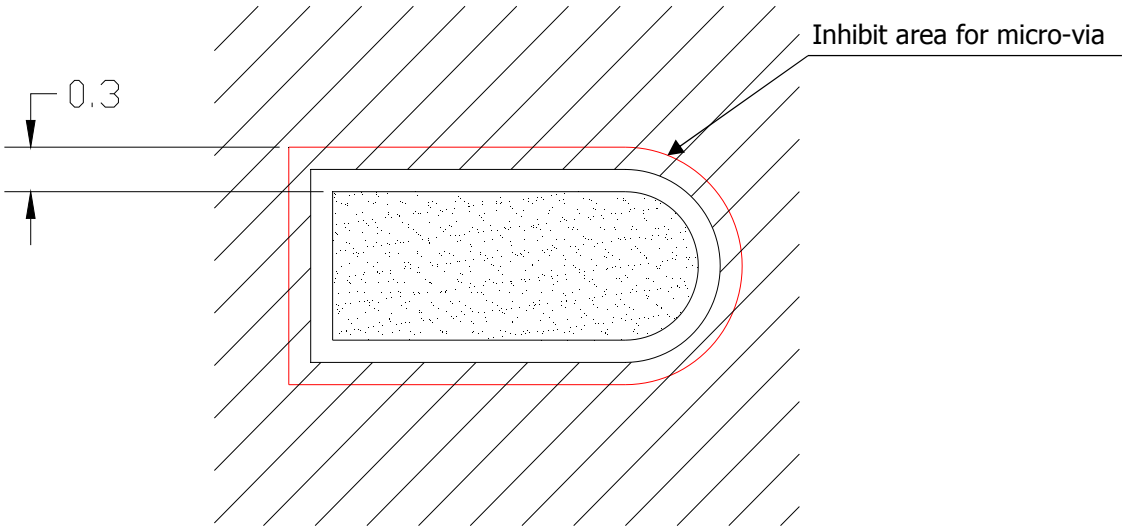
Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



15.6. Recommendations for PCB pad dimensions (mm):



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

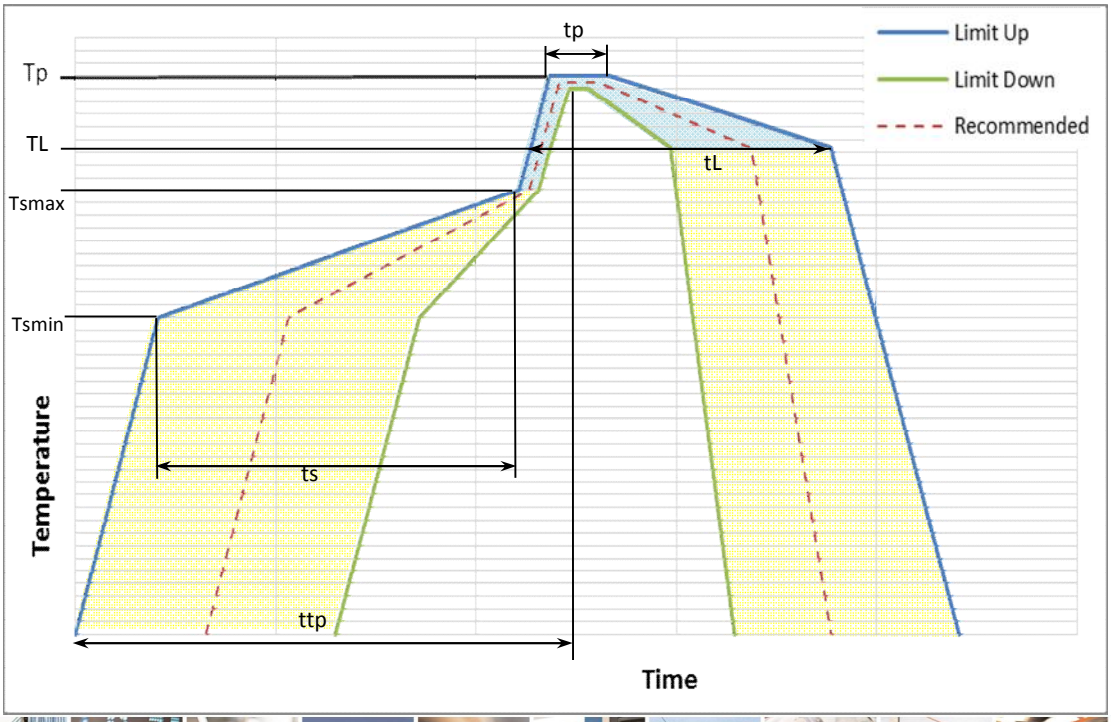
15.7. Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

15.8. UL865-N3G V2 Solder reflow

Recommended solder reflow profile



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	 3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature (ttp)	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

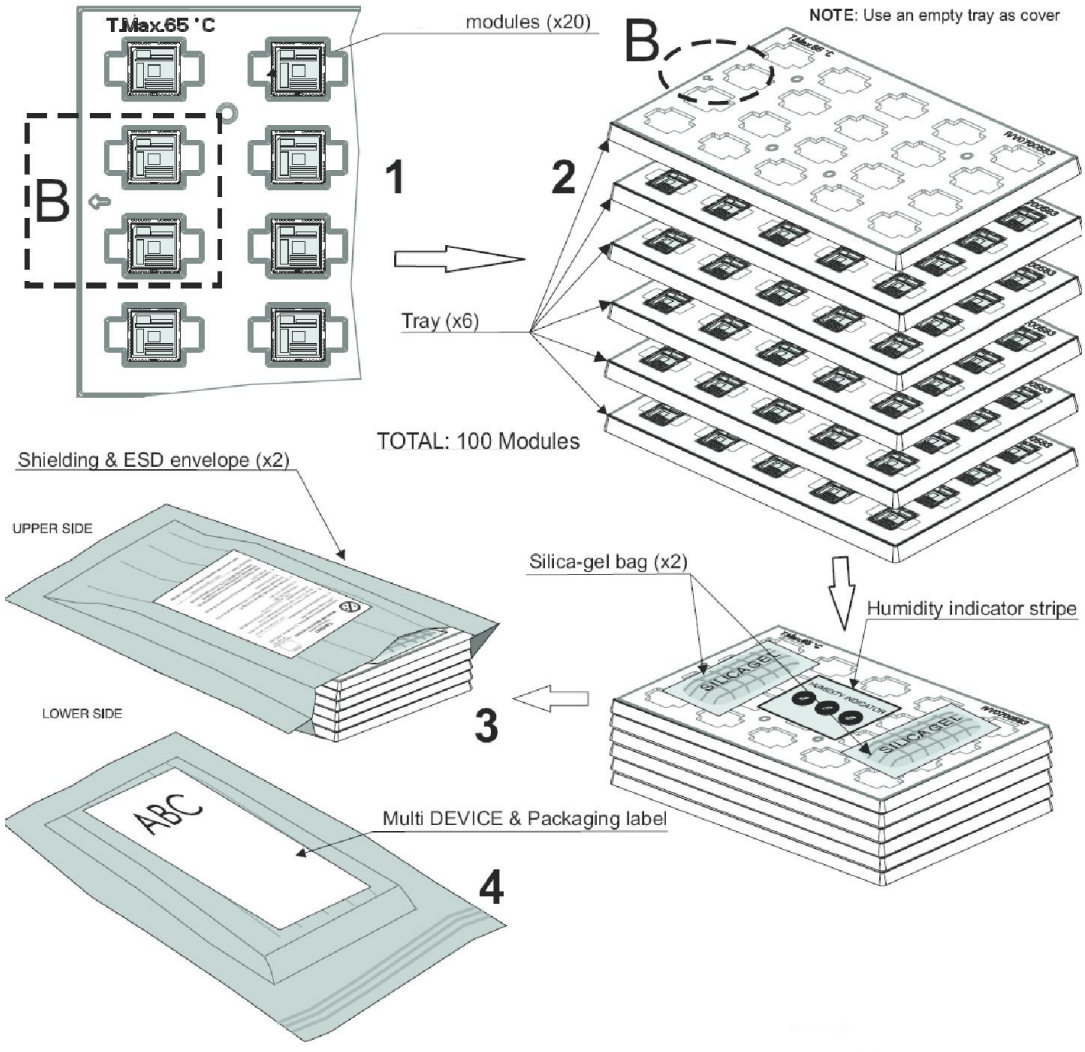
WARNING:

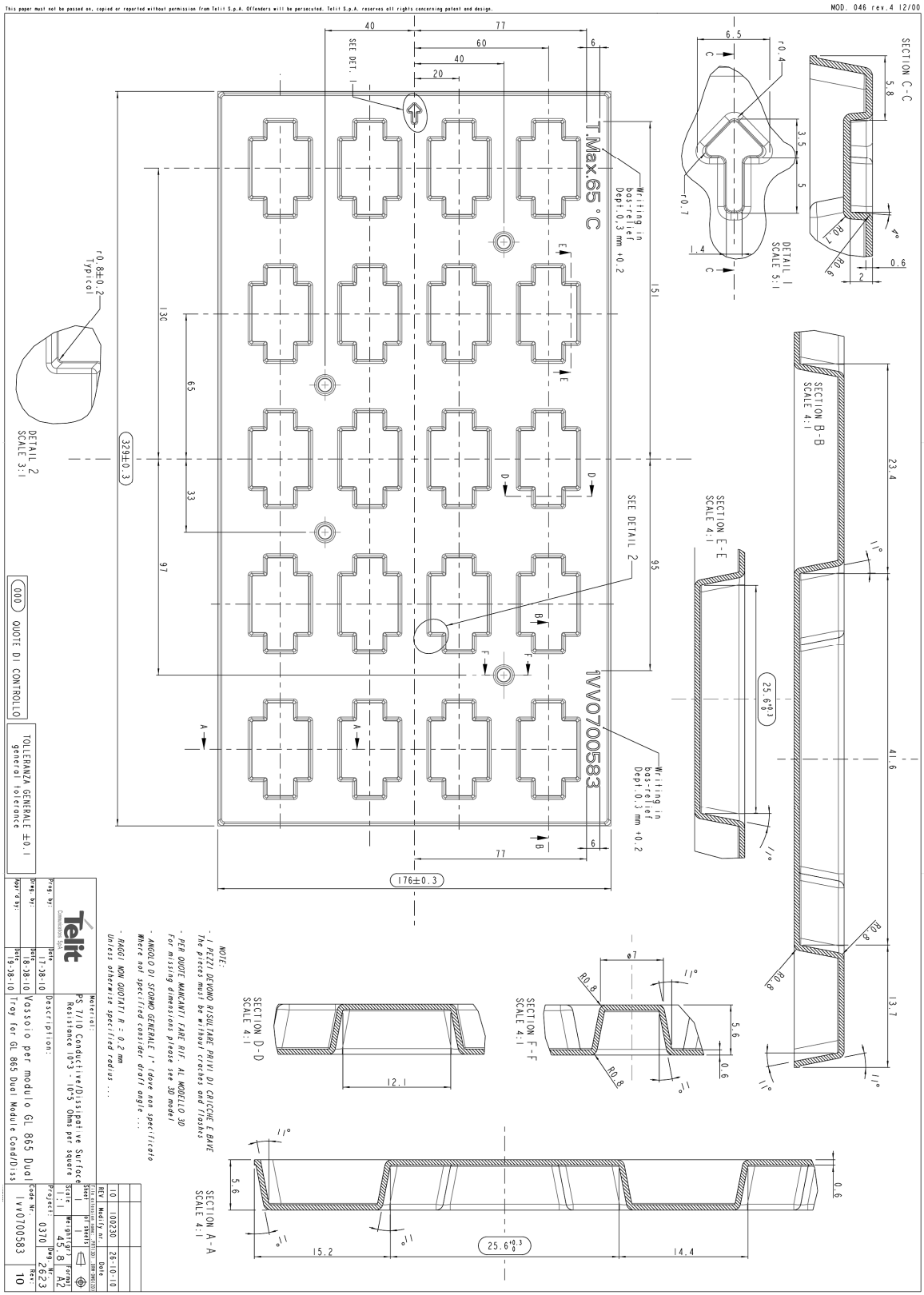
The UL865-N3G V2 module withstands one reflow process only.

16. Packing system

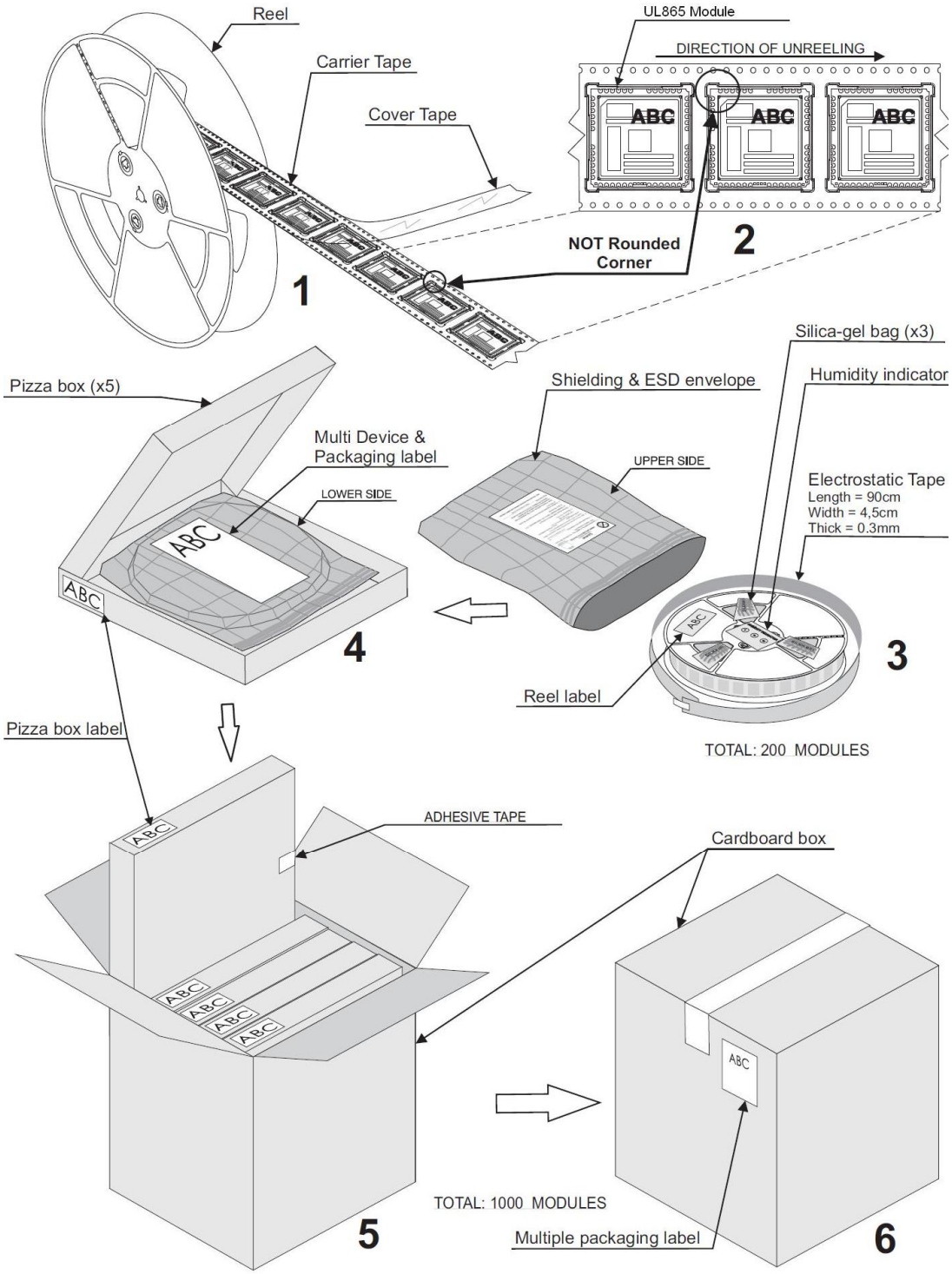
16.1. Packing on tray

The UL865-N3G V2 modules are packaged on trays of ***20*** pieces each. These trays can be used in SMT processes for pick & place handling.





16.2. Packing in Reel



16.3. Moisture sensitivity

The moisture sensitivity level of the Product is “3” according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.
b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph 5.2” is respected.
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

17. SAFETY RECOMMANDATIONS

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:
Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
Where there is risk of explosion such as gasoline stations, oil refineries, etc
It is responsibility of the user to enforce the country regulation and the specific environment regulation.
Do not disassemble the product; any mark of tampering will compromise the warranty validity.
We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.
The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.
The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security.
Should there be any doubt, please refer to the technical documentation and the regulations in force.
Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.
The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information's are available on the European Community website:
http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm
The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:
http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm

18. FCC/IC REGULATORY NOTICES

Modification statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature.
Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This equipment complies with FCC and IC radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. Antenna gain must be below:

Frequency Band	**Gain**
Band II (1900 MHz)	9.01 dBi
Band V (850 MHz)	7.76 dBd

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet appareil est conforme aux limites d'exposition aux rayonnements de la IC pour un environnement non contrôlé. L'antenne doit être installé de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. Gain de l'antenne doit être ci-dessous:

Bande de fréquence	**Gain**
Band II (1 900 MHz)	9.01 dBi
Band V (850 MHz)	7.76 dBd

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autreémetteur.

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna
Increase the separation between the equipment and receiver.
Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
Consult the dealer or an experienced radio/TV technician for help.

Labelling Requirements for the Host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains FCC ID: RI7UL865N3G
Contains IC: 5131A- UL865N3G

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le FCC ID et le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme suit :

Contains FCC ID: RI7UL865N3G
Contains IC: 5131A- UL865N3G

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.