
Technical Manual

**Operation, Maintenance, Installation Instructions
and Illustrated Parts Breakdown**

HF/VHF/UHF DSP RECEIVER RX-400

**TEN-TEC, INC.
1185 DOLLY PARTON PARKWAY
SEVIERVILLE, TN 37862**

WARNING

HIGH VOLTAGE

is used in the operation of this equipment.

DEATH ON CONTACT

may result if personnel fail to observe safety precautions.

Learn the areas containing high voltage within the equipment.

Be careful not to contact high voltage connections when installing, operating or maintaining this equipment.

Before working inside the equipment, turn power and ground points of high potential OFF before touching them.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

1. Reorient or relocate the receiving antenna.
2. Increase the separation between the equipment and receiver.
3. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
4. Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by Ten-Tec, Inc. could void the user's authority to operate the equipment.

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RX400 DSP RECEIVER

This manual provides operation and maintenance instructions for the RX-400 HF/VHF/UHF DSP Receiver. The manual was prepared in accordance with MIL-HDBK-1221, "Department of Defense Handbook for Evaluation of Commercial Off-The-Shelf (COTS) Manuals."

Introduction

The RX-400 HF/VHF/UHF receiver couples a rugged wide-band RF front end to a high-performance Digital Signal Processing back end. Multiple detection modes, simplified programming interface and streaming audio make the RX-400 a very flexible platform.

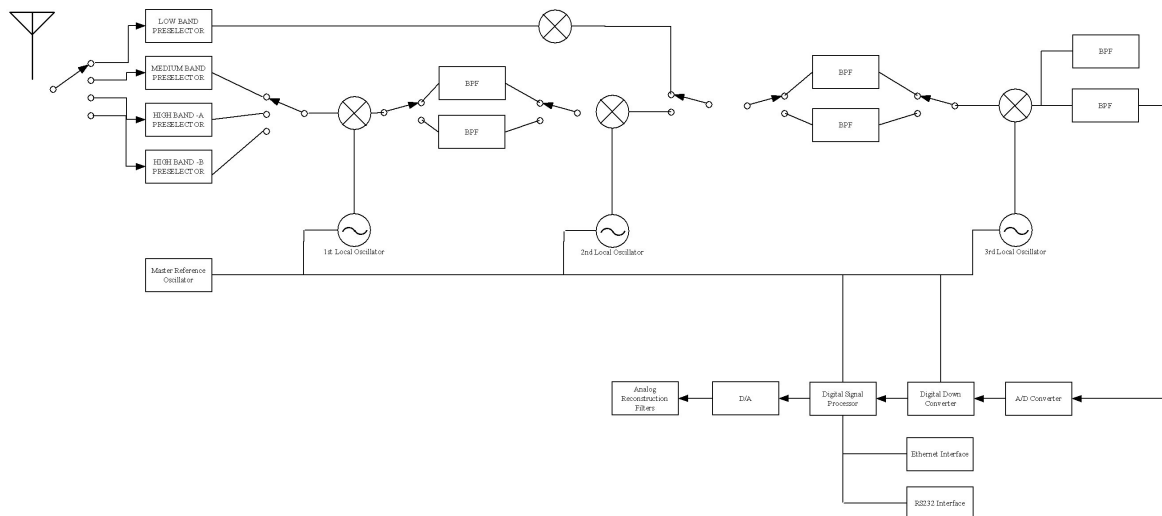


Figure 1 Block Diagram

RF signal path:

The RX-400 contains separate HF and VHF/UHF front ends. The HF section covers the 2-88 MHz range. The range between 88 MHz and 3 GHz is covered by the other. A single antenna connector is used to feed RF signals to the receiver. All signals are routed first to the VHF/UHF preselector at which point they are routed to the HF preselector if the tuned frequency is below 88 MHz. In most cases the internal routing of received signals is automatic and there are no user selectable features that affect the front-end operation. The exception is the HF section, which contains a user-activated RF attenuator. In addition, the IF output bandwidth may be set to 2 MHz or 6 MHz when the tuned frequency is above 20 MHz. Below 20 MHz the IF output bandwidth is fixed at 2 MHz. When the tuned frequency

HF Operation:

Signals entering the HF front-end will pass through a user-activated RF attenuator followed by 1 of 8 band-pass filters. Each filter is designed to eliminate potential interference from other undesired signals. The RF attenuator may be used to reduce interference from undesired signals that may overload the receiver hardware.

VHF/UHF operation:

For operation above 88 MHz the received signals are routed to the VHF/UHF preselector which covers 88 MHz through 3 GHz (USA versions will not provide access to cellular frequencies except for government authorized users).

IF Output:

A 21.4 MHz wideband IF output is provided with selectable 6 MHz or 2 MHz bandwidth. Below 20 MHz the bandwidth is fixed at 2 MHz.

Control Interface:

The RX-400 contains two command and control ports, a standard RS-232 serial interface and an Ethernet IP interface. Both interfaces support the same command set with the exception of those features that relate to Streaming Audio. Streaming Audio can be tuned on and off via the RS-232 interface, the Streaming Audio data is delivered only on the Ethernet interface.

Firmware Updates:

RX-400 Receiver operation, control and demodulation are contained in internal firmware which can be updated in the field. See the RX400 [UPDATE INSTRUCTIONS](#) document for details.

2. General Information

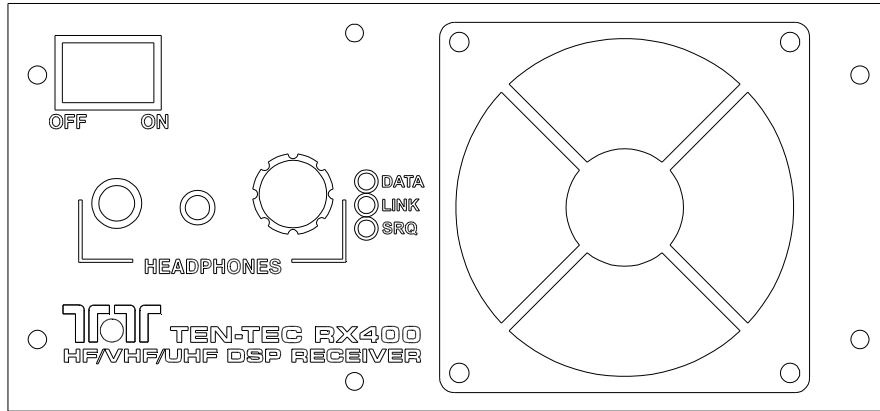


Figure 3 Front Panel Connections

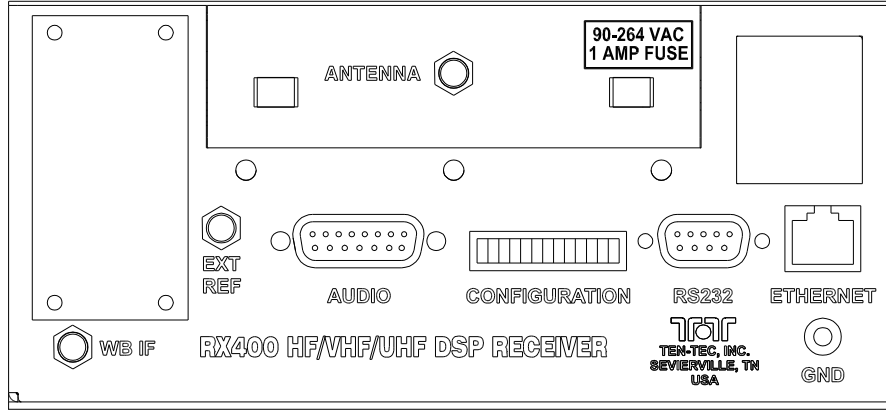


Figure 4 - Rear Panel Connections

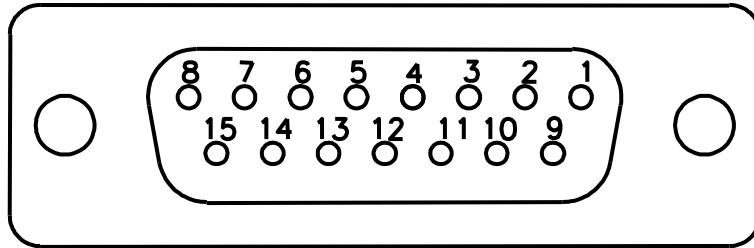


Figure 5 - Audio Connections

Pin	Description	
1	Chassis Ground	
2	A/C Coupled Mono Audio	Unbalanced +10dBm output.
3	Line B-	600 Ohm balanced output. 0 dBm nominal
4	Line B center tap	
5	Line B+	
6	Line A-	600 Ohm balanced output. 0 dBm nominal
7	Line A center tap	
8	Line A+	
9	Chassis Ground	
10	DC Coupled Mono Audio	Unbalanced +10dBm output.
11	No Connection	
12	User Programmable Output #1 (not available when frequency extender attached)	Low = 0 volts, High = 3.3v
13	User Programmable Output #2 (not available when frequency extender attached)	Low = 0 volts, High = 3.3v
14	User Programmable Output #3 (not available when frequency extender attached)	Low = 0 volts, High = 3.3v
15	User Programmable Output #4 (not available when frequency extender attached)	Low = 0 volts, High = 3.3v

3. General Theory of Operation

OVERVIEW

The Ten-Tec model RX400 is a narrowband DSP-based receiver with a wide-band IF output available at 21.4MHz. The superhetrodyne architecture is triple-conversion to the IF output for received frequencies of 88 MHz to 3GHz, and double conversion when tuned below 88 MHz. The IF output bandwidth is 6 MHz for tuned frequencies of 20 MHz to 3 GHz, and 2 MHz when tuned below 20 MHz receive frequency. Tuning step size is 10 kHz (1 kHz optional) at the 21.4 MHz IF output. Conversion gain from antenna to IF output is 3 dB nominal. The [GAIN BLOCK](#) diagram outlines the signal path and gain distribution throughout the RX-400 architecture.

The 21.4 MHz 3rd IF is bandpass filtered to 300 kHz bandwidth in the 3RD CONVERTER module, AGC leveled, and presented to the DSP board. On the DSP board, a high-speed A/D converter drives an AD6620 Digital Down Converter which applies fine tuning, further bandpass filtering, and decimation to the digitized IF signal to prepare the data for a Digital Signal Processor. Final selectivity filtering and mode-specific detection functions are accomplished by the DSP.

Audio/Video outputs are available via connectors on either rear or front panel. The outputs are designed for a nominal 600-ohm load.

Tuned center frequency, selectivity bandwidth, mode selection, and all other receiver parameter setting is by computer control via rear panel RS232 or Ethernet interface. Only power ON/OFF and Headphone Level controls are user-accessible on the front panel.

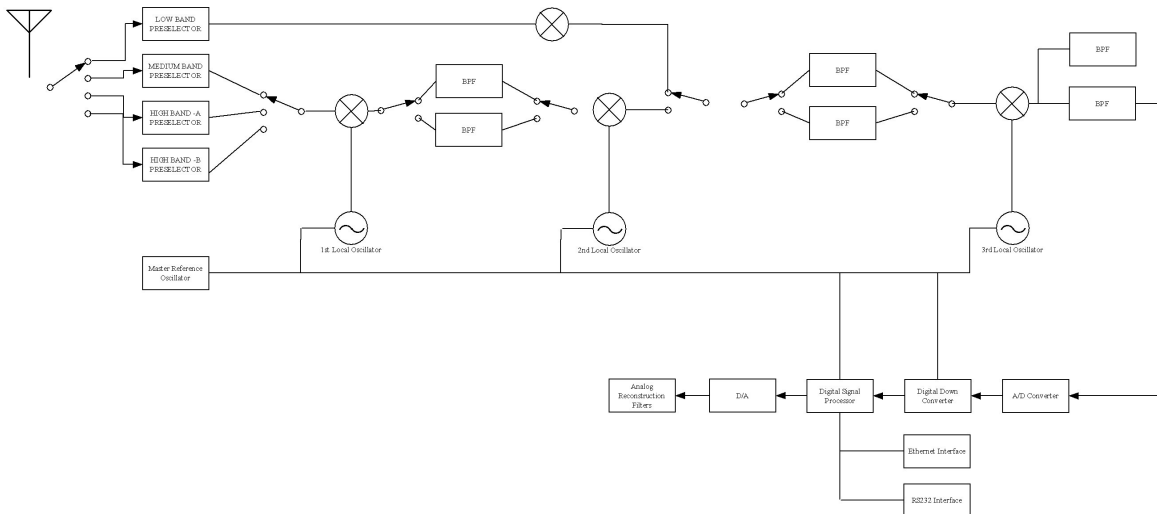


Figure 6 – Block Diagram

MECHANICAL CONFIGURATION

Six modules located on the bottom chassis deck accomplish the analog frequency conversion functions. These interconnected modules are the FIRST, SECOND, and THIRD CONVERTERS and the FIRST, SECOND, and THIRD LOCAL OSCILLATORS. Signal interconnection between modules is by miniature semi-rigid coax.

Two interconnected PRESELECTOR BOARDS located on the top foldout chassis deck perform frequency band preselection and signal pre-amplification between the antenna input and the FIRST CONVERTER module.

The DSP BOARD located on the inner chassis deck performs all digital signal conditioning, detection algorithms, and logic control functions. The DSP BOARD also contains the audio/video output amplifiers and the TCXO master frequency reference. Distribution of control signals and power to the various radio modules and boards is via connectorized ribbon cable between the DSP BOARD and the target board/module.

All DC power is supplied by a shielded universal AC input switching supply located on the inner chassis deck. The DSP BOARD receives the outputs from this main power supply for post-regulation and distribution to the other radio modules.

A front-mounted fan supplies forced-air ventilation. Cooling air enters at the front-mounted filter and exits through vent holes around the rear perimeter of the chassis. The front panel board provides both high-speed and low-speed fan connections to allow user-selected air flow and fan noise to suit specific installation environments.

CIRCUIT DESCRIPTIONS

The rear panel antenna input is protected by spark gap SV2 and filtered by 3 GHz lowpass FL3 on the MID/HIGH BAND PRESELECTOR board, then routed to the common terminal of 4-position switch U3. Below 88 MHz receive frequency, positions 1 and 2 of U3 and positions RF1 and RF2 of U1, connect the antenna to the LOW BAND PRESELECTOR board, either directly or through the 20 dB resistive pad R10-12. Logic lines A1 and B1 determine the U3 switch position.

LOW BAND PRESELECTOR

Dual PIN diodes D1-8 on the LOW BAND PRESELECTOR select one of eight sub-octave bandpass filters. Each of the eight filters selects a frequency band approximately $2/3$ octave wide to cumulatively cover the Low Band range of 2 to 88 MHz (slightly over $5 \frac{1}{3}$ octaves). After bandpass filtering, the selected fractional-octave band is amplified by U2 and passed through 140 MHz band-reject filter L70, L22-25, C19-24. This band-reject filter provides additional attenuation of the Low Band 1st IF frequency. U4 buffers serial data to the PIN diode driver U1. Data from the OUT3 pin of U1 enables power to preamplifier U2 via Q1 and Q2.

MID/HIGH BAND PRESELECTOR

Position 3 of switch U3 on the MID/HIGH BAND PRESELECTOR board routes the antenna signal through a bank of seven mid-band filters selected by switches U4 and U5. Logic lines A3, B3, and C3 determine complimentary switch positions of U4 and U5. The first mid band filter is dedicated to the US FM broadcast band of 88-108 MHz. The remaining six filters have approximate $2/3$ octave passbands to

cover 108 to 1650 MHz. The selected filter output is amplified by U2 and lowpass filtered by FIL4 en route to the RF1 terminal of Mid Band / High Band switch U6.

Position 4 of U3 on the MID/HIGH BAND PRESELECTOR board routes the High Band antenna signals through one of two highpass/lowpass filter cascades selected by switches U7 and U8. Complimentary switch positions of U7/U8 are determined by logic line A4. This arrangement creates two half-octave subbands of 1650-2200 MHz and 2200-3000 MHz. The selected portion of the High Band is further conditioned by amplifier U9 and highpass filter FIL7 before being presented, along with the Mid Band subband to switch U6. Based on a logical AND combination of lines A1 and B1, switch U6 routes the selected subband through amplifier U10 to the MID/HIGH BAND PRESELECTOR board output.

FIRST CONVERTER

The FIRST CONVERTER module contains the first mixer and first IF amplifier for all receive frequencies above 88 MHz. The first local oscillator, moving in 2 MHz steps from 2528 to 4090 MHz, is highpass filtered by FIL9, amplified by U7, and applied as high side injection to mixer MX1. On the Mid Band receive frequencies of 88-1650 MHz, MX1 produces a 2440 MHz first IF which is filtered and amplified by the cascade comprising FIL6, FIL1, U2, FIL2, U3, and FIL7, selected by switches U1 and U4. This 2440 MHz IF has approximately 80 MHz bandwidth determined by SAW filters FIL1 and FIL2.

On the High Band receive frequencies of 1651-3000 MHz, MX1 produces a 1090 MHz first IF filtered and amplified by FIL8, FIL3, U5, FIL4, U6, and FIL5, selected by the complimentary positions of U1 and U4. The 1090 MHz IF has approximately 14 MHz bandwidth determined by dielectric filters FIL3 and FIL4.

Connections E4/E5 pass the Low Band 1st LO output of the FIRST LOCAL OSCILLATOR module straight through to the SECOND CONVERTER.

SECOND CONVERTER

The SECOND CONVERTER module contains the second mixer for all receive frequencies above 88 MHz. It also contains the first mixer for receive frequencies below 88 MHz. Each mixer, selected by switch U1, drives a common 140 MHz IF amplifier. Switches U6 and U7 select an IF filter of either 6 MHz bandwidth for receive frequencies above 20 MHz, or 2 MHz bandwidth for use below 20 MHz.

The input Mid Band and High Band first IF frequencies of 2440 or 1090 MHz are mixed with fixed Second LO injection frequencies of 2300 or 950 MHz respectively. Each injection signal is provided by the SECOND LOCAL OSCILLATOR module, filtered by FIL7, amplified by U3, and applied to the LO port of mixer MX1.

On Low Band, the LOW BAND PRESELECTOR board supplies the 2-88 MHz RF signal to the RF port of MX2. The Low Band injection signal is developed in the FIRST LOCAL OSCILLATOR module by dividing a 2272-3648 MHz VCO by 16 to produce 142-228 MHz in 250 kHz steps. This frequency-divided first LO is routed through the FIRST CONVERTER module E4/E5 to SECOND CONVERTER E2/FIL6 and U2, then applied to the LO port of MX2.

The 140 MHz IF output from switch U7 is lowpass/highpass filtered by FIL5 and C50-52, L10-11, amplified by U8, and routed to the THIRD CONVERTER module via E5.

THIRD CONVERTER

In the THIRD CONVERTER module, MX1 is the third mixer for receive frequencies above 88 MHz (Mid/High bands) and the second mixer for receive frequencies below 88 MHz (Low Band). The LO injection signal, developed in the THIRD LOCAL OSCILLATOR module, tunes a 2 MHz range from

117.71 to 119.7 MHz in 10 kHz steps (1 kHz optional). Low Band receive frequencies use a 240 kHz segment of this range from 118.48 to 118.72 MHz to fill in the 250 kHz tuning steps produced by the divided-down first LO. The third LO injection signal is amplified by U4 and U15 and applied to the LO port of mixer MX1. The 159 MHz trap L11/C70 attenuates a potential image frequency band at the input to U4.

The 21.4 MHz IF resulting from this low-side mix provides two outputs from the THIRD CONVERTER module: The Wideband IF Output at E5 is sampled by directional coupler U1 and lowpass filtered by the L7-L8, C43, C47-C48 combination. This output is either 2 MHz or 6 MHz wide, depending on the receiver tuned frequency, and has 10 kHz (1 kHz optional) tuning resolution. The Narrowband Output is filtered to 300 kHz bandwidth, amplified and AGC leveled, then delivered to the DSP BOARD via connection E4.

Double-resonator filters L1/C9, L3/C11, and L5/C18, L6/C20, along with U2 form a 21.4 MHz tuned IF amplifier which delivers a 300 kHz subband of the MX1 output to Variable Gain Amplifier U3. Fixed gain amplifiers U5 and U6 boost the signal to a maximum of 1 volt peak-to-peak for lowpass filtering by L9-L10, C49-C51 and output to E4.

Balanced diode detector IC1BC/U7A samples the IF signal at the output of amplifier U5 and provides a rectified signal envelope to AGC amplifier U7B. Above a threshold established by R69, the low-going output of U7B forward-biases diode IC1A, pulling AGC node BB low. Pull-up resistor R79 and integrating capacitor C71 establish the analog AGC time constant. Through R42, op-amp U8B buffers the AGC node voltage from C71 to the gain control input of VGA U3, completing the AGC loop. The active region of the VGA control input is 0.25 to 1.5 volts with a positive slope of 32 dB/V establishing a 40 dB control range.

Manual Gain Control buffer U9 and window comparator U8A provide a means for the DSP processor to modify the analog AGC function. When a digital-to-analog converter on the DSP BOARD reduces the MGC voltage below the existing analog AGC voltage, U9 pulls the AGC node BB lower through the base-emitter junction of Q1. Feedback to U9 through R42 regulates the AGC voltage to the new set value. The ANALOG and DIGITAL outputs from U8A and Q4 inform the DSP which driving source is asserting analog AGC gain reduction - the analog envelope detector or the digital-to-analog converter. This mechanism allows software implementation of both manual gain control and slower analog AGC decay rates.

Another function enabled by the U8A/U9 arrangement, useful in narrowband detection modes, is DSP correction of analog AGC action caused by strong signals located outside the digitally implemented selectivity bandwidth. Because the analog AGC detector samples the entire 300 kHz analog IF bandwidth, some signals causing AGC action may be invisible to the DSP when narrow selectivity filtering (partially implemented in a AD6620 Digital Down Converter) precedes the digital detection algorithm. The information provided to the DSP by the AGC, ANALOG, and DIGITAL outputs of U8/U9/Q4 allows the software to identify and compensate for the effects of these strong "out-of-band" signals. As a result, signal strength calculation and overall AGC action is based only on those signals that are inside the chosen selectivity bandwidth.

FIRST LOCAL OSCILLATOR

The FIRST LOCAL OSCILLATOR module contains a single-loop fractional-N frequency synthesizer producing 2272-4090 MHz in 2 MHz steps. Serial data from the DSP board configures synthesizer U1 to divide the provided 100 MHz reference by five and the selected VCO U3 or U10 by a MODULO 10 fractional N-number of 113.6 to 204.5 for phase comparison. U2 integrates phase pulses from the synthesizer chip to develop a DC tuning voltage for the active VCO. The U2 tuning voltage output is sampled by R52-R54 and delivered to the DSP board for possible charge pump gain calibration based on VCO tuning voltage slope variation. Loop filter L1, L2, L5, C6-C10, C72-C73 reduces reference and phase-correction ripple on the tuning voltage before it is applied to the VCO control input. The active VCO output selected by switch U11 splits to two buffer amplifiers U4 and U5. U5 provides feedback to

the synthesizer chip, completing the loop. U4 develops the Mid/High Band First LO output which splits between the module output at E1 and MODULO 16 divider U6/U7 to provide the Low Band First LO of 142-228 MHz.

The 100 MHz master frequency reference signal is developed on the DSP board and is delivered through this module to the SECOND LOCAL OSCILLATOR module via emitter follower Q11.

SECOND LOCAL OSCILLATOR

The SECOND LOCAL OSCILLATOR module contains a single-loop fractional-N frequency synthesizer producing a fixed frequency of 2300 or 950 MHz. Serial data from the DSP board configures synthesizer U1 to divide the provided 100 MHz reference by 5 or 10 and the selected VCO U3 or U6 by a MODULO 10 fractional N-number of 115.0 or 95.0 for phase comparison. U2 integrates phase pulses from the synthesizer chip to develop the DC tuning voltage for the active VCO. Loop filter L1, L2, L4, C6-C10, C50-C51 reduces reference and phase-correction ripple on the tuning voltage before it is applied to the VCO control input. The active VCO output selected by switch U4 drives the module output E1 through buffer amplifier U5. A sample of the U4 output at R18 provides feedback to the synthesizer chip, completing the loop.

The 100 MHz master frequency reference signal from the FIRST LOCAL OSCILLATOR module is delivered through this module to the THIRD LOCAL OSCILLATOR module via emitter follower Q1.

THIRD LOCAL OSCILLATOR

The THIRD LOCAL OSCILLATOR module contains a single-loop integer-N frequency synthesizer driving an N=1 mixing loop to develop a 117.71 to 119.7 MHz output tuning in 10 kHz (or optionally 1 kHz) steps.

Serial data from the DSP board configures synthesizer U1 to divide the provided 100 MHz reference by 250 (or optionally 2500) and VCO U3 by 1771 to 1970 (or optionally 17701 to 19700). Q11 and Q12 modify the (nominally 400 kHz) loop filter for the optional 40 kHz reference frequency when the fine tuning option is selected.

VCO U3 delivers 708.4 to 788 MHz in 400 kHz (or optionally 40 kHz) steps to the RF input of PLL U10 which is programmed to divide by 40 producing a 17.71 to 19.7 MHz reference in 10 kHz (or optionally 1 kHz) steps at the U10 phase comparator. VCO Q5/Q9 driving buffer U4 develops the module output at E1. The mixing loop is closed via mixer U11 which subtracts 100 MHz from the VCO output of 117.71 to 119.7 MHz to provide 17.71 to 19.7 MHz directly to the U10 phase comparator (R=1) through lowpass filter L4-L6.

When the receiver is tuning the Low Band (2-88 MHz), the Third LO output frequency is restricted to the range 118.48 to 118.72 (or optionally 118.471 to 118.720) to fill in the 250 kHz stepping of the divided-down First LO.

Logic/DSP System

The RX400 Logic/DSP assembly incorporates Digital down Conversion, Signal Processing, Control & Interface, Power and Master Clock Reference circuitry on a single circuit board. The Logic/DSP board controls all Preselector, RF Converter and Local Oscillator (LO) boards over ribbon cables. The RF/LO and Preselector boards are programmed by the DSP processor via the attached ribbon cables to achieve the correct RF tuning. In addition, the DSP board monitors LOCK DETECT (LD) signals from the LO boards to be reported to the controller as status information.

POWER:

The system power supply delivers +/-12V and +/-5V to the Logic/DSP board via connector J23. On-board power regulators U57,58 and U47 provide the proper +1.2 and +3.3 volt supply for the DSP core and I/O system. Regulators U48 and U44 develop +24 and +9 volts which are provided to other boards via the same ribbon cables which provide control and monitoring. Connector J24 provides a user-selectable +5 or +12 volts to fan depending on application requirements.

LOGIC SYSTEM:

The processor (U1) is an Analog Devices ADSP-21262 DSP processor. The DSP processor communicates with various other on-board components to implement a unified signal processing and control system. In addition to the DSP processor the system includes an Analog Devices AD6620 digital down converter (U16 & U17), 16C500 RS-232 UART (U7), 10/100 Ethernet interface chip (U6), FLASH memory components (U14,U15,U49), A/D U13 and D/A U14. System bus management and I/O are contained in U27, a Xilinx Programmable Logic Device (PLD) U27.

IF PROCESSING:

The AD6620 down-converter accepts the 3rd IF signal via coax connector J18. The 3rd IF center frequency is 21.4 MHz. The Digital down Converter (DDC) (comprised of AD6620 (U16) and AD9244 (U17)) converts the signal to base band for further processing inside the DSP. The sample rate between the AD6620 and the DSP is dependent on the selected IF bandwidth. During power-up the DDC is initialized via its parallel control interface (U53, U54). After initialization of the DSP processing system the DDC is controlled via the serial control interface.

AGC PROCESSING:

The AGC processing system includes U12, U13 and I/O connections ABIT and DBIT in addition to circuitry located on the 3rd converter board.

CONTROL INTERFACE:

The DSP processor provides user control through RS-232 or Ethernet Interfaces. Digital audio is provided on the Ethernet Interface only. Please see the [RX400 Control Interface Command Set](#) for command interface details.

4. Maintenance & Troubleshooting

RX-400 MAINTENANCE INSTRUCTIONS

INTRODUCTION: To perform maintenance tasks, the technician shall identify faulty modules or subassemblies. The faulty module or subassembly shall be replaced with a known good one.

CLEANING AND LUBRICATION: Front panel and control surfaces may be cleaned using a soft cloth dampened with a mild detergent solution. *Never use caustic cleaners on knobs or panel surfaces.* The RX-400 has no lubrication points.

TROUBLESHOOTING: Troubleshooting consists of identifying faulty modules or subassemblies by running the BITE tests. Level2 and 3 BITE tests list symptoms and the probable module or modules associated with the fault.

INSPECTION: Mechanical switches, potentiometers, and front panel connectors should be checked periodically for signs of wear or intermittent operation. Rear panel connectors should be inspected for damage or contamination whenever the unit is removed.

PERFORMANCE VERIFICATION TEST FOR MDEL RX-400: The following verification tests may be performed if there is a suspected failure. Perform each check in the order listed, as previous checks may contain setup procedures required for succeeding tests.

TEST EQUIPMENT REQUIRED:

- RF signal generators, 2 each HP8648C or equivalent.
- 2-way hybrid combiner, Mini-Circuits ZFSC-2-4S and ZN2PD2-50S, or equivalent appropriate to the frequency range of the desired tests.
- Audio analyzer, HP8903B or equivalent, capable of SINAD measurement.
- IF spectrum analyzer, HP3585A or equivalent, useable at 21.4 MHz.
- Computer terminal with RS-232 interface, Wise 50, DEC VT-100, or a computer running an equivalent emulation program.

FUNCTIONAL TESTS FOR MODEL RX-400:

Note1: When performing the following tests, daisy-chain the signal generator frequency reference inputs/outputs with the RX-400 external reference input to lock all equipment to one standard.

*Note2: In USB mode, **the receiver tuned frequency shall be 1 kHz below** either the generator frequency or the frequency of an expected distortion product to produce a 1 kHz audio beat note for the audio analyzer.*

Note3: Attenuation (loss) of the specific cables and hybrid combiners used must be known and calibrated out of the generator amplitude settings.

SPECIFICATION	TEST SETUP	TYP.	MIN/MAX
Sensitivity			
Attenuator OFF	Connect a signal generator to the receiver		
USB mode	RF Input. (Calibrate cable loss first.)		
3 kHz bandwidth	Connect an audio analyzer with SINAD measurement capability to the mono audio output.		
Low Band -114 dBm 15 dB max NF	For each frequency in the following list, apply -114 dBm to the receiver input: 2.0, 2.6, 3.19, 3.2, 4.1, 4.99, 5.0, 6.5, 7.99, 8.0, 10.0, 11.99, 12.0, 16.5, 20.99, 21.0, 27.5, 33.99, 34.0, 44.5, 54.99, 55.0, 71.5, 87.99 MHz	SINAD 12 dB typ.	10 dBmin.
Mid Band -113 dBm dBmin. 16 dB max NF	For each frequency in the following list, apply -113 dB to the receiver input: 88.0, 98.0, 107.98, 108.0, 138.0, 169.99, 170.0, 220.0, 269.99, 270.0, 348.0, 424.99, 425.0, 547.5, 669.99, 670.0, 860.0, 1049.99, 1050.0, 1350.0, 1649.99 MHz	12 dB typ.	10
High Band -112 dBm 17 dB max NF	For each frequency in the following list, apply -112 dBm to the receiver input: 1650.0, 1870.0, 2089.99, 2090.0, 2545.0, 2999.0 MHz	12 dB typ.	10 dBmin.
Second Order Intercept Point +50 dBm	Connect two signal generators through the appropriate hybrid combiner for the frequency to be used. Connect the combiner output (calibrated to compensate for combiner and cable loss) to the RX-400 RF Input. Connect an audio analyzer with SINAD measurement capability to the mono audio output.		

SPECIFICATION	TEST SETUP	TYP.	MIN/MAX
min.	<p>For each frequency in the list below: Temporarily set generator #1 on frequency to supply a level of -110 dBm to the receiver input. Record the SINAD displayed on the audio analyzer as "reference". Move generator #1 to (frequency / 2) -9 kHz. Set generator #2 to (frequency / 2) +9 kHz. Set both generator amplitudes to produce -30 dBm each at the receiver input connector. Observe the SINAD of the second order distortion product on the audio analyzer. Calculate the Second Order Intercept as:</p> <p>50 +(ref. SINAD) -(dist. prod. SINAD)</p>	55 dBm typ.	50 dBm
	<p>3.19, 4.99, 7.99, 11.99, 20.99, 33.99, 54.99, 87.99, 107.98, 169.99, 269.99, 424.99, 669.99, 1049.99, 1649.99, 2089.99, 2999.0 MHz</p>		
<p>Third Order Intercept Point -7 dBm</p>	<p>Connect two signal generators through the appropriate hybrid combiner for the frequency to be used. Connect the combiner output (calibrated to compensate for combiner and cable loss) to the RX-400 RF Input. Connect a spectrum analyzer to the RX-400 21.4 MHz IF output.</p>		
min.	<p>Using the frequencies listed above for the Second Order test: Set generator #1 to frequency -10 kHz. Set generator #2 to frequency +10 kHz. Set both generator amplitudes to each produce -20 dBm at the receiver input connector. If the third order products displayed on the spectrum analyzer have amplitudes that are equal or within 6 dB, use their average amplitude to calculate the Third Order Intercept as:</p>	-5 dBm typ.	-7 dBm
	<p>{[(tone level) - (dist. prod. level)] / 2 } -20</p>		
	<p>If the distortion products differ by more than 6 dB, use the higher level product in the calculation.</p>		

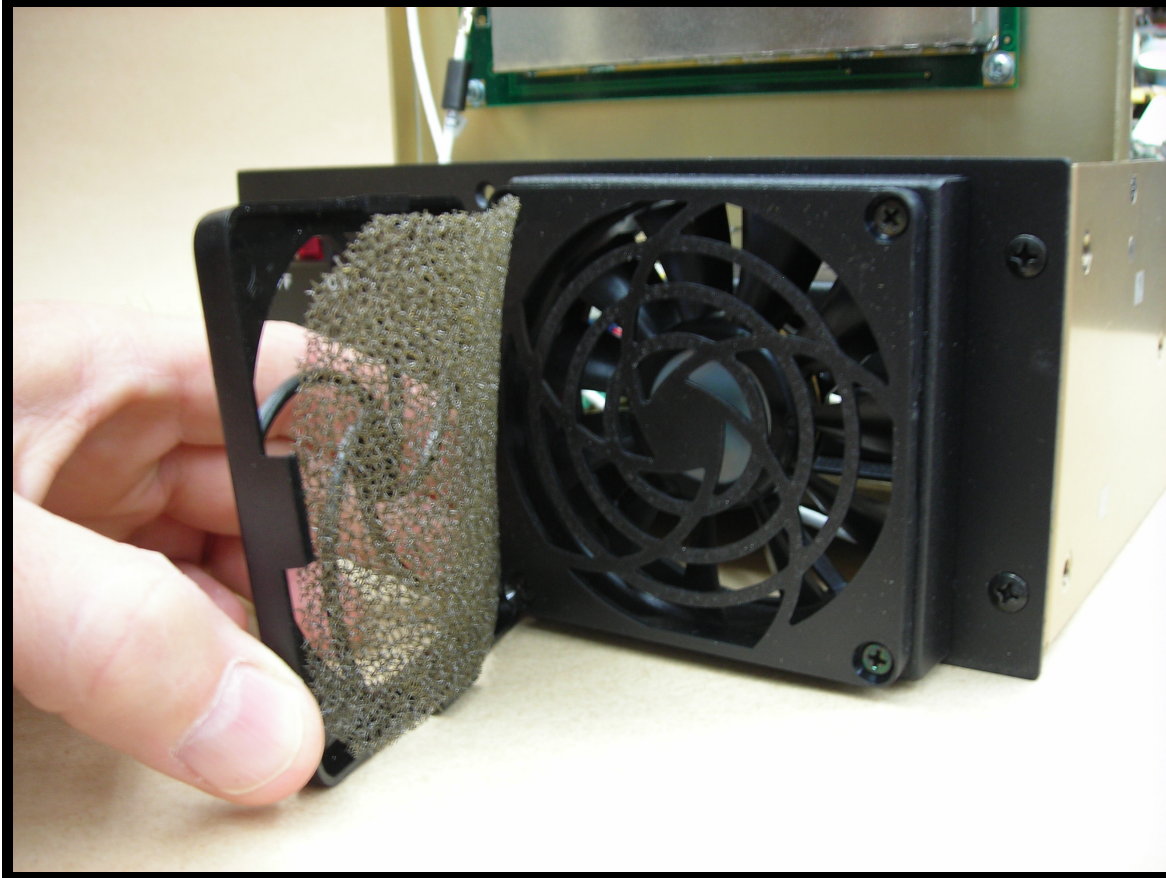


Figure 7 – Air filter Replacement

The air filter can be cleaned or replaced by removal of the fan shroud located on the front of the RX-400.

5. Illustrations & Parts Lists

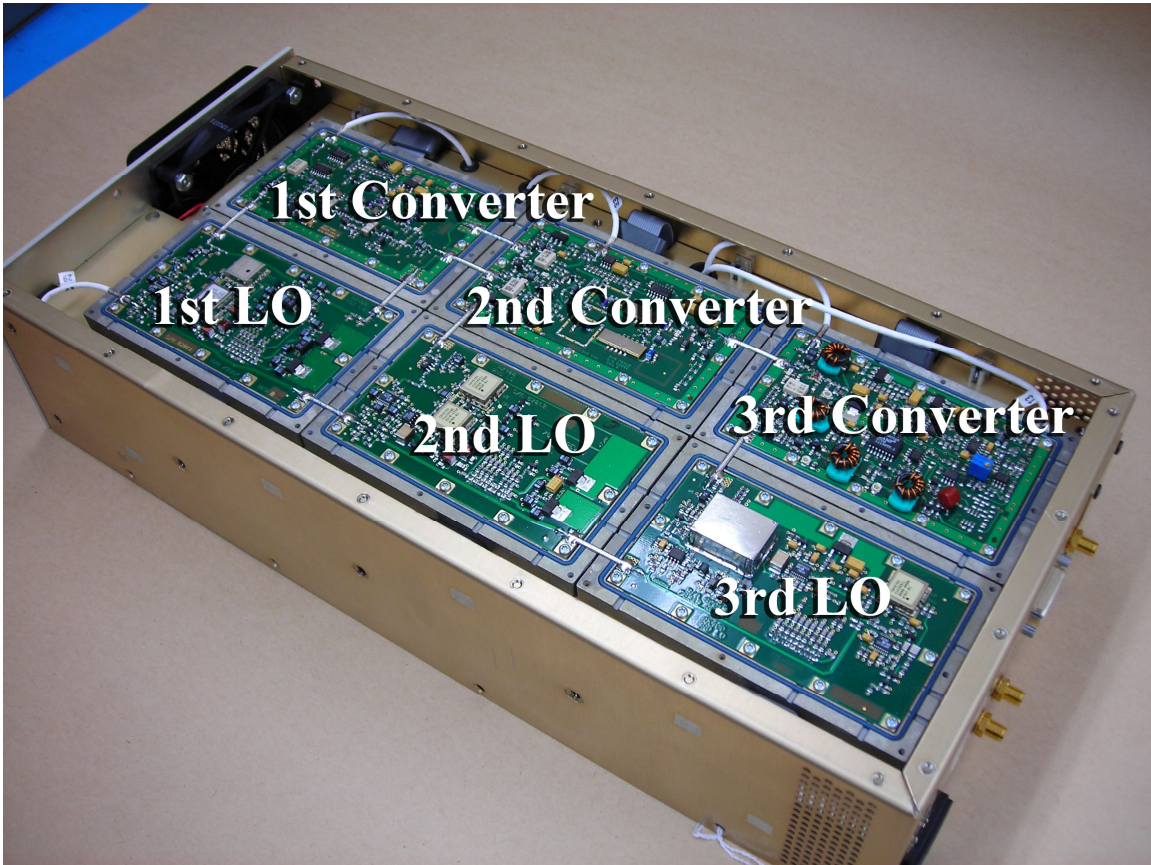


Figure 8 - Location of Receiver Assemblies

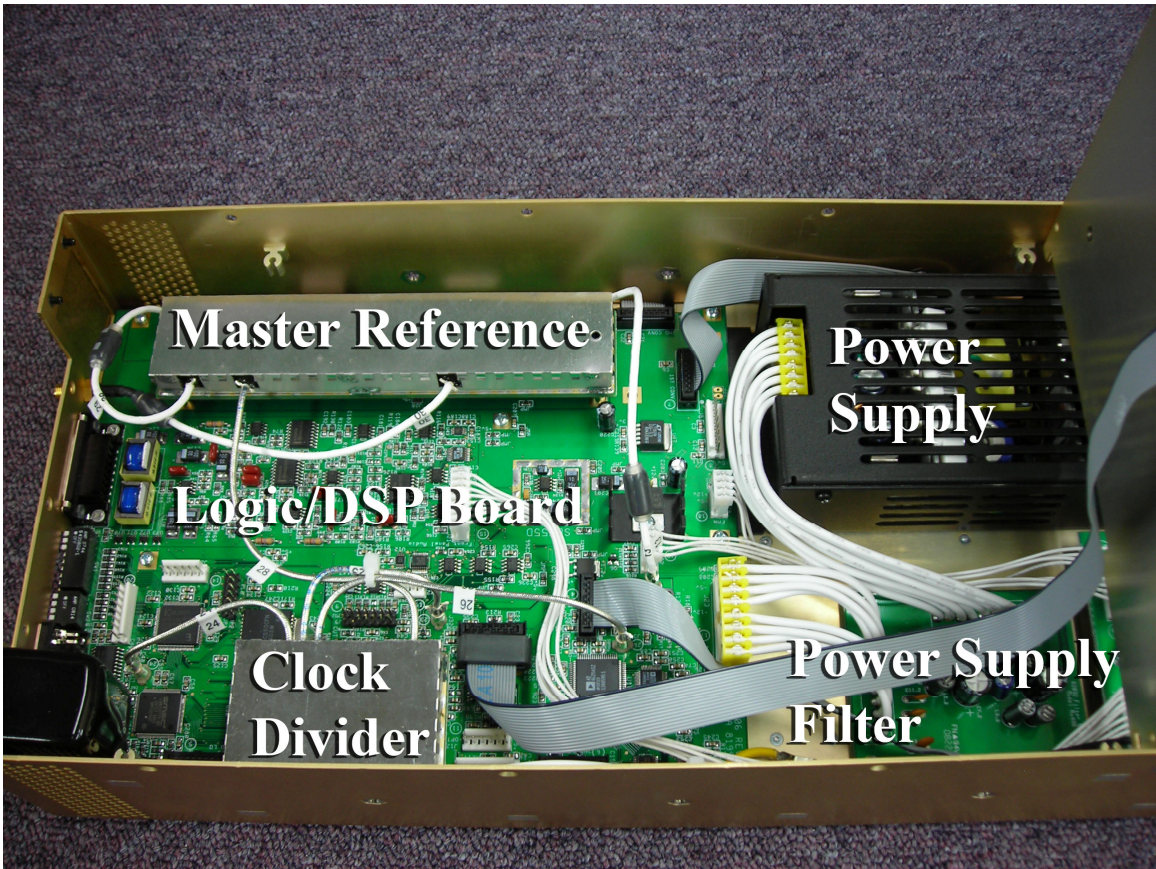


Figure 9 - Location of Logic, Control & Power Assemblies

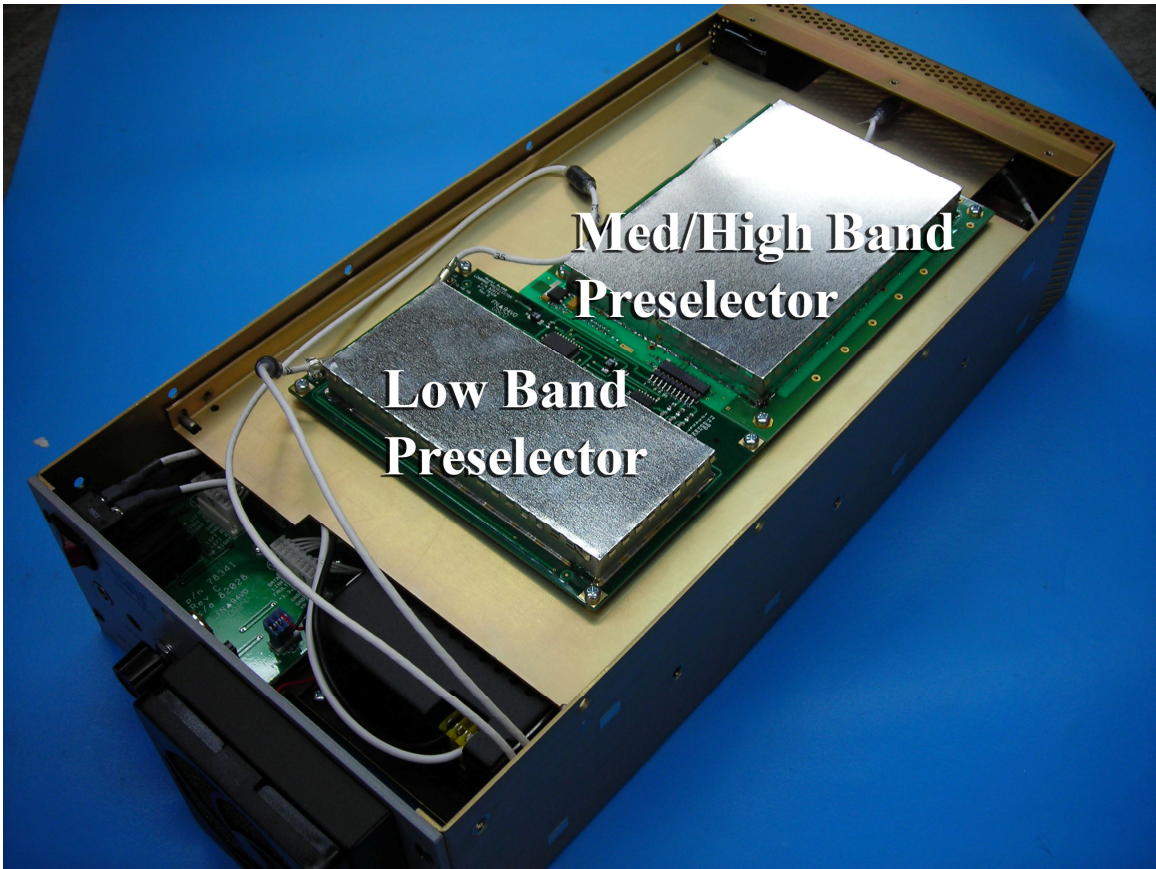


Figure 10 - Location of Preselector Assemblies

Circuit Boards, Materials and Placement

Assembly

82011	1 st LO Board	Schematic	Material List	Parts Placement
82012	2 nd LO board	Schematic	Material List	Parts Placement
82013	3 rd LO Board	Schematic	Material List	Parts Placement
82010	3 rd Converter Board	Schematic	Material List	Parts Placement
82009	2 nd Converter Board	Schematic	Material List	Parts Placement
82008	1 st Converter Board	Schematic	Material List	Parts Placement
82014	Low-Band Preselector	Schematic	Material List	Parts Placement
82015	Mid-High Band Preselector	Schematic	Material List	Parts Placement
81996	Logic/DSP Board	Schematic	Material List	Parts Placement
82031	Divider Board	Schematic	Material List	Parts Placement
82029	Reference Board	Schematic	Material List	Parts Placement
82028	Front Panel Board	Schematic	Material List	Parts Placement
82032	Power Supply Filter Board	Schematic	Material List	Parts Placement