MK20A DDS SYNTHESIZER THEORY OF OPERATION
120496

The new MK20A DDS dual synthesizer is a complete ILS synthesizer covering both dual and single frequencies for the Localizer and Glideslope. It also includes the ability to cover the VOR band in 50 kHz channel spacing. The frequency(s) are locked to a single 39.95 MHz TCXO. The frequencies are developed via. DDS integrated circuit which outputs approximately 9 MHz (channel frequency divided by 12 for Localizer and VOR and divided by 30 for the Glideslope). The operator selects the frequency via. BCD jumpers. The Dual/Single mode is selected by a single jumper set either on Dual or Single. Only legitimate 50 kHz VOR or ILS frequencies are allowed to be selected. Any other frequency will shut off the RF output and light the "VCO's OFF" light.

For a detailed theory, refer to the "MK20A DDS SYNTHESIZER BLOCK SCHEMATIC" and "MK20A DDS SYNTHESIZER" (EL120496) schematic.

The frequency is selected by placing jumpers on the correct position for the desired frequency. For 110.15 MHz, a jumper would be put on the 100 pin, the 10 pin, the 0.1 pin, and the 0.05 pin. Even though the 0.075 and 0.025 pins are present they are not used at this time. The PROM (U1) would have to be programmed to include the 25 kHz channels.

Most of the jumpers (see schematic) go directly to the PROM, however some are decoded by the by the EPLD. The EPLD provides some decoding and the timing to load the frequency words into the DDS IC's (U7 and U17). The DDS IC's require 5 single byte words to fully select the frequency. The 5 bytes are composed of one byte for setup and a 32 bit frequency selection word. The frequency is sent to the DDS IC's approximately 2 time a second. Even though the DDS IC's will retain the selected frequency indefinitely, the frequency is continually input to insure correct tuning in the event of a power supply glitch. The EPLD clock is provided by an RC oscillator U28A operating at about 1.8 kHz.

The approximate 9 MHz out of the DDS IC's is a digitally generated signal, generated by a division of the 39.95 MHz TCXO frequency. The frequency out of the DDS IC's can be stepped in approximately 0.01 Hz steps and is calculated by the formula, desired frequency = ((39.95MHz)*N)/(2^32)).
The desired frequency for an output frequency of 112MHz, would be the channel frequency, 112MHz divided by 12 which would give 9.333333 MHz. To figure the closest value of N would give (112e6/12)*2^32)/(39.95e6). This requires N to have a decimal value of 1,003,413,302. This is not an exact value but is less than 0.1 Hz error in 112 MHz (not counting the TCXO error). The PROM is programmed to load in the nearest N value to get the desired frequency. In dual mode the N value for the Fo+4kHz sets that side 4 kHz above the channel frequency and the other side, 4 kHz below channel frequency. When the Dual/Single jumper is in the Single position, the EPLD selects a different set of frequencies to put the Fo+4kHz side on the channel frequency and turns off the Fo-4 kHz side. For all VOR frequencies, selecting Dual will turn off the VCO's and light the VCO's OFF light.

The digitally derived 9 MHz is filtered by a lowpass filter and squared up by U20 and U34. The PLL IC, U8 and U18 have a direct input to it's phase/frequency detector so the phase/frequency detector operates at the 9 MHz. Also to the phase/frequency detector, is a sample of the channel frequency divided by 12 for the Localizer and VOR and 30 for the Glideslope. The divide ratio is selected by pins 7,10, and 16 of U8/U18. This line is pulled low when the 100 MHz select jumper is selected. The PLL IC's have built in charge pumps to directly drive an active low pass filter.

The low pass filters are standard second order loop types composed of U9/U19 and associated components. The low pass filter output drives two VCO's inputs. Only one of the VCO's are powered, depending on whether a LOC/VOR frequency or a Glideslope frequency has been selected. This is depicted in the Block

schematic by a SPDT relay. The VCO's output goes to a passive combining unit and is amplified by U4/U12.

The amplified output is routed directly through the Glideslope LPF or if a LOC/VOR frequency is selected, through both low pass filters. This switching is depicted on the Block schematic using two STDT relays. These relays are solid state relays.

To further assure frequency integrity, the Fo+4 kHz (or Fo for a single frequency synthesizer) frequency is divided and sent to the monitor. The channel frequency set into the monitor must agree with this frequency or an alarm will be indicated. In addition when the synthesizer is operating in the dual mode, both frequencies are mixed to give a frequency of 8 kHz which is divided down to 125 Hz.(for future use the direct 8 kHz is available by jumper selection). If there is an error in the 8 kHz, an alarm will be indicated.

To assure the unit meets all of the specifications, all of the frequency control lines and the Dual/Single line are brought out to the connector for testing purposes. Each unit is 100 % tested on all frequencies for frequency accuracy, spurious generation, and power out (See attached spectrum plots).

THEORY OF OPERATION AUDIO GENERATOR ASSEMBLY
120497

1.0 Audio Generator Circuit-Card Assembly. - See schematic 120497. Audio generator cca provides audio modulation components for glide slope group operation. Audio generator cca generates path transmitter csb audio (90 + 150 Hz), path transmitter sbo audio (90 - 150 Hz), clearance transmitter csb audio (150 Hz), course zero crossing, clearance zero crossing, course phase, and clearance phase signals for glide slope modulator/power amplifier assemblies. The audio generator cca consists of the following circuits: programmable logic circuit, clock circuit, memory circuit, digital-to-analog conversion circuit, summing amplifiers and offset amplifiers circuit, variable attenuator circuit, and analog switch circuit. Each of the audio generator circuits is discussed in the following paragraphs.

1.1 Programmable Logic Circuit. - See schematic 120497. The programmable logic circuit is an interface between the microprocessor on glide slope monitor cca (not shown) and the circuits on audio generator cca. The programmable logic circuit provides addresses for the onboard memory circuits and controls for all of the onboard circuits. The programmable logic circuit consists of programmable logic device (PLD) U8. The central processing unit (cpu) data lines to U8 can be tested by wiring a byte of data from glide slope monitor cca external data lines to U8 and reading the data back for comparison. The functions of the PLD signals are discussed in the following paragraphs.

1.2 Programmable Logic Device Address Lines Function. - See schematic 120497. The address lines for PLD U8, shown as cpu address lines CPU A0 through CPU A4, are external addresses A0 through A4 from glide slope monitor cca at P2-B27 through P2-B31. The PLD address lines select internal registers in U8 for storing setup data.

1.3 Programmable Logic Device Data Lines Function. - See schematic 120497. The PLD data lines for U8, CPU D0 through CPU D7, are external data lines from glide slope monitor cca at P2-C24 through P2-C31. The function performed by the data lines is to write setup data to U8 and to store digital waveforms in U1 at system start up. Setup data is written to U8 when the external write signal from glide slope monitor cca at P2-B26 is a rising edge and is routed to U8 as a cpu write (/CPU WR) signal. Setup data stored in U8 is read when the external read signal from localizer/glide slope monitor cca at P2-B25 is logic 0 and is routed to U8 as a cpu read (/CPU RD) signal.

1.4 Static Random-Access Memory Lines Function. - See schematic 120497.The random-access memory (ram.) address lines (RAMA0 through RAM A11) address the 32K by 8-bit memory in static random-access memory (sram) U1 for data storage. The sram address lines RAM A12, RAM A13, and RAM A14 select a bank of 4096 by 8-bit memory locations in sram U1. Eight different memory locations of 4096 by 8 bits can be selected. When glide slope monitor cca is writing or reading sram data, the address counter inside U8 is incremented by the /CPU RD or /CPU WR signal. Localizer/glide slope monitor cca reads data from U1 and writes data to U1 via octal transceiver U14 as U1 is addressed by U8. During equipment start up, glide slope monitor cca resets the

address counter in PLD U8 to write new setup data to U1 as ram. Data 0 through 7 (RAMD0 through RAM D7) via octal transceiver U14 as U1 is addressed by U8.

1.5 Digital-to-Analog Control Lines and Level Address Lines Function. - See schematic 120497, sheets 2 and 3. The digital-to-analog (d/a) control signals from U8 (D/A A0 through D/A A6) latch data (RAM D0 through RAM D7) into internal latches of d/a converters U4, U6, 11, and U16. (The d/a converters are part of the conversion circuit.) The level address (LEVEL A0 through LEVEL A3) lines are supplied by U8. These lines, along with CPU A0, latch data (CPU D0 through CPU D7) into the internal latches of dual 8-bit d/a converters U3, U7, U10, and U15. (These d/a converters are part of the variable attenuator circuit and are used to vary the amplitude of the output signal.)

1.6 Clock Circuit. - See schematic 120497. Clock G1 supplies a 2.4576-MHz clock signal to U8-C1 through the jumper from J1-1 to J1-2. (The jumper is always installed except during a test with ATE.) The clock increments the ram. Address outputs of U8 (RAM A0 through RAM A14). The 2.4576-MHz clock signal sent to P2-A22 is not used.

1.7 Memory Circuit. - See schematic 120497. The memory circuit stores the digital audio patterns that are converted to analog signals and used to modulate glide slope modulator/power amplifier assembly. The memory circuit consists of sram U1 and octal transceiver U14. The sram U1 is a 32K by 8-bit memory chip that stores the digital audio patters. Octal transceiver U14 routes cpu data to/from sram U1 and glide slope monitor cca. Data is written to U1 via octal transceiver U14 when the /CPU RD signal at U14-1 and /BUS EN signal at U14-19 are logic 0. The data pattern written to U1 is addressed by U8 with RAM A0 through RAM A14. During a data write to U1, the NEW DAT signal at U1-22 is logic 1 and the /RAM WR signal at U1-27 is logic 0. The data is written to U1 in an 8-byte pattern 512 times to store 4096 bytes of data. The ram. Address lines RAM A12, RAM A13, and RAM A14 from U8 are latched outputs that allow the glide slope monitor cca to bank-select up to eight, completely different, 4096 area locations in the sram. When the glide slope monitor cca has finished writing the data block (4096 bytes),. the glide slope monitor cca reads the data back and compares the data to ensure that there were no errors in the data transfer.

1.8 Digital-to-Analog Conversion Circuit. - See schematic 120497. The d/a conversion circuit converts the digital waveform patterns stored in the memory circuit to analog signals for modulating the transmitters. The d/a conversion circuit consists of the internal integrated circuit function and the d/a conversion function. The functions are described in the following subparagraphs.

1.9 Internal Integrated Circuit Functions. - See schematic 120497. Each d/a conversion circuit is a 12-bit d/a converter and has a double buffered latch input. Each d/a converter contains a set of three 4-bit input latches that latch the input data. These input latches are followed by an internal 12-bit latch that latches the data for the d/a converter. This latch configuration enables writing a byte of data (8bits) to two input

latches and a nibble of data (4bits) to the other input latch before latching the data in the 12-bit latch for the d/a converter. When data address line 6 (D/A A6), which is common to each d/a converter, is strobed, the analog outputs of all the 12-bit d/a converters are converted to analog signals simultaneously. The simultaneous conversion of data prevents phase error in the outputs of U4, U6, U11, and U16.

1.10 Digital-to-Analog Conversion Function. - See schematic 120497, sheet 3. The d/a conversion function converts the digital waveform patterns stored in the memory circuit to analog signals for modulating the transmitters. The d/a conversion function consists of U4, U6, U11, and U16. The output of d/a converter U4-9 is the course csb (CSE) signal and is a 90 + 150 Hz composite audio signal. The output of d/a converter U6-9 is the course sbo (Y20) signal and is a 90 - 150 Hz composite audio. The outputs of U4 and U6 modulate the path (course) transmitter. The output of U11-9 is the clearance csb (CLR) signal and is a 150-Hz audio signal. The CLR output of U11 modulates the clearance transmitter. The dc reference output at U6-6 is a dc voltage input to offset amplifier U5D. The dc reference output at U16-6 is a dc voltage input to offset amplifier U9D. The offset amplifiers are discussed in the following paragraph.

1.11 Summing Amplifiers and Offset Amplifiers Circuit. - See schematic 120497. The summing amplifiers sum the analog signals required for modulating the glide slope path (course) and clearance transmitters. The offset amplifiers determine the zero reference for the summed analog signals. The summing amplifiers are U2A, U2D, U12A, and U12D. The offset amplifiers are U5D and U9D. Summing amplifier U2D receives the course csb signal (CSE) from U4-9 and outputs the signal at U2D-14. The signal is the input to U3-4. The IDENT input and the airport weather observation system (AWOS) input to summing amplifier U2D are not used in the Mark 20 ILS glide slope group equipment. Summing amplifier U2A sums the course sbo signal (Y20) from U6-9 and a dc offset voltage from U5/d-14. The dc offset voltage ensures that the output of U2A goes above and below the zero reference. Summing amplifiers U12D and U12A and offset amplifier U9D are similar and are not discussed.

1.12 Variable Attenuator Circuit. - See schematic 120497. The variable attenuator circuit consists of dual d/a converters U3, U7, U10, and U15 and operational amplifiers U5A, U2C, U2B, U9C, U17D, U12C, U12B, U17B, U5C, U5B, U17C, and U17A. Each d/a converter functions as two digitally controlled variable attenuators. The variable attenuators enable varying the amplitude of the output analog signal. The operational amplifiers are cascaded in pairs to form a buffer and voltage follower. A 90 + 150 signal is the input analog signal at U3-4 and the attenuated 90 + 150 Hz signal is output at U3-2. Operational amplifier U2C supplies the course and carrier sideband (CSE CSB) to P2-C2 via quad single-pole single-throw (spst) analog switch U13. The CSE CSB signal is the modulation signal for glide slope modulator/power amplifier assembly. Operational amplifier U5A is a voltage follower and supplies a monitor course csb signal (MON CSE CSB) to P2-C3. This signal is routed via the backplane to the applicable glide slope monitor cca. A 90 - 150 Hz signal is the analog input at U3-18 and the attenuated signal

is output at U3-20. Operational amplifiers U2B and U9C function the same as U2C and U5A and are not discussed. Dual d/a converters U10, U7, and U15 and associated operational amplifiers function similar to U3 and are not discussed.

GLIDE SLOPE POWER AMPLIFIER THEORY OF OPERATION AND MODULATION
120504

1.0 Glide Slope Modulator/Power Amplifier. - See schematic 120504 glide slope modulator/power amplifier assembly. Two transmitters, known as Glide slope modulator/power amplifier assemblies, are used to provide the course (path) csb, course (path) sbo signals and the clearance csb output signals to be routed to transfer switches and on to the antennas. Each glide slope modulator/power amplifier assembly receives carrier signals from a DDS controlled RF synthesizer assembly (see schematic 120496). Modulation signals are generated from an audio generator cca.(see schematic 120497) The carrier signals are continuous wave RF in (CW RF IN) signals and the modulation signals are the csb 1 (90+ 150 Hz), csb 2 (150 Hz), and sbo 1 (90 - 150 Hz) signals. Glide slope modulator/power amplifier assemblies then perform AM modulation, power amplification on the path input signals (csb 1 and sbo 1) and clearance csb (150Hz) and provide monitor input data (such as forward and reverse power measurements) to the monitor cca. Glide slope Modulator/Power amplifier assembly consists of the csb circuit and sbo circuit. These circuits are discussed in the following paragraphs.

1.1 Carrier-Plus-Sideband Circuit. - See schematic 120504, sheets 2, 3, and 5. The csb circuit amplifies, modulates, and samples the RF supplied to the glide slope synthesizer assembly at RF IN connector J1 and a 90 + 150 Hz (CSB CONTROL) modulation signal at connector J4-11. The csb channel circuit performs the required modulation and outputs a course CSB OUT signal at CSB OUT connector J2. The CSB OUT signal is routed to the antenna via a glide slope transfer switch assembly and glide slope divider /combiner assemblies. The csb channel produces the CSB OUT signal. The csb channel circuit also includes a detected forward power circuit and detected reverse power circuit for monitoring the signals supplied to the antenna and a high voltage standing-wave ratio (vswr) protection circuit. These circuits are discussed in detail in the following paragraphs.

1.2 RF Input Circuit. - See schematic 120504, sheet 2. The RF input circuit splits the incoming RF and supplies one input drives the csb channel and the other input drives the sbo channel. The RF input circuit consists of power splitter hybrid HY2 and amplifier U2. Power splitter hybrid HY2 is a broadband transformer-type power splitter that receives the CW RF IN signal and splits the signal to supply two RF outputs. One RF output is a signal for the csb circuit and the other RF output is a signal for the sbo circuit. Amplifier U2 provides additional gain for the csb RF signal but has the primary propose of isolating the glide slope synthesizer assembly from the Glide slope Modulator/Power amplifier assembly circuits. The CW RF IN signal is routed to power splitter HY2-1 and split with output HY2-6 supplied to the sbo circuit and output HY2-5 supplied to amplifier U201. Amplifier U2 outputs the amplified continuous wave (cw) signal at U2-3 and routes it to the modulation circuits via C26.

1.3 Modulation Circuit, Transmitter 1,csb channel. - See schematic 120504, sheet 2. The csb modulation circuit modulates the glide slope synthesizer assembly RF with the 90 + 150 Hz audio. The modulation circuit consists of positive-intrinsic-negative (pin.) diode attenuators CR1 and CR2, low-pass filter HY1, and pin diode bridge attenuator HY3. The signal path from amplifier U2-3 is C26, CR2-cathode, CR1-anode, HY1-1, HY1-8, HY3-1, and HY3-8. There are two audio modulation inputs. One audio modulation input is at the anodes of CR1 and CR2 and the other audio modulation input is at HY3-3 and HY3-4. Pin. diode attenuators CR1 and CR2 are forward biased and, as the audio modulation on the anodes varies in amplitude, the cathode-to-anode resistance of CR1 and CR2 varies. This varying resistance (attenuation) results in amplitude modulation of the amplified cw RF signal. The modulated cw RF signal from CR1-anode is filtered by low-pass filter HY1 to remove harmonics and is further modulated by pin. diode bridge attenuator HY3. The modulated signal from HY3-8 is routed to U1-1 in the RF amplification circuit.

1.4 RF Amplification Circuit, CSB. - See schematic 120504, sheet 2. The RF amplification circuit amplifies the RF after it has been modulated. The RF amplification circuit consists of U1, Q1, and Q2. The output of the modulation circuit is amplified a normal 43 dB by three-stage amplifier U1, Q1, and Q2; filtered through a low-pass filter; and sent through a directional coupler circuit to CSB OUT connector J2. The signal to RF amplifier U1-1 is from HY3-8. Amplifier U1 is a linear class A amplifier. The amplitude-modulated signal is routed via C18 to field-effect transistor (FET) Q1, an interstage matching network (consisting of L7, C15, L4, C2, and L5) FET Q2, an output matching network (consisting of transmission line Z1, C12, C13, C6, L1, and C7), a low-pass filter (L8 and L9 and associated capacitors), a directional coupler circuit, and another low-pass filter (L11 and L6 and associated capacitors) to CSB OUT connector J2. The FET amplifiers Q1 and Q2 are N-channel insulated gate FET operating class A/B and have a nominal gain of 21 dB. Potentiometers R7 and R10 set the bias current of Q1 and Q2, respectively. The bias for Q1 is set at a nominal value of 200 milliamperes and Q2 is set at a nominal value of 1.0 ampere. These bias settings are not critical and are factory set. The bias is reset only if either Q1 or Q2 is replaced. Swamping resistors R14, R2, R3, and R11 stabilize amplifiers Q1 and Q2. Connector J5 aligns the low-pass filter and is normally jumpered from J5-1 to J5-2.

1.5 Audio Amplification Circuit. - See schematic 120504, sheets 2, and 3, and 5. The audio amplification circuit provides audio amplification for the modulation circuit. The audio amplification circuit consists of U4 and U5. The CSB CONTROL signal input to connector J4-11 is coupled via R41, potentiometer R35, audio amplifier U4, audio amplifier U5, and diodes CR10 and CR7 to the modulation circuit for modulating the RF cw signal. Diode CR10 couples the signal to the anodes of pin. diode attenuators CR1 and CR2. Diode CR7 couples the signal to pin. diode bridge attenuator HY3-3 and HY3-4 via L18 and R6. The CSB CONTROL signal contains a dc level and desired percent of modulation of 90- and 150-Hz signals. Audio amplifier U4 is an inverting amplifier with unity gain that inverts the control signals to achieve the correct phase for negative

envelope feedback. Audio amplifier U5 is the primary modulation control amplifier. Audio amplifier U5 is a summing amplifier that sums the control signal from U4-6 via summing resistor R29 and the csb feedback (CSB-FDB) via summing resistor R48. The csb feedback ensures a good reproduction of the control signal. Diode CR14 is a clamping diode and prevents the possibility of a latch up due to a positive feedback signal from U6 in the detected forward power circuit.

1.6 Detected Forward Power Circuit. - See schematic 120504, sheets 2 and 5. The detected forward power circuit samples and rectifies the transmitted power using a directional coupler circuit to give a measurement of the transmitted power. The detected forward power circuit consists of a directional coupler made up of discrete components, R17, CR5, CR8, and U6. A sample of the csb RF power, about 12 dB down in voltage from the csb signal, is coupled by the directional coupler circuit, developed across terminating resistor R17, and detected by CR5. This voltage is routed to U6-3 and the buffered output at U6-6 is used for power measurement, fault isolation, and as a feedback signal. The feedback signal (CSB-FDB) is routed via R48 to U6-2 and summed out of phase with the control signal. Diode CR8 at inverting input U6-2 is used for temperature tracking. Both diodes CR5 and CR8 are biased with identical currents through R23 and R24, respectively. The output to two pins on connector J4. One output from U6-6 goes through voltage divider R40 and R45 and is routed to J4-23 for fault isolation. Another output from U6-6 is developed across potentiometer R38 and is routed to J4-24 for forward power measurement. Potentiometer R38 is factory set.

1.7 Detected Reverse Power Circuit. - See schematic 120504, sheets 2 and 5. The detected reverse power circuit samples and rectifies the reflected transmitter power using a directional coupler circuit to give a measurement of the reflected transmitted power. The detected reverse power circuit consists of a directional coupler made up of discrete components, R13, CR4, CR9, and U7C. The detected reverse power is coupled by the directional coupler circuit, developed across terminating resistor R13, and detected by CR4. The signal is coupled via L16 to unity amplifier U7C-10. The detected reverse power is buffered by U7C and used to measure reflected power and to reduce the power output of the glide slope modulator/power amplifier assembly to nearly 0 if a very high vswr occurs. Diode CR9 at inverting input U7C-9 is used for temperature tracking. Both diodes CR4 and CR9 are biased with identical currents through R30 and R31, respectively. The output of U7C-8 is developed across potentiometer R34 and is routed to J4-22 for reverse power measurement and fault isolation. Potentiometer R34 calibrates the reverse power and is factory set.

1.8 High Voltage Standing-Wave Ratio Protection Circuit. - See schematic 120504, sheets 2 and 5. The high vswr protection circuit reduces the output power of the glide slope Modulator/Power amplifier assembly to nearly 0 to protect the Glide slope Modulator/Power amplifier assembly if an excessive vswr occurs. The high vswr circuit consists of CR21, Q6, Q4, Q3, and Q7. If the amplified detected reverse voltage at U7C-8 exceeds a limit set by voltage divider R51 and R78, Zener diode CR21 will avalanche and charge C75 to the trigger voltage of semiconductor-controlled rectifier (scr) Q6. This

latches scr Q6 on and supplies a negative voltage from the anode of Q6 to the gates of FET Q1 and FET Q2. This reduces the power output to nearly 0. The negative voltage is also coupled through CR6 and R22 and from the emitter to the collector of Q4 to J4-8 as a HIGH VSWR DET signal. The SCR, Q6 remains on until the glide slope electronic subsystem is turned off and back on or a reset occurs. The RC time constant of R79 and C75 assures that transients (such as caused by electrical storms) will not trigger SCR Q6 and cause a high vswr shutdown. A RESET signal at J4-20 is routed to the base of Q3 and turns on transistor Q3. The reset signal is inverted and coupled to the base of transistor Q7 and turns on transistor Q7. With transistor Q7 on, SCR Q6 is shunted from cathode to anode and turns off (unlatches).

1.9 Sideband-Only Circuit. - See schematic 120504, sheets 2 through 5. The sbo channel circuit receives the carrier frequency (CW RF IN) from power splitter HY2-6. The sbo channel circuit performs the required AM modulation and outputs the SBO OUT signal at SBO OUT connector J3. The SBO OUT signal is routed to the antenna via transfer switch assemblies and glide slope divider/combiner. The sbo channel circuit consists of the RF input, phase shifter, and amplifier circuit; modulation circuit; RF amplification circuit; and audio amplification, audio switch, and level detector circuits for producing the SBO OUT signal. The sbo channel circuit also includes a detected forward power circuit and detected reverse power circuit for monitoring the signals supplied to the antenna, a phase detector circuit, and a high vswr protection circuit. These circuit are discussed in the following paragraphs.

1.10 RF Input, Phase Shifter, and Amplifier Circuit. - See schematic 120504 sheets 2 through 4. The RF input and phase shifter circuit enables shifting the phase of the RF input to compensate for changes in component values and to allow pmdt (software control through external terminal) setting of the RF phase between the csb and sbo channels. The RF input and phase shifter and amplifier circuit consists of CR30, CR34, and U14. The circuit also provides amplification of the RF signal. Varactor diodes CR30 and CR34 are in series with the CW RF IN signal from power splitter HY2-6. These diodes function as variable capacitors that are electronically controlled. Diodes CR30 and CR34 are reverse biased. As the bias is varied, the capacitance is varied also. By varying the capacitance, the phase shift of the signal can be varied electronically. The bias voltage is supplied as the output of U10D-14. Amplifier U14 provides additional gain for the sbo RF signal but has the primary purpose of isolating the RF input from the modulating circuits. The CW RF IN signal from power splitter HY2-6 is routed via L27, L34, CR30-anode, CR34-cathode, and C111 to U14-1. Amplifier U14-3 and routes it to the modulation circuit via C110.

1.11 Modulation Circuit, Transmitter 1, sbo channel. - See schematic 120504, sheets 3 and 4. The sbo modulation circuit modulates the glide slope synthesizer assembly RF input with the 90 - 150 Hz audio. The sbo modulation circuit consists of pin. diode attenuators CR33 and CR32, low-pass filter HY5, and pin. diode bridge attenuator HY6. The signal path from amplifier U14-3 is C110, CR33-cathode, CR32-anode, HY5-1, HY5-8, HY6-1, and HY6-8. There are two audio modulation inputs. One audio

modulation input is at the anodes of CR33 and CR32 and the other audio modulation input is at HY6-3 and HY6-4. Pin diode attenuators CR33 and CR32 are forward biased and , as the audio modulation on the anodes varies in amplitude, the cathode-to-anode resistance of CR33 and CR32 varies. Diodes CR32 and CR33 set the level of RF to HY6. This is necessary to achieve the vary high modulation range of the sbo signal. Amplifiers U10C and U10D set the average RF level to HY6 to allow maximum modulation for a given power out. This varying resistance (attenuation) results in a modulation of the amplified cw RF signal. The modulated cw RF signal from CR32-cathode is filtered by low-pass filter HY5 to remove harmonics and is further modulated by pin. diode bridge attenuator HY6. The modulated signal from HY608 is routed to U13-1 in the RF amplification circuit.

1.12 Modulation Circuit, Transmitter 2,csb channel. - See schematic 120504, sheet 2. The csb modulation circuit for transmitter 2 modulates the glide slope synthesizer assembly RF with the 150 Hz audio. The modulation circuit is identical to Transmitter 1 and consists of positive-intrinsic-negative (pin.) diode attenuators CR1 and CR2, low-pass filter HY1, and pin diode bridge attenuator HY3. The signal path from amplifier U2-3 is C26, CR2-cathode, CR1-anode, HY1-1, HY1-8, HY3-1, and HY3-8. There are two audio modulation inputs. One audio modulation input is at the anodes of CR1 and CR2 and the other audio modulation input is at HY3-3 and HY3-4. Pin. diode attenuators CR1 and CR2 are forward biased and, as the audio modulation on the anodes varies in amplitude, the cathode-to-anode resistance of CR1 and CR2 varies. This varying resistance (attenuation) results in amplitude modulation of the amplified cw RF signal. The modulated cw RF signal from CR1-anode is filtered by low-pass filter HY1 to remove harmonics and is further modulated by pin. diode bridge attenuator HY3. The modulated signal from HY3-8 is routed to U1-1 in the RF amplification circuit. The sbo channel is again identical to Transmitter 1but the output is not used and is terminated into a 50 ohm load. This output is not routed to the antenna. Transmitter 1 and Transmitter 2 differ only in the input audio used for modulation and this terminated output (sbo out) on Transmitter 2.

1-13 RF Amplification Circuit, SBO. - See schematic 120504, sheet 4. The RF amplification circuit amplifies the RF after it has been modulated. The RF amplification circuit consists of U13 and Q9. The output of the modulation circuit is amplified by two-stage amplifier U13 and Q9, filtered through a low-pass filter, sent through a directional coupler circuit, filtered again, and output at SBO OUT connector J3. The signal to RF amplifier U13-1 is from HY6-8. Amplifier U13 is a linear class A amplifier. The amplitude-modulated signal is routed via matching network L41 and C95 to FET Q9, a matching network (consisting of L45, C93, L46, C99, and C106), a low-pass filter (L47 and L48 and associated capacitors), a directional coupler circuit, and another low-pass filter (L39 and L50 and associated capacitors) to SBO OUT connector J3. The FET amplifier Q9 is an N-channel insulated gate FET operating class A/B. Potentiometer R109 sets the bias current. The bias current is factory set. The bias is reset only of Q9 is replaced. Swamping resistors R11 and R103 stabilize transistor Q9. Connector J7 aligns the low-pass filter and is normally jumpered from J7-1 to J7-2.

1.14 Audio Amplification, Audio Switch, and Level Detector Circuits. - See schematic 120504, sheets 3 through 5. The audio amplification circuit consists of audio amplifiers U9 and U10 and audio switch U11. The level detector circuit consists of U8 and CR28 and maintains the desired level of the RF signal at SBO OUT connector J3. The 90 - 150 Hz and modulation signal from the audio generator cca is the sbo control (SBO-CRL) signal at J4-5. The SBO-CTL signal is coupled via R60, potentiometer R82, sudio amplifier U9, audio amplifiers U10B and U10A, audio switch U11, and diodes CR22 and CR23 to the modulation circuit for modulating the RF cw signal. The diodes couple the modulation to pin. diode bridge attenuator HY6-3 and HY6-4 via L32 and R110. Audio amplifier U9 is an inverting amplifier with unity gain that inverts the control signals to achieve the correct phase for negative envelope feedback. Audio amplifier U10b is the primary modulation control amplifier. Audio amplifier U10B is a summing amplifier that sums the control signal from U9-6 via summing resistor R98 and the sbo feedback (SBO-FDB) signal via summing resistor R56. The sbo feedback ensures a good reproduction of the control signal. Diode CR18 is a clamping diode and prevents a positive feedback signal from U8 in the detected forward power circuit. Amplifier U10A is an inverting amplifier with unity gain. The outputs of U10B and U10A are equal and inverted with U10B-7 output routed to audio switch U11-2 and U10A-1 output routed to U11-8. Audio switch U11 switches between these inputs to produce an output that varies above and below the 0 reference line. The switching is accomplished by a zero cross (0-CROSS) signal at U11-6 routed from the audio generator cca via J4-7. The output of U10B-7 is also routed to a level detector circuit consisting of U10C-10 is amplified, detected by CR15 and buffered at U10D-14. The output of U10D-14 is the control voltage for pin. diode attenuators CR33 and CR32.

1-15 Detected Forward Power Circuit. - See schematic 120504. The detected forward power circuit samples and rectifies the transmitted power using a directional coupler circuit to give a measurement of the transmitted power. The detected forward power circuit consists of a directional coupler made up of discrete components, R106, CR28, CR20, and U8. A sample of the sob RF power, about 12 dB down in voltage from the sbo signal, is coupled by the directional coupler circuit, developed across terminating resistor R106, and detected by CR28. This voltage is routed to U8-3 and the bufffered output at U8-6 is used for forward power measurements and fault isolation. Diode CR20 at inverting input U8-2 is used for temperature tracking. Both diodes CR20 and CR28 are based with identical currents through R77 and R76, respectively. The output of U8-6 is also output to two pins on connector J4. One output from U8-6 goes through voltage divider R74 and R81 and is routed to J4-16 for fault isolation. Another output from U8-6 is developed across potentiometer R75 and is routed to J4-15 for forward power measurement. Potentiometer R75 is factory set.

1.16 Detected Reverse Power Circuit. - See schematic 120504. The detected reverse power circuit samples and rectifies the reflected transmitter power using a directional coupler circuit to give a measurement of the reflected transmitted power. The detected reverse power circuit consists of a directional coupler made up of discrete components,

R108, CR25, and U7B. The detected reverse power is buffered by 7B and used to measure reflected power and to reduce the power output of the glide slope modulator/power amplifier assembly to nearly 0 if a very high vswr occurs. Diode CR25 at inverting input U7B-6 is used for temperature tracking. Both diodes CR29 and CR25 are biased with identical currents through R93 and R94, respectively. The output of U7B-7 is developed across potentiometer R96 and is routed to J4-19 for reverse power measurement and fault isolation. Potentiometer R96 calibrates the reverse power and is factory set.

1.17 Phase Detector Circuit. - See schematic 120504. The phase detector circuit corrects any phase errors between the csb and sbo RF signals. A coupler at both the csb and sbo RF outputs samples a portion of the RF. The phase detector circuit consists of directional coupler circuits, HY4, U3, U7A, and U7D. The csb signal is sampled by a directional coupler circuit, terminated by R8, and developed across R9. The sbo signal is sampled by a directional coupler circuit, developed across terminating resistor R112, and across R113. This RF is routed to phase detector HY4-8 and HY4-1. The phase detector error output (HY4-4 and HY4-3) is switched via U3 to produce two outputs that are amplified by differential amplifiers U7A and U7D. The switching of U3 is controlled by a ZERO CROSS signal at U3-6 from J4-7. The amplified signal drives electronic phase shifter CR30 and CR34 to correct any phase errors between the csb and sbo RF signals. Electronic phase shifter CR26 and CR27 between the sbo RF sample and the phase detector is controlled via the pmdt keyboard to set the csb-to-sbo RF phase. This is the PHASE CONTROL signal from J4-4 that is amplified by U12.

1.18 High Voltage Standing.-Wave Ratio Protection Circuit. - See schematic 120504, sheets 4 and 5. The high vswr protection circuit reduces the output power of the glide slope modulator/power amplifier assembly to nearly 0 to protect the glide slope modulator/power amplifier assembly if an excessive vswr occurs. The high vswr protection circuit consists of CR13, scr Q5, Q4, Q8, and Q3. If the amplified detected reverse voltage at U7B-7 exceeds a limit set by voltage divider R96 and R95, Zener diode CR13 will avalanche and charge C34 to the trigger voltage of scr Q5. This latches scr Q5 on and supplies a negative voltage from the anode of Q5 to the gate of Q9. This reduces the power output to nearly 0. The high negative voltage is also coupled through CR24 and R84 and from the emitter to the collector of Q4 to J4-8 as a HIGH VSWR DET signal. The scr Q5 will remain on until the glide slope electronic subsystem is turned off and back on or a reset occurs. The RC time constant of R57 and C34 assures that transients (such as caused by electrical storms) will not trigger scr Q5 and cause a high vswr shutdown. A RESET signal at J4-20 is routed to the base of Q3 and turns on transistor Q3. The reset signal is inverted and coupled to the base of transistor Q8 and turns on transistor Q8. With transistor Q8 on, scr Q5 is shunted from cathode to anode and turns off (unlatches).