AW2540 Bluetooth Low Energy module Specification

Version 1.0

2014-5-5

1.1 Introduction

The AW5240 Module is designed to be used in 2.4GHZ Bluetooth low energy solution。It enables robust BLE master or slave nodes。It base on the CC2540 IC of TI。The CC2540 combines an excellent RF transceiver with an industry-standard Enhanced 8051 MCU,in-system programable flash memory,8-KB RAM,and many other features and peripherals。It can run both application and BLE protocol stack，includes peripher als to interface with wide range of sensors。

1.2 Features

- Bluetooth Low Energy compatible
- Exellent Link Budget
- Accurate digital Received Signal-Strength Indicator
- Suitable for systems targeting compliance with worldwide radio frequency regulations
- Low power
- Wide supply voltage range（2V~3.6V）
- Integratd high-performance OP-AMP and ultralow-power comparator
- Support SPI interface
- Interrup control
- Debug interface
- General-purpose Timers
- Battery voltage monitor
- Temperature sensor
- Each CC2540 contains a unique 48-bit IEEE address

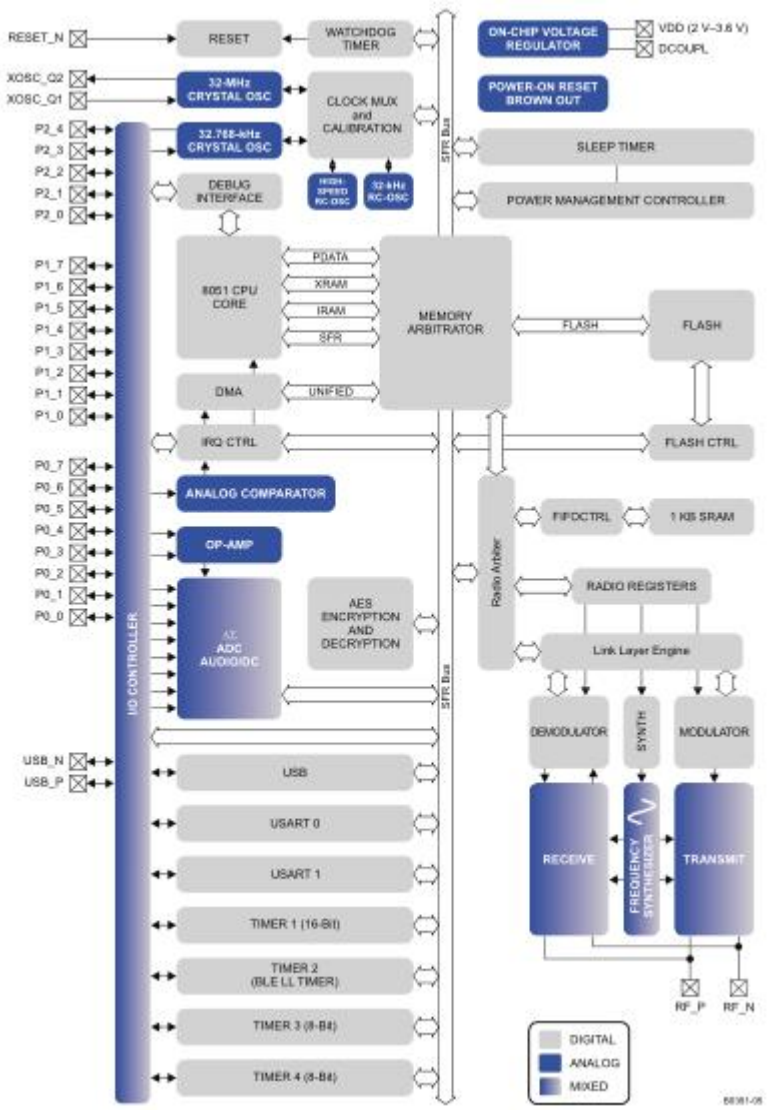
1.3 APPLICATIONS

- 2.4GHZ Bluetooth Low Energy System
- Health Care and Medical
- Sports and leisure Equiment
- Consumer Eletronics
- Human Interface Devices
- Mobile phone Accessorise
- Proximity tags

2.1 Product Information

The AW2540 is a cost-effective, low-power for Bluetooth low energy applications. It enables robust BLE master or slave nodes to be built with very low total bill-of-material costs. It combines an excellent RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful supporting features and peripherals. The AW2540 is suitable for systems where very low power consumption is required. Very low-power sleep modes are available. Short transition times between operating modes further enable low power consumption.

BLOCK DIAGRAM:



AW2540 block diagram

The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules。

CPU and Memory：

The 8051 CPU core is a single-cycle 8051-compatible core. It has three different memory access busses (SFR,DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit。

8 KB SRAM and 128/256 KB flash

Peripherals：

A versatile five-channel DMA controller is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

The debug interface implements a proprietary two-wire serial interface that is used for in-circuit debugging.Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates。

The interrupt controller services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the AW2540 back to the active mode。

2.2 Operating conditions

The operating conditions are the physical parameters that AW2540 can operate within.

	MIN	MAX	UNIT
Operating ambient temperature range, T_A	–40	85	℃
Operating supply voltage	2	3.6	V

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	VDD + 0.3, ≤ 3.9	V
Input RF level			10	dBm
Storage temperature range		–40	125	℃
ESD(2)	All pads, according to human-body model, JEDEC STD 22, method A114		2	kV
	According to charged-device model, JEDEC STD 22, method C101		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) CAUTION: ESD sensitive device. Precautions should be used when handing the device in order to prevent permanent damage.

2.3Radio characteristics

AW2540 electrical characterization is defined in Table . The operating conditions are: VDD = 3.0V, TA =25℃

RF frequency range	Programmable in 2-MHz steps	2402	2480	MHz
Data rate and modulation format	1 Mbps, GFSK, 250 kHz deviation			

RF RECEIVE SECTION

TA= 25°C, VDD = 3 V, fc= 2440 MHz，1 Mbps, GFSK, 250-kHz deviation, Bluetooth low energy mode, and 0.1% BER(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity(2)	High-gain mode		–93		dBm
Receiver sensitivity(2)	Standard mode		–87		dBm
Saturation(3)			6		dBm
Co-channel rejection(3)			–5		dB
Adjacent-channel rejection(3)	±1 MHz		–5		dB
Alternate-channel rejection(3)	±2 MHz		30		dB
Blocking(3)			–30		dBm
Frequency error tolerance(4)	Including both initial tolerance and drift	–250		250	kHz
Symbol rate error tolerance(5)		–80		80	ppm
Spurious emission. Only largest spurious emission stated within each band.	Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–75		dBm
Current consumption	RX mode, standard mode, no peripherals active, low MCU activity, MCU at 250 kHz		19.6		mA
	RX mode, high-gain mode, no peripherals active, low MCU activity, MCU at 250 kHz		22.1		

(1) 0.1% BER maps to 30.8% PER
(2) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.
(3) Results based on standard gain mode
(4) Difference between center frequency of the received RF signal and local oscillator frequency
(5) Difference between incoming symbol rate and the internally generated symbol rate

RF TRANSMIT SECTION

TA= 25°C, VDD = 3 V and fc= 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting		4		dBm
	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		–23		
Programmable output power range	Delivered to a single-ended 50 Ω load through a balun		27		dB
Spurious emissions	Conducted measurement with a 50-Ω single-ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66(1)		–41		dBm
Current consumption	TX mode, –23-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		21.1		mA
	TX mode, –6-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		23.8		
	TX mode, 0-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		27		
	TX mode, 4-dBm output power, no peripherals active, low MCU activity, MCU at 250 kHz		31.6		
Optimum load impedance	Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna		70 + j30		Ω

(1) Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

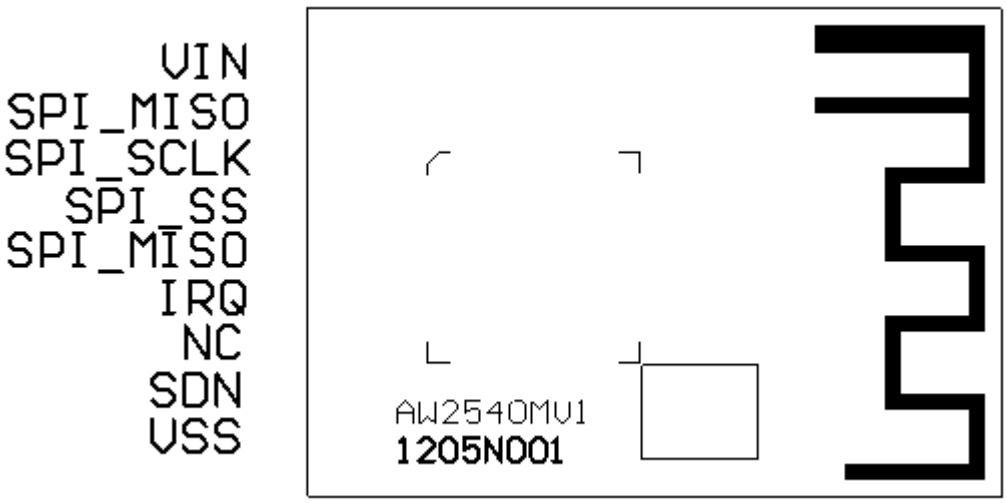
2.4ELECTRICAL CHARACTERISTICS

TA= 25°C and VDD = 3 V

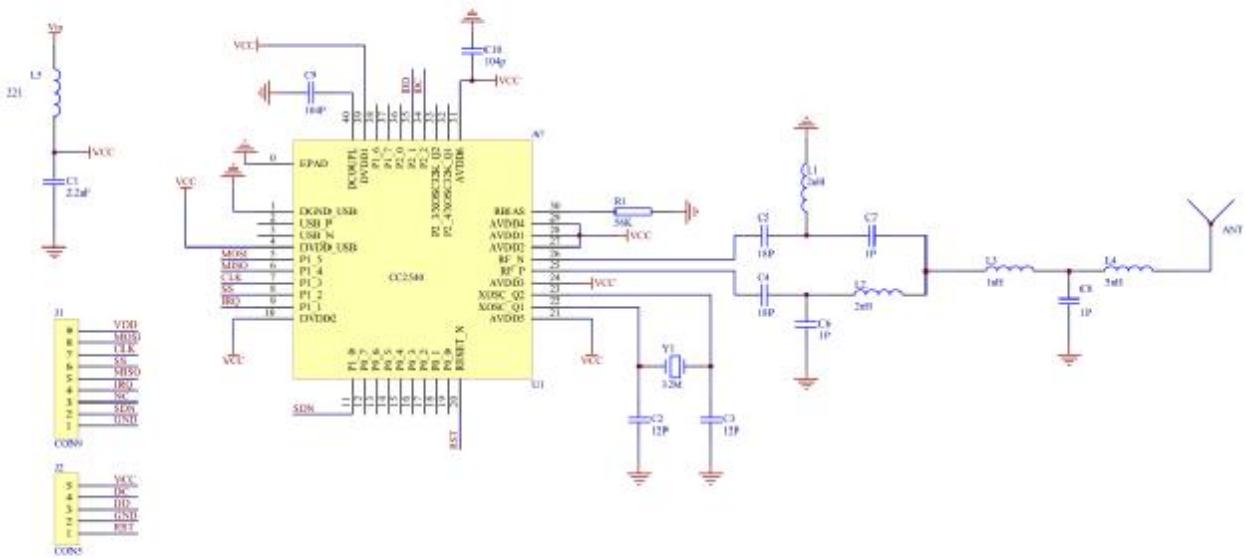
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		235		µA
		Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		0.9		
		Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.4		
		Low MCU activity: 32-MHz XOSC running. No radio or peripherals. No flash access, no RAM access.		6.7		mA
I_{peri}	Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated)	Timer 1. Timer running, 32-MHz XOSC used		90		µA
		Timer 2. Timer running, 32-MHz XOSC used		90		µA
		Timer 3. Timer running, 32-MHz XOSC used		60		µA
		Timer 4. Timer running, 32-MHz XOSC used		70		µA
		Sleep timer, including 32.753-kHz RCOSC		0.6		µA
		ADC, when converting		1.2		mA

3.1 Mechanical Information

3.2 PIN Information



3.3 module schematic

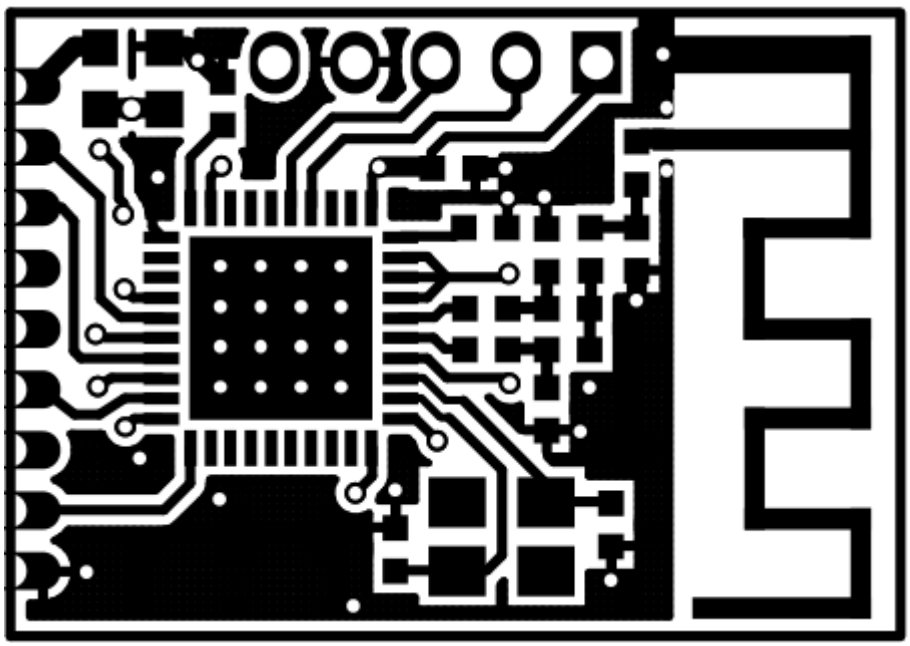


3.4 Component List

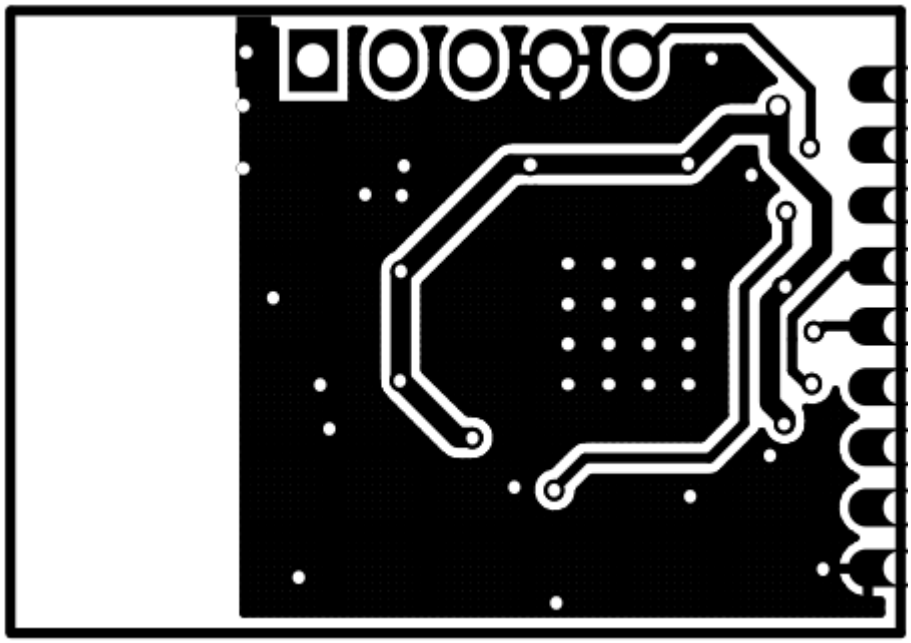
Component	Description	Value
R1	0402 Resistor	56KΩ
C1	0603 Capacitor	2.2uF
C2	0402 Capacitor	12pF
C3	0402 Capacitor	12PF
C4	0402 Capacitor	18PF
C5	0402 Capacitor	18PF
C6	0402 Capacitor	1PF
C7	0402 Capacitor	1PF
C8	0402 Capacitor	1PF
C9	0402 Capacitor	104PF
C10	0402 Capacitor	104PF
L1	0402 Inductor	2nH
L2	0402 Inductor	2nH
L3	0402 Inductor	1nH
L4	0402 Inductor	3nH
L5	0603 Bead	220Ω
X1	3225 Crystal	32MHZ
U1	IC	CC2540

3.5 Module Layout

Toplayer：



Bottomlayer：



Caution: Any changed or modifications not expressly approved by the party responsible for compliance could void the user`s authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device,pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This device should be installed and must not be co-located or operating in conjunction with any other antenna or transmitter.

The module in this product is labeled with its own FCC ID and the FCC ID is not visible when the module is installed inside another device. To satisfy FCC exterior labeling requirements, the following text must be placed on the exterior of the end product.

Contains Transmitter Module FCC ID: OU9AW2540-LS