DWHP83 Module

Digital Wireless Audio Transceiver

Preliminary Technical Product Specification

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1. DWHP83 Module

1.1. Product Description

The DWHP83 Module is an OEM module (20x40mm) based on the DARR-83. It is an uncompressed wireless digital audio transceiver operating in the 5.8GHz band. The wireless audio link supports up to 4 stereo audio streams and comes together with additional features such as: data encryption, pairing functionality, bi-directional control data messages, low power audio snooze mode, WLAN detection and Automatic Frequency Allocation. The DARR83 chip itself provides the basic functions of Audio Processing and buffering, Data Link Layer and Physical Layer. The module integrates all functionality for a wireless digital audio connection, comprising:

- DARR-83 Wireless Audio Processor
- 5.8 GHz RF Transceiver
- Embedded Antennas
- Digital audio interfaces (I^2S and/or S/PDIF)
- I^2C control interface
- 26 pins header connector for power, digital audio and control interface and GPIOs

1.2. Basic Features

1.2.1. High Quality Audio

• Up to four stereo audio channels, fully bidirectional, up to 24-bit/96 ksps uncompressed audio
• Low latency <20ms for real-time audio and lip sync
• Low latency compression algorithm - optimized for voice applications, headphones
• Inter-speaker synchronization; Low-jitter audio clock sync
• Programmable digital audio gain

1.2.2. Networking and Connectivity

• 22Mbps Bandwidth in 5.8 GHz Bands
• Point-to-Point and Point-to-Multipoint
• Bidirectional data channel (100 kbps)
• Simple Pairing and Association Function
• 4 I^2S Data pins, each provided with their own pair of BCK/LRCK signals or stereo S/PDIF input/output
• Master and Slave I2C bus for external control functions

1.2.3. Coexistence and Robustness

• Enhanced robustness against both in- and out of band interferers like: Wi-Fi and cordless phones
• Coexistence with 802.11a, b, g and n
• Automatic receiver antenna diversity minimizes fading and multi-path effects
• Link quality monitoring
• Soft audio muting under poor link circumstances

1.2.4. Power Management

• Low power consumption
• Automatic RF output power control
• Power Down Duty Cycle mode: If no link is established, modules (both TX and RX) will enter power down mode

1.2.5. Integrated 8052 MCU

The DARR83 integrates an 8052 MCU. This includes the following features:
• 45 kByte Code RAM
• 8 kByte Data RAM
• 4 Timer/Counters
• UART

1.2.6. Digital Audio Clock Synchronization

The digital audio clock synchronization is an additional more cost effective method for synchronization of audio samples on the receiving side with respect to the transmitted audio samples. The digital clock synchronization feature works for output audio sample rates of 96 and 48 ksps.

2. DWHP83 Module Specifications

System Specifications				
ID	**Parameter**	**Value**	**Unit**	**Remarks**
RF Characteristics				
	RF frequency range	5736 - 5814	MHz	
	Number of RF channels	3		In each Frequency band.
Air framing				
	Addressing	24	Bit	
	Data message size	32	Byte	Application dependent
	CRC	16, 24 and 32	Bit	Hybrid
Control				
	Control interface	I^2C		Compliant with the I^2C protocol (slave), 0…400kbps. Base address 0x80.
Data				
	Data Bandwidth	100	Kbps	Bi-directional wireless data channel
	Data latency	5	ms	Minimum under good RF link conditions for applications that support the 100kbps data rate.
Interference Robustness				
	Fixed frequency devices (e.g. WLAN, microwave oven)			Fully coexistent[1]
	Frequency hopping devices (e.g. 5.8GHz cordless phones)			Fully coexistent[1]

[1] Laboratory tests have verified coexistence with interference sources collocated. Exact ranges are scenario dependent (function of latency, output power, audio compression, etc.). A mix of interference sources is allowed. Interference of fixed frequency devices may result in the loss of one useable RF channel.

Audio Interface				
	Available Interface Types	I^2S		Can be used simultaneously Incl. S/PDIF detection.
Audio Quality				
	Sample rate	48	ksps	
	Sample width	16 or 24	bit	
	Latency	20	ms	Configurable from 10 to 23.6ms, depending on the application.
	Dynamic Range	98 146	dB dB	16 bit 48ksps, A-weighted 24 bit 48ksps, A-weighted
	THD+N	-96 -143	dB dB	16 bit 48ksps 24 bit 48ksps
	Frequency response	0	dB	20Hz…22kHz [2]
Dimensions				
	Board dimensions	20 x 40	mm	

[2] In applications where Digital Clock Sync is not used.

2.1. Absolute Maximum Rating

Symbol	Parameter	Min.	Typ	Max	Unit
VCC	Supply Voltage			3.8	V
$T_{storage}$	Storage Temperature	-25	−	85	°C
V_{ESD}	ESD Contact Discharge	-3	−	+3	kV

2.2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
VCC	Supply Voltage		3.3		V
VCC Ripple	Peak to Peak Ripple (In-circuit)	−	0	100	mV
T_{amb}	Operating Temperature	-10	25	60	°C

2.3. DC Characteristics

All digital IO levels are 3.3V CMOS. The digital IO ports are not 5V compliant.
Please refer to datasheet of DARR83 for more information.

2.4. Connector Electrical Rating

Item	Parameter	Max	Units
Max. Rated Voltage	AC (RMS) / DC	500	V
Max. Rated Current	AC (RMS) / DC	1	A

2.5. Pin out of 26pin header Connector

26 Ways, Male Type Pin Header, 1.27mm pitch, SMT type:

Pin Number	Pin Name	I/O	Description
1	VDD	Power	Regulated 3.3V Input
2	GND	Ground	Ground
3	MCLK	In	12.288 audio clock In
4	DARR83_GPIO_2	I/O	Configurable. Please refer to the DARR83 datasheet
5	DARR83_GPIO_7	I/O	Configurable. Please refer to the DARR83 datasheet
6	DARR83_GPIO_4	I/O	Configurable. Please refer to the DARR83 datasheet
7	DARR83_GPIO_23	I/O	Configurable. Please refer to the DARR83 datasheet
8	DARR83_GPIO_13	I/O	Configurable. Please refer to the DARR83 datasheet
9	DARR83_GPIO_3	I/O	Configurable. Please refer to the DARR83 datasheet
10	DARR83_GPIO_15	I/O	Configurable. Please refer to the DARR83 datasheet
11,12, 23	GND	Ground	Ground
13	DARR83_GPIO_24	I/O	Serial Async Data,for test purposes
14	DARR83_GPIO_14	I/O	Not Applicable
15	DARR83_GPIO_16	I/O	Configurable. Please refer to the DARR83 datasheet
16	NC		
17	DARR_/RST	In	Active low. Should be connected to a reset IC or to a pull-up resistor with a capacitor to ground.
18	I2C_SCL_SLV	I/O	I^2C serial clock Slave
19	I2C_SDA_SLV	I/O	I^2C serial data Slave
20	DARR83_GPIO_12 (SDIO_Z)	I/O	I^2S port Z serial data
21	DARR83_GPIO_11_SDIO_X	I/O	I^2S port X serial data
22	DARR83_GPIO_10_LRCK_W	I/O	I^2S Left Right Clock
24	DARR83_GPIO_8_BCK_W	I/O	I^2S Bit Clock
25	DARR83_GPIO_6_SDIO_Y	I/O	I^2S port Y serial data
26	DARR83_GPIO_5_SDIO_W	I/O	I^2S port W serial data

Note1: the digital IO pins are CMOS 3V3 compliant and not 5V compliant.

2.6. Antennas

The module uses embedded PCB track Dual-Band antennas. RX and TX diversity antennas are used to avoid dropouts due to multipath fading.

- Antenna A (ANT A) fixed track antenna on the module
- Antenna B (ANT B) fixed track antenna on the module