

## Chapter 4 Circuit Descriptions

### 4.0 (A1) UHF Exciter Assembly (1278-1400; Appendix C)

The (A1) UHF Exciter Assembly contains (A1) a UHF Exciter Tray (1142458 or 1245-1100), (A4 & A5) two Variable Gain/Phase Trays (1245-1200), (A6) a Metering Panel (1136811 or 1245-1400), (A7) a UHF Receiver Tray (1142479 or 1265-1100), (A8) an Exciter AC Distribution Assembly (1245-1500) and (A9) a Remote Interface Assembly (1245-1801).

The (A7) UHF Receiver Tray, uses the ON Channel RF input, at J5 for 75Ω or J1 for 50Ω, and produces a Combined IF output at J4 that connects to the UHF Exciter at J6.

The (A1) UHF Exciter Tray, if the Optional Modulator Kit is present in the tray, takes the Baseband Audio and Video Inputs and mixes them with internally generated 45.75 MHz and 41.25 MHz Ifs that combines them. The Combined IF, from the Receiver Tray or from the Modulator Kit, is upconverted to the On Channel RF output frequency by mixing it with a L.O. signal generated by the Channel Oscillator Assembly. The RF Output of the UHF Exciter at J15 connects to (A3) a Splitter which splits the RF two ways with the RF Output #1 connected to the input of the (A5) Variable Gain/Phase Tray (1245-1200) and the RF Output #2 connected to the input of the (A4) Variable Gain/Phase Tray (1245-1200). The output of the (A4) Variable Gain/Phase Tray connects to (A2) the Side A Amplifier Array Assembly. The output of the (A5) Variable Gain/Phase Tray connects to (A3) the Side B Amplifier Array Assembly.

### 4.0.1 Control and Status

The Control and Status of the Translator are provided by the Meter indications on the Metering Panel and the Variable Gain Phase Trays. There are also Control, Status and LED Indications located on the front panel of the UHF Exciter Tray. The switches and LED indicators, which are mounted so that the switches and LEDs are operated or viewed from the front Panel of the UHF Exciter, are part of the Transmitter Control Board (1245-1101). On the UHF Exciter Tray, switch (S1) is an Operate/Standby Switch that provides the Operate Commands (Enables), when in Operate, to each of the Amplifier Arrays. The power supply Enable is needed to turn on the Switching Power Supplies located in each of the UHF Amplifier Trays. The Fan Enable is needed to turn on the exhaust fan in the (Optional) External Exhaust Kit. When the UHF Exciter is in Operate, the Green LED (DS2) is On and when in Standby the Amber LED (DS1) is On. **NOTE:** If the Translator does not switch to Operate, when S1 is switched to Operate, check that a Dummy Jumper Plug is connected to Jack J7, with a Jumper between Pins 1 & 2, located on (A9) the Remote Interface Assembly in the Single UHF Exciter Assembly. The Jumper provides the Interlock to the UHF Exciter needed for the operation of the Translator. If the Interlock is present, the Green LED (DS5), located on the Transmitter Control Board, should be lit.

Operation of the Translator is controlled by the front panel switches located on the UHF Exciter Tray. During Normal operation of the Translator, Switch S2 should be in the Auto position. The front panel of the UHF Exciter also has LEDs that indicate a Video Fault (Loss),

Red LED (DS9) and a VSWR Cutback, Amber LED (DS7).

#### 4.0.2 RF, Baseband Input and Remote Connections

The RF, Baseband Video and Audio Inputs to the Translator, connect to the (A9) Remote Interface Panel located on the rear of the Single UHF Exciter Assembly. The On Channel RF input connects to the "F" connector J3 for 75Ω or the "N" connector J1 for 50Ω. If the (Optional) Modulator Kit is present, the Baseband Video Input connects to Jack J2 that is wired to J1 on the Exciter. The Baseband Audio Input connects to the Terminal Block TB1 for Balanced Audio or to Jack J6 that is wired to J3 on the Exciter, for Composite, Stereo, Audio.

Remote Monitoring and Operation of the Translator is provided through the Jacks (J8, J9 & J10) located on (A9) the Remote Interface Assembly mounted toward the rear of the Single UHF Exciter Assembly. Jack (J7) should have a dummy plug connected to it, which has a jumper connected between Pins 1 & 2, that provides the Interlock to the Exciter needed to operate the Translator. If the Jumper is missing, the Translator will not switch to Operate. If remote connections are made to the Translator they should be made through the plugs provided in the Installation Material as noted on the Interconnect Drawing (1278-8400) for the Single UHF Exciter.

#### 4.0.3 AC Input

The Single UHF Exciter Assembly needs an AC input of 208/240 VAC at 20 Amps. The AC Input to the Single UHF Exciter Assembly connects to (A8) the AC Distribution Assembly, UHF Exciter Assembly (1245-1500) located in the right, center rear of the Cabinet. The Assembly contains the 4 Terminal Block (TB1) to which the 208/240 VAC connects. Line 1 to TB1-1A, Line 2 to

TB1-3A and Safety Ground to TB1-2A. The AC Distribution Panel contains CB1 one 20 Amp Circuit Breaker that supplies the AC to the rest of the Single Exciter Assembly.

The Input AC is connected to (CB1) the Main AC Circuit Breaker (20 Amps). The output of CB1 has three MOVs, VR1 connected from Line 1 to ground, VR2 connected from Line 2 to ground and VR3 connected across the two legs. The AC output of CB1 connects to A1 and A2 that are IEC Outlet Strips. The (A1) Exciter Tray and the (A4) Variable Gain/Phase Tray plug into the (A1) IEC Outlet Strip. The (A5) Variable Gain/Phase Tray, the (A8) Metering Panel and the (A7) Receiver Tray plug into the (A2) IEC Outlet Strip.

When the Circuit Breaker CB1, mounted on the AC Distribution Assembly, is switched On, +12 VDC from the Exciter, is supplied to the two Amplifier Arrays for the operation of the LED Status Indicators in each of the UHF Amplifier Trays. The +12 VDC is also connected to the (Optional) External Exhaust Kits in each of the Amplifier Arrays, if purchased.

#### 4.1 (A7) UHF/VHF Receiver (1142479 or 1265-1100; Appendix C)

The UHF/VHF Receiver Tray w/(Optional) Frequency Correction selects the desired UHF or VHF On Channel Input Signal and converts it to a Combined IF Signal of 45.75 MHz Visual + 41.25 MHz Aural. The Tray also has provisions for a Frequency Correction Option that consists of a VCXO Channel Oscillator Assembly with a PLL Circuit which maintains an exact IF Output Frequency, over the capture range of the PLL circuit, even if the Input UHF or VHF frequency varies.

## **RF Signal Path**

### **4.1.1 (A7) 50Ω Filter, DC Multiplexed, UHF (1035-1204), VHF L.B. (1035-1902) or VHF H.B. (2065-1024) or 75Ω, UHF (1035-1207), VHF L.B. (1035-1903) or VHF H.B. (2065-1023); Appendix D)**

The RF Input to the Tray, (-61 dBm to -16 dBm in Level), is fed through J1 for 50Ω to (A7) the input 50Ω Filter, DC Multiplexed (1035-1204 UHF, 1035-1902 VHF LB or 2065-1024 VHF HB) or through J5 for 75Ω to (A7) the 75Ω input Filter, DC Multiplexed (1035-1207 UHF, 1035-1903 VHF LB or 2065-1023 VHF HB), which is of a double tuned design that is adjusted to the desired Input UHF or VHF Channel Frequency. Note: If the input signal is greater than -25dBm, an attenuator should be used to limit the level to -25dBm. +12 VDC, for use by an (Optional) external Preamplifier Assembly, connects to the filter through F1 a 1 Amp Fuse. This +12 VDC is DC Multiplexed onto the input signal cable from the Preamplifier. DS1 a Red LED located on TB1 in the Tray will be lit if the +12 VDC is present on the input cable. If a Preamplifier is not used, F1 should be removed and DS1 should not be lit.

### **4.1.2 (A8) Dual Stage Amplifier Assembly (1227-1503) ; Appendix D)**

The signal is next amplified +12 dB to approximately the -49 to -4 dBm level by a low noise amplifier located on (A8-A1) the Dual Stage Amplifier Board (1227-1501) that is contained in (A8) the Dual Stage Amplifier Assembly (1227-1503). The board has approximately +13 dB or +26 dB of gain, depending on whether Jumper W1 on J5 is in place. The amplified output connects out of the board at J2.

### **4.1.3 (A9) Channel Filter, UHF (1007-1101), VHF L.B. (1034-1202) or VHF H.B. (2065-1000) ; Appendix D)**

The signal is then filtered in (A9) a Channel Filter (1007-1101 UHF, 1034-1202 VHF LB or 2065-1000 VHF HB) and then applied back to (A8-A1) the Dual Stage Board at J3.

More amplification of the signal takes place on the Dual Stage Board, if needed. Jumper W1 on J7 should be removed if the Receiver Input level is greater than -40dBm.

### **4.1.4 (A10) Downconverter Amplifier Assembly, 45.75 MHz. (1227-1505) ; Appendix D)**

The output is connected to (A10) the Downconverter Amplifier Assembly (1227-1505) that contains (A10-A1) the Downconverter Amplifier Board (1227-1502). The RF, at the -47 dBm to -2 dBm Level, connects to the "R" Input Jack of the Mixer Z1 located on the Downconverter Amplifier Board.

## **Local Oscillator Signal Path**

The Local Oscillator Signal is derived from a cut to channel crystal mounted in an oven that is factory set at 45° C. The Oscillator operates at 1/8 for UHF, 1/4 for VHF High Band or 1/2 for VHF Low Band of the desired local oscillator frequency.

### **4.1.5 (A4) Channel Oscillator Assembly (1145-1202) ; Appendix D)**

The crystal is mounted on (A4-A1) the Channel Oscillator Board, Dual Oven (1145-1201), that is part of the Channel Oscillator Assembly (1145-1202). The oscillator circuitry is a modified Colpitts design operating in a separate oven set at 50° C. for improved stability. If the Frequency Correction Option is purchased, the

VCXO Channel Oscillator Assembly (1145-1206), which contains the VCXO Channel Oscillator Board (1145-1204), is used in place of the standard Channel Oscillator Assembly, and an AFC voltage from the PLL circuit maintains the frequency of the VCXO.

**4.1.6 (A5-A1) x8 Multiplier Board (1227-1002), x2 Multiplier Board (1227-1524) or x4 Multiplier Board (1227-1525) ; Appendix D)**

The output of the Channel Oscillator is connected to the (A5-A1) the x8 Multiplier Board (1227-1002) for UHF, the x4 Multiplier Board (1227-1525) for VHF HB or the x2 Multiplier Board (1227-1524) for VHF LB, which is located in (A5) the Multiplier Enclosure (1265-1125). The proper multiplier board takes the output of the Channel Oscillator (+3 dBm) and multiplies it eight, four or two times by a series of three, two or one x2 Broadband Doublers ( $2 \times 2 \times 2 = x8$ ), which produces the L.O. signal on the desired frequency needed for the upconversion process. The signal is then amplified to the +16 dBm level. A sample of the multiplied L.O. Signal is fed to a detector circuit which lights the Green LED DS1 that indicates that the L.O. is present at the Output Jack J2 of the Multiplier Board. This Green LED is seen through a hole the lid of the Multiplier Assembly and is an indication, when lit, that there is a signal present at the output of the Multiplier Board.

**4.1.7 (A6) L.O. Filter, UHF (1007-1101), VHF L.B. (1034-1211) or VHF H.B. (2065-1000) ; Appendix D)**

The L.O. signal is filtered in (A6) a L.O. Filter 1007-1101 UHF, 2065-1000 VHF HB or 1034-1211 VHF LB) and then sent (+15 dBm) to J2 on (A10-A1) the Downconverter Amplifier Board.

The L.O. Input to the Downconverter Amplifier Board is connected thru a 3 dB matching pad to the "L" Input of the Mixer (Z1) at a +12 dBm level.

**Combined IF Signal Path**

The L.O. and the RF signals are mixed in the Mixer Stage of the Downconverter Amplifier Board to produce the desired IF difference frequency at -55 dBm to -10 dBm in level, depending on the RF Input Level.

**4.1.8 (A11-A1) IF Filter/ALC Board (1227-1504) ; Appendix D)**

The Combined IF Signal is routed to (A11-A1) the IF Filter/ALC Board (1227-1504), which is mounted in (A11) the IF Filter/ALC Enclosure (1265-1105). The IF Filter/ALC Board contains a Pin Diode Attenuator circuit which is part of the Automatic Level Control (ALC) that controls the level of the IF Signal to the two stage amplifier ICs U1 and U2.

**4.1.9 (A11-A2) (Optional) SAW Filter/Amplifier Board (1035-1211) ; Appendix D)**

The (Optional) (A11-A2) SAW Filter/Amplifier Board (1035-1211) is also contained in the IF Filter/ALC Enclosure. The SAW Filter/Amplifier Board connects to J5 and J6 of the IF Filter/ALC Board if more attenuation of the Out Of Band products is needed. If the SAW Filter/Amplifier Board is not needed, a jumper connects the Combined IF from J5 to J6 on the IF Filter/ALC Board.

The Combined IF is then bandpass filtered to the needed 6 MHz IF bandwidth around the 41.25 MHz + 45.75 MHz Combined IF signal and amplified by U3 to the -41 dBm to +4 dBm Level before it is split. One output is detected by U4 for use as the ALC reference level to the Pin Diode Attenuator Circuit. The ALC

comparator drives the Pin Diode Attenuator Circuit to maintain the desired output level, typically +2 dBm. The other split output connects to J2 the Combined IF Output of the board that is cabled to the IF Output Jack of the Tray at J4 (+2 dBm).

#### **Frequency Correction Option**

If the Frequency Correction Option (1227-1528) is purchased, (A13) the IF Filter/Limiter Board (1109-1001), (A14) the IF PLL Board (1109-1002), the (A15) IF Carrier Oven Oscillator Board (1100-1206), (A4) the VCXO Channel Oscillator Assembly (1145-1206) and (A16) an IF Amplifier Board, High Gain (1197-1126) are part of the System.

#### **4.1.10 (A13) (Optional) IF Amplifier Board (1197-1126) ; Appendix D)**

A Sample of the amplified and ALC controlled signal from the IF Filter/ALC Board is directed to the IF Amplifier Board, High Gain (1197-1126) where it is amplified and connected to J2 on (A13) the IF Filter/Limiter Board (1109-1001).

#### **4.1.11 (A13) (Optional) IF Filter/Limiter Board (1109-1001) ; Appendix D)**

The IF is filtered by a SAW Filter, which passes Visual Carrier and Aural Carrier only, and amplified before it is split. The Aural IF Output is not used in this Tray. The other output of the splitter is amplified and applied to a Notch Filter. The Notch Filter is tuned to the Aural Frequency by C17 and R10 which reduces or eliminates the Aural IF from the Visual IF signal. The Visual IF Only signal then connects to a video detector circuit which in conjunction with U5 strips the video from the Visual IF signal. The IF CW Signal is amplified and buffered before it is connected to the output of the board at J6. The IF

CW connects to J2 of (A14) the IF PLL Board (1109-1002).

#### **4.1.12 (A14) (Optional) IF PLL Board (1109-1002) ; Appendix D)**

The IF CW Signal (+3 dBm) on the IF PLL Board is wired to U1 a Divider IC which, in conjunction with U2, sets up one of the reference signals to the comparator circuit. The other reference signal is derived from the 50 kHz reference Input at J4 which is a divided down 50 kHz sample of the 38.9 MHz signal generated on (A15) the IF Carrier Oven Oscillator Board (1100-1206).

#### **4.1.13 (A15) (Optional) IF Carrier Oven Oscillator Board (1100-1206) ; Appendix D)**

The 38.9 MHz IF Carrier Oven Oscillator Board is used instead of the 45.75 MHz IF Carrier Oven Oscillator Board to minimize the interference between the generated 45.75 MHz IF and the signal generated on the (A15) IF Carrier Oscillator Board. The 38.9 MHz signal itself is not used, just the divided down 50 kHz reference of the 38.9 MHz Signal is used. The two reference signals applied to the IF PLL Board are compared by U2 and a difference voltage (AFC) is produced. The difference voltage (AFC), approximately -3 VDC, is fed from J3 of the board to FL2 of (A4) the VCXO Assembly. If the frequency of the VHF or UHF Input to the Tray should drift, the ALC voltage will change to increase or decrease the output frequency of the VCXO Assembly which increases or decreases the L.O. Frequency that maintains the IF Frequency at the standard 45.75 + 41.25 MHz Frequency. If the frequency of the Input Signal should drift out of the capture range of the PLL Circuit, DS1 the Red LED Unlock Indicator, located on the IF PLL Board, lights.

### **Voltages for Operation of the Tray**

The AC input to the Tray is 117 VAC or 230 VAC and is directed thru Jack J2, of the (A1) Power Entry Module (1265-1104), to the step down Toroid (A2). The Power Entry Module contains an On/Off Switch, a 4 Amp Slo-Blo Fuse and three MOVs which protect the Tray from transients or surges which may occur on the AC Input Lines. When the On/Off Switch is switched On, AC is applied to the (A2) Toroid. The Toroid steps down the voltage into two 16 VAC outputs which are fed to (A3) the +12V(3A)/-12V Power Supply Board (1092-1206).

#### **4.1.14 (A3) +12V(3A)/-12V Power Supply Board (1092-1206) ; Appendix D)**

The 16 VAC Inputs are connected to the two full wave bridge networks one for +12 VDC and one for -12 VDC. The output of the +12 VDC rectifier is fed to three 7812 IC regulators (U1, U2 and U3) and the output of the -12 VDC rectifier is fed to one 7912 IC regulator (U4). The  $\pm 12$ V Power Supply Board provides the voltage regulated and current limited +12 VDC and -12 VDC to the rest of the boards in the Tray.

#### **+12VDC for External Preamplifier**

+12 VDC is also applied through a 1 Amp Fuse F1 to (A7) the input DC Multiplexed UHF or VHF Filter. The +12 VDC is multiplexed in the Filter onto the input coaxial cable that connects from the (Optional) Remote Preamplifier Unit to the Receiver Tray. This supplies the Preamplifier with the +12 VDC needed for operation. The Red LED DS1 mounted on the Terminal Block TB1 will be lit if the +12 VDC is applied to the coaxial cable. **Note:** If the Red LED, DS1, is lit, the +12 VDC may damage Test Equipment that is connected to the input of the Receiver Tray. If a Preamplifier Assembly is not part of your System, F1 should be removed,

therefore DS1 should not be lit and the +12 VDC is not multiplexed onto the input coaxial cable. A spare Fuse for F1 is supplied and stored near the fuse holder for F1.

### **4.2 (A4) UHF Exciter (1245-1100; Appendix C)**

#### **4.2.1 (A4) (Optional) Aural IF Synthesizer Board, 4.5 MHz (1265-1303; Appendix D)**

The aural IF synthesizer board amplifies each of the three possible audio inputs and the amplifier circuits that supply the single audio output. The balanced audio or the composite audio input is connected to the board while the subcarrier audio (SCA) input can be connected at the same time as either of the other two inputs. The board has the 4.5-MHz voltage-controlled oscillator (VCO) and the aural modulation circuitry that produces the modulated 4.5-MHz output. The board also contains a phase lock loop (PLL) circuit that maintains the precise 4.5-MHz separation between the aural (41.25 MHz) and the visual (45.75 MHz) IF frequencies.

##### *4.2.1.1 Balanced Audio Input*

The first of the three possible baseband inputs to the board is a 600- $\Omega$ , balanced-audio input (+10 dBm) that enters through jack J2, pins 1 (+), 2 (GND), and 3 (-), and is buffered by U1B and U1C. Diodes CR1 to CR4 protect the input stages of U1B and U1C if an excessive signal level is present on the input leads of jack J2. The outputs of U1B and U1C are applied to differential amplifier U1A; U1A eliminates the common mode signals (hum) on its input leads. A pre-emphasis of 75 ms is provided by R11, C11, and R10 and can be eliminated by removing jumper W5 on J5. The signal is then applied to amplifier U1D whose gain is controlled

by jumper W3 on J11. Jumper W3 on jack J11 is positioned according to the input level of the audio signal (0 or +10 dBm). If the input level is approximately 0 dBm, the mini-jumper should be in the high gain position between pins 1 and 2 of jack J11. If the input level is approximately +10 dBm, the mini-jumper should be in low gain position between pins 2 and 3 of jack J11. The balanced audio is then connected to buffer amplifier U2A whose input level is determined by the setting of balanced audio gain pot R13. The output of the amplifier stage is wired to the summing point at U2D, pin 13.

#### 4.2.1.2 Composite Audio Input

The second possible audio input to the board is the composite audio (stereo) input at BNC jacks J3 and J13. The two jacks are loop-through connected; as a result, the audio can be used in another application by connecting the unused jack and removing W4 from J12. Jumper W4 on jack J12 provides a  $75\Omega$ -input impedance when the jumper is between pins 1 and 2 of jack J12 and a high impedance when it is between pins 2 and 3. Diodes CR9 to CR12 protect the input stages of U6A and U6B if an excessive signal level is applied to the board. The outputs of U6A and U6B are applied to differential amplifier U2C, which eliminates common mode signals (hum) on its input leads. The composite input signal is then applied to amplifier U2B; the gain of this amplifier is controlled by composite audio gain pot R17. The composite audio signal is connected to the summing point at U2D, pin 13.

#### 4.2.1.3 Subcarrier Audio Input

The third possible input to the board is the SCA input at BNC jack J4. The SCA input has an input impedance of  $75\Omega$  that can be eliminated by removing jumper W2 from pins 1 and 2 of J14. The SCA input is bandpass filtered by

C66, C14, R22, C15, C67, and R23 and is fed to buffer amplifier U3A. The amplified signal is then applied through SCA gain pot R24 to the summing point at pin 13 of U2D.

#### 4.2.1.4 Audio Modulation of the VCO

The balanced audio, or the composite audio and/or the SCA-buffered audio signals, are fed to the common junction of resistors R14, R20, and R27 that connect to pin 13 of amplifier U2D. The output audio signal at pin 14 of U2D is typically .8 Vpk-pk at a  $\pm 25$ -kHz deviation for balanced audio or .8 Vpk-pk at  $\pm 75$ -kHz deviation for composite audio as measured at TP1. This signal is applied to VCO U10. A sample of the deviation level is amplified, detected by U7A and U7B, and connected to J10 on the board. This audio-deviation level is connected to the front panel meter through the transmitter control board.

The audio is connected to CR13 to CR16; these are varactor diodes that frequency modulate the audio signal onto the generated 4.5-MHz signal in U10. U10 is the 4.5-MHz VCO that generates the 4.5-MHz continuous wave (CW) signal. The output frequency of this signal is maintained and controlled by the correction voltage output of U5 PLL integrated circuit (IC). The audio-modulated, 4.5-MHz signal is fed to amplifiers U11A and U11B. The output of U11B is connected to the 4.5-MHz output jacks at J7 and J8.

#### 4.2.1.5 Phase Lock Loop (PLL) Circuit

A sample of the signal from the 4.5-MHz aural VCO at the output of U11A is applied to PLL IC U5 at the  $F_{in}$  connection. In U5, the signal is divided down to 50 kHz and is compared to a 50-kHz reference signal. The reference signal is a divided-down sample of the visual IF, 45.75-MHz signal that is applied to the oscillator-in connection on the PLL chip through jack J6 on the board. These two 50-kHz signals are

compared in the IC and the  $f_V$ , and  $f_R$  is applied to the differential amplifier U3B. The output of U3B is fed back through CR17 to the 4.5-MHz VCO IC U10; this sets up a PLL circuit. The 4.5-MHz VCO will maintain the extremely accurate 4.5-MHz separation between the visual and aural IF signals; any change in frequency will be corrected by the AFC error voltage.

PLL chip U5 also contains an internal lock detector that indicates the status of the PLL circuit. When U5 is in a "locked" state, pin 28 goes high and causes the green LED DS1 to illuminate. If the 4.5-MHz VCO and the 45.75-MHz oscillator become "unlocked," out of the capture range of the PLL circuit, pin 28 of U5 will go to a logic low and cause the red LED DS2 to light. A mute output signal from Q3 (unlock mute) will be applied to jack J9. This mute is connected to the transmitter control board.

#### 4.2.1.6 Voltage Requirements

The  $\pm 12$  VDC needed for the operation of the board enters through jack J1. The +12 VDC is connected to J1-3 and filtered by L2, C3, and C4 before it is connected to the rest of the board. The -12 VDC is connected to J1-5 and filtered by L1, C1, and C2 before it is connected to the rest of the board. The +12 VDC is connected to U8 and U9; these are 5-volt regulator ICs that provide the voltage to the U10 and U5 ICs.

#### 4.2.2 (A5) (Optional) Sync Tip Clamp/ Modulator Board (1265-1302; Appendix D)

The sync tip clamp/modulator board is made up of five circuits: the main video circuit, the sync tip clamp circuit, the visual modulator circuit, the aural IF mixer circuit, and the diplexer circuit.

The sync tip clamp/modulator board takes the baseband video or 4.5-MHz

composite input that is connected to the video input jack (either J1 or J2, which are loop-through connected) and produces a modulated visual IF + aural IF output at output jack J20 on the board. The clamp portion of the board maintains a constant peak of sync level over varying average picture levels (APL). The modulator portion of the board contains the circuitry that generates an amplitude-modulated vestigial sideband visual IF signal output that is made up of the baseband video input signal (1 Vpk-pk) modulated onto an externally generated 45.75-MHz IF carrier frequency. The visual IF signal and the aural IF signal are then combined in the diplexer circuit to produce the visual IF + aural IF output that is connected to J20, the IF output jack of the board.

#### 4.2.2.1 Main Video Signal Path (Part 1 of 2)

The baseband video or the 4.5-MHz composite input connects to the board at J2. J2 is loop-through connected to J1 and terminated to 75 watts if jumper W4 is on jack J3. With jumper W4 removed, the input can be connected to another translator through J1; J1 is loop-through connected to J2.

Test point TP1 is provided to monitor the level of the input. The input is fed to the non-inverting and inverting inputs of U1A, a differential amplifier that minimizes any common-mode hum that may be present on the incoming signal. Diodes CR1 to CR4 form a voltage-limiter network in which, if the input voltages exceed the supply voltages for U1A, the diodes conduct, preventing damage to U1A. CR1 and CR3 conduct if the input voltage exceeds the negative supply and CR2 and CR4 conduct if the input voltage exceeds the positive supply voltage.

The video output of U1A is connected to J22 on the board. Normally, the video at J22 is jumpered to J27 on the



board. If the 4.5-MHz composite input kit is purchased, the 4.5-MHz composite signal at J22 connects to the external composite 4.5-MHz filter board and the 4.5-MHz bandpass filter board. These two boards provide the video-only signal to J27 and the 4.5-MHz intercarrier signal to J28 from the 4.5-MHz composite input. The video through video gain pot R12 (adjusted for 1 Vpk-pk at TP2) connects to amplifier U1B.

The output of U1B, if the delay equalizer board is present in the tray, connects the video from J6, pin 2, to the external delay equalizer board and back to the sync tip clamp/modulator board at J6, pin 4. If the delay equalizer board is not present, the video connects through jumper W1 on J5, pins 1 and 2. The delay equalizer board plugs directly to J6 on the sync tip clamp/modulator board. The video from J6, pin 4, is then connected through jumper W1 on J5, pins 2 and 3, to amplifier Q1. The output of Q1 connects to Q2; the base voltage of Q2 is set by the DC offset voltage output of the sync tip clamp circuit.

#### 4.2.2.2 Sync Tip Clamp Circuit

The automatic sync tip clamp circuit is made up of U4A, Q7, U3B, and associated components. The circuit begins with a sample of the clamped video that is split off from the main video path at the emitter of Q3. The video sample is buffered by U3A and connected to U4A. The level at which the tip of sync is clamped, approximately -1.04 VDC as measured at TP2, is set by the voltage-divider network connected to U4A. If the video level changes, the sample applied to U4A changes. If jumper W7 on J4 is in the Clamp-On position, the voltage from the clamp circuit that is applied to the summing circuit at the base of Q2 will change; this will bring the sync tip level back to approximately -1.04 VDC. Q7 will be turned off and on according

to the peak of sync voltage level that is applied to U4A. The capacitors C14, C51, C77, and C41 will charge or discharge to the new voltage level, which biases U3B more or less, through jumper W7 on J4 in the Auto Clamp-On position. U3 will increase or decrease its output, as needed, to bring the peak of sync back to the correct level as set by R152 and R12. This voltage level is applied through U3B to Q2. In the Manual position, jumper W7 on J4 is in the Clamp-Off position, between pins 1 and 2, and adjustable resistor R41 provides the manual clamp bias adjustment for the video that connects to Q2.

Jumper W6 on jack J35 must be in the Normal position, between pins 2 and 3, for the clamp circuit to operate with a normal non-scrambled signal. If a scrambled signal is used, the tray is operated with jumper W6 in the Encoded position, connected between pins 1 and 2. The clamp circuit is set by adjusting depth of modulation pot R152 for the correct depth of modulation as measured at TP2.

Depending on the input video level, the waveform as measured at TP2 may not be 1 Vpk-pk. If W7 on J4 is moved to the Clamp-Off (Manual) position, between pins 1 and 2, the clamp level is adjusted by R41 and will not automatically be clamped to the set level. The output of buffer amplifier U3A drives the sync tip clamp circuit that consists of differential amplifier U4A, field effect transistor (FET) Q7, and buffer amplifier U3B. U4A is biased by R124, R125, R184, R152, and R126 so that the clamped voltage level at peak of sync is approximately -1.04 VDC as measured at TP2.

#### 4.2.2.3 Main Video Signal Path (Part 2 of 2)

The clamped video from Q2 is connected to white clipper circuit Q3. Q3 is adjusted with R20 and set to

prevent video transients from overmodulating the video carrier. The clamped video is connected to sync clipper circuit Q4 (adjusted by R24); Q4 limits the sync to -40 IRE units. The corrected video connects to emitter follower Q4 whose output is wired to unity gain amplifier U2A and provides a low-impedance, clamped video output at pin 1.

#### 4.2.2.4 Visual Modulator Circuit

The clamped video signal from U2A is split. One part connects to a metering circuit, consisting of U20 and associated components, that produces a video output sample at J8-6 and connects through the translator control board to the front panel meter for monitoring. The other clamped video path from U2A is through a sync-stretch circuit that consists of Q5 and Q6. The sync-stretch circuit contains R48; R48 adjusts the sync stretch magnitude (amount) and R45 adjusts the cut-in. This sync-stretch adjustment should not be used to correct for output sync problems, but it can be used for video input sync problems. The output of the sync-stretch circuit connects to pin 5, the I input of mixer Z1.

The video signal is heterodyned in mixer Z1 with the visual IF CW signal (45.75 MHz). The visual IF CW signal enters the board at jack J15 and is connected to U9, where it is amplified and wired to pin 1, the L input of mixer Z1. Adjustable capacitor C78 and resistor R53 are set up to add a small amount of incidental carrier phase modulation (ICPM) correction to the output of the mixer stage to compensate for any non-linearities generated by the mixer.

The modulated 45.75-MHz RF output of mixer Z1 is amplified by U5 and is fed to double-sideband visual IF output jack J18. The level of this output jack is adjusted by R70. J18 is the visual IF

loop-through output jack that is normally jumpered to J19 on the board. If the optional visual IF loop-through kit is purchased, the visual is connected out of the board to external IF processor trays.

After any external processing, the modulated visual IF, double-sideband signal re-enters the board through J19. The visual IF from J19 is amplified by U10 and U11 and routed through the vestigial sideband filter network, consisting of T1, FL1, and T2, and produces a vestigial sideband visual IF signal output. The filtered vestigial sideband visual IF is amplified by U7 and connected to a T-type attenuator. R62 can be adjusted to set the visual IF gain; this is the amount of the visual IF signal that is coupled to amplifier IC U8. R63 and C30 are adjusted for the best VSBF frequency response. The amplified IF signal is fed to the input of the diplexer circuit that consists of R76, L13, and L12. A detected voltage sample of the visual IF is available at test point TP5.

#### 4.2.2.5 41.25-MHz Aural IF Circuit

On this board, the 41.25-MHz aural IF is created by mixing the modulated 4.5-MHz aural intercarrier signal, produced by the aural IF synthesizer board or from the composite 4.5-MHz filter board, with the 45.75-MHz CW signal produced by the 45.75-MHz IF carrier oven oscillator board. The modulated 4.5-MHz aural intercarrier signal enters the board at J14 or J28 and is connected to IF relay K1. Jumper W3 on J7 determines whether the 4.5-MHz used by the board is internally generated or from an external source. With jumper W3 connected between pins 2 and 3, the 4.5 MHz from the aural IF synthesizer board or from the 4.5-MHz composite input is connected to mixer Z2. If an external 4.5-MHz signal is used, it enters the board at J12 and is fed through gain pot R88 to amplifier IC U13A. The amplified 4.5

MHz is then connected to J7 and, if jumper W3 is between pins 1 and 2, the 4.5-MHz signal from the external source is connected to the mixer. Mixer Z2 heterodynes the aural-modulated, 4.5-MHz signal with the 45.75-MHz CW signal to produce the modulated 41.25-MHz aural IF signal.

The output of the mixer is fed to a bandpass filter that is tuned to pass only the modulated 41.25-MHz aural IF signal that is fed to jack J16, the 41.25-MHz loop-through out jack of the board.

For normal operation, the 41.25-MHz signal is jumpered by a coaxial cable from J16 to J17 on the board. If the (optional) aural IF loop-through kit is purchased, the 41.25-MHz signal is connected to the rear of the tray, to which any processing trays can be connected, and then back to jack J17 on the board. The modulated 41.25-MHz aural IF signal from J17 is connected through amplifier ICs U15 and U16. The amplified output is connected to the attenuator-matching circuit that is adjusted by R85. R85 increases or decreases the level of the 41.25 MHz that sets the A/V ratio for the diplexer circuit. The diplexer circuit takes the modulated 45.75-MHz visual IF and the modulated aural IF and combines them to produce the 45.75-MHz + 41.25-MHz IF output. The combined 45.75-MHz + 41.25-MHz IF signal is amplified by U12 and connected to combined IF output jack J20 on the board. A sample of the combined IF output is provided at J21 on the board. If a NICAM input is used, it connects to J36 on the board. The level of the NICAM signal is set by R109 before it is fed to the diplexer circuit consisting of L28, L29, and R115. This circuit combines the NICAM signal with the 45.75-MHz visual IF + 41.25-MHz aural IF signal.

#### 4.2.2.6 Operational Voltages

The +12 VDC needed to operate the translator control board enters the board at J23, pin 3, and is filtered by L26, L33, and C73 before it is fed to the rest of the board.

The -12 VDC needed to operate the board enters the board at J23, pin 5, and is filtered by L27 and C74 before being fed to the rest of the board.

#### 4.2.3 (A6) (Optional) Delay Equalizer Board (1227-1204; Appendix D)

The optional delay equalizer board provides a delay to the video signal, correction to the frequency response, and amplification of the video signal.

The video signal enters the board at J1-2 and is connected to a pi-type, low-pass filter consisting of C16, L7, and C17. This filter prevents any unwanted higher frequencies from entering the board. The output of the filter is connected to amplifier stage U1; the gain is controlled by R29. The video output of the amplifier stage is wired to the first of four delay-equalizing circuits that shape the video signal to the FCC specification for delay equalization or to the shape needed for the system. The board has been factory-adjusted to this FCC specification and should not be readjusted without the proper equipment.

Resistors R7, R12, R17, and R22 adjust the sharpness of the response curve while inductors L1, L2, L3, and L4 adjust the position of the curve. With a delay equalizer test generator signal or a sine x/x video test pattern input, the resistors and inductors can be adjusted, while monitoring a Tektronix VM700 test measurement set, until the desired FCC delay equalization curve or system curve is attained. The delay-equalized video signal is connected to J1-4, the video output of the board. A

sample of the delayed video signal is connected to J2 on the board and can be used for testing purposes.

The  $\pm 12$  VDC needed to operate the board enters the board at J1. The +12 VDC connects to J1-9, which is filtered by L5 and C11 before it is directed to the rest of the board. The -12 VDC connects to J1-6, which is filtered by L6 and C12 before it is directed to the rest of the board.

#### **4.2.4 (A7) (Optional) IF Carrier Oven Oscillator Board (1191-1404; Appendix D)**

The IF carrier oven oscillator board generates the visual IF CW signal at 45.75 MHz for NTSC system "M" usage.

The +12 VDC is applied through jack J10 to crystal oven HR1, which is preset to operate at 60° C. The oven encloses crystal Y1 and stabilizes the crystal temperature. The crystal is the principal device that determines the operating frequency and is the most sensitive in terms of temperature stability.

Crystal Y1 operates in an oscillator circuit consisting of transistor Q1 and its associated components. Feedback is provided through a capacitor-voltage divider, consisting of C5 and C6, that operates the crystal in a common-base amplifier configuration using Q1. The operating frequency of the oscillator can be adjusted by variable capacitor C17. The oscillator circuit around Q1 has a separate regulated voltage, 6.8 VDC, which is produced by a combination of dropping resistor R4 and zener diode VR1. The output of the oscillator at the collector of Q1 is capacitively coupled through C8 to the base of Q2. The small value of C8, 10 pF, keeps the oscillator from being loaded down by Q2.

Q2 is operated as a common-emitter amplifier stage whose bias is provided

through R8 from the +12 VDC line. The output of Q2, at its collector, is split between two emitter-follower transistor stages, Q3 and Q4. The output of Q3 is taken from its emitter through R11 to establish an approximate 50-ohm source impedance through C11 to J3, the main output jack. This 45.75-MHz signal is at about the +5 dBm power level. In most systems, this output is either directed to a visual modulator board or to some splitting and amplifying arrangement that distributes the visual IF carrier for other purposes. The second output from the collector of Q2 is fed to the base of Q4, the emitter follower transistor.

Q4 drives two different output circuits. One output is directed through voltage dividers R14 and R15 to jack J2 and is fed to a frequency counter. While monitoring J2, the oscillator can be set exactly on the operating frequency (45.75 MHz) by adjusting C17. The output at J2 is at a power level of approximately -2 dBm, which is sufficient to drive most frequency counters. The other output of Q4 connects to prescaler chip U1, which divides the signal by 15. The output of U1 is applied to U2, a programmable divider IC. U2 is programmed through pins 11 to 20 to divide by 61. This results in a 50-kHz signal at pin 9 that is available as an output at J1. The output of 50 kHz is generally used in systems where the visual IF carrier oven oscillator is used as the reference for a PLL circuit; an example of this is when the PLL circuit uses the aural IF synthesizer board and the aural VCO. The 50-kHz CMOS output at jack J1 is not capable of achieving enough drive level for a long coaxial cable length. As a result, when a long coaxial cable is needed, the output at jack J5 is utilized. The push-pull transistor stage Q5 and Q6, along with emitter resistor R18, provide a large-load output capability at J5.

The stages U1, U2, Q5, and Q6 are powered by +5.1 VDC, which is obtained by using the +12 VDC line voltage, and voltage-dropping resistor R16 and zener diode VR2.

The +12 VDC power is applied to the board through jack J4, pin 3, and is isolated from the RF signals which may occur in the +12 VDC line through the use of RF choke L2 and filter capacitor C10.

#### **4.2.5 (A8) ALC Board, NTSC (1265-1305; Appendix D)**

The automatic level control (ALC) board provides the ALC and amplitude linearity correction of the IF signal. The ALC adjusts the level of the IF signal through the board to control the output power of the translator.

The visual + aural IF input (0 dBm) from the receiver tray connects to receiver IF input jack J1. The visual + aural IF input (0 dBm) signal from the (Optional) Modulator Kit enters the board at modulator IF input jack J32. The modulator IF input connects to relay K3 and the receiver IF input connects to relay K4. The two relays are controlled by the Modulator Select command that is connected to J30 on the board. Modulator select enable/disable jumper W11 on J29 controls whether the Modulator Select command at J30 controls the operation of the relays. With jumper W11 on J29, pins 1 and 2, the Modulator Select command at J30 controls the operation of the relays; with jumper W11 on J29, pins 2 and 3, the modulator is selected all of the time.

##### *4.2.5.1 Receiver Selected*

With the receiver selected, which is J11-10 and J11-28 on the rear of the UHF exciter tray (connected to J30 on the board) not connected together, relays K3 and K4 are energized. When K4 is energized, it connects the

receiver IF input at J1, if present, to the rest of the board. When K3 is energized, it connects to the modulator IF input at J32 to 50 watts; Modulator Enable LED DS5 will not be illuminated.

##### *4.2.5.2 (Optional) Modulator Kit Selected*

With the modulator selected, J11-10 and J11-28 on the rear of the UHF exciter tray are connected together; this makes J30 low and causes relays K3 and K4 to de-energize. When K4 is de-energized, it connects the receiver IF input at J1, if present, to 50 watts. When K3 is de-energized, it connects the modulator IF input at J32 to the rest of the board; Modulator Enable LED DS5 will be illuminated.

##### *4.2.5.3 Main IF Signal Path (Part 1 of 3)*

The selected visual + aural IF input (0 dBm) signal is split, with one half of the signal entering a bandpass filter that consists of L3, L4, C4, L5, and L6. This bandpass filter can be tuned with C4 and is substantially broader than the IF signal bandwidth. It is used to slightly steer the frequency response of the IF to make up for any small discrepancies in the frequency response in the stages that precede this point. The filter also serves the additional function of rejecting unwanted frequencies that may occur if the tray cover is off and the tray is in a high RF environment. (NOTE: If this is the case, the translator will have to be serviced with the tray cover off in spite of the presence of other RF signals). The filtered IF signal is fed through a pi-type matching pad consisting of R2, R3, and R4 to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3.

##### *4.2.5.4 Input Level Detector Circuit*

The other part of the split IF input is connected through L2 and C44 to U7; U7 is an IC amplifier that is the input to

the input level detector circuit. The amplified IF is fed to T4; T4 is a step-up transformer that feeds diode detector CR14. The positive-going detected signal is then low-pass filtered by C49, L18, and C50. This allows only the video with positive sync to be applied through emitter follower Q1. The signal is then connected to detector CR15 to produce a peak-sync voltage that is applied to op-amp U9A. There is a test point at TP3 that provides a voltage-reference check of the input level. The detector serves the dual function of providing a reference that determines the input IF signal level to the board and also serves as an input threshold detector.

The input threshold detector prevents the automatic level control from reducing the attenuation of the pin-diode attenuator to minimum (the maximum signal) if the IF input to the board is removed. The ALC, video loss cutback, and the threshold detector circuits will only operate when jumper W3 on jack J6 is in the Auto position, between pins 1 and 2. Without the threshold detector, and with the pin-diode attenuator at minimum, the signal will overdrive the stages following this board when it is restored.

As part of the threshold detector operation, the minimum IF input level at TP3 is fed through detector CR15 to op-amp IC U9A pin 2. The reference voltage for the op-amp is determined by the voltage divider that consists of R50 and R51 (off the +12 VDC line). When the detected input signal level at U9A, pin 2, falls below this reference threshold (approximately 10 dB below the normal input level), the output of U9A at pin 1 goes to the +12 VDC rail. This high is connected to the base of Q2. At this point, Q2 is forward biased and creates a current path. This path runs from the -12 VDC line and through red LED DS1, the input level fault indicator, which becomes lit, resistor R54, and transistor Q2 to +12 VDC.

The high from U9A also connects through diode CR16 to U9B, pin 5, whose output at pin 7 goes high. The high connects through range adjust pot R74 to J20, which connects to the front panel-mounted power adjust pot. This high connects to U10A, pin 2, and causes it to go low at output U10A, pin 1. The low is applied through jumper W3 on J6 to the pin-diode attenuator circuit that cuts back the IF level and, therefore, the output power level, to 0. When the input signal level increases above the threshold level, the output power will raise, as the input level increases, until normal output power is reached.

The video input level at TP3 is also fed to a sync-separator circuit, consisting of IC U8, CR17, Q3, and associated components, and then to a comparator circuit made up of U9C and U9D. The reference voltage for the comparators is determined by a voltage divider consisting of R129, R64, R65, R66, and R130 (off the -12 VDC line). When the input signal level to the detector at TP3 falls below this reference threshold, which acts as a loss-of-sync detector circuit, the output of U9C and U9D goes towards the -12 VDC rail and is split, with one part biasing on transistor Q5. A current path is then established from the +12 VDC line through Q5, the resistors R69 and R137, and the red LED DS3 (video loss indicator), which is illuminated. When Q5 is on, it applies a high to the gates of Q6 and Q7. This causes them to conduct and apply video loss fault pull-down outputs to J18 pins 5 and 2.

The other low output of U9C and U9D is connected through CR20 to jack J5. Jumper W2 on J5, in the Cutback Enable position (between pins 2 and 3), connects the low to the base of the forward-biased Q4. If jumper W2 is in the Disable position, between pins 1 and 2, the auto cutback will not operate. With Q4 biased on, a level determined by the setting of cutback

level pot R71, which is set at the factory to cut back the output to approximately 25%, is applied to U9B, pin 5. The output of U9B at pin 7 goes low and is applied through the power adjust pot to U10A, pin 2, whose output goes low. This low is applied to the pin-diode attenuator to cut back the level of the output to approximately 25%.

#### 4.2.5.5 Pin-Diode Attenuator Circuit

The input IF signal is fed to a pin-diode attenuator circuit that consists of CR1 to CR3. Each of the pin diodes contains a wide intrinsic region; this makes the diodes function as voltage-variable resistors at this intermediate frequency. The value of the resistance is controlled by the DC bias supplied to the diode. The pin diodes are configured in a pi-type attenuator configuration where CR1 is the first shunt element, CR3 is the series element, and CR2 is the second shunt element. The control voltage, which can be measured at TP1, originates either from the ALC circuit when jumper W3 on J6 is in the ALC Auto position, between pins 1 and 2, or from pot R87 when the jumper is in the Manual Gain position.

On the pin-diode attenuator circuit, a current path exists from J6 through R6 and then through the diodes of the pin attenuator. Changing the amount of current through the diodes by forward biasing them changes the IF output level of the board. There are two extremes of attenuation ranges for the pin-diode attenuators. In the minimum attenuation case, the voltage, measured at TP1, approaches the +12 VDC line. There is a current path created through R6, through series diode CR3, and finally through R9 to ground. This path forward biases CR3 and causes it to act as a relatively low-value resistor. In addition, the larger current flow increases the voltage drop across R9 that tends to turn off diodes

CR1 and CR2 and causes them to act as high-value resistors. In this case, the shunt elements act as a high resistance and the series element acts as a low resistance to represent the minimum loss condition of the attenuator (maximum signal output). The other extreme case occurs as the voltage at TP1 is reduced and goes towards ground or even slightly negative. This tends to turn off (reverse bias) diode CR3, the series element, causing it to act as a high-value resistor. An existing fixed current path from the +12 VDC line, and through R5, CR1, CR2, and R9, biases series element CR3 off and shunt elements, diodes CR1 and CR2, on, causing them to act as relatively low-value resistors. This represents the maximum attenuation case of the pin attenuator (minimum signal output). By controlling the value of the voltage applied to the pin diodes, the IF signal level is maintained at the set level.

#### 4.2.5.6 Main IF Signal Path (Part 2 of 3)

When the IF signal passes out of the pin-diode attenuator through C11, it is applied to modular amplifier U1. This device contains the biasing and impedance-matching circuits that makes it operate as a wide-band IF amplifier. The output of U1 is available, as a sample of the pre-correction IF for troubleshooting purposes and system setup, at jack J2. The IF signal is then connected to the linearity corrector portion of the board.

#### 4.2.5.7 Linearity Corrector Circuits

The linearity corrector circuits use three stages of correction to adjust for any amplitude non-linearities of the IF signal. Each stage has a variable threshold control adjustment, R34, R37, or R40, and a variable magnitude control adjustment, R13, R18, or R23. The threshold control determines the point at which the gain is changed and

the magnitude control determines the amount of gain change that occurs once the breakpoint is reached. Two reference voltages are needed for the operation of the corrector circuits. Zener diode VR1, with R33 and R135, provides a +6.8 VDC reference and the diodes CR11 and CR12 provide a .9 VDC reference that temperature compensates for the two diodes in each corrector stage.

For the linearity correctors to operate, an IF signal is applied to transformer T1, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R14, R15, and R16 form an L-pad that lowers the level of the signal. The amount that the level is lowered can be adjusted by adding more or less resistance, using R13, in parallel with the L-pad resistors. R13 is only in parallel when the signal reaches a level large enough to turn on diodes CR4 and CR5. When the diodes turn on, current flows through R13, putting it in parallel with the L-pad.

When R13 is put in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch (the amount determined by the adjustment of R13). The signal is next applied to amplifier U2 to compensate for the loss through the L-pad. The breakpoint, or cut-in point, for the first corrector is set by controlling where CR4 and CR5 turn on. This is accomplished by adjusting cut-in resistor R34; R34 forms a voltage-divider network from +6.8 VDC to ground. The voltage at the wiper arm of R34 is buffered by the unity-gain amplifier U5D. This reference voltage is then applied to R35, R36, and C39 through L12 to the CR4 diode. C39 keeps the reference from sagging during the vertical interval. The .9 VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U5B. The reference voltage is then connected to diode CR5 through choke L11. The two

chokes L11 and L12 form a high impedance for RF that serves to isolate the op-amp ICs from the IF.

After the signal is amplified by U2, it is applied to the second corrector stage through T2. This corrector and the third corrector operate in the same fashion as the first. All three corrector stages are independent and do not interact with each other.

The correctors can be disabled by moving jumper W1 on J4 to the Disable position, between pins 2 and 3; this moves all of the breakpoints past the tip of sync so that they will have no affect. The IF signal exits the board at IF output jack J3 after passing through the three corrector stages and is normally connected to an external IF phase corrector board.

#### 4.2.5.8 Main IF Signal Path (Part 3 of 3)

After the IF signal passes through the external IF phase corrector board, it returns to the ALC board at IF input jack J7. The IF then passes through a bandpass filter consisting of L20, C97, C62, L21, C63, L22, L23, C64, and C99. This filter is intended to make up for small errors in frequency response that are incurred by the signal while being processed through the linearity and incidental phase correction circuits.

Following the bandpass filter, the signal is split using L24, L25, and R89. The signal passing through L24 is the main IF path through the board. A sample of the corrected IF signal is split off and connected to J10, the IF sample jack. The IF connects to jacks J27 and J28. These jacks control whether a 6-dB pad is included in the circuit by the positioning of jumpers W9 and W10. The 6-dB pad-in occurs when jumpers W9 and W10 are connected between pins 2 and 3 on J27 and J28. The 6-dB pad-out occurs when jumpers W9 and W10 are connected between pins 1 and



2 on J27 and J28. Normally, the pad is out. The IF signal is then applied to a two-stage, frequency-response corrector circuit that is adjusted as needed.

Variable resistors R103 and R106 are used to adjust the depth and gain of the notches and variable caps C71 and C72 are used to adjust the frequency position of the notches. The IF signal is amplified by U13 and U14 before it is connected to J12, the IF output jack of the board. R99 is an output level adjustment that is set to provide approximately 0 dBm of IF output at J12. A sample of the IF is fed to J11 to provide an IF sample point that can be monitored without breaking the signal path and gives an indication of the IF signal after the linearity and the frequency-response correction takes place.

#### 4.2.5.9 ALC Circuit

The other path of the corrected IF signal is used in the ALC circuit. The IF is wired out of the splitter through L25 and connects to op-amp U12. The output of U12 is wired to jacks J8 and J9 on which jumpers W4 and W8 control the normal or encoded operation of the ALC circuitry. For normal operation, jumper W4 on J8 is between pins 1 and 2 and jumper W8 on J9 is between pins 1 and 2. The IF signal is applied to transformer T5; T5 doubles the voltage swing by means of a 1:4 impedance transformation before it is connected to the ALC detector circuit on the board and amplified by U10B.

For normal operation, jumper W7 on J26 is between pins 1 and 2 and jumper W5 on J21 is between pins 1 and 2. The detected ALC voltage is wired to U10A, pin 2, where it is summed with the front panel power control setting. The output power adjustment for the translator is achieved, if the (optional) remote

power raise/lower kit (1227-1039) is purchased, by R75, a motor-driven pot controlled by switch S1 on the board, or screwdriver adjust pot R1 on the front panel of the UHF exciter tray. An external power raise/lower switch can be used by connecting it to jack J10, at J10-11 power raise, J10-13 power raise/lower return, and J10-12 power lower, on the rear of the UHF exciter tray. S1, or the Remote switch, controls relays K1 and K2, which control motor M1 that moves variable resistor R75. If the (optional) remote power raise/lower kit is not purchased, the ALC voltage is controlled only by screwdriver adjust pot R1 on the front panel of the UHF exciter tray. The ALC voltage is set for .8 VDC at TP4 with a 0-dBm output at J12 of the board. A sample of the ALC at J19, pin 2, is wired to the transmitter control board where it is used on the front panel meter and in the AGC circuits.

This ALC voltage, and the DC level corresponding to the IF level after signal correction, are fed to U10A, pin 2, whose output at pin 1 connects to the ALC pin-diode attenuator circuit. If there is a loss of gain somewhere in an IF circuit, the output power of the translator will drop. The ALC circuit senses this drop at U10A and automatically eases the loss of the pin-diode attenuator circuit by increasing its gain.

The ALC action starts with the ALC detector level monitored at TP4. The detector output at TP4 is nominally +.8 VDC and is applied through resistor R77 to a summing point at op-amp U10A, pin 2. The current available from the ALC detector is offset, or complemented, by current taken away from the summing junction. In normal operation, U10A, pin 2, is at 0 VDC when the loop is satisfied. If the recovered or peak-detected IF signal level at IF input jack J7 of this board should drop, which normally means that the output power is decreasing,

the null condition would no longer occur at U10A, pin 2. When the level drops, the output of U10A, pin 1, will go more positive. If jumper W3 on J6 is in the Automatic position, it will cause the ALC pin-diode attenuators CR1, CR2, and CR3 to have less attenuation and increase the IF level; this will compensate for the decrease in the level. If the ALC cannot increase the input level enough to satisfy the ALC loop, due to there not being enough range, an ALC fault will occur. The fault is generated because U10D, pin 12, increases above the trip point set by R84 and R83 until it conducts. This causes U10D pin 14 to go high and the red ALC Fault LED DS2 to light.

#### 4.2.5.10 Scrambled Operation with Encoding

For encoded, scrambled operation, jumper W4 on J8 must be connected between pins 2 and 3, jumper W8 on J9 must be between pins 3 and 2, jumper W7 on J26 must be between pins 2 and 3, and jumper W5 on J21 must be between pins 2 and 3. The IF is connected through W4 on J8 to the sync regeneration circuits.

If this board is operated with scrambling, using suppressed sync, the ALC circuit operates differently because there is no peak of sync present on the IF input. A timing pulse from the scrambling encoder connects to the board at J24. This timing pulse is converted to sync pulses by U17A and U17B, which control the operation of Q8. The sync amplitude is controlled by R149 and then applied to U15A, where it is added to the detected IF signal to produce a peak of sync level. The output of U15A is peak detected by CR26 and fed to U15B. If necessary, intercarrier notch L39 can be placed in the circuit by placing W6 on J22. The intercarrier notch is adjusted to filter any aural and 4.5-MHz intercarrier frequencies. The peak of sync signal is fed through R162, the ALC calibration

control, to amplifier U15C. The amplified peak of sync output is connected through J21, pins 2 and 3, to U10A, where it is used as the reference for the ALC circuit and the AGC reference to the transmitter control board. Voltage TP4 should be the same in either the normal or the encoded video mode. Monitor J9, pins 3 and 4, with a spectrum analyzer, check that the board is in the AGC mode, and tune C103 to notch-out the aural IF carrier.

#### 4.2.5.11 Fault Command

The ALC board also has circuitry for an external mute fault input at J19, pin 6. This is a Mute command and, in most systems, it protects the circuits of high-gain output amplifier devices against VSWR faults. In this case, the action should occur faster than just pulling the ALC reference down. Two different mechanisms are employed: one is a very fast-acting circuit to increase the attenuation of the pin-diode attenuator, CR3, CR1, and CR2, and the second is the reference voltage being pulled away from the ALC amplifier device. An external Mute is a pull-down applied to J19, pin 6, to provide a current path from the +12 VDC line through R78 and R139, the LED DS4 (Mute indicator), and the LED section of opto-isolator U11.

These actions turn on the transistor section of U11 that applies -12 VDC through CR21 to U10A, pin 3, and pulls down the reference voltage. This is a fairly slow action that is kept at this pace by the low-pass filter function of R81 and C61. When the transistor section of U11 is on, -12 VDC is also connected through CR22 to the pin-diode attenuator circuit. This establishes a very fast muting action, by reverse biasing CR3, in the event of an external VSWR fault.

#### 4.2.5.12 $\pm 12$ VDC Needed to Operate the Board

The  $\pm 12$  VDC connects to the board at J14. The +12 VDC connects to J14-3 and is filtered by L30, L41, and C80 before it is applied to the rest of the board. The -12 VDC connects to J14-5 and is filtered by L31 and C81 before it is applied to the rest of the board.

The +12 VDC also connects to U16, a 5-VDC regulator IC, which produces the +5 VDC needed to operate timing IC U17.

#### 4.2.6 (A9) IF Phase Corrector Board (1227-1250; Appendix D)

The IF phase corrector board has adjustments that pre-correct for any IF phase modulation distortion that may occur in output amplifier devices such as Klystron power tubes and solid-state amplifiers. Two separate, adjustable IF paths are on the board: a quadrature IF path and an in-phase IF path. The quadrature IF is  $90^\circ$  out of phase and much larger in amplitude than the in-phase IF. When they are combined in Z1, it provides the required, adjustable phase correction to the IF signal.

The IF input signal enters at J1 and is AC coupled to U1. U1 amplifies the IF before it is connected to Z1, a splitter that creates two equal IF outputs: IF output 1 is connected to J2 and IF output 2 is connected to J3. IF output 1 at J2 is jumpered through coaxial cable W4 to jack J6, the quadrature input, on the board. IF output 2 at J3 is jumpered through coaxial cable W5 to jack J7, the in-phase input, on the board.

##### 4.2.6.1 Phase Corrector Circuit

The phase corrector circuit corrects for any amplitude nonlinearities of the IF signal. It is designed to work at IF and has three stages of correction. Each stage has a variable threshold and

magnitude control. The threshold control determines the point at which the gain is changed and the magnitude control determines the gain change once the breakpoint is reached. The second stage has a jumper that determines the direction of correction, so that the gain can be increased either above or below the threshold and either black or white stretch can be achieved.

In the phase-corrector circuit, the IF signal from J6 is applied to transformer T1; T1 doubles the voltage swing using a 1:4 impedance transformation. Resistors R8, R61, R9, and R48 form an L-pad that attenuates the signal. This attenuation is adjusted by adding R7, a variable resistor, in parallel with the L-pad. R7 is only in parallel when the signal reaches a level large enough to bias on CR1 and CR2 and allow current to flow through R7. When R7 is put in parallel with the L-pad, the attenuation through the L-pad is lowered, causing black stretch.

Two reference voltages are utilized in the corrector stages and both are derived from the +12 VDC line. Zener diode VR1, with R46 as a dropping resistor, provides +6.8 VDC from the +12 VDC line. Diodes CR11 and CR12 provide a .9 VDC reference to temperature compensate the corrector circuits from the effects of the two diodes in each corrector stage.

The threshold for the first corrector stage is set by controlling where CR1 and CR2 turn on. This is accomplished by adjusting R3 to form a voltage divider from +6.8 VDC to ground. The voltage at the wiper of R3 is buffered by U9C, a unity-gain amplifier, and applied to CR1. The .9 VDC reference is connected to U9D, a unity-gain amplifier, whose output is wired to CR2. These two references are connected to diodes CR1 and CR2 through chokes L2 and L3. The two chokes form a high impedance for RF to isolate the op-amps from the RF. The

adjusted signal is next applied to amplifier U2 to compensate for the loss through the L-pad. U2 is powered through L4 and R10 from the +12 VDC line. After the signal is amplified by U2, it is applied to the second corrector stage through T2 and then to a third corrector stage through T3. The other two corrector stages operate in the same manner as the first; they are independent and do not interact with each other.

When jumper W1 on J8 is connected from center to ground, R15 is put in series with ground. In this configuration, black stretch (white compression) is applied to the IF signal by controlling the attenuation through the path. When W1 is connected from the center pin to the end that connects to T2, R15 is put in parallel with the L-pad. In this configuration, black compression (white stretch) is applied to the IF signal by controlling the attenuation through the path.

The phase correctors can be bypassed by moving jumper W2 on J9 to the Disable position. This action will move all of the threshold points past sync tip so that they will have no effect. R68 can be adjusted and set for the correction range that is needed. TP2 is a test point that gives the operator a place to measure the level of the quadrature IF signal that is connected to pin 6 on combiner Z2.

#### 4.2.6.2 Amplitude Corrector Circuit

The amplitude corrector circuit uses one stage of correction to adjust for any amplitude nonlinearities of the IF signal. The stage has a variable threshold control, R31, and a variable magnitude control, R35. The threshold control determines the point at which the gain is changed and the magnitude control determines the amount of gain change once the breakpoint is reached.

Two reference voltages are needed for the operation of the corrector circuit. Zener diode VR1 with R46 provides +6.8 VDC and the diodes CR11 and CR12 provide a .9 VDC reference voltage to temperature compensate for the two diodes in the corrector stage. In the amplitude corrector circuit, the IF signal from J7 is applied to transformer T4 to double the voltage swing by means of a 1:4 impedance transformation. Resistors R36, R55, R56, and R37 form an L-pad that lowers the level of the signal. The amount that the level is lowered is adjusted by adding more, or less, resistance, using R35 in parallel with the L-pad resistors. R35 is only in parallel when the signal reaches a level large enough to turn on diodes CR8 and CR9. When the diodes turn on, current flows through R35 and puts it in parallel with the L-pad. When R35 is in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch (the amount of stretch determined by the adjustment of R35).

The signal is next applied to amplifier U5 to compensate for the loss in level through the L-pad. The breakpoint, or cut-in point, for the corrector stage is set by controlling where CR8 and CR9 turn on. This is achieved by adjusting cut-in resistor R31 to form a voltage divider from +6.8 VDC to ground. The voltage at the wiper arm of R31 is buffered by the unity-gain amplifier U8B. This voltage is then applied to R34 through L11 to the CR9 diode. The .9-VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U8A. C36 keeps the reference from sagging during the vertical interval. The reference voltage is then connected to diode CR8 through choke L12. Chokes L11 and L12 form a high impedance for RF to isolate the op-amp ICs from the IF.

After the signal is amplified by U5, it is applied to a second stage through T5. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R39, R57, R58, and R40 form an L-pad that lowers the level of the signal. The signal is applied to amplifier U6 to compensate for the loss in level through the L-pad. After the signal is amplified by U6, it is applied to a third stage through T6. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R42, R59, R60, and R43 form an L-pad to lower the level of the signal. The signal is applied to amplifier U7 to compensate for the loss in level through the L-pad. TP1 is a test point that gives the operator a place to measure the level of the in-phase IF signal that is connected to mixer stage Z2. The amplitude corrector can be disabled by moving jumper W3 on J10 to the Disable position; this will move the breakpoint past sync tip and will have no effect on the signal.

#### 4.2.6.3 Output Circuit

The phase-corrected signal from pin 1 on combiner Z2 exits the board at IF output jack J4 after passing through a matching network consisting of six resistors.

### 4.2.7 (A17) Transmitter Control Board (1245-1101; Appendix D)

The transmitter control board provides information on system control functions and the operational LED indications; these can be viewed on the front panel of the translator. The main control functions are for the Operate/Standby and Auto/Manual selections. When the translator is switched to Operate, the board supplies the enables to any external amplifier trays. The board also performs the automatic switching of the translator to Standby upon the loss of the video input when the translator is in Auto.

The transmitter control board contains a VSWR cutback circuit. If the VSWR of the translator increases above 20%, the VSWR cutback circuit will become active and cut back the output level of the translator, as needed, to maintain a maximum of 20% VSWR. An interlock (low) must be present at J8-24 for the translator to be switched to Operate. When the interlock is present, the green Interlock LED DS5 will be lit.

#### 4.2.7.1 Operate/Standby Switch S1

K1 is a magnetic latching relay that controls the switching of the translator from Operate to Standby. When Operate/Standby switch S1, on the front panel of the tray, is moved to Operate, one coil of relay K1 energizes and causes the contacts to close and apply a low to U4B-9. If the translator interlock is present, and there is no overtemperature fault, lows will also be applied to U4B-10, U4B-11, and U4B-12.

With all of the low inputs to U4B, the output at U4B-13 will be low. The low biases off Q1 and this turns off the amber Standby LED DS1 on the front panel. In addition, this action applies a high to Q2 and turns on and lights the green Operate LED DS2 (also on the front panel). When Q2 is biased on, it connects a low to Q12 and biases it off; this allows the ALC to be applied to J1 and connect to any external amplifier trays. The low from U4B-13 is also applied to Q4 and Q24, which are biased off, and removes the disables from J1-4 and J18-1. The low from U4B-13 also connects to Q10, which is biased on, and connects a high to Q6, Q7, Q8, and Q9; these are biased on and apply -12 VDC enables to J8-2, J8-3, J8-4, and J8-5, which connect to any external amplifier trays. The high applied to Q2 is also connected to Q5 and Q26, which are biased on, and apply a low enable to J1-3, which connects to a remote operate indicator.

The translator is now in the Operate mode.

When Operate/Standby switch S1 is moved to Standby, the other coil of relay K1 energizes, causing the contacts to open and a high (+12 VDC) to be applied to U4B-9. The high at the input causes the output at U4B-13 to go high. The high biases on Q1 and applies a low to the amber Standby LED DS1, on the front panel, which turns on and applies a low to Q2. This causes Q2 to turn off and extinguishes the green Operate LED DS2. When Q12 is biased on, the output from U2C goes low and pulls the ALC voltages at J1 low; this lowers the gain of the external amplifier trays. The high from U4B-13 is applied to Q4 and Q24, which are biased on, and applies disables at J1-4 and J18-1. The high from U4B-13 connects to Q10, which is biased off. The Q10 bias off removes the high from Q6, Q7, Q8, and Q9, which are biased off, and removes the -12 VDC enables at J8-2, J8-3, J8-4, and J8-5, which connect to the external amplifier trays. The low applied to Q2 is also connected to Q5 and Q26, which are biased off, and the remote enable at J1-3 is removed. The translator is now in the Standby mode.

#### 4.2.7.2 Automatic/Manual Switch S2

K2 is a magnetic latching relay that switches the operation of the translator to Automatic or Manual using Auto/Manual switch S2 on the front panel of the tray.

When S2 is set to the Auto position, the operation of the translator is controlled by the fault circuits and will stay in Operate even if Operate/ Standby switch S1 is moved to Standby. With S2 in Auto, a low is applied to one coil in the relay and this energizes and closes the contacts. The closed contacts apply a low to the green Automatic LED DS3; as a result, DS3 is illuminated. The low from the relay connects to

U5A, pin 2; U5D, pin 13; Q21; and Q23. When Q21 and Q23 are biased off, this causes their outputs to go high. The high from Q21 connects to the amber Manual LED DS4, on the front panel, biasing it off, and to Q22, biasing it on. The drain of Q22 goes low and is applied to J8-7; this enables any remote auto indicator connected to J8-7. The low to Q23 biases it off and removes the enable to any remote manual indicator connected to J8-6.

When S2 is set to the Manual position, the operation of the translator is no longer controlled by the fault circuits, it is controlled by Operate/Standby switch S1. With S2 in Manual, a low is applied to the other coil in the relay and this energizes and opens the contacts. The open contacts of the relay remove the low from the green Automatic LED DS3 on the front panel and causes it to not light. The high connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. Q21 and Q23 are biased on; this causes their outputs to go low. The low from Q21 connects to the amber Manual LED DS4 on the front panel, biasing it on, and to Q22, biasing it off. The drain of Q22 goes high and is applied to J8-7; this will disable any remote auto indicators connected to J8-7. Q23 is biased on and applies a low enable to any remote manual indicator connected to J8-6.

#### 4.2.7.3 Automatic Turning On and Off of the Translator Using the Presence of Video

The transmitter control board also allows the translator to be turned on and off by the presence of video at the translator, when the translator is in Auto. When a video fault occurs due to the loss of video, J7-5 goes low. The low is applied through W1, on J10, to Q16, which is biased off, and to the red Video Loss Fault LED DS9, on the front panel, which will light. The drain of Q16 goes high and connects to U5B, pin 5, causing the output at pin 4 to go low. The low connects to Q18, which is

biased off, and causes the drain of Q18 to go high. The high connects to U3D, pin 12, whose output at pin 14 goes high. The high connects to U5C, pins 8 and 9, causing its output at pin 10 to go low, and to U5A, pin 1, causing its output at pin 3 to go low.

With S2 set to Automatic, a low is applied to U5A, pin 2, and to U5D, pin 13. When U5A, pin 1, is high and U5A, pin 2, is low, it causes the output at pin 3 to go low. When U5D, pin 12, is low and U5D, pin 13, is low, it causes its output to go high. When U5A, pin 3, is low, it biases off Q20 and removes any pull down to the Operate switch. A high at U5D, pin 11, biases on Q19 and applies a low enable to the Standby switch that places the translator in the Standby mode.

When the video signal is returned, J7-5 goes high. The high is applied to Q16, which is biased on, and to the red Video Fault LED DS9, which is extinguished. The output of Q16 goes low and connects to U5B, pin 5. If there is no receiver ALC fault, U5B, pin 6, is also low; this causes the output at pin 4 to go high. The high connects to Q18, which is biased on, and causes the drain of Q18 to go low. The low connects to U3D, pin 12, whose output at pin 14 goes low. The low connects to U5C, pins 8 and 9, which causes its output at pin 10 to go high, and to U5A, pin 1. With Auto/Manual switch S2 in Auto, a low is applied to U5A, pin 2, and to U5D, pin 13. When U5A, pins 1 and 2, is low, its output at pin 3 goes high. When pin 12 of U5D is high, the output of U5D at pin 11 goes low. When U5A, pin 3, is high, it biases on Q20 and applies a pull-down enable to the Operate switch. A low at U5D, pin 11, biases off Q19 and removes any pull down to the Standby switch. As a result of these actions, the translator is switched to Operate.

#### 4.2.7.4 Faults

There are four possible faults, video loss fault, VSWR cutback fault, overtemperature fault, and ALC fault, which may occur in the translator and are applied to the transmitter control board. During normal operation, no faults are sent to the board. The overtemperature fault is connected to the (A8-A1) thermal switch on the (A8) 2500W reject load for the translator.

#### Video Loss Fault

If a video loss occurs while the translator is in Auto, the system will change to the Standby mode until the video is returned; at that point, it will immediately revert to Operate. A video loss fault applies a low from the ALC board to the video fault input at J7-5 on the board.

With jumper W1 in place on J10, the video fault is connected to LED DS9 and to Q16. The red Video Loss Fault LED DS9 on the front panel will light. Q16 is biased off and causes its drain to go high. The high is wired to U5B, pin 5, whose output at U5B, pin 4, goes low. The low is wired to Q18, which is biased off, and causes the drain to go high. The high is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go high. The high connects to U5A, pin 1, and, if the translator is in Auto, pin 2 of U5A is low. When pin 1 is high and pin 2 is low, the output of U5A goes low and reverse biases Q20, shutting it off. The high at U5C, pins 8 and 9, causes its output at pin 10 to go low. This low is connected to U5D, pin 12, and, if the translator is in Auto, pin 13 of U5D is also low. The lows on pins 12 and 13 cause the output to go high and forward bias Q19. The drain of Q19 goes low and connects the coil in relay K1, causing it to switch to Standby.

When the video returns, the video loss fault is removed from the video fault input at J7-5. With jumper W1 in place

on J10, the base of Q16 goes high. The red Video Loss Fault LED DS9 on the front panel will be extinguished. Q16 is biased on, which causes its drain to go low. The low is wired to U5B, pin 5; U5B, pin 6, will be low if no ALC fault occurs. The two lows at the inputs make the output at U5B, pin 4, go high. The high is wired to Q18, which is biased on, causing the drain to go low. The low is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go low. The low connects to U5A, pin 1, and, if the translator is in Auto, pin 2 of U5A is also low. With both inputs low, the output of U5A at pin 3 goes high. The high forward biases Q20 and causes its drain to go low. The low connects to the operate coil on relay K1 that switches the translator to Operate. The low at U5C, pins 8 and 9, causes its output at pin 10 to go high. This high is connected to U5D, pin 12, and, if the translator is in Auto, pin 13 of U5D is low. The high on pin 12 causes the output of U5D to go low and reverse bias Q19. The drain of Q19 goes high and this removes the low from the standby coil in relay K1.

#### Overtemperature Fault

The (A8-A1) thermal switch on the (A8) output reject load connects to J8-1 on the board. If the temperature of the thermal switch raises above 170° F, it closes and applies a low to J8-1. The low connects to Q3, which is biased off, and to the red Overtemperature LED DS6, which is biased on. The drain of Q3 goes high and connects to pins 11 and 12 of U4B. The high at the input to U4B causes it to go high and switches the system to Standby; this removes the Operate Enable commands to the external amplifier trays and also to the (Optional) External Exhaust Kits.

#### VSWR Cutback Fault

The reflected power sample of the RF output of the translator is connected to J2, pin 9, on the translator control

board. The sample connects to op-amp U1B, pin 5, which buffers the signal before it is split. One of the split-reflected samples connects to J1-5 on the board; J1-5 is wired to J10-5 on the rear of the tray for remote monitoring. Another split-reflected sample connects to position 3 on the front panel meter for the tray. The final split remote-reflected sample connects to U2B, pin 5.

If the reflected sample level increases above the level set by R22, the VSWR cutback pot, the output of U2B at pin 7, goes high. The high is connected to Q11 through CR11, which is biased on, making U2C, pin 10, low and causing U2C, pin 8, to go low. This low is split and fed out of the tray at J1-6, J1-7, J1-8, and J1-9. These are ALC outputs to the amplifier tray that cut back the output power of the amplifier tray. The low from U2C, pin 8, is also fed through coaxial jumper W2 on J13 and J14 to R73. R73 is a bias-adjust pot that sets the level of the pin attenuator bias that is available as an output at J16. The high at U2B, pin 7, is also fed to the base of Q14 and Q13, which are forward biased. This produces a low at the drains that connect to the front panel amber VSWR Cutback LED DS7, causing it to light and indicate that the tray is in cutback, and to output jack J8-37 for the connection to a remote VSWR cutback indicator.

#### Receiver ALC Fault

A sample of the ALC voltage from the Receiver tray is connected to J8-11 on the transmitter control board. If the receiver is operating normally, the ALC level that is applied to U3C, pin 9, remains below the trip level set by R35; as a result, the output at pin 13 stays high. The high is applied to the red ALC Fault LED DS8, which is off. The high also connects to U3A, pin 2, and to Q15. Q15 is biased on and the drain goes low. The low connects to U5B, pin 6. In addition, U5B normally



has a low that is connected to U5B, pin 5, and produces a high at output pin 4. The high is wired to Q18, which is biased on, and makes its drain low. The low connects to U3D, pin 12, which, because the level is below the preset, causes the output at U3D, pin 14, to go low. A low at this point indicates a no-fault condition. The high that is connected to U3A, pin 2, causes its output to go low. The low is connected to Q25, which is biased off. The low is removed from J8-12, which will not light any remote receiver fault indicator that is connected to it.

If the receiver malfunctions, the ALC level applied to U3C, pin 9, goes high. This is above the level set by R35 and it causes the output at pin 13 to go low. The low is applied to the red ALC Fault LED DS8, which lights. The low also connects to U3A, pin 2, and to Q15. Q15 is biased off and the drain goes high. The high connects to U5B, pin 6, and produces a low at output pin 4. The low is wired to Q18, which is biased off, and this makes its drain go high. The high connects to U3D, pin 12 and, because the level is above the preset, the output at U3D, pin 14, goes high. A high at this point indicates a fault condition that switches the translator to Standby. The low connected to U3A, pin 2, causes its output to go high. The high is connected to Q25, which is biased on, and causes the drain to go low. The low is connected to J8-12, which can light any remote receiver fault indicator that is connected to it.

#### 4.2.7.5 Metering

The front panel meter connects to J3-1 (-) and J3-2 (+), the output of switch S3, on the transmitter control board. The front panel meter has seven metering positions that are controlled by S3: Audio, Video, % Aural Power, % Visual Power, % Reflected Power, % Exciter, and ALC. The video sample connects to the board at J5-4 and is connected through video calibration pot

R20 to position 6 on Front panel meter switch S3. The audio sample enters the board at J5-6 and is connected through audio calibration pot R19 to position 7 on Front Panel Meter switch S3.

The reflected sample connects to the board at J2-9 and is connected through buffer amplifier U1B and 100- $\Omega$  resistor R84 to position 3 on Front Panel Meter switch S3. The visual sample connects to the board at J2-5 and is connected through buffer amplifier U1D and 100- $\Omega$  resistor R86 to position 4 on Front Panel Meter switch S3. The aural sample connects to the board at J2-7 and is connected through buffer amplifier U1C and 100-ohm resistor R85 to position 5 on Front Panel Meter switch S3. The exciter sample connects to the board at J2-3 and is connected through buffer amplifier U1A and 100- $\Omega$  resistor R87 to position 2 on Front Panel Meter switch S3. The ALC sample connects to the board at J6-1 and is connected through buffer amplifier U2C, ALC calibration pot R15 (which adjusts the output of U2A, pin 1), and through 100- $\Omega$  resistor R18 to position 1 on Front Panel Meter Switch S3.

Typical readings on the meter are:

- Video = 1 Vpk-pk at white
- % Reflected = < 5%
- % Visual power = 100%
- % Aural power = 100%
- % Exciter = The level on the meter needed to attain 100% output power from the translator

Refer to the test data sheet for the translator for the actual reading:

- ALC = .8 VDC
- Audio =  $\pm 25$  kHz with a balanced audio input or  $\pm 75$  kHz with a composite audio input

Samples are provided for the remote metering of the exciter at J1-10, the visual at J8-26, the aural at J8-27, and the reflected at J1-5.

U6 is a temperature-sensor IC that gives the operator the ability to measure the temperature inside the tray by measuring the voltage at TP1. The sensor is set up for +10 mV equals 1° F (for example, 750 mV equals 75° F).

#### 4.2.7.6 Operational Voltages

The +12 VDC needed for the operation of the transmitter control board enters the board at jack J4, pin 3. C28, L1, and L3 are for the filtering and isolation of the +12 VDC before it is split and applied to the rest of the board. The -12 VDC needed for the operation of the board enters the board at jack J4, pin 5. C29 and L2 are for the filtering and isolation of the -12 VDC before it is split and applied to the rest of the board.

The +12 VDC is split when it is connected to the board. Four of the +12 VDC outputs are fed out of the board at J8-16, J8-17, J8-18, and J8-19 through diodes CR7, CR8, CR9, or CR10. Resistors R50, R51, R52, or R53 are fed to any external amplifier trays for use in their logic circuits. The +12 VDC is also fed to the (Optional) External Exhaust Kits in the Amplifier Array Assemblies. The resistors are for current limiting and the diodes are to prevent voltage feedback from the external amplifier trays.

#### 4.2.8 (A14) Channel Oscillator Assembly, Dual Oven (1145-1202; Appendix D)

The channel oscillator assembly contains (A14-A1) the channel oscillator board (1145-1201) that generates a stable frequency-reference signal of approximately 100 MHz. The channel oscillator assembly is an enclosure that provides temperature stability for the crystal oscillator. An SMA output at jack J1 and an RF sample at BNC connector jack J2 are also part of the assembly.

Adjustments can be made through access holes in the top cover of the assembly. These adjustments are set at the factory and should not be tampered with unless it is absolutely necessary and the proper, calibrated equipment is available. R1 is the temperature adjustment; C11 is the course-frequency adjustment; C9 is the fine-frequency adjustment; and C6, C18, L2, and L4 are adjusted for the maximum output of the frequency as measured at jacks J1 or J2.

The +12 VDC for the assembly enters through FL1 and the circuit-ground connection is made at E1.

#### 4.2.9 (A14) (Optional) VCXO Assembly, Dual Oven (1145-1206; Appendix D)

The VCXO assembly contains the VCXO channel oscillator board (1145-1204) which generates a stable frequency reference signal of approximately 100 MHz. The VCXO channel oscillator assembly is an enclosure that provides temperature stability for the crystal oscillator. An SMA output at jack J1 feeds the x8 multiplier assembly and an RF sample at BNC connector jack J2 provides an oscillator sample.

Adjustments are provided through access holes in the top cover of the assembly. These adjustments are set at the factory and should not be adjusted unless it is absolutely necessary and the properly calibrated equipment is available. R1 is the temperature adjustment; C11 is the course frequency adjustment; and C6, C18, L2, and L4 are adjusted for maximum output of the frequency as measured at jacks J1 or J2. The AFC voltage, which is fed to FL2 from an external source, is the fine frequency adjustment.

The +12 VDC for the assembly enters through FL1 and the circuit ground connection is made at E1.

#### **4.2.10 (A13) (Optional) EEPROM FSK Identifier Board (1265-1308; Appendix D)**

The optional FSK identifier board, with EEPROM, generates a morse code identification call sign by frequency-shift keying the VCXO oscillator in the upconverter or by sending a bias voltage to the IF attenuator board to amplitude modulate the aural carrier. This gives the station a means of automatically repeating its identification call sign, at a given time interval, to meet FCC requirements.

The starting circuit is made up of U1B and U1D, which are connected as a flip-flop, with gate U1A used as the set flip-flop. U1A automatically starts the flip-flop each time U3 completes its timing cycle. At the start of a cycle, U1B enables clock U2. U2 applies the clock pulses that set the speed, which is adjusted by R2, for when the identification code is sent to 12-bit binary counter U4. R2, fully clockwise (CW), is the fastest pulse train and R2, fully counter-clockwise (CCW), is the slowest pulse train. U4 provides binary outputs that address EEPROM U5.

The scans in U4 will continue until field effect transistor (FET) Q1 is gated on. The gate of Q1 is connected to pin 13 on U4, which is the maximum count used in the EEPROM, and will provide a reset pulse each time the binary counter goes high on pin 13. The reset pulse, when the drain of Q1 goes low, is applied to the flip-flop and the timer U3, which determines the length of time between the sending of the identification code. R14 is adjusted to set this time interval. R14, fully CW, is the longest interval between identification calls, approximately eight minutes. R14, fully CCW, is the shortest interval between the sending of the code (approximately 10 seconds).

U6B is an amplifier connected to the output of U5, which turns the LED DS1 on and off at the rate set by R2. This gives the operator a visual indication that the FSK identifier board is operating and at the rate at which it is operating.

The data output of U5, which is serial, is connected to U6A, whose output shifts low and high, and is applied to the VCXO board, which shifts the frequency according to the programming of U5. The deviation of the shift is adjusted by R4 and is typically set at 1 kHz. Once R4 is set, R9 is re-adjusted to -1.5 VDC at J3-2.

The +12 VDC from an external power supply enters the board at J1, pin 3. The voltage is fed through RF choke L1 and is filtered by C1 before being applied to the rest of the tray. The +12 VDC is also applied to U7, which is a voltage regulator that regulates its output at +5 VDC. The +5 VDC is fed to the ICs on the board. The -12 VDC from an external power supply enters the board at J1, pin 5. The voltage is fed through RF choke L2 and filtered by C2 before being applied to the rest of the tray.

#### **4.2.11 (A24) (Optional) Composite 4.5-MHz Filter Board (1227-1244; Appendix D)**

The composite 4.5-MHz filter board is mounted in the UHF exciter tray and is part of the composite 4.5-MHz input kit. The board filters the 4.5-MHz composite signal to produce a video-only output that connects to the sync tip clamp/modulator board.

The composite 4.5-MHz signal from the sync tip clamp/modulator board enters the board at J1 and is amplified by U1A and then split. A sample of the composite 4.5-MHz signal is connected out of the board at J2 and connects to the 4.5-MHz bandpass filter board. The other split portion of the composite 4.5-

MHz signal is connected to a four-section, low-pass filter circuit, which is adjusted by C2, L1, C5, L2, C8, L3, L4, C11, L5, C15, L6, and C19, and has a sharp roll-off that eliminates the 4.5-MHz signal. The filter is set up at the factory for the desired video-only output and should not be adjusted by the customer. The video low-pass signal is amplified by U2B and applied to the video low-pass output jack of the board at J5, which is connected to the sync tip clamp/modulator board. C21, with jumper W1 on J9, can be adjusted to set up the frequency response of the video. The video-only signal is amplified by U2A and connected to three group delay circuits, which are adjusted by L8 and R18, L9 and R22, and L10 and R27. These circuits correct for frequency-response problems created by the filtering process.

A 4.5-MHz intercarrier signal from the 4.5-MHz bandpass filter board connects to J3, the intercarrier input jack. The intercarrier signal is amplified by U1B, whose gain is set by R38, and connected out of the board at J4. The 4.5-MHz signal connects to J28 on the sync tip clamp/modulator board.

The  $\pm 12$  VDC needed by the board is supplied by an external power supply in the tray. The +12 VDC enters the board at J8, pin 3, and is filtered and isolated from the rest of the tray by L12 and C36 before being applied to the rest of the board. The -12 VDC enters the board at J8, pin 5, and is filtered and isolated from the rest of the tray by L32 and C37 before being applied to the rest of the board.

#### **4.2.12 (A25) (Optional) 4.5-MHz Bandpass Filter Board (1265-1307; Appendix D)**

The 4.5-MHz bandpass filter board passes the 4.5-MHz aural subcarrier frequency and filters out any out-of-band products that may be present.

The board consists of two circuits: a bandpass filter circuit and an envelope delay equalizer circuit. The filter circuit has a bandpass characteristic that is relatively flat around the aural subcarrier frequency of 4.5 MHz  $\pm 100$  kHz. It also has zeros (or notches) at frequencies near 4 and 5 MHz that prevent asymmetrical envelope delay error in the pass-band. There is some symmetrical delay error introduced, but this is corrected by the envelope delay equalizer circuit portion of the board. This circuit places a hump for correction in the center of the band at 4.5 MHz.

The composite input to the board is through J1 at an impedance of 75 $\Omega$ . The filter circuit consists of the capacitors C1 to C11 and inductors L1 to L5. The variable components L2, C3, L4, and C7 are tuned for a peak in the response around 4.5 MHz; this forms a relatively flat-frequency response of 4.5 MHz  $\pm 100$  kHz. The filtered output is amplified by U1A before it is connected to the envelope delay equalizer circuit.

The equalizer portion of the board consists of capacitors C14 to C19 and inductors L6 and L7. The tuning of the equalizer is accomplished by removing jumper W1 on J5 and adjusting L6 for a notch in the frequency response at the desired maximum envelope delay frequency. Replace jumper W1 on J5, the Operate position, and tune C19 for a flat response around 4.5 MHz. The L-pass network creates a flat response around 4.5 MHz and also generates a hump in the envelope delay response to cancel the effects caused by the filter half of the board that proceeds it.

The filtered and equalized output is amplified by U1B and connected to J2, the output jack of the board.

The DC voltages needed to operate the board enter at jack J4. The +12 VDC connects to the board at J4-3 and is filtered and isolated by L8 and C20 before it is connected to the rest of the

board. The -12 VDC connects to the board at J4-5 and is filtered and isolated by L9 and C21 before it is connected to the rest of the board.

#### **4.2.13 (A3)+12V(4A)/-12V(1A) Power Supply Board (1265-1312; Appendix D)**

The  $\pm 12$ -volt power supply board consists of three separate power supplies, two of which produce the +12 VDC and one for the -12 VDC needed to power the circuit boards in the exciter tray.

##### *4.2.13.1 +12 VDC Power Supply*

The 18 VAC from the external step-down toroid in the tray connects to J1, pins 7 and 8. The 18 VAC connects through 7-amp fuse F2, for over-current protection, to two full-wave bridge rectifier circuits.

CR1, CR2, CR3, and CR4 rectify the AC that is then filtered by C2 and connected to U3 and U4; U3 and U4 are voltage-regulator ICs for the +12 VDC. The voltage-regulated and current-limited +12-VDC output of U3 connects to J4, pins 1, 2, 3, and 4, which is one of the +12-VDC outputs of the board. The green LED DS3 will be lit if +12 VDC is present to J4; C7 and C8 are bypass capacitors. The +12 VDC output of U4 connects to J5, pins 1, 2, 3, and 4, which is another one of the +12-VDC outputs of the board. The green LED DS4 will be lit if +12 VDC is present to J5; C9 and C10 are bypass capacitors.

CR5, CR6, CR7, and CR8 rectify the AC that is then filtered by C1 and connected to U1 and U2; U1 and U2 are voltage-regulator ICs for the +12 VDC. The voltage-regulated and current-limited +12-VDC output of U1 connects to J6, pins 1, 2, 3, and 4, which is one of the +12-VDC outputs of the board. The green LED DS1 will be lit if +12 VDC is present to J6; C3 and

C4 are bypass capacitors. The +12-VDC output of U2 connects to J3, pins 1, 2, 3, and 4, which is another one of the +12-VDC outputs of the board. The green LED DS2 will be lit if +12 VDC is present to J3; C5 and C6 are bypass capacitors.

##### *4.2.13.2 -12 VDC Power Supply*

The 18 VAC from an external step-down toroid connects to J1, pins 1 and 4, of the board and is wired to CR9, CR10, CR11, and CR12 which form a full-wave bridge rectifier network for the -12-VDC power supply. F1 is a 3-amp fuse that provides over-current protection. The rectified output is filtered by C11 and fed to U5, the voltage-regulator IC for the -12 VDC. The voltage-regulated and current-limited -12 VDC is connected to the -12-VDC output jacks J7, pins 5 through 10, and J8, pins 5 through 10. The green LED DS5 will be lit if -12 VDC is present to J7 and J8; C12 and C13 are bypass capacitors.

#### **4.2.14 (A15) x8 Multiplier Enclosure (1265-1347; Appendix D)**

The x8 multiplier enclosure is an aluminum box that provides RFI and EMI protection for the x8 multiplier board (1227-1002) that is mounted inside of it. This protection is needed to prevent any interference from obstructing the upconversion process.

The output from the channel oscillator at +5 dBm enters the enclosure at J1. The oscillator signal is multiplied and amplified by the x8 multiplier board to +16 dBm and sent out of the enclosure at J2.

The +12 VDC needed to operate the board enters the enclosure through FL1 and connects to J3-3 on the board. The return for the +12 VDC enters the enclosure through E1 and connects to J3-4 on the board.

#### **4.2.15 (A15-A1) x8 Multiplier Board (1227-1002; Appendix D)**

The x8 multiplier board multiplies the frequency of an RF input signal by a factor of eight. The board is made up of three identical x2 broadband frequency doublers.

The input signal (+5 dBm) at the fundamental frequency enters through SMA jack J1 and is fed through a 3-dB matching pad, consisting of R1, R2, and R3, to amplifier IC U1. The output of the amplifier stage is directed through a bandpass filter, consisting of L2 and C4, that is tuned to the fundamental frequency (87 to 114 MHz). The voltage measured at TP1 is typically +.6 VDC.

The first doubler stage consists of Z1 with bandpass filter L3 and C6 tuned to the second harmonic (174 to 228 MHz). The harmonic is amplified by U2 and it is again bandpass filtered at the second-harmonic frequency by C10 and L5 (174 to 228 MHz). The voltage measured at TP2 is typically +1.2 VDC.

The next doubler stage consists of Z2 with bandpass filter C12 and L6 tuned to the fourth harmonic of the fundamental frequency (348 to 456 MHz). The fourth harmonic is then amplified by U3 and fed through another bandpass filter, consisting of L11 and C18, that is tuned to the fourth harmonic (348 to 456 MHz). The voltage measured at TP3 is typically +2.0 VDC.

The final doubler stage consists of Z3 with bandpass filter C20 and L12 tuned to the eighth harmonic of the fundamental frequency (696 to 912 MHz). The signal is amplified by U4, U5, and U6 to a typical value of +2 to +4 VDC as measured at test point TP4. The amplified eighth harmonic is then fed to J2, the SMA output jack of the board. The typical LO signal output level is +15 dBm nominal.

The detected sample of the output of the x8 multiplier board at TP4 is also fed to the base of Q1, which forward biases it and lights the green LED DS1 on the board to indicate that the LO signal is present.

The +12 VDC for the board enters through jack J3-3 and is filtered by L7 and C16 before being distributed to the circuits on the board.

#### **4.2.16 (A12 and A16) UHF Filters (1007-1101; Appendix D)**

Each of the UHF filters is a tunable two-section cavity filter that is typically tuned for a bandwidth of 6 MHz and has a loss of -1 dB through the filter.

#### **4.2.17 (A11) UHF Upconverter Board (1265-1310; Appendix D)**

The UHF upconverter board provides upconversion processing by mixing the IF and LO signals in mixer Z1 to produce the desired RF-frequency output. The RF output is connected through J3 to an external filter and applied back to the board at J4 where the gain is set by R10. The RF is amplified and connected to the RF output jack of the board at J5.

The IF signal (0 dBm) enters the board at J1, an SMA connector, and is applied through a filter circuit consisting of L10 and C25 to C28 and to a matching pad. This pad consists of R1, R2, and R3, which presents a relatively good source impedance, and feeds the signal to pins 3 and 4, the I input of mixer Z1. The local oscillator signal (+13 dBm) from the x8 multiplier connects to the board at jack J2, an SMA connector, through a UHF channel filter and is connected directly to pin 8, the L input of the mixer.

The frequency of the LO is the sum of the IF frequency above the required visual carrier. For instance, in system M, the IF visual frequency is at 45.75 MHz and the relative location of the aural would be 4.5 MHz lower, or 41.25 MHz. For digital applications, the LO is the center frequency of the digital channel added to the 44-MHz IF frequency. By picking the local oscillator to be 45.75 MHz above the visual carrier, a conversion in frequency occurs by selecting the difference product. The difference product, the local oscillator minus the IF, will be at the required visual carrier frequency output. There will also be other signals present at the RF output connector J3 at a lower level. These are the sum conversion product: the LO and the IF frequencies. Usually, the output product that is selected by the tuning of the external filter is the difference product: the LO minus the 45.75-MHz IF. The difference product has its sidebands flipped so that the visual carrier is lower in frequency than the aural carrier.

If a bad reactive load is connected to the mixer, the LO signal that is fed through it can be increased because the mixer no longer serves as a double-balanced mixer. The mixer has the inherent property of suppressing signals that may leak from one input port to any of the other ports. This property is enhanced by having the inputs and outputs of the mixer at a 50- $\Omega$  impedance. The reactive filter that is externally connected to J3 of the board does not appear as a good 50- $\Omega$  load at all frequencies. The pad, in the output line of the board, consists of R5, R4, R6, and R7. The pad buffers the bad effects of the reactive filter load and makes it appear as a 50- $\Omega$  impedance. The RF signal is amplified by U1, a modular amplifier, and contains biasing and impedance-matching networks that makes U1 act as a wideband-RF amplifier device. This amplifier, in a 50- $\Omega$  system, has

approximately 12 dB of gain. U1 is powered from the +12-VDC line through RF decoupling components R27, R28, C30, R8, and L1. Inductor L1 is a broadband-RF choke and is resonance free through the UHF band. The amplified RF connects to SMA RF output jack J3, which is cabled to the external filter.

The RF input signal from the external filter re-enters the board at J4 (-11 to -14 dBm) and is capacitively coupled to the pin-diode attenuator circuit consisting of CR1, CR2, and CR5. The pin-diode attenuator acts as a voltage-variable attenuator in which each pin diode functions as a voltage-variable resistor that depends on the DC bias supplied to the diode for its resistance value. The pin diodes, because of a large, intrinsic region, cannot rectify signals at this RF frequency; as a result, they act as a linear voltage-variable resistor.

The pin diodes are configured in shunt configuration: CR1 is the first shunt element, CR2 is the second shunt element, and CR5 is the series element. The manual gain AGC, W1 on J10 between pins 1 and 2, is used in most cases. The control voltage from manual gain pot R10 sets up a current path through R11 and the diodes in the pin attenuator. The level-controlled RF signal, from the pin-diode attenuator circuit, is amplified by wideband-hybrid amplifier IC U2 that is configured in the same way as U1. The RF signal is buffered by Q1 and applied to the push-pull Class A amplifier circuit consisting of Q2 and Q3. At the input to the transistors, the RF is converted to a balanced, dual feed by balun L4, which is made from a short length of UT-141 coaxial cable.

Capacitors C12 and C13 provide DC blocking for the input signal to the amplifier devices. The RF outputs at the collectors of the transistors are applied through C19 and C20, which provide

DC blocking for the output signals. The RF signals connect to L7, which consists of UT-141 coaxial cable. L7 combines the RF back to a single-RF output at a 50- $\Omega$  impedance and sends it to L8, which provides a sample of the RF. The main path through L10 is to J5, the RF output jack of the board (+10 to +20 dBm). The sample of the RF connects to a splitter that provides a sample output (0 dBm) at J6 of the board. The other output of the splitter connects to a peak-detector circuit consisting of CR3 and U3, which provides a DC level at J7 that represents the RF output of the UHF exciter to the front panel meter. R29 sets up the calibration of the front panel meter for 100% in the UHF Exciter position when the output power of the exciter is at +17 dBm peak visual or +10 dBm average for digital applications.

The board is powered by  $\pm 12$  VDC that is produced by an external power supply. The +12 VDC enters the board through J8, pin 3, and is filtered and isolated by RF choke L9 and shunt capacitors C24 and C33. This circuit isolates the RF signals from the board away from those of other devices connected to the same +12 VDC line external to the UHF upconverter board. The +12 VDC is then applied to the rest of the board.

The -12 VDC enters the board through J8, pin 5, and is filtered and isolated by RF choke L11 and shunt capacitors C34 and C35. This circuit isolates the RF signals from this board away from those of other devices connected to the same -12 VDC line external to the UHF upconverter board; the -12 VDC is then applied to the rest of the board.

#### **4.2.18 (A1) Power Entry Module Assembly (1227-1206; Appendix D)**

The power entry module assembly provides overvoltage and surge protection for the input AC lines that connect to the exciter tray. The AC

input plug connects to J14; J14 is part of the power entry module on the rear panel of the exciter tray.

The module assembly contains two 130-VAC varistors and one 250-VAC varistor that connect across the AC lines and to ground. The module also contains two 4-amp fuses for overcurrent protection, one in each input line.

### **4.3 (A4 and A5) Variable Phase/Gain Trays (1245-1200; Appendix C)**

The Variable Phase/Gain Tray sets the phase and gain adjustments of the RF to provide maximum output when the outputs of the two Amplifier Arrays are combined. There are two Variable Phase/Gain Trays in the 837B UHF Translator, each controlling the phase and gain of one of the two Amplifier Arrays.

The Tray is made up of (A4) a Variable Phase/Gain Assembly (1245-1204), which contains (A4-A1) a Variable Phase/Gain Board (1245-1201), (A5) a Metering Board (1245-1202) and (A3) a +15V/-12V Power Supply Board (1245-1203).

#### **4.3.1 (A4-A1) Variable Gain/Phase Board (1245-1201; Appendix D)**

The RF Input signal connects to the rear panel of the Tray at J1 and is cabled to J1 on (A4-A1) the Variable Phase/Gain Board (1245-1201) that is mounted inside (A4) the Variable Phase/Gain Assembly (1245-1204) for RFI and EMI protection. The Variable Phase/Gain Board contains two main circuits, one for ALC and one for Phase adjustment of the RF signal. A front panel mounted ALC adjust Pot (A8) connects through (A5) the Metering Board (1245-1202) to J5 on the Board which controls the output level to the tray. A front panel mounted Phase



adjust Pot (A7) connects through the Metering Board to J4 on the Variable Phase/Gain Board which controls the phasing of the RF output. The Phasing adjust is needed to phase the two RF outputs of the Amplifier Arrays, when they are combined, to achieve maximum output. The phase and level controlled RF signal connects to J2 of the Variable Phase/Gain Board which connects to the RF Output Jack J3 located on the rear panel of the Tray. A sample of the RF from the Variable Phase/Gain Board connects to J4 the output Sample Jack located on the front panel of the Tray.

#### **4.3.2 (A5) Metering Board (1245-1202; Appendix D)**

A detected output sample level connects to the Metering Board at J7 Pins 3 & 4 which is connected to the % Power Level position on (A6) the front panel meter of the Tray. S1 is a two position front panel mounted switch that allows the operator to view the ALC Level, typically reads .6V - 1V, or the % Power, which is calibrated for 100 % is +23 dBm output.

#### **4.3.3 (A1) Power Entry Module Assembly (1227-1206; Appendix D)**

120/240 VAC connects to the Tray at J2 on (A1) the Power Entry Module Assembly. Jumpers on the Power Entry Module are set for the desired AC Voltage Input. The assembly contains an On/Off Switch, two 4 Amp Fuses and three Varistors for AC line protection. The AC is connected to (A2) a step down Toroid that supplies an 18 VAC output to the +15VDC/-12VDC Power Supply Board.

#### **4.3.4 (A3) +15V/-12V Power Supply Board (1245-1203; Appendix D)**

The +15 VDC and -12 VDC needed to operate the boards in the Tray are generated on (A3) the +15 VDC/-12

VDC Power Supply Board (1245-1203). The +15VDC/-12VDC Power Supply Board supplies voltage regulated +15 VDC and -12 VDC Outputs to the rest of the Tray. The Green LED DS1 is lit if +15 VDC is present and the Green LED DS2 is lit if -12 VDC is present at the output of the +15V/-12V Power Supply Board.

#### **4.4 (A6) Metering Panel (1136811 or 1245-1400; Appendix C)**

The Metering Panel provides three meters, one for Combined, one for Side A Amplifier Array and one for Side B Amplifier Array Outputs. The Side A Meter (A15) displays the % Forward and the % Reflected Power samples for the Side A Amplifier Array. The Side B Meter (A17) displays the % Forward and the % Reflected Power samples for the Side B Amplifier Array. The Combined Meter (A13) displays the % Reject, % Visual, % Aural and the % Reflected Power samples for the Combined Output of the 4-6 kW Translator. The Metering Panel also takes the ALC Reference Inputs from the (A4 & A5) Variable Phase/Gain Trays and splits them six ways which are then connected to the UHF Amplifier Trays in the two amplifier arrays.

The Metering Panel (A6) contains (A4, A5, A6 & A11) four Splitter Boards (1181-1002), (A7, A8 & A9) three Dual Peak Detector Modules (1159965), (A10) a Visual/Aural Metering Board (1265-1309), (A18) a Detector Threshold Board (1245-1402) and (A3) a  $\pm 12$ V Power Supply Board (1062-1013).

The (A13) Front Panel Meter monitors the Combined Output Power and is controlled by (S1) the Meter Control Switch. The (A15) Front Panel Meter monitors the Side A Output Power with (S2) the Meter Control Switch. The (A17) Front Panel Meter monitors Side

B Output Power with (S3) the Meter Control Switch.

#### **4.4.1 (A4, A5, A6 & A11) Splitter Board (1181-1002; Appendix D)**

The (A4) Splitter Board (1181-1002) takes the ALC reference from the (A4) Variable Phase/Gain Tray at J1-1 and splits it six ways that connect to the UHF Amplifier Trays mounted in the Side A Amplifier Array.

The (A5) Splitter Board (1181-1002) takes the ALC reference from the (A5) Variable Phase/Gain Tray at J1-1 and splits it six ways that connect to the UHF Amplifier Trays mounted in the Side B Amplifier Array.

The (A6) Splitter Board takes the Combined Reflected Sample Input at J1-1 and splits it. One of the split Combined Samples connects to the front panel Meter, one is used for Remote Monitoring and the other two connect back to the UHF Exciters for use in the VSWR Cutback circuitry.

The (A11) Splitter Board (1181-1002) takes the Combined Aural Sample Input at J1-1 from the (A10) Visual/Aural Metering Board and splits it. One of the split Aural Samples connects to the front panel Meter and the other is used for Remote Monitoring.

#### **4.4.2 (A10) Visual/Aural Metering Board (1265-1309; Appendix D)**

The (A10) Visual/Aural Metering Board has a Combined Forward Sample from the Output Coupler Assembly of the Translator connected to J1 on the Board where it is split. One Forward Sample connects to J2 on the board that is cabled to J9, the Translator Output Sample Jack, located on the front panel of the Metering Panel. The Combined Forward Sample on the Visual/Aural Metering Board is split again with one Sample used to produce

a Combined Visual Sample, that connects to the front panel Meter (A13) and also to the rear panel for Remote monitoring. The other Combined Forward Sample produces a combined Aural Sample that connects to the (A11) Splitter Board.

#### **4.4.3 (A7, A8 & A9) Dual Peak Detectors (1159965; Appendix D)**

The (A7) Dual Peak Detector takes the Combined Reflected Sample Input from the Output Coupler Module and splits it. A peak detected output of the reflected sample connects to the (A6) Splitter Board. The (A7) Dual Peak Detector also has a Reject Sample Input from the Reject Output Coupler Module and splits it. One of the peak detected split Reject Samples connects to the front panel Meter and the other is used for Remote Monitoring.

The (A8) Dual Peak Detector Module takes a Reflected Sample from the Side B Amplifier Array that is peak detected and connected to the (A17) front panel meter. Another input to the (A8) Dual Peak Detector Module is a Forward Sample from the Side B Amplifier Array that is peak detected and connected to the (A17) front panel meter.

The (A9) Dual Peak Detector Module receives the Reflected Sample from the Side A Amplifier Array which is peak detected and connected to the (A15) front panel meter. Another input to the (A9) Dual Peak Detector Module is the Forward Sample from the Side A Amplifier Array which is peak detected and connected to the (A15) front panel meter.

#### **4.4.4 (A18) Detector Threshold Board (1245-1402; Appendix D)**

The Detector Threshold Board consists of three identical signal paths. One path uses a detected Reflected sample from Side A, another the detected Reflected sample from Side B and the

final path uses a detected Combined Reflected sample. These samples are compared to the threshold settings, 20% Reflected level, and provide an output to cut back the translator if the reflected level of any of the input samples increase above 20%.

A Sample of the Side A Reflected level enters the board at J1-1. The level is split and one path connects to J1-2 to be used as a Side A Remote Reflected output. The other path connects to the Operational Amplifier U1A whose turn on level is controlled by the setting of R5. R5 is set to cause U1A to conduct if the reflected sample input increases above the 20% level. The output, at J2-1 and also J2-5 through the jumper W1 on J4, connects to the Transmitter Control Board, located in the UHF Exciter, where it cuts back the translator using the VSWR cut back circuits.

A Sample of the Side B Reflected level enters the board at J8-1. The level is split and one path connects to J8-2 to be used as a Side B Remote Reflected output. The other path connects to the Operational Amplifier U1B whose turn on level is controlled by the setting of R12. R12 is set to cause U1B to conduct if the reflected sample input increases above the 20% level. The output, at J2-5 and also J2-1 through the jumper W1 on J4 connects to the Transmitter Control Board, located in the UHF Exciter, where it cuts back the translator using the VSWR cut back circuits.

A Sample of the Combined Reflected level enters the board at J7-1. The level is split and one path connects to J7-2 to be used as a Remote Combined Reflected output. The other path connects to the Operational Amplifier U1C whose turn on level is controlled by the setting of R19. R19 is set to cause U1C to conduct if the combined reflected input sample increases above the 20% level. The output, at J6-1 and

also J2-5 through the jumper W2 on J5 connects to the Transmitter Control Board, located in the UHF Exciter, where it cuts back the translator using the VSWR cut back circuits

#### **4.4.5 (A1) Power Entry Module Assembly (1227-1206; Appendix D)**

120/240 VAC connects to the Tray at J8 on (A1) the Power Entry Module Assembly. Jumpers on the Power Entry Module are set for the desired AC Voltage Input. The assembly contains an On/Off Switch, two 4 Amp Fuses and three Varistors for AC line protection. The AC is connected to (A2) a step down Toroid that supplies an 18 VAC output thru TB1 to the  $\pm 12V$  Power Supply Board.

#### **4.4.6 (A3) $\pm 12V$ Power Supply Board (1062-1013; Appendix D)**

The  $\pm 12$  VDC needed to operate the Boards in the Metering Panel are provided by the  $\pm 12$  VDC Power Supply Board (1062-1013).

The 18 VAC, from an external step-down Transformer, is directed to the Board thru J5 Pins 1 & 4, with Pin 2 connected to the center tap of the secondary of the Transformer.

The +12 VDC is produced by using a Full-Wave rectifier circuit consisting of CR1 and CR2 whose output is filtered by capacitor C1 and bypassed by C2 to prevent oscillations. The filtered +12 VDC is applied to U1 a 7812 IC voltage regulator and current limiter. C3 is a bypass capacitor to prevent oscillations in the output DC lines. DS1 is a Green LED which when lit indicates that the +12VDC is present at the output of the board. The +12 VDC is distributed thru Pins 2 & 7 of each of the Output Jacks, J1, J2, J3 & J4, to the rest of the boards in the Tray.

The -12 VDC is produced by using a Full-Wave rectifier circuit that consists of CR3 and CR4 whose output is filtered

by capacitor C4 and bypassed by C5 to prevent oscillations. The filtered -12 VDC is applied to U2 a 7912 IC voltage regulator and current limiter. C6 is a bypass capacitor to prevent oscillations in the output DC lines. C7 is a holding capacitor to maintain -12VDC for an instance even if the supply is lost. This is to allow the positive voltages to be removed from the Amplifier devices to prevent damage to the devices. DS2 is a Green LED which when lit indicates that the -12 VDC is present at the output of the board. The -12VDC is distributed to the rest of the Boards in the Tray thru Pins 4 & 5 of each of the Output Jacks, J1, J2, J3 & J4.

The  $\pm 12$  VDC outputs of the board are connected to the rest of the boards in the Metering Panel.

#### **4.5 (A8) AC Distribution Assembly (1245-1500; Appendix C)**

The AC Distribution Assembly distributes the Main AC Input, 208/240 VAC @ 20 Amps, that connects to the UHF Exciter Assembly Cabinet to the Trays and Assemblies which make up the Exciter.

The 208/240 VAC Main AC Input to the Exciter Cabinet connects to the Terminal Block TB1, Line 1 to TB1-1A, Line 2 to TB1-3A and Ground to TB1-2A.

The 208/240 VAC Main AC Input connects from the Terminal Block TB1-1B (Line 1) to the 20 Amp Circuit Breaker CB1-1, TB1-2B (Ground) to Chassis Ground & TB1-3B (Line 2) to the Circuit Breaker CB1-3. Three MOVs, for surge and transient protection, are connected to the AC Lines from the Circuit Breaker, VR1 from Line 1 to Ground, VR3 from Line 2 to Ground and VR2 across the AC Lines.

The switched 208/240 VAC Main AC Input is wired from the Circuit Breaker

Terminal 2 to the L inputs and Terminal 4 to the N Inputs of the (A1 & A2) IEC Outlet Strips. The E Inputs to both IEC Outlet Strips connect to Chassis Ground.

There are four outputs for both the (A1) and the (A2) IEC Outlet Strips. On the A1 Outlet Strip, J1 connects to J14 on the (A1) Exciter #1, J2 connects to J14 on the (Optional) (A2) Exciter #1, J3 connects to J8 on the (Optional) (A3) Exciter Switcher Tray and J4 connects to J2 on the (A4) Variable Phase/Gain Tray. On the A2 Outlet Strip, J5 connects to J2 on the (A5) Variable Phase/Gain Tray, J6 connects to J8 on the (A6) Metering Panel, J7 connects to J2 on the (A7) Receiver Tray or to the AC Input Jack on the (Optional) Digital Modulator and J8 is not used in this System.

#### **4.6 (A2 & A3) 2-3 kW Amplifier Arrays (1278-1300; Appendix C)**

There are two Amplifier Array Assemblies in the 837B 4-6 kW UHF Solid State Internally Diplexed Television Translator. The (A2 & A3) Amplifier Array Assemblies (1278-1300) are identical. Each Amplifier Array contains; (A9-A1) an 8 Way Splitter (ZFSC-8-43), (A1 thru A4, A5(5kW) and A6(6kW)) UHF Amplifier Trays, (A7) a 4, 5 or 6 Way Combiner, (A12) a Reject Load Assembly (Only with 5 & 6 kW transmitters), (A8) an Output Coupler, (A10) an AC Distribution Assembly (1278-1100 three phase or 1278-1200 single phase) and (A11) an Interface Panel.

The output of the (A4) Variable Phase/Gain Tray, located in the Exciter Assembly, connects to (A2) the Side A Amplifier Assembly. The output of the (A5) Variable Phase/Gain Tray connects to (A3) the Side B Amplifier Assembly. The RF Input (+16 dBm) from the Variable Phase/Gain Tray connects to the RF Input Jack J1 on (A11) the

Interface Panel located in the Amplifier Array Assembly. The RF is cabled to the COM Input of (A9-A1) the 8 Way Splitter that splits it eight ways. Four, five or six of the RF outputs (+6 dBm) of the Splitter are connected to J1, the RF Input Jack on each of the four, five or six UHF Amplifier Trays. The outputs of the Splitter that are not used are terminated with 50Ω. Each of the UHF Amplifier Trays amplify the RF signals to approximately (+60 dBm), which is the power needed to produce a total of 4000 - 6000 Watts Peak of Sync after combining of the two Amplifier Assemblies, with a maximum of 600 Watts Peak of Sync output per Tray. The outputs of the UHF Amplifier Trays are combined in the (A7) 4, 5 or 6 Way Combiner. The Reject Output of the Combiner is connected to (A12) the Reject Load Assembly (Only in 5 or 6 kW transmitters).

The RF Output of the Combiner is connected to (A8) the Output Coupler Assembly which supplies a Forward and a Reflected Power Sample of the output from the Amplifier Assembly that connect through the SMA Connectors J2 and J3 located on the (A11) Interface Panel to the Metering Panel located in the UHF Exciter Assembly.

The RF output of the Amplifier Array (+63.5 to +65.2 dBm) is at J2 (1-5/8") of the Output Coupler.

In each UHF Amplifier Tray, a Forward Power Sample and a Reflected Power Sample, from the 4 Way Combiner Board, are connected to the Dual Peak Detector Board, Single Supply. The Dual Peak Detector provides peak detected forward samples to the Amplifier Control Board that supplies the samples to the front panel meter of the UHF Amplifier Tray and also to the Interface Panel for remote monitoring. Before exiting each UHF Amplifier Tray the RF is fed through a Circulator which protects the Tray from high VSWR

conditions. The Reject Port of the Circulator provides a Reject Sample to the 4 Way Combiner Board which supplies the Reflected Sample to the Dual Peak Detector Board, Single Supply located in the UHF Amplifier Tray that connects to the front panel meter.

The two power supply Enable (Operate) Commands from the UHF Exciter Tray, located in the UHF Exciter Assembly, connect to the Terminal Block (A9-TB2) mounted in each Amplifier Array. The terminal block splits the Enables fur, five or six ways in each array and supplies them to all of the UHF Amplifier Trays. The Enable is needed to turn on the Switching Power Supply located in each UHF Amplifier Tray. If the Amplifier Array contains an (Optional) External Exhaust Kit, then a Fan Enable is supplied at J4-19 along with +12V at J4-20 that connect to the fan mounted on the roof, which turns it on.

### **Main AC Input**

Each Amplifier Assembly needs an AC Input of 208/240 VAC at 55 Amps three phase or 100 Amps Single Phase wired to it. The 208/240 VAC Input to each Amplifier Assembly connects to (A10) the AC Distribution Assembly, Amplifier Array (1278-1100 three phase or 1278-1200 single phase) located on the right side, center rear of each Cabinet. Each AC Distribution Assembly contains the Terminal Block (TB1) to which the 208/240 VAC connects.

For three phase, connect Line 1 to TB1-1A, Line 2 to TB1-2A, Line 3 to TB1-3A and Ground to TB1-4A. The AC Distribution Panel contains Circuit Breakers that supply the AC to the rest of the Amplifier Assembly. The Input AC from TB1 is connected to (CB1) the Main AC Circuit Breaker (55 Amps) that distributes the 220 VAC to the other circuit breakers (CB2-CB9). The output of CB1 has six MOVs for protection, VR1 from Line 1 to Line 2, VR2 from

Line 2 to Line 3, VR3 from Line 1 to Line 3, VR4 from Line 1 to Ground, VR5 from Line 2 to Ground and VR6 from Line 3 to Ground.

For single phase, connect Line 1 to TB1-1A, Line 2 to TB1-3A and Ground to TB1-4A. The AC Distribution Panel contains Circuit Breakers that supply the AC to the rest of the Amplifier Assembly. The Input AC from TB1 is connected to (CB1) the Main AC Circuit Breaker (100 Amps) that distributes the 220 VAC to the other circuit breakers (CB2-CB9). The output of CB1 has three MOVs, VR4 from Line 1 to Ground, VR6 from Line 2 to Ground and VR3 connected across the legs.

The switched Input AC is wired through six Circuit Breakers, CB2-CB7, to the six UHF Amplifier Trays in the Amplifier Array Cabinets. CB2 is a 20 Amp Circuit Breaker that supplies the AC voltage to the (A1) UHF Amplifier Tray. CB3 is a 20 Amp Circuit Breaker that supplies the AC voltage to the (A2) UHF Amplifier Tray. CB4 is a 20 Amp Circuit Breaker that supplies the AC voltage to the (A3) UHF Amplifier Tray. CB5 is a 20 Amp Circuit Breaker that supplies the AC voltage to the (A4) UHF Amplifier Tray. In 5 & 6 kW, CB6 is a 20 Amp Circuit Breaker that supplies the AC voltage to the (A5) UHF Amplifier Tray. In 6 kW, CB7 is a 20 Amp Circuit Breaker that supplies the AC voltage to the (A6) UHF Amplifier Tray. CB8 and CB9 are 3 Amp circuit breakers that supply AC to the two cooling fans located in the Reject Load Assembly.

When the Circuit Breaker CB1 on the AC Distribution Assembly in the UHF Exciter Assembly is switched On, +12 VDC from the Exciter is supplied to each of the Amplifier Array Cabinets. In the Amplifier Array, the +12 VDC is split and connected to each of the UHF Amplifier Trays for operation of the LED Status Indicators in the Tray. +12 VDC from the Exciter is also supplied to each

of the (Optional) External Exhaust Kits in the Amplifier Array Cabinets for operation of the isolation relays.

#### **4.7 {A1, A2, A3, A4, A5(5&6kW) & A6(6kW)} UHF Amplifier Trays, LDMOS (1301560 low band/1301561 mid band/1301562 high band; Appendix C)**

The LDMOS amplifier tray, with an RF input of approximately +3 dBm, provides a maximum power level of +57.8 dBm, 600W + sound. All the amplifier modules are broadband in nature and require no tuning.

#### **4.7.1 (A2) Variable Gain/Phase Board Enclosure (1301548; Appendix D)**

The variable gain/phase enclosure assembly provides EMI and RFI protection for the variable gain/phase board (1301549) that is mounted inside of the assembly.

The RF input to the assembly is at SMA jack J1 and the RF output is at SMA jack J2. There are two control inputs that connect to the assembly: the attenuator bias input and the phase control input. The attenuator bias input from the amplifier control board connects to FL4 and FL5 on the assembly and is wired to J5 on the board. The phase control input from the amplifier control board connects to FL2 and E1 on the assembly and is wired to J4 on the board. The input fault to the amplifier control board connects to FL3 on the assembly and is wired to J6-1 on the board. Ground E1 on the assembly connects to J3-4 on the board.

The +32 VDC needed to operate the board connects to FL1 on the assembly which is wired to J3-3 on the board.

### 4.7.2 (A2-A1) Variable Gain/Phase Board (1301549; Appendix D)

The variable gain/phase board provides the circuits that adjust the phase and the gain of the RF signal for the amplifier tray in which it is mounted.

The RF input signal at J1 (+3dBm) is split, with one output connected to a detector circuit consisting of C8, CR4, and U3A. This detected level is then applied to comparator U3D, which provides a high output when the input signal level drops below a threshold set by R16, R17, and CR5. This high is applied to the red Input Fault LED DS1, which lights to indicate an input fault has occurred. DS1 can be seen through the hole in the lid on the variable gain/phase assembly. The high is also connected to the gate of Q1, which biases it on and causes its drain to go low. The low is applied to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3. The low to CR3 decreases the current through it and increases its resistance, decreasing or completely shutting off the RF applied through it.

The other output of the RF input signal from J1 is connected through C1 to a voltage-controlled, pin-diode attenuator circuit consisting of diodes CR1, CR2, and CR3. The diodes are pin diodes in a pi-type configuration whose resistance varies inversely with the DC current flow through them.

As the AGC voltage, attenuator bias, applied to J5 increases, CR3 is forward biased even more. This increases the current flow through it by decreasing its resistance; the RF signal that flows through it increases in level. CR1 and CR2 have less current through them; this raises their resistance, causing the RF signal that is applied to them to decrease in level. The three diodes form a pi-type attenuator whose attenuation decreases with the increasing AGC voltage.

U4 provides amplification, approximately 8 dB, of the RF signal before it is connected to the phase-shifter circuit. The phase-shifter circuit consists of L1, C16, C17, CR7, and CR8. L1 is a 90°, 2-way splitter. The signal at pin 1 of L1 is split and applied to pins 2 and 4. The signal reflects off CR7 and CR8 and is passed to pin 3. The phase shift between pins 1 and 3 changes with the voltage applied across CR7 and CR8. This voltage is controlled by an external phase-adjust pot that connects to J4. The +32 VDC from the external switching power supply is used as the reference that is applied to the phase-control pot. The IC U2 provides approximately 10 dB of gain at the output of the phase-shifter circuit that connects to two class A amplifier stages, Q2 and Q3, with a total gain of approximately 20 dB.

The first amplifier stage, Q2, is biased at a collector current of approximately 100 mA. This current is set by R29, R30, VR1, and Q2. VR1 forces the voltage at the collector to stay at 8.9 VDC. This biases on Q2 and draws enough current through R29 and R30 to keep the collector voltage at 8.9 VDC. The amplified output connects to the second amplifier Q3. The bias circuit for Q3 works in a manner similar to the bias circuit for Q2. VR2 and VR3 maintain a collector voltage of 21 VDC, while R36 and R37 limit the collector current to 650 mA.

The output connects to J2 on the board. A sample of the output is detected by CR10 and connected to TP4. A DVM can be connected to TP4 to give a voltage indication of the RF output level.

The +32 VDC connects to the board at J3-3 and is split, with one half connected to the two, class A amplifier circuits. The other half of the +32 VDC input is filtered, isolated by L4 and C13, and connected to U1. U1 is a +12 VDC regulator IC that produces the +12

VDC needed to operate the ICs on the board.

The output of the variable gain/phase board (+19 dBm) at J2 connects through A16 a 6dB pad to J1 (+13 dBm) on the 1 Watt amplifier board assembly.

#### **4.7.3 (A3) 1-Watt Amplifier Board Assembly (1301546; Appendix D)**

The 1-watt UHF amplifier board assembly provides radio frequency interference (RFI) and electromagnetic interference (EMI) protection, as well as the heatsink, for the 1-watt UHF amplifier board, 32V (1301547) that is mounted inside the assembly. Depending on the frequency of the channel of operation, the assembly has approximately 9 dB of gain.

The RF input to the assembly connects to SMA jack J1. The amplified RF output of the assembly is at SMA jack J2. Typically, with an input signal of +13 dBm at J1 of the assembly, an output of +22 dBm can be expected at J2.

The +32-VDC bias voltage connects through FL1, a RF-bypassed, feed-through capacitor, to E1 on the amplifier board.

#### **4.7.4 (A3-A1) 1-Watt Amplifier Board, 32V (1301547; Appendix D)**

The 1-watt UHF amplifier board, 32V is mounted in the 1-watt UHF amplifier assembly (1301546) and provides approximately +9 dB of gain.

The UHF signal enters the board at J1, a SMA connector, and is applied through coupling capacitor C1 and a stripline circuit to Q1, a UTV040F UHF wideband-amplifier device. The base and collector voltages needed to operate the transistor are obtained from the +32 VDC line that connects to the board at E1 and is divided down to 26 volts by R4 and R5. The collector

voltage is fed through L4 and the base voltage is fed through R3, VR1, VR2 the divider network R1 and R2 and L2. The amplified UHF output of Q1 is coupled through a stripline circuit and C14 to J2, the output SMA jack of the board.

The board is powered by the +32 VDC that is produced by an external power supply in the tray. The +32 VDC enters through E1 and is fed across R4 and R5, which drops approximately 6 volts, to the collector (+26 VDC). The voltage is filtered by RF decoupling components L4, C11, C12, and C15 before it is connected to the collector. The base bias voltage is connected across R3, VR1, VR2, R1, and R2, which sets the base bias voltage at +.8 VDC and forward biases Q1. C6, L1, and L2 provide RF decoupling of the bias voltage before it is connected to the base.

The board has a self-bias protection circuit that uses Zener diodes VR1 and VR2. If the current draw of the device increases, the voltage drop across R4 and R5 increases; this decreases the voltage that is applied to VR1 and VR2. These two diodes drop a fixed voltage of 20 VDC across them. As a result, if the voltage drop across R4 and R5 increases, the voltage available to the base of Q1 decreases and the device will eventually be shut off.

#### **4.7.5 (A1) UHF Filter (1007-1101; Appendix D)**

The UHF filter is a tunable two-section cavity filter that is typically tuned for a bandwidth of 6 MHz and has a loss of -1 dB through the filter.

#### **4.7.6 (A4-A1) 40 Watt UHF Amplifier Assembly (1206693; Appendix D)**

The output of the UHF filter is connected to the input J1 of (A4-A1) the 40 Watt UHF amplifier assembly that is mounted on (A4) the amplifier enclosure. The (A4-A1) 40 watt UHF



amplifier assembly is made up of a (51-5378-308-00) module, which is a class AB module that is a highly linear broadband amplifier for the frequency range of 470 to 860 MHz. It can deliver an output power of 40 watts (CW) at an amplification of approximately 13 dB.

The amplification circuit consists of LDMOS transistors V804 and V805 connected in parallel and operating in class AB. The paralleling network is achieved with the aid of 3 dB couplers Z802 and Z803. A further 3 dB coupler Z801, in conjunction with capacitors C800 and C819, serves as a phase shifter. Phase alignment (for the complete amplifier), as well as quiescent current setting by means of potentiometers R807 and R808. It is factory implemented and should not be altered.

PIN diodes V810/V811 form a variable-damping circuit that is used to adjust the amplification of the 40-watt module. The adjustment is performed with the Gain potentiometer R838. A readjustment of the amplification may be required, e.g., after repair work, to ensure that all amplifiers in a translator deliver the same output power

#### **4.7.7 (A4-A2) Coupler Board Assembly (1227-1316; Appendix D)**

The UHF coupler assembly is mounted in the A4 amplifier enclosure and provides a forward power sample of the input drive level to the (A4-A3) LDMOS amplifier assembly. The drive-level sample from J3 is cabled to the amplifier control board where it connects to the input of the overdrive-protection circuit.

The RF input to the UHF coupler assembly, from the 40 Watt UHF amplifier module, connects to SMA jack J1. The RF is connected by a stripline

track to SMA output jack J2. A hybrid-coupler circuit picks off a forward sample that is connected to SMA type connector jack J3. R1 is a dissipation load for the reject port of the coupler.

#### **4.7.8 (A4-A3) LDMOS Amplifier Assembly (1301556; Appendix D)**

The output of the coupler assembly is fed to (A4-A3) the LDMOS amplifier assembly. The LDMOS amplifier assembly is made up of a (51-5379-309-00) module that operates class AB. The module is a broadband amplifier for the frequency range of 470 to 860 MHz. The amplification is approximately 13 dB.

The amplification circuit consists of the parallel connected push-pull amplifier blocks V1 and V2 operating in class AB. In order to match the transistor impedance to the characteristic impedance of the input and output sides, matching networks are placed ahead and behind the amplifier blocks. Transformers Z3 to Z6 serve to balance the input and output signals. The paralleling circuit is achieved with the aid of 3 dB couplers Z1 and Z2.

The working point setting is factory implemented by means of potentiometers R9, R11 and R12 and should not be altered.

The output of the (A4-A3) LDMOS amplifier module is connected to (A5-A1) the 4 way splitter board.

#### **4.7.9 (A5-A1) 4-Way Splitter Assembly (1301580; Appendix D)**

The 4-way splitter assembly is made up of three 2-way Wilkinson stripline splitters. One RF input to the board provides four, equal RF outputs.

The RF input to the board is connected to the input of the first 2-way splitter that contains R1. R1 is a 100  $\Omega$  balancing resistor in which any RF due

to mismatching in the first splitter will be dissipated. One of the two outputs from the splitter connects to another 2-way splitter that contains R2. R2 is a 100  $\Omega$  balancing resistor in which any RF due to mismatching in the splitter will be dissipated. The other output of the first splitter connects to the third 2-way splitter that contains R3. R3 is a 100  $\Omega$  balancing resistor in which any RF due to mismatching in the splitter will be dissipated. The two output splitters provide four, equal RF outputs, two each, which are connected to the inputs of the (A5-A2, A5-A3, A5-A4 & A5-A5) amplifier modules.

#### **4.7.10 (A5-A2 to A5-A5) LDMOS Amplifier Assemblies (1301556; Appendix D)**

The outputs of the splitter assembly are fed to the inputs of the four LDMOS amplifier assemblies. Each of the LDMOS amplifier assemblies is made up of a (51-5379-309-00) module that operates class AB. The module is a broadband amplifier for the frequency range of 470 to 860 MHz. The amplification is approximately 13 dB.

The amplification circuit consists of the parallel connected push-pull amplifier blocks V1 and V2 operating in class AB. In order to match the transistor impedance to the characteristic impedance of the input and output sides, matching networks are placed ahead and behind the amplifier blocks. Transformers Z3 to Z6 serve to balance the input and output signals. The paralleling circuit is achieved with the aid of 3 dB couplers Z1 and Z2.

The working point setting is factory implemented by means of potentiometers R9, R11 and R12 and should not be altered.

The output of the four LDMOS amplifier modules are connected to (A5-A6) the 4 way combiner assembly.

#### **4.7.11 (A5-A6) 4-Way Combiner Assembly (1301557 [CH. 14 to 26], 1301558 [CH. 27 to 43], and 1301559 [CH. 44 to 69]; Appendix D)**

The 4-way combiner assembly contains (A5-A6-A1) a 4-way combiner board, (A5-A6-A2) a circulator, (A5-A6-A3) a thermal switch and (A5-A6-A4) another thermal switch.

The 4-way combiner board is made up of three, 2-way Wilkinson stripline combiners. Two of the RF inputs to the board are soldered directly to the inputs for the 2-way combiner that contains R5. R5 is a balancing resistor in which any RF due to mismatching in the combiner will be dissipated. The other two RF inputs are soldered directly to the 2-way combiner that contains R6. R6 is a balancing resistor in which any RF due to mismatching in the combiner will be dissipated. The outputs of the two, input 2-way combiners connect to the third 2-way combiner that contains R7. R7 is a balancing resistor in which any RF due to mismatching in the combiner will be dissipated. The output of the third combiner is connected to the output of the 4-way combiner board that is cabled to an external circulator.

The circulator protects the tray from high-reflected power. A directional coupler is built into the RF output circuit on the 4-way combiner board. The coupler provides a forward power sample at J1 that is -40 dB down from the level of the RF output signal.

A reject power sample from the circulator is fed to the reject sample input jack J2 on the 4-way combiner board that is terminated into a 50- $\Omega$  load. A directional coupler is built into the reject sample circuit that provides at J3 a signal that is -40 dB down from the level of the reject power sample. Both the reject and forward samples are fed to (A6) the dual peak detector enclosure.

#### **4.7.12 (A6) Dual Peak Detector Enclosure (1227-1317; Appendix D)**

The dual peak detector enclosure provides EMI and RFI protection for the dual peak detector board, single supply (1227-1333), which is mounted inside the enclosure. The enclosure has two inputs: a forward power sample at SMA jack J1 and a reflected power sample at SMA jack J2. The module has two peak-detected sample outputs: a forward power sample at FL2 from J4-4 on the board and a reflected power sample at FL3 from J4-2 on the board. The module also has a forward power sample output at SMA jack J3 that connects to a BNC jack J5 located on the front panel.

The voltage, +32 VDC from the amplifier protection board, connects to FL1 on the assembly, which is wired to J4-7 on the board.

#### **4.7.13 (A6-A1) Dual Peak Detector Board, Single Supply (1227-1333; Appendix D)**

The function of the dual peak detector board is to detect forward and reflected samples of visual or aural RF signals and generate an output voltage proportional to the power levels of the sampled signals for metering purposes.

There are two identical signal paths on the board: one for forward power and one for reflected power. A sample of forward output power, from the 4 way combiner, enters the board at SMA jack J1. Resistors R1, R2, and R3 form an input impedance-matching network of 50 $\Omega$ . The forward power signal is detected by CR1, R4, R5, R7, R10, C1, and C2. The output is buffered by operational amplifiers U3B and U1C before it is connected to forward power output jack J4-4. U3 has a very high input impedance that makes the IC less sensitive to changes in the video level. A sample of the forward power is

tapped off by R6 and R8 and fed to J3, the forward sample output jack. Diode CR2 provides temperature compensation for diode CR1. An input signal level of approximately +17 dBm is enough to give a 1-VDC level at the output of U1C.

A reflected output power sample, from the 4 way combiner, enters the board at SMA jack J2. Resistors R18, R19, and R20 form an input impedance-matching network of 50 $\Omega$ . The reflected power signal is then detected by CR3, R21, R22, R24, C5, and C6 and the output is buffered by operational amplifiers U3A and U1B before it is connected to reflected power output jack J4-2. U3 has a very high input impedance that makes the IC less sensitive to changes in the video level. Diode CR4 provides temperature compensation for diode CR3. An input signal level of approximately +17 dBm is enough to give a 1-VDC level at the output of U1B.

The +12 VDC needed for the operation of U1 on the board is generated from the +32 VDC that enters at J4, pin 7. The +32 VDC is fed to U2, a voltage regulator IC that produces +12 VDC at its output, which is connected to U1.

#### **4.7.14 (A7) Amplifier Protection Board (1207117; Appendix D)**

The amplifier protection board distributes the biasing voltages to the transistor amplifier devices that are mounted on the amplifier boards in the UHF amplifier tray. It also protects the LDMOS devices on (A5-A2 to A5-A5) the output amplifier modules from overcurrent conditions using the board-mounted 15-amp fuses F3 to F6. F1 is board-mounted 10-amp fuse that protects the LDMOS devices on (A4-A1) the 40 Watt amplifier assembly and also the transistor mounted on A3-A1 the 1 Watt amplifier board from overcurrent conditions. F9 is a 3-amp board-mounted fuse that protects the +32 VDC that is applied to the amplifier

control board and is connected to the dual peak detector board. F7 is a 15-amp and F8 is a 3-amp spare fuse.

The +32 VDC from the switching power supply enters the board at TB1, with the plus (+) connections sent to pins 1 to 4 and the minus (-) connections sent to pins 5 and 6. The +32 VDC is connected across the .01-W/3-Ω voltage-dropping resistors R14 to R26

that are used to set up the idling currents for the transistor devices; the fuses F1 to F6 that protect the transistor devices during an overcurrent condition through the outputs of the board at TB2, TB3; and also to output jack J1. Table 4-1 indicates the fuse, the amplifier device it protects, and the idling current settings for the class AB amplifier devices.

Table 4-1. Fuses, Idling Currents, and Voltage Settings for the Class AB Amplifier Devices

SWITCH POSITION	AMPLIFIER MODULE	LD MOS DEVICE	BIAS ADJUST POT	IDLING CURRENT	VOLTAGE SETTING	FUSE
I1	A3-A1*	Q1* Transistor	NONE	.65A* operating current	11.5mV	F1 10A
	A4-A1	V804 & V805	R807 & R808	.5A		
I2	A4-A3	V1 & V2	R206	2A	20mV	F2 10A
I3	A5-A2	V1 & V2	R9, R11 & R12	2A	20mV	F3 15A
I4	A5-A3	V1 & V2	R9, R11 & R12	2A	20mV	F4 15A
I5	A5-A4	V1 & V2	R9, R11 & R12	2A	20mV	F5 15A
I6	A5-A5	V1 & V2	R9, R11 & R12	2A	20mV	F6 15A

\*The A3-A1 transistor Q1 operates class A at .65 amps of operating current.

The voltage drop across the selected resistor that uses switch S1 is read with a digital voltmeter (DVM) that is connected from E2 to E3 on the board. This voltage reading converts to the idling current, with no RF drive applied, or the operating current, with RF drive applied, of the Q1 transistor device operating Class A.

#### 4.7.15 (A8) Amplifier Control Board (1265-1414; Appendix D)

The amplifier control board provides LED fault and enable indications on the front panel of the tray and also performs the following functions: automatic gain control (AGC); overdrive cutback, when the drive level reaches the amount needed to attain 110% output power; and overtemperature, VSWR, and overdrive faults. The board also provides connections to the front panel meter for

monitoring the AGC, % Reflected Power, % Output Power, and the power supply voltage.

A -12-VDC enable is applied to the board at J4-1 from the transmitter control board in the UHF exciter tray. The enable causes the J-FET Q5 to be biased off, making the drain go high; the high is applied to Q4, which is biased on. The drain of Q4 goes low and lights the green Enable LED DS4 on the front panel. The high at the drain of Q5 is also applied through CR5 to J4, pin 7, which is a high enable, to the +32-VDC switching power supply, switching it on.

If there is an overtemperature fault, which is a low applied to J4, pin 3, the low connects through CR4 and overrides the high enable, switching off the switching power supply. As long as the fault is present, the switching power supply is off and the red Overtemperature LED DS3 on the front panel is lit.

#### 4.7.15.1 Phase Control

The phase control pot on the front of the tray connects to J8-1 (+32 VDC), J8-3 (phase I/P), and J8-4 (RTN) on the board. The phase-control output connects from J7 on the board to the input of the phase-control circuit on the variable gain/phase board (1301549).

#### 4.7.15.2 Automatic and Manual Gain Control Circuits

The amplifier control board contains the AGC function for the UHF amplifier tray in which it is mounted. An AGC reference-level input from the UHF exciter tray is applied to J3 pin 1, and is amplified by U3B. The output of U3B is connected to J5, which is wired to the front panel gain pot that sets the output power level of the tray when the AGC is in the Auto position. The voltage at the arm of the front panel gain pot is amplified by U2D and is compared to a

sample of the output power of the tray in U2A. The error voltage from U2A is sent through Auto/Manual switch S1 to J10, which connects to the pin-diode attenuator circuit on the variable gain/phase board. A sample of the AGC voltage level is connected to position 1 on the front panel meter switch. The tray can also be operated in manual gain by switching S1 to the Manual position and adjusting R16 for the desired output power level.

FETs Q1 and Q3 delay and slowly reapply the AGC voltage to the variable gain/phase board when the system is switched on or when the board is switched from Auto to Manual (or back) to prevent the overdriving of the tray.

#### 4.7.15.3 Overdrive Circuit

A sample of the output of the 40 Watt amplifier assembly, from the coupler board assembly connects to J11 on the amplifier control board. The sample is peak detected by CR7 and U3A and the output is connected to U3D.

If the input drive level increases above the overdrive threshold reference set by R71, which is the drive level needed to produce 110% output power, the output of U3D goes high and is split three ways. One of the highs is connected through R38 and CR3 to U3C, causing its output to go high and lighting the red Overdrive LED DS2 on the front panel. Another of the highs is connected through R74 and R75 to Q6, which is biased on, causing its output to go low. The low is connected through J10 to the variable gain/phase board that cuts back its output level.

The final high from U3D is connected through CR2 and R37 to U1D, which is biased on, causing its output to go high. The high is connected to U2A, whose output decreases and its output power is cut back. If this path is not present, the AGC, because the forward power decreases, will try to drive the variable gain/phase board harder

creating a positive feedback loop that could damage the amplifier tray.

#### 4.7.15.4 Metering Circuits

The +32 VDC that is connected to the board from the switching power supply is applied to jack J6, pin 1, of the board and connected through R63, R96, R66, R65, and R76 to the front panel meter for monitoring. R65 can be adjusted to calibrate the voltage reading to >30 VDC (+32 VDC) on the front panel meter. This calibration was completed at the factory and should not need to be adjusted at this time.

A forward power sample of the output of the tray is applied to jack J1-1 and J1-2 of the board from the dual peak detector board, single supply. The forward power sample is connected through R1 and R2 to U1A, a buffer amplifier. The output of U1A is split, with one part going to the AGC circuits, another sample connected to J1-5 for remote metering, and the final sample applied to the meter at position 3 on S2, the front panel meter switch. R2 can be adjusted to calibrate the % Forward Power indication on the front panel meter.

A sample of the reflected power output of the tray is applied to jack J2-1 and J2-2 of the board from the dual peak detector board, single supply. The reflected power sample is connected through R21 and R22 to U1B, a buffer amplifier. The output of U1B is split, with one part going to the VSWR threshold circuit, another sample connected to J2-5 for remote metering, and the final sample applied to the meter at position 2 on S2, the front panel meter switch. R22 can be adjusted to calibrate the % Reflected Power indication on the front panel meter. A sample of the AGC voltage level at R20 on the board is connected through a divider network consisting of R87, R88, R19, and R18 to the meter

at position 1 of S2, the Front Panel Meter switch.

#### 4.7.15.5 Operational Voltages

The voltage input to the board is +32 VDC from the switching power supply. The +32 VDC connects to the board at J6-1 and is wired to U4, which is a 3-terminal regulator IC that takes the +32 VDC input and produces the +12 VDC needed for the operation of the board.

The +12 VDC from U4 is connected through CR6 to U5, a +5-VDC regulator, that takes the +12 VDC input from U4, or the transmitter control board in the UHF exciter tray, through J6, pin 3, and produces a +5-VDC output that is applied to the rest of the board. This +12 VDC is connected to U5, a regulator IC, which produces a +5-VDC output that is applied to the Enable and Overtemperature LEDs that operate even when the +32 VDC input to the board from the switching power supply is removed.

### 4.8 (A13) (Optional) External Exhaust Kit (1061320)

Each of the 2-3kW Amplifier Array Assemblies may have an (Optional) (A13) External Exhaust Kit mounted on the roof of the cabinets. This kit provides greater cooling by venting the hot air outside the transmitter room using a blower fan. +12 VDC is applied to TB1-4A in the Exhaust enclosure when the UHF Exciter circuit breaker is switched On. An Enable is connected to TB1-3A when the UHF Exciter, Translator, is switched to Operate. The Enable energizes the Isolation Relay that applies the 120 VAC to the fan that will operate.

### 4.9 Translator Output Assemblies

The outputs of the (A2 & A3) 2-3 kW Amplifier Assemblies (+63.5-+65.2 dBm) connect through 1-5/8" hard-line and (A5 or A6) 1-5/8" to 3-1/8" Adapters to (A4) a Hybrid Combiner. The combiner combines the output from each Amplifier Assembly into a single output. The Reject Output of the Hybrid Combiner is connected through (A12) a 1-5/8" to 3-1/8" Adapter to (A7) a Directional Coupler (1016-1043) that provides a Reject Sample from J3 to the Metering Panel located in the UHF Exciter Assembly for monitoring purposes. The output of the Directional Coupler connects to (A8) a 2500 Watt Reject Load which dissipates any reject due to problems in one of the Amplifier Arrays. Mounted on the 2500 Watt Load is (A8-A1) a Thermal Switch that connects to the Overtemperature Fault circuit located on the Transmitter Control Board in the UHF Exciter Tray. If the temperature of the load reaches 155°F. the switch closes and causes an Overtemperature Fault to occur which shuts down the Translator.

The output of the Hybrid Combiner at J3 is fed to (A9) a Bandpass Filter, (A10) an Output Trap Filter Assembly,

then to (A11) the Output Coupler Assembly and finally to the Antenna for your System. The Bandpass Filter and Trap Filter are tuned to provide high out of band rejection of unwanted generated products. The filtered signal is connected to (A11) an Output Coupler Assembly which provides a Combined Forward and a Combined Reflected Power Sample to the Metering Panel located in the Single UHF Exciter Assembly. The Forward Sample is processed to provide peak detected Visual and Aural Power Output Samples to the front panel Meter of the Metering Panel. The Reflected Power Sample is also peak detected and wired to the front panel Meter. A Sample of the RF Output, for test purposes can be taken from J5 on the Coupler, but a 20 dB Attenuator must be connected to J6 for the Sample port to operate. An appropriate attenuator must be connected to J5 to protect any test equipment connected to it.

The RF output of the Coupler at J2 (+66 to + 67.7 dBm pk of sync) is the RF output of the translator and is connected to the Antenna for your System.