Chapter 4
Circuit Descriptions

4.1. (A1) Dual 250-Watt Driver/Amplifier Assembly (1094334; Appendix A)

4.1.1 (A1-A4) UHF Exciter Tray (1094019; Appendix A)

4.1.1.1 (A4) Aural IF Synthesizer Board, 4.5 MHz (1265-1303; Appendix B)

The aural IF synthesizer board amplifies each of the three possible audio inputs and the amplifier circuits that supply the single audio output. The balanced audio or the composite audio input is connected to the board while the subcarrier audio (SCA) input can be connected at the same time as either of the other two inputs. The board has the 4.5-MHz voltage-controlled oscillator (VCO) and the aural modulation circuitry that produces the modulated 4.5-MHz output. The board also contains a phase lock loop (PLL) circuit that maintains the precise 4.5-MHz separation between the aural (41.25 MHz) and the visual (45.75 MHz) IF frequencies.

Balanced Audio Input

The first of the three possible baseband inputs to the board is a 600Ω-balanced audio input (+10 dBm) that enters through jack J2, pins 1 (+), 2 (GND), and 3 (-), and is buffered by U1B and U1C. Diodes CR1 to CR4 protect the input stages of U1B and U1C if an excessive signal level is present on the input leads of jack J2. The outputs of U1B and U1C are applied to differential amplifier U1A; U1A eliminates the common mode signals (hum) on its input leads. A pre-emphasis of 75 ms is provided by R11, C11, and R10 and can be eliminated by removing jumper W5 on J5. The signal is then applied to amplifier U1D whose gain is controlled by jumper W3 on J11. Jumper W3 on jack J11 is positioned according to the input level of the audio signal (0 or +10 dBm). If the input level is approximately 0 dBm, the mini-jumper should be in the high gain position between pins 1 and 2 of jack J11. If the input level is approximately +10 dBm, the mini-jumper should be in low gain position between pins 2 and 3 of jack J11. The balanced audio is then connected to buffer amplifier U2A whose input level is determined by the setting of balanced audio gain pot R13. The output of the amplifier stage is wired to the summing point at U2D, pin 13.

Composite Audio Input

The second possible audio input to the board is the composite audio (stereo) input at BNC jacks J3 and J13. The two jacks are loop-through connected; as a result, the audio can be used in another application by connecting the unused jack and removing W4 from J12. Jumper W4 on jack J12 provides a 75Ω-input impedance when the jumper is between pins 1 and 2 of jack J12 and a high impedance when it is between pins 2 and 3. Diodes CR9 to CR12 protect the input stages of U6A and U6B if an excessive signal level is applied to the board. The outputs of U6A and U6B are applied to differential amplifier U2C, which eliminates common mode signals (hum) on its input leads. The composite input signal is then applied to amplifier U2B; the gain of this amplifier is controlled by composite audio gain pot R17. The composite audio signal is connected to the summing point at U2D, pin 13.

Subcarrier Audio Input

The third possible input to the board is the SCA input at BNC jack J4. The SCA input has an input impedance of 75Ω that can be eliminated by removing jumper W2 from pins 1 and 2 of J14. The SCA input is bandpass filtered by C66, C14, R22, C15, C67, and R23 and is fed to

buffer amplifier U3A. The amplified signal is then applied though SCA gain pot R24 to the summing point at pin 13 of U2D.

Audio Modulation of the VCO

The balanced audio, or the composite audio and/or the SCA-buffered audio signals, are fed to the common junction of resistors R14, R20, and R27 that connect to pin 13 of amplifier U2D. The output audio signal at pin 14 of U2D is typically .8 Vpk-pk at a ±25-kHz deviation for balanced or .8 Vpk-pk at ±75-kHz deviation for composite as measured at TP1. This signal is applied to VCO U10. A sample of the deviation level is amplified, detected by U7A and U7B, and connected to J10 on the board. This audio-deviation level is connected to the front panel meter through the transmitter control board.

The audio is connected to CR13 to CR16; these are varactor diodes that frequency modulate the audio signal onto the generated 4.5-MHz signal in U10. U10 is the 4.5-MHz VCO that generates the 4.5-MHz continuous wave (CW) signal. The output frequency of this signal is maintained and controlled by the correction voltage output of U5 PLL IC. The audio-modulated, 4.5-MHz signal is fed to amplifiers U11A and U11B. The output of U11B is connected to the 4.5-MHz output jacks at J7 and J8.

Phase Lock Loop (PLL) Circuit

A sample of the signal from the 4.5-MHz aural VCO at the output of U11A is applied to PLL IC U5 at the F_{in} connection. In U5, the signal is divided down to 50 kHz and is compared to a 50-kHz reference signal. The reference signal is a divided-down sample of the visual IF, 45.75-MHz signal that is applied to the oscillator-in connection on the PLL chip through jack J6 on the board. These two 50-kHz signals are compared in the IC and the fV, and fR is applied to the differential amplifier U3B. The output of U3B is fed back through CR17 to the 4.5-MHz VCO IC U10; this sets up a PLL circuit. The 4.5-MHz VCO will maintain the extremely accurate 4.5-MHz separation between the visual and aural IF signals; any change in frequency will be corrected by the AFC error voltage.

PLL chip U5 also contains an internal lock detector that indicates the status of the PLL circuit. When U5 is in a "locked" state, pin 28 goes high and causes the green LED DS1 to illuminate. If the 4.5-MHz VCO and the 45.75-MHz oscillator become "unlocked," out of the capture range of the PLL circuit, pin 28 of U5 will go to a logic low and cause the red LED DS2 to light. A mute output signal from Q3 (unlock mute) will be applied to jack J9. This mute is connected to the transmitter control board.

Voltage Requirements

The ±12 VDC needed for the operation of the board enters through jack J1. The +12 VDC is connected to J1-3 and filtered by L2, C3, and C4 before it is connected to the rest of the board. The -12 VDC is connected to J1-5 and filtered by L1, C1, and C2 before it is connected to the rest of the board. +12 VDC is connected to U8 and U9; these are 5-volt regulator ICs that provide the voltage to the U10 and U5 ICs.

4.1.1.2 (A5) Sync Tip Clamp/Modulator Board (1265-1302; Appendix B)

The sync tip clamp/modulator board can be divided into five circuits: the main video circuit, the sync tip clamp circuit, the visual modulator circuit, the aural IF mixer circuit, and the diplexer circuit.

The sync tip clamp/modulator board takes the baseband video or 4.5-MHz composite input that is connected to the video input jack (either J1 or J2, which are loop-through connected), and produces a modulated visual IF + aural IF output at output jack J20 on the board. The clamp portion of the board

maintains a constant peak of sync level over varying average picture levels (APL). The modulator portion of the board contains the circuitry that generates an amplitude-modulated vestigial sideband visual IF signal output that is made up of the baseband video input signal (1 Vpk-pk) modulated onto an externally generated 45.75-MHz IF carrier frequency. The visual IF signal and the aural IF signal are then combined in the diplexer circuit to produce the visual IF + aural IF output that is connected to J20, the IF output jack of the board.

Main Video Signal Path (Part 1 of 2)

The baseband video or the 4.5-MHz composite input connects to the board at J2. J2 is loop-through connected to J1 and terminated to 75 watts if jumper W4 is on jack J3. With jumper W4 removed, the input can be connected to another transmitter through J1; J1 is loop-through connected to J2.

Test point TP1 is provided to monitor the level of the input. The input is fed to the non-inverting and inverting inputs of U1A, a differential amplifier that minimizes any common-mode hum that may be present on the incoming signal. Diodes CR1 to CR4 form a voltage-limiter network in which, if the input voltages exceed the supply voltages for U1A, the diodes conduct, preventing damage to U1A. CR1 and CR3 conduct if the input voltage exceeds the negative supply and CR2 and CR4 conduct if the input voltage exceeds the positive supply voltage.

The video output of U1A is connected to J22 on the board. Normally, the video at J22 is jumpered to J27 on the board. If the 4.5-MHz composite input kit is purchased, the 4.5-MHz composite signal at J22 connects to the external composite 4.5-MHz filter board and the 4.5-MHz bandpass filter board. These two boards provide the video-only signal to J27 and the 4.5-MHz intercarrier signal to J28 from the 4.5-MHz composite input. The video through the video gain pot R12 (adjusted for 1 Vpk-pk at TP2) connects to amplifier U1B.

The output of U1B, if the delay equalizer board is present in the tray, connects the video from J6, pin 2, to the external delay equalizer board and back to the sync tip clamp/modulator board at J6, pin 4. If the delay equalizer is not present, the video connects through jumper W1 on J5, pins 1 and 2. The delay equalizer board plugs directly to J6 on the sync tip clamp/modulator board. The video from J6, pin 4, is then connected through jumper W1 on J5, pins 2 and 3, to the amplifier Q1. The output of Q1 connects to Q2; the base voltage of Q2 is set by the DC offset voltage output of the sync tip clamp circuit.

Sync Tip Clamp Circuit

The automatic sync tip clamp circuit is made up of U4A, Q7, U3B, and associated components. The circuit begins with a sample of the clamped video that is split off from the main video path at the emitter of Q3. The video sample is buffered by U3A and connected to U4A. The level at which the tip of sync is clamped, approximately -1.04 VDC as measured at TP2, is set by the voltage-divider network connected to U4A. If the video level changes, the sample applied to U4A changes. If jumper W7 on J4 is in the Clamp-On position, the voltage from the clamp circuit that is applied to the summing circuit at the base of Q2 will change; this will bring the sync tip level back to approximately -1.04 VDC. Q7 will be turned off and on according to the peak of sync voltage level that is applied to U4A. The capacitors C14, C51, C77, and C41 will charge or discharge to the new voltage level, which biases U3B more or less, through jumper W7 on J4 in the Auto Clamp-On position. U3 will increase or decrease its output, as needed, to bring the peak of sync back to the correct level as set by R152 and R12. This voltage level is applied through U3B

to Q2. In the Manual position, jumper W7 on J4 is in the Clamp-Off position, between pins 1 and 2, and adjustable resistor R41 provides the manual clamp bias adjustment for the video that connects to Q2.

Jumper W6 on jack J35 must be in the Normal position, between pins 2 and 3, for the clamp circuit to operate with a normal non-scrambled signal. If a scrambled signal is used, the tray is operated with jumper W6 in the Encoded position, connected between pins 1 and 2. The clamp circuit is set by adjusting depth of modulation pot R152 for the correct depth of modulation as measured at TP2.

Depending on the input video level, the waveform as measured at TP2 may not be 1 Vpk-pk. If W7 on J4 is moved to the Clamp-Off (Manual) position, between pins 1 and 2, the clamp level is adjusted by R41 and will not automatically be clamped to the set level. The output of buffer amplifier U3A drives the sync tip clamp circuit consisting of differential amplifier U4A, FET Q7, and buffer amplifier U3B. U4A is biased by R124, R125, R184, R152, and R126 so that the clamped voltage level at peak of sync is approximately -1.04 VDC as measured at TP2.

Main Video Signal Path (Part 2 of 2)

The clamped video from Q2 is connected to white clipper circuit Q3. Q3 is adjusted with R20 and set to prevent video transients from overmodulating the video carrier. The clamped video is connected to sync clipper circuit Q4 (adjusted by R24); Q4 limits the sync to -40 IRE units. The corrected video connects to emitter follower Q4 whose output is wired to unity gain amplifier U2A and provides a low-impedance, clamped video output at pin 1.

Visual Modulator Circuit

The clamped video signal from U2A is split. One part connects to a metering circuit, consisting of U20 and associated components, that produces a video output sample at J8-6 and connects through the transmitter control board to the front panel meter for monitoring. The other clamped video path from U2A is through a sync-stretch circuit that consists of Q5 and Q6. The sync-stretch circuit contains R48; R48 adjusts the sync stretch magnitude (amount) and R45 adjusts the cut-in. This sync-stretch adjustment should not be used to correct for output sync problems, but it can be used for video input sync problems. The output of the sync-stretch circuit connects to pin 5, the I input of mixer Z1.

The video signal is heterodyned in mixer Z1 with the visual IF CW signal (45.75 MHz). The visual IF CW signal enters the board at jack J15 and is connected to U9, where it is amplified and wired to pin 1, the L input of mixer Z1. The adjustable capacitor C78 and resistor R53 are set up to add a small amount of incidental carrier phase modulation (ICPM) correction to the output of the mixer stage to compensate for any non-linearities generated by the mixer.

The modulated 45.75-MHz RF output of mixer Z1 is amplified by U5 and is fed to double-sideband visual IF output jack J18. The level of this output jack is adjusted by R70. J18 is the visual IF loop-through output jack that is normally jumpered to J19 on the board. If the optional visual IF loop-through kit is purchased, the visual is connected out of the board to any external IF processor trays.

After any external processing, the modulated visual IF, double-sideband signal re-enters the board through J19. The visual IF from J19 is amplified by U10 and U11 and routed through the vestigial sideband filter network,

consisting of T1, FL1, and T2, and produces a vestigial sideband visual IF signal output. The filtered vestigial sideband visual IF is amplified by U7 and connected to a T-type attenuator. R62 can be adjusted to set the visual IF gain; this is the amount of visual IF signal that is coupled to amplifier IC U8. R63 and C30 are adjusted for the best VSBF frequency response. The amplified IF signal is fed to the input of the diplexer circuit that consists of R76, L13, and L12. A detected voltage sample of the visual IF is available at test point TP5.

41.25-MHz Aural IF Circuit

On this board, the 41.25-MHz aural IF is created by mixing the modulated 4.5-MHz aural intercarrier signal, produced by the aural IF synthesizer board or from the composite 4.5-MHz filter board, with the 45.75-MHz CW signal produced by the 45.75-MHz IF carrier oven oscillator board. The modulated 4.5-MHz aural intercarrier signal enters the board at J14 or J28 and is connected to IF relay K1. Jumper W3 on J7 determines whether the 4.5-MHz used by the board is internally generated or from an external source. With jumper W3 connected between pins 2 and 3, the 4.5 MHz from the aural IF synthesizer board or from the 4.5-MHz composite input is connected to mixer Z2. If an external 4.5-MHz signal is used, it enters the board at J12 and is fed through gain pot R88 to amplifier IC U13A. The amplified 4.5 MHz is then connected to J7 and, if jumper W3 is between pins 1 and 2, the 4.5-MHz signal from the external source is connected to the mixer. Mixer Z2 heterodynes the aural-modulated, 4.5-MHz signal with the 45.75-MHz CW signal to produce the modulated 41.25-MHz aural IF signal.

The output of the mixer is fed to a bandpass filter that is tuned to pass only the modulated 41.25-MHz aural IF signal that is fed to jack J16, the 41.25-MHz loop-through out jack of the board.

For normal operation, the 41.25-MHz signal is jumpered by a coaxial cable from J16 to J17 on the board. If the (optional) aural IF loop-through kit is purchased, the 41.25-MHz signal is connected to the rear of the tray, to which any processing trays can be connected, and then back to jack J17 on the board. The modulated 41.25-MHz aural IF signal from J17 is connected through amplifier ICs U15 and U16. The amplified output is connected to the attenuator-matching circuit that is adjusted by R85. R85 increases or decreases the level of the 41.25 MHz that sets the A/V ratio for the diplexer circuit. The diplexer circuit takes the modulated 45.75-MHz visual IF and the modulated aural IF and combines them to produce the 45.75-MHz + 41.25-MHz IF output. The combined 45.75-MHz + 41.25-MHz IF signal is amplified by U12 and connected to combined IF output jack J20 on the board. A sample of the combined IF output is provided at J21 on the board. If a NICAM input is used, it connects to J36 on the board. The level of the NICAM signal is set by R109 before it is fed to the diplexer circuit consisting of L28, L29, and R115. This circuit combines the NICAM signal with the 45.75-MHz visual IF + 41.25-MHz aural IF signal.

Operational Voltages

The +12 VDC needed to operate the transmitter control board enters the board at J23, pin 3, and is filtered by L26, L33, and C73 before it is fed to the rest of the board.

The -12 VDC needed to operate the board enters the board at J23, pin 5, and is filtered by L27 and C74 before being fed to the rest of the board.

4.1.1.3 (A6) Delay Equalizer Board (1227-1204; Appendix B)

The delay equalizer board provides a delay to the video signal, correction to

the frequency response, and amplification of the video signal.

The video signal enters the board at J1-2 and is connected to a pi-type, low-pass filter consisting of C16, L7, and C17. This filter eliminates any unwanted higher frequencies from entering the board. The output of the filter is connected to amplifier stage U1; the gain is controlled by R29. The video output of the amplifier stage is wired to the first of four delay-equalizing circuits that shape the video signal to the FCC specification for delay equalization or to the desired shape needed for the system. The board has been factory-adjusted to this FCC specification and should not be readjusted without the proper equipment.

Resistors R7, R12, R17, and R22 adjust the sharpness of the response curve while inductors L1, L2, L3, and L4 adjust the position of the curve. With a delay equalizer test generator signal or a sine x/x video test pattern input, the resistors and inductors can be adjusted, while monitoring a Tektronix VM700 test measurement set, until the desired FCC delay equalization curve or system curve is attained. The delay-equalized video signal is connected to J1-4, the video output of the board. A sample of the delayed video signal is connected to J2 on the board and can be used for testing purposes.

The ±12 VDC needed to operate the board enters the board at J1. The +12 VDC connects to J1-9, which is filtered by L5 and C11 before it is directed to the rest of the board. The -12 VDC connects to J1-6, which is filtered by L6 and C12 before it is directed to the rest of the board.

4.1.1.4 (A7) IF Carrier Oven Oscillator Board (1191-1404; Appendix B)

The IF carrier oven oscillator board generates the visual IF CW signal at 45.75 MHz for NTSC system "M" usage. The +12 VDC is applied through jack J10 to crystal oven HR1; HR1 is preset to operate at 60° C. The oven encloses crystal Y1 and stabilizes the crystal temperature. The crystal is the primary device that determines the operating frequency and is the most sensitive in terms of temperature stability.

Crystal Y1 is operating in an oscillator circuit consisting of transistor Q1 and its associated components. Feedback is provided through a capacitor-voltage divider, consisting of C5 and C6, that operates the crystal in a common-base amplifier configuration using Q1. The operating frequency of the oscillator can be adjusted by variable capacitor C17. The oscillator circuit around Q1 has a separately regulated voltage, 6.8 VDC, which is produced by a combination of dropping resistor R4 and zener diode VR1. The output of the oscillator at the collector of Q1 is capacitively coupled through C8 to the base of Q2. The small value of C8, 10 pF, keeps the oscillator from being loaded down by Q2.

Q2 is operated as a common-emitter amplifier stage whose bias is provided through R8 from the +12 VDC line. The output of Q2, at its collector, is split between two emitter-follower transistor stages, Q3 and Q4. The output of Q3 is taken from its emitter through R11 to establish an approximately 50-ohm source impedance through C11 to main output jack J3. This 45.75-MHz signal is at a power level of approximately +5 dBm. In most systems this output is either directed to a visual modulator board or to some splitting and amplifying arrangement that distributes the visual IF carrier for other needs. The second output from the collector of Q2 is fed to the base of emitter-follower transistor Q4.

Q4 drives two different output circuits. One output is directed through voltage divider R14 and R15 to jack J2 and is fed to a frequency counter. While monitoring J2, the oscillator can be set exactly on the operating frequency (45.75 MHz) by adjusting C17. The output at J2 is at a power level of approximately -2 dBm, which is sufficient to drive most frequency counters. The other output of Q4 connects to U1, a prescaler chip that divides the signal by 15. The output of U1 is applied to U2, a programmable divider IC. U2 is programmed through pins 11 to 20 to divide by 61. This results in a 50-kHz signal at pin 9 that is available as an output at J1. The output of 50 kHz is generally used in systems where the visual IF carrier oven VCXO is used as the reference for a PLL circuit. An example of this is a PLL circuit used on the aural IF synthesizer board, the aural VCO, or the precise frequency control tray. The 50-kHz CMOS output at jack J1 is not capable of providing enough drive level for a long coaxial cable length; as a result, when a long coaxial cable is needed, the output at jack J5 is utilized. The push-pull transistor stage Q5 and Q6, along with emitter resistor R18, provides a large-load output capability at J5.

The stages U1, U2, Q5, and Q6 are powered by +5.1 VDC. The +5.1 VDC is obtained by using the +12 VDC line voltage and voltage-dropping resistor R16 and zener diode VR2.

The +12 VDC power is applied to the board through jack J4, pin 3, and is isolated from RF signals that may occur in the +12 VDC line through the use of RF choke L2 and filter capacitor C10.

4.1.1.5 (A8) ALC Board, NTSC (1265-1305; Appendix B)

The automatic level control (ALC) board provides the ALC and amplitude linearity correction of the IF signal. The ALC adjusts the level of the IF signal through the board to control the output power of the transmitter.

The visual + aural IF input (0 dBm) signal from the modulator enters the board at modulator IF input jack J32. If the (optional) receiver tray is present, the visual + aural IF input (0 dBm) from the receiver tray connects to receiver IF input jack J1. The modulator IF input connects to relay K3 and the receiver IF input connects to relay K4. The two relays are controlled by the Modulator Select command that is connected to J30 on the board. Modulator select enable/disable jumper W11 on J29 controls whether the Modulator Select command at J30 controls the operation of the relays or not. With jumper W11 on J29, pins 1 and 2, the Modulator Select command at J30 controls the operation of the relays; with jumper W11 on J29, pins 2 and 3, the modulator is selected all of the time.

Modulator Selected

With the modulator selected, J11-10 and J11-28 on the rear of the UHF exciter tray are connected together; this makes J30 low and causes relays K3 and K4 to de-energize. When K4 is de-energized, it connects the receiver IF input at J1, if present, to 50 watts. When K3 is de-energized, it connects the modulator IF input at J32 to the rest of the board; Modulator Enable LED DS5 will be illuminated.

Receiver Selected

With the receiver selected, which is J11-10 and J11-28 on the rear of the UHF exciter tray (connected to J30 on the board) not connected together, relays K3 and K4 are energized. When K4 is energized, it connects the receiver IF input at J1, if present, to the rest of the board. When K3 is energized, it connects to the modulator IF input at J32 to 50 watts; Modulator Enable LED DS5 will be illuminated.

Main IF Signal Path (Part 1 of 3)

The selected visual + aural IF input (0 dBm) signal is split, with one half of the signal entering a bandpass filter that consists of L3, L4, C4, L5, and L6. This bandpass filter can be tuned with C4 and is substantially broader than the IF signal bandwidth. It is used to slightly steer the frequency response of the IF to make up for any small discrepancies in the frequency response in the stages that precede this point. The filter also serves the additional function of rejecting unwanted frequencies that may occur if the tray cover is off and the tray is in a high RF environment (if this is the case, the transmitter will have to be serviced with the tray cover off in spite of the presence of other RF signals). The filtered IF signal is fed through a pi-type matching pad consisting of R2, R3, and R4 to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3.

Input Level Detector Circuit

The other part of the split IF input is connected through L2 and C44 to U7; U7 is an IC amplifier that is the input to the input level detector circuit. The amplified IF is fed to T4; T4 is a step-up transformer that feeds diode detector CR14. The positive-going detected signal is then low-pass filtered by C49, L18, and C50. This allows only the video with positive sync to be applied through emitter follower Q1. The signal is then connected to detector CR15 to produce a peak-sync voltage that is applied to op-amp U9A. There is a test point at TP3 that provides a voltage reference check of the input level. The detector serves the dual function of providing a reference that determines the input IF signal level to the board and also serves as an input threshold detector.

The input threshold detector prevents the automatic level control from reducing the attenuation of the pin-diode attenuator to minimum (the maximum signal) if the IF input to the board is removed. The ALC, video loss cutback, and the threshold detector circuits will only operate when jumper W3 on jack J6 is in the Auto position, between pins 1 and 2. Without the threshold detector, and with the pin-diode attenuator at minimum, when the signal is restored it will overdrive the stages following this board.

As part of the threshold detector operation, the minimum IF input level at TP3 is fed through detector CR15 to op-amp IC U9A, pin 2. The reference voltage for the op-amp is determined by the voltage divider that consists of R50 and R51 (off the +12 VDC line). When the detected-input signal level at U9A, pin 2, falls below this reference threshold (approximately 10 dB below the normal input level), the output of U9A at pin 1 goes to the +12 VDC rail. This high is connected to the base of Q2. At this point, Q2 is forward biased and creates a current path from the -12 VDC line and through red LED DS1, the input level fault indicator, which becomes lit, resistor R54, and transistor Q2 to +12 VDC. The high from U9A also connects through diode CR16 to U9B, pin 5, whose output at pin 7 goes high. The high connects through range adjust pot R74 to J20, which connects to the front panel-mounted power adjust pot. This high connects to U10A, pin 2, and causes it to go low at output U10A, pin 1. The low is applied through jumper W3 on J6 to the pin-diode attenuator circuit that cuts back the IF level and, therefore, the output power level, to 0. When the input signal level increases above the threshold level, the output power will raise, as the input level increases, until normal output power is reached.

The video input level at TP3 is also fed to a sync-separator circuit, consisting of IC U8, CR17, Q3, and associated components, and then to a comparator circuit made up of U9C and U9D. The reference voltage for the comparators is determined by a voltage divider consisting of R129, R64, R65, R66, and R130 (off the -12 VDC line). When the

input signal level to the detector at TP3 falls below this reference threshold, which acts as a loss of sync detector circuit, the output of U9C and U9D goes towards the -12 VDC rail and is split, with one part biasing on transistor Q5. A current path is then established from the +12 VDC line through Q5, the resistors R69, R137, and the red LED DS3 (video loss indicator), which becomes lit. When Q5 is on, it applies a high to the gates of Q6 and Q7. This causes them to conduct and apply video loss fault pull-down outputs to J18, pins 5 and 2.

The other low output of U9C and U9D is connected through CR20 to jack J5. Jumper W2 on J5, in the Cutback Enable position (between pins 2 and 3), connects the low to the base of the forward-biased Q4. If jumper W2 is in the Disable position, between pins 1 and 2, the auto cutback will not operate. With Q4 biased on, a level determined by the setting of cutback level pot R71, which is set at the factory to cut back the output to approximately 25%, is applied to U9B, pin 5. The output of U9B at pin 7 goes low and is applied through the power adjust pot to U10A, pin 2, whose output goes low. This low is applied to the pin-diode attenuator to cut back the level of the output to approximately 25%.

Pin-Diode Attenuator Circuit

The input IF signal is fed to a pin-diode attenuator circuit that consists of CR1 to CR3. Each of the pin diodes contain a wide intrinsic region; this makes the diodes function as voltage-variable resistors at this intermediate frequency. The value of the resistance is controlled by the DC bias supplied to the diode. The pin diodes are configured in a pi-type attenuator configuration where CR1 is the first shunt element, CR3 is the series element, and CR2 is the second shunt element. The control voltage, which can be measured at TP1, originates either from the ALC circuit when jumper W3 on J6 is in the ALC Auto position, between pins 1 and 2, or from pot R87 when the jumper is in the Manual Gain position.

On the pin-diode attenuator circuit, a current path exists from J6 through R6 and then through the diodes of the pin attenuator. Changing the amount of current through the diodes by forward biasing them changes the IF output level of the board. There are two extremes of attenuation ranges for the pin-diode attenuators. In the minimum attenuation case, the voltage, measured at TP1, approaches the +12 VDC line. There is a current path created through R6, through series diode CR3, and finally through R9 to ground. This path forward biases CR3 and causes it to act as a relatively low-value resistor. In addition, the larger current flow increases the voltage drop across R9 that tends to turn off diodes CR1 and CR2 and causes them to act as high-value resistors. In this case, the shunt elements act as a high resistance and the series element acts as a low resistance to represent the minimum loss condition of the attenuator (maximum signal output). The other extreme case occurs as the voltage at TP1 is reduced and goes towards ground or even slightly negative. This tends to turn off (reverse bias) diode CR3, the series element, causing it to act as a high-value resistor. An existing fixed current path from the +12 VDC line, and through R5, CR1, CR2, and R9, biases series element CR3 off and shunt elements, diodes CR1 and CR2 on, causing them to act as relatively low-value resistors. This represents the maximum attenuation case of the pin attenuator (minimum signal output). By controlling the value of the voltage applied to the pin diodes, the IF signal level is maintained at the set level.

Main IF Signal Path (Part 2 of 3)

When the IF signal passes out of the pin-diode attenuator through C11, it is applied to modular amplifier U1. This device includes within it the biasing and impedance matching circuits that makes it operate as a wide-band IF amplifier.

The output of U1 is available, as a sample of the pre-correction IF for troubleshooting purposes and system setup, at jack J2. The IF signal is then connected to the linearity corrector portion of the board.

Linearity Corrector Circuits

The linearity corrector circuits use three stages of correction to correct for any amplitude non-linearities of the IF signal. Each stage has a variable threshold control adjustment, R34, R37, or R40, and a variable magnitude control adjustment, R13, R18, or R23. The threshold control determines the point at which the gain is changed and the magnitude control determines the amount of gain change that occurs once the breakpoint is reached. Two reference voltages are needed for the operation of the corrector circuits. Zener diode VR1, with R33 and R135, provides a +6.8 VDC reference and the diodes CR11 and CR12 provide a .9 VDC reference that temperature compensates for the two diodes in each corrector stage.

For the linearity correctors to operate, an IF signal is applied to transformer T1, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R14, R15, and R16 form an L-pad that lowers the level of the signal. The amount that the level is lowered is adjusted by adding more or less resistance, using R13, in parallel with the L-pad resistors. R13 is only in parallel when the signal reaches a level large enough to turn on the diodes CR4 and CR5. When the diodes turn on, current flows through R13, putting it in parallel with the L-pad.

When R13 is put in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch (the amount determined by the adjustment of R13). The signal is next applied to amplifier U2 to compensate for the loss through the L-pad. The breakpoint, or cut-in point, for the first corrector is set by controlling where CR4 and CR5 turn on. This is accomplished by adjusting cut-in resistor R34; R34 forms a voltage-divider network from +6.8 VDC to ground. The voltage at the wiper arm of R34 is buffered by unity-gain amplifier U5D. This reference voltage is then applied to R35, R36, and C39 through L12 to the CR4 diode. C39 keeps the reference from sagging during the vertical interval. The .9 VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U5B. The reference voltage is then connected to diode CR5 through choke L11. The two chokes L11 and L12 form a high impedance for RF that serves to isolate the op-amp ICs from the IF.

After the signal is amplified by U2, it is applied to the second corrector stage through T2. This corrector and the third corrector operate in the same fashion as the first. All three corrector stages are independent and do not interact with each other.

The correctors can be disabled by moving jumper W1 on J4 to the Disable position, between pins 2 and 3; this moves all of the breakpoints past the tip of sync so that they will have no affect. The IF signal exits the board at IF output jack J3 after passing through the three corrector stages and is normally connected to an external IF phase corrector board.

Main IF Signal Path (Part 3 of 3)

After the IF signal passes through the external IF phase corrector board, it returns to the ALC board at IF input jack J7. The IF then passes through a bandpass filter consisting of L20, C97, C62, L21, C63, L22, L23, C64, and C99. This bandpass filter is identical in both form and function to the one described in Section 4.3 of this chapter. In this case, the filter is intended to make up for small errors in frequency response that are incurred by the signal while being processed through the linearity and incidental phase correction circuits.

Following the bandpass filter, the signal is split using L24, L25, and R89. The signal passing through L24 is the main IF path through the board. A sample of the corrected IF signal is split off and connected to J10, the IF sample jack. The IF connects to jacks J27 and J28. These jacks control whether a 6-dB pad is included in the circuit by the positioning of jumpers W9 and W10. The 6-dB pad-in is when jumpers W9 and W10 are connected between pins 2 and 3 on J27 and J28. The 6-dB pad-out is when jumpers W9 and W10 are connected between pins 1 and 2 on J27 and J28. Normally, the pad is out. The IF signal is then applied to a two-stage, frequency-response corrector circuit that is adjusted as needed.

Variable resistors R103 and R106 adjust the depth and gain of the notches and variable caps C71 and C72 adjust the frequency position of the notches. The IF signal is amplified by U13 and U14 before it is connected to J12, the IF output jack of the board. R99 is an output level adjustment that is set to provide approximately 0 dBm of IF output at J12. A sample of the IF is fed to J11 to provide an IF sample point that can be monitored without breaking the signal path and gives an indication of the IF signal after the linearity and the frequency-response correction takes place.

ALC Circuit

The other path of the corrected IF signal is used in the ALC circuit. The IF is wired out of the splitter through L25 and connects to op-amp U12. The output of U12 is wired to jacks J8 and J9 on which jumpers W4 and W8 control the normal or encoded operation of the ALC circuitry. For normal operation, jumper W4 on J8 is between pins 1 and 2 and jumper W8 on J9 is between pins 1 and 2. The IF signal is applied to transformer T5; T5 doubles the voltage swing by means of a 1:4 impedance transformation before it is connected to the ALC detector circuit on the board and amplified by U10B.

For normal operation, jumper W7 on J26 is between pins 1 and 2 and jumper W5 on J21 is between pins 1 and 2. The detected ALC voltage is wired to U10A, pin 2, where it is summed with the front panel power control setting. The output power adjustment for the transmitter is achieved, if the (optional) remote power raise/lower kit (1227-1039) is purchased, by R75, a motor-driven pot controlled by switch S1 on the board, or screwdriver adjust pot R1 on the front panel of the UHF exciter tray. An external power raise/lower switch can be used by connecting it to jack J10, at J10-11 power raise, J10-13 power raise/lower return, and J10-12 power lower, on the rear of the UHF exciter tray. S1, or the remote switch, controls relays K1 and K2, which control motor M1 that moves variable resistor R75. If the (optional) remote power raise/lower kit is not purchased, the ALC voltage is controlled only by screwdriver adjust pot R1 on the front panel of the UHF exciter tray. The ALC voltage is set for .8 VDC at TP4 with a 0 dBm output at J12 of the board. A sample of the ALC at J19, pin 2, is wired to the transmitter control board where it is used on the front panel meter and in the AGC circuits.

This ALC voltage, and the DC level corresponding to the IF level after signal correction, are fed to U10A, pin 2, whose output at pin 1 connects to the ALC pin-diode attenuator circuit. If there is a loss of gain somewhere in an IF circuit, the output power of the transmitter will drop. The ALC circuit senses this drop at U10A and automatically lowers the loss of the pin-diode attenuator circuit to compensate by increasing the gain.

The ALC action starts with the ALC detector level that is monitored at TP4. The detector output at TP4 is nominally +.8 VDC and is applied through resistor R77 to a summing point at op-amp U10A, pin 2. The current available from

the ALC detector is offset, or complemented, by current taken away from the summing junction. In normal operation, U10A, pin 2, is at 0 VDC when the loop is satisfied. If the recovered or peak-detected IF signal at IF input jack J7 of this board should drop in level, which normally means that the output power is decreasing, the null condition would no longer occur at U10A, pin 2. When the level drops, the output of U10A, pin 1, will go more positive. If jumper W3 on J6 is in the Automatic position, it will cause the ALC pin-diode attenuators CR1, CR2, and CR3 to have less attenuation and increase the IF level; this will act to compensate for the decrease in level. If the ALC cannot increase the input level enough to satisfy the ALC loop, due to there not being enough range, an ALC fault will occur. The fault is generated because U10D, pin 12, increases above the trip point set by R84 and R83 until it conducts. This makes U10D, pin 14, high and causes the red ALC Fault LED DS2 to light.

Scrambled Operation with Encoding

For encoded, scrambled operation, jumper W4 on J8 must be connected between pins 2 and 3, jumper W8 on J9 must be between pins 3 and 2, jumper W7 on J26 must be between pins 2 and 3, and jumper W5 on J21 must be between pins 2 and 3. The IF is connected through W4 on J8 to the sync regeneration circuits.

If this board is operated with scrambling, using suppressed sync, the ALC circuit operates differently than described above because there is no peak of sync present on the IF input. A timing pulse from the scrambling encoder connects to the board at J24. This timing pulse is converted to sync pulses by U17A and U17B, which control the operation of Q8. The sync amplitude is controlled by R149 and is then applied to U15A, where it is added to the detected IF signal to produce a peak of sync level. The output of U15A is peak detected by CR26 and fed to U15B. If necessary, intercarrier notch L39 can be placed in the circuit by placing W6 on J22. The intercarrier notch is adjusted to filter any aural and 4.5-MHz intercarrier frequencies. The peak of sync signal is fed through R162, the ALC calibration control, to amplifier U15C. The amplified peak of sync output is connected through J21, pins 2 and 3, to U10A, where it is used as the reference for the ALC circuit and the AGC reference to the transmitter control board. Voltage TP4 should be the same in either the normal or the encoded video mode. Monitor J9, pins 3 and 4, with a spectrum analyzer, check that the board is in the AGC mode, and tune C103 to notch-out the aural IF carrier.

Fault Command

The ALC board also has circuitry for an external mute fault input at J19, pin 6. This is a Mute command and, in most systems, it is involved in the protection of the circuits of high-gain output amplifier devices. The Mute command is intended to protect the amplifier devices against VSWR faults. In this case, the action should occur faster than just pulling the ALC reference down. Two different mechanisms are employed: one is a very fast-acting circuit to increase the attenuation of the pin-diode attenuator, CR3, CR1, and CR2, and the second is the reference voltage being pulled away from the ALC amplifier device. An external Mute is a pull-down applied to J19, pin 6, to provide a current path from the +12 VDC line through R78 and R139, the LED DS4 (Mute indicator), and the LED section of opto-isolator U11.

These actions turn on the transistor section of U11 that applies -12 VDC through CR21 to U10A, pin 3, and pulls down the reference voltage. This is a fairly slow action that is kept at this pace by the low-pass filter function of R81 and C61. When the transistor section of U11 is on, -12 VDC is also connected through CR22 to the pin-diode attenuator circuit. This establishes a very fast muting

action, by reverse biasing CR3, in the event of an external VSWR fault.

±12 VDC Needed to Operate the Board

The ±12 VDC connects to the board at J14. The +12 VDC connects to J14-3 and is filtered by L30, L41, and C80 before it is applied to the rest of the board. The -12 VDC connects to J14-5 and is filtered by L31 and C81 before it is applied to the rest of the board.

The +12 VDC also connects to U16, a 5-VDC regulator IC, that produces the +5 VDC needed to operate timing IC U17.

4.1.1.6 (A9) IF Phase Corrector Board (1227-1250; Appendix B)

The IF phase corrector board has adjustments that pre-correct for any IF phase modulation distortion that may occur in output amplifier devices such as Klystron power tubes and solid-state amplifiers. Two separate, adjustable IF paths are on the board: a quadrature IF path and an in-phase IF path. The quadrature IF is 90° out of phase and much larger in amplitude than the in-phase IF. When they are combined in Z1, it provides the required adjustable phase correction to the IF signal.

The IF input signal enters at J1 and is AC coupled to U1. U1 amplifies the IF before it is connected to Z1, a splitter that creates two equal IF outputs: IF output 1 is connected to J2 and IF output 2 is connected to J3. The IF output 1 at J2 is jumpered through coaxial cable W4 to jack J6, the quadrature input, on the board. The IF output 2 at J3 is jumpered through coaxial cable W5 to jack J7, the in-phase input, on the board.

Phase Corrector Circuit

The phase corrector circuit corrects for any amplitude nonlinearities of the IF signal. It is designed to work at IF and has three stages of correction. Each stage has a variable threshold and magnitude control. The threshold control determines the point at which the gain is changed and the magnitude control determines the gain change once the breakpoint is reached. The second stage has a jumper that determines the direction of correction, so that the gain can increased either above or below the threshold, and either black or white stretch can be achieved.

In the phase corrector circuit, the IF signal from J6 is applied to transformer T1; T1 doubles the voltage swing using a 1:4 impedance transformation. Resistors R8, R61, R9, and R48 form an L-pad that attenuates the signal. This attenuation is adjusted by adding R7, a variable resistor, in parallel with the L-pad. R7 is only in parallel when the signal reaches a level large enough to bias on CR1 and CR2 and allow current to flow through R7. When R7 is put in parallel with the L-pad, the attenuation through the L-pad is lowered, causing black stretch.

Two reference voltages are utilized in the corrector stages and both are derived from the +12 VDC line. Zener diode VR1, with R46 as a dropping resistor, provides +6.8 VDC from the +12 VDC line. Diodes CR11 and CR12 provide a .9 VDC reference to temperature compensate the corrector circuits from the effects of the two diodes in each corrector stage.

The threshold for the first corrector stage is set by controlling where CR1 and CR2 turn on. This is accomplished by adjusting R3 to form a voltage divider from +6.8 VDC to ground. The voltage at the wiper of R3 is buffered by U9C, a unity-gain amplifier, and applied to CR1. The .9 VDC reference is connected to U9D, a unity-gain amplifier, whose output is wired to CR2. These two references are connected to diodes CR1 and CR2 through chokes L2 and L3. The two chokes form a high impedance for RF to isolate the op-amps from the RF. The adjusted signal is next applied to amplifier U2 to compensate for the loss through the L-pad. U2 is powered

through L4 and R10 from the +12 VDC line. After the signal is amplified by U2, it is applied to the second corrector stage through T2 and then to a third corrector stage through T3. The other two corrector stages operate in the same manner as the first; they are independent and do not interact with each other.

When jumper W1 on J8 is connected from center to ground, R15 is put in series with ground. In this configuration, black stretch (white compression) is applied to the IF signal by controlling the attenuation through the path. When W1 is connected from the center pin to the end that connects to T2, R15 is put in parallel with the L-pad. In this configuration, black compression (white stretch) is applied to the IF signal by controlling the attenuation through the path.

The phase correctors can be bypassed by moving jumper W2 on J9 to the Disable position. This action will move all of the threshold points past sync tip so that they will have no effect. R68 can be adjusted and set for the correction range that is needed. TP2 is a test point that gives the operator a place to measure the level of the quadrature IF signal that is connected to pin 6 on combiner Z2.

Amplitude Corrector Circuit

The amplitude corrector circuit uses one stage of correction to correct for any amplitude nonlinearities of the IF signal. The stage has a variable threshold control, R31, and a variable magnitude control, R35. The threshold control determines the point at which the gain is changed and the magnitude control determines the amount of gain change once the breakpoint is reached.

Two reference voltages are needed for the operation of the corrector circuit. Zener diode VR1 with R46 provides +6.8 VDC and the diodes CR11 and CR12 provide a .9 VDC reference voltage to temperature compensate for the two diodes in the corrector stage. In the amplitude corrector circuit, the IF signal from J7 is applied to transformer T4 to double the voltage swing by means of a 1:4 impedance transformation. Resistors R36, R55, R56, and R37 form an L-pad that lowers the level of the signal. The amount that the level is lowered is adjusted by adding more, or less, resistance, using R35 in parallel with the L-pad resistors. R35 is only in parallel when the signal reaches a level large enough to turn on diodes CR8 and CR9. When the diodes turn on, current flows through R35 and puts it in parallel with the L-pad. When R35 is in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch (the amount of stretch determined by the adjustment of R35).

The signal is next applied to amplifier U5 to compensate for the loss in level through the L-pad. The breakpoint, or cut-in point, for the corrector stage is set by controlling where CR8 and CR9 turn on. This is achieved by adjusting cut-in resistor R31 to form a voltage divider from +6.8 VDC to ground. The voltage at the wiper arm of R31 is buffered by unity-gain amplifier U8B. This voltage is then applied to R34 through L11 to the CR9 diode. The .9 VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U8A. C36 keeps the reference from sagging during the vertical interval. The reference voltage is then connected to diode CR8 through choke L12. The two chokes L11 and L12 form a high impedance for RF to isolate the op-amp ICs from the IF.

After the signal is amplified by U5, it is applied to a second stage through T5. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R39, R57, R58, and R40 form an L-pad that lowers the level of the signal. The signal is applied to amplifier U6 to compensate for the loss in level through the L-pad. After the signal is amplified by U6, it is applied to a

third stage through T6. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R42, R59, R60, and R43 form an L-pad to lower the level of the signal. The signal is applied to amplifier U7 to compensate for the loss in level through the L-pad. TP1 is a test point that gives the operator a place to measure the level of the in-phase IF signal that is connected to mixer stage Z2. The amplitude corrector can be disabled by moving jumper W3 on J10 to the Disable position; this will move the breakpoint past sync tip and will have no effect on the signal.

Output Circuit

The phase-corrected signal from pin 1 on combiner Z2 exits the board at IF output jack J4 after passing through a matching network consisting of six resistors.

4.1.1.7 (A11) UHF Upconverter Board (1265-1310; Appendix B)

The UHF upconverter board provides upconversion for the transmitter by mixing the IF and local oscillator (LO) signals in mixer Z1 to produce the desired RF frequency output. The RF output is connected through J3 to an external filter and applied back to the board at J4 where the gain is set by R10. The RF is amplified and connected to the RF output jack of the board at J5.

The IF signal (0 dBm) enters the board at J1, an SMA connector, and is applied through a filter circuit (L10 and C25 to C28) to a matching pad that consists of R1, R2, and R3. The matching pad presents a relatively good source impedance to the I input of mixer Z1, which is made up of pins 3 and 4. The LO signal (+13 dBm) from the x8 multiplier connects to the board at jack J2, an SMA connector, through a UHF channel filter and is connected directly to pin 8, the L input of the mixer. The frequency of the LO is the sum of the IF frequency above the desired visual carrier. For instance, in system M, the IF visual frequency is at 45.75 MHz and the relative location of the aural would be 4.5 MHz lower (41.25 MHz). By choosing the local oscillator to be 45.75 MHz above the visual carrier, a conversion in frequency occurs with the selection of the difference product. The difference product, which is the local oscillator minus the IF, will be at the chosen visual carrier frequency output. There will also be other signals present at RF output connector J3 at a lower level. These are the sum conversion product, the LO, and the IF frequencies. Usually, the output product that is selected by the tuning of the external filter is the difference product (LO minus the 45.75-MHz IF). The difference product has the sidebands flipped so that the visual carrier is lower in frequency than the aural carrier.

If a bad reactive load is connected to the mixer, the LO signal fed through it can be increased because the mixer no longer serves as a double-balanced mixer. The mixer suppresses signals that may leak from one input port to any of the other ports. This activity is enhanced by having inputs and outputs of the mixer at a 50Ω impedance.

The reactive filter, which is externally connected to J3 of the board, does not appear as a good 50Ω-load at all frequencies. The pad, in the output line of the board, consists of R5, R4, R6, and R7. It buffers the bad effects of the reactive filter load and makes it appear as a 50Ω impedance. The RF signal is amplified by U1, a modular amplifier that contains biasing and impedance matching networks that make U1 act as a wideband RF amplifier device. This amplifier, in a 50Ω system, has approximately 12 dB of gain. U1 is powered from the +12 VDC line through RF decoupling components R27, R28, C30, R8, and L1. The inductor L1 is a broadband RF choke, resonance free through the UHF band. The amplified RF connects to SMA RF output jack J3 which is cabled to the external filter.

The RF input signal from the external filter re-enters the board at J4 (-11 to -14 dBm) and is capacitively coupled to the pin-diode attenuator circuit that consists of CR1, CR2, and CR5. The pin-diode attenuator acts as a voltage-variable attenuator in which each pin diode functions as a voltage-variable resistor and depends on the DC bias supplied to the diode for the resistance value. The pin diodes, because of a large, intrinsic region, cannot rectify signals at this RF frequency; they act as a linear voltage-variable resistor. The pin diodes are configured in a shunt configuration where CR1 is the first shunt element, CR2 is the second shunt element, and CR5 is the series element. In most cases, the manual gain AGC, W1 on J10 between pins 1 and 2, is used. The control voltage from manual gain pot R10 sets up a current path through R11 and the diodes in the pin attenuator.

The level-controlled RF signal from the pin-diode attenuator circuit is amplified by wideband-hybrid amplifier IC U2; U2 is configured in the same way as U1. The RF signal is buffered by Q1 and applied to the push-pull class A amplifier circuit that consists of Q2 and Q3. At the input to the transistors, the RF is converted to a balanced dual feed by a balun L4 made from a short length of UT-141 coaxial cable. Capacitors C12 and C13 provide DC blocking for the input signal to the amplifier devices. The RF outputs at the collectors of the transistors are applied through C19 and C20, which provide DC blocking for the output signals. The RF signals connect to L7, which consists of UT-141 coaxial cable, that combines the RF back to a single RF output at a 50Ω impedance to L8; L8 provides a sample of the RF.

The main path through L10 is to J5, the RF output jack of the board (+10 to +20 dBm). The sample of the RF connects to a splitter that provides a sample output (0 dBm) at J6 of the board. The other output of the splitter connects to a peak-detector circuit, consisting of CR3 and U3, that provides a DC level at J7 representing the RF output of the UHF exciter to the front panel meter. R29 sets up the calibration of the front panel meter for 100% in the UHF exciter position when the output power of the exciter is at +17 dBm peak visual.

The upconverter board is powered by ±12 VDC that is produced by an external power supply. +12 VDC enters through J8, pin 3, and is filtered and isolated by RF choke L9 and shunt capacitors C24 and C33. This circuit isolates the RF signals of the board from those of other devices connected to the same +12 VDC line external to the upconverter board. The +12 VDC is then applied to the rest of the board.

4.1.1.8 (A15) x8 Multiplier Board (1227-1002; Appendix B)

The x8 multiplier board multiplies the frequency of an RF input signal by a factor of eight. The board is made up of three identical x2 broadband frequency doublers.

The input signal (+5 dBm) at the fundamental frequency enters through SMA jack J1 and is fed through a 3-dB matching pad, consisting of R1, R2, and R3, to amplifier IC U1. The output of the amplifier stage is directed through a bandpass filter, consisting of L2 and C4, which is tuned to the fundamental frequency (87 to 114 MHz). The voltage measured at TP1 is typically +.6 VDC.

The first doubler stage consists of Z1 with bandpass filter L3 and C6 tuned to the second harmonic (174 to 228 MHz). The harmonic is amplified by U2 and again bandpass filtered at the second harmonic frequency by C10 and L5 (174 to 228 MHz). The voltage measured at TP2 is typically +1.2 VDC.

The next doubler stage consists of Z2 with bandpass filter C12 and L6 tuned to the fourth harmonic of the fundamental frequency (348 to 456 MHz). The fourth

harmonic is then amplified by U3 and fed through another bandpass filter tuned to the fourth harmonic consisting of L11 and C18 (348 to 456 MHz). The voltage measured at TP3 is typically +2.0 VDC.

The final doubler stage consists of Z3 with bandpass filter C20 and L12 tuned to the eighth harmonic of the fundamental frequency (696 to 912 MHz). The signal is amplified by U4, U5, and U6 to a typical value of from +2 to +4 VDC as measured at test point TP4. The amplified eighth harmonic is then fed to the SMA output jack of the board at J2.

The typical LO signal output level is +15 dBm nominal. The detected sample of the output of the x8 multiplier board at TP4 is also fed to the base of Q1, which forward biases it and lights the green LED DS1 on the board to indicate that the LO signal is present.

The +12 VDC for the board enters through jack J3-3 and is filtered by L7 and C16 before being distributed to the circuits on the board.

4.1.1.9 (A17) Transmitter Control Board (1293-1221; Appendix B)

The transmitter control board (1293-1221) provides the system control functions and the operational LED indications that can be viewed on the front panel of the transmitter. The main control functions of the board are for Operate/Standby and Auto/Manual selection. When the transmitter is switched to Operate, the board supplies the enables to any external amplifier trays. The board also performs the automatic switching of the transmitter to Standby upon the loss of the video input when the transmitter is in Auto. The board contains a VSWR cutback circuit which, if the VSWR of the transmitter increases above 12.5%, will cut back the output level of the transmitter, as needed, to maintain a maximum of 12.5% VSWR. An interlock (low) must be present at J8-24 for the transmitter to be switched to Operate and, when the interlock is present, the green Interlock LED DS5 will be lit.

Operate/Standby Switch S1

K1 is a magnetic latching relay that controls the switching of the transmitter from Operate to Standby. When the Operate/Standby switch S1 on the front panel of the tray is moved to Operate, one coil of relay K1 energizes and causes the contacts to close and apply a low to U4B-9. If the transmitter interlock is present, and there is no overtemperature fault, lows will also be applied to U4B-10, U4B-11, and U4B-12. With all the inputs to U4B low, the output at U4B-13 will also be low. The low biases off Q1, which turns off the amber Standby LED DS1 on the front panel, and applies a high to Q2. This action turns on and lights the green Operate LED DS2 on the front panel.

When Q2 is biased on, it connects a low to Q12 and biases it off. This allows the ALC to be applied to J1, which connects to any external amplifier trays. The low from U4B-13 is also applied to Q4 and Q24, which are biased off, and removes the disables from J1-4 and J18-1. The low from U4B-13 connects to Q10, which is biased on, and to Q6, Q7, Q8, and Q9, which are also biased on. In addition, it applies -12 VDC enables at J8-2, J8-3, J8-4, and J8-5 that connect to any external amplifier trays. The high applied to Q2 is connected to Q5 and Q26, which are biased on, and applies a low enable to J1-3, which can connect to a remote operate indicator. The transmitter is now in the Operate mode.

When the Operate/Standby switch S1 is moved to Standby, the other coil of relay K1 energizes; this causes the contacts to open and a high, +12 VDC, to be applied to U4B-9. The high at the input causes the output at U4B-13 to go high. The high biases on Q1 and applies a low to the amber Standby LED DS1 on the front panel. The indicator turns on and applies

a low to Q2, which turns off and extinguishes the green Operate LED DS2. In addition, Q12 is biased on; it connects to U2C, whose output goes low and pulls the ALC voltages at J1 low, lowering the gain of the external amplifier trays. The high from U4B-13 is also applied to Q4 and Q24, which are biased on and apply disables at J1-4 and J18-1. The high from U4B-13 connects to Q10, which is biased off. Q10 Off removes the high from Q6, Q7, Q8, and Q9, which are biased off, and removes the -12 VDC enables at J8-2, J8-3, J8-4, and J8-5 that connect to the external amplifier trays. The low applied to Q2 is connected to Q5 and Q26, which are biased off, and removes the remote enable at J1-3. The transmitter is now in the Standby mode.

Automatic/Manual Switch S2

K2 is a magnetic latching relay that switches the operation of the transmitter to Automatic or Manual by using Auto/Manual switch S2 on the front panel of the tray.

When the S2 switch is set to the Auto position, the operation of the transmitter is controlled by the fault circuits and will stay in Operate even if Operate/Standby switch S1 is moved to Standby. With the S2 switch in Auto, a low is applied to one coil in the relay; this energizes and closes the contacts. The closed contacts apply a low to the green Automatic LED DS3, causing it to illuminate. The low from the relay connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. Q21 and Q23 are biased off, which causes their outputs to go high. The high from Q21 connects to the amber Manual LED DS4 on the front panel, biasing it off, and to Q22, biasing it on. The drain of Q22 goes low and is applied to J8-7, which will enable any remote auto indicator connected to it. The low to Q23 biases it off and removes the enable to any remote manual indicator connected to J8-6.

When the S2 switch is set to the Manual position, the operation of the transmitter is no longer controlled by the fault circuits and is controlled by Operate/Standby switch S1. With the S2 switch in Manual, a low is applied to the other coil in the relay to energize and open the contacts. The open contacts remove the low from the green Automatic LED DS3 on the front panel and cause it to not light. The high connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. Q21 and Q23 are biased on, which causes their outputs to go low. The low from Q21 connects to the amber Manual LED DS4 on the front panel, biasing it on, and to Q22, biasing it off. The drain of Q22 goes high and the high is applied to J8-7, which will disable any remote auto indicator connected to it. Q23 is biased on, which applies a low enable to any remote manual indicator connected to J8-6.

Automatic Turning On and Off of the Transmitter

The transmitter control board also allows the transmitter to be turned on and off by the presence of video when the transmitter is in Auto. When a video fault occurs due to the loss of video, J7-5 goes low. The low is applied through W1 on J10 to Q16, which is biased off, and to the red Video Loss Fault LED DS9 on the front panel, which will light. The drain of Q16 goes high and connects to U5B, pin 5, causing the output at pin 4 to go low. The low connects to Q18, which is biased off, and causes the drain of Q18 to go high. The high connects to U3D, pin 12, whose output at pin 14 goes high. The high connects to U5C, pins 8 and 9, which causes its output at pin 10 to go low, and to U5A, pin 1, which causes its output at pin 3 to go low. With switch S2 set to Automatic, a low is applied to U5A, pin 2, and to U5D, pin 13. When U5A, pin 1, is high and U5A, pin 2, is low, it causes the output at pin 3 to go low. When U5D, pin 12, is low and U5D, pin 13, is low, it causes the output to go high. When U5A, pin 3, is low, it biases off Q20, which removes any pulldown to the Operate switch. A high at U5D, pin

11, biases on Q19, which applies a low enable to the Standby switch; this places the transmitter in the Standby mode.

When the video is returned, J7-5 goes high. The high is applied to Q16, which is biased on, and to the red Video Fault LED DS9, which is extinguished. The output of Q16 goes low and connects to U5B, pin 5. If there is no receiver ALC fault, U5B, pin 6, is also low, which causes the output at pin 4 to go high. The high connects to Q18, which is biased on, causing the drain of Q18 to go low. The low connects to U3D, pin 12, whose output at pin 14 goes low. The low connects to U5C, pins 8 and 9, which causes its output at pin 10 to go high, and to U5A, pin 1. With Auto/Manual switch S2 in Auto, a low is applied to U5A, pin 2, and to U5D, pin 13. With U5A, pins 1 and 2, low, its output at pin 3 goes high. With pin 12 of U5D high, the output of U5D at pin 11 goes low. With U5A, pin 3, high, it biases on Q20, which applies a pulldown enable to the Operate switch. A low at U5D, pin 11, biases off Q19, which removes any pulldown to the Standby switch. The transmitter is switched to Operate.

Faults

There are four possible faults that may occur in the transmitter and are applied to the transmitter control board: video loss fault, VSWR cutback fault, overtemperature fault, and ALC fault. There will be no faults to the board during normal transmitter operations. The receiver ALC fault circuit will only function if a receiver tray is part of the system.

Video Loss Fault. If a video loss occurs, the transmitter, while in Auto, will go to Standby after a few seconds, until the video is returned; at that point it will immediately revert to Operate. A video loss fault applies a low from the ALC board to the video fault input at J7-5 on the board.

With jumper W1 in place on J10, the video fault is connected to the red Video Loss Fault LED DS9 and to Q16. The LED DS9 on the front panel will light and Q16 will be biased off, causing its drain to go high. The high is wired to U5B, pin 5, whose output at U5B, pin 4, goes low. The low is wired to Q18, which is biased off; this causes the drain to go high. The high is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go high. The high connects to U5A, pin 1, and, if the transmitter is in Auto, pin 2 of U5A is low. With pin 1 high and pin 2 low, the output of U5A goes low and reverse biases Q20, shutting it off. The high at U5C, pins 8 and 9, causes its output at pin 10 to go low. This low is connected to U5D, pin 12, and, if the transmitter is in Auto, pin 13 of U5D is also low. The lows on pins 12 and 13 cause the output to go high, which forward biases Q19. The drain of Q19 goes low and connects the coil in relay K1, causing it to switch to Standby.

When the video returns, the video loss fault is removed from the video fault input at J7-5. With jumper W1 in place on J10, the base of Q16 goes high. The red Video Loss Fault LED DS9 on the front panel will go out. Q16 is biased on, causing its drain to go low. The low is wired to U5B, pin 5, and U5B, pin 6, will be low if no ALC fault occurs. The two lows at the inputs make the output at U5B, pin 4, go high. The high is wired to Q18, which is biased on and causes the drain to go low. The low is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go low. The low connects to U5A, pin 1, and, if the transmitter is in Auto, pin 2 of U5A is also low. With both inputs low, the output of U5A at pin 3 goes high. The high forward biases Q20 and causes its drain to go low. The low connects to the operate coil on relay K1 that switches the transmitter to Operate. The low at U5C, pins 8 and 9, causes the output at pin 10 to go high. This high is connected to U5D, pin 12, and, if the transmitter is in Auto, pin 13 of U5D is low. The high on pin 12 causes the

output of U5D to go low and reverse bias Q19. The drain of Q19 goes high and removes the low from the standby coil in relay K1.

VSWR Cutback Fault. The reflected power sample of the RF output of the diacrode transmitter is connected to J2, pin 9, of the board. The sample connects to op-amp U1B, pin 5, which buffers the signal. The remote reflected sample connects to U2B, pin 5. If the reflected sample level increases above the level set by R22, the VSWR cutback pot, the output of U2B at pin 7 goes high. The high is connected to Q11 through CR11, which is biased on and makes U2C, pin 10, low; this causes U2C, pin 8, to go low. This low is split and fed out of the tray at J1-6, J1-7, J1-8, and J1-9. These are ALC outputs to the amplifier trays that cut back the output power of those trays. The low from U2C, pin 8, is also fed through the coaxial jumper W2 on J13 and J14 to R73. R73 is a bias adjust pot that sets the level of the pin attenuator bias that is available as an output at J16.

The high at U2B, pin 7, is fed to the base of Q14 and Q13, which are forward biased, and produces a low at the drains. The low connects to the front panel amber VSWR Cutback LED DS7, causing it to light and indicate that the tray is in cutback, and to output jack J8-37 for the connection to a remote VSWR cutback indicator.

Metering

The front panel meter connects to J3-1 (-) and J3-2 (+) on the board; these are the outputs of Front Panel Meter switch S3. The front panel meter has six metering positions that are controlled by S3: Audio, Video, % Aural Power, % Visual Power, % Exciter, and ALC.

The video sample connects to the board at J5-4 and is connected through R20, the video calibration pot, to position 6 of switch S3. The audio sample enters the board at J5-6 and is connected through R19, the audio calibration pot, to position 7 of switch S3. The visual sample connects to the board at J2-5 and is connected through buffer amplifier U1D and 100Ω resistor R86 to position 4 of switch S3. The aural sample connects to the board at J2-7 and is connected through buffer amplifier U1C and 100W resistor R85 to position 5 of switch S3. The exciter sample connects to the board at J2-3 and is connected through buffer amplifier U1A and 100Ω resistor R87 to position 2 of switch S3. The ALC sample connects to the board at J6-1 and is connected through buffer amplifier U2C, and R15, the ALC calibration pot, which adjusts the output of U2A, pin 1, through a 100Ω resistor R18 to position 1 on switch S3.

Typical readings on the meter are:

- Video = 1 Vpk-pk at white
- % Visual Power = 60% to 90%
- % Aural Power = 60% to 90%
- % Exciter = The level on the meter needed to attain 100% output power from the transmitter

Refer to the test specifications sheet for the transmitter for the actual reading:

- ALC = .8 VDC
- Audio = ±25 kHz with a balanced audio input or ±75 kHz with a composite audio input

Samples of the exciter at J1-10, the visual at J8-26, the aural at J8-27, and the reflected at J1-5 are provided for remote metering.

U6 is a temperature-sensor IC that gives the operator the ability to measure the temperature inside the tray by measuring the voltage at TP1. The sensor is set up for +10 mV equals 1° F (for example, 750 mV equals 75° F.)

Operational Voltages

The +12 VDC needed for the operation of the transmitter control board enters the board at jack J4, pin 3. C28, L1, and L3 are for the filtering and isolation of the +12 VDC before it is split and applied to the rest of the board. The -12 VDC needed for the operation of the board enters the board at jack J4, pin 5. C29 and L2 are for the filtering and isolation of the -12 VDC before it is split and applied to the rest of the board.

When the +12 VDC is connected to the board, it is split; four of the +12 VDC outputs are fed out of the board at J8-16, J8-17, J8-18, and J8-19 through diode CR7, CR8, CR9, or CR10 and resistor R50, R51, R52, or R53 to any external amplifier trays for use in their logic circuits. The resistors are for current limiting and the diodes are to prevent voltage feedback from the external amplifier trays.

4.1.1.10 (A19) Visual/Aural Metering Board (1265-1309; Appendix B)

The visual/aural metering board provides detected outputs of the visual and aural output samples that are used for monitoring on the front panel meter. The board also provides adjustments for the calibration of the readings on the meter. These readings are attained from samples of the forward power and reflected power outputs of the tray.

A forward power sample, visual + aural, is applied to SMA jack J1 on the board. The input signal is split, with one path connected to forward power sample SMA jack J2 for monitoring purposes. The other path is connected through C1 to CR2, R4, R5, R6, C4, and CR1, which make up a detector circuit. The detected visual + aural signal is amplified by U6B and its output is split. One amplified output of U6B connects to the aural level circuit and the other output connects to the visual level circuit.

Aural Level Circuit

One of the detected visual + aural level outputs of U6B connects through C6 to the intercarrier filter circuit that consists of R13, R14, L1, C7, and C8; C8 and L1, the intercarrier filter, can be adjusted for a maximum aural reading. The filter notches out the video + aural and only leaves the 4.5-MHz difference frequency between the visual and aural, which is a good representation of the aural level. The 4.5-MHz signal is fed to buffer amplifier U6A. The output of U6A is detected by diode detector CR3 and U1A and then fed through aural calibration control R20 to amplifier U2D. The amplified output of U2D is split, with the main output connected through R21 to J6, pin 1, which supplies the aural level output to the front panel meter for monitoring. The other output of U2D is connected to aural null adjust R51 and offset null adjust R48, which are adjusted to set up the visual power calibration.

Visual Level Circuit

The other detected visual + aural level output from U6B is connected to U1C and, if there is no scrambling, connects directly to intercarrier notch L3, which is adjusted to filter out the aural and the 4.5-MHz intercarrier frequencies, leaving only a visual-with-sync output. The visual-with-sync output is fed to a peak-detector circuit consisting of CR5 and U2A. The signal is then fed through visual calibration control R28, which is adjusted for a 100% visual reading with no aural, to amplifier U2B. The amplified visual peak of sync output is connected to comparator U2C. The other input to U2C is the level set by aural null adjust R51, which is adjusted for 100% visual power after the aural is added and the peak power is adjusted back to the reference level. Inputs to U2C also come from offset null adjust R48, which is adjusted for 0% visual power with the transmitter in Standby. The adjusted output is amplified by U3D and connected to the other input of U2C. The output of U2C

connects to J6, pins 2 and 3, which supply the peak of sync visual level output to the front panel meter for monitoring.

If this board is operated with scrambling, using suppressed sync, the visual level circuit operates differently than described above because there is no peak of sync present on the forward sample input. For the board to operate properly, a timing pulse from the scrambling encoder must connect to the board at J4. This timing pulse is converted to sync pulses by U4A and U4B, which control the operation of Q2. Intercarrier notch L2 is tuned to remove any visual + aural signal that may remain.

The sync amplitude is controlled by gate amplitude adjust R25 and then applied to the minus input of U1C. At this point, it is inserted into the visual + aural signal that is connected to the plus input of U1C, producing a peak of sync in the signal. The output of U1C is connected to intercarrier notch L3, which is adjusted to filter out the aural and the 4.5-MHz intercarrier frequencies. The visual-with-sync output is fed to a peak-detector circuit, consisting of CR5 and U2A, and then fed through visual calibration control R28 to amplifier U2B. The amplified visual peak of sync output is connected to J6, pins 2 and 3, that supply the peak of sync visual level output to the front panel meter for monitoring. R32 moves the pulse to where the sync should be and R25 sets the visual metering calibration with no sync present.

Voltages for Circuit Operation

The ±12 VDC is applied to the board at J5. The +12 VDC is connected to J5, pin 3, and is isolated and filtered by L4 and C34 before it is connected to the rest of the board. The +12 VDC also connects to U5, a 5-VDC regulator that provides the voltage needed to operate U4. The -12 VDC is applied to J5, pin 1, and is isolated and filtered by L5 and C35 before it is connected to the rest of the board.

4.1.1.11 (A4-A14) Channel Oscillator Assembly, Dual Oven (1145-1202; Appendix B)

The channel oscillator assembly contains the channel oscillator board (1145-1201) that generates a stable frequency-reference signal of approximately 100 MHz. The channel oscillator assembly is an enclosure that provides temperature stability for the crystal oscillator. An SMA output at jack J1 and an RF sample at BNC connector jack J2 are also part of the assembly.

Adjustments can be made through access holes in the top cover of the assembly. These adjustments are set at the factory and should not be tampered with unless it is absolutely necessary and the proper, calibrated equipment is available. R1 is the temperature adjustment; C11 is the course-frequency adjustment; and C6, C18, L2, and L4 are adjusted for the maximum output of the frequency as measured at jack J1. C9 is the fine-frequency adjustment.

The +12 VDC for the assembly enters through FL1 and the circuit-ground connection is made at E1.

4.1.2 (A1-A9) 3-Watt UHF Amplifier Tray (1068203; Appendix A)

The modulated RF carrier signal (+8 dBm) from the 3-watt UHF amplifier enters through J1 and is filtered by (A1) a bandpass filter (1007-1101). The signal (+7 dBm) is then fed to (A2) the AGC board (1007-1201). The AGC board controls the overall gain of the amplifier tray by comparing a sample of the output signal from the dual peak detector board through the AGC control board. An AGC reference voltage is generated either externally or internally depending on the system operation and the position of the jumper on J7. The jumper should be

between J7-1 and J7-2 for the operation of the diacrode (external reference).

The (A25) AGC control board (1137-1201) compares a sample of the output of the diacrode with a sample of the 3-watt tray. The front panel gain control R2 adjusts the overall gain of the tray. The output voltage of the comparator drives a pin attenuator circuit that corrects for drift by maintaining a constant output even though temperatures, therefore gain, of the amplifier devices in A3, A5, or A7 may vary.

The AGC board also contains circuitry that monitors the AGC level and provides for an AGC override detector. If the final 3-watt amplifier stage is overdriven, the AGC override LED DS2 on the front panel will light to indicate a cutback of the AGC that cuts the gain of the tray. The AGC override detector is also used as the system Mute (Standby, VSWR fault, and other faults). There is also a ramp control signal input to the AGC control board. When the 3-watt amplifier is externally enabled, the drive output of the amplifier ramps up over a time frame of several seconds. The output of the pin attenuator is amplified to approximately 0 dBm and fed to output jack J2 of the board.

The RF from the AGC board is fed to (A27) the UHF phase shifter board (1142-1315). The phase-corrected signal is then amplified by (A3) the UHF amplifier/regulator board (1007-1204) that has a nominal gain of +17 dB. Next, the signal (+17 dBm typical) is amplified by (A5) the 3-watt amplifier board #1 (1007-1211) that has a nominal gain of +9 dB. The operating drive current, no RF input, for the 3-watt amplifier board #1 is set by the (A6) opto-bias board (1002-1109). The signal (+26 dBm typical) is amplified further by (A7) the 3-watt amplifier board #2 (1007-1211) that also has a nominal gain of +9 dB. The operating drive current for the 3-watt amplifier board #2 is set by (A8) the opto-bias board (1002-1109).

The output (typically +35 dBm) of the second 3-watt amplifier board is fed to (A29) the overdrive protection board (1142-1626). The signal enters the board at J4 and is connected directly out of the board at J5. A sample of the RF signal is coupled off the input and fed to a detector circuit to set up the AGC override level. If the RF output level of the transmitter increases to 120%, the override circuit will cut back the output of the 3-watt tray to prevent damage to the amplifier devices.

The output of the overdrive protection board is fed to (A9) a dual coupler assembly (1007-1208) that supplies a forward and reverse power sample to (A10) the dual peak detector board (1137-1510). The dual peak detector drives the front panel meter for a % Reflected Power reading and also provides a forward power sample (inner loop AGC) to (A25) the AGC control board (1137-1201). The AGC control board provides an output to the front panel meter for the % Forward Power reading and also provides an output to the AGC board that is used as the AGC sample of the output. If an outer loop AGC is used from an external amplifier tray, it is fed to the AGC control board through J5 on the rear of the tray. The output from the dual coupler is directed to the RF output jack J2 on the rear of the tray (+35 dBm).

Two power supplies are used in the tray. The (A16) +24V power supply board (1007-1207) supplies power for the amplifier devices through the opto-bias boards in the 3-watt amplifiers and the UHF amplifier/regulator board. The (A22) general purpose ±12V power supply board (1062-1013) supplies voltage to the rest of the boards in the tray.

AC is applied to the tray through J4 on the rear panel and is connected to terminal block TB2. MOVs VR1 and VR2 are provided as protection from transients or surges on the AC input line. When CB1, the 2.5-amp circuit breaker,

is switched on, AC is applied to fans A19 and A20 and also to (A21) the step-down transformer for the ±12V power supply. The stepped-down AC is applied to (A22) the ±12V power supply board (1062-1013) that supplies the regulated ±12V to the rest of the boards in the tray. LEDs DS1 for +12V and DS2 for -12V on the board will light to indicate that the power supply is operational.

Even with the circuit breaker switched on, the +24V power supply will not turn on until the power supply enable control line J3-8 is taken Low (Enabled). This occurs by jumpering J3-8 to J3-7 or by an external pull-down, which is normally provided by the power supply Enable from the metering control panel.

With the pull-down present, (A11) the power supply control board (1007-1202) will energize (A12) the isolation relay board (1002-1108). The 120 VAC is then applied to (A13) the toroid and then to (A14) the full-wave bridge rectifier network that supplies approximately 40 volts to the +24 volt power supply board.

4.1.3 (A1-A6 and A1-A7) 250-Watt Amplifier Trays (1044027, low band / 1044028, mid band / 1044029, high band; Appendix A)

The 250-watt amplifier tray, with an RF input of +24 dBm peak visual and 10% aural, provides an average output power level of +54 dBm peak visual. The amplifier utilizes feedforward circuitry to minimize distortion and increase output.

RF Path

The input to the 250-watt amplifier tray at the BNC-type connector jack J1 is the diplexed on-channel visual + aural signal. The input RF is connected to J1 of (A1-A1) the single stage amplifier assembly that is mounted on (A1) the amplifier enclosure. The (A1-A1) single stage amplifier assembly, which contains a generic single stage amplifier board (1265-1415) and the required frequency determining kit, is a class A amplifier supplying 11.5 dBm of gain at J2. The output is fed to (A1-A3) the stripline coupler board. The coupler board supplies a –10 dB sample for (A3) the phase/gain adjust module at J3. This sample is the linear portion of the feedforward signal. The output of the stripline coupler board is fed to (A1-A5) the single stage amplifier assembly, class AB. The single stage amplifier assembly is mounted on (A1) the amplifier enclosure and consists of a generic single stage amplifier board, class AB (1286-1234), with the required frequency determining kit. This assembly has a minimum gain of approximately 8 dB.

The (A1-A5) amplifier assembly output is connected to (A19-A6) the splitter board. The splitter board is a two-way wilkinson splitter that feeds the inputs of (A19-A7, A19-A8) the dual output power amplifier assemblies, class AB. The dual output power amplifier assembly, class AB, is made using a generic dual stage amplifier board, class AB (1265-1404), and the appropriate frequency dependent kit. The two assemblies, A1-A7 and A1-A8, are identical. The dual output power amplifier board uses two PTB20101 transistors in parallel-biased class AB to amplify the signal. The bias adjust R106 sets the operating current for Q101 and the bias adjust R206 sets the operating current for Q201. The output of both assemblies is soldered directly to (A19-A9) the 2-way combiner board. The total gain through the splitter board, amplifier assemblies, and combiner board is a minimum of 8 dB.

The (A19-A9) 2-way combiner board is frequency dependent for low-band, middle-band, and high-band. The combiner board also has a –40 dB coupler for forward and reflected power samples. The forward port J1 is cabled to (A5) the dual stripline coupler board as a sample for the feedforward circuit. This is the non-linear portion of the feedforward signal and is used as a reference to

cancel any remaining non-linear distortion at the output.

The reflected port is terminated into a 1-watt, 50Ω load (A19-A10). After the linear and non-linear samples have been matched for gain and delay, and their phases have been adjusted to a 180° difference, they are summed together in the (A5) dual stripline coupler board. From A5-J2, the mixed signals are fed to the (A20) correction phase/gain enclosure at J1. The (A20-A1) error amplifier phase/gain module is used to match the gain of the correction path to the output level of the main amplifier at the RF O/P part of the (A7) 7 dB coupler. The phase/gain module also sets the 180° phase imbalance between the two signals. These two signals, when combined, cancel most of the distortion in the signal at the RF output connection.

The A20 module is terminated in the reject load (A19-A18) in (A19) the amplifier enclosure. The RF output from the coupler output is fed to the input, J1, of (A8) the UHF coupler assembly. J3, the forward sample on the coupler board, is fed to J1 of (A17) the peak detector board. The reflected sample at J4 is terminated into a 1-watt, 50Ω load. The output, J2, is fed to (A10) the circulator, which protects the tray from high-reflected power, to the output of the tray at the N-type connector J2. Any reflected power at J2 is fed to (A2-A6) the reject load/coupler board mounted inside (A1) the correction amplifier enclosure.

Feedforward Correction

The feedforward correction circuits consist of phase and gain adjustment boards, delay lines, and amplifiers to sample and cancel any non-linear distortions introduced into the RF signal by the power amplifiers. A sample of the linear RF signal sampled at (A19-A3) the stripline coupler board is adjusted and amplified to be of equal gain and 180° out of phase with the non-linear sample from the (A19-A9) 2-way combiner board. The linear sample is phase adjusted through the use of C1 and C2 on the (A3) phase/gain adjust module. The gain for the module is set by R22 on the (A16) amplifier control board. This linear signal is combined with the non-linear signal at (A5) the stripline coupler board. The combined out-of-phase non-linear and in-phase linear signal is amplified and then combined with the RF signal at the 7-dB coupler board. The gain of the combined signals is controlled on the amplifier control board by R20 and they are phase adjusted by R29 on the same board. The resulting output signal will have a 20 dB cancellation of non-linearities.

Amplifier Control Board

The (A16) amplifier control board provides output level sample inputs to (A12) the meter and protection of the tray against overheating. The (A8) UHF coupler board and (A2-A6) the reject load/coupler board supply forward and a reflected output power samples to (A17) the dual peak detector board. The dual peak detector board takes the forward and reflected output power samples and provides peak-detected DC levels to the amplifier control board and uses them for metering purposes. If an overtemperature fault occurs because one of (A1-A13 or A1-A14) the thermal switches closes due to the overheating of the output amplifier heatsink, the +5 VDC inhibit to the switching power supply will be applied. This will disable the switching power supply. The amplifier control board can be adjusted to set the calibration of the front panel meter for the Forward, Reflected, and Power Supply positions.

Operation of the Tray

The 220 VAC input needed to operate the tray connects to the tray at J3 and is supplied to the rest of the tray when the circuit breaker, CB1, is switched on. The input AC connects to (A11) a +26.5V/1500W switching power supply

that provides the +26.5 VDC to the two cooling fans and, when the tray is enabled, through the amplifier protection board to the rest of the boards in the tray. The enable is applied to the tray at J4-5 on the back of the tray. The output of the switching power supply is connected to (A15) the amplifier protection board and also to (A13 and A14), which are two fans used for cooling the tray. The amplifier protection board provides 7-amp fused protection of the +26.5 VDC outputs before they are distributed to the amplifier boards in the tray. An external +12 VDC needed for the operation of the status LEDs mounted on the amplifier control board is applied to the 250-watt amplifier tray, from the UHF upconverter tray, through J4-7. The +12 VDC is present when the main AC is applied to the UHF upconverter tray.

4.2 (A2) 10-kW Diacrode Amplifier (1299-1100; Appendix A)

4.2.1 10-kW Bias Power Supply Board, 230 VAC Input (1181- 1001; Appendix B)

The 10-kW bias power supply board provides the -80 VDC bias voltage, typical setting, that is applied to the control grid of the TH610 diacrode power tube. This tube is mounted in the TH18610 cavity assembly in the 10-kW amplifier assembly.

The bias power supply board (1181-1001) has a 230 VAC input that is applied to J1, pins 1 and 4, when the bias circuit breaker on the AC distribution panel is switched on, and (A3) the isolation relay board, part of the control and bias power supply assembly, is energized. The 230 VAC is applied to a full-wave bridge network, consisting of CR1 to CR4, that rectifies the AC. The output of the full-wave bridge is filtered by capacitors C1 and C10 and applied to a shunt-regulator circuit that utilizes comparator IC U1. The shunt path includes VR1, Q1, and U1; R10 is the bias adjust that applies the control voltage to the (+) terminal of U1 at pin 12. The negative output of IC U1 at pin 14 connects to the base of Q1 and sets up the biasing for the transistor. The amount of forward bias that is applied to the transistor determines the voltage drop across the transistor. The value of the output voltage, as measured across zener diode VR1 and Q1, is variable because of the changes in the voltage drop across the transistor. The bias voltage output of the board at J3, pins 1 and 2, is typically adjusted for -80 VDC. The supply voltages to U1 are set at approximately -1 VDC and -11 VDC by zener diode VR2. The main current path to the tube is from ground through R4, R17, and R8 to the tube.

VR8 and VR9 are protection zener diodes that prevent the output voltage from rising above -174 VDC. CR7 prevents the output from going positive and causing damage to the tube. VR10 and VR11 are zener diodes that prevent voltage spikes above +10 VDC or below -10 VDC from entering the voltage metering circuit if an arc occurs in the tube or in the tube cavity assembly. VR6 and VR7 are zener diodes that prevent voltage spikes above +10 VDC or below -10 VDC from entering the current metering circuit if an arc occurs in the tube or in the tube cavity assembly. If R4 opens, VR4 and VR5 prevent the voltage on the floating ground from rising above a maximum of 4 VDC.

The 5 kΩ bias adjust pot R10 is located on the front, left-hand side of the amplifier assembly, behind the swing-out panel. It connects to J2, pins 3, 5, and 6, on the board. The bias adjust pot sets the bias (grid) voltage output level, -80 VDC (typical). The bias is adjusted for 1.5 amps of static plate current.

Note: The static plate current is adjusted without RF drive applied to the tube.

R14 calibrates the bias voltage reading at J2, pin 8, that is applied to the voltage

meter on the metering control panel. R6 calibrates the bias (control grid) current meter reading at J2, pins 1 and 2, that is applied to the current meter on the metering control panel. These meter calibration adjustments were set at the factory for typical operation and should not need adjustments at this time.

4.2.2 Control and Bias Power Supply Assembly

The control and bias power supply assembly (1181-1402) contains two separate power supplies. The control power supply consists of input terminal block TB2; T1, a step-down transformer; (A1) a ±12 VDC power supply board (1092-1206; Appendix B); and TB4, an output terminal block. The bias power supply consists of input terminal block TB1; (A3) an isolation relay board (1002-1108; Appendix B); (A2) a bias power supply board (1181-1001; Appendix B); and TB3, an output terminal block.

The 220 VAC main input to the control power supply connects to terminal block TB2, terminals 1A and 3A (neutral) and 4A (ground). VR3 and VR4 are metal-oxide varistors (MOVs) that protect the supply from any AC input line surges. The 220 VAC is applied to the terminal block as long as the control circuit breaker on the AC control assembly is switched on. The AC is directed to T1, a step-down transformer, that produces two AC outputs. The two stepped-down AC outputs connect to J1, pins 1 and 4, and J1, pins 7 and 8, on (A1) the ±12 VDC power supply board. The AC inputs are full-wave bridge rectified and filtered and regulated to produce the ±12 VDC outputs at TB4 that connect to the control circuits in the metering control panel. This also produces the +12 VDC that is sent to the isolation relays in the power supplies and the blower assembly.

The 220 VAC main input to the bias power supply connects to terminal block TB1, terminals 1A and 2A (neutral) and 3A (ground). VR1 and VR2 are MOVs that protect the supply from any AC input line surges. The 220 VAC is applied through the closed contacts of (A3) the isolation relay to (A2) the bias power supply board as long as the bias circuit breaker on the AC control assembly is switched on. The bias-on command is applied to TB1-6 and the control power supply is on to produce the +12 VDC applied to TB1-5. The AC is connected to J1, pins 1 and 4, of (A2) the bias power supply board. The AC input is full-wave bridge rectified and filtered and regulated to produce the bias output at TB3-6 and TB3-7 that connect to the grid of the TH610 diacrode tube (typically –80 VDC).

4.2.3 Screen Power Supply Assembly

The (A6) screen power supply assembly, 60 Hz (1293-1321), provides the 500 VDC at 30 mA screen voltage to the tube mounted in the 10-kW diacrode amplifier assembly. The automatic turn-on procedure applies the screen voltage to the tube after it has applied the high voltage to prevent damage to the tube. The assembly consists of TB1, an input terminal block; (A7) an isolation relay board (1002-1108; Appendix B); (A8) a Sola 60-Hz regulator assembly; T1, a step-up transformer; (A6-A1) a screen power supply board (1293-1319; Appendix B); (A6-A3) a fan; and the output connections to the tube and the metering control panel.

The 220 VAC main input to the screen power supply connects to terminal block TB1, terminals 1A and 2A and 3A (ground). VR1 and VR2 are metal-oxide varistors (MOVs) that protect the supply from any AC input line surges. The 220 VAC is applied to the terminal block as long as the screen circuit breaker on the AC control assembly is switched on. The (A6-A3) fan will operate as long as the AC is applied to the terminal block. In addition, the red LED DS1 will be lit.

The 220 VAC is applied through the closed contacts of (A7) the isolation relay board, to (A8) the Sola regulator assembly, and to transformer T1 as long as the screen circuit breaker on the AC control assembly is switched on. The screen-on command is applied to TB1-6 and the control power supply is on to produce the +12 VDC that is applied to TB1-5.

The 220 VAC is connected to step-up transformer T1 to produce an approximately 540 VAC output that is applied to J1, pins 1 and 4, of (A6-A1) the screen power supply board. The AC input is full-wave bridge rectified, each path with four diodes in series; filtered by four 8-uF capacitors; and regulated by the zener diodes to produce the screen output at J3-1 and J3-5 that connects to the screen of the TH610 tube (typically 500 VDC). SCR-1 provides a crowbar protection circuit that eliminates the screen voltage, if it increases beyond the preset limit, to prevent damage to the tube. SCR-1 also causes a screen current fault condition and sends this information to the transmitter.

4.2.3.1 Screen Power Supply Board (1293-1319; Appendix B)

The screen power supply board provides the screen voltage (nominal 500 VDC) to the TH610 diacrode tube mounted in the cavity assembly of the 10-kW amplifier.

The screen power supply board operates when the screen circuit breaker on the AC control assembly is switched on and the (A7) isolation relay board, part of the screen power supply assembly, is energized by the screen-on command. The output of T1, the step-down transformer that is part of the screen power supply assembly, provides 550 VAC to J1-1 and J1-4 of the screen power supply board. The 550 VAC is applied to a full-wave bridge network that consists of CR1 to CR16. The diodes are in sets of four per leg for high-current and over-voltage protection. The output of the full-wave rectifier connects to four capacitors, C1 and C14 to C16, that are used for filtering. The filtered 780 VDC connects through the loading resistors R5 and R24 to the output regulating circuitry. If the output voltage increases above approximately 750 VDC, SCR-1 will energize and pull the output down to protect the tube from damage.

Zener diode VR21 prevents the output voltage from going negative. VR19 and VR20 protect the current metering circuit from damage in case of an arc in the tube or in the cavity assembly. VR22 and VR23 protect the voltage metering circuit from damage in case of overvoltage or an arc in the tube or in the cavity assembly. The voltage and current regulated DC (nominal +500 VDC) output of the board at J3, pins 1 and 5, is fed to the screen input connector of the 10-kW tube cavity assembly.

The screen voltage output can be adjusted by using variable resistor R14 on the board. Together, U1A and Q1 provide a voltage-regulator circuit for the screen voltage. U1A acts as a comparator that monitors the voltage setting of R14 at U1A, pin 12, and the voltage of the input at U1A, pin 13. The voltage levels that are applied to U1A will determine the amount of bias that is applied to Q1 as well as the output voltage level.

R20 can be adjusted and is used to calibrate the screen voltage at J4, pins 4 and 5, that connects to the voltage meter on the metering control panel. R9 can be adjusted and is used to calibrate the screen current reading at J4, pins 1 and 2, that connects to the current meter on the metering control panel. These adjustments were calibrated at the factory for typical operation and should not be readjusted.

4.2.4 Filament Power Supply Assembly

The filament power supply assembly (1299-1107) consists of input terminal block TB2, status and control terminal block TB1, the (A1) filament power supply control board (1293-1304; Appendix B), and the (A2) programmable filament power supply (1293-6302).

The 220 VAC is supplied at TB2-1A and TB2-2A and ground at TB2-3A. There are three MOVs (VR1 to VR3) mounted on the terminal block to protect against voltage spikes and transients. The 220 VAC is fed from TB2-1B, TB2-2B, and TB2-3B to (A2) the programmable filament power supply at TB1-L, TB1-N, and TB1-GND. The output of the power supply is fed to the filament of (A2-A1) the diacrode tube.

4.2.4.1 (A1) Filament Power Supply Control Board (1293-1304; Appendix B)

The filament power supply control board has five functions:

- Control and status of the three states of filament voltage (float, ramp, and operate) for the filament power supply
- Provide two on-board LEDs for status indication
- Provide adjustments to the operate voltage
- Monitor the operate status through monitoring the +12 VDC supply and 220 VAC power
- Adjust the front panel metering for the filament voltage and the tube run-time hour meter control

These functions are controlled through the software programming in U4, a Motorola MC68 microcontroller.

Filament Control

When the filament circuit breaker on the front panel is activated, the filament control board sets the program control at J3-1 to achieve an output from the power supply of 1.5 VDC. The output from U4 PA0-PA7 controls the DAC U3 voltage output at pin 16, which is buffered by U5 and sent to J3-1. After ten minutes of valid power supply operation, the control board sends a filament-ready signal at J4-2 out to the transmitter control board (1137-1003), allowing the transmitter to be placed in the Operate mode. Once the Operate switch has been enabled at the front panel, the power supply controller gradually increases the filament operating voltage. During the ramp-up phase, every 0.80 seconds the DAC output at J3-1 to the filament power supply is increased by one bit. Assuming no faults, the tube voltage reaches the operating range three minutes after closure of the Operate switch. J4-2 (filament OK) is a logic output to the transmitter control board. Logic 1 indicates that the filament power supply is at the operate or ramp-down voltage (-5.0 VDC). Logic 0 indicates that the power supply is at the float or ramp-up voltage (- less than 5.0 VDC). During ramp-down, this logic level is held high to direct the transmitter control board to keep the blower operating. The blower will continue to operate for three minutes after the float voltage level is reached.

On-board LED indicators

The on-board visual indication of the controller state is provided by LED DS1. This LED is off if the power supply is disabled; blinking at about 1 Hz if the float voltage is being held for ten minutes; blinking at about 2 Hz if the controller is ready to ramp up the filament voltage; blinking at 4 Hz if the controller is ramping the voltage up or down; and continuously on when the filament is at operate voltage levels. The

control for DS1 is from U4, PLMA, pin 20, to FET Q2.

DS2 is the Output Verified LED. It is used to indicate system status and is activated through pin 35 of U4 and FET Q3. Table 4-1 below lists the state, condition and flash-rate of the LED.

Table 4-1. State, Condition, and Flash Rate of LED DS2

STATE	CONDITION	LED FLASH RATE
Normal Condition	--	1.0 second on, 1.0 second off (0.5 Hz; 50% duty cycle)
AC Fault	J4-1 <4 VDC	One flash (0.2 second on), then pause 5 seconds
DC Fault	J1-3 <9 VDC	Two flashes (0.2 second on), then pause 5 seconds
DAC Fault	DAC = 4.625 Vout DAC = 0.0 Vout	Three flashes or four flashes (0.2 second on), then pause 5 seconds
Power Supply Fault	Power supply not regulating at float voltage	Five flashes (0.2 second on), then pause 5 seconds

Manual Operate Voltage Adjustment

Adjustment of the filament power supply is a two-step process. The system calibration of DAC, U3, using variable resistor R6 must first be verified. With the ten-minute ramp-up time complete and the transmitter still in stand-by, place SW1-7 in the On position. Verify that the output at J3-1 is 5.0 VDC; if it is not, adjust R6 until this voltage is achieved.

Note: Do not make the above adjustments with the transmitter in the Operate mode.

Once the system calibration voltage has been verified, monitor the output of the filament power supply during full power operation. This value should be 5.0 VDC. Adjust R28 on the filament control board to set this voltage.

Power Monitoring

Both the +12 VDC and the 220 VAC supply voltages are monitored. If the 220 VAC power is lost, the logic low at J4-1 will go high. This logic high is seen at PD1 of U4, which directs the microcontroller to ramp the filament control back to the float voltage. If the +12 VDC supply at J1-3 drops below nine volts, the filament control also ramps back to the float voltage. The +12 VDC voltage is monitored at U4, pin 3.

Front Panel Metering Control

The front panel metering adjustment is controlled by R15. Verify that the metering control rotary switch below the left-hand meter on the front panel is set to Filament. Monitor the filament power supply output and adjust R15 to obtain the same reading. The current metering adjustment on the control board is not used.

Tube Run-Time Hour Metering

When the operator closes the operate switch, J4-6 changes from a voltage level of twelve volts to approximately two volts. With J4-6 at two volts, relay R1 on the controller board is closed. This

enables the tube hour counter that is connected through connector J7-1 and J7-5.

Operational Voltages

The +12 VDC needed to operate the board enters at J1, pin 3, and is filtered by L1, C1, and C4 before it is fed to the rest of the board.

The -12 VDC needed to operate the board enters at J1, pin 5, and is filtered by L2 and C21 and C22 before being fed to the rest of the board.

The +5 VDC is supplied by 5-VDC regulator U1 and is filtered by C1 and C3 before being fed to the rest of the board.

C3 is used to maintain power on the +5-VDC line for short duration power losses.

DIP Switch Configuration

The DIP switch configurations for the board are shown in Table 4-2.

Table 4-2. DIP Switch Configurations for the Filament Power Supply Control Board

POSITION	FUNCTION
SW1-1	Not connected
SW1-2	Accelerate timers: When set high, the ramp-up, ramp-down, and blower delay timers operate four times faster
SW1-3	Ten-minute by-pass: When set high, and all other DIP switch settings are low except SW1-5, the ten-minute warm-up is skipped
SW1-4	SCADA: When set high, SCADA interrupts will be processed (future development)
SW1-5	Set DAC 0.0 VDC: When in the Standby mode, setting this switch high causes the DAC to output 0.0 VDC
SW1-6	Set DAC 4.625 VDC: When in the Standby mode, setting this switch high causes the DAC to output 4.625 VDC
SW1-7	Set DAC 5.0 VDC: When in the Standby mode, setting this switch high causes the DAC to output 5.0 VDC
SW1-8	Micro reset: When this is set high, the microcontroller is held in reset

4.2.5 Metering Control Panel

The (A7) metering control panel (1293-1308) contains three meters: one for voltages, one for currents, and one for power output. The voltage meter displays the plate, screen, bias, and filament voltages that are applied to the tube. The current meter displays the plate, screen, and grid currents that are produced by the tube. The power meter displays the % Aural Output power, % Visual Output power, and % Reflected Output power of the 10-kW amplifier. The metering control panel also provides the system control functions for the 10-kW transmitter.

The metering control panel consists of (A1) the control logic board (1137-1402), (A7) the transmitter control board (1137-1003), (A2 and A3) two differential buffer boards (1008-1017), (A4) fault sensing board, diacrode (1293-1307), (A5) fault sensing board, inverting (1016-1401), and (A6) the fault sensing board, dual polarity (1016-1402). The panel also has (M1) a front panel voltage meter with (S1) the meter control switch; (M2) a front panel current meter with (S2) the meter control switch and (S3) the meter reverse switch; and (M3) a front panel power meter with (S4) the meter control switch. The panel has (S5) the Operate/Standby switch, (S6) the Auto/Manual Mode Select switch, (S7) the High-Voltage Enable/Disable switch,

(S10) the Driver Mode Normal/Test switch, (S9) the Fault Reset switch, and (S8) the Power Output Raise/Lower switch.

The ±12 VDC needed to operate the boards in the metering control panel are provided to J2-1 (+12 VDC), J2-2 (±12 VDC Return), and J1-50 (-12 VDC) by the control section of (A5) the control and bias power supply assembly. The ±12 VDC is applied to the metering control panel when the control circuit breaker is switched on. The ±12 VDC connects to terminal block TB1 that, using jumpers, splits the ±12 VDC which is then fed to the boards in the metering control panel.

4.2.5.1 (A1) Control Logic Board (1137-1402; Appendix B)

The control logic board in the metering control panel provides the circuitry needed for the control of the automatic on/off sequence of the transmitter and the monitoring of the operation of the transmitter for fault conditions. An Operate command and the interlocks for the transmitter are also connected to the board. The board monitors the Air-On Sense, the Filament-On Sense, the Bias-On Sense, the High Voltage-On Sense, and the Screen-On Sense commands during each step of the automatic turn-on procedure. The board provides the On command outputs in the proper sequence as well as the enables to the Command Status and Operating Status LEDs on the front panel. The fault circuits monitor the operation of the power supplies and the tube, the air flow to the tube, and the temperature of the transmitter and will shut down the transmitter if any of these faults occur.

The board supplies the Air-On, Filament-On, Bias-On, Screen-On, High Voltage-On, and RF-On commands to the transmitter. The control logic board is connected to the High Voltage Enable/Disable switch and provides the commands to K1, the magnetic latching relay mounted on the board.

Operation of the Control Logic Board

When the Operate/Standby switch on the front panel of the metering control panel is switched to Operate, a Low Operate command from the transmitter control board is applied to J2-1 and lights the Operate LED connected to J12-1 and J12-2. The low at J2-1 is connected to the OR gate at U1-1. An external, total-shutdown interlock must be closed for the transmitter to operate. The low of the total-shutdown interlock is wired to J2-3, and connects to the board-mounted Total-Shutdown Interlock LED at J12-4 and J12-5, which will light. The low is also connected to OR gate U1-2 and, with both U1-1 and U1-2 low, the output at U1-3 will be low. The low from U1-3 connects to AND gates U2-1, U2-5, and U2-8. The low also connects to the OR gate U6-9. The IC U2, pins 1, 2, and 3, is located in the Blower-On command circuit. The U2-1 low causes the output at U2-3 to go low. This low connects to inverter IC U4, whose output at U4-2 goes high. The high forward biases Q1, whose collector goes low and applies the Low Blower, Air, On command at J17-1 of the board. The Blower, Air, On command connects through the front panel-mounted Command Status LED DS8, which will light. The blower control relay that energizes and turns on the blower is controlled by Q1. The operation of the blower causes air flow through the tube cavity assembly which is monitored by an air-flow switch mounted in the chimney. If the air flow is adequate, the switch closes and applies a low, air-on sense, to J2-5 of the board. This lights the front panel-mounted Operating Status Blower LED DS16.

The low, air-on sense at J2-5 connects to U1-5 in the Filament-On command circuit and lights the Blower, Air, On LED connected to J12-7 and J12-8. U2-5 is low and causes the output at U2-6 to be low. U1-6 and U1-5 are both low, which causes the output to go low. The low connects to inverter U4, whose output at

pin 4 goes high. The high forward biases Q2, whose collector goes low and applies the Low Filament-On command through the front panel-mounted Command Status Filament LED DS9, which will light, to the Filament Control Relay. The low energizes the relay and turns On the filament power supply. The output voltage from the filament power supply is monitored and produces a low, filament-on sense input to the board at J2-7. This action lights the front panel-mounted Operating Status Filament LED DS17.

The low, filament-on sense at J2-7 is applied to U8, a clock IC that times out at approximately two minutes to allow the tube to preheat before the rest of the voltages are applied. Moving jumper W1 on J11 changes the timer from two minutes to approximately 18 seconds. When the timer clocks out, a high is applied to inverter U7-5, whose output at U7-4 goes low and connects to U6-2 in the Bias-On command circuit. As long as the filament voltage stays above 3.5 VDC, the filament under-voltage input at J2-9 will be low and is applied to U6-3. U6-4 will be a low as long as the transmitter is in Operate or the bias voltage is present to the tube. Since U2 is an AND gate, either input low will cause the output to be low. With all inputs to U6 low, the output at U6-1 will be low. The low is connected to inverter U4-7, whose output at U4-6 goes high. The high is applied to Q3, which is forward biased, and causes the collector to go low. The Low Bias-On command output at J7-6 connects through the front panel-mounted Command Status Bias LED DS12, causing it to light, to the bias control relay, which energizes and turns on the bias power supply. The output voltage from the bias power supply is monitored and produces a low, bias on sense input to the board at J3-3, which lights the front panel-mounted Operating Status Bias LED DS18, connected to J13-1 and J13-2.

The low, bias on sense at J3-3 is applied to U3-3 in the High Voltage-On command circuit and to U2-6 in the Filament-On command circuit. U3-4 connects to the fault circuit on the board and will be low unless a fault occurs. U3-5 will be low unless both the high voltage is disabled and the screen voltage is removed from the tube. With U3-3, U3-4, and U3-5 all low, this causes a low at U3-6 that is connected to inverter IC U4-9, whose output at U4-10 goes high. The high forward biases Q4 and causes its collector to go low and apply the High Voltage-On command through the front panel-mounted Command Status High Voltage LED DS11, which will light, to the high-voltage control relay. The relay energizes and turns on the high-voltage power supply. The output voltage from the high-voltage power supply is monitored and produces a low, high voltage-on sense input to the board at J3-7 and lights the front panel-mounted Operating Status High Voltage LED DS19.

The low, high voltage on sense at J3-7 is applied to U21-6 in the Screen Voltage-On Command circuit and to U2-9 in the Bias On command circuit. U21-5 will be a low if both the high voltage is enabled, U21-8 low, and the screen interlock is closed, U21-9 low. When U21-5 and U21-6 are both low, this causes a low at U21-4 that is connected to inverter IC U13-3, whose output at U13-2 goes high. The high forward biases Q5 and causes its collector to go low, which applies the Screen-On command through the front panel-mounted Command Status Screen LED DS12, causing it to light, to the screen control relay. The relay energizes and turns on the screen power supply. This logic circuit prevents the screen power supply from turning on unless the high voltage is present to the tube. The output voltage from the screen power supply is monitored and produces a low, screen on sense input to the board at J3-11, which lights the front panel-mounted Operating Status Screen LED DS20.

The low, screen voltage-on sense at J3-11 is applied to U21-2 in the RF-On command circuit and to U2-13 in the

High Voltage-On command circuit. U21-1, which connects to U21-10, will be a low if both the high voltage is enabled, U21-8 low, and the screen interlock is closed, U21-9 low. When U21-1 and U21-2 are both low, this causes a low at U21-3, which is connected to inverter IC U13-5, and whose output at U13-4 goes high. The high forward biases Q7, causing its collector at J9-11 to go low and apply the RF-On command to the exciter. J9-10 also goes low and lights the front panel-mounted Command Status RF Request LED DS13. The low at U21-3 is also connected to the base of Q6, which reverse biases it and removes the mute from the 3-watt amplifier tray.

The transmitter should be fully operational at this time with an RF output.

Operation of the Fault Circuits

The control logic board monitors thermal switch A11-S1, control grid I, cathode I, and the reflected power, VSWR, for faults. If a fault occurs in any of the circuits monitored, a low from the thermal switch and/or the cathode current and/or a high from the control grid current, screen I, or VSWR is applied to the board. The fault causes the transmitter to reset itself three times, each time trying to go back on the air, to make sure that the fault is real. After three resets, the transmitter switches to Standby.

If thermal switch A11-S1, mounted in the exhaust stack of the tube cavity assembly, closes due to overheating, a low is connected to J5-3. The low connects to inverter IC U7-11, whose output at U11-12 goes high. The high connects to pin 6, the S1 set input, to one of four quad R-S latches that make up U16. The output of the latch at pin 9 goes high and connects to U1-9 and also to the base of Q8. Q8 is forward biased and its collector goes low, lighting the Overtemperature LED DS22 on the front panel. The output of the OR gate U1-10 goes high and connects to U6-12. The output of U6 goes high and removes the high voltage enable from the logic circuit that removes the enables to the screen voltage and the high-voltage power supplies.

If a problem occurs with the control grid current, a high is connected to J5-5. The fault high connects to pin 4 the S0 set input to one of four quad R-S latches that make up U16. The output of the latch at pin 2 goes high and connects to U3-11, whose output at pin 10 goes high. The high connects to U15-1, the three-fault counter, and also to U19-8 and U19-9. U19-10 goes high and forward biases Q9, whose collector goes low, lighting the Fault Indicator LED DS7 on the front panel.

The fault high at J5-5 also connects to the set S3 input at pin 14 to one of four quad R-S latches that make up U20 and to U11-5. The output of the latch at U20-1 goes high and is inverted by U18. The low is applied to DS12, the Bias Fault LED, on the board, which will light. Because the input to U11 at pin 5 is high, the output of U11 at pin 1 goes high, which resets clock IC U9. The Q1 and Q0 outputs of U9 go low during reset, then back to high, and are applied to U14, whose output will be high when both inputs are high. The high from U14-4 is connected to U14-2 and, when U14-1 goes high, the output at U14-3 goes high and resets three of the R-S latches that make up U16. The transmitter will reset three times to confirm that a fault has actually occurred and counter IC U15 will count each time a high is applied to pin 1. After the third fault, the U15 IC will latch and produce a low at U7-15 that connects to the Three Fault LED DS11, causing it to light.

If a problem occurs with reflected power, VSWR, a high is connected to J5-7. The fault high connects to pin 14, the S3 set input, to one of four quad R-S latches that make up U16. The output of the latch at pin 1 goes high and connects to

U3-12, whose output at pin 10 goes high. The high connects to U15-1, the three fault counter IC, and also to U19-8 and U19-9. U19-10 goes high and forward biases Q9, whose collector goes low and lights the Fault Indicator LED DS7 on the front panel. The fault high at J5-7 also connects to the set S1 input at pin 6, to one of four quad R-S latches that make up U20, and to U11-4. The output of the latch at U20-9 goes high and is inverted by U18. The low is applied to DS13, the VSWR Fault LED on the board, which will light. Because the input of U11 at pin 4 is high, the output of U11 at pin 1 goes high and resets clock IC U9. The Q1 and Q0 outputs of U9 go low during reset, then back to high, and are applied to U14, whose output will be high when both inputs are high. The high from U14-4 is connected to U14-2 and, when U14-1 also goes high, the output at U14-3 goes high, resetting the three R-S latches that make up U16. The transmitter will reset three times to confirm that a fault has actually occurred and counter IC U15 will count each time a high is applied to pin 1. After the third fault, the U15 IC will latch and produce a low at U7-15, which connects to the Three Fault LED DS11, causing it to light.

If a problem occurs with screen I, a high is connected to J6-1. The fault high connects to pin 12 of U12, whose output at pin 11 goes high. The high connects to pin 12, the S2 set input of one of four quad R-S latches that make up U16, and to U11-3. The output of the latch at pin 10 goes high and connects to U3-13 and U3-4. The U3-4 high causes the output of U3 at pin 6 to go high and be inverted by U4. The low output at pin 10 connects to Q4, which turns the transistor off and removes the High Voltage-On command.

With U3-13 high, the output of U3 at pin 10 goes high. The high connects to U15-1, the three fault counter, and also to U19-8 and U19-9. U19-10 goes high and forward biases Q9, whose collector goes low and lights the Fault Indicator LED DS7 on the front panel. The fault high at J6-1 also connects to the set S2 input at pin 12 and to one of four quad R-S latches that make up U20. U20-10 goes high and is inverted by U18 and applied to DS14, the Screen I Fault LED on the Board, causing it to light.

Because of the high on its input at U11-3, the output of U11 at pin 1 goes high and resets clock IC U9. The Q1 and Q0 outputs of U9 go low during reset, then back to high, and are applied to U14, whose output will be high when both inputs are high. The high is connected to U14-2 and, when U14-1 goes high, the output at U14-3 also goes high and resets the three R-S latches that make up U16. The transmitter will reset three times to confirm that a fault has actually occurred and counter IC U15 will count each time a high is applied to pin 1. After the third fault, the U15 IC will latch. It produces a low at U7-15 and connects to the Three Fault LED DS11, causing it to light.

If a problem occurs with cathode I, a low is connected to J6-6. The fault low is inverted to a high by U18 and then connects to pin 13 of U12, whose output at pin 11 goes high. The high connects to pin 12, the S2 set input of one of four quad R-S latches that make up U16, and to U11-3. The output of the latch at pin 10 goes high and connects to U3-13 and to U3-4. When U3-4 is high, it causes the output of U3 at pin 6 to go high and be inverted by U4. The low output at pin 10 connects to Q4; this turns the transistor off and removes the High Voltage-On command. A high on U3-13 causes the output at pin 10 to go high. The high connects to U15-1, the three fault counter, and to U19-8 and U19-9. U19-10 goes high and forward biases Q9, whose collector goes low and lights the Fault Indicator LED DS7 on the front panel.

The fault high from U18 connects to the set S0 input at pin 4 and to one of four quad R-S latches that make up U20. U20-2 goes high and is inverted by U18;

this is applied to DS15, the Cathode I Fault LED on the board, causing it to light. Because of the high on its input at U11-3, the output of U11 at pin 1 goes high and resets clock IC U9. The Q1 and Q0 outputs of U9 go low during reset, then back to high, and are applied to U14, whose output will be high when both inputs are high. The high is connected to U14-2 and, when U14-1 goes high, the output at U14-3 also goes high and resets the three R-S latches that make up U16. The transmitter will reset three times, to confirm that a fault has actually occurred, and counter IC U15 will count each time a high is applied to pin 1. After the third fault, the U15 IC will latch and produce a low at U7-15 that connects to the Three Fault LED DS11, causing it to light.

After the problem that caused the fault is corrected, the fault circuit is reset by switching the front panel-mounted reset switch S9. This places a low at J6-9 on the board that is inverted by U18. The high is connected to pin 7, the R1 reset input of one of four quad R-S latches that make up U16, and to U12-8. The high at pin 7 of U16 resets the temperature fault circuit. The high at U12-8 causes the output of U12 at pin 10 to go high and connects to the reset input at pin 7 of U15. U15 then resets the front panel-mounted fault indicator and the fault circuits associated with U16. The three-fault indicator and the other fault indicators that are lit on the board are reset by switching S1.

The +12 VDC needed for the operation of the board enters at jack J1, pin 1. C1, C2 and C3, and L1 are for the filtering and isolation of the +12 VDC before it is applied to the rest of the board.

4.2.5.2 Transmitter Control Board (1137-1003; Appendix B)

The transmitter control board in the metering control panel provides the system control functions for the transmitter. The board supplies the interlock to the exciter tray and also provides the outputs to the function indicator LEDs on the front panel of the metering control panel. The transmitter control board will switch the transmitter to Standby upon the loss of the video input from the modulator or from the receiver tray, if present, when the transmitter is in Automatic.

When the Operate/Standby switch on the front panel of the metering control panel is switched to Operate (J11-8 low), and the Normal/Exciter Test switch is in Normal (K4 energized), K3 energizes and applies a low to inverter U8F, causing its output to go high. The low from K3 also biases off Q23 and Q24; this removes the Standby commands. The high output of U8F, at pin 15, forward biases Q18 to Q22 and applies the Operate commands to the control logic board. The low is also applied through diode CR12 to pin 11 of inverter U8E, causing its output to go high. The high forward biases Q26 and Q27; this causes the drains to go low and lights DS14, the front panel Normal LED connected to J14, pins 8 and 6. The high output of U8E also connects to pin 5, the input to inverter U8B, causing the output at pin 4 to go low. The low is applied to Q28 to Q33, biasing them off and removing the exciter test functions.

When the Operate/Standby switch on the front panel of the metering control panel is switched to Standby (J11-2 low), and the Normal/Exciter Test switch is in Normal (K4 energized), K3 de-energizes and applies a high to inverter U8F, pin 14, and also to Q23 and Q24. As a result, Q23 and Q24 are forward biased; this produces a low at J12, pin 3, and lights DS2, the front panel-mounted Standby LED. The high on inverter U8F, pin 14, causes the output at pin 15 to go low. The low reverse biases Q18 to Q22 and removes the Operate commands to the control logic board and the amplifier trays. The high from K3 is also applied to diode CR12, causing it to reverse bias.

When the Exciter Test switch is in Normal, with K4 energized, it applies a low to CR13 and then to inverter U8E, pin 11, whose output at pin 12 then goes high. The high also forward biases Q26 and Q27 and lights DS14, the front panel-mounted Normal LED connected to J14, pins 8 and 6. The high input to inverter U8B, pin 5, causes the output at pin 4 to go low. The low is applied to Q28 to Q33, biasing them off and removing the exciter test functions.

The exciter can be operated without using the 10-kW amplifier by switching the Normal/Exciter Test switch on the front panel of the metering control panel to the Exciter Test position. With the switch in this position, K4 is de-energized and a high is applied to diode CR13, causing it to reverse bias. The high from K4 is also applied to Q25, which forward biases it and produces a low at pin 4 of the K3 relay. The low at pin 4 de-energizes the relay and produces a high that is applied to diode CR12, causing it to reverse bias. Both CR12 and CR13 are reverse biased; as a result, a high from +12 VDC and R61 is applied to pin 11 of U8E and causes its output at pin 12 to go low. The low connects to Q26 and Q27 and biases them off. The low is also applied to inverter U8B, pin 5, whose output at pin 4 goes high. The high connects to Q28 to Q33, forward biases them, applies a low to the exciter tray, lights the Exciter Test LED, and sets up the exciter to operate without the need for the 10-kW amplifier.

The Auto/Manual Test switch S6 on the front panel controls K1, the magnetic latching relay, by connecting a low input to the board at J2, pins 7 and 8, for Manual or to J2, pins 4 and 3, for Automatic. When the Test switch is moved to the Auto position, a low is applied to K1, pin 6, that energizes the relay and applies a low to U7F, pin 14, causing its output to go high. The high is applied to Q5 and Q7, forward biasing them, and produces a low at their drain. The low lights the front panel Automatic LED. With the Test switch in the Manual position, a low is applied to K1, pin 4; this de-energizes the relay and connects a high from K1, pin 2, to Q6, forward biasing it and producing a low at its drain. The low lights the front panel-mounted Manual LED DS4. The high output of K1 is also applied to U7F, pin 14, whose output goes low. The low is applied to Q5 and Q7, which reverse biases them, and extinguishes the front panel Automatic LED.

The board also supplies the option that allows for the automatic switching of the transmitter between a receiver tray or a modulator tray that is used as the input tray based on the presence of video to the modulator or the receiver tray. A receiver tray, a modulator tray, and an IF relay, to switch between the two outputs, must be present in the transmitter for the automatic switching to take place. For automatic switching, jumper W2 on J17 must be in Auto, between pins 1 and 2. Jumper W1 on J18 determines which tray will be in control. The modulator tray will be in control if W1 is between pins 1 and 2.

If a modulator and a receiver tray are in place, the jumpers are set as stated above, and the video input to the modulator is present, a high will be present at J2, pin 11. The high connects to inverter U7B, pin 5, whose output at pin 4 goes low. The low turns off the red Video Fault LED DS3. The high also connects to timer U1A, pin 5, and directly to NOR gate U5C, pin 9. The high at the NOR gate produces a low output at U5C, pin 10; this low is applied through jumper W1 on J18 and jumper W2 on J17 to the bases of Q8 to Q11. Q8 to Q11 are reversed biased and apply the disables to the IF relay to keep the output of the modulator tray connected to the input of the upconverter tray. In addition, because Q11 is biased off, Q12 to Q14 will have highs applied to their bases to bias them on. DS5, the green Modulator On LED, will be lit.

If the video input to the modulator is removed, a video fault low is applied to J2, pin 11. The low connects to inverter U7B, pin 5, whose output at pin 4 goes high. The high lights the red Video Fault LED DS3. The low connects to timer U1A, pin 5, and also connects directly to NOR gate U5C, pin 9. After 5 seconds, enough time for the loss of video to be determined as permanent, the output of U1A at pin 8 will go low; the low is applied to U5C, pin 8. With U5C pins 8 and 9 both low, the output of U5C at pin 10 will go high. The high is applied through jumper W1 on J18 and jumper W2 on J17 to the bases of Q8 to Q11. Q8 to Q11 are forward biased and apply the low enables to the IF relay to connect the output of the receiver tray to the input of the upconverter tray and also to the green Receiver On LED DS4 and the external Receiver On LED.

During normal operation, there is no video fault input from the exciter tray and there is a high at J16, pin 1. The high is applied to inverter U7C, pin 7, whose output at pin 6 goes low and extinguishes the red Video Fault LED DS2. The high is also applied to AND gate U6B, pin 6. Pin 5 of U6B will be a high during normal operation. A high on pins 5 and 6 of U6B produces a high output at pin 4. The high is applied immediately to pin 6 of NOR gate U5B and to pin 11 of counter U1B. After approximately 6 seconds, enough time to determine that a genuine fault has occurred, a high is applied to pin 5 of U5B. The high on pin 5 and pin 6 of U5B produces a low on pin 4. The low is applied to NOR gate U5D, pin 12, and, if the Automatic/Manual switch is in Auto, a low will also be on U5D, pin 13. Lows on pins 12 and 13 of U5D will cause the output at pin 11 to go high and forward bias Q2. The drain of Q2 will go low and is applied to J11, pin 8, and then to Operate/Standby relay K3. The relay stays energized and in Operate. The low from pin 4 of U5B is also fed through inverter U7E, whose output at pin 12 is now high. The high connects to NOR gate U5A, pin 2. If either pin 1 or 2, or both pin 1 and 2, are high, a low is produced at the output of U5A, pin 3. The low reverse biases Q3 and removes the low from the drain and from J4, pin 4.

If a video fault from the exciter tray occurs due to the loss of video, J16, pin 1, goes low. This low is applied to inverter U7C, pin 7, whose output at pin 6 goes high and lights the red Video Fault LED DS2. The low video fault is also applied to AND gate U6B, pin 6. The level of the ALC voltage from the receiver tray is fed through op-amp U3D and produces a high output as long as the ALC level from the receiver tray is above the reference set by R3. This normally high output from U3D connects to pin 5 of AND gate U6B.

If the ALC level drops below the threshold set by R3, pin 5 of U6B will go low. A low on pin 5 or pin 6, or both pin 5 and pin 6, will produce a low on U6B, pin 4. The low is applied immediately to pin 6 of NOR gate U5B and to pin 11 of counter U1B. After approximately 6 seconds, enough time to determine that a genuine fault has occurred, the low is applied to pin 5 of U5B. The low on pin 5 and pin 6 of NOR gate U5B produces a high output on pin 4. The high is applied to NOR gate U5D, pin 12, and causes the output at pin 11 to go low and reverse bias Q2. The drain of Q2 will go high and the high is applied to J11, pin 8, and then to the Operate/Standby relay K3. The high from pin 4 of U5B is also fed through inverter U7E whose output at pin 12 is now low. The low connects to NOR gate U5A, pin 2. If the Auto/Manual switch is in Auto, U5A, pin 1, will be low. When pins 1 and 2 on U5A are both low, it produces a high at pin 3 that forward biases Q3. The drain of Q3 goes low and is applied to J11, pin 2, and then to the Operate/ Standby switch, which switches the transmitter to Standby. If the Auto/Manual switch is in Manual, U5A, pin 1, will be high and the output of U5A at pin 3 will be low; this does not affect the operation of the transmitter.

A forward power sample of the RF output of the transmitter is connected to J15, pin 7, of the board. The sample connects to op-amp U3A, pin 3. If the input sample level stays above the level set by R38, the output of U3A at pin 1 will be high. The high forward biases Q15 and Q16 and causes their drains to go low. J14, pin 2, is low and connects to the front panel RF Present LED DS21, causing it to light.

A reflected power sample of the RF output of the transmitter is connected to J15, pin 1, of the board. The sample connects to op-amp U3C, pin 10. If the input sample level increases above the level set by R44, the output of U3C at pin 8 will go high. The high is fed out of the board at J16, pins 10 and 9, to the 3-watt tray. This cuts back the output of the tray and, in turn, the output power of the transmitter. The high is also fed to the base of Q17 and forward biases the transistor to produce a low at J16, pin 7. The low connects to the front panel VSWR Cutback LED DS23 and causes it to light.

The +12 VDC needed for the operation of the board enters the board at jack J1, pin 3. C18 and L1 are for the filtering and isolation of the +12 VDC before it is applied to the rest of the board.

4.2.5.3 (A2) Differential Buffer Board (1008-1017; Appendix B)

The (A2) differential buffer board (1008-1017) takes the sample voltage readings from the external power supplies and provides readings to the voltage panel meter and the metering control panel interface for remote monitoring. The differential buffer board also supplies screen-on sense and filament-on sense readings to (A4) the fault sensing board, diacrode. The fault sensing board, inverting, supplies the high voltage-on sense, the screen-on sense, the filament-on sense, and the filament under-voltage readings to the control logic board. In addition, the differential buffer board supplies a bias-on sense to (A5) the fault sensing board.

The (A3) differential buffer board (1008-1017) takes the sample current readings from the external power supplies and provides readings to the current panel meter and the metering control panel interface for remote monitoring.

The (A3) differential buffer board also supplies screen current and grid current readings to (A6) the fault sensing board, dual polarity. The fault sensing board, dual polarity, supplies the screen current and grid current fault readings to the control logic board. The (A3) differential buffer board supplies cathode-on sense readings to (A5) the fault sensing board, inverting. The fault sensing board, inverting, supplies the cathode current fault readings to the control logic board.

4.2.5.4 Fault Sense Board, Diacrode (1293-1307; Appendix B)

The fault sense board, diacrode, provides an inverted output for a sample input.

All the circuits on the board are the same. A filament-on sense sample is applied to J1-8 of the board. This high, which indicates that the filament is operating, is fed to comparator IC U1, pin 9, and is compared to a reference level set by R18. If the sample filament voltage level is greater than this reference level, a high output from U1, pin 14, is connected to U2, pin 7, an inverting amplifier. The high is inverted to a low at U2, pin 6. The low output of the board at J4, pin 8, is connected to the control logic board where it provides the low filament-on sense to the automatic on/off sequence. If the sample input is less than the reference set by the pot, a low output from U1, pin 14, is connected to U2, pin 7, which is an inverting amplifier. The low is inverted to a high at U2, pin 6. The high output of the board at J4, pin 8, is connected to the control logic board. The control logic

board removes the filament-on sense to the automatic on/off sequence.

The fault sense board is supplied by a +12VDC source at J3-3. The capacitors C1 and C2 provide filtering.

4.2.5.5 Inverting Fault Sense Board (1016-1401; Appendix B)

The inverting fault sense board provides an inverted output for a sample input, generally from the differential buffer board.

For example, a filament-on sense sample is applied to J1-8 of the board. This high, which indicates that the filament is operating, is fed to comparator IC U1, pin 9, and compared to a reference level set by R18. If the sample filament voltage level is greater than this reference level, a high output from U1, pin 14, is connected to U2, pin 7, which is an inverting amplifier. The high is inverted to a low at U2, pin 6. The low output of the board at J4, pin 8, is connected to the control logic board where it provides the low filament-on sense to the automatic on/off sequence. If the sample input is less than the reference set by the pot, a low output from U1, pin 14, is connected to U2, pin 7, the inverting amplifier. The low is inverted to a high at U2, pin 6. The high output of the board at J4, pin 8, is connected to the control logic board. The control logic board removes the filament-on sense to the automatic on/off sequence.

The other inputs to the board are handled in the same way.

4.2.5.6 Dual Polarity Fault Sensing Board (1016-1402; Appendix B)

The dual polarity fault sensing board provides a high-fault output or a low-normal output at J2-5 or J2-4 that is typically connected to the control logic board. When this board is used in the 10-kW amplifier, J4-1 is jumpered to J4-4 and J1-3 is jumpered to J1-6. The jumpering provides an upper and lower limit circuit for the two current sample inputs.

A sample of the screen current is applied to J4-2 on the board. From J4-2, the screen current sample is connected to comparator U1, pin 5. R6 sets the upper limit trip point for this section of the IC. If the screen current remains below this reference level, U1, pin 2, will go low and the low is applied to NAND gate U2, pins 1 and 2. U2, pin 3, will go high and the high is applied to NAND gate U2, pin 5. Because J4-1 is jumpered to J4-4, the input sample of the screen current is also applied to U1, pin 7. R12 sets the lower limit trip point for this section of the IC. If the screen current remains above this reference level, U1, pin 1, will go high and the high is applied to NAND gate U2, pin 6. U2, pin 5, is high and U2, pin 6, is also high during normal operation; this causes NAND gate U2, pin 4, to be low. During normal operation, there is a low output on the board at J2, pin 5.

If the screen current sample applied to comparator U1, pin 5, increases above the upper limit trip point set by R6, U1, pin 2, will go high. The high is applied to NAND gate U2, pins 1 and 2. U2, pin 3, will go low and the low is applied to NAND gate U2, pin 5. Because J4-1 is jumpered to J4-4, the input sample of the screen current is also applied to U1, pin 7. R12 sets the lower limit trip point for this section of the IC. If the screen current remains above this reference level, U1, pin 1, will go high and the high is applied to NAND gate U2, pin 6. U2, pin 5, is now low and U2, pin 6, is high; this causes NAND gate U2, pin 4, to be high. A high output of the board at J2, pin 5, is a screen current fault condition.

The screen current sample is applied to J4-2 of the board and jumpered to J4-4. From J4-2, the current sample is connected to comparator U1, pin 5. R6 sets the upper limit trip point for this section of the IC. If the screen current

remains below this reference level, U1, pin 2, will go low and the low is applied to NAND gate U2, pins 1 and 2. U2, pin 3, will go high and the high is applied to NAND gate U2, pin 5. Because J4-1 is jumpered to J4-4, the input sample of the low screen current is also applied to U1, pin 7. R12 sets the lower limit trip point for this section of the IC. If the screen current decreases below this reference level, U1, pin 1, will go low and the low is applied to NAND gate U2, pin 6. At this point, U2, pin 5, is high and U2, pin 6, is low, causing NAND gate U2, pin 4, to be high. A high output from the board at J2, pin 5, is a screen current fault condition.

A sample of the grid current is applied to J1-4 of the board. From J1-4, the current sample is connected to comparator U1, pin 9. R18 sets the upper limit trip point for this section of the IC. If the grid current remains below this reference level, U1, pin 14, will go low and the low is applied to NAND gate U2, pins 8 and 9. U2, pin 10, will go high and the high is applied to NAND gate U2, pin 12. Because J1-3 is jumpered to J1-6, the input sample of the grid current is also applied to U1, pin 11. R25 sets the lower limit trip point for this section of the IC. If the grid current remains above this reference level, U1, pin 13, will go high and the high is applied to NAND gate U2, pin 13. During normal operation, U2, pin 12, and U2, pin 13, are both high. This causes NAND gate U2, pin 11, to be low. A low output from the board at J2, pin 4, occurs during normal operation.

If the grid current sample applied to comparator U1, pin 9, increases above the upper limit trip point set by R18, U1, pin 14, will go high. The high is applied to NAND gate U2, pins 8 and 9. U2, pin 10, will go low and the low is applied to NAND gate U2, pin 12. Because J1-3 is jumpered to J1-6, the input sample of the grid current is also applied to U1, pin 11. R25 sets the lower limit trip point for this section of the IC. If the grid current remains above this reference level, U1, pin 13, will go high and the high is applied to NAND gate U2, pin 13. U2, pin 12, is now low and U2, pin 13, is high; this causes NAND gate U2, pin 11, to be high. A high output from the board at J2, pin 4, is a grid current fault condition.

The grid current sample is applied to J1-4 on the board and jumpered to J1-7. From J1-4, the current sample is connected to comparator U1, pin 9. R18 sets the upper limit trip point for this section of the IC. If the grid current remains below this reference level, U1, pin 14, will go low and the low is applied to NAND gate U2, pins 8 and 9. U2, pin 10, will go high and the high is applied to NAND gate U2, pin 12. Because J1-3 is jumpered to J1-6, the input sample of the low grid current is also applied to U1, pin 11. R25 sets the lower limit trip point for this section of the IC. If the grid current decreases below this reference level, U1, pin 13, will go low and the low is applied to NAND gate U2, pin 13. At this point, U2, pin 12, is high and U2, pin 13, is low, causing NAND gate U2, pin 11, to be high. A high output from the board at J2, pin 4, is a grid current fault condition.

4.3 (A3) High-Voltage Power Supply Assembly, 208/240 VAC (1068022; Appendix A)

4.3.1 Current Metering Board (1084-1205; Appendix B)

The current metering board takes a voltage sample from an operating power supply and provides an output level that can be used in a current metering circuit.

The sample voltage input is applied at J1, pins 1 and 3, and is fed to a pi-attenuator network consisting of R1, R2, R3, and R4. The value of R1 can be changed to increase or lower the value of the input voltage for the desired current meter reading. R3 can be adjusted to calibrate the output level and display an accurate meter reading of the current value.

VR1 and VR2 are back-to-back 10 VDC zener diodes that protect the external metering circuits from a high-voltage problem by shunting out the higher voltage and allowing only a maximum of ±10 VDC to be present at the output.

C1 is an AC bypass capacitor for the reduction of any AC ripple at the output. The external current metering circuit connects to J2, pins 1 and 3.

4.3.2 (A10 and A11) Power Supply Metering Boards (1084-1213 and 1016-1028; Appendix B)

The power supply metering board takes a voltage sample from an operating power supply and provides an output level that is used in a metering circuit.

The sample voltage input is applied at J1, pins 1 and 3, and is fed to a pi-attenuator network consisting of R1, R2, R3, and R4. The value of R1 can be changed to increase or lower the value of the input voltage for the chosen output meter reading. R3 can be adjusted to calibrate the output level to allow an accurate meter reading of the value to be displayed.

VR1 and VR2 are back-to-back 10-VDC zener diodes that protect the external metering circuits from a high-voltage problem by shunting out the higher voltage and allowing only a maximum of ±10 VDC to be present at the output.

C1 is an AC bypass capacitor for the reduction of any AC ripple at the output. The external metering circuit connects to J2, pins 1 and 3.

4.3.3 (A5, A6, and A7) High-Voltage Rectifier Board (1293-1101; Appendix B)

The high-voltage rectifier board provides a full-wave rectifier for the AC input. A total of three high-voltage rectifier boards are used with a three-phase AC input: one for each of the three 2.6 kVAC output legs of the high-voltage transformer.

The high-voltage rectifier board has a 4-amp fuse mounted at the (E1) AC input to protect the board from surges or spikes on the AC input line. The input AC is applied to two rows of diodes: one for positive and one for negative rectification. Each row contains 17 diodes in series that provide for peak inverse high-voltage protection. Each diode has a 1 MW/½-W resistor and a .001 mF/3-kV capacitor, mounted in parallel, that creates equal distribution of the voltage across each diode.

The positive leg of diodes connects to the E2 (+) terminal. The negative leg of diodes connects to the E3 (-) terminal. The positive and negative outputs of one high-voltage rectifier board connects to the positive and negative outputs of the other two high-voltage rectifier boards.