INSTRUCTION MANUAL

DT830A

300-WATT DIGITAL UHF TRANSMITTER

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Chapter 1
Introduction

This manual explains the installation, setup, alignment, and maintenance procedures for the DT830A 300-watt digital UHF transmitter. It is important that you read all of the instructions, especially the safety information in this chapter, before you begin to install or operate the unit.

1.1 Manual Overview

This instruction manual is divided into five chapters and supporting appendices. Chapter 1, Introduction, contains information on safety, the Axcera method of assigning assembly designation numbers, maintenance, return procedures, and warranties. The second chapter describes the transmitter and its system control and status indicators and remote control connections. Chapter 3 explains how to unpack, install, set up, and operate the transmitter. Chapter 4, Circuit Descriptions, describes the circuits that make up the trays and assemblies in the transmitter. Chapter 5, Detailed Alignment Procedures, provides information on adjusting the system assemblies for optimal operation. The appendices contain sample log sheets, typical operational readings, assembly and subassembly drawings and parts list, and product information for vendor-supplied products used in the transmitter.

1.2 Assembly Designation Numbers

Axcera has assigned assembly numbers, such as Ax (x=1,2,3…), to all assemblies, trays, and boards that are referenced in the text of this manual and shown on the block diagrams and interconnect drawings provided in the appendices. These supporting documents are arranged in increasing numerical order in the appendices. Section titles in the text for assembly or tray descriptions or alignment procedures also indicate the associated part number(s) and the relevant appendices. Sections describing vendor-supplied items, such as meters and power supplies, do not contain this information.

1.3 Safety

The 300-watt UHF transmitters manufactured by Axcera are designed to be easy to use and repair while providing protection from electrical and mechanical hazards. Listed throughout the manual are notes, cautions, and warnings concerning possible safety hazards that may be encountered while operating or servicing the transmitter. Please review these warnings and familiarize yourself with the operation and servicing procedures before working on the transmitter.

Read All Instructions – All of the operating and safety instructions should be read and understood before operating this equipment.

Retain Manuals – The manuals for the transmitter should be retained at the transmitter site for future reference. We provide two sets of manuals for this purpose; one set can be left at the office while one set can be kept at the site.

Heed Notes, Warnings, and Cautions – All of the notes, warnings, and cautions listed in this safety section and throughout the manual must be followed.

Follow Instructions – All of the operating and use instructions for the transmitter should be followed.

Cleaning – Unplug or otherwise disconnect power from the equipment before cleaning. Do not use liquid or aerosol cleaners. Use a damp cloth for cleaning.

Ventilation – Openings in the cabinets and tray front panels are provided for ventilation. To ensure reliable operation, and to protect the unit from overheating, these openings must not be blocked.

Servicing – Do not attempt to service this product until becoming familiar with the equipment. If in doubt, refer all servicing questions to qualified Axcera service personnel.

Replacement Parts – When replacement parts are used, be sure that the parts have the same functional and performance characteristics as the original part. Unauthorized substitutions may result in fire, electric shock, or other hazards. Please contact the Axcera Technical Service Department if you have any questions regarding service or replacement parts.

Caution: Because the capacitors used in the high-voltage circuits have the potential of recharging themselves, care must be taken when handling them. The capacitors should first be shorted with a grounding stick and then a piece of wire should be connected across the terminals until they can be put into service. Remember to remove the shorting wire before energizing the high-voltage supply.

1.4 Maintenance

The DT830A is designed with components that require little or no periodic maintenance except for the routine cleaning of the fans and the front panels of the trays.

The amount and time interval between cleanings depends on the conditions within the transmitter room. While the electronics have been designed to function even if covered with dust, a heavy buildup of dust, dirt, or insects will hinder the effectiveness of the cooling of the components. This could lead to a thermal shutdown or the premature failure of the affected trays.

When the front panels of the trays become dust covered, the top covers should be removed and any accumulated foreign material should be removed. A vacuum cleaner, utilizing a small, wand-type attachment, is an excellent way to suction out the dirt. Alcohol and other cleaning agents should not be used unless you are certain that the solvents will not damage components or the silk-screened markings on the trays and boards. Water-based cleaners can be used, but do not saturate the components. The fans and heatsinks should be cleaned of all dust or dirt to permit the free flow of air for cooling purposes.

It is recommended that the operating parameters of the transmitter be recorded from the meters on the trays and the system metering control panel at least once a month. It is suggested that this data be retained in a rugged folder or envelope for the life of the equipment. A sample format for a log sheet is provided in Appendix A. Photocopies of the log sheet should be made for future data entries.

1.5 Material Return Procedure

To insure the efficient handling of equipment or components that have been returned for repair, Axcera requests that each returned item be accompanied by a Material Return Authorization Number (MRA#).

An MRA# can be obtained from any Axcera field service engineer by calling the Axcera Field Service Department at (724) 873-8100. This procedure applies to all items sent to the Field Service Department regardless of whether the item was originally manufactured by Axcera.

Note: To prevent damage to the product during shipping, Axcera will supply a shipping container to the customer at no cost.

When equipment is sent to the field on loan, an MRA# is included with the unit. The MRA# is intended to be used for the return of the unit to Axcera. In addition, all shipping material should be retained for the return of the unit to Axcera. Replacement assemblies are also sent with an MRA# to allow for the proper routing of the exchanged hardware. Failure to close out this type of MRA# will normally result in the customer being invoiced for the value of the loaner item or the exchange assembly.

When shipping an item to Axcera, please include the MRA# on the packing list and on the Axcera-provided shipping container. The packing slip should also include contact information and a brief description of why the unit is being returned.

Please forward all MRA items to:

Axcera
103 Freedom Drive
P.O. Box 525
Lawrence, PA 15055-0525 USA

For more information concerning this procedure, call Axcera Field Service at **(724) 873-8100** or by fax at **(724) 873-8105**.

Axcera can also be contacted through e-mail at info@axcera.com and on the Web at www.axcera.com**.**

1.6 Warranty for Broadcast Products – Limited One-Year Warranty

Axcera warrants each new product that it has manufactured and sold against defects in material and workmanship under normal use and service for a period of one (1) year from the date of shipment from Axcera's plant, when operated in accordance with Axcera's operating instructions. This warranty shall not apply to tubes, fuses, batteries, or bulbs.

Warranties are valid only when and if (a) Axcera receives prompt written notice of breach within the period of warranty, (b) the defective product is properly packed and returned by the buyer (transportation and insurance prepaid), and (c) Axcera determines, in its sole judgment, that the product is defective and not subject to any misuse, neglect, improper installation, negligence, accident, or (unless authorized in writing by Axcera) repair or alteration. Axcera's exclusive liability for any personal and/or property damage (including direct, consequential, or incidental) caused by the breach of any or all warranties, shall be limited to the following: (a) repairing or replacing (in Axcera's sole discretion) any defective parts free of charge (F.O.B. Axcera's plant) and/or (b) crediting (in Axcera's sole discretion) all or a portion of the purchase price to the buyer.

Equipment furnished by Axcera, but not bearing its trade name, shall bear no warranties other than the special hours-of-use or other warranties extended by or enforceable against the manufacturer at the time of delivery to the buyer. **NO WARRANTIES, WHETHER STATUTORY, EXPRESSED, OR IMPLIED, AND NO WARRANTIES OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR FREEDOM FROM INFRINGEMENT, OR THE LIKE, OTHER THAN AS SPECIFIED IN PATENT LIABILITY ARTICLES, AND IN THIS ARTICLE, SHALL APPLY TO THE EQUIPMENT FURNISHED HEREUNDER.**

Chapter 2
System Description

The DT830A is a complete 300-watt (average) UHF solid-state digital television transmitter that operates at a nominal average output power of 300 watts.

2.1 System Overview

The DT830A consists of the assemblies and trays listed in Table 2-1.

Table 2-1. DT830A Major Assemblies and Trays

MAJOR ASSEMBLY NUMBER	TRAY/ASSEMBLY NAME
A4	UHF digital exciter tray
A6 and A7	UHF amplifier trays
A11	Coupler assembly
A2	AC distribution assembly
A19	8-VSB modulator tray
A12	Input and remote interface assembly
A8	UHF "tee"

2.1.1 (A19) 8-VSB Modulator Tray (1075164; Appendix C)

The 8-VSB modulator accepts an MPEG-2 transport stream input and outputs an 8 VSB IF signal centered at 44 MHz. To operate the modulator, the MPEG is connected to one of the three connectors on the rear panel, depending on the format of the MPEG data stream. The formats presently available are SMPTE 310M, Differential Serial TTL, and ECL. In addition, the modulator has an internal test source that can generate an MPEG data stream for test purposes. This signal is then modulated to a 44 MHz IF and fed to the output at J1.

2.1.2 (A4) UHF Digital Exciter Tray (1294-1111; Appendix C)

The output from the modulator connects to J6 on the rear of the UHF exciter tray, which is wired to J18 on the IF delay equalizer board, 44 MHz (1072090) and exits the board at J10. The processed digital IF signal is then wired to the ALC board (1265-1305) at J32. With digital IF input selected, the jumper W11 on J29 is connected between pins 2 and 3 on the ALC board; the digital IF is wired through the K3 and K4 relays to the rest of the ALC board. The LED DS5, digital IF modulator enable, should be lit. The ALC board has the capability to switch between two different IF inputs; in this case, only the digital IF input is used. The output of the ALC board (0 dBm peak) connects to (A11) the UHF upconverter board (1265-1310) in the upconverter section of the UHF digital exciter. The upconverter takes the LO and heterodynes it with the IF; the signal is then filtered to produce the RF on-channel output.

The (A15-A1) UHF generator board (1565-1109) is mounted in the UHF Generator Enclosure (1519-1144) for EMI and RFI protection. The board contains a VCXO circuit and additional circuitry to multiply the VCXO frequency by eight. The output is split and provides an input to the x8 multiplier circuitry as well as a sample for the PLL board.

The amplified eighth harmonic is then fed to the SMA output jack of the board at J3.

Typical output level of the signal is +16 dBm nominal.

The (A14-A1) 10-MHz reference generator board (1519-1126) is located in (A10) the 10-MHz reference kit (1286-1108). The board contains a high-stability crystal oscillator that provides a 10-MHz output that is used as reference frequency for the transmitter. The board is mounted within an enclosed assembly that helps to maintain the operating temperature of the oscillator board.

The (A13) PLL board (1286-1104) is part of the phase lock loop (PLL) circuit, which provides the automatic frequency control (AFC) voltage, that connects to the VCXO assembly, and maintains the accurate output frequency of the VCXO. The AFC is generated by comparing a sample of the 10-MHz reference to a sample of the VCXO frequency. The PLL board uses an external 10-MHz signal as the reference unless it is missing, then an internally generated 10-MHz signal is used.

A sample of the signal from the UHF generator board connects to SMA jack J9, the sample input on the board. The signal is amplified by U8 and coupled to U9, a divide by 20/21 IC. A sample of the signal at the output of U8 is connected to J10, the sample output jack on the board, which is typically connected to the front panel of the tray.

The selected 10-MHz reference connects to amplifier IC U1 whose output is split. A sample of the 10-MHz reference is cabled to jack J3, the 10-MHz output jack, which is connected to J5 on the rear of the tray.

If the 50 kHz from the 10-MHz reference and the 50-kHz from the UHF generator board become unlocked, the red Unlock LED, lights and the Lock LED, located on the LED display board, is extinguished.

2.1.3 UHF Digital RF Output Components

The RF output of the UHF exciter is fed to an (A5) splitter and then to two UHF amplifier trays that amplify the RF signal to approximately 300 watts. A forward power sample from the 4-way combiner board inside each tray is connected to the dual peak detector board that provides a peak-detected forward sample to the amplifier control board. This board supplies the sample to the front panel meter of the UHF amplifier tray.

Before exiting the UHF amplifier tray, the RF is fed through a circulator to protect the tray from high VSWR conditions. The reject port of the circulator provides a reject sample to the 4-way combiner board that supplies the reflected sample to the dual peak detector board. The reflected sample connects to the amplifier control board that provides the sample to the front panel meter of the tray. The output of (A6 and A7) the UHF amplifier trays are combined in a tee and then provide approximately 550 watts average power. The output is connected to a bandpass filter and then to the output coupler assembly. There is a coupler on the output of the bandpass filter that provides –40 dB forward and reflected samples to the system control panel. The bandpass filter is tuned to provide high out-of-band rejection of unwanted products. The 7/8" coupler assembly provides two forward power samples and one reflected power sample. The forward and reflected samples are cabled to the visual/aural metering boards in the UHF exciter. The forward and reflected samples are processed to provide detected power output samples to the transmitter control board. The transmitter control board connects the forward and reflected power output samples to the front panel meter for monitoring.

2.1.5 Transmitter Power Requirements

The transmitter needs an AC input of 220 VAC at 40 amps, or 80 amps for the upgradeable version, connected to it in order to operate. The 220 VAC input connects to terminal block (TB1) in the upper right rear of the cabinet and is part

of the (A2) AC distribution panel. The AC distribution panel contains four circuit breakers, six in the upgradeable version, which supply the AC to the rest of the transmitter.

The input AC from TB1 is connected to (CB1) the main AC circuit breaker (40 amps for DT830A and 80 amps for the upgradeable version) which distributes the 220 VAC to the terminal block (TB2). TB2 has three MOVs mounted to the terminal block: one is connected from each leg of the input AC to ground and the other one is connected across the two legs.

The input AC is wired from TB2 through three circuit breakers, CB2, CB3 and CB4, CB5 and CB6 are used in the upgradeable version, to the rest of the transmitter. CB2 (10 amps) supplies the AC voltage to the IEC outlet strip (A1) into which the UHF exciter and any other optional accessories are connected. CB3 (20 amps) supplies AC through J5 to (A6) the UHF amplifier tray. CB4 (20 amps) supplies AC through J6 to (A7) the UHF amplifier tray. In the upgradeable version, CB5 (20 amps) supplies AC through J6 to (A8) the UHF amplifier tray and CB6 (20 amps) supplies AC through J6 to (A9) UHF amplifier tray. .When the UHF exciter circuit breaker is switched on, +12 VDC is supplied to the UHF amplifier tray for the operation of the LED status indicators in the tray.

2.2 Control and Status

Control and status indications of the transmitter are provided by the meters and LED indicators on the front panel of the UHF exciter. The switches and LED indicators are part of the transmitter control board (1265-1311) which is mounted so that the switches and the LEDs can be operated or viewed from the front panel of the UHF exciter. Switch S1 is an Operate/Standby switch that controls the output of the transmitter by providing the Enables, when in Operate, needed to turn on the switching power supplies in the two or four UHF amplifier trays. In Operate, the green LED DS2 is on and in Standby the amber LED DS1 is on.

If the transmitter does not switch to Operate when S1 is switched to Operate, check that a dummy jumper plug, with a jumper between pins 23 and 24, is connected to jack J11 on the rear of the UHF exciter tray or with a jumper between pins 21 and 22 on jack J9 on (A17) the (optional) input and remote interface panel. This jumper provides the interlock needed for the transmitter to operate. If the interlock is present, the green LED DS5 on the transmitter control board should be lit. The front panel of the UHF exciter also has an LED for VSWR cutback (amber LED DS7).

2.2.1 (A19) 8-VSB Digital Modulator (1075164; Appendix C)

Table 2-2. Digital Modulator Display

DISPLAY	FUNCTION
LCD	Provides a three-line readout of the internal functions, external inputs, and status. See Chapter 4, Detailed Alignment Procedures, for a listing of display parameters.

The front panel has three pushbuttons for the control of the external and internal functions.

Table 2-3. Digital Modulator Control Pushbuttons

PUSHBUTTON	FUNCTION
Menu	Controls which menu is displayed on the LCD readout
Up Arrow (↑)	Moves the active line up one position on the LCD display
Down Arrow (↓)	Moves the active line down one position on the LCD display

There are four front panel status indicator LEDs.

Table 2-4. Digital Modulator Status Indicators

LED	FUNCTION
MPEG (Green)	Indicates the presence of an MPEG-2 signal; can be internal or external depending on menu selection
REF (Green)	Indicates the presence of an external 10 MHz reference source
PLL Locked (Green)	Indicates that the phase-locked loop circuit is functioning and locked
Power (Green)	Indicates that the DC power supply is functioning

Table 2-5. Digital Modulator Sample

SAMPLE	DESCRIPTION
Front panel sample	Sample of the 44 MHz IF output

2.2.2 (A4) UHF Digital Exciter Tray (1294-1111; Appendix C)

Table 2-6. UHF Exciter Tray Meters

METER	FUNCTION
Meter (A4-A18)	Reads power in terms of a percentage of the calibrated output power level on the upper scale. The voltage level is read on one of the bottom two scales. A full scale reading on the top scale is 0-120%, which is equivalent to the full-rated 300 watts or 1000 watts in the upgradeable version, average power. Also reads % Exciter Power, % Reflected Power, and ALC reading.
Switch (S3), meter	Selects the desired ALC voltage reading, % Exciter Power, % Output Power, and % Reflected Power
ALC (0-1 V)	Reads the ALC voltage level, .8 VDC, on the 0-10 scale

METER	FUNCTION
% Exciter (0-120)	Reads the % Exciter Output Power level needed to attain 100% output of the transmitter on the top scale
% Output power (0-120)	Reads the % Output Power of the transmitter on the top scale
% Reflected (0-120)	Reads the % Reflected Output Power, <5%, on the top scale

Table 2-7. UHF Exciter Tray Controls

SWITCH	FUNCTION
Transmitter (S1) Operate/Standby	The momentary switch (S1) applies a ground to K1, a latching relay on the transmitter control board. K1 will switch either to Operate or to Standby depending on which direction S1 is pushed. When switched to Operate, the low Enable commands are applied to the two or four 600-watt amplifier trays. These Enables will turn on the 600-watt amplifier trays. The opposite occurs when the transmitter is switched to Standby.
Mode Select (S2) Auto/Manual	The momentary contact switch (S2) applies a ground to K2, a latching relay on the transmitter control board. K2 will switch the transmitter to Automatic or Manual depending on which direction S2 is pushed. In Automatic, the Video Fault command from the ALC board will control the operation of the transmitter. The transmitter will switch to Standby, after a slight delay, if the input video is lost. It will quickly switch back to Operate when the video is restored. In Manual, the transmitter is controlled by the operator using the front panel Operate/Standby switch or by remote control.
Power adjust (R1)	Pot A20 sets the ALC level on the ALC board to set the output power of the transmitter.

Table 2-8. UHF Exciter Tray Fault Indicators

INDICATOR	FUNCTION
VSWR cutback (DS7 amber)	Indicates that the reflected power level of the transmitter has increased above 20% which will automatically cut back the output power level to 20%. The fault is generated on the transmitter control board in the UHF exciter tray.

Table 2-9. UHF Exciter Tray Samples

SAMPLE	DESCRIPTION
f(s)	A sample of the channel oscillator output, taken from the sample jack of the channel oscillator assembly
Exciter O/P	An output power sample of the exciter taken from the UHF upconverter board
Transmitter O/P	A forward power sample of the transmitter taken from the visual/aural metering board before the signal reaches the bandpass filter

2.2.3 (A6 and A7) UHF Amplifier Trays (1294-1112 Low Band, 1294-1113 Mid Band or 1294-1114 High Band ; Appendix C)

Table 2-10. UHF Amplifier Tray Meters

METER	FUNCTION
Meter (A6)	Reads power in terms of a percent of the calibrated power output value. A full-scale reading is 100%, which is equivalent to the full-rated 300 watts of average power. Also reads % Reflected Power, power supply, and AGC voltage levels.
Switch (S2), meter	Selects the desired % Power or the voltage reading
% Output pwr	Displays the % Output Power of the tray
% Refl (Reflected)	Displays the % Reflected Output Power of the tray, <10% on the top scale
Power supply	Reads the power supply voltage, +26.5 VDC, on middle scale
AGC voltage	Reads the AGC voltage level, +1 to +2 VDC, on the bottom scale

Table 2-11. UHF Amplifier Tray Status Indicators

INDICATOR	FUNCTION
Enable (DS4 green)	Indicates that an Enable, Operate, command is applied to the UHF amplifier tray from the UHF exciter tray
Overdrive (DS2 red)	Indicates that the level of the drive is too high. The protection circuit will limit the drive to the set threshold. The fault is generated on the amplifier control board.
VSWR cutback (DS1 red)	Indicates that the reflected power level of the tray has increased above 50%, which will automatically cut back the output power level to 50%. The fault is generated on the amplifier control board.
Overtemp (DS3 red)	Indicates that the temperature of (A5-A6-A3 and A5-A6-A4) one or both of the two thermal switches mounted on the heatsink assembly for the output amplifiers is above 175° F. When this fault occurs, the Enable to the switching power supply in the affected amplifier tray is removed immediately and it will shut down.
Input fault (DS5 red)	Indicates that the input RF level to the amplifier tray dropped below 0 dBm

Table 2-12. UHF Amplifier Tray Controls

CONTROL	FUNCTION
Phase (A10-R5)	Adjusts the phase of the RF output with a range of approximately 90°
Gain (A11-R6)	Adjusts the gain of RF output when the amplifier control board is in the AGC mode

Table 2-13. UHF Amplifier Tray Sample

SAMPLE	DESCRIPTION
Module O/P (0 dBm)	A sample of the combined output of the four dual-stage amplifier boards taken from the dual peak detector board

2.3 Remote Connections

The IF input to the transmitter connects to the rear of the UHF exciter or to (A12) the input and remote interface panel (Figure 2-1). Jacks J10 and J11 on the rear of the UHF exciter provide connections for the remote monitoring and operation of the transmitter. Jack J11 should have a dummy plug connected to it with a jumper between pins 23 and 24 that provides the interlock needed to operate the transmitter. If remote connections are made to the transmitter, they should be made through the plug in J10 or J11 in the positions noted on the interconnect drawing (1127833).

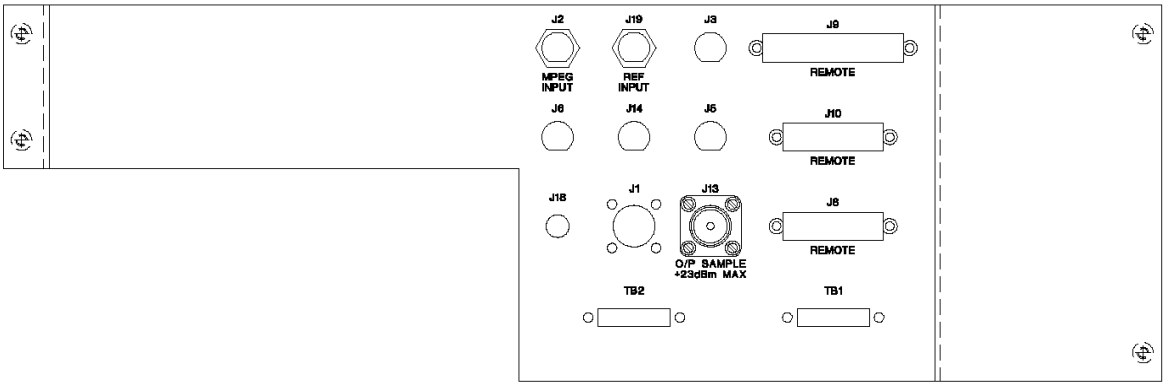

Figure 2-1. Remote Interface Panel

The remote connections shown in Tables 2-14 and 2-15 are made if (A12) the input and remote interface assembly is present in the system. The remote connections are made to jacks J9 and J10 on the assembly. Refer to the interconnect drawing (1127833) for the proper pin remote connections.

Table 2-14. Remote Interface Panel Connections

FUNCTION	REMOTE JACK/PIN NUMBER	INTERFACE TYPE
Transmitter Enable Interlock	J9-21	J9-21 and 22 must be jumpered for normal operation; (1176-1038) jumper jack is used.
Transmitter Enable Interlock Rtn	J9-22	
Remote Control Commands		
Transmitter Standby (Disable)	J9-9	Contact closure
Transmitter Standby/Operate Rtn	J9-10	
Transmitter Operate (Enable)	J9-11	Contact closure
Transmitter Manual	J9-15	Contact closure
Transmitter Auto/Manual Rtn	J9-16	
Transmitter Auto	J9-17	Contact closure
Power Level Raise (optional)	J9-27	Contact closure
Pwr Level Raise/Lower Rtn (optional)	J9-28	
Power Level Lower (optional)	J9-29	Contact closure
Remote Status Indications		
Transmitter Operate (Enable) Ind	J9-12	50 mA max current sink
Operate/Standby Ind. Return	J9-13	
Transmitter Standby (Disable) Ind	J9-14	50 mA max current sink
Transmitter Auto Indicator	J9-18	50 mA max current sink
Auto/Manual Indicator Return	J9-19	
Transmitter Manual Indicator	J9-20	50 mA max current sink
VSWR Cutback Indicator	J9-23	50 mA max current sink
VSWR Cutback Indicator Return	J9-24	

FUNCTION	REMOTE JACK/PIN NUMBER	INTERFACE TYPE
Remote Metering		
Digital Output Power	J9-1	1V full scale at 1kΩ source resistance
Digital Output Power Rtn	J9-2	
Reflected Power	J9-5	1V full scale at 1kΩ source resistance
Reflected Power Rtn	J9-6	
Exciter Output Power	J9-7	1V full scale at 1kΩ source resistance
Exciter Output Power Rtn	J9-8	

Table 2-15.UHF Amplifier Tray Remote Connections

FUNCTION	REMOTE JACK/PIN NUMBER	INTERFACE TYPE
Forward Output Power (A6) UHF Amp	J10-1	1V full scale at 1kΩ source resistance
Forward Output Power (A6) Rtn	J10-2	
Reflected O/P Power (A6) UHF Amp	J10-3	1V full scale at 1kΩ source resistance
Reflected O/P Power (A6) Rtn	J10-4	
Forward Output Power (A7) UHF Amp	J10-6	1V full scale at 1kΩ source resistance
Forward Output Power (A7) Rtn	J10-7	
Forward O/P Power (A8) UHF Amp	J10-10	1V full scale at 1kΩ source resistance
Forward Output Power (A8) UHF Amp Rtn	J10-11	
Reflected O/P Power (A8) UHF Amp	J10-12	1V full scale at 1kΩ source resistance
Reflected O/P Power (A8) Rtn	J10-13	
Forward O/P Power (A9) UHF Amp	J10-14	1V full scale at 1kΩ source resistance
Forward Output Power (A9) UHF Amp Rtn	J10-15	
Reflected O/P Power (A9) UHF Amp	J10-16	1V full scale at 1kΩ source resistance
Reflected O/P Power (A9) Rtn	J10-17	

Chapter 3
Installation and Setup Procedures

There are special considerations that need to be taken into account before the DT830A can be installed. For example, if the installation is completed during cool weather, a heat-related problem may not surface for many months, suddenly appearing during the heat of summer. This section provides planning information for the installation and set up of the transmitter.

3.1 Site Considerations

The transmitter requires an AC input line of 220 VAC with a rating of 40 amps and 80 amps for the upgradeable version Make sure that the proposed site for the transmitter has the voltage requirements that are needed.

The DT830A is designed and built to provide long life with a minimum of maintenance. The environment in which it is placed is important and certain precautions must be taken. The three greatest dangers to the transmitter are heat, dirt, and moisture. Heat is usually the greatest problem, followed by dirt, and then moisture. Over-temperature can cause heat-related problems such as thermal runaway and component failure. Each amplifier tray in the transmitter contains a thermal interlock protection circuit that will shut down that tray until the temperature drops to an acceptable level.

A suitable environment for the transmitter can enhance the overall performance and reliability of the transmitter and maximize revenues by minimizing down time. A properly designed facility will have an adequate supply of cool, clean air, free of airborne particulates of any kind, and without excessive humidity. An ideal environment will require temperature in the range of 40° F to 70° F throughout the year, reasonably low humidity, and a dust-free room. This is rarely attainable in the real world. However, the closer the environment is to this design, the greater the operating capacity of the transmitter.

The fans and blowers designed and built into the transmitter will remove the heat from within the trays, but additional means are required for removing this heat from the building. To achieve this, a few considerations should be taken into account. The first step is to determine the amount of heat to be removed. There are generally three sources of heat that must be considered. The first and most obvious is the heat from the 300-watt transmitter itself.

The second source of heat is other equipment in the same room. This number is calculated in the same way as the equation for BTUs. The third source of heat is equally obvious but not as simple to calculate. This is the heat coming through the walls, roof, and windows on a hot summer day. Unless the underside is exposed, the floor is usually not a problem. Determining this number is usually best left up to a qualified HVAC technician. There are far too many variables to even estimate this number without detailed drawings of the site showing all construction details. The sum of these three sources is the total amount of heat that must be removed. There may be other sources of heat, such as personnel, and all should be taken into account.

Now that the amount of heat that must be removed is known, the next step is to determine how to accomplish this. The options are air conditioning, ventilation, or a combination of the two. Air conditioning is always the preferred method and is the only way to create anything close to an ideal environment.

Ventilation will work quite well if the ambient air temperature is below 100° F, or about 38° C, and the humidity is be kept at a reasonable level. In addition, the air stream must be adequately filtered to ensure that no airborne particulate of any kind will be carried into the transmitter. The combination of air conditioning for summer and ventilation during the cooler months is acceptable when the proper cooling cannot be obtained through the use of ventilation alone and using air conditioning throughout the year is not feasible.

Caution: The operation of air conditioning and ventilation simultaneously is not recommended. This can cause condensation in transmitters. For tube type transmitters, this can be especially serious if the condensation forms in the tube cavity and creates damaging arcs.

The following precautions should be observed regarding air conditioning systems:

1. Air conditioners have an ARI nominal cooling capacity rating. In selecting an air conditioner, do not assume that this number can be equated to the requirements of the site. Make certain that the contractor uses the actual conditions that are to be maintained at the site in determining the size of the air conditioning unit. With the desired conditioned room temperature under 80° F, the unit must be derated, possibly by a substantial amount.

2. Do not have the air conditioner blowing directly onto the transmitter. Condensation may occur on, or worse in, the transmitter under certain conditions.

3. Do not isolate the front of the transmitter from the back with the thought of air conditioning only the front of the unit. Cooling air is drawn in at the front of all transmitters and in the front and back of others. Any attempt to isolate the front from the rear will adversely affect the cooling air flow.

4. Interlocking the transmitter with the air conditioner is recommended to keep the transmitter from operating without the necessary cooling.

5. The periodic cleaning of all filters is a must.

When using ventilation alone, the following general statements apply:

1. The blower, with attendant filters, should be on the inlet, thereby pressurizing the room and preventing the ingress of dirt.

2. The inlet and outlet vents should be on the same side of the building, preferably the leeward side. As a result, the pressure differential created by wind will be minimized. Only the outlet vent may be released through the roof.

3. The inlet and outlet vents should be screened with 1/8" hardware cloth (preferred) or galvanized hardware cloth (acceptable).

4. Cooling air should enter the room as low as practical but in no case higher than four feet above the floor. The inlet must be located where dirt, leaves, snow, etc., will not be carried in with the cooling air.

5. The exhaust should be located as high as possible. Some ducting is usually required to insure the complete flushing of heated air with no stagnant areas.

6. The filter area must be adequate to insure a maximum air velocity of 300 feet per minute through the

filter. This is not a conservative number but a never-exceed number. In a dusty or remote location, this number should be reduced to 150 CFM.

7. The inlet and outlet(s) must have automatic dampers that close any time the ventilation blower is off.

8. In those cases in which transmitters are regularly off for a portion of each day, a temperature-differential sensor that controls a small heater must be installed. This sensor will monitor inside and outside temperatures simultaneously. If the inside temperature falls to within 5° F of the outside temperature, the heater will come on. This will prevent condensation when the ventilation blower comes on and applies even in the summer.

9. A controlled-air bypass system must be installed to prevent the temperature in the room from falling below 40° F during transmitter operation.

10. The blower should have two speeds, which are thermostatically controlled, and interlocked with the transmitter.

11. The blower on high speed must be capable of moving the required volume of air into a half inch of water pressure at the required elevation. The free air delivery method must not be used.

12. Regular maintenance of the filters, if used, can not be overemphasized.

13. Tube transmitters should not rely on the internal blower to exhaust cooling air at elevations above 4000 feet. For external venting, the air vent on the cabinet top must be increased to an 8" diameter for a 1-kW transmitter and to 10" for 5-kW and 10-kW transmitters. An equivalent rectangular duct may be used but, in all cases, the outlet must be increased in area by 50% through the outlet screen.

14. It is recommended that a site plan be submitted to Axcera for comments before installation commences.

In calculating the blower requirements, filter size, and exhaust size, if the total load is known in watts, 2000 CFM into 1/2" of water will be required for each 5000 watts. If the load is known in BTUs, 2000 CFM into 1/2" of water will be required for each 17,000 BTUs. The inlet filter must be a minimum of seven square feet, larger for dusty and remote locations, for each 5000 watts or 17,000 BTUs. The exhaust must be at least four square feet at the exhaust screen for each 5000 watts or 17,000 BTUs.

The information presented in this section is intended to serve only as a general guide and may need to be modified for unusually severe conditions. A combination of air conditioning and ventilation should not be difficult to design (see Figure 3-1). System interlocking and thermostat settings should be reviewed with Axcera. As with any equipment installation, it is always good practice to consult the manufacturer when questions arise. Axcera can be contacted at (724) 873-8100.

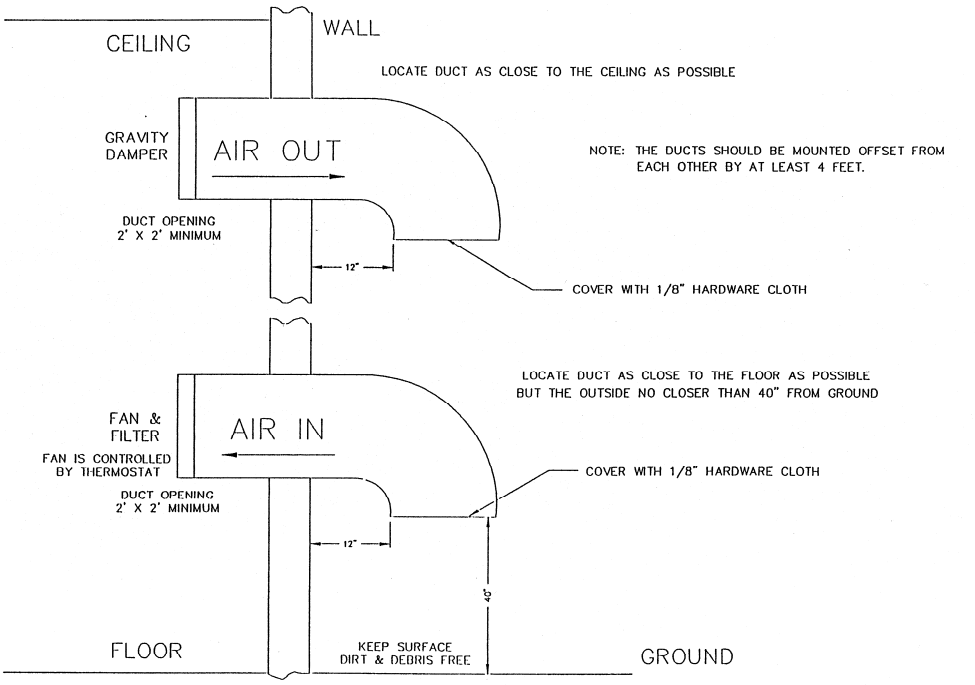

Figure 3-1. 1 kW Minimum Ventilation Configuration

3.2 Unpacking the Cabinets

Note: Air conditioning and any related heat exhaust ducts should be in place before continuing with the installation of the transmitter.

Thoroughly inspect the cabinet and all other materials upon their arrival. Axcera certifies that upon leaving our facility the equipment was undamaged and in proper working order. The shipping containers should be inspected for obvious damage that is indicative of rough handling. Check for dents and scratches or broken switches, meters, or connectors. Any claims against in-transit damage should be directed to the carrier. Inform Axcera as to the extent of any damage as soon as possible.

Remove the cabinet with trays, UHF tee assembly, bandpass filter, digital modulator, (optional) trap filter, directional coupler, and the installation material from the crates and boxes. Remove the straps that hold the cabinet to the shipping skid and slide the cabinet from the skid. Remove the plastic wrap and foam protection from around the cabinet. Do not remove any labeling or tags from any cables or connectors; these are identification markers that make assembly of the transmitter much easier.

Remove the four L-brackets, mounted on the front panel rails, which held the trays in place during shipment. The trays are mounted in the cabinet using Chassis Trak cabinet slides. The tray slides are on the top and bottom of the UHF amplifier trays and on the sides of the UHF exciter and digital modulator trays. Inspect the trays for any loose hardware or connectors, tightening where needed. Open the rear door and inspect the interior for packing material, carefully removing any that is found. Slowly slide each tray in and out to verify that they do not rub against each other and have no restrictions to free movement.

Caution: Each UHF amplifier tray has a hardline coaxial cable connected to the bottom panel. The tray will not slide out unless this cable is first removed. To pull the tray out for test purposes, use the extender coaxial cable included in the installation material kit for connections from the tray to the output cable.

Adjustments to the position of the trays may be necessary. To accomplish this, loosen the cabinet slide mounting bolts that hold the front of the slide to the mounting frame of the cabinet and move the tray up or down as needed to correct for the rubbing.

The air intake to the transmitter is intended for room air only. The cabinet should be positioned with consideration given to adequate air intake and exhaust, the opening of the rear door, access to the trays (including sliding them out for testing), the main AC hookup, and the installation of the output transmission line. The cabinet should be grounded using copper strapping material and should also be permanently mounted to the floor of the site using the holes in the bottom of the cabinet.

3.3 Installation of the Cabinets and Trays

Once the cabinet is in place and the trays are checked for damage, the main AC hookup is ready to be made.

Caution: Before connecting the 230 VAC, make certain that all of the circuit breakers associated with the transmitter are switched off.

The main AC input circuit to the transmitter should be a 40-amp, 80-amp for upgradeable version, 230-VAC line, using AWG 8 wire inside of a 1-1/4" conduit. The 230-VAC input connections (terminals 1 and 2 [230 VAC] and terminal 3 [chassis ground]) are made to terminal block TB1, which is part of (A2) the AC distribution panel near the rear door of the transmitter. Line 2 is the neutral for international systems using 220 VAC hot and neutral.

The RF output at J2 of (A11) the coupler assembly, which is 7/8" rigid coax, should connect to the transmission line that is connected to the antenna system.

The MPEG digital source input connects to J3, ECL, or TTL, depending on the configuration, at the rear panel of (A19) the modulator or J2 on (A12) the remote interface panel. Remote functions connect to the rear of (A4) the UHF exciter or to (A12) the input and remote interface panel mounted on the rear top of the transmitter. A plug is connected to jack J11 with pins 23 and 24 jumpered together on the UHF exciter or to jack J9 with pins 21 and 22 jumpered together on the (optional) remote interface panel. These are 37-pin, "D"-connectors that provide the interlock for the transmitter. Jacks J10 and J11 on the UHF exciter, and jacks J9 and J10 on the (optional) remote interface panel, are used to connect the remote control functions to the transmitter.

This completes the unpacking and installation procedures for the DT830A Digital UHF Transmitter. Refer to the setup and operation procedures that follow before applying power to the transmitter.

3.4 Setup and Operation Procedures

The transmitter should initially be turned on with the RF output of the bandpass filter/coupler assembly terminated into a dummy load of at least 500 watts. If a load is not available, check that the output of the coupler assembly is connected to the antenna.

Switch on the main AC, UHF exciter, digital modulator, and the amplifier #1 and #2, amplifier #3 and #4 are used after upgrade, circuit breakers located on the AC distribution panel facing the rear

of the cabinet and mounted behind the rear door. On the UHF exciter tray, switch the Operate/Standby switch to Standby.

Move the Operate/Standby switch, located on the UHF exciter tray, to Operate. Observe the power supply reading, +26.5 VDC, on the front panel of the UHF amplifier trays.

Note: If the transmitter does not switch to Operate when the Operate/Standby switch is switched to Operate, check that an external interlock plug, with a jumper wired from pins 23 to 24, is connected to jack J11 on the rear of the UHF exciter. Or, if (A17) the optional input and remote interface assembly is present in the system, the external interlock plug, with a jumper wired from pins 21 to 22, should be connected to jack J9 on the assembly.

Observe the front panel meter reading in the % Output Power position on the UHF exciter tray; after allowing several minutes of warm-up time, it should read 100%. If necessary, readjust the screwdriver adjust power pot on the front panel of the UHF exciter for 100%. As you are checking the power level, check the meter reading in the % Reflected Power position. If the % Reflected Power is very high (above 10%), a problem with the output coaxial lines is present and needs to be checked. A center bullet missing from the 7/8" rigid coax lines or loose bolts on the connections can cause this problem. Return the Operate/ Standby switch to Standby.

The gain and phase controls on the front panel of the UHF amplifier tray were adjusted at the factory to attain 100% output of the transmitter and should not need to be readjusted. Refer to the Test Data Sheet for the transmitter to compare the final reading from the factory with the reading on the tray after the setup. They should be very similar. If a reading is off by a significant amount, refer to the phasing and power adjustment procedures for the UHF amplifier tray in Chapter 5, Detailed Alignment Procedures, of this manual before trying to make any adjustments.

If a dummy load is connected to the transmitter, switch the transmitter to Standby and switch off the main AC circuit breaker. Remove the dummy load and make all of the connections needed to connect the transmitter to the antenna. Switch the main AC circuit breaker on and the Operate/Standby switch to operate. Adjust the output power screwdriver pot to attain 100% output.

If the transmitter is already connected to the antenna, check that the output is 100%. If necessary, adjust the power screwdriver pot.

If a problem occurred during the setup and operation procedures, refer to Chapter 5, Detailed Alignment Procedures, of this manual for more information.

This completes the setup and operation procedures for the DT830A transmitter. The transmitter can now be operated normally.

Chapter 4
Circuit Descriptions

4.1 (A4) UHF Exciter Tray (1294-1111; Appendix C)

4.1.1 (A12 and A18) UHF Filter (1007-1101; Appendix D)

The UHF filter is a tunable two-section cavity filter that is typically tuned for a bandwidth of 5 MHz and has a loss of -1 dB through the filter.

4.1.2 (A15-A1) UHF Generator Board (1565-1109; Appendix D)

The UHF generator board is mounted in the UHF Generator Enclosure (1519-1144) for EMI and RFI protection. The board contains a VCXO circuit and additional circuitry to multiply the VCXO frequency by eight. The VCXO produces an output of ≈ 67 MHz to 132 MHz, depending on the desired channel frequency. Course adjustment to the frequency is made by C11, while fine adjustments are accomplished by the AFC voltage from (A11) the PLL board (1286-1104). The VCXO frequency level is adjusted by C6, L2, and L4. The output is split and provides an input to the x8 multiplier circuitry as well as a sample for the PLL board.

The x8 circuitry consists of three identical x2 broadband frequency doublers. The input signal at the fundamental frequency is fed through a 6-dB pad consisting of R21, R24, and R25 to amplifier U3. The output of the amplifier stage is directed through a bandpass filter consisting of L8 and C32, which is tuned to the fundamental frequency (67 MHz to 132 MHz). The voltage measured at TP1 is typically +.6 VDC. The first doubler stage consists of Z1 with bandpass filter L9 and C34 tuned to the second harmonic (134 MHz to 264 MHz). The harmonic is amplified by U4 and again bandpass filtered at the second harmonic by C38 and L11 (134 MHz to 264 MHz). The voltage measured at TP2 is typically +1.2 VDC. The next doubler stage consists of Z2 with bandpass filter C40 and L12 tuned to the fourth harmonic of the fundamental frequency (268 MHz to 528 MHz). The fourth harmonic is then amplified by U5 and fed through another bandpass filter tuned to the fourth harmonic consisting of L14 and C44 (268 MHz to 528 MHz). The voltage measured at TP3 is typically +2.0 VDC. The final doubler stage consists of Z3 with bandpass filter C46 and L15 tuned to the eighth harmonic of the fundamental frequency (536 MHz to 1056 MHz). The signal is amplified by U6 and U7 to a typical value of from +2 to +4 VDC as measured at TP4. The amplified eighth harmonic is then fed to the SMA output jack of the board at J3.

Typical output level of the signal is +16 dBm nominal.

The +12 VDC for the board enters through jack J4-3 and is filtered by L22 and C54-C58 before being distributed to the circuits on the board.

4.1.3 (A14-A1) 10-MHz Reference Generator Board (1519-1126; Appendix D)

The 10-MHz reference generator board is located in (A10) the 10-MHz reference kit (1286-1108). The board contains a high-stability crystal oscillator that provides a 10-MHz output that is used as reference frequency for the transmitter. The board is mounted within an enclosed assembly that helps to maintain the operating temperature of the oscillator board.

The oscillator operates at 10 MHz. Transistor Q1 is the oscillating transistor with the frequency of oscillation set by the crystal Y1. L2, C2, and C3 have second-order effects on the frequency, with C2 and C3 used to pull the oscillator

exactly on frequency. Capacitors C4 and C5 provide the positive feedback necessary for oscillation.

The output of the oscillator is buffered by Q2 and Q3. L4 and C12 form a 40-MHz bandpass filter. The 40-MHz signal passes through a digital divider IC U4, which divides the signal down to 10 MHz. Transistor Q5 provides a buffered, 10-MHz output at jack J1.

The crystal is heated in an enclosed crystal oven (HR-1) that is internally set at 60° C. The oscillator board is heated by a separate oven that is set at 50° C. U1 is a temperature sensor/controller IC that monitors the temperature of the oscillator assembly and controls the operation of Q4 and U2. The operating temperature of the assembly is set by adjusting R15. If the temperature of the assembly falls below 50° C, U1 will bias Q4 on, which in turn increases the amount of current flow through U2. The flange of U2 is thermally connected to the heatsink of the assembly. The temperature of the heatsink will increase as the current through U2 increases. As a result, U2 will dissipate more power in the form of heat, and the temperature of the assembly will increase. If the assembly temperature rises above 50° C, the opposite action will occur, thus lowering the temperature of the assembly.

The +12 VDC enters the board at J2 and is filtered by L1 and C1 before it is applied to the remaining circuits on the board.

4.1.4 (A13) PLL Board (1286-1104; Appendix D)

The PLL board is part of the phase lock loop (PLL) circuit, which provides the automatic frequency control (AFC) voltage, that connects to the VCXO assembly, and maintains the accurate output frequency of the VCXO. The AFC is generated by comparing a sample of the 10-MHz reference to a sample of the VCXO frequency. The PLL board uses an external 10-MHz signal as the reference unless it is missing, then an internally generated 10-MHz signal is used. The two 10-MHz reference signals are connected to the K1 relay and the selected reference to U1. The switching between the two references is accomplished by the K1 relay which, when energized, applies the external 10-MHz reference to U1, as long as an externally generated 10-MHz reference signal is present and an interlock is connected to J8, pin 1.

If the interlock is removed or the external 10-MHz reference is missing, the relay is de-energized and the internal 10-MHz reference is applied through the relay to U1. The internally generated 10-MHz reference connects from J7 to pins 3 and 6 of relay K1. The externally generated 10-MHz reference connects from J2 to pins 2 and 5 of relay K1. The unused 10-MHz reference is connected through the relay to R10, a 51-Ω load.

With the relay energized, the internally generated 10-MHz reference from J7 connects through the closed contact of the relay from pin 6 to pin 7 to R10, the 51-Ω load. The externally generated 10-MHz from jack J2 connects through the closed contact of the relay from pin 2 to pin 1 to amplifier U1. With the relay not energized, the internally generated 10-MHz reference from J7 connects through the closed contact of the relay from pin 3 to pin 1 to amplifier U1. The externally generated 10-MHz from jack J2 connects through the closed contact of the relay from pin 5 to pin 7 to R10, the 51-Ω load.

External 10-MHz Reference Present Circuitry

The external 10-MHz reference signal enters the board at J2 and is filtered by C4, L2, and C5 before it is connected to the K1 relay. A sample of the 10 MHz is rectified by CR3 and connected to U3A. If the sample level of the external 10 MHz

is above the reference set by R13 and R14, which is connected to pin 2 of U3A, the output of U3A stays high. The high connects to gates of Q4 and Q9, which are biased on and cause their drains to go low. The low from the drain of Q9 is wired to J8, pin 6, for connection to a remote external 10-MHz present indicator. The low from the drain of Q4 connects to the green LED DS2 which lights to indicate that an external 10-MHz reference is present. The low from the drain of Q4 also connects to the gate of Q5, biasing it off and causing its drain to go high.

This high reverse biases CR4 and allows a high to be applied to the gates of Q6, Q8, and Q3, if an interlock, low, is present at J8, pin 1. The high to the gate of Q6 biases it on and causing its drain to go low; the low is connected to the green LED DS3, which lights, indicating that an external 10-MHz reference is selected. The high to the gate of Q8 biases it on and applies a low to J8, pin 7, for connection to a remote reference select indicator. The high that is applied to the gate of Q3 biases it on and causes its drain to go low, which energizes the K1 relay and applies the external 10-MHz reference signal to U1 for use in the PLL circuits.

Internal 10-MHz Reference Circuitry

The internally generated 10-MHz reference signal connects from jack J7 on the board to pins 3 and 6 of relay K1. If the external 10-MHz reference is missing, or the interlock is not present at J8, pin 1, the relay is de-energized. The internally generated 10-MHz reference connects through the closed contact of the relay from pin 3 to pin 1 to amplifier U1. The externally generated 10-MHz signal from jack J2 connects through the closed contact of the relay from pin 5 to pin 7 to R10, the 51-Ω load.

Sample Input Circuitry

A sample of the signal from the UHF generator board connects to SMA jack J9, the sample input on the board. The signal is amplified by U8 and coupled to U9, a divide by 20/21 IC. A sample of the output of U8 is connected to J10, the sample output jack on the board, which is typically connected to the front panel of the tray.

Comparator Phase Lock Loop Circuit

The selected 10-MHz reference connects to amplifier IC U1 whose output is split by the circuit consisting of L3, L4, and R8. A sample of the 10-MHz reference is cabled to jack J3, the 10-MHz output jack, which is connected to J5 on the rear of the tray. The 10-MHz reference connects to IC U4, a divider PLL chip. The divided-down sample of the 10-MHz reference, which is measurable at TP2, connects from pin 10 of U4 to pin 27 of U5.

The divided-down sample from U9 is connected to U5, a divider comparator IC, which divides this signal to a 50-kHz reference. The 50-kHz references are compared in the U5 IC to a 50-kHz sample of the 10-MHz signal that is generated from an external 10-MHz reference input or internally from a 10-MHz reference kit. The three DIP switches, SW1, SW2, and SW3, are set up to divide down the reference sample input generated by the VCXO to 50 kHz. The reference is then compared to the 50-kHz sample from the 10-MHz input in the U5 IC.

The output of U5 at pins 7 and 8 connect to U6A, a differential comparator, whose output is the difference between the two 50-kHz references which is the AFC voltage. The AFC voltage is amplified by U6B and connected to jack J4. W1 on J4 must be in the AFC auto position, between pins 1 and 2, for the PLL circuit to operate. With jumper W1 between pins 2 and 3 on J6, fixed bias, the AFC

bias is set by R12. The AFC output at J6 on the board connects to the VCXO on the UHF generator board. The PLL circuit will maintain the very accurate VCXO output because any change in frequency will be corrected by the AFC error voltage.

Lock Detector Circuit

IC chip U2 contains an internal lock detector that indicates the status of the PLL circuit. When U2 is in a locked state, pin 3 and pin 7 go low; the low is applied to Q1, which is biased off. With Q1 off, pin 1 of J1 goes high and is connected to the Lock LED on the LED display board that lights. The low applied to DS1, the Red Unlock LED, causes it not to light.

If the 50 kHz from the 10-MHz reference and the 50-kHz from the UHF generator board become unlocked, out of the capture range of the PLL, pins 2 and 6 of U2 go to a logic low; this causes U2, pins 3 and 7, to go high. The high connects to DS1, the red Unlock LED, which lights, and to Q1 and Q2, which are biased on. When Q2 is biased on, it connects a low remote unlock to jack J1, pin 4. With Q1 biased On, the drain goes low and removes the high to pin 1 of J1, which is connected to the Lock LED, on the LED display board, which is extinguished.

Voltage Requirements

The ±12 VDC needed for the operation of the board enters through jack J11. The +12 VDC is connected to J11-3, which is filtered and isolated by L6 and C38 before it is connected to the rest of the board. The -12 VDC is connected to J11-5, which is filtered and isolated by L7 and C39 before it is connected to the rest of the board.

The +12 VDC is connected to U7, a 5-volt regulator IC, that provides the +5 VDC operating voltage to the U2, U4, U5, and U9 ICs.

4.1.5 (A1) Power Entry Module Assembly (1227-1206; Appendix D)

The power entry module assembly provides overvoltage and surge protection for the input AC lines that connect to the exciter tray. The AC input plug connects to J14; J14 is part of the power entry module on the rear panel of the exciter tray.

The module assembly contains two 130-VAC varistors and one 250-VAC varistor that connect across the AC lines and to ground. The module also contains two 4-amp fuses, one in each input line for overcurrent protection.

4.1.6 (A9) IF Phase Corrector Board (1227-1250; Appendix D)

The IF phase corrector board has adjustments that pre-correct for any IF phase modulation distortion that might occur in output amplifier devices such as Klystron power tubes and solid-state amplifiers. Two separate, adjustable IF paths are on the board: a quadrature IF path and an in-phase IF path. The quadrature IF is 90° out of phase and much larger in amplitude than the in-phase IF. When these paths are combined in Z1, they provide the required adjustable phase correction to the IF signal.

The IF input signal enters at J1 and is capacitively coupled to U1. U1 amplifies the IF before it is connected to Z1, a splitter, to create two, equal IF outputs. IF output #1 is connected to J2 and IF output #2 is connected to J3. IF output #1 at J2 is jumpered through coaxial cable W4 to jack J6, the quadrature input, on the board. IF output #2 at J3 is jumpered through coaxial cable W5 to jack J7, the in-phase input, on the board.

4.1.6.1 Phase Corrector Circuit

The phase corrector circuit adjusts for any amplitude nonlinearities of the IF signal. It is designed to work at IF and

has three stages of correction. Each stage has a variable threshold and magnitude control. The threshold control determines the point where the gain is changed and the magnitude control determines the gain change once the breakpoint is reached. The second stage has a jumper that determines the direction of the correction so that the gain can be made to increase either above or below the threshold and either black or white stretch can be accomplished in stage two.

When the phase corrector circuit is operating, the IF signal from J6 is applied to transformer T1, which doubles the voltage swing using a 1:4 impedance transformation. Resistors R8, R61, R9, and R48 form an L-pad that attenuates the signal. This attenuation is adjusted by adding R7, a variable resistor, in parallel with the L-pad. R7 is only in parallel when the signal reaches a level large enough to bias on CR1 and CR2 and allow current to flow through R7. When R7 is put in parallel with the L-pad, the attenuation through the L-pad is lowered, causing black stretch.

Two reference voltages are utilized in the corrector stages and both are derived from the +12 VDC line. Zener diode VR1, with R46 as a dropping resistor, provides +6.8 VDC from the +12 VDC line. Diodes CR11 and CR12 provide a .9-VDC reference that temperature compensates the corrector circuits from the affects of the two diodes in each corrector stage. The threshold for the first corrector stage is set by controlling where CR1 and CR2 turn on. This is accomplished by adjusting R3 and forming a voltage divider from +6.8 VDC to ground. The voltage at the wiper of R3 is buffered by U9C, a unity-gain amplifier, and applied to CR1. The .9-VDC reference is connected to U9D, a unity-gain amplifier, whose output is wired to CR2. These two references are connected to diodes CR1 and CR2 through chokes L2 and L3. The two chokes form a high impedance for RF that isolates the op-amps from the RF.

The adjusted signal is next applied to amplifier U2, which compensates for the loss through the L-pad. U2 is powered through L4 and R10 from the +12 VDC line. After the signal is amplified by U2, it is applied to the second corrector stage through T2 and then to a third corrector stage through T3. The two other corrector stages operate the same as the first; they are independent and do not interact with each other.

When jumper W1 on J8 is connected from center to ground, R15 is put in series with ground. In this configuration, black stretch (white compression) is applied to the IF signal by controlling the attenuation through the path. When W1 is connected from the center pin to the end that connects to T2, R15 is put in parallel with the L-pad. In this configuration, black compression (white stretch) is applied to the IF signal by controlling the attenuation through the path.

The phase correctors can be bypassed by moving jumper W2 on J9 to the Disable position. This will move all of the threshold points past sync tip so that they will have no affect. R68 can be adjusted and set for the required correction range. TP2 is a test point that gives the operator a place to measure the level of the quadrature IF signal that is connected to pin 6 on combiner Z2.

4.1.6.2 Amplitude Corrector Circuit

The amplitude corrector circuit adjusts for any amplitude nonlinearities of the IF signal using one stage of correction. The stage has a variable threshold control, R31, and a variable magnitude control, R35. The threshold control determines the point where the gain is changed and the magnitude control determines the amount of gain change once the breakpoint is reached.

Two reference voltages are needed for the operation of the corrector circuit. Zener diode VR1 with R46 provides +6.8

VDC and diodes CR11 and CR12 provide a .9-VDC reference voltage that is used to temperature compensate for the two diodes in the corrector stage.

When the amplitude corrector circuit is operating, the IF signal from J7 is applied to transformer T4, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R36, R55, R56, and R37 form an L-pad that lowers the level of the signal. The amount that the level is lowered can be adjusted by adding more or less resistance, using R35, in parallel with the L-pad resistors. R35 is only in parallel when the signal reaches a level large enough to turn on diodes CR8 and CR9. When the diodes turn on, current flows through R35, putting it in parallel with the L-pad. When R35 is in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch, which is the amount of stretch determined by the adjustment of R35.

The signal is next applied to amplifier U5 to compensate for the loss in level through the L-pad. The breakpoint, cut-in, for the corrector stage is set by controlling where CR8 and CR9 turn on. This is accomplished by adjusting cut-in resistor R31, which forms a voltage divider from +6.8 VDC to ground. The voltage at the wiper arm of R31 is buffered by unity-gain amplifier U8B. This voltage is then applied to R34, through L11, and to diode CR9. The .9-VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U8A. C36 keeps the reference from sagging during the vertical interval. The reference voltage is then connected to diode CR8 through choke L12. Chokes L11 and L12 form a high impedance for RF that isolates the op-amp ICs from the IF.

After the signal is amplified by U5, it is applied to a second stage through T5. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R39, R57, R58, and R40 form an L-pad that lowers the level of the signal. The signal is applied to amplifier U6 to compensate for the loss in level through the L-pad. After the signal is amplified by U6, it is applied to a third stage through T6. The transformer doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R42, R59, R60, and R43 form an L-pad that lowers the level of the signal. The signal is applied to amplifier U7 to compensate for the loss in level through the L-pad.

TP1 is a test point that gives the operator a place to measure the level of the in-phase IF signal that is connected to mixer stage Z2. The amplitude corrector can be disabled by moving jumper W3 on J10 to the Disable position; this will move the breakpoint past sync tip so that it will have no affect on the signal.

4.1.6.3 Output Circuit

The phase-corrected signal from pin 1 on combiner Z2 exits the board at IF output jack J4 after passing through a matching network consisting of six resistors.

4.1.7 (A8) ALC Board (1265-1305; Appendix D)

The ALC board provides for automatic level control (ALC) and amplitude linearity correction of the IF signal. The ALC adjusts the level of the IF signal through the ALC board which, in turn, controls the output power of the transmitter.

The visual + aural IF input (0 dBm) signal from the modulator enters the board at modulator IF input jack J32 and, if the (optional) receiver tray is present, the visual + aural IF input (0 dBm) from the receiver tray connects to J1, the receiver IF input jack. The modulator IF input connects to relay K3 and the receiver IF input connects to relay K4. The two relays are controlled by the Modulator Select command that is connected to J30 on the board. Modulator

select enable/disable jumper W11 on J29 controls whether the Modulator Select command at J30 controls the operation of the relays. With jumper W11 on J29, pins 1 and 2, the Modulator Select command at J30 controls the operation of the relays but, with jumper W11 on J29, pins 2 and 3, the modulator is selected all of the time.

4.1.7.1 Modulator Selected

With the modulator selected, J11-10 and J11-28 on the rear of the UHF exciter tray are connected together; this makes J30 low and causes relays K3 and K4 to de-energize. When K4 is de-energized, it connects the receiver IF input at J1, if present, to 50 watts. When K3 is de-energized, it connects to the modulator IF input at J32 and from there to the rest of the board. At this point, the Modulator Enable LED DS5 will be lit.

4.1.7.2 Receiver Selected

With the receiver selected, J11-10 and J11-28, which are on the rear of the UHF exciter tray and connect to J30 on the board, are not connected together; relays K3 and K4 are energized. When K4 is energized, it connects the receiver IF input at J1, if present, to the rest of the board. When K3 is energized, it connects to the modulator IF input at J32 to 50 watts. At this point, the Modulator Enable LED DS5 will not be lit.

4.1.7.3 Main IF Signal Path (Part 1 of 3)

The selected visual + aural IF input (0 dBm) signal is split, with one half entering a bandpass filter consisting of L3, L4, C4, L5, and L6. This bandpass filter, which can be tuned with C4, is substantially broader than the IF signal bandwidth. It is used to slightly steer the frequency response of the IF and make up for any small discrepancies in the frequency response in the stages that precede this point. The filter also serves the additional function of rejecting unwanted frequencies that may occur if the tray cover is off and the tray is in a high RF environment. This allows for the servicing of this transmitter with the tray cover off in spite of being in the presence of other RF signals. The filtered IF signal is fed through a pi-type matching pad, consisting of R2, R3, and R4, to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3.

4.1.7.4 Input Level Detector Circuit

The other part of the split IF input is connected through L2 and C44 to U7, an IC amplifier, which is the input to the input level detector circuit. The amplified IF is fed to T4, a step-up transformer, that feeds diode detector CR14. The positive-going detected signal is then low-pass filtered by C49, L18, and C50; this allows only the video with positive sync to be applied through emitter follower Q1. The signal is then connected to detector CR15, which produces a peak-sync voltage that is applied to op-amp U9A. There is a test point at TP3 that provides a voltage reference check of the input level. The detector serves the dual function of providing a reference that determines the input IF signal level to the board and acting as an input threshold detector.

The input threshold detector prevents the automatic level control from reducing the attenuation of the pin-diode attenuator to minimum (maximum signal) if the IF input to the board is removed. The ALC, video loss cutback, and the threshold detector circuits will only operate when jumper W3 on jack J6 is in the Auto position, between pins 1 and 2. Without the threshold detector, with the pin-diode attenuator at minimum when the signal is restored, the stages following this board will be overdriven.

On the threshold detector, the minimum IF input level at TP3 is fed through detector CR15 to op-amp IC U9A, pin 2. The reference voltage for the op-amp is determined by the voltage divider consisting of R50 and R51 off of the +12

VDC line. When the detected input signal level at U9A, pin 2, falls below this reference threshold, approximately 10 dB below the normal input level, the output of U9A, pin 1, goes to the +12 VDC rail. This high is connected to the base of Q2, which is forward biased, and creates a current path from the -12 VDC line, through the red Input Level Fault Indicator LED DS1 (which lights), resistor R54, and transistor Q2 to +12 VDC. The high from U9A also connects through diode CR16 to U9B, pin 5, whose output at pin 7 goes high. The high connects through range adjust pot R74 to J20, which connects to the front panel-mounted power adjust pot. This high connects to U10A, pin 2, which causes it to go low at output U10A, pin 1. The low is applied through jumper W3 on J6 to the pin-diode attenuator circuit that cuts back the IF level and also cuts back the output power level to 0. When the input signal level increases above the threshold level, the output power will rise as the input level increases until normal output power is reached.

The video input level at TP3 is also fed to a sync-separator circuit, consisting of IC U8, CR17, Q3, and associated components, and then to a comparator circuit made up of U9C and U9D. The reference voltage for the comparators are determined by the voltage divider, consisting of R129, R64, R65, R66, and R130, off of the -12 VDC line. When the input signal level to the detector at TP3 falls below this reference threshold, which acts as a loss of sync detector circuit, the output of U9C and U9D goes towards the -12 VDC rail, which is split, with one part biasing on the transistor Q5. A current path is then established from the +12 VDC line through Q5, resistors R69 and R137, and the red Video Loss Indicator LED DS3, which lights. When Q5 is on, it applies a high to the gates of Q6 and Q7, causing them to conduct; this applies video loss fault pull-down outputs to J18, pins 5 and 2.

The other low output of U9C and U9D is connected through CR20 to jack J5. Jumper W2 on J5, in the cutback enable position between pins 2 and 3, connects the low to the base of Q4, which is forward biased. If jumper W2 is in the Disable position, between pins 1 and 2, the automatic cutback will not operate. With Q4 biased on, a level determined by the setting of cutback level pot R71, which is set at the factory to cut back the output to approximately 25%, is applied to U9B, pin 5. The output of U9B, pin 7, goes low and is applied through the power adjust pot to U10A, pin 2, whose output goes low. This low is applied to the pin-diode attenuator, which will cut back the level of the output to approximately 25%.

4.1.7.5 Pin-Diode Attenuator Circuit

The input IF signal is fed to the pin-diode attenuator circuit, consisting of CR1 to CR3. Each of the pin diodes contain a wide, intrinsic region, which makes the diodes function as voltage-variable resistors at this intermediate frequency. The value of the resistance is controlled by the DC bias supplied to the diode. The pin diodes are configured in a pi-type attenuator configuration where CR1 is the first shunt element, CR3 is the series element, and CR2 is the second shunt element. The control voltage, which can be measured at TP1, originates either from the ALC circuit, when jumper W3 on J6 is in the ALC Auto position between pins 1 and 2, or from pot R87 when the jumper is in the Manual Gain position.

In the pin-diode attenuator circuit, a current path exists from J6 through R6 and then through the diodes of the pin attenuator. Changing the amount of current through the diodes by forward biasing them changes the IF output level of the board. There are two extremes of attenuation ranges for the pin-diode attenuators. In the minimum attenuation case, the voltage is measured as TP1 approaches the +12 VDC line. There is a current path created through R6, through

series diode CR3, and finally through R9 to ground. This path forward biases CR3 and causes it to act as a relatively low-value resistor. The larger current flow increases the voltage drop across R9 and tends to turn off the diodes CR1 and CR2, causing them to act as high-value resistors. In this case, the shunt elements act as high resistance and the series element acts as low resistance, which represents the minimum loss condition of the attenuator, maximum signal output.

The other extreme case occurs as the voltage at TP1 is reduced, going towards ground or even slightly negative. This tends to turn off and reverse bias diode CR3, the series element, which causes it to act as a high-value resistor. An existing fixed-current path from the +12 VDC line through R5, CR1, CR2, and R9 biases the series element CR3 off and the shunt elements, diodes CR1 and CR2, on, causing them to act as relatively low-value resistors. This represents the maximum attenuation case of the pin attenuator, minimum signal output. By controlling the value of the voltage applied to the pin diodes, the IF signal level is maintained at the set level.

4.1.7.6 Main IF Signal Path (Part 2 of 3)

When the IF signal passes out of the pin-diode attenuator through C11, it is applied to modular amplifier U1. This device includes the biasing and impedance-matching circuits that allows it operate as a wideband IF amplifier. The output of U1 is available at jack J2, as a sample of the pre-correction IF, for troubleshooting purposes and system set-up. The IF signal is then connected to the linearity corrector portion of the board.

4.1.7.7 Linearity Corrector Circuits

The linearity corrector circuits adjust for any amplitude non-linearities of the IF signal using three stages of correction. Each stage has a variable threshold control adjustment, R34, R37, or R40, and a variable magnitude control adjustment, R13, R18, or R23. The threshold control determines the point at which the gain is changed and the magnitude control determines the amount of gain change that occurs once the breakpoint is reached. Two reference voltages are needed for the operation of the corrector circuits. Zener diode VR1, with R33 and R135, provides a +6.8-VDC reference and diodes CR11 and CR12 provide a .9-VDC reference that temperature compensates for the two diodes in each corrector stage.

When the linearity correctors are operating, the IF signal is applied to transformer T1, which doubles the voltage swing by means of a 1:4 impedance transformation. Resistors R14, R15, and R16 form an L-pad that lowers the level of the signal. The amount the level is lowered can be adjusted with R13, in parallel with the L-pad resistors. R13 is only in parallel when the signal reaches a level large enough to turn on diodes CR4 and CR5. When the diodes turn on, current flows through R13, putting it in parallel with the L-pad. When R13 is put in parallel with the resistors, the attenuation through the L-pad is lowered, causing signal stretch, the amount of which is determined by the adjustment of R13. The signal is next applied to amplifier U2, which compensates for the loss through the L-pad.

The breakpoint, cut-in, for the first corrector is set by controlling where CR4 and CR5 turn on. This is accomplished by adjusting cut-in resistor R34, which forms a voltage-divider network from +6.8 VDC to ground. The voltage at the wiper arm of R34 is buffered by unity-gain amplifier U5D. This reference voltage is then applied to R35, R36, and C39, through L12, to the CR4 diode. C39 keeps the reference from sagging during the vertical interval. The .9-VDC reference created by CR11 and CR12 is applied to unity-gain amplifier U5B. The

reference voltage is then connected to diode CR5 through choke L11. Chokes L11 and L12 form a high impedance for the RF that serves to isolate the op-amp ICs from the IF.

After the signal is amplified by U2, it is applied to the second corrector stage through T2. This corrector and the third corrector operate in the same fashion as the first. All three corrector stages are independent and do not interact with each other.

The correctors can be disabled by moving jumper W1 on J4 to the Disable position, between pins 2 and 3; this moves all of the breakpoints past the tip of sync so that they will have no affect. The IF signal exits the board at IF output jack J3 after passing through the three corrector stages and is normally connected to an external IF phase corrector board.

4.1.7.8 Main IF Signal Path (Part 3 of 3)

After the IF signal passes through the external IF phase corrector board, it returns to the ALC board at IF input jack J7. The IF then passes through a bandpass filter consisting of L20, C97, C62, L21, C63, L22, L23, C64, and C99. This bandpass filter is identical in both form and function to the one described at IF input jack J1. In this case, the filter is intended to make up for the small errors in frequency response that are incurred by the signal while it is being processed through the linearity and incidental phase correction circuits. Following the bandpass filter, the signal is split using L24, L25, and R89. The signal passing through L24 is the main IF path through the board.

A sample of the corrected IF signal is split off and connected to J10, the IF sample jack. The IF connects to jacks J27 and J28, which control whether a 6-dB pad is included in the circuit by the positioning of jumpers W9 and W10. The 6-dB pad is in when jumpers W9 and W10 are connected between pins 2 and 3 on J27 and J28. The 6-dB pad is out when jumpers W9 and W10 are connected between pins 1 and 2 on J27 and J28. Normally, the pad is out. The IF signal is then applied to a two-stage frequency response corrector circuit that is adjusted as necessary.

Variable resistors R103 and R106 adjust the depth, or gain, of the notches and variable caps C71 and C72 adjust the frequency, or position, of the notches. The IF signal is amplified by U13 and U14 before it is connected to J12, the IF output jack of the board. R99 is an output level adjustment that is set to provide approximately 0 dBm of IF output at J12. A sample of the IF is fed to J11, which provides an IF sample point that can be monitored without breaking the signal path and gives an indication of the IF signal after the linearity and frequency response correction takes place.

4.1.7.9 ALC Circuit

The other path of the corrected IF signal is used in the ALC circuit. The IF is wired out of the splitter through L25, which is connected to op-amp U12. The output of U12 is wired to jacks J8 and J9; jumpers W4 and W8 control the normal, or encoded, operation of the ALC circuitry. For normal operation, jumper W4 on J8 is between pins 1 and 2 and jumper W8 on J9 is between pins 1 and 2.

The IF signal is applied to transformer T5, which doubles the voltage swing by means of a 1:4 impedance transformation before it is connected to the ALC detector circuit on the board and amplified by U10B. For normal operation, jumper W7 on J26 is between pins 1 and 2 and jumper W5 on J21 is between pins 1 and 2. The detected ALC voltage is wired to U10A, pin 2, where it is summed with the front panel power control setting. The output power adjustment for the transmitter is accomplished, if the (optional) remote power raise/lower kit (1227-1039) is purchased, by R75, a

motor-driven pot controlled by switch S1 on the board or screwdriver adjust pot R1 on the front panel of the UHF exciter tray. An external power raise/lower switch can be used by connecting it to jack J10, at J10-11 power raise, J10-13 power raise/lower return, and J10-12 power lower on the rear of the UHF exciter tray.

S1, or the remote switch, controls relays K1 and K2 which, in turn, the control motor M1 that moves variable resistor R75. If the (optional) remote power raise/lower kit is not purchased, the ALC voltage is controlled only by screwdriver adjust pot R1 on the front panel of the UHF exciter tray. The ALC voltage is set for .8 VDC at TP4 with 0 dBm output at J12 of the board. A sample of the ALC at J19, pin 2, is wired to the transmitter control board where it is passed on to the front panel meter and the AGC circuits. The ALC voltage and the DC level corresponding to the IF level after signal correction are fed to U10A, pin 2, whose output at pin 1 connects to the ALC pin-diode attenuator circuit. If there is a loss of gain somewhere in an IF circuit, the output power of the transmitter will drop, which the ALC circuit senses at U10A, automatically lowering the loss of the pin-diode attenuator circuit and increasing the gain to compensate.

The ALC action starts with the ALC detector level that is monitored at TP4. The detector output at TP4 is nominally +.8 VDC and is applied through resistor R77 to a summing point at op-amp U10A, pin 2. The current available from the ALC detector is offset, or complimented, by current that is taken away from the summing junction. In normal operation, U10A, pin 2, is at 0 VDC when the loop is satisfied. If the recovered or peak-detected IF signal at IF input jack J7 of this board should drop in level, which would normally mean that the output power is decreasing, the null condition would no longer occur at U10A, pin 2. When the level drops, the output of U10A at pin 1 will go more positive and, if jumper W3 on J6 is in the Automatic position, it will cause ALC pin-diode attenuators CR1, CR2, and CR3 to have less attenuation. This will increase the IF level and compensate for the decrease in level. If the ALC cannot sufficiently increase the input level to satisfy the ALC loop, because of not enough range, an ALC fault will occur. The fault is generated because U10D, pin 12, increases above the trip point set by R84 and R83 until it conducts. This makes U10D, pin 14, high, and lights the red ALC Fault LED DS2 on the board.

4.1.7.10 For Scrambled Operation with Encoding

For encoded, or scrambled, operation, jumper W4 on J8 must be connected between pins 2 and 3; jumper W8 on J9 must be between pins 3 and 2; jumper W7 on J26 must be between pins 2 and 3; and jumper W5 on J21 must be between pins 2 and 3. The IF is connected through W4 on J8 to the sync-regeneration circuits.

If this board is operated with scrambling, using suppressed sync, the ALC circuit operates differently than just described, because there is no peak-of-sync present on the IF input. A timing pulse from the scrambling encoder connects to the board at J24. This timing pulse is converted to sync pulses by U17A and U17B, controlling the operation of Q8. The sync amplitude is controlled by R149, which is then applied to U15A where it is added to the detected IF signal to produce a peak-of-sync level. The output of U15A is peak detected by CR26 and fed to U15B. If necessary, intercarrier notch L39 can be placed in the circuit by placing W6 on J22. The intercarrier notch is adjusted to filter any aural and 4.5-MHz intercarrier frequencies. The peak-of-sync signal is fed through R162, the ALC calibration control, to amplifier U15C. The amplified peak-of-sync output is connected through J21, pins 2 and 3, to U10A, where it is used as the reference for the

ALC circuit as well as the AGC reference to the transmitter control board (1265-1311).

Voltage TP4 should be the same in either the normal or the encoded video mode. Monitor J9, pins 3 and 4, with a spectrum analyzer, check that the board is in the AGC mode, and tune C103 to notch out the aural IF carrier.

4.1.7.11 Fault Command

The ALC board also has circuitry for an external mute fault input at J19, pin 6. This is a Mute command and, in most systems, it is part of the interface for the protection circuits of high-gain output amplifier devices. The Mute command is intended to protect the amplifier devices against VSWR faults. In this case, it is required that the actions occur faster than just pulling the ALC reference down. Two different mechanisms are employed: one is a fast-acting circuit to increase the attenuation of pin-diode attenuator CR3, CR1, and CR2, and the second, as just described, is the reference voltage being pulled away from the ALC amplifier device. An external mute is a pull-down applied to J19, pin 6, that provides a current path from the +12 VDC line through R78 and R139, the Mute Indicator LED DS4, and the LED section of opto-isolator U11.

These actions turn on the transistor section of U11 that applies -12 VDC through CR21 to U10A, pin 3, which pulls down the reference voltage. This is a fairly slow action that is slowed down by the low-pass filter function of R81 and C61. When the transistor section of U11 is on, -12 VDC is also connected through CR22 to the pin-diode attenuator circuit. This establishes a very fast muting action, by reverse biasing CR3, in the event of an external VSWR fault.

4.1.7.12 ±12 VDC to Operate the Board

The ±12 VDC connects to the board at J14. +12 VDC connects to J14-3 and is filtered by L30, L41, and C80 before it is applied to the rest of the board. The -12 VDC connects to J14-5 and is filtered by L31 and C81 before it is applied to the rest of the board.

The +12 VDC also connects to U16, a 5-VDC regulator IC, which produces the +5 VDC needed to operate timing IC U17.

4.1.8 (A19) Visual/Aural Metering Board (1265-1309; Appendix D)

Note: This board was originally designed for analog television signal operation. For digital applications, forward digital can be substituted for forward visual and the aural circuits along with the scrambling circuits are not used.

The visual/aural metering board provides detected outputs of the forward digital and reflected output samples that are used for monitoring on the front panel meter. The board also provides adjustments for the calibration of the readings on the meter. These readings are obtained from the samples of the forward power and reflected power outputs of the tray.

A forward power sample is applied to SMA jack J1 of the board. The input signal is split, with one path connected to forward power sample SMA jack J2 for monitoring purposes. The other path is connected through C1 to CR2, R4, R5, R6, C4, and CR1, which make up a detector circuit. The detected signal is amplified by U6B and its output is split. One amplified output of U6B connects to the digital level circuit, the other output is not used in digital operation.

4.1.8.1 Digital Level Circuit

The detected digital level output from U6B is connected to U1C. The intercarrier notch L3 is not used with digital. The digital output of U1C is fed to a peak-detector circuit consisting of CR5 and U2A and then fed through R28, the visual

(digital) calibration control that is adjusted for a 100% digital reading, to amplifier U2B. The amplified digital output is connected to comparator U2C. The other input to U2C is the level set by aural null adjust R51, which is not used with digital. Pots R51 and R20 should be set full CCW. The offset null adjust R48 is adjusted for 0% digital power with the transmitter in Standby. The adjusted output is amplified by U3D and connected to the other input of U2C. The output of U2C connects to J6, pins 2 and 3, which supplies the forward digital level output to the front panel meter for monitoring.

The scrambling circuits are not used with digital operation.

4.1.8.2 Reflected Level Circuit

A reflected power sample is applied to J3 of the board and is detected by diode detector CR7 and U3B. The detected output is fed through R39, the reflected calibration pot, which can be adjusted to control the gain of U3C. The output of U3C connects to J6, pin 7, which supplies a reflected power level output to the front panel meter.

4.1.8.3 Voltages for Circuit Operation

The ±12 VDC is applied to the board at J5. +12 VDC is connected to J5, pin 3, and is isolated and filtered by L4 and C34 before it is connected to the rest of the board. The +12 VDC also connects to U5, a 5-VDC regulator that provides the voltage needed to operate U4. The -12 VDC is applied to J5, pin 1, and is isolated and filtered by L5 and C35 before it is connected to the rest of the board.

4.1.9 (A11) UHF Upconverter Board (1265-1310; Appendix D)

The UHF upconverter board provides upconversion processing by mixing the IF and LO signals in mixer Z1 to produce the desired RF frequency output. The RF output is connected through J3 to an external filter and applied back to the board at J4 where the gain is set by R10. The RF is amplified and connected to the RF output jack of the board at J5.

The IF signal (0 dBm) enters the board at J1, an SMA connector, and is applied through a filter circuit consisting of L10 and C25 to C28 to a matching pad. This pad consists of R1, R2, and R3, which presents a relatively good source impedance, and feeds the signal to pins 3 and 4, the I input of mixer Z1. The local oscillator signal (+13 dBm) from the x8 multiplier connects to the board at jack J2, an SMA connector, through a UHF channel filter and is connected directly to pin 8, the L input of the mixer.

The frequency of the LO is the sum of the IF frequency above the required visual carrier. For instance, in system M, the IF visual frequency is at 45.75 MHz and the relative location of the aural would be 4.5 MHz lower, or 41.25 MHz. For digital applications, the LO is the center frequency of the digital channel added to the 44-MHz IF frequency. By picking the local oscillator to be 45.75 MHz above the visual carrier, a conversion in frequency occurs by selecting the difference product. The difference product, the local oscillator minus the IF, will be at the required visual carrier frequency output. There will also be other signals present at the RF output connector J3 at a lower level. These are the sum conversion product: the LO and the IF frequencies. Usually, the output product that is selected by the tuning of the external filter is the difference product: the LO minus the 45.75-MHz IF. The difference product has its sidebands flipped so that the visual carrier is lower in frequency than the aural carrier.

If a bad reactive load is connected to the mixer, the LO signal that is fed through it can be increased because the mixer no longer serves as a double-balanced mixer. The mixer has the inherent property of suppressing signals that may

leak from one input port to any of the other ports. This property is enhanced by having inputs and outputs of the mixer at 50Ω impedance. The reactive filter that is externally connected to J3 of the board does not appear as a good 50-Ω load at all frequencies. The pad, in the output line of the board, consists of R5, R4, R6, and R7. The pad buffers the bad effects of the reactive filter load and makes it appear as a 50-Ω impedance. The RF signal is amplified by U1, a modular amplifier, and includes within it biasing and impedance matching networks that makes U1 act as a wideband-RF amplifier device. This amplifier, in a 50-Ω system, has approximately 12 dB of gain. U1 is powered from the +12 VDC line through RF decoupling components R27, R28, C30, R8, and L1. Inductor L1 is a broadband-RF choke and is resonance free through the UHF band. The amplified RF connects to SMA RF output jack J3 which is cabled to the external filter.

The RF input signal from the external filter re-enters the board at J4 (-11 to -14 dBm) and is capacitively coupled to the pin-diode attenuator circuit consisting of CR1, CR2, and CR5. The pin-diode attenuator acts as a voltage-variable attenuator in which each pin diode functions as a voltage-variable resistor that depends on the DC bias supplied to the diode for the resistance value. The pin diodes, because of a large, intrinsic region, cannot rectify signals at this RF frequency; therefore, they act as a linear voltage-variable resistor.

The pin diodes are configured in shunt configuration: CR1 is the first shunt element, CR2 is the second shunt element, and CR5 is the series element. The manual gain AGC, W1 on J10 between pins 1 and 2, is used in most cases. The control voltage from manual gain pot R10 sets up a current path through R11 and the diodes in the pin attenuator. The level-controlled RF signal from the pin-diode attenuator circuit is amplified by wideband-hybrid amplifier IC U2 which is configured in the same way as U1. The RF signal is buffered by Q1 and applied to the push-pull class A amplifier circuit consisting of Q2 and Q3. At the input to the transistors, the RF is converted to a balanced, dual feed by balun L4, which is made from a short length of UT-141 coaxial cable.

Capacitors C12 and C13 provide DC blocking for the input signal to the amplifier devices. The RF outputs at the collectors of the transistors are applied through C19 and C20, which provide DC blocking for the output signals. The RF signals connect to L7, which consists of UT-141 coaxial cable. L7 combines the RF back to a single-RF output at a 50-Ω impedance to L8, which provides a sample of the RF. The main path through L10 is to J5, the RF output jack of the board (+10 to +20 dBm). The sample of the RF connects to a splitter that provides a sample output (0 dBm) at J6 of the board. The other output of the splitter connects to a peak-detector circuit consisting of CR3 and U3, which provides a DC level at J7 that represents the RF output of the UHF exciter to the front panel meter. R29 sets up the calibration of the front panel meter for 100% in the UHF exciter position when the output power of the exciter is at +17 dBm peak visual or +10 dBm average for digital applications.

The board is powered by ±12 VDC that is produced by an external power supply. +12 VDC enters the board through J8, pin 3, and is filtered and isolated by RF choke L9 and shunt capacitors C24 and C33. This circuit isolates the RF signals from the board away from those of other devices connected to the same +12 VDC line external to the UHF upconverter board. The +12 VDC is then applied to the rest of the board.

The -12 VDC enters the board through J8, pin 5, and is filtered and isolated by RF choke L11 and shunt capacitors C34 and C35. This circuit isolates the RF signals from this board away from those of other devices connected to the same

-12 VDC line that is external to the UHF upconverter board; the -12 VDC is then applied to the rest of the board.

4.1.10 (A17) Transmitter Control Board (1265-1311; Appendix D)

The transmitter control board provides the system control functions and the operational LED indications that can be viewed on the front panel of the transmitter. The main control functions are for Operate/Standby and Auto/Manual selection. When the transmitter is switched to Operate, the board supplies the enables to any external amplifier trays. When the transmitter is in Auto, the board also performs the automatic switching of the transmitter to Standby upon the loss of the video input. The board contains a VSWR cutback circuit. If the VSWR of the transmitter increases above 20%, the VSWR cutback circuit will operate and cut back the output level of the transmitter, as needed, to maintain a maximum of 20% VSWR. An interlock (low) must be present at J8-24 for the transmitter to be switched to Operate and, when the interlock is present, the green Interlock LED DS5 will be lit.

4.1.10.1 Operate/Standby Switch

K1 is a magnetic latching relay that controls the switching of the transmitter from Operate and Standby. When the Operate/Standby switch S1 on the front panel of the tray is switched to Operate, one coil of relay K1 energizes; this causes the contacts to close and apply a low to U4B-9. If the transmitter interlock is present, and there are no overtemperature faults, lows will also be applied to U4B-10, U4B-11, and U4B-12. With all the inputs to U4B low, the output at U4B-13 will be low. This low biases off Q1, which turns off the amber Standby LED DS1 on the front panel, and applies a high to Q2. The high turns on and lights the green Operate LED DS2 also on the front panel. When Q2 is biased on, it connects a low to Q12, which biases it off, and allows the ALC to be applied to J1, which is connected to any external amplifier trays. The low from U4B-13 is also applied to Q4 and Q24, which are biased off, and removes the disables from J1-4 and J18-1. The low from U4B-13 also connects to Q10, which is biased on, connects a high to Q6, Q7, Q8, and Q9, which are also biased on, and applies -12 VDC enables at J8-2, 3, 4, and 5, which connect to any external amplifier trays. The high applied to Q2 is also connected to Q5 and Q26, which are biased on, and applies a low enable to J1-3, which can connect to a remote operate indicator. The transmitter is now in Operate.

When the Operate/Standby switch S1 is switched to Standby, the other coil of relay K1 energizes, which causes the contacts to open. A high, +12 VDC, is applied to U4B-9. The high at the input causes the output at U4B-13 to go high. The high biases on Q1, which applies a low to the amber Standby LED DS1 on the front panel and turns it on. Q1 also applies a low to Q2, which turns off and extinguishes the green Operate LED DS2. In addition, Q12 is biased on and connects to U2C, whose output goes low and pulls the ALC voltages at J1 low, lowering the gain of the external amplifier trays. The high from U4B-13 is applied to Q4 and Q24, which are biased on, and applies disables at J1-4 and J18-1. The high from U4B-13 also connects to Q10, which is biased off. When Q10 is off, it removes the high from Q6, Q7, Q8, and Q9, which are biased off, and removes the -12 VDC enables at J8-2, 3, 4, and 5 that connect to the external amplifier trays. The low applied to Q2 is also connected to Q5 and Q26, which are biased off, and removes the remote enable at J1-3. The transmitter is now in Standby.

4.1.10.2 Automatic/Manual Switch

K2 is a magnetic latching relay that switches the operation of the transmitter to Automatic or Manual using

Auto/Manual switch S2 on the front panel of the tray.

When the S2 switch is set to the Auto position, the operation of the transmitter is controlled by the fault circuits and will stay in Operate even if Operate/Standby switch S1 is switched to Standby.

With switch S2 in Auto, a low is applied to one coil in the relay that energizes and closes the contacts. The closed contacts apply a low to the green Automatic LED DS3, causing it to light. The low from the relay connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. Q21 and Q23 are biased off, which causes their outputs to go high. The high from Q21 connects to the amber Manual LED DS4 on the front panel, biasing it off, and to Q22, biasing it on. The drain of Q22 goes low. The low is applied to J8-7 and this will enable any remote auto indicator that is connected to it. The low to Q23 biases it off and removes the enable to any remote manual indicator connected to J8-6.

When switch S2 is set to the Manual position, the operation of the transmitter is no longer controlled by the fault circuits; it is controlled by Operate/ Standby switch S1. With switch S2 in Manual, a low is applied to the other coil in the relay, which energizes and opens the contacts. The open contacts remove the low from the green Automatic LED DS3 on the front panel, causing it to not light. The high connects to U5A, pin 2; U5D, pin 13; Q21; and Q23. Q21 and Q23 are biased on, causing their outputs to go low. The low from Q21 connects to the amber Manual LED DS4 on the front panel, biasing it on, and to Q22, biasing it off. The drain of Q22 goes high. This high is applied to J8-7 and will disable any remote auto indicator that is connected to it. Q23 is biased on and applies a low enable to any remote manual indicator connected to J8-6.

4.1.10.3 Automatic Control of the Transmitter

The transmitter control board also allows the transmitter to be turned on and off by the presence of video or modulation to the transmitter when the transmitter is in Auto. When a video fault occurs due to the loss of the video or modulation input, J7-5 goes low. The low is applied through W1 on J10 to Q16, which is biased off, and to the red Video Loss Fault LED DS9 on the front panel, causing it to light. The drain of Q16 goes high and connects to U5B, pin 5, causing the output at pin 4 to go low. The low connects to Q18, which is biased off, causing the drain of Q18 to go high. The high connects to U3D, pin 12, whose output at pin 14 goes high. The high connects to U5C, pins 8 and 9, which causes its output at pin 10 to go low, and to U5A, pin 1, causing its output at pin 3 to go low. With S2 set to Automatic, a low is applied to U5A, pin 2, and to U5D, pin 13. When U5A, pin 1, is high and U5A, pin 2, is low, it causes the output at pin 3 to go low. When U5D, pin 12, and U5D, pin 13, are both low, it causes the output to go high. When U5A, pin 3, is low, it biases off Q20 and removes any pull-down to the Operate switch. A high at U5D, pin 11, biases on Q19 and applies a low enable to the Standby switch; this places the transmitter in the Standby mode.

When the video or modulation input is returned, J7-5 goes high. The high is applied to Q16, which is biased on, and to the red Video Fault LED DS9, which goes out. The output of Q16 goes low and connects to U5B, pin 5. If there is no receiver ALC fault, U5B, pin 6, is also low, which causes the output at pin 4 to go high. This high connects to Q18, which is biased on, and causes the drain of Q18 to go low. The low connects to U3D, pin 12, whose output at pin 14 goes low. The low connects to U5C, pins 8 and 9, which causes the output at pin 10 to go high, and to U5A, pin 1. With Auto/Manual switch S2 in Auto, a low is applied to U5A, pin 2, and to U5D, pin

13. With U5A, pins 1 and 2, low, the output at pin 3 goes high. With pin 12 of U5D high, the output of U5D at pin 11 goes low. When U5A, pin 3, is high, it biases on Q20, which applies a pull-down enable to the Operate switch. A low at U5D, pin 11, biases off Q19, which removes any pull-down to the Standby switch. The transmitter is switched to Operate.

4.1.10.4 Faults

There are four possible faults that may occur in the transmitter and are applied to the board: video or modulation loss fault, VSWR cutback fault, overtemperature fault, and ALC fault. During normal operations there are no faults to the board. The receiver ALC fault circuit will only function if a receiver tray is part of the system. The overtemperature fault is only used with the 2-kW transmitter and is controlled by the temperature of the reject load.

Video or Modulation Loss Fault

If a video or modulation loss occurs while the transmitter is in Auto, the system will go to Standby after a few seconds until the video is returned. The transmitter will immediately revert to Operate. A video loss fault applies a low from the ALC board to the video fault input at J7-5 on the board.

With jumper W1 in place on J10, the video fault is connected to the red Video Loss Fault LED DS9, causing it to light, and to Q16. Q16 is biased off, causing its drain to go high. The high is wired to U5B, pin 5, whose output at U5B, pin 4, goes low. The low is wired to Q18, which is biased off, and causes the drain to go high. The high is connected to U3D, pin 12, which causes the output at U3D, pin 14, to go high. The high connects to U5A, pin 1, and, if the transmitter is in Auto, pin 2 of U5A is low. With pin 1 high and pin 2 low, the output of U5A goes low and reverse biases Q20, shutting it off. The high at U5C, pins 8 and 9, causes its output at pin 10 to go low. This low is connected to U5D, pin 12, and, if the transmitter is in Auto, pin 13 of U5D is also low. The lows on pins 12 and 13 cause the output to go high and forward bias Q19. The drain of Q19 goes low and connects the coil in relay K1, causing it to switch to Standby.

When the video returns, the video loss fault is removed from the video fault input at J7-5. With jumper W1 in place on J10, the base of Q16 goes high. The red Video Loss Fault LED DS9 on the front panel will go out. Q16 is biased on, causing the drain to go low. This low is wired to U5B, pin 5, and U5B, pin 6, will be low if no ALC fault occurs. The two lows at the inputs make the output at U5B, pin 4, go high. The high is wired to Q18, which is biased on, and causes the drain to go low. The low is connected to U3D, pin 12, which causes its output at U3D, pin 14, to go low. The low connects to U5A, pin 1, and, if the transmitter is in Auto, pin 2 of U5A is also low. With both inputs low, the output of U5A at pin 3 goes high. The high forward biases Q20, causing its drain to go low. The low connects to the Operate coil on the K1 relay that switches the transmitter to Operate. The low at U5C, pins 8 and 9, causes the output at pin 10 to go high. This high is connected to U5D, pin 12, and, if the transmitter is in Auto, pin 13 of U5D is low. The high on pin 12 causes the output of U5D to go low and reverse bias Q19. The drain of Q19 goes high and removes the low from the Standby coil in relay K1.

Overtemperature Fault

In a transmitter of 1 kW or less, there is no connection to the overtemperature circuit on the board. In the 2-kW transmitter the thermal switch on the output dummy load connects to J8-1 on the board. In the 100-watt transmitter (A6) the thermal switch on (A23) the 100-watt amplifier heatsink assembly connects to J12 on the board. If the temperature of the thermal switch rises

above 170° F, it closes and applies a low to J8-1 or J12. The low connects to Q3, which is biased off, and to the red Overtemperature LED DS6, which is biased on. The drain of Q3 goes high and connects to pins 11 and 12 of U4B. The high at the input to U4B causes it to go high and switches the system to standby. This removes the Operate enable commands to any external amplifier trays.

VSWR Cutback Fault

The reflected power sample of the RF output of the transmitter is connected to J2, pin 9, of the board. The sample connects to op-amp U1B, pin 5, which buffers the signal before it is split. One of the reflected samples that is split is connected to J1-5, which is wired to J10-5 on the rear of the tray, for remote monitoring. The other reflected sample that is split is connected to position 3 on the front panel meter of the tray. The final remote reflected sample that is split is connected to U2B, pin 5.

If the reflected sample level increases above the level set by R22, the VSWR cutback pot, the output of U2B at pin 7 goes high. The high is connected to Q11 through CR11, which is biased on, making U2C, pin 10, low and causing U2C, pin 8, to go low. This low is split and fed out of the tray at J1-6, J1-7, J1-8, and J1-9; these are ALC outputs to the amplifier trays that cut back the output power of the amplifier trays. The low from U2C, pin 8, is also fed through coaxial jumper W2 on J13 and J14 to R73. R73 is a bias adjust pot that sets the level of the pin-attenuator bias that is available as an output at J16.

The high at U2B, pin 7, is fed to the base of Q14 and Q13, which are forward biased, and produces a low at the drains. The low connects to the front panel amber VSWR Cutback LED DS7 and causes it to light, indicating that the tray is in cutback, and to output jack J8-37 for a connection to a remote VSWR cutback indicator.

Receiver ALC Fault

If a receiver tray is part of the system, a sample of the ALC voltage from the receiver tray is connected to J8-11 on the board. If the receiver is operating normally, the ALC level applied to U3C, pin 9, remains below the trip level set by R35; the output at pin 13 stays high. The high is applied to the red ALC Fault LED DS8, which is off. The high also connects to U3A, pin 2, and to Q15. Q15 is biased on and the drain goes low. The low connects to U5B, pin 6. U5B normally has a low that is connected to U5B, pin 5, and produces a high at the output pin 4. The high is wired to Q18, which is biased on, and makes its drain low. The low connects to U3D, pin 12, which, because the level is below the preset, its output at U3D, pin 14, goes low. A low at this point indicates a no-fault condition. The high connected to U3A, pin 2, causing its output to go low. The low is connected to Q25, which is biased off. The low is removed from J8-12, which will not light any remote receiver fault indicator that is connected to it.

If the receiver should malfunction, the ALC level applied to U3C, pin 9, goes high; because this is above the level set by R35, the output at pin 13 will go low. The low is applied to the red ALC Fault LED DS8, which lights. The low also connects to U3A, pin 2, and to Q15. Q15 is biased off and the drain goes high. The high connects to U5B, pin 6, which produces a low at its output at pin 4. The low is wired to Q18, which is biased off, and makes its drain high. The high connects to U3D, pin 12; because the level is above the preset, the output at U3D, pin 14, goes high. A high at this point indicates a fault condition that switches the transmitter to Standby. The low connected to U3A, pin 2, causes its output to go high. The high is connected to Q25, which is biased on, causing its drain to go low. The low is connected to

J8-12, which can light any remote receiver fault indicator that is connected to it.

4.1.10.5 Metering

The front panel meter connects to J3-1(-) and J3-2(+) on the board; this is the output of switch S3. The front panel meter has four metering positions that are controlled by switch S3: % Forward Power, % Reflected Power, % Exciter, and ALC.

The reflected sample connects to the board at J2-9 and is connected through buffer amplifier U1B and 100-Ω resistor R84 to position 3 of switch S3. The forward sample connects to the board at J2-5 and is connected through buffer amplifier U1D and 100-Ω resistor R86 to position 4 of switch S3. The exciter sample connects to the board at J2-3 and is connected through buffer amplifier U1A and 100-Ω resistor R87 to position 2 of switch S3. The ALC sample connects to the board at J6-1 and is connected through buffer amplifier U2C; R15, the ALC calibration pot that adjusts the output of U2A, pin 1; through 100-Ω resistor R18; and to position 1 on switch S3.

Typical readings on the meter are:

- % Reflected = <5%
- % Forward Power = 100%
- % Exciter = The level on the meter needed to attain 100% output power from the transmitter

Refer to the test specifications sheet for the transmitter for the actual readings for the items shown below:

- ALC = .8 VDC

Samples of the exciter at J1-10, the visual at J8-26, the aural at J8-27, and the reflected at J1-5 are provided for remote metering.

U6 is a temperature sensor IC that gives the operator the ability to measure the temperature inside the tray by measuring the voltage at TP1. The sensor is set up for +10 mV equals 1° F (for example, 750 mV equals 75° F).

4.1.10.6 Operational Voltages

The +12 VDC needed for the operation of the board enters the board at jack J4, pin 3. C28, L1, and L3 are for the filtering and isolation of the +12 VDC before it is split and applied to the rest of the board. The -12 VDC needed for the operation of the board enters at jack J4, pin 5. C29 and L2 are for the filtering and isolation of the -12 VDC before it is split and applied to the rest of the board.

When the +12 VDC is connected to the board, it is split. Four of the +12 VDC outputs are fed out of the board at J8-16, J8-17, J8-18, and J8-19 through diode CR7, CR8, CR9, or CR10 and resistor R50, R51, R52, or R53 to any external amplifier trays for use in their logic circuits. The resistors are for current limiting and the diodes are to prevent voltage feedback from the external amplifier trays.

4.1.11 (A3)+12V(4A)/-12V(1A) Power Supply Board (1265-1312; Appendix D)

The ±12-volt power supply board consists of three separate power supplies, two of which produce the +12 VDC and one for the -12 VDC needed to power the circuit boards in the exciter tray.

4.1.11.1 +12 VDC Power Supply

The 18 VAC from the external step-down toroid in the tray connects to J1, pins 7 and 8. The 18 VAC connects through 7-amp fuse F2, for over-current protection, to two full-wave bridge rectifier circuits.

CR1, CR2, CR3, and CR4 rectify the AC that is then filtered by C2 and connected

to U3 and U4; U3 and U4 are voltage-regulator ICs for the +12 VDC. The voltage-regulated and current-limited +12-VDC output of U3 connects to J4, pins 1, 2, 3, and 4, which is one of the +12-VDC outputs of the board. The green LED DS3 will be lit if +12 VDC is present to J4; C7 and C8 are bypass capacitors. The +12 VDC output of U4 connects to J5, pins 1, 2, 3, and 4, which is another one of the +12-VDC outputs of the board. The green LED DS4 will be lit if +12 VDC is present to J5; C9 and C10 are bypass capacitors.

CR5, CR6, CR7, and CR8 rectify the AC that is then filtered by C1 and connected to U1 and U2; U1 and U2 are voltage-regulator ICs for the +12 VDC. The voltage-regulated and current-limited +12-VDC output of U1 connects to J6, pins 1, 2, 3, and 4, which is one of the +12-VDC outputs of the board. The green LED DS1 will be lit if +12 VDC is present to J6; C3 and C4 are bypass capacitors. The +12-VDC output of U2 connects to J3, pins 1, 2, 3, and 4, which is another one of the +12-VDC outputs of the board. The green LED DS2 will be lit if +12 VDC is present to J3; C5 and C6 are bypass capacitors.

4.1.11.2 -12 VDC Power Supply

The 18 VAC from an external step-down toroid connects to J1, pins 1 and 4, of the board and is wired to CR9, CR10, CR11, and CR12 which form a full-wave bridge rectifier network for the –12-VDC power supply. F1 is a 3-amp fuse that provides over-current protection. The rectified output is filtered by C11 and fed to U5, the voltage-regulator IC for the -12 VDC. The voltage-regulated and current-limited -12 VDC is connected to the -12-VDC output jacks J7, pins 5 through 10, and J8, pins 5 through 10. The green LED DS5 will be lit if -12 VDC is present to J7 and J8; C12 and C13 are bypass capacitors.

4.1.12 (A21) 5-Section Delay Equalizer Board, 44 MHz (1072090; Appendix D)

The 5-section delay equalizer board, 44 MHz, is designed to correct for any group delay errors that have been created by the digital mask filter. The board consists of five separate delay/attenuation equalizer sections. Each section is tuned across the 41 to 47 MHz band depending on where the correction is needed. J9 on W3 determines the input impedance for the IF source:

- J19-1, J19-2=50 Ω
- J19-2, J19-3=75 Ω

J23, J27 determines 6 dB attenuation; J23-1, J23-2 and J27-1, J27-2 means that there is no attenuation; and J23-2, J23-3 and J27-2, J27-3 means that there is 6-dB attenuation.

Delay equalizers 1 through 5 are each tuned to a different frequency to equalize the delay characteristics of that frequency. Attenuation equalizers 1 through 5 are tuned to the same frequency as their matched delay equalizer section and are isolated from them by a 3-dB pad. Each equalizer/attenuation pair is followed by a 12-dB gain stage with 6 dB of attenuation between the sections. Depending on where the jumpers are positioned, each equalizer section can be jumpered into the circuit or bypassed by using a 2-dB pad.

4.2 (A19) 8-VSB Digital Modulator (1075164; Appendix C)

4.2.1 (A6) Vector Modulator Board (1520-1107; Appendix D)

The vector modulator board receives the I and Q outputs from the VSB modulator board (1561-1201) and modulates and mixes the signals for a 44-MHz IF output signal. The board allows for the adjustment of the offset and gain of the I (in-phase) and Q (90° out-of-phase)

signals. The board also provides for the frequency response and gain adjustment of the IF signal. The circuitry for the I and Q signals to the mixers is identical.

The I signal enters the board at J3-2. Diodes CR1 to CR3 provide surge protection to buffer U4. The output of U4 is fed through variable resistor R32, the gain pot for the unmodulated signal. The circuit consisting of U1 and its associated components provides the DC-offset adjustment at the input of U5. Variable resistor R5 provides the shift in DC level to the input of U1, causing a corresponding shift in the output. The resulting output from U1 is fed to the input of U5; the output of U5 is fed to mixer Z1.

The 46.49056-MHz signal enters the board at J7 and is amplified through two MAV-11 op-amps. The signal is then fed to phase/splitter U8 and the outputs of U8 provide the in-phase and out-of-phase local oscillator signals for the I and Q mixers, respectively. The outputs from the I and Q mixers can be phase and gain adjusted by C29, R58, C32, and R79. These two signals are then mixed together at Z2 with a resulting output of 44 MHz. The frequency response of the IF signal is adjusted using variable resistors R29 and R30 and capacitors C19 and C20. The gain is adjusted using variable resistor R3.

The ±12 VDC required to operate the board enters at J8. The ±10 VDC for the offset circuits is supplied by U12 and U13A and their associated components. U12 is a regulator with a +12-VDC input and a +10-VDC output. U13A inverts this voltage for the –10-VDC source.

4.2.2 (A2) Switch Board (1561-1202; Appendix D)

The switch board provides three front-panel momentary contact switches for user control and interface with the front-panel LCD menu selections. The switches, SW1 to SW3, complete the circuit through connector J1 to connector J17 on the VSB modulator board (1561-1201). When they are closed, the switches place a logic low at U14 on the VSB modulator board. Jumper J2 provides a logic low to U14 on the VSB modulator board to enable the Test mode.

4.2.3 (A7) Local Oscillator Board (1561-1203; Appendix D)

The local oscillator board provides the 46.690560-MHz phase-locked output for the vector modulator board (1520-1107). The on-board oscillator, U2, feeds the IF output at J6 and the IF sample at J8. The oscillator also provides a sample to phase-lock control IC U4. When switches SW1 to SW3 are set to a predetermined state, and the 10-MHz reference is present on the board, U4 will output a correction voltage to maintain the phase lock of oscillator U2. The correction voltage is fed through buffers U1A, U1B, and U5B to pin 2 of the oscillator. The switch settings are determined by the following equation (the resulting value is converted to binary with the least significant bit at SW3-1):

Switch setting = (LO frequency/2) –3

Once the switch settings are calculated, and there is a 10-MHz reference present at the rear of the tray, the board will begin the process of phase locking the VCXO. There are three amber LEDs on the board indicating the progress of the PLL circuit; these LEDs are designated step 1, step 2, and step 3.

When the circuit begins the PLL process, step 1 will illuminate. As the process continues, step 1 extinguishes and step 2 illuminates. Finally, step 2 extinguishes and step 3 illuminates. Once step 3 extinguishes, the front panel PLL Locked LED will illuminate within 30 seconds.

The board drives two LEDs on the front panel LED board. The PLL Locked

indicator is driven from U4, pin 60, through field effect transistors (FETs) Q2 to J9-4. The 10-MHz reference present indicator is driven from the collector of Q1 through transistor Q3 and associated components to J9-2.

The +12 and -12 VDC source is supplied at J2. The +5 VDC is supplied at J1. L2, L3, C13, C21, and C23 are for filtering.

4.2.4 (A3) LED Board (1561-1204; Appendix D)

The LED board provides front-panel verification of the status of the MPEG input signal, 10-MHz reference signal, phase-locked status of the IF oscillator, and the +5-VDC power supply.

DS1 is driven from the VSB modulator board (1561-1201) that provides a constant +5 VDC to J1-1 and a logic low at J1-2 when the MPEG input signal is present. DS2 is driven from the local oscillator board (1561-1203) that provides a constant +5 VDC and a logic low at J1-4 when the 10-MHz reference signal is present at the oscillator board. DS3 is driven from the local oscillator board that provides a constant +5 VDC and a logic low at J1-6 when the IF oscillator is phase locked. DS4 is driven from the +5 VDC source on the DC power supply board (1520-1103) through J1-7.

4.2.5 (A11) VSB Modulator Interface Board (1561-1205; Appendix D)

The VSB modulator interface board interfaces with the external MPEG source to the VSB modulator board (1561-1201) in the front of the tray. The interface board receives MPEG either at J11 in the Society for Motion Picture and Television Engineers (SMPTE) format, at J1 in differential emitter-to-coupler logic (ECL) format, or at J2 in differential transistor-to-transistor logic (TTL) format and converts it to single-ended TTL. The output is in the form of data (J10) and a clock (J3). The jumpers at J13 and J14 on this card select between the various input formats. These jumper settings are outlined in Chapter 5, Detailed Alignment Procedures, of this manual. Jumpers J4 through J7 were used during the initial design of the board and have been preset at the factory. These four jumpers should all be placed in positions 1-2 with the exception of jumper J6, which should be placed in position 2-3. Jumper block J15 was also used in the initial design of the board and should be set to position 3.

This card also provides the capability for a future parallel interface. This future parallel interface can be in either a TTL or ECL format. Test connector J8 will be used for the future parallel interfaces.

Note: This future interface will utilize the PLL Locked LED at the bottom, right-hand corner of this board; the LED will not illuminate with the existing interfaces.

The board is supplied by a –12-VDC and a +5-VDC source. Regulator U16 converts the -12 VDC to a -5.2-VDC source.

4.2.6 (A5) VSB Filter Board (1561-1301; Appendix D)

The VSB filter board performs the digital pulse-shaping filter function of the ATSC specification. The board receives equalized symbol data at J1 and applies it to an I pulse-shaping filter and a Q pulse-shaping filter. The I filter is implemented in U1 and U2 and the Q filter is implemented in U3 and U4. The pulse-shaping filter outputs are applied to D/A converters through jumper blocks J25 and J28. The output of the D/A converters is filtered to remove the 32.28-MHz converter update rate. The I data is available at J26 and the Q data is available at J29.

4.2.7 (A10) DC Power Supply Board (1047033; Appendix D)

The DC power supply board generates both positive and negative 12 and 5 VDC, as well as positive 3.3 VDC, at a current level that is sufficient to operate the other boards in the modulator tray. Visual indicators, using LEDs, are provided on the board to show the normal operation of each voltage regulator.

The DC outputs (+15, +5, and -15 VDC) from the switching power supply (1049886) are directed to jack J1. The voltages are then filtered by C1 to C6 and fed to voltage regulators U1 to U7. The outputs are protected from over-current conditions by the regulators. The regulators are designed to fold back the voltage if a short-circuit condition occurs external to the board and will continue to do so until the short is eliminated. If a short appears, the on-board LED associated with that regulator will extinguish with the loss of the output.

4.2.8 (A8) VSB IF Filter Board (1047976; Appendix D)

The VSB IF filter board performs the low-pass filtering of frequencies above 63 MHz.

The board receives the output IF signal from the vector modulator board at J1. The input signal is fed through the 50-Ω matching circuit of R1, R2, and R3. The signal is then filtered by low-pass filter circuit L1 to L5 and C2 to C6. The signal is amplified by U1 and fed to SMA connector J2. The signal is also fed through the IF sample circuit of U2 and associated components to J4, the IF sample. This sample is fed to the front panel sample port.

The board is supplied by an external +12-VDC source.

4.2.9 (A4) VSB Symbol Generator Board (1049396; Appendix D)

The symbol generator board takes the MPEG data and clock signals from the interface card and performs the digital signal-processing functions outlined in the ATSC specification for 8-VSB modulation. These functions involve data randomization, the Reed Solomon encoder, the data interleaver, and the trellis encoder. These functions are implemented in the programmable logic chip U1 on the symbol generator card. In addition, this card performs the linear equalization function. This function is implemented in U14.

The output of this card is symbol data that has been equalized. The data is available at J25 in the form of ten data lines and a 32.28-MHz clock. In addition, the microcontroller data and address bus is available at this output connector.

The LCD display and the switch panel are also controlled by the symbol generator card. The interface to the LCD display is provided at J20 and the interface to the switch panel is provided at J21. The RS-232 interface to Port A is provided at J19 on this card. This interface is wired to the rear of the tray and is used to load the linear equalizer and perform adaptive equalization. The Port B serial interface is wired through connector J4 on this card.

4.3 (A6 and A7, A8 and A9 with upgrade) UHF Amplifier Trays (1294-1112, 1294-1113 or 1294-1114; Appendix C)

4.3.1 (A3) 1-Watt Amplifier Board Assembly (1227-1319; Appendix D)

The 1-watt UHF amplifier board assembly provides radio frequency interference (RFI) and electromagnetic interference (EMI) protection, as well as the heatsink, for the 1-watt UHF amplifier board (1227-1303) that is mounted inside the module assembly. Depending on the

frequency of the channel of operation, the assembly has approximately 9 dB of gain.

The RF input to the assembly connects to SMA jack J1. The amplified RF output of the assembly is at SMA jack J2. Typically, with an input signal of +21 dBm at J1 of the assembly, an output of +30 dBm can be expected at J2.

The +28-VDC bias voltage connects through FL1, an RF bypass feed-through capacitor, that is mounted on the amplifier assembly to E1 on the board.

4.3.2 (A3-A1) 1-Watt Amplifier Board (1227-1303; Appendix D)

The 1-watt UHF amplifier board is part of the 1-watt UHF amplifier assembly (1227-1319) and provides approximately +10 dB of gain.

The UHF signal enters the board at J1, an SMA connector, and is applied through coupling capacitor C1 and a stripline circuit to Q1, a UTV040F UHF wideband-amplifier device. The base and collector voltages needed to operate the transistor are obtained from the +26.5 VDC line that connects to the board at E1. The collector voltages fed through VR1, VR2, R3, and R4 and the base voltages fed through R2 and R1. The amplified UHF output of Q1 is coupled through a stripline circuit and C14 to J2, the output SMA jack of the board.

The board is powered by the +26.5 VDC that is produced by an external power supply in the tray. The +26.5 VDC enters through E1 and is fed across R4 and R5, which drops approximately 6 volts, to the collector (+20 VDC). The voltage is filtered by RF decoupling components L4, C11, C12, and C15 before it is connected to the collector. The bias voltage is connected across R3, VR1, VR2, R1, and R2, which sets the base bias voltage at +.8 VDC and forward biases Q1. C6, L1, and L2 provide RF decoupling of the bias voltage before it is connected to the base.

The board has a self-bias protection circuit that uses zener diodes VR1 and VR2. If the current draw of the device increases, the voltage drop across R4 and R5 increases; this decreases the voltage that is applied to VR1 and VR2. These two diodes drop a fixed voltage of 20 VDC across them. As a result, if the voltage drop across R4 and R5 increases, the voltage available to the base of Q1 decreases and will eventually shut off the device.

4.3.3 (A5-A1) 4-Way Splitter Assembly (Appendix D)

The 4-way splitter assembly contains a 4-way splitter board that is made up of three 2-way Wilkinson stripline splitters. One RF input to the board provides four, equal RF outputs.

The RF input to the board is connected to the input of the first 2-way splitter that contains R1. R1 is a balancing resistor in which any RF due to mismatching in the first splitter will be dissipated. One of the two outputs from the splitter connects to another 2-way splitter that contains R2. R2 is a balancing resistor in which any RF due to mismatching in the splitter will be dissipated. The other output of the first splitter connects to the third 2-way splitter that contains R3. R3 is a balancing resistor in which any RF due to mismatching in the splitter will be dissipated. The two output splitters provide four, equal RF outputs, two each, that are connected to the inputs of the external amplifier boards.

4.3.4 4-Way Splitter Board (Appendix D)

The 4-way splitter board is made up of three 2-way Wilkinson stripline splitters. One RF input to the board provides four, equal RF outputs.

The RF input to the board is connected to the input of the first 2-way splitter that contains R1. R1 is a balancing resistor in which any RF due to mismatching in the first splitter will be dissipated. One of the two outputs from the splitter connects to another 2-way splitter that contains R2. R2 is a balancing resistor in which any RF due to mismatching in the splitter will be dissipated. The other output of the first splitter connects to the third 2-way splitter that contains R3. R3 is a balancing resistor in which any RF due to mismatching in the splitter will be dissipated. The two output splitters provide four, equal RF outputs, two each, that are connected to the inputs of the external amplifier boards.

4.3.5 (A4-A2) Coupler Board Assembly (1227-1316; Appendix D)

The UHF coupler assembly is mounted in the UHF amplifier tray and provides a forward power sample of the input drive level to the dual stage amplifier assembly, class AB. The drive-level sample from J3 is cabled to the amplifier control board where it connects to the input of the overdrive-protection circuit.

The RF input to the UHF coupler assembly from the dual stage amplifier assembly, class A, connects to SMA jack J1. The RF is connected by a stripline track to SMA output jack J2. A hybrid-coupler circuit picks off a forward sample that is connected to SMA type connector jack J3. R1 is a dissipation load for the reject port of the coupler.

4.3.6 (A6) Dual Peak Detector Enclosure (1227-1317; Appendix D)

The dual peak detector enclosure provides EMI and RFI protection for the dual peak detector board, single supply (1227-1333), that is mounted inside of the enclosure. The module has two inputs: a forward power sample at SMA jack J1 and a reflected power sample at SMA jack J2. The module has two peak-detected sample outputs: a forward power sample at FL3 from J4-4 on the board and a reflected power sample at FL2 from J4-2 on the board. The module also has a forward power sample output at SMA jack J3.

The voltage, +28 VDC, needed to operate the board connects to FL1 on the assembly that is wired to J4-7 on the board.

4.3.7 (A6-A1) Dual Peak Detector Board, Single Supply (1227-1333; Appendix D)

The function of the dual peak detector board is to detect forward and reflected samples of visual or aural RF signals and generate an output voltage proportional to the power levels of the sampled signals for metering purposes.

There are two identical signal paths on the board: one for forward power and one for reflected power. A sample of forward output power enters the board at SMA jack J1. Resistors R1, R2, and R3 form an input impedance-matching network of 50Ω. The forward power signal is detected by CR1, R4, R5, R7, R10, C1, and C2. The output is buffered by operational amplifiers U3B and U1C before it is connected to forward power output jack J4-4. U3 has a very high input impedance that makes the IC less sensitive to changes in the video level. A sample of the forward power is tapped off by R6 and R8 and fed to J3, the forward sample output jack. Diode CR2 provides temperature compensation for diode CR1. An input signal level of approximately +17 dBm is enough to give a 1-VDC level at the output of U1C.

A reflected output power sample enters the board at SMA jack J2. Resistors R18, R19, and R20 form an input impedance matching network of 50Ω. The reflected power signal is then detected by CR3, R21, R22, R24, C5, and C6 and the output is buffered by operational amplifiers U3A and U1B before it is connected to reflected power output jack

J4-2. U3 has a very high input impedance that makes the IC less sensitive to changes in the video level. Diode CR4 provides temperature compensation for diode CR3. An input signal level of approximately +17 dBm is enough to give a 1-VDC level at the output of U1B.

The +12 VDC needed for the operation of U1 IC on the board is generated from the +28 VDC which enters at J4, pin 7. The +28 VDC is fed to U2, a voltage regulator IC, which produces +12 VDC at its output that is connected to the U1 IC.

4.3.8 Dual Stage Amplifier Assembly, Class AB; Appendix D)

The dual stage UHF amplifier assembly, Class AB is made using a generic dual stage amplifier board, class AB (1265-1404). The board uses two PTB20101 Ericsson transistors in parallel-biased class AB to amplify the signal by approximately +9 dB. Bias adjust R106 sets the idling current for Q101 at 300 mA and bias adjust R206 sets the idling current for Q201 at 300 mA. Each dual amplifier device is mounted in identical parallel circuits. These devices may be biased up to 600 mA depending on the linearity of the tray.

4.3.8.1 Input Description

The input signal from J1 on the dual stage amplifier assembly connects to E1 on the board. The signal is split in a 2-way wilkinson splitter, using R1, which provides two equal inputs, one to each identical amplifier side.

4.3.8.2 Q101 and Associated Circuitry

One of the outputs of the splitter is applied through an AC coupling and DC blocking capacitor (C101 to L101) and associated circuitry. This forms a balun that converts the input signal from a 50-Ω unbalanced impedance to a 12.5-Ω balanced impedance configuration. C106 and C105, which are adjusted for peak output, are for impedance matching to the input of the parallel transistors making up Q101.

The bias voltage to the bases of the paralleled transistors in Q101 is applied at E101. The transistors are protected from overvoltage by Q102, Q103, R104, R105, and R106, which can be adjusted to set the bias, operating currents of the transistors. The base voltage is RF bypassed by C129, C102, C107, C108, C109, and C110 and applied to the bases through R102 and R103.

The collectors are impedance matched to 12.5Ω by C116, C120, C122, C123, and C119, which can be adjusted for peak output with best linearity and lowest current. C125 provides AC coupling and DC blocking for the output signal to the combiner. L102 and associated circuitry form a balun that transforms the signal back to an unbalanced 50-Ω impedance signal.

The collector voltage is applied at E101. The collector voltage is connected through R108 to the collectors on the two devices that make up Q101. R106 can be adjusted to set up the operating currents. The collector circuit is RF bypassed by C112 to C115, C117, C118, C121, C124, C130, and C131.

4.3.8.3 Q201 and Associated Circuitry

The other output of the splitter is applied through an AC coupling and DC blocking capacitor (C201 to L201) and associated circuitry. This forms a balun that converts the input signal from a 50-Ω unbalanced impedance to a 12.5-Ω balanced impedance configuration. C206 and C205, which can be adjusted for peak output, are for impedance matching to the input of the parallel transistors (Q201).

The bias voltage to the bases of the paralleled transistors, Q201, is applied at E201. The transistors are protected from overvoltage by Q202, Q203, R204, R205, and R206, which can be adjusted to set

the bias, operating currents of the transistors. The base voltage is RF bypassed by C229, C202, C207, C208, C209, and C210 and applied to the bases through R202 and R203.

The collectors are impedance matched to 12.5Ω by C216, C220, C222, C223, and C219, which can be adjusted for peak output with best linearity and lowest current. C225 provides AC coupling and DC blocking for the output signal to the combiner. L202 and associated circuitry form a balun that transforms the signal back to an unbalanced 50-Ω impedance signal.

The collector voltage is applied at E201. The collector voltage is connected through R208 to the collectors on the two devices that make up Q201. R206 can be adjusted to set up the operating currents. The collector circuit is RF bypassed by C212 to C215, C217, C218, C221, C224, C230, and C231.

4.3.8.4 Output Description

The outputs of the two sides are combined by a 2-way wilkinson combiner, using R2, and applied to the RF output of the board at E2. The output is connected to J2, the SMA output jack on the dual stage amplifier assembly.

4.3.9 Generic Dual Stage Amplifier Board, Class AB (1265-1404; Appendix D)

The generic, dual stage UHF amplifier board, class AB, is used as the basic board in building the dual stage amplifier assembly, class AB.

Mounted on the generic board are the components that have no frequency-determining factors. The low-band, mid-band, and high-band assemblies are produced by adding the specific frequency-related components to the generic board to make the specific-frequency assembly.

4.3.10 (A7) Amplifier Protection Board (1265-1412; Appendix D)

The amplifier protection board distributes the biasing voltages to the transistor amplifier devices that are mounted on the amplifier boards in the UHF amplifier tray. It also protects the transistor devices from overcurrent conditions using the board-mounted 7-amp fuses F1 to F12. F13 is a board-mounted 3-amp fuse that protects the +26.5 VDC that is applied to the amplifier control board and is needed for the operation of the board. F14 and F15 are 7-amp spare fuses.

The +26.5 VDC from the switching power supply enters the board at TB1, with the plus (+) connections to pins 1 to 4 and the minus (-) connections to pins 5 and 6. The +26.5 VDC is connected across the .01W/3Ω voltage-dropping resistors R14 to R26 that are used to set up the idling currents for the transistor devices; the fuses F1 to F13 that protect the transistor devices during an overcurrent condition through the outputs of the board at TB2, TB3; and also to output jack J1. Table 4-1 indicates the fuse, the amplifier device it protects, and the idling current settings for the class AB amplifier devices.

Table 4-1. Fuses, Idling Currents, and Voltage Settings for the Class AB Amplifier Devices

SWITCH POSITION	AMPLIFIER MODULE	TRANSISTOR DEVICE	BIAS ADJUST POT	IDLING CURRENT	VOLTAGE SETTING	FUSE
I1	A4-A1	Q1	R6	*5 Amps	50 mV	F1
I2	A4-A3	Q201	R206	600 mA	6.0 mV	F2
I3	A4-A3	Q101	R106	600 mA	6.0 mV	F3
I4	A5-A2	Q201	R206	300 mA	3.0 mV	F4
I5	A5-A2	Q101	R106	300 mA	3.0 mV	F5
I6	A5-A3	Q201	R206	300 mA	3.0 mV	F6
I7	A5-A3	Q101	R106	300 mA	3.0 mV	F7
I8	A5-A4	Q201	R206	300 mA	3.0 mV	F8
I9	A5-A4	Q101	R106	300 mA	3.0 mV	F9
I10	A5-A5	Q201	R206	300 mA	3.0 mV	F10
I11	A5-A5	Q101	R106	300 mA	3.0 mV	F11

*The A4-A1 transistor Q1 operates class A and is adjusted for 5 amps of operating current.

The voltage drop across the selected resistor using switch S1 is read with a digital voltmeter (DVM) that is connected from E1 to E2 on the board. This voltage reading converts to the idling current, with no RF drive applied, or the operating current, with RF drive applied, of the transistor.

4.3.11 (A8) Amplifier Control Board (1265-1414; Appendix D)

The amplifier control board provides LED fault and enable indications on the front panel of the tray and also performs the following functions: automatic gain control (AGC); overdrive cutback, when the drive level reaches the amount needed to attain 110% output power; and overtemperature, VSWR, and overdrive faults. The board also provides connections to the front panel meter for monitoring the AGC, % Reflected Power, % Output Power, and the power supply voltage.

A –12-VDC enable is applied to the board at J4-1 from the transmitter control board in the UHF exciter tray. The enable causes the J-FET Q5 to be biased off, making the drain to go high; the high is applied to Q4, which is biased on. The drain of Q4 goes low and lights the green Enable LED DS4 on the front panel. The high at the drain of Q5 is also applied through CR5 to J4, pin 7, which is a high enable, to the +26-VDC switching power supply switching it on.

If there is an overtemperature fault, which is a low applied to J4, pin 3, the low connects through CR4 and overrides the high enable, switching off the switching power supply. As long as the fault is present, the switching power supply is off and the red Overtemperature LED DS3 on the front panel is lit.

4.3.11.1 Phase Control

The phase control pot on the front of the tray connects to J8-1 (+26 VDC), J8-3 (phase I/P), and J8-4 (RTN) on the board. The phase-control output connects from J7 on the board to the input of the phase-control circuit on the variable gain/phase board (1265-1425).

4.3.11.2 Automatic and Manual Gain Control Circuits

The amplifier control board contains the AGC function for the UHF amplifier tray in which it is mounted. An AGC reference-level input from the UHF exciter tray is applied to J3, pin 1, and is amplified by U3B. The output of U3B is connected to J5, which is wired to the front panel gain pot that sets the output power level of the tray when the AGC is in the Auto position. The voltage at the arm of the front panel gain pot is amplified by U2D and is compared to a sample of the output power of the tray in U2A. The error voltage from U2A is sent through Auto/Manual switch S1 to J10, which connects to the pin-diode attenuator circuit on the variable gain/phase board. A sample of the AGC voltage level is connected to position 1 on the front panel meter switch. The tray can also be operated in manual gain by switching S1 to the Manual position and adjusting R16 for the desired output power level.

FETs Q1 and Q3 delay and slowly reapply the AGC voltage to the variable gain/phase board when the system is switched on or when the board is switched from Auto to Manual (or back) to prevent the overdriving of the tray.

4.3.11.3 Overdrive Circuit

A sample of the output of the single stage amplifier assembly, class A, from the coupler board assembly connects to J11 on the amplifier control board. The sample is peak detected by CR7 and U3A and the output is connected to U3D. If the input drive level increases above the overdrive threshold reference set by R71, which is the drive level needed to produce 110% output power, the output of U3D goes high and is split three ways. One of the highs is connected through R38 and CR3 to U3C, causing its output to go high and lighting the red Overdrive LED DS2 on the front panel. Another of the highs is connected through R74 and R75 to Q6, which is biased on and causes its output to go low. The low is connected through J10 to the variable gain/phase board and cuts back its output power.

The final high from U3D is connected through CR2 and R37 to U1D, which is biased on, and causes its output to go high. The high is connected to U2A, whose output decreases and cuts back the output power. If this path is not present, the AGC, because the forward power decreases, will try to drive the variable gain/phase board harder, creating a positive feedback loop that could damage the amplifier tray.

4.3.11.4 Metering Circuits

The +26 VDC that is connected to the board from the switching power supply is applied to jack J6, pin 1, of the board and connected through R63, R96, R66, R65, and R76 to the front panel meter for monitoring. R65 can be adjusted to calibrate the voltage reading to +26 VDC on the front panel meter. This calibration was completed at the factory and should not need to be adjusted at this time.

A forward power sample of the output of the tray is applied to jack J1-1 and J1-2 of the board from the dual peak detector board, single supply. The forward power sample is connected through R1 and R2 to U1A, a buffer amplifier. The output of U1A is split, with one part going to the AGC circuits, another sample connected to J1-5 for remote metering, and the final sample applied to the meter at position 3 on S2, the front panel meter switch. R2 can be adjusted to calibrate the % Forward Power indication on the front panel meter.

A sample of the reflected power output of the tray is applied to jack J2-1 and J2-2 of the board from the dual peak detector board, single supply. The reflected power sample is connected through R21 and R22 to U1B, a buffer amplifier. The output of U1B is split, with one part going to the VSWR threshold circuit, another sample connected to J2-5 for remote metering, and the final sample applied to the meter at position 2 on S2, the front panel meter switch. R22 can be adjusted to calibrate the % Reflected Power indication on the front panel meter.

A sample of the AGC voltage level at R20 on the board is connected through a divider network consisting of R87, R88, R19, and R18 to the meter at position 1 of S2, the front panel meter switch.

4.3.11.5 Operational Voltages

The voltage input to the board is +26 VDC from the switching power supply. The +26 VDC connects to the board at J6-1 and is wired to U4, which is a 3-terminal regulator IC that takes the +26 VDC input and produces the +12 VDC needed for the operation of the board.

The +12 VDC from U4 is connected through CR6 to U5, which is a +5-VDC regulator that takes the +12 VDC input from U4, or the transmitter control board in the UHF exciter tray, through J6, pin 3, and produces a +5-VDC output that is applied to the rest of the board. This +12 VDC is connected to U5, a regulator IC, which produces a +5-VDC output that is applied to the Enable and Overtemperature LEDs that operate even when the +26-VDC input to the board from the switching power supply is removed.

4.3.12 (A4-A1) Single Stage Amplifier Assembly, Class A; Appendix D)

The single stage UHF amplifier assembly, class A is made from the generic single stage amplifier board, class A (1265-1415). The assembly uses a single PTB20101 Ericsson device, made up of two transistors in parallel, and operating class A to amplify the signal by approximately +11 dB. Bias adjust pot R6 sets the operating current for Q1.

4.3.12.1 Q1 and Associated Circuitry

The RF input signal connects to SMA jack J1 on the board. The RF input is applied through an AC coupling and DC blocking capacitor (C1 to L1) and associated circuitry to form a balun. The balun converts the input signal from a 50-Ω unbalanced impedance to a 12.5-Ω balanced impedance configuration with the two outputs, applied to the bases of Q1, 180° out of phase with each other. C3, C4, C6, and C5, which can be adjusted for peak output, are for impedance matching to the input of the parallel transistors that make up Q1. The base circuit is RF bypassed by C2, C7, C17, and C29.

The collectors are impedance matched to 12.5Ω by C22, C23, and C19, which can be adjusted for peak output with the best linearity. C25 provides AC coupling and DC blocking for the output signal to SMA RF output connector J2. L2 and associated circuitry form a balun that transforms the two balanced signals back to a single, unbalanced 50-Ω impedance output. The collector circuit is RF bypassed by C9, C12 to C15, C18, C21, C24, C26, C30, and C31.

The +26 VDC needed for biasing Q1 is applied to E1, which is the high side of A4-A4. E1 is a .5-Ω/2-watt external metering resistor that is mounted on the heatsink next to the single stage amplifier assembly. The metering resistor is in the collector circuit of the RF transistor, Q1, and provides the main current path for Q1. The base bias applied to Q1 is supplied through R11, R4, R2, and R3.

The collector bias voltage drop across the A4-A4 metering resistor is in parallel with

the branch consisting of R10 and DS1, a green LED current indicator; as a result, it has the same voltage across it. The collector bias voltage drop biases on the green LED DS1. The current flow through R10 and DS1 gives a visual indication of the current draw of Q1 by the relative brightness of DS1. The higher the collector current of the transistor, the larger the voltage drop across the metering resistor. This, in turn, increases the voltage across DS1 and R10. This greater voltage level increases the current flow through them and increases the brightness of DS1. The opposite occurs when the collector current decreases.

The use of an opto-isolator (U1) allows no direct connection between the base and collector-biasing circuits, other than R11, the 200-Ω/5-watt control resistor that determines the actual base current flowing in Q1. R11 provides the primary current path from the collector circuit to the base of Q1. If there is no current flowing initially through Q1, R11 provides a substantial amount of base drive. When the collector current of Q1 increases to the desired operating level, the opto-isolator LED, which is across U1, is turned on. The turn-on point, or threshold, is set by the voltage-divider network that consists of R7, R9, and adjustable resistor R6. R6 is adjusted to set up the operating current at 5 amps.

When the opto-isolator LED turns on, it causes the transistor portion to also turn on. When the transistor portion turns on, it biases on Q2, which acts as a shunt regulator for the base current of Q1. Negative feedback for the circuit is preset so that if Q1 draws more than the desired amount of collector current, the voltage drop across A4-A4, the metering resistor, becomes greater than normal. This increase causes the voltage across the opto-isolator to increase; as a result, the opto-isolator LED is brighter than normal and forward biases Q2 even more. This action tends to shunt the available current that was fed through R11 and Q1 to flowing more through Q2, from collector to the emitter ground, setting up the negative feedback path. The negative feedback tends to stabilize the current flow through Q1. Capacitor C8 provides an active filtering action for this current source, which provides an improved response in Q1 during the vertical interval average current changes that take place.

4.3.13 Generic Single Stage Amplifier Board, Class A (1265-1415; Appendix D)

The generic single stage UHF amplifier board, class A, is used as the basic board in building the low-band single stage amplifier assembly, class A (1265-1418); the mid-band single stage amplifier assembly, class A (1265-1416); and the high-band single stage amplifier assembly, class A (1265-1417), an aluminum enclosure in which the dual stage amplifier board (1227-1501) is mounted. The assembly provides RFI and EMI protection for the amplifier board.

Mounted on the generic board are the components that have no frequency-determining factors. The low-band, mid-band, and high-band assemblies are produced by adding the specific frequency-related components to the generic board to make the specific frequency assembly.

4.3.14 (A2) Variable Gain/Phase Board Enclosure (1265-1426; Appendix D)

The variable gain/phase enclosure assembly provides EMI and RFI protection for the variable gain/phase board (1265-1425) that is mounted inside of the assembly.

The RF input to the assembly is at SMA jack J1 and the RF output is at SMA jack J2. There are two control inputs that connect to the assembly: the attenuator bias input and the phase control input. The attenuator bias input from the

amplifier control board connects to FL4 and FL5 on the assembly and is wired to J5 on the board. The phase control input from the amplifier control board connects to FL2 and E1 on the assembly and is wired to J4 on the board. The input fault to the amplifier control board connects to FL3 on the assembly and is wired to J6-1 on the board. E1 on the assembly connects to J3-4 on the board.

The +26 VDC needed to operate the board connects to FL1 on the assembly that is wired to J3-3 on the board.

4.3.15 (A2-A1) Variable Gain/Phase Board (1265-1425; Appendix D)

The variable gain/phase board provides the circuits that adjust the phase and the gain of the RF signal for the amplifier tray in which it is mounted.

The RF input signal at J1 is split, with one output connected to a detector circuit consisting of C8, CR4, and U3A. This detected level is then applied to comparator U3D, which provides a high output when the input signal level drops below a threshold set by R16, R17, and CR5. This high is applied to the red Input Fault LED DS1, which lights to indicate an input fault. DS1 can be seen through the hole in the lid on the variable gain/phase Assembly. The high is also connected to the gate of Q1, which biases it on and causes its drain to go low. The low is applied to the pin-diode attenuator circuit consisting of CR1, CR2, and CR3. The low to CR3 decreases the current through it and increases its resistance, decreasing or completely shutting off the RF that flows through it.

The other output of the RF input signal from J1 is connected through C1 to a voltage-controlled pin-diode attenuator circuit consisting of diodes CR1, CR2, and CR3. The diodes are pin diodes in a pi-type configuration whose resistance varies inversely with the DC current flow through them.

As the AGC voltage, the attenuator bias that is applied to J5 increases and CR3 is forward biased even more. This increases the current flow through it by decreasing its resistance; the RF signal that flows through it increases in level. CR1 and CR2 have less current through them; this raises their resistance, causing the RF signal that is applied to them to decrease in level.

The three diodes form a pi-type attenuator whose attenuation decreases with the increasing AGC voltage. U4 provides amplification, approximately 8 dB, of the RF signal before it is connected to the phase-shifter circuit. The phase-shifter circuit consists of L1, C16, C17, CR7, and CR8. L1 is a 90°, 2-way splitter. The signal at pin 1 of L1 is split and applied to pins 2 and 4. The signal reflects off CR7 and CR8 and is passed to pin 3. The phase shift between pins 1 and 3 changes with the voltage applied across CR7 and CR8. This voltage is controlled by an external phase-adjust pot that connects to J4. The +26 VDC from the external switching power supply is used as the reference that is applied to the phase-control pot. The IC U2 provides approximately 10 dB of gain at the output of the phase-shifter circuit that connects to two class A amplifier stages, Q2 and Q3, with a total gain of approximately 20 dB.

The first amplifier stage, Q2, is biased at a collector current of approximately 100 mA. This current is set by R29, R30, VR1, and Q2. VR1 forces the voltage at the collector to stay at 8.9 VDC. This biases on Q2 and draws enough current through R29 and R30 to keep the collector voltage at 8.9 VDC. The amplified output connects to the second amplifier Q3. The bias circuit for Q3 works in a manner similar to the bias circuit for Q2. VR2 and VR3 maintain a collector voltage of 21 VDC, while R36 and R37 limit the collector current to 650 mA.

The output connects to J2 on the board. A sample of the output is detected by CR10 and connected to TP4. A DVM can be connected to TP4 to give a voltage indication of the RF output level.

The +26 VDC connects to the board at J3-3 and is split, with one half connected to the two, class A amplifier circuits. The other half of the +26-VDC input is filtered, isolated by L4 and C13, and connected to U1. U1 is a +12-VDC regulator IC that produces the +12 VDC needed to operate the ICs on the board.

4.3.16 (A5-A6) 4-Way Combiner Assembly; Appendix D)

The 4-way combiner assembly contains a 4-way combiner board. The 4-way combiner board is made up of three 2-way wilkinson stripline combiners.

Two of the RF inputs to the board are soldered directly to the inputs of a 2-way combiner that contains R5. R5 is a balancing resistor that dissipates any RF due to mismatching in the combiner. The other two RF inputs are soldered directly to a 2-way combiner that contains R6. R6 is a balancing resistor that dissipates any RF due to mismatching in the combiner. The outputs of the two input 2-way combiners connect to a third 2-way combiner that contains R7. R7 is a balancing resistor that dissipates any RF due to mismatching in the combiner. The output of the third combiner is connected to the output of a 4-way combiner board that is cabled to an external circulator.

A directional coupler is built into the RF output circuit on the 4-way combiner board to provide a forward power sample at J1 that is -40 dB down from the level of the RF output signal.

A reject power sample from the circulator is fed to reject sample input jack J2 on the 4-way combiner board. A directional coupler is built into the reject sample circuit to provide a signal at J3 that is -40 dB down from the level of the reject power sample.

Chapter 5
Detailed Alignment Procedures

This transmitter was aligned at the factory and should not require additional alignments to achieve normal operation.

This transmitter operates using a single 64-QAM or 8-VSB digital input.

Check that the RF output at J2 of (A11) the coupler is terminated into a dummy load of at least 300 watts. While performing the alignment, refer to the Test Data Sheet for the transmitter and compare the final readings from the factory with the readings on each of the trays. The readings should be very similar. If a reading is way off, the problem is likely to be in that tray.

Switch on the main AC and the UHF exciter circuit breakers on the AC distribution panel behind the rear cabinet door.

5.1 (A4) UHF Exciter Tray (1294-1111; Appendix C)

The UHF exciter tray operates using a digital IF input from the DT1B modulator or other digital IF source.

The digital IF connects to J6 on the rear of the UHF exciter, which is cabled to the delay equalizer board, and then to the IF relays on the ALC board. To operate using the digital input, the modulator select must be present. The jumper must be connected from J11-10 and J11-28 on the rear of the UHF exciter or jumper W11 on J29 must be on pins 2 and 3.

To align the UHF exciter tray using the digital IF input, apply the digital IF, with the test signals used as needed, to the IF input jack (J6) on the rear of the tray. In addition, check that the modulator select is enabled by having W11 on J29 on the ALC board between pins 2 and 3.

Set the input matching jumper J9 to positions 1 and 2 for a 50-Ω input, or to positions 2 and 3 for 75Ω, on the delay equalizer board (1072090).

Table 5-1 shows the jumper positions for the 6-dB pad on the delay equalizer board for an input level of between 0 to -10 dBm.

Table 5-1. Jumper Positions on the 6-dB Pad

IF Input Range	6-dB Pad	W1 on J23 & W2 on J27	
-5 to 0 dBm	Enable	2-3	2-3
-10 to -5 dBm	Disable	1-2	1-2

The output level of the delay equalizer board should be -11 to -6 dBm with a response of 0.1 dB across the channel. The IF connects to the (A8) ALC board (1265-1305). The IF section of the UHF exciter tray includes adjustments for automatic level control (ALC), linearity (amplitude pre-distortion), and phase (phase change vs. level) pre-distortion for correction of the non-linearities of the RF amplifier trays. The upconverter section also includes adjustments to the local oscillator chain tuning and the local oscillator center frequency tuning. Both of these were completed at the factory and should not require adjustments at this time.

Move the Operate/Standby switch located on the UHF exciter tray to Standby. The setup of the RF output includes adjustments to the drive level of the four UHF amplifier trays, the adjustment of the linearity and phase predistortion to compensate for any nonlinear response of the amplifier trays, and also gain and

phasing adjustments to the four UHF amplifier trays.

Verify that all red LEDs on the ALC board are extinguished. The following details the meaning of each LED when illuminated:

- DS1 (input fault) – Indicates that either abnormally low or no IF is present at the input of the board
- DS2 (ALC fault) – Indicates that the ALC circuit is unable to maintain the signal level requested by the ALC reference. This is normally due to excessive attenuation in the linearity signal path or the IF phase corrector signal path, or that jumper W3 on J6 is in the Manual ALC Gain position.
- DS3 (modulation loss) – Indicates a loss of modulation at the input of the board
- DS4 (Mute) – Indicates that a Visual Mute command is present (DS4 is not used in this configuration.)
- DS5 (modulator enable) – Indicates that the modulator IF output is selected. This is only used if a receiver tray is present in the system. DS5 is always on with no receiver.

The ALC is muted when the transmitter is in Standby. To monitor the ALC, turn off the four amplifier on/off circuit breakers on the AC input assembly in the rear of the cabinet and switch the transmitter to Operate. Adjust the power adjust gain pot on the front panel of the UHF exciter tray to obtain +0.8 VDC on the front panel meter in the ALC position. On the ALC board (1265-1305), move the jumper W3 on J6 to the Manual position, between pins 2 and 3, and adjust R87 on the ALC board for +0.8 VDC on the front panel meter in the ALC position. Move the jumper W3 back to Auto, between pins 1 and 2, which is the normal operating position. The detected IF signal level at J19-2 of the ALC board is connected to the transmitter control board. This board distributes the level to the two UHF amplifier trays where it is used as a reference for the automatic gain control (AGC) in each amplifier tray.

5.1.1 Delay Equalization Adjustment

The procedure for performing a delay equalization adjustment for the UHF exciter tray is described in the following steps:

1. Set J19 to the proper position (for either a 50-Ω or 75-Ω input) and monitor the output of the board at J10 with a spectrum analyzer.
2. Bypass all attenuation and equalizer sections, except delay equalizer #1. With W12 removed, tune L30 for the proper center frequency as shown in Table 5-2. Install W12 on J22 and adjust L21 and C43 for the best frequency response across the band. Jumper in attenuator equalizer #1.
3. Pull W14 from J26 and adjust L29 for the proper center frequency. Install W14 and adjust L18 for the best frequency response.
4. Repeat Steps 2 and 3 for each delay/attenuation equalizer while tuning the proper inductor for each section.
5. After all five delay/attenuation equalizers have been adjusted according to Table 5-2, individually jumper in all of the sections and fine tune, as needed, for the best group delay and frequency response.

Table 5-2. Center Frequencies for the Delay Equalizer Sections

DELAY EQUALIZER SECTION	CENTER FREQUENCY
1	46.5 MHz
2	44 MHz
3	44 MHz
4	41.5 MHz
5	44 MHz

5.1.2 IF Phase Corrector Adjustment

As shipped, the exciters were preset to include linearity (gain vs. level) and phase pre-distortion. The pre-distortion was adjusted to approximately compensate the corresponding non-linear distortions of the amplifier trays.

Locate (A9) the IF phase corrector board (1227-1250) mounted in the UHF exciter tray. Because the amplitude correction portion of the board is not utilized in this configuration, the jumper W3 on J10 should be in the disable position and R35 and R31 should be fully counter-clockwise (CCW). R68 is the range adjustment and should be set in the middle. The phase correction enable/disable jumper W2 on J9 should be in the Enable position to ground.

Set up a spectrum analyzer with 30 kHz resolution bandwidth and 30 kHz video bandwidth to monitor the intermodulation products of the RF output signal. A typical digital spectrum is shown in Figure 5-1. There are three corrector stages on the IF phase corrector board, each with a magnitude and a threshold adjustment which are adjusted as needed to correct for any intermod problems. Adjust the R3 threshold for the cut in point of the correction and the R7 magnitude for the amount of the correction that is needed. The jumper W1 on J8 is set to give the desired polarity of the correction shaped by the threshold R11 and magnitude R15 adjustments. After setting the polarity, adjust the R11 threshold for the cut in point of the correction and the R15 magnitude for the amount of the correction that is needed. Finally, adjust the R19 threshold for the cut in point of the correction and the R23 magnitude for the amount of the correction that is needed. The above pots are adjusted for the greatest separation between the digital signal and the intermod at the channel edges.

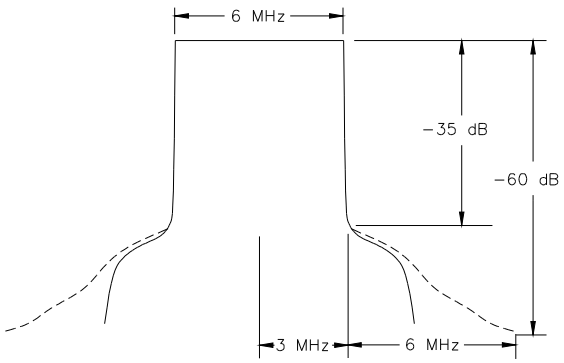

Figure 5-1. Typical Digital Spectrum

5.1.3 (A15-A1) UHF Generator Board (1565-1109)

The (A15-A1) UHF generator board is mounted in (A15) the UHF generator enclosure. This procedure should be performed to align this board.

In the Manual Adjust position, W1 on J4 on (A13) the PLL board (1286-1104) must be moved for –2.5 volts.

Connect J1, the sample output of the section of the UHF generator board, to a spectrum analyzer, tuned to the crystal frequency, and peak tuning capacitors C6 and C18 for maximum output. Also tune L2 and L4 for maximum output. The output level should be about +5 dBm. The channel oscillator should maintain an oven temperature of 50° C.

If a spectrum analyzer is not available, connect a digital voltmeter (DVM) to TP1 on the UHF generator board. Tune capacitor C32 for maximum voltage at TP1.

Connect J2, the sample output of the channel oscillator, to a suitable counter and tune C11, the coarse adjust, to the crystal frequency. The fine frequency is controlled by the external PLL circuit when in the Auto mode.

Caution: Do not repeak C32. This can change the output level.

Connect a spectrum analyzer to J2, the output jack of the board.

Tune C32, C34, C38, C40, C44, and C46 for maximum output.

Re-adjust all of the capacitors to minimize the seventh and the ninth harmonics of the channel oscillator frequency. They should be down at least -30 dB without affecting the output of the UHF generator board.

If a spectrum analyzer is not available, a DC voltmeter can be used. When a voltmeter is used, the harmonic frequencies must be minimized to prevent interference with other channels.

While monitoring each test point with a DC voltmeter, maximize each test point by tuning the broadband multipliers in the following sequence:

- Monitor TP1 with a DVM and tune C32 for maximum (typical 0.6 VDC).
- Monitor TP2 and tune C34 and C38 for maximum (typical 1.2 VDC).
- Monitor TP3 and tune C40 and C44 for maximum (typical 2.0 VDC).
- Monitor TP4 and tune C46 for maximum.
- Repeak C40 and C38 while monitoring TP4 (typical 3.5 VDC).
- The typical output level is +15 dBm.

5.1.4 (A14-A1) 10-MHz Reference Generator Board (1519-1126)

Monitor J1 with a spectrum analyzer. Adjust C12 for a maximum 10-MHz signal.

Attach a frequency counter. Tune C3 for a coarse frequency adjustment close to 10 MHz and C2 for exactly 10 MHz. Re-adjust C12 for peak signal amplitude at J1 using the spectrum analyzer. Adjust R15 to maintain a constant crystal temperature of 50° C.

5.1.5 (A13) PLL Board (1286-1104)

With W1 on J4-2 and J4-3, adjust R12 for –2.5 volts on J6-2. Adjust C11 on the (A8-A1) UHF generator board (1565-1109) for the correct channel oscillator frequency. Monitor J10 on the board. Install jumper W1 between J4-1 and J4-2. With switches SW1, SW2, and SW3 in the positions shown in Table 7-1 (refer to the PLL board schematic [1286-3104]), the PLL Unlock LED should go out.

Table 5-3. Switch Positions

SWITCH	POSITION
SW1-8	N5
SW1-7	N4
SW1-6	N3
SW1-5	N2
SW2-8	N1
SW2-7	N0
SW2-6	A5
SW2-5	A4
SW3-8	A3
SW3-7	A2
SW3-6	A1
SW3-5	A0

Table 7-2 shows the proper switch positions according to channel frequencies.

Note: N7 and N6 are fixed values and can not be programmed.

Table 5-4. Switch Positions for Channel Frequencies

CHANNEL	FREQUENCY (MHz)	N	N7-N0	A	A5-A0
14	517	64	01000000	40	101000
15	523	65	01000001	24	011000
16	529	66	01000010	8	001000
17	535	66	01000010	56	111000
18	541	67	01000011	40	101000
19	547	68	01000100	24	011000
20	553	69	01000101	8	001000
21	559	69	01000101	56	111000
22	565	70	01000110	40	101000
23	571	71	01000111	24	011000
24	577	72	01001000	8	001000
25	583	72	01001000	56	111000
26	589	73	01001001	40	101000
27	595	74	01001010	24	011000
28	601	75	01001011	8	001000
29	607	75	01001011	56	111000
30	613	76	01001100	40	101000
31	619	77	01001101	24	011000
32	625	78	01001110	8	001000
33	631	78	01001110	56	111000
34	637	79	01001111	40	101000
35	643	80	01010000	24	011000
36	649	81	01010001	8	001000

CHANNEL	FREQUENCY (MHz)	N	N7-N0	A	A5-A0
37	655	81	01010001	56	111000
38	661	82	01010010	40	101000
39	667	83	01010011	24	011000
40	673	84	01010100	8	001000
41	679	84	01010100	56	111000
42	685	85	01010101	40	101000
43	691	86	01010110	24	011000
44	697	87	01010111	8	001000
45	703	87	01010111	56	111000
46	709	88	01011000	40	101000
47	715	89	01011001	24	011000
48	721	90	01011010	8	001000
49	727	90	01011010	56	111000
50	733	91	01011011	40	101000
51	739	92	01011100	24	011000
52	745	93	01011101	8	001000
53	751	93	01011101	56	111000
54	757	94	01011110	40	101000
55	763	95	01011111	24	011000
56	769	96	01100000	8	001000
57	775	96	01100000	56	111000
58	781	97	01100001	40	101000
59	787	98	01100010	24	011000
60	793	99	01100011	8	001000
61	799	99	01100011	56	111000
62	805	100	01100100	40	101000
63	811	101	01100101	24	011000
64	817	102	01100110	8	001000
65	823	102	01100110	56	111000
66	829	103	01100111	40	101000
67	835	104	01101000	24	011000
68	841	105	01101001	8	001000
69	847	105	01101001	56	111000

5.2 (A6 and A7, A8 and A9 with upgrade) UHF Amplifier Trays (1294-1112, 1294-1113 or 1294-1114; Appendix C)

When testing the UHF amplifier trays, the other circuit breakers on the AC distribution panel, and mounted toward the rear of the cabinet, should be turned off. Circuit breaker CB3 applies power to (A6) the UHF amplifier tray from J5 on the AC distribution system. Circuit breaker CB4 applies power to (A7) the UHF amplifier tray from J6 on the AC distribution system. After upgrade, CB5 applies power to (A8) the UHF amplifier tray from J7 on the AC distribution system and circuit breaker CB6 applies power to (A9) the UHF amplifier tray from J8 on the AC distribution system.

The UHF amplifier tray should be turned on into a dummy load of at least 300 watts to verify that the tray is functioning. Prior to testing, disconnect the amplifier tray at the UHF tee and connect it to a dummy load of at least 300 watts. Preset S1, the AGC switch on

(A8) the amplifier control board (1265-1414), to the AGC On position.

To align (A6) the UHF amplifier tray, switch on CB3 on the AC distribution panel. Move the transmitter Operate/ Standby switch on the UHF exciter to Operate and observe the power supply metering position on the UHF amplifier tray. It should read +26.5 VDC when the tray is switched on and the transmitter is in Operate. The (A12) ASTEC America +26V/2000W switching power supply (VS3-L6-B6-21) is factory set for the +26.5 VDC and has no customer-needed adjustments.

Switch the tray to the % Output Power Meter position and adjust the front panel gain pot on that amplifier tray to 100% on the meter. Back off the gain pot to the reading on the Test Data Sheet. Switch the transmitter to Standby and reconnect the UHF amplifier tray.

To align (A7) the UHF amplifier tray, switch off CB3 and switch on CB4 on the AC distribution panel. Move the transmitter Operate/Standby switch on the UHF exciter to Operate and observe the power supply metering position on the UHF amplifier tray. It should read +26.5 VDC when the tray is switched on and the transmitter is in Operate. The (A12) ASTEC America +26V/2000W switching power supply (VS3-L6-B6-21) is factory set for the +26.5 VDC and has no customer-needed adjustments.

Switch the tray to the % Output Power Meter position and adjust the front panel gain pot on that amplifier tray to 100% on the meter. Back off the gain pot to the reading on the Test Data Sheet. Switch the transmitter to Standby and reconnect the UHF amplifier tray.

Switch the transmitter to Operate. The output power reading on the front panel meter of UHF exciter should be 100%. Check that the ALC voltage, as read on the front panel meter, is set to .8V. The voltage can be adjusted by using the power screwdriver adjust pot on the front panel of the UHF exciter tray. The amplifier tray can then be adjusted as needed to achieve the 100% output. As shipped, the exciter was preset to include linearity (gain vs. level) and phase (phase vs. level) pre-distortion. The pre-distortion was adjusted to approximately compensate the corresponding non-linear distortions of the amplifier. Move the jumper W1 on J4 of the ALC board to the corrector enable position. Refer to the Test Data Sheet for the final test readings on the amplifier tray. Adjust the phase pot on the front panel of the UHF amplifier tray to obtain maximum % Output Power on the front panel meter of the UHF exciter. Adjust the gain pot on the UHF amplifier tray to obtain 100% Output Power on the front panel meter of the UHF exciter.

5.2.1 Phase and Gain Adjustment of the UHF Amplifier Trays

The following procedure was completed at the factory and should only be repeated if one of the UHF amplifier trays is replaced.

Preset the phase and gain potentiometer on each UHF amplifier tray full CCW. Turn off the A6, A7 amps at the AC distribution panel. Switch the transmitter to Operate and adjust the gain pot on each tray for 25% Output Power. Adjust the phase control CW on the left, bottom UHF amplifier tray. If the % Visual Output Power goes up, continue to adjust the phase control until either the peak is reached or the end-of-travel is reached. If the % Output Power goes down, reset the phase control on the UHF amplifier tray full CCW and repeat the above procedure with the phase control of the other amplifier tray.

If the end-of-travel is reached on the phase adjust, reset the phase control CCW and add a 2-inch length of cable to the output of the (A5) splitter module that connects to the affected UHF amplifier tray at J1. Readjust the phase

of that tray until a peak is reached or until the end-of-travel is achieved. If the end-of-travel is reached, repeat the above procedure, replacing the 2-inch length of cable with a 4-inch length of cable. Once a peak is reached, move the phase control that is full CCW up two turns and repeat it using the phase control on the other tray. This allows both trays to have some range of adjustment.

5.3 (A19) 8-VSB Digital Modulator (1075164; Appendix C)

The connections to the 8-VSB modulator are made through the rear panel except for the IF sample output, which is made through the front panel. These connections are shown in Table 5-3.

Table 5-5. 8-VSB Modulator Connections

REFERENCE	LABEL	FUNCTION
J1	IF O/P	IF output from the modulator; nominal output power level is –18 dBm
J2	10 MHz I/P	10 MHz reference input; signal level is 0 to +3 dBm
J3	MPEG I/P	SMPTE 310M input; only used when the MPEG source is in accordance with the SMPTE 310M specification
-	ECL	37-pin D connector used to interface to serial ECL MPEG signals. The pinout of this connector is defined in the setup and operation procedures in Chapter 2 of this manual. This input is used only when SMPTE 310M signals or serial TTL signals are not provided.
-	TTL	25-pin D connector used to interface to serial TTL MPEG signals. The pinout of this connector is defined in the setup and operation procedures in Chapter 2 of this manual. This input is used only when SMPTE 310M signals or serial ECL signals are not provided.
-	IF SAMPLE	Provides a front panel sample of the IF output
-	PORT A	9-pin, D, RS-232 interface used to load the preset coefficients and is also used as an interface to the demodulator when ADAPTIVE is implemented.
-	PORT B	9-pin, D, RS-232 interface used to monitor the operation of the modulator via a laptop computer.
-	REMOTE	15-pin, D interface that provides hard-wired indications of the front panel LEDs. All of the lines are active low. The available signals are: • Pin 6 – MPEG present • Pin 7 – Reference present • Pin 8 – Ref PLL locked • Pin 9 – Power present • Pin 5 – Ground

5.3.1 (A11) VSB Modulator Interface Board (1561-1205; Appendix D)

The VSB modulator interface board interfaces the external MPEG source to the 8-VSB symbol generator board. The interface board receives MPEG either at J11 in SMPTE format, at J1 in differential emitter-to-coupler logic (ECL) format, or at J2 in differential TTL format, and converts it to single-ended transistor-to-transistor (TTL) in the form of data (J10) and a clock (J3). The jumpers J13 and J14 on this card select between the various input formats. These jumper settings are outlined in the discussion on the 8-VSB modulator in Chapter 2 of this manual. Jumpers J4 through J7 were used during the initial design of the board and have been preset at the factory. These four jumpers should all be placed in positions 1-2 with the exception of jumper J6, which should be placed in position 2-3. Jumper block J15 was also used in the initial design of the board and should be set to position 3.

In addition, if required, this card can be used for a future parallel interface that is either in a TTL or an ECL format. The interface will utilize the PLL Locked LED at the bottom, right-hand corner of the board; this LED will not illuminate with the existing interfaces. Test connector J8 will also be used, as needed, for future parallel interfaces.

5.3.2 (A4) VSB Symbol Generator Board (1049396; Appendix D)

The symbol generator board takes the MPEG data and clock signals from the interface card and performs the digital signal-processing functions outlined in the ATSC specification for 8-VSB modulation. These functions involve data randomization, the Reed Solomon encoder, data interleaver, and the trellis encoder. These functions are implemented in programmable logic chip U1 on the symbol generator card. In addition, this card performs the linear equalization function. This function is implemented in U14.

The output of this card is symbol data that has been equalized. The data is available at J25 in the form of ten data lines and a 32.28-MHz clock. In addition, the microcontroller data and address bus is available at this output connector.

The LCD display and the switch panel are also controlled by the symbol generator card. The interface to the LCD display is provided at J20 and the interface to the switch panel is provided at J21. The RS-232 interface to Port A is provided at J19 on this card. This interface is wired to the rear of the tray and is used to load the linear equalizer and perform adaptive equalization. The Port B serial interface is wired through connector J4 on this card.

Note: The symbol generator board contains jumper blocks that have been set at the factory. No additional alignment is required to achieve normal operation.

In the event that the board becomes incorrectly aligned, the jumpers on the card should be placed in the configurations shown in Table 5-4.

Table 5-6. Jumper Configurations for the Symbol Generator Board

REFERENCE DESIGNATOR	FUNCTION	SETTING
J5	19.39M/2.42M clock select: Used for test purposes only. 1-2 selects 2.42 MHz, 2-3 selects 19.39 MHz	No jumper required
J8	/DPWEN, 2.69 MHz clock select: Used for test purposes only. 1-2 selects 2.69 MHz, 2-3 selects /DPWEN clock.	No jumper required
J11	10.76 MHz/32 MHz clock select: Used for test purposes only. 1-2 selects 32 MHz, 2-3 selects 10.76 MHz.	No jumper required
J23	External Reset	No jumper required
J24	Spare Input	No jumper required
J26	Impulse Select: Used for test purposes. 1-2 applies the output of the ATSC EPLD to the linear equalizer. 2-3 applies repetitive impulses to the equalizer so that the user can observe the impulse response of the equalizer.	1-2 is the setting for normal operation.
J27	Rounding Enable: 1-2 enables the rounding on the linear equalizer. 2-3 disables the feature.	1-2 is the setting for normal operation.
J28	Gain Select for the linear equalizer: 1-2 forces the linear equalizer to use the gain set by the DIP switch 2. 2-3 allows the linear equalizer to use the gain set by the microcontroller.	2-3 is the setting for normal operation.
J29	Clip Reset: Resets the clip detector in the linear equalizer. 1-2 allows the clip detector to reset itself. 2-3 holds the clip detector in constant reset.	2-3 is the setting for normal operation.
SW1	8-position DIP Switch: Used for testing. Position 1 has a dual function. It can establish the relationship between the clock and the data on the incoming MPEG source when the TTL or ECL interfaces are used.	Position1: Off when the data changes on the falling edges of the incoming clock. On when the data changes on the rising edge. Off is the normal setting Positions 2-8: All positions should remain off during normal operation.

REFERENCE DESIGNATOR	FUNCTION	SETTING
SW2	4-position DIP switch: Used to adjust the gain of the linear equalizer when J28 is set to 1-2. Divide – Sw 1,2 On, On – divide by 1 On, Off – divide by 2 Off, On – divide by 4 Off, Off – divide by 8 Divide – Sw 3,4 On, On – multiply by 1 On, Off – multiply by 1.25 Off, On – multiply by 1.5	Positions 1-4: All positions should remain off during normal operation.

The last adjustment on the symbol generator card is the LCD contrast. This potentiometer, R32, can be adjusted until the desired level of contrast appears on the front panel display.

5.3.3 (A5) VSB Filter Board (1561-1301; Appendix D)

The VSB filter board performs the digital pulse-shaping filter function of the ATSC specification. The board receives equalized symbol data at J1 and applies it to an in-phase (I) pulse-shaping filter and a quadrature (Q) pulse-shaping filter. The I filter is implemented in U1 and U2 and the Q filter is implemented in U3 and U4. The pulse-shaping filter outputs are applied to digital-to-analog (D/A) converters through jumper blocks J25 and J28. The output of the D/A converters is filtered to remove the 32.28-MHz converter update rate. The I data are available at J26 and the Q data are available at J29.

Note: The 8-VSB filter board contains jumper blocks and adjustment potentiometers which have been set at the factory. No additional alignment is required to achieve normal operation.

In the event that the board becomes incorrectly aligned, the jumpers on the board should be placed in the configurations shown in Table 5-5.

Table 5-7. Jumper Configurations for the VSB Filter Board

REFERENCE DESIGNATOR	FUNCTION	SETTING
J2, J3	Impulse Select/Clock Select: Used for board testing purposes. When both are placed in position 2-3, the impulse response of the I and Q filters appear at the I and Q even in the absence of any input to the board.	Both should be set to positions 1-2 for normal operation
J6-J9	Jumper Blocks: Used during initial integration and test.	No jumpers are required.
J10, J12	Gain Select: Selects between the gain set by the microcontroller or the gain set by the external settings. 1-2 selects external gain. 2-3 selects internal.	Both should be set to positions 1-2 for normal operation
J11, J13	External Gain: Sets the gain of the filters when J10 and J12 are in positions 1-2. Gain is as follows: J11 J13 Gain 1-2 1-2 1 1-2 2-3 2 2-3 1-2 4 2-3 2-3 8	Under normal operation, J11 should be 1-2 and J13 should be 2-3.
J14	Round: 1-2 disables the rounding feature. 2-3 enables the rounding feature.	2-3 is the setting for normal operation.
J15	Twos Compliment: Enables twos compliment data to be sent to the D/As. Position 1-2 enables twos compliment data.	2-3 is the setting for normal operation.
J16	Clock Invert: Inverts the incoming clock at J1. 1-2 inverts the clock.	1-2 is the setting for normal operation.
J17	External Reset: Resets the symbol generator card. Used for test only. 2-3 resets the board.	1-2 is the setting for normal operation.
J19	I Clip Reset: Position 2-3 resets the I clip detector.	1-2 is the setting for normal operation.
J19	Q Clip Reset: Position 2-3 resets the Q clip detector.	1-2 is the setting for normal operation.
J25	I Data: Passes the data to the D/A converters.	This jumper block is a dual-row, 12-location jumper block. Jumpers should be placed on the top 10 rows in normal operation.
J28	Q Data: Passes the data to the D/A converters.	This jumper block is a dual-row, 12-location jumper block. Jumpers should be placed on the top 10 rows in normal operation.

The potentiometers on this board consist of the I and Q gain and offset adjustments. Since the overall gain balance between the I and Q channels will be adjusted in the vector modulator, the gain is not critical. As a result, gain potentiometers R50 and R71 should be set to the middle of their range. The offset potentiometers are adjusted in the following order:

1. Power up the modulator with the test jumper placed in the enable position on the rear of the (A2) switch board.

2. Using the up arrow button, change the operating mode from NORMAL to CW ZERO POWER.

3. Remove the connector to J26 on the VSB modulator board. Connect a voltmeter to J26, with the positive lead connected to the center of the 3-pin connector and the negative lead connected to one of the outer pins.

4. Set the voltmeter to read in millivolts and adjust R47 until the voltmeter reads zero.

5. Repeat this procedure for J29 while adjusting R68.

6. Return all jumpers and connectors to the standard configuration.

This completes the I and Q offset adjustment.

5.3.4 (A2) Switch Board (1561-1202; Appendix D)

The switch board is mounted on the rear of the front panel. It houses the front panel pushbuttons for the LCD readout.

There is one jumper, J2, to enable or disable the TEST mode. The TEST mode enables several MPEG digital signals that are used for the test and the alignment of the tray. In order to enable the TEST mode, turn off the tray and move jumper J2 from position 1-2 to position 2-3.

Note: The tray must be turned off, jumper J2 moved back to the disable position (1-2), and the tray powered back up in order for the tray to be restored to the NORMAL mode.

5.3.5 (A7) Local Oscillator Board (1561-1203; Appendix D)

The local oscillator board does not have any adjustments for the VCXO oscillator; however, there are several jumpers and DIP switches on the board to set the PLL circuits.

Verify that jumpers J7 and J3 are in the 1-2 position. Jumper J3 is set based on the polarity of the VCXO that has been installed. The VCXO installed in the 8-VSB modulator requires that J3 be set in position 1-2. Jumper J7 is the most significant part of the divide ratio that determines the final local oscillator (LO) frequency. If J7 is in the 1-2 position, the MSB is set to 1. Using J7, along with SW1 through SW3, the LO frequency is determined from the following equation:

LO Frequency = 2*(Switch Setting+3)

or in terms of the switch setting:

Switch Setting = (LO Frequency/2)-3.

For the LO card to produce 46.690560 MHz, verify that DIP switches J7, SW1, SW2, and SW3 are set as shown in Table 5-6.

Table 5-8. DIP Switch Settings

J7	SW1	SW2	SW3 LSB
1	01100100	00111000	01111101

Once the DIP switches are set, and there is a 10-MHz reference source present at the rear of the tray, the board will begin the process of phase locking the VCXO. There are three amber LEDs on the board that indicate the progress of the PLL circuit. These LEDs have been designated Step 1, Step 2, and Step 3.

When the circuit begins the PLL process, Step 1 will illuminate. As the process continues, Step 1 extinguishes and Step 2 illuminates. Finally, Step 2 extinguishes and Step 3 illuminates. Once Step 3 extinguishes, the front-panel PLL Locked LED will illuminate within 30 seconds.

Note: The front panel PLL Locked LED may flicker once or twice before settling into lock; this is a normal condition. The frequency of the VCXO is 46.690560 MHz and can be monitored at the IF sample, J8, on the LO card.

5.3.6 (A6) VSB Vector Modulator Board (1520-1107; Appendix D)

The vector modulator board modulates the baseband 8-VSB signal coming from the VSB filter board with the LO supplied from the local oscillator card. The baseband signal consists of an I and a Q component. The I component enters the board at J3 and is frequency-response adjusted by C16. The DC offset of this signal path is set to zero with R5 and the gain of this path is adjusted using R32. This signal is then mixed at Z1 with a 46.49056-MHz local oscillator. In a similar fashion, the Q signal comes into the board at J11 and is frequency-response corrected with C43, offset adjusted with R78, and gain adjusted by R105. The Q signal is then mixed with the 46.69056-MHz local oscillator, which is 90 degrees out of phase with the local oscillator that is mixed with the I channel. The LO signals are generated by quadrature splitter U8.

After the baseband I and Q signals are mixed with the LO signals, they are combined with combiner Z2 to produce the final IF signal centered at 44 MHz. This signal is amplified with U2 and U3 to produce a nominal –18 dBm signal at J1. A sample of the IF signal is also provided at J2; a 50-Ω termination must be present at J1 before the signal from sample port J2 can be used. The gain of the final output can be adjusted using R3. The frequency response of the IF signal can be flattened using C19, C20, R29, and R30.

Note: The vector modulator board contains jumper blocks and adjustment potentiometers that have been preset at the factory. Because of this, no additional alignment is required to achieve normal operation.

In the event that the vector modulator becomes incorrectly aligned, the following steps can be used to align the board:

1. Power up the modulator with the test jumper placed in the Enable position on the rear of the switch board.

2. Using the up-arrow button, change the operating mode from NORMAL to CW ZERO POWER.

3. Using the MENU button, go to the INPUT SOURCE menu. Use the up-arrow button to select INTERNAL PRBS23 as the input source.

5.3.7 (A10) DC Power Supply Board (1047033; Appendix D)

The DC power supply board generates both the positive and negative 12 and 5 VDC and the positive 3.3 VDC at sufficient current levels to operate the other boards in the modulator tray. Visual indicators, using LEDs, are provided on the board to show the normal operation of each voltage regulator.

The DC outputs (+15, +5, and -15 VDC) from the switching power supply (1049886) are directed to jack J1. The voltages are then filtered by C1 to C6 and fed to voltage regulators U1 to U7. The outputs are protected from overcurrent conditions by the regulators. The regulators are designed to fold back the voltage if a short-circuit condition occurs externally and will continue to do so until the short is eliminated. If a short appears, the on-board LED associated with that regulator will extinguish with the loss of output.

5.3.8 (A8) VSB IF Filter Board (1047976; Appendix D)

The VSB IF filter board provides low-pass filtering for frequencies above 63 MHz.

The board receives the output IF signal from the vector modulator board at J1. The input signal is fed through the 50-Ω matching circuit of R1, R2, and R3. The signal is then filtered by low-pass filter circuit L1 to L5 and C2 to C6. The signal is amplified by U1 and fed to SMA connector J2. The signal is also fed through the IF sample circuit of U2 and associated components to J4, IF sample. This sample is fed to the front panel sample port.

The voltage to this board is supplied by an external +12 VDC source.

5.3.9 (A3) LED Board (1561-1204; Appendix D)

The LED board provides front panel verification of the status of the MPEG input signal, 10-MHz reference signal, and phase-locked status of the IF oscillator and the +5-VDC power supply.

DS1 is driven from the VSB modulator board and provides a constant +5 VDC to J1-1 and a logic low at J1-2 when the MPEG input signal is present. DS2 is driven from the local oscillator board and provides a constant +5 VDC and a logic low at J1-4 when the 10-MHz reference signal is present at the oscillator board. DS3 is driven from the local oscillator board and provides a constant +5 VDC and a logic low at J1-6 when the IF oscillator is phase locked. DS4 is driven from the +5-VDC source on the power supply board through J1-7.

5.3.10 Offset Adjust

1. Set gain potentiometers R32 and R105 to the center of their travel.

2. Remove the jumper that connects the center pins of J5 and J6. Connect a voltmeter to TP4.

3. Adjust R5 until less than 1 mV appears on the voltmeter. This sets the offset of the I channel to zero.

4. Remove the jumper that connects the center pins of J9 and J10. The voltmeter is placed on TP8.

5. Adjust R78 until there is less than 1 mV on the voltmeter. This sets the offset of the Q channel to zero.

5.3.11 Local Oscillator Leak-Through Adjustment

1. With the setup in the same configuration as it was at the end of step 5 of the Offset Adjust procedure, connect a spectrum analyzer to J5. Set the spectrum analyzer to look at the 44-MHz center frequency with a 15-MHz span.

2. Since the offset to the mixer is now zero, the output of the mixer that blends the in-band signal (0V) with the LO should now be zero. With the spectrum analyzer, adjust C29 and R58 until the local oscillator does not have a presence at 46.69056 MHz on the spectrum analyzer. This same process is repeated for the Q channel. The spectrum analyzer is connected to J9, and C32 and R79

are adjusted until there is no leak-through of the 46.69056 MHz on the spectrum analyzer.

5.3.12 I and Q Baseband Frequency Response Adjustments

1. With the setup in the same configuration as it was in step 3 of the Local Oscillator Leak-Through Adjustment procedure, move the spectrum analyzer back to J5.

2. Using the MENU button, go to the OPERATING MODE menu. Use the up arrow to select NORMAL.

3. Observe the spectrum analyzer until a 12 MHz-wide spectrum appears. Set the spectrum analyzer to read .2 dB/division on the vertical scale and turn the video averaging on to 200 averages or greater. Set the reference level so that the top of the spectrum is visible on the display. Some time may be required to allow the averaging feature to produce a spectrum.

4. Adjust C16 until the spectrum looks flat within .1 dB.

5. Repeat this process for the Q channel, connecting the spectrum analyzer to J9 and adjusting the frequency response at C43.

This completes the frequency-response adjustment.

5.3.13 Gain and Quadrature Adjustments

1. With the setup in the same configuration as step 5 of the I and Q Baseband Frequency Response Adjustments procedure, replace the jumpers that were removed on J5/J6 and on J9/J10. Connect the spectrum analyzer to J1, the IF output at the rear of the tray. A spectrum will be produced that is 12-MHz wide. Perform the gain and quadrature adjustments described in the next two steps to remove the upper 6 MHz of this spectrum.

2. Rotate quadrature adjust capacitor C27 until the upper 6 MHz of the spectrum is reduced as low as possible.

3. Adjust I channel gain potentiometer R32 until the upper 6 MHz of the spectrum is reduced as low as possible.

4. Repeat steps 2 and 3 until the right side of the spectrum is reduced as far as possible. When this is complete, the out-of-band on the right side should look similar to the out-of-band on the left side.

5.3.14 Output Level Adjust

The final output level of the modulator is set by R3. A spectrum analyzer with a power measurement capability, or a vector signal analyzer, can be used to adjust the output level. This level is set at the factory to a nominal –18 dBm.

At this point, the alignment of the modulator tray is complete. When the modulator tray has been aligned correctly, the out-of-band rejection should be at least 40 dB (typically 42 dB) and the signal-to-ratio should be at least 34 dB (typically 36 dB). If either of these specifications is not met, the steps described above for aligning the vector modulator should be repeated. When the desired modulator performance has been achieved, the test jumper on the (A2) switch board (1561-1202) should be returned to position 1-2 to disable the test modes. Power will need to be cycled off and back on to return the unit to the OPERATE mode.

5.4 Output Power Level

Using a forward-calibrated coupler and an HP power meter, or equivalent, adjust the output power for a reading of 500 watts out of the bandpass filter on the true average power meter. Adjust R28 on (A10) the visual/aural metering board in the exciter tray for 100% in the % Forward Output position. The aural power is not used; set the pots R20 and R51 on (A10) the visual/ aural metering board fully CCW.

Turn the power-adjust pot to 20% on the meter in the Forward Power position. Reverse the SMA cables on J1 and J3 of (A7) the visual/aural metering board (1265-1309) in the exciter tray assembly. Adjust R39 on the visual/aural metering board for a 20% reading in the Reflected Output Power position.

Adjust R22 on the transmitter control board (1265-1311) in the exciter tray until the VSWR LED just begins to light on the exciter front panel. Place the SMA cables on the visual/aural metering board in their original positions. The reflected output power is now calibrated.

This completes the detailed alignment procedures for the DT830A transmitter. If a problem occurred during the alignment, refer to the detailed alignment procedures for that tray for more information.

APPENDIX A

SAMPLE LOG REPORT SHEET

UHF Exciter

% Output Power (0-120)= _____% % Exciter (0-120)= _____%

ALC (0-1 V)= _____V% Reflected (0-120)= _____%

UHF Amplifier Trays

(A6)

AGC Voltage (0-10 V)= _____V

% Reflected Power (0-120)= _____%

% Output Power (0-120)= ___ _____%

Power Supply Voltage (0-30 V)= _____V

(A7)

AGC Voltage (0-10 V)= _____V

% Reflected Power (0-120)= _____%

% Output Power (0-120)= ___ _____%

Power Supply Voltage (0-30 V)= _____V

Date _____

Customer Name _____ Call Letters _____

Technician _____

APPENDIX B

TYPICAL OPERATIONAL READINGS

UHF Exciter

ALC=.8 VDC.

% Exciter=The level is as needed to attain 100% output power from the transmitter.

% Reflected=< 5%

% Output Power=100%

UHF Amplifier Trays

(A6)

AGC voltage=1 to 2 VDC

% Reflected=< 5% with one tray

% Output Forward=The level is as needed to attain 100% Output Power from the transmitter (150 watts)

Power supply=+26.5 VDC

(A7)

AGC voltage=1 to 2 VDC

% Reflected=< 5% with one tray

% Output Forward=The level is as needed to attain 100% Output Power from the transmitter (150 watts)

Power supply=+26.5 VDC

APPENDIX C

ASSEMBLY DRAWINGS

DT830A

APPENDIX D

SUBASSEMBLY DRAWINGS

APPENDIX E

DT830A SYSTEM SPECIFICATIONS