

User Manual Guide

Project Name: IMA3

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Revision History

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1. Introduction

IMA3 is a CAT-M1 (1 Mbps/1 Mbps DL/UL respectively) LTE modem which incorporates an application CPU subsystem and a host of peripheral interfaces and functions uniquely designed to address the power/performance/cost requirements of IoT and M2M applications. The chip is based on SDR-v3.0 (Software Defined Radio) architecture which offers OFDMA-related software based signal processing capabilities that significantly exceed traditional communications DSP cores, yet consumes a fraction of the power.

The CPU subsystem features a high performance MIPS MicroAptiv™ processor running a Linux OS with a variety of host interfaces including USB 2.0, I2C, SPI, and UART.

1.1. Abbreviation

Table 1. Pin Interface Family

Abbreviation	Definition
AC	Alternating Current
DC	Direct Current
ETSI	European Telecommunications Standards Institute
GND	GrouND
GPS	Global Positioning System
GNSS	Any single or combined satellite navigation system (GPS, GLONASS and combined GPS/GLONASS)
GPIO	General Purpose Input Output
I/O	Input/Output
IoT	Internet of Things
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound or Integrated Interchip Sound
IMS	IP Multimedia Subsystem
LGA	Land Grid Array
LTE	Long Term Evolution

M2M	Machine to Machine
Mbps	Megabits per second
MIPS	Millions of Instructions Per Second
N/A	Not/Applicable
OS	Operating System
OTA	Over The Air
PC	Personal Computer
PCM	Pulse Code Modulation
PIN	Personal Identification Number
PSM	Power Saving Mode
RRC	Radio Resource Control
SIM	Subscriber Identity Module
SMA	Surface Mount Antenna
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
UIM	User Identity Module
USB	Universal Serial Bus
Vref	Voltage reference
WCDMA	Wideband Code Division Multiple Access
WNC	Winstron NeWeb Corporation

1.2. Features

- 3GPP category support: LTE CAT-M1 with 1 Mbps for DL/UL
- Embedded 512Mbit LPDDR
- Embedded 256Mbit SPI NOR Flash
- Ultra-high performance enhanced SDR processor
- Embedded network processor with Linux OS
- Integrated PMU circuitry
- Integrated RTC support
- Interference Cancellation (INCA™) capability
- Optimized for the M2M and IoT markets
- Interfaces:
 - HS USB2.0 with integrated PHY
 - Dual UART interfaces (4 bit and 2 bit) for high-speed data transfer and diagnostic tools support
 - SPI master interface
 - Mobile LPDDR and PSRAM support
 - Serial NOR flash controller
 - USIM interface
 - I2S/PCM audio interface
 - GPIOs
 - One I2C interface (master mode)

2. Electrical Specifications

2.1. Interface pin assignments

2.1.1. LGA Pad Diagram

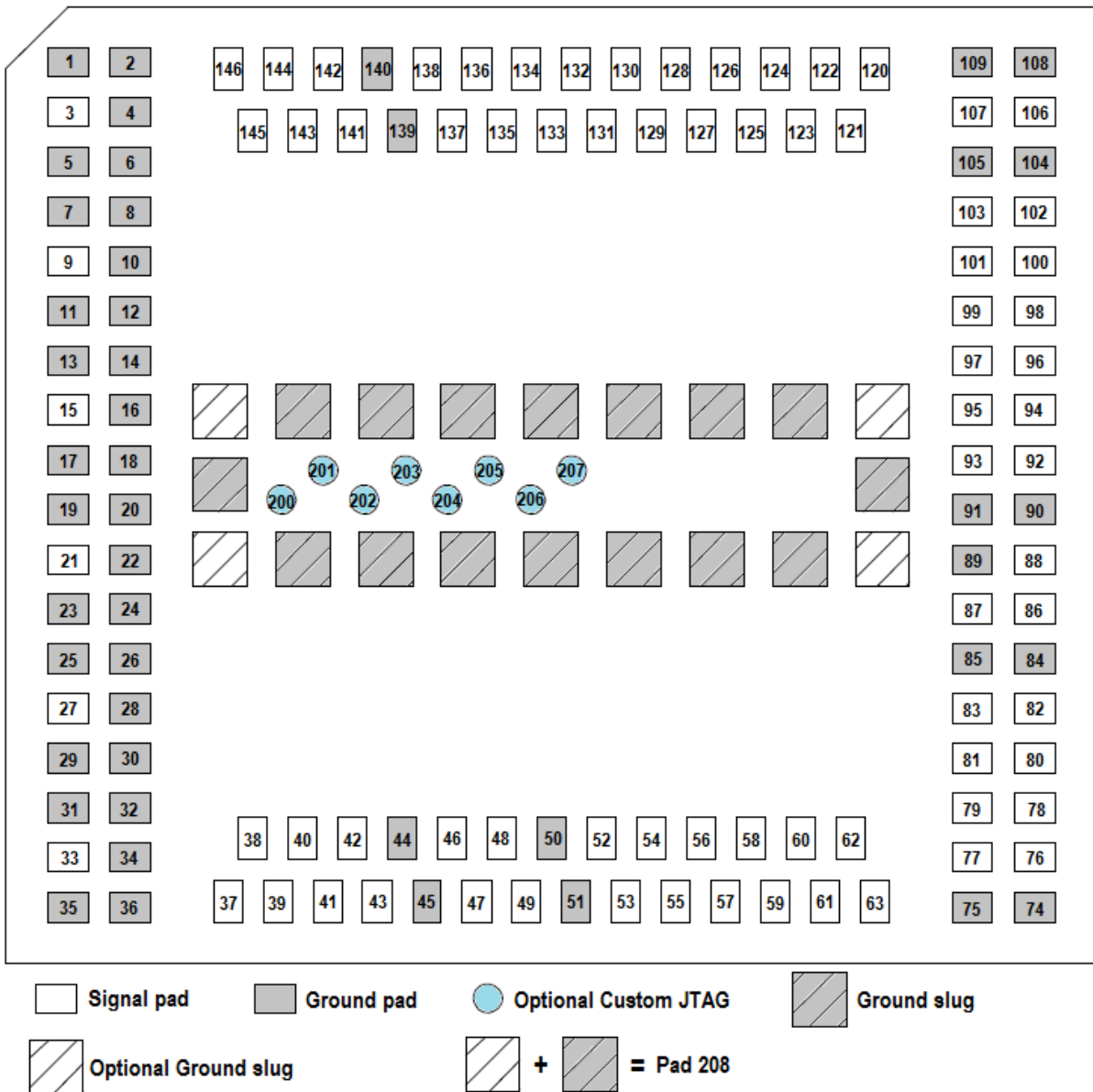


Figure 1. LGA pad diagram (top view)

2.1.2. Pin Assignments

I/O type description :

- AO : Analog Output
- AI : Analog Input
- DO : Digital Output
- DI : Digital Input

Table 2. Pin Interface Family

Interface Family	Signal Name	Description	I/O
RF Interfaces			
	RF_1	Main Antenna	AI/AO
	RF_2	Aux Antenna	AI
User Identity Module			
	UIM_VCC	UIM Power	DO
	UIM_DATA	UIM Data in/out	DI/DO
	UIM_CLK	UIM Clock	DO
	UIM_RESET	UIM Reset	DO
	UIM_DETECT	UIM Detect	DI/DO
Data Interfaces- USB2.0			
	USB_Dp	USB Data Positive	DI/DO
	USB_Dn	USB Data Negative	DI/DO
Data Interfaces- UART1			
	UART1_CTS	Clear To Send for UART 1	DI
	UART1_RTS	Request To Send for UART 1	DO
	UART1_RX	Receive for UART 1	DI
	UART1_TX	Transmit for UART 1	DO
Data Interfaces- UART2			
	UART2_RX	Receive for UART2	DI
	UART2_TX	Transmit for UART2	DO
Data Interfaces- I2C			
	I2C_SDA	I2C Data	DI/DO
	I2C_SCL	I2C Clock	DO

Data Interfaces- SPI			
	SPIM_MOSI	SPI Master Out Slave In	DO
	SPIM_MISO	SPI Master In Slave Out	DI
	SPIM_EN	SPI master interface enable	DO
	SPIM_CLK	SPI master interface clock	DO
Module Control and State Interfaces			
	WWAN_STATE	Wireless WAN Radio State	DO
	POWER_ON	Power On the module	DI
	WAKEUP_OUT	Module wakes up host OR GPIO	DO
	WAKEUP_IN	Host wakes up module OR GPIO.	DI
	RESET	Reset the module	DI
Power and GND			
	VREF	Reference Logic Voltage	AO
	VCC	Main Power	AI
	GND	Ground	AI
General Purpose			
	GPIO	General Purpose I/O	DI/DO
	ADC	Analog to Digital Convertor	AI
Audio- PCM/I2S			
	PCM_SYNC	PCM_SYNC	DI /DO
	PCM_IN	PCM_IN	DI
	PCM_OUT	PCM_OUT	DO
	PCM_CLK	PCM_CLK	DO

Table 3. Pin Assignments

Pin No.	Signal Name	Description	Voltage Levels (V)		
			Min.	Typ.	Max.
1	GND	Ground	-	0	-
2	GND	Ground	-	0	-
3	NC	NC	-	-	-
4	GND	Ground	-	0	-
5	GND	Ground	-	0	-
6	GND	Ground	-	0	-
7	GND	Ground	-	0	-
8	GND	Ground	-	0	-
9	NC	NC	-	-	-
10	GND	Ground	-	0	-
11	GND	Ground	-	0	-
12	GND	Ground	-	0	-
13	GND	Ground	-	0	-
14	GND	Ground	-	0	-
15	RF_1	Main Antenna	-	-	-
16	GND	Ground	-	0	-
17	GND	Ground	-	0	-
18	GND	Ground	-	0	-
19	GND	Ground	-	0	-
20	GND	Ground	-	0	-
21	RF_2	Aux Antenna	-	-	-
22	GND	Ground	-	0	-
23	GND	Ground	-	0	-
24	GND	Ground	-	0	-
25	GND	Ground	-	0	-
26	GND	Ground	-	0	-
27	NC	NC	-	-	-
28	GND	Ground	-	0	-
29	GND	Ground	-	0	-
30	GND	Ground	-	0	-

31	GND	Ground	-	0	-
32	GND	Ground	-	0	-
33	NC	NC	-	-	-
34	GND	Ground	-	0	-
35	GND	Ground	-	0	-
36	GND	Ground	-	0	-
37	VCC1	Power	3.3	3.8	4.2
38	VCC2	Power	3.3	3.8	4.2
39	VCC3	Power	3.3	3.8	4.2
40	VCC4	Power	3.3	3.8	4.2
41	VCC5	Power	3.3	3.8	4.2
42	VCC6	Power	3.3	3.8	4.2
43	NC	NC	-	-	-
44	GND	Ground	-	0	-
45	GND	Ground	-	0	-
46	PCM_SYNC/GPIO46	PCM_SYNC or GPIO	1.7	1.8	1.9
47	PCM_IN/GPIO47	PCM_IN or GPIO	1.7	1.8	1.9
48	PCM_OUT/GPIO48	PCM_OUT or GPIO	1.7	1.8	1.9
49	PCM_CLK/GPIO49	PCM_CLK or GPIO	1.7	1.8	1.9
50	GND	Ground	-	0	-
51	GND	Ground	-	0	-
52	GPIO01	GPIO	1.7	1.8	1.9
53	GPIO02	GPIO	1.7	1.8	1.9
54	GPIO03	GPIO	1.7	1.8	1.9
55	GPIO04	GPIO	1.7	1.8	1.9
56	NC	NC	-	-	-
57	NC	NC	-	-	-
58	NC	NC	-	-	-
59	NC	NC	-	-	-
60	I2C_SDA	I2C Data	1.7	1.8	1.9
61	I2C_SCL	I2C Clock	1.7	1.8	1.9
62	NC	NC	-	-	-
63	NC	NC	-	-	-

74	GND	Ground	-	0	-
75	GND	Ground	-	0	-
76	NC	NC	-	-	-
77	NC	NC	-	-	-
78	NC	NC	-	-	-
79	NC	NC	-	-	-
80	UART1_CTS (UART1)	Clear To Send for UART 1	1.7	1.8	1.9
81	UART1_RTS (UART1)	Request To Send for UART 1	1.7	1.8	1.9
82	UART1_RX (UART1)	Receive for UART 1	1.7	1.8	1.9
83	UART1_TX (UART1)	Transmit for UART 1	1.7	1.8	1.9
84	GND	Ground	-	0	-
85	GND	Ground	-	0	-
86	USB_Dp	USB Data Positive	-	-	-
87	GPIO87	GPIO	1.7	1.8	1.9
88	USB_Dn	USB Data Negative	-	-	-
89	GND	Ground	-	0	-
90	GND	Ground	-	0	-
91	GND	Ground	-	0	-
92	NC	NC	-	-	-
93	GPIO93	GPIO	1.7	1.8	1.9
94	GPIO94	GPIO	1.7	1.8	1.9
95	GPIO95	GPIO	1.7	1.8	1.9
96	GPIO96	GPIO	1.7	1.8	1.9
97	GPIO97	GPIO	1.7	1.8	1.9
98	NC	NC	-	-	-
99	NC	NC	-	-	-
100	NC	NC	-	-	-
101	NC	NC	-	-	-
102	NC	NC	-	-	-
103	NC	NC	-	-	-
104	GND	Ground	-	0	-
105	GND	Ground	-	0	-
106	UART2_RX (UART2)	Receive for UART2	1.7	1.8	1.9

107	UART2_TX (UART2)	Transmit for UART2	1.7	1.8	1.9
108	GND	Ground	-	0	-
109	GND	Ground	-	0	-
120	NC	NC	-	-	-
121	NC	NC	-	-	-
122	ADC	Analog to Digital Converter	1.7	1.8	1.9
123	NC	NC	-	-	-
124	NC	NC	-	-	-
125	SPIM_MOSI	SPI Master Out Slave In data line	1.7	1.8	1.9
126	SPIM_MISO	SPI Master In Slave Out data line	1.7	1.8	1.9
127	SPIM_EN	SPI master interface enable signal	1.7	1.8	1.9
128	SPIM_CLK	SPI master interface clock	1.7	1.8	1.9
129	GPIO05	GPIO	1.7	1.8	1.9
130	GPIO06	GPIO	1.7	1.8	1.9
131	GPIO07	GPIO	1.7	1.8	1.9
132	GPIO08	GPIO	1.7	1.8	1.9
133	UIM_VCC	SIM Card Power	1.7 2.7	1.8 3.0	1.9 3.3
134	UIM_DATA	SIM Card Data Line	1.7 2.7	1.8 3.0	1.9 3.3
135	UIM_CLK	SIM Card Clock Line	1.7 2.7	1.8 3.0	1.9 3.3
136	UIM_RESET	SIM Card Reset Line	1.7 2.7	1.8 3.0	1.9 3.3
137	UIM_DETECT	SIM Card Detect Line	1.7	1.8	1.9
138	NC	NC	-	-	-
139	GND	Ground	-	0	-
140	GND	Ground	-	0	-
141	WWAN_STATE	Wireless WAN Radio State	1.7	1.8	1.9
142	POWER_ON	Power On the module: Low is Module ON and High is	1.7	1.8	1.9

Module OFF.					
143	WAKEUP_OUT	Module wakes up host.	1.7	1.8	1.9
144	WAKEUP_IN	Host wakes up module.	1.7	1.8	1.9
145	RESET	Main reset line. Active low	1.7	1.8	1.9
146	VREF	Reference Logic Voltage	1.7	1.8	1.9
200	NC	NC	-	-	-
201	JTAG_TCK	JTAG/EJTAG clock	1.7	1.8	1.9
202	JTAG_TDI	JTAG/EJTAG input data	1.7	1.8	1.9
203	JTAG_TDO	JTAG/EJTAG output data	1.7	1.8	1.9
204	JTAG_TMS	JTAG/EJTAG test mode select	1.7	1.8	1.9
205	JTAG_TRST_N	EJTAG reset; emulation JTAG is used to debug and run software on embedded MIPS processors. Only driven high when in use	1.7	1.8	1.9
206	NC	NC	-	-	-
207	NC	NC	-	-	-
208	GND	Ground	-	0	-

Below is the I/O default setting table to describe the level. It was recommended to follow the pulling High or Low to choose a suitable GPIO for application.

PU : Pull Up.

PD : Pull Down

NP : Non-Pull

I/O default setting table

Pin No.	Signal Name	Type	Default setting in Normal mode
15	RF_1	AI/AO	-
21	RF_2	AI	-
46	PCM_SYNC/GPIO46	DI /DO	PD
47	PCM_IN/GPIO47	DI	PU
48	PCM_OUT/GPIO48	DO	PU
49	PCM_CLK/GPIO49	DO	PD
52	GPIO01	DI/DO	PD
53	GPIO02	DI/DO	PD
54	GPIO03	DI/DO	PD
55	GPIO04	DI/DO	PD
60	I2C_SDA	DI/DO	PU
61	I2C_SCL	DO	PU
80	UART1_CTS (UART1)	DI	PD
81	UART1_RTS (UART1)	DO	PD
82	UART1_RX (UART1)	DI	PU
83	UART1_TX (UART1)	DO	PU
86	USB_Dp	DI/DO	-
87	GPIO87	DI/DO	PD
88	USB_Dn	DI/DO	-
93	GPIO93	DI/DO	PU
94	GPIO94	DI/DO	PD
95	GPIO95	DI/DO	PD
96	GPIO96	DI/DO	PD

97	GPIO97	DI/DO	PU
106	UART2_RX (UART2)	DI	PU
107	UART2_TX (UART2)	DO	PU
122	ADC	AI	PU
125	SPIM_MOSI	DO	PU
126	SPIM_MISO	DI	PU
127	SPIM_EN	DO	PD
128	SPIM_CLK	DO	PD
129	GPIO05	DI/DO	PD
130	GPIO06	DI/DO	PD
131	GPIO07	DI/DO	PD
132	GPIO08	DI/DO	PD
134	UIM_DATA	DI/DO	PU
135	UIM_CLK	DO	PU
136	UIM_RESET	DO	PU
137	UIM_DETECT	DI/DO	PU
141	WWAN_STATE	DO	PD
142	POWER_ON	DI	PD
143	WAKEUP_OUT	DO	PD
144	WAKEUP_IN	DI	PU
145	RESET	DI	PU
201	JTAG_TCK	DI	PD
202	JTAG_TDI	DI	PD
203	JTAG_TDO	DO	PU
204	JTAG_TMS	DI	PD
205	JTAG_TRST_N	DI	PD

Table 4. Digital I/O specifications

Parameter	Description	Min.	Typ.	Max.	Units
V_{IH}	Logic High Input Voltage	0.85*VREF	-	VREF + 0.3	V
V_{IL}	Logic Low Input Voltage	-0.3	-	0.25*VREF	V
I_{IH}	Input Leakage Current (Either Low or High and No Pull enabled)	-	-	± 10	µA
V_{OH}	Logic High Output Voltage	VREF – 0.45	-	VREF	V
V_{OL}	Logic Low Output Voltage	0	-	0.8	V
I_{OZH}	Tri-state Output Leakage Current (either Low or High)	-	-	±10	µA
R_{PU}	Internal Pull Up Resistor	53	89	16	KΩ
R_{PD}	Internal Pull Down Resistor	54	96	189	KΩ
Input Capacitance					
	Input Pin Capacitance	-	-	7	pF

Notes:

- *1. If voltage level of digital I/O from the other side is not compatible with module, level shifter is recommended to transfer the voltage level to 1.8V.

2.2. Power supply

IMA3 includes an integrated Power Manager enabling single and direct voltage supply from the battery and reducing the overall bill of materials.

Table 5. Power supply specifications

Power	Signal Name	Pin No.	Description	Voltage Levels (V)		
				Min.	Typ.	Max.
VCC	VCC1 to VCC6	37–42	Main Power Supply	3.3	3.8	4.2

Layout Suggestion: Each power trace should possess sufficient line width to withstand its respective current listed in the table below:

Net Name	Current Value
VCC(1–6) total	1.5A
UIM_VCC	150 mA
VREF	100 mA

Note : The current of VCC in real measurement is less than 800mA, but it would be better to routed under 1.5A design for getting stable power.

2.3. USB interface

IMA3 complies with USB 2.0 high-speed protocol. The USB input/output lines comply with USB 2.0 specifications. **If USB interface is not used, recommended to reserve USB_Dp and USB_Dn test points.**

Table 6. Signals of the USB interface

Name	Description	Input/Output (Direction to module)	Voltage Levels (V)		
			Min.	Typ.	Max.
D+	USB data positive (low-/full-speed)	Input High	2	3.3	3.6
		Input Low	0	–	0.8

	Output High	2.8	3.3	3.6
	Output Low	–	–	0.3
USB data positive (high-speed)				
	Input High	0.3	–	0.44
	Input Low	0	–	0.01
	Output High	0.36	0.38	0.44
	Output Low	0	–	0.01
D–				
USB data negative (low-/full-speed)				
	Input High	2	3.3	3.6
	Input Low	0	–	0.8
	Output High	2.8	3.3	3.6
	Output Low	–	–	0.3
USB data negative (high-speed)				
	Input High	0.3	–	0.44
	Input Low	0	–	0.01
	Output High	0.36	0.38	0.44
	Output Low	0	–	0.01

Layout suggestion:

- Differential impedance: 90 Ω
- Space to other signals should be at least 20 mils
- Intra-pair length mismatch should be less than 150 mils
- If reserved USB test point, it also suggest the trace should be followed differential impedance 90 Ω and put the USB_Dp, USB_Dn test points together

USB Length in IMA3 is tuned as below:

Function	Net Name	Length (mil)
USB		
	USB_Dp	167.08
	USB_Dn	197.62

2.4. SIM interface

IMA3 includes an SC controller, interface pins, and a dedicated LDO (3.0 V or 1.8 V).

Since IMA3 is not equipped with a SIM socket, it must place a SIM socket on the user interface board.

IMA3 provides a UIM_DETECT input pin to detect if the SIM card is present. If the USIM card is present, UIM_DETECT should be high. (The voltage level should be 1.8 V) If the USIM card is absent, UIM_DETECT should be low. (The module is internally pulled down.) It was recommended to choose a SIM socket with the Card Detect pin. If the SIM card is present, the pin will not contact the ground and pull up to 1.8 V through a 2 kΩ resistor. If the SIM card is absent, the pin will normally contact the ground. Other types of SIM sockets which can achieve this feature are also acceptable.

A 100 nF capacitor and a 1 μF capacitor are placed between the UIM_VCC and Ground pins in a parallel manner. (If the UIM_VCC circuit is too long, a larger capacitor such as a 4.7 μF capacitor can be employed if necessary.) Four 33 pF capacitors (0402 package is recommended.) are placed between the UIM_VCC and Ground pins, the UIM_CLK and Ground pins, the UIM_DATA and Ground pins, and the UIM_RESET and Ground pins in parallel to filter out interference from RF signals. (An R/C circuit on pin UIM_CLK is optional. If there is an EMI issue on this clock signal, try to adjust these R/C values.)

We recommend taking protective measures against electrostatic discharge (ESD) near the SIM socket. The TVS diode with a V_{RWM} of 5 V and junction capacitance of less than 10 pF must be placed as close as possible to the SIM socket, and the Ground pin of the ESD protection component must be well connected to the power Ground pin that supplies power to IMA3.

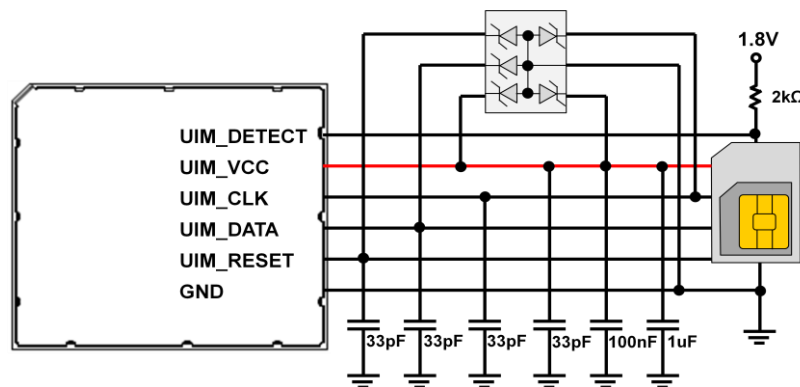


Figure 2. SIM card interface circuit

2.5. Control interface (signals)

This section describes the host-to-modem wake-up interface and power-on signal to enable or disable the control module.

2.5.1. Power-on Signal

The POWER_ON pad is an input signal used to control whether the module is in the Module Enabled or Module Disabled state. Do not toggle the PERST# pin during power-on. This signal has the highest priority over the wakeup, the alarms signals, and the digital control pins.

The POWER_ON signal is Active Low (VIL for VREF), its voltage level is 1.8V if going to High for Module Disabled:

- POWER_ON is High: Module is OFF
- POWER_ON is Low: Module is ON

There are three possible states of the module:

- Module Off - VCC is not present.
- Module Enabled - VCC is supplied, and the module is enabled.
- Module Disabled - VCC is supplied, and the module is disabled.

The state transitions are defined as follows:

- When voltage is applied to VCC, the module shall enter the Module Disabled state.
- An input to the POWER_ON pad shall trigger the transition from the Module Disabled to the Module Enabled state.
- An input to the POWER_ON pad shall trigger the transition from the Module Enabled to the Module Disabled state.

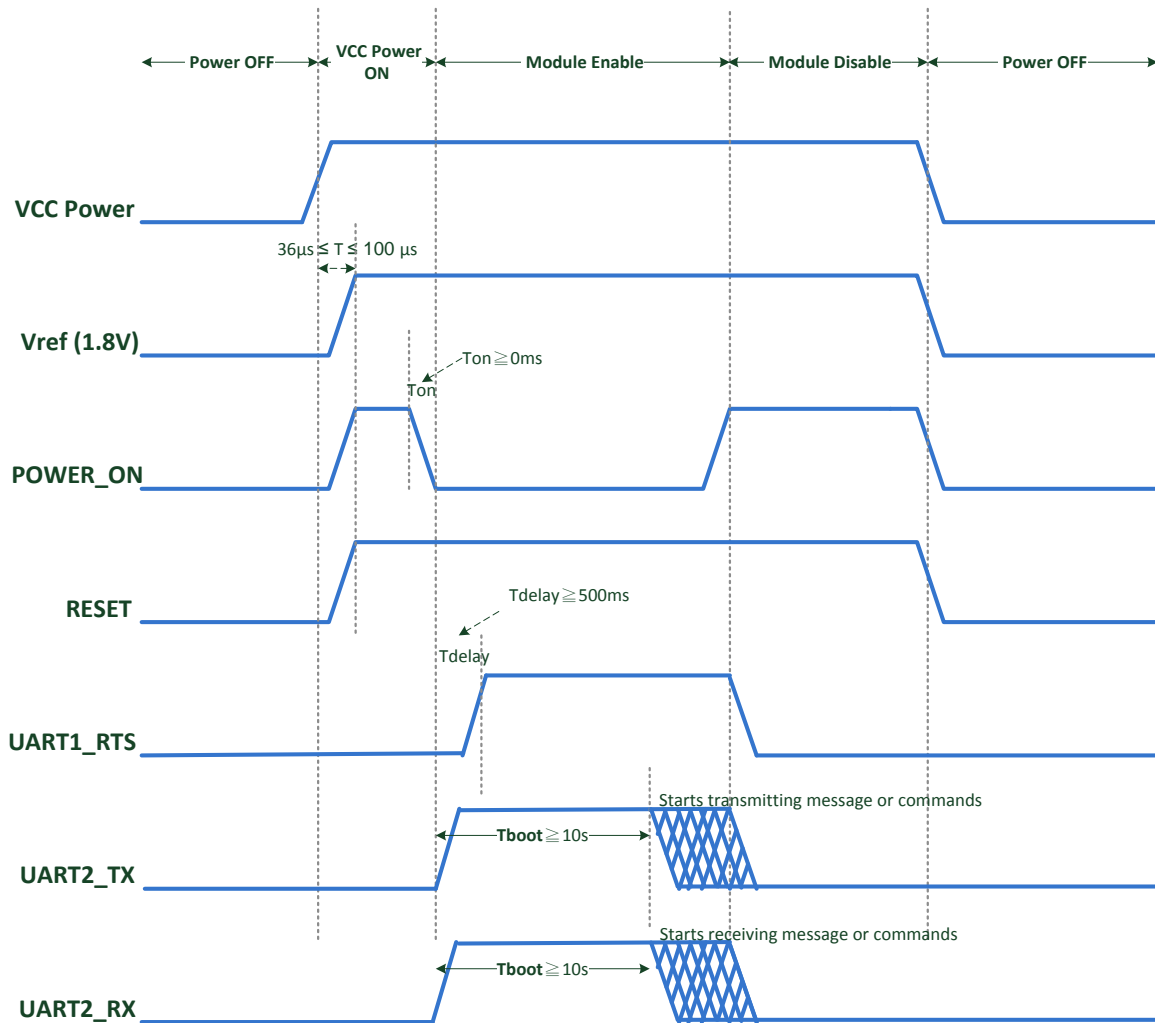


Figure 3. Power ON/OFF timing

In order to prevent the POWER_ON signal in a floating state, default had a internal pull low 200 kΩ resistor to power on the module. For controlling the module well, it was recommended to pull LOW for Module Enabled, or pull HIGH to VREF for Module Disabled.

UART1_RTS signal should be LOW at least 500ms while booting up the system, since there is a internal booting configuration limited.

UART2_TX and UART2_RX signals should keep HIGH over 10 seconds, since any transmittion activity in the period will let the system stop in u-boot mode.

2.5.2. Host-to-modem wake-up interface

In applications where the device power consumption is a major target of optimization such as battery-operated sensors that are based on IOT/M2M modem solution and in addition, include a third-party host, it is necessary to define a simple interface that will allow both the modem and the host to be able to enter low power states whenever possible while allowing the other side to wake it up when required.

For example, if the host has no data to transmit or any other tasks, it may wish to enter some low power state according to its own capabilities and configurations. If during the time the host is in a low power state and the modem suddenly receives data, it must wake-up the host.

A similar requirement exists from the other side. If, for example, the modem is in a low power state and suddenly the host must transmit data, it must to be able to wake-up the modem.

Each side has notification functionality when they are up and ready to follow a wake-up request.

The idea behind the suggested method is to have a very simple interface that will also be pin-limited (requires only two pins) to fit into such limited-pin-count applications and packages.

The interface consists of two lines: one is driven by the host and received by the modem, and the other is driven by the modem and received by the host.

Each side can wake the other side by toggling it high and allowing the other side to go to sleep when not needed by toggling it low.

Toggling the signal high does not necessary mean the other side will enter the low power state; the toggling function is only intended to notify the other side that its functions will not be required in the near term and that it is allowed to enter a low power state if he can (according to its own tasks, configurations, and capabilities).

The following diagram depicts how this simple interface works. In addition to the two hardware signals, additional higher-level messages may be defined to pass further information or details between the host and the modem if required.

If the Power states of “Sleep” and “Hibernation” feature are required, it was recommended to connect WAKEUP_IN and WAKEUP_OUT signal to Host. This design can make sure IMA3 can be waked up by Host.

- “WAKEUP_IN” (Host: Output, Modem: Input):
 - LOW: Host does not need the MODEM (allowing it to sleep).
 - HIGH: Host needs the MODEM or acknowledges it is ready following a wakeup request from the MODEM.
- “WAKEUP_OUT” (Host: Input, Modem: Output):
 - LOW: MODEM does not need the Host (allowing it to sleep).
 - HIGH: MODEM needs the Host or acknowledges it is ready following a wakeup request from the Host.

The first part is “Close UART interface”. To confirm that both Host and Modem will not send data with each other. If there is no data traffic, then enter low power state. The second part is “Open UART interface”. Host can notify Modem to wakeup via “WAKEUP_IN” High, or Modem can notify Host via “WAKEUP_OUT” high. There are some steps to make a communication between Host and Modem. Please refer to Figure 4 and Figure 5.

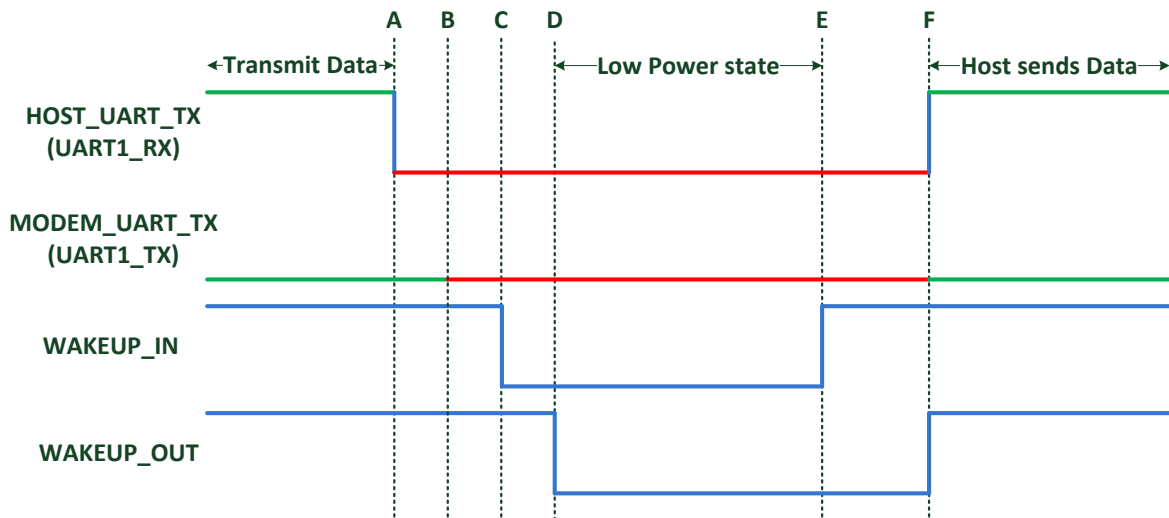


Figure 4. Open UART interface – Host to Modem

- A. Host detects that it has nothing to send and Modem isn't transmitting any data (HOST_UART_TX = 0). Host requests Modem to enter low power state and send "AT%IFSUSP" to Modem.
- B. Modem receives "AT%IFSUSP" and decides whether to send "OK" or "Not Ready" response. If Modem wants to suspend communication, it will not send any data (MODEM_UART_TX = 0). If Host receives "Not Ready", it can send data over HOST_UART_TX. If Host still wants to suspend the UART interface, it should continue trying to send "AT%IFSUSP" every 100ms. (This number should be adjusted soon)
- C. Host receives "OK". Then Host drops WAKEUP_IN to request Modem to enter Low Power state, which includes Sleep mode, Hibernation mode, or PSM mode. It depends on the software configure.
- D. Modem detects WAKEUP_IN is down, and drops WAKEUP_OUT. Modem enters Low Power state.
- E. Host wants to send data to Modem. WAKEUP_IN is up.
- F. Modem is awaking and brings WAKEUP_OUT up when Modem is ready. Then Host can start to send data to Modem.

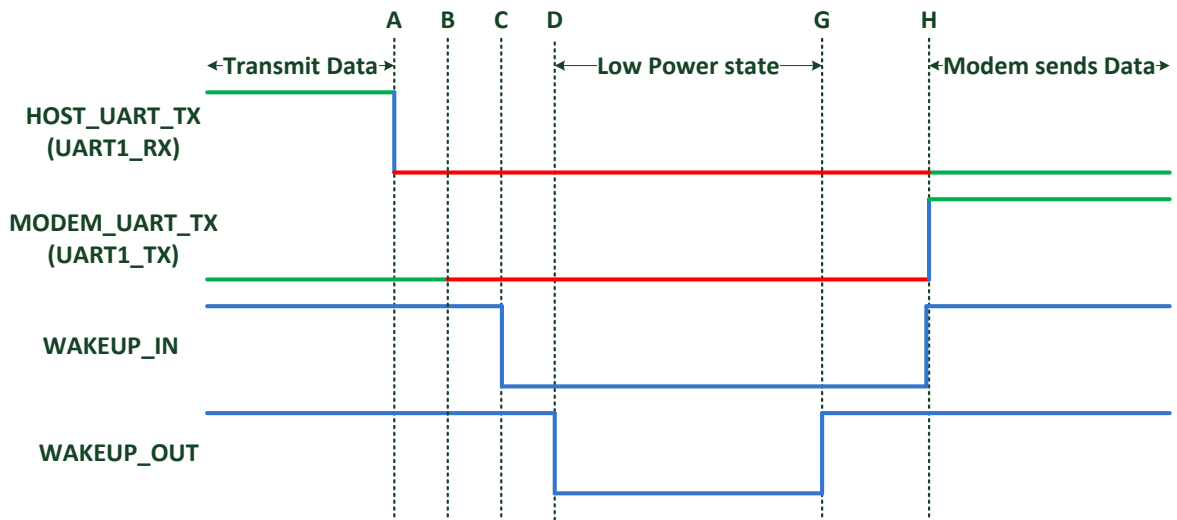


Figure 5. Open UART interface – Modem to Host

There is another scenario to open UART interface by Modem. The step A to D is same as opening UART interface by Host. But step G and H is different.

G. Modem wants to send data to Host. WAKEUP_IN is up

H. Host is awaking and brings WAKEUP_IN up when Host is ready. Then Host can start to send data to Modem.

2.5.3. Reset Signal

The Reset Signal is a hardware reset signal to control the system reset directly. You can connect it to a key or a control signal. It was recommended to reserve a pull up resistor and a capacitor to ground. Default is not installed.

It is required that the Reset Signal is kept LOW at least 3 seconds after a command to reset the module has been issued to ensure that there is time for the module reset properly.

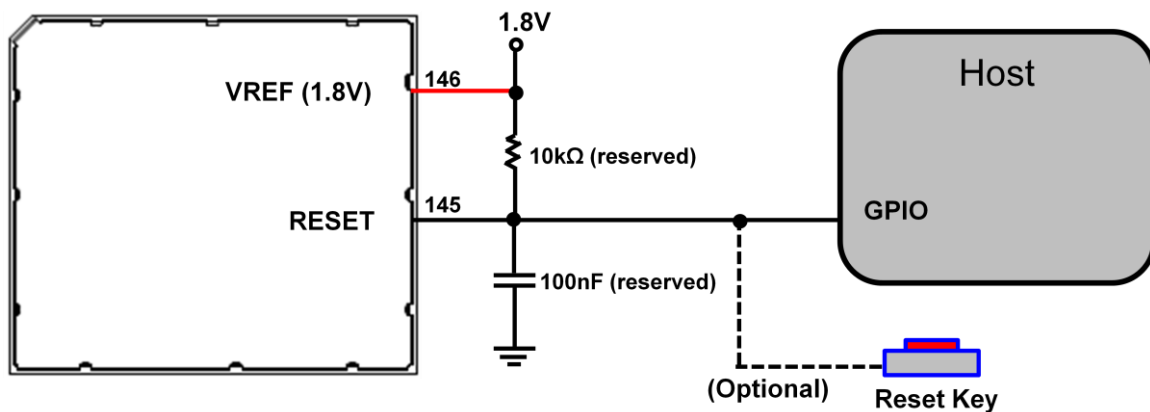


Figure 6. Reset Signals circuit

2.6. Digital interface

This section provides the required AC timing information relating to Module Digital Interfaces.

2.6.1. SPI Master Interface

Operating Modes

The SPI master controller supports two operating modes:

Standard SPI protocol:

- SPIM_CLK – Output clock
- SPIM_CS – Output, chip-select
- SPIM_MOSI – Output, data to slave
- SPIM_MISO – Input, data from slave

LCD interface protocol:

- SPIM_CLK – Output clock
- SPIM_CS – Output, chip-select
- SPIM_MOSI – Output, data to slave
- SPIM_MISO – Output, command/data control bit to slave

Interface timing is defined separately for each SPI operating mode.

Timing Modes

Each operating mode, as described above, can be configured to one of the following timing modes:

SPI_CLK_POS: Both output data and input data are related to the clock's rising edge

SPI_CLK_NEG: Both output data and input data are related to the clock's falling edge

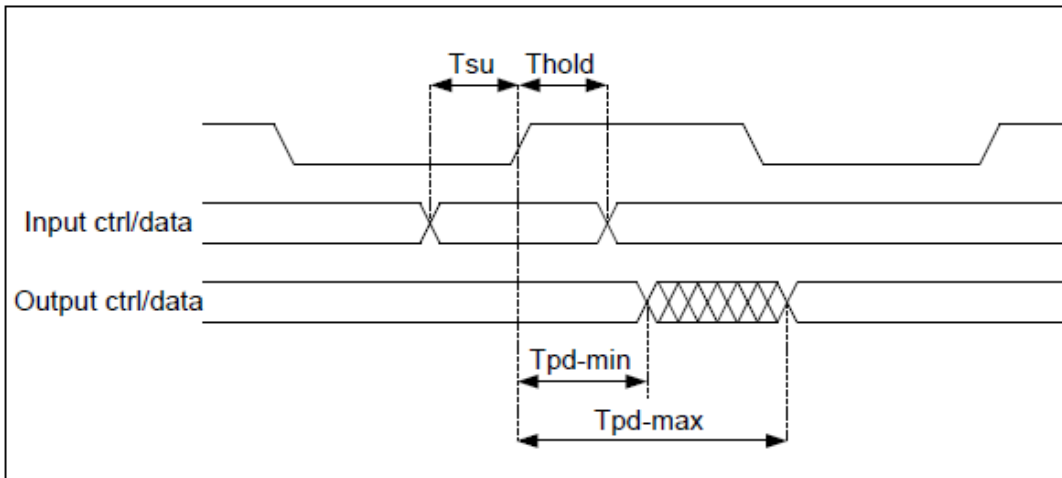


Figure 7. SPI_CLK_POS timing diagram

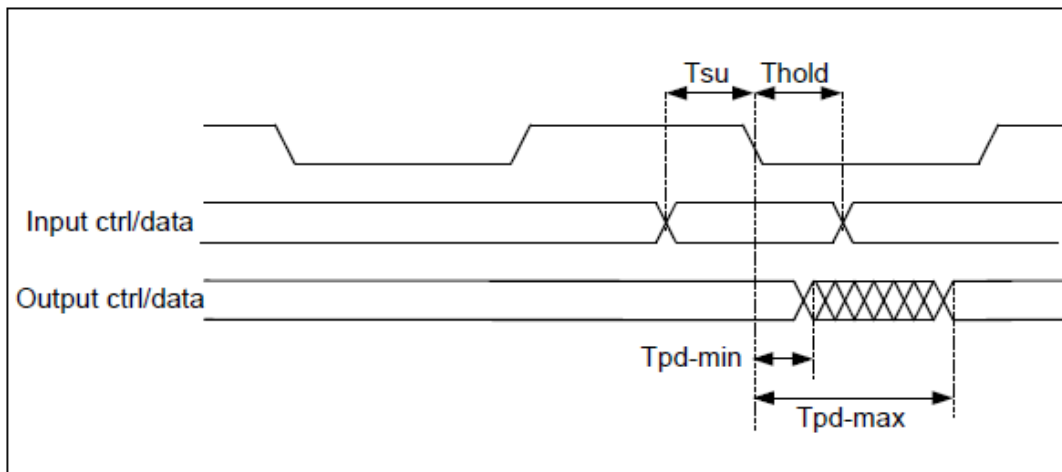


Figure 8. SPI_CLK_NEG timing diagram

Table 7. Standard SPI mode timing (both SPI_CLK_OS and SPI_CLK_NEG)

Parameter	Minimum	Maximum	Unit	Description
T _{CYCLE}	20	-	ns	Clock cycle time
T _{SU}	5	-	ns	Input setup time
T _{HO}	0	-	ns	Input hold time
T _{PD}	1.5	8.5	ns	Output delay

Table 8. LCD mode timing (both SPI_CLK_OS and SPI_CLK_NEG)

Parameter	Minimum	Maximum	Unit	Description
T _{CYCLE}	20	-	ns	Clock cycle time
T _{SU}	5	-	ns	Input setup time
T _{HO}	0	-	ns	Input hold time
MOSI T _{PO}	1.5	8.5	ns	Output delay
MISO T _{PD}	1.5	16	ns	Output delay

2.6.2. PCM Interface

IMA3 provides one PCM digital audio interface.

The PCM interface enables communication with an external codec to support a linear format.

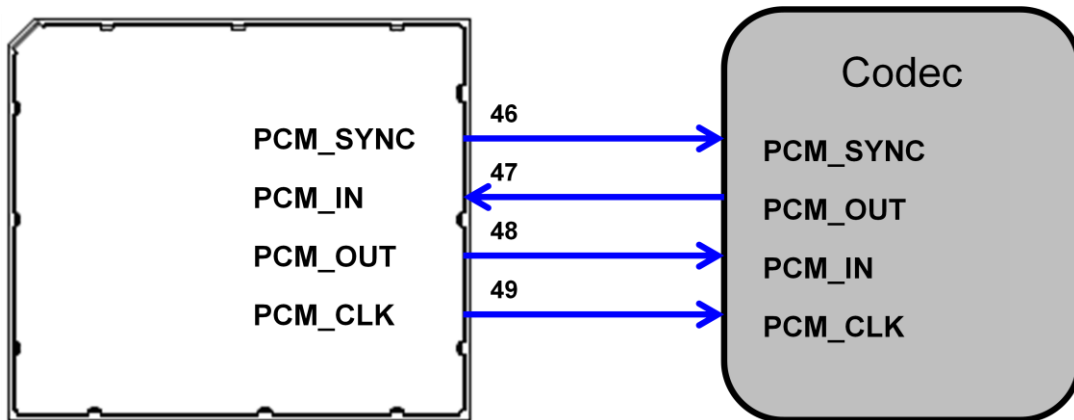


Figure 9. Recommended circuit for the PCM interface

Use a TVS on the related interface to prevent electrostatic discharge and protect integrated-circuit (IC) components.

2.6.3. I2S Interface

PCM and I2S share the same pins on IMA3, the PCM signal pins can be configured as an I2S interface.

Pad	Config1	Config2
46	PCM_SYNC	I2S_LRCK
47	PCM_DIN	I2S_DATA_IN
48	PCM_DOUT	I2S_DATA_OUT
49	PCM_CLK	I2S_BCK

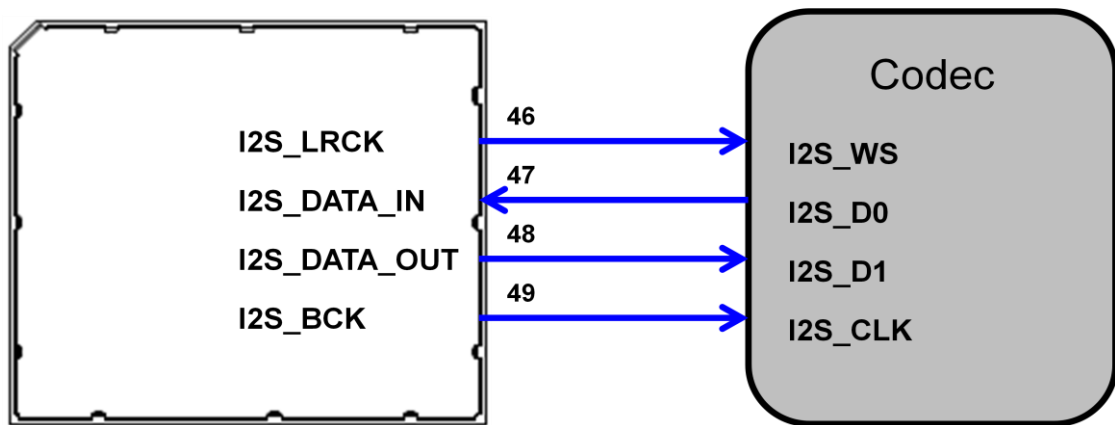


Figure 10. Recommended circuit for the I2S interface

2.6.4. I2C Interface

There is one I2C interface in IMA3. It was recommended to add pull high to 1.8 V through resistors with values of 2.2 k Ω to 4.7 k Ω . ICs and sensors can use the same I2C interface. IMA3 can recognize them by different addresses. I2C interface only supports master mode.

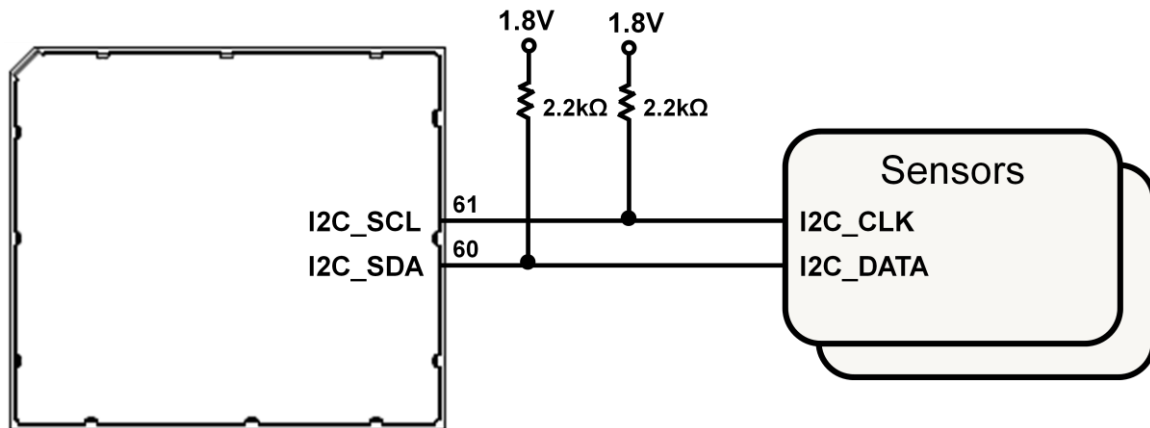


Figure 11. Recommended circuit for the I2C interface

2.6.5. UART Interface

There are dual UART interfaces. One is 4 bit for high-speed data transfer, and the other is 2 bit for diagnostic tools and debugging. Recommended to reserve a pull down 1kΩ resistor on UART1_RTS signal near IMA3 module side for booting up normally.

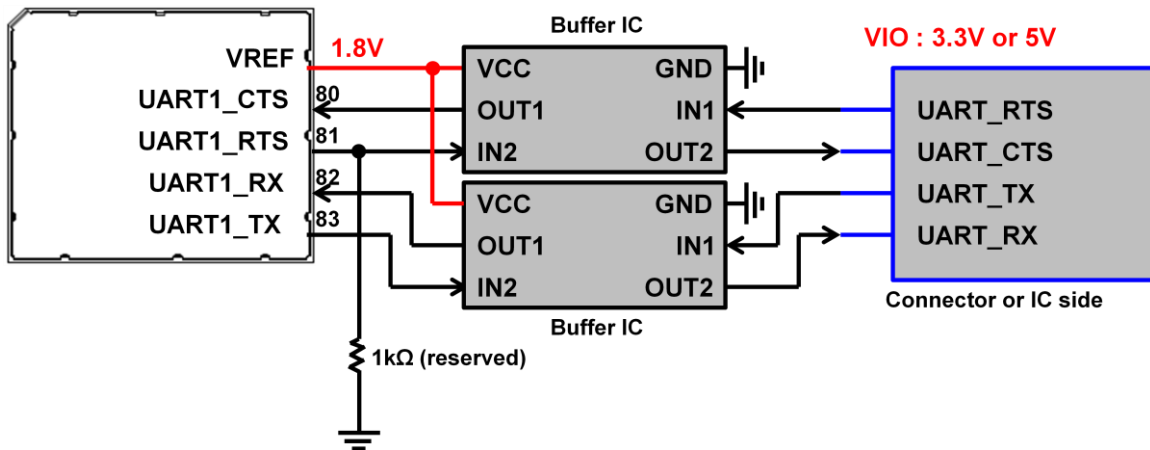


Figure 12. Recommended circuit for UART interface (4 bit) with Level translator

Note : UART1_RTS signal should be LOW at least 500ms while booting up the system, since there is a internal booting configuration limited.

2.7. ADC interface

One Analog to Digital Converter (ADC) input is provided by IMA3. The converter is of a 10 bit resolution, ranging from 0.1 V to 1.8 V with a sampling rate of 2 MHz. They can be used for customer applications.

Table 9. ADC interface

Signal Name	Pads	Type	Description
ADC	122	Analog	Analog to digital conversion input

Table 10. Electrical characteristics of the ADC interface

Parameter	Minimum	Typical	Maximum	Unit
Input signal range	0.1	-	1.8	V
Resolution	-	10	-	bit
Offset error	-	1	2	%FS
Sampling time	-	10	-	Clock Cycles
Conversion clock	0.04	2	-	MHz
Throughput rate	-	2	-	MSPS

Notes : 1. %FS = % Full Scale

2. MSPS = Million Samples per Second

2.8. GPIO

IMA3 includes general purpose I/O signals that are summarized in the following table. These GPIOs are available for customer-defined purposes such as control, signaling, and monitoring. Some GPIO signals also can be configured as PCM signals for audio applications.

Table 11. GPIOs

Signal Name	Pads	Description	Alt. Function
GPIO01	52	Configurable general purpose I/O	
GPIO02	53	Configurable general purpose I/O	
GPIO03	54	Configurable general purpose I/O	
GPIO04	55	Configurable general purpose I/O	
GPIO05	129	Configurable general purpose I/O	
GPIO06	130	Configurable general purpose I/O	
GPIO07	131	Configurable general purpose I/O	
GPIO08	132	Configurable general purpose I/O	
GPIO46	46	Configurable general purpose I/O	PCM_SYNC
GPIO47	47	Configurable general purpose I/O	PCM_IN
GPIO48	48	Configurable general purpose I/O	PCM_OUT
GPIO49	49	Configurable general purpose I/O	PCM_CLK
GPIO87	87	Configurable general purpose I/O	
GPIO93	93	Configurable general purpose I/O	
GPIO94	94	Configurable general purpose I/O	
GPIO95	95	Configurable general purpose I/O	
GPIO96	96	Configurable general purpose I/O	
GPIO97	97	Configurable general purpose I/O	

3. RF Specifications

3.1. RF connections

IMA3 provides two RF pads; developers can connect them via 50 Ω traces to the main board.

TRX pads – RX/TX path

It is recommended to have keep-out under RF pads.

3.2. Interference and sensitivity

This section is to help developers to identify the interference that may affect IMA3 when adopting it in systems.

Interference from other wireless devices

Harmonics or inter-modulated signals generated from wireless devices that fall in RX ranges of IMA3 may result in degraded RX performance.

It is highly recommended to check the RX performance of the entire systems in the shielding environment.

Interference from the host interface

High-speed switching signal elements in the system can easily couple noise to the module (Ex.: DDR memory, LCD modules, DC-DC converter).

Methods to avoid sources of interference

Antenna location is important; it is recommended that the antenna away from high-speed switching signals. Tracing from the module to the antenna is recommended to be as short as possible and must be shielded by complete grounding.

However, IMA3 is well-shielded. The high-speed elements in the system are recommend to be reserved for shielding during an early stage of a project's development.

3.3. Radiated sensitivity measurement

Over-the-air testing can demonstrate the TRX ability of the whole system. Keys elements that affect the measurement are:

- Module ability (refer Specification)
- Antenna Gain
- System noise source

The OTA performance should be performed in an OTA chamber.

3.4. Supported frequencies

Table 12. IMA3 supported frequencies

Band	Uplink (MHz)	Downlink (MHz)
LTE Band 2	1,850–1,910	1,930–1,990
LTE Band 4	1,710–1,755	2,110–2,155
LTE Band 12	699–716	729–746

Table 13.

Band	Bandwidth					
	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz
LTE Band 2			V	V	V	V
LTE Band 4			V	V	V	V
LTE Band 12			V	V		

3.5. Power consumption

IMA3 was designed for the IoT and M2M markets. WNC has devoted special attention from the beginning of development to low power design and has undergone major efforts to further reduce the system power consumption in order to achieve unprecedented figures for an LTE device.

The system can exist at any given time in one of the defined power states. Each of these power states defines what power supplies are available, what clock the system is operating on, and additional hardware requirements such as IO usage and connectivity.

In the operational mode the system will move from one power state to another based on the specific operational mode/scenario and based on different parameters such as: system configured permissions, hardware limitations, and the time left until the next required activity.

Table 14. System Power States

Power State	Description	Available Interfaces
Active	The system is active, operating on the high PLL clock.	All interfaces may be used according to the system configuration
Sleep	All systems are halted. Module registers data is retained. DRAM is in self-refresh. The system can be configured to wake up from a slow clock counter at a specific time or by one of the specific pins.	These pins can be used to wake up the device from deep-sleep state: WAKEUP_IN pin. The USB interface can also wake the device from the sleep state
Hibernation	All system data is retained in DDR memory, but all user interfaces are disabled. A 32.768 KHz clock counter can be configured to wake the system at a specific time or use the "WAKEUP_IN" Pin. After entering Hibernation, USB interface was disabled. If user want to resume USB interface,	WAKEUP_IN pin

please reboot IMA3		
PSM	Power Saving Mode is newly added feature in 3GPP Release 12 and is specified in 3GPP 24.301-5.3.11 Power saving mode and 23.682-4.5.4 UE Power Saving Mode. PSM is applied between the expiration of T3324 and T3412.	None
Off	The modem has no power supply; there is no system clock.	None

The following figure depicts the possible transitions between the system power states. The system can be turned off from any power state (by shutting the external supplies or by toggling high POWER_ON pin input). All transitions between all other states (not "Off") are performed from the active state. Deep Hibernation state was not supported in this module.

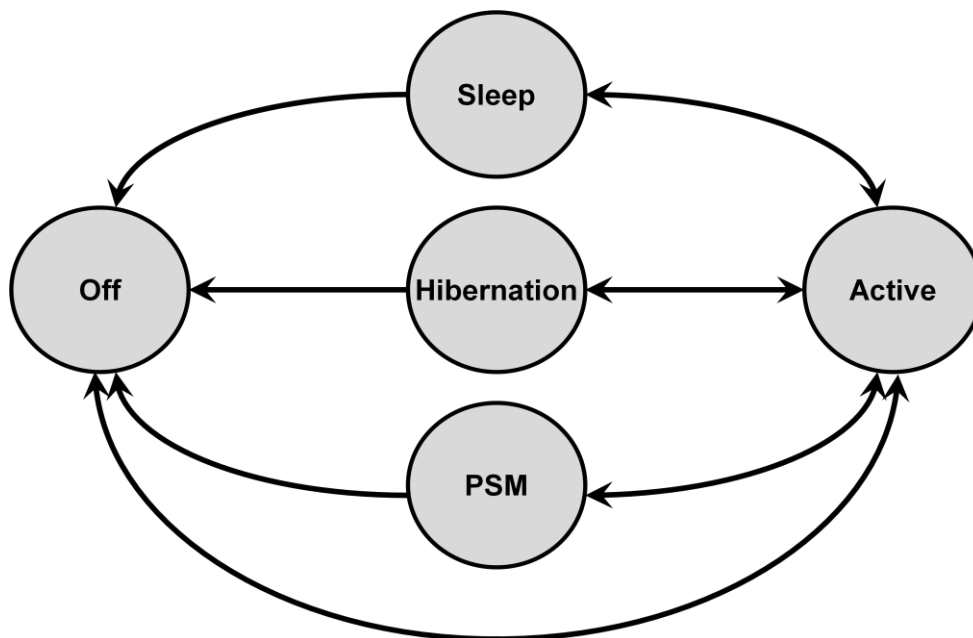


Figure 13. Power-state transitions

Figure 14 can describe the PSM mechanism between User Equipment (UE) and Network (NW). The time of T3412 could be configured by users. Please refer to the document “WNC IMA3 Application Notes for Power Saving Mode v0.9.4.pdf” for the commands of PSM.

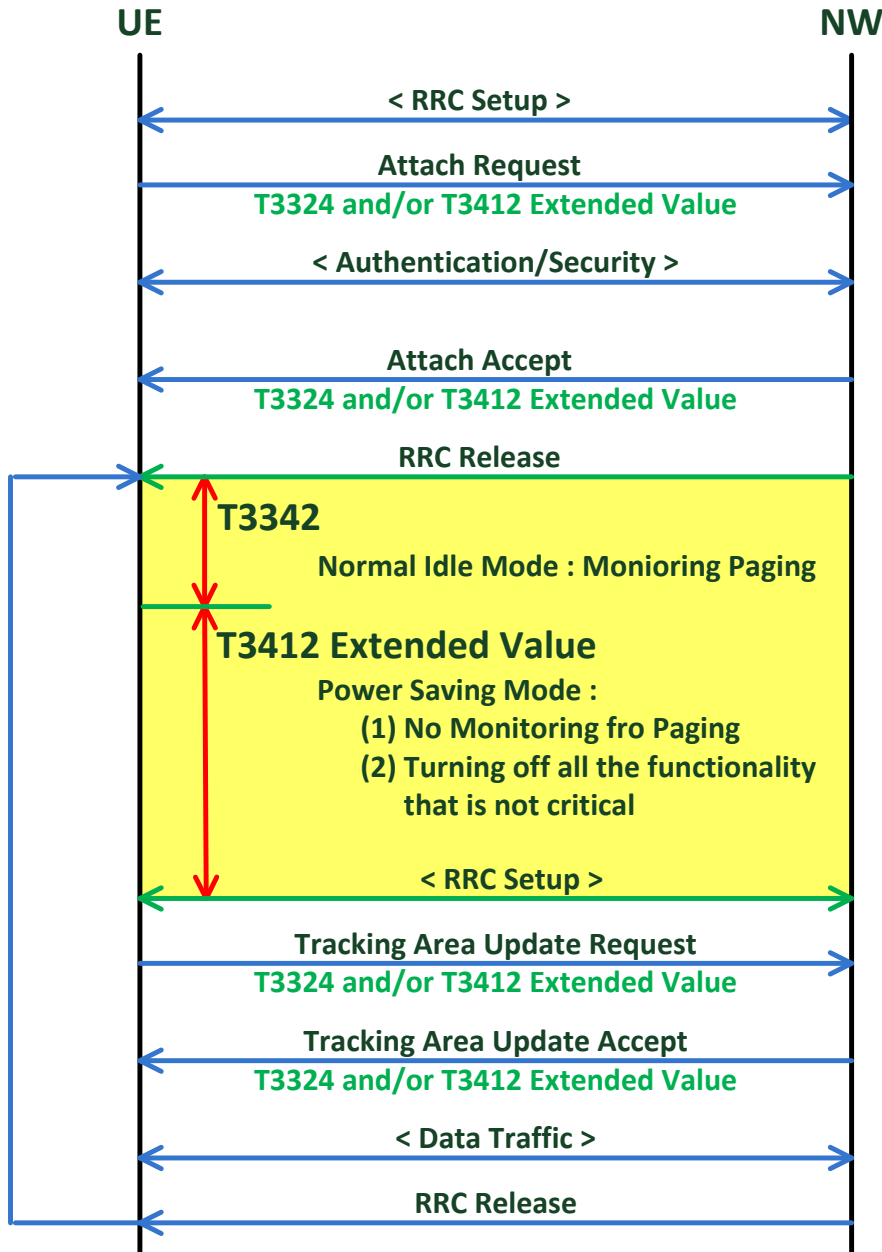


Figure 14. PSM mechanism between UE and NW

3.6. Module power states

In the operational modes, the system can be configured to use the different power states.

The system state is selected according to the permissions, required activity, and the available expected time until the next power state.

This method allows the power management to be very dynamic and flexible and to be tuned according to the needs of each product/application and according to specific conditions.

The following table shows several main system operational modes and the different system power states used in each mode.

If the Power states of “Sleep” and “Hibernation” feature are required, it was recommended to connect WAKEUP_IN and WAKEUP_OUT signal to Host. This design can make sure IMA3 can be waked up by Host.

Table 15. Power Consumption result

LTE Working Mode	Conditions	Result (VCC=3.8V)
Airplane mode		
	Only Module, no other device	TBD
LTE standby – Hibernation (1.28 sec)		
	Band2 –LTE Standby mode, DRX = 1.28 sec	TBD
	Band4 –LTE Standby mode, DRX = 1.28 sec	TBD
	Band12 –LTE Standby mode, DRX = 1.28 sec	TBD
LTE standby – Sleep (1.28 sec)		
	Band2 –LTE Standby mode, DRX = 1.28 sec	TBD
	Band4 –LTE Standby mode, DRX = 1.28 sec	TBD
	Band12 –LTE Standby mode, DRX = 1.28 sec	TBD
Band2 Working mode		
	Band2 – Bandwidth 10MHz, TX Power=23dbm Cat. M1, Downlink 1Mbps/ Uplink 1Mbps via USB interface by iperf tool	TBD

Band4 Working mode		
	Band4 – Bandwidth 10MHz, TX TBD Power=23dbm Cat. M1, Downlink 1Mbps/ Uplink 1Mbps via USB interface by iperf tool	
Band12 Working mode		
	Band12 – Bandwidth 10MHz, TX TBD Power=23dbm Cat. M1, Downlink 1Mbps/ Uplink 1Mbps via USB interface by iperf tool	
Powering on	Conditions	Result (VCC=3.8V)
Peak power consumption		
	Power consumption peak when the module is powering up	TBD
Power off	Conditions	Result (VCC=3.8V)
Module disable		
	Provided VCC Power but POWER_ON is High to disable module	< 8uA

Note : The current value was measured at “VCC = 3.8V” voltage level.

4. Software Interface

IMA3 can be configured with several types of configurations for different external host processors which require data communication to the Internet. The basic concept is that the module provides proper interfaces for its control and for the data traffic, which supports as many external host processors as possible with different capabilities for network connection.

Please refer to the “IMA3 SW Developer Guide” for further detail.

5. Mechanical and Environmental Specifications

5.1. PCBA form factor

Dimensions and recommended PCB Layout footprint for IMA3.

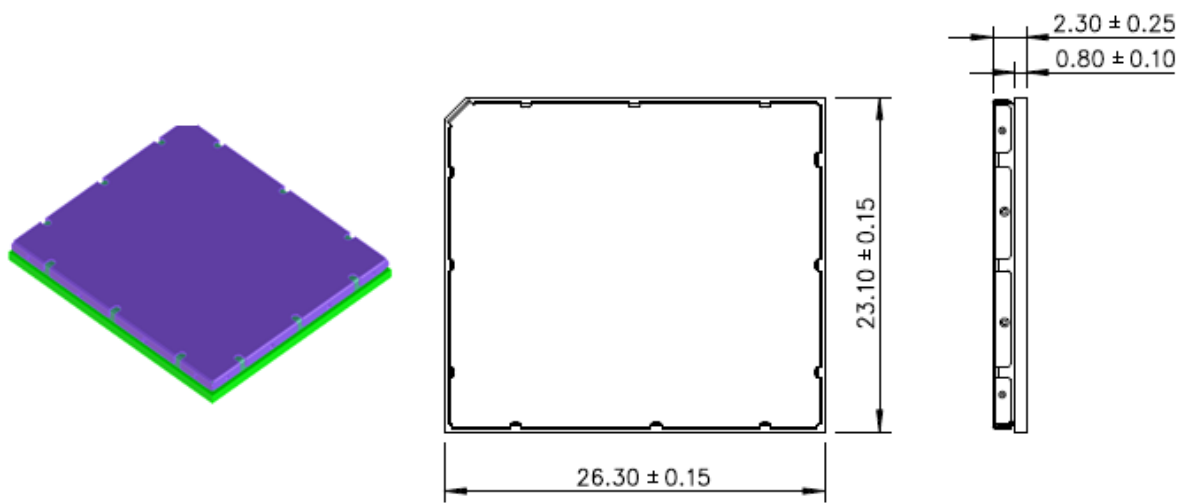


Figure 15. PCBA dimensions

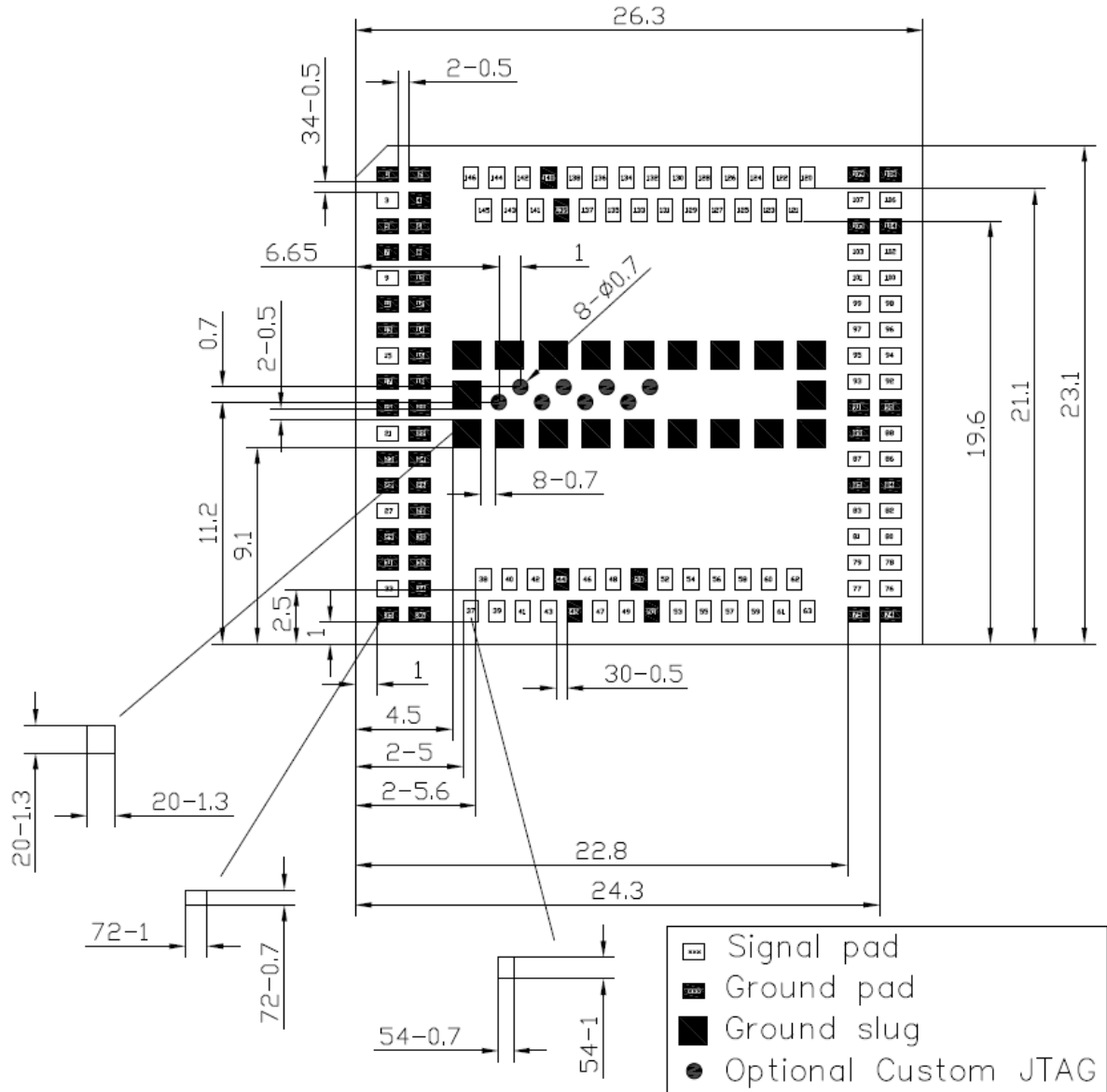


Figure 16. Recommended PCB layout footprint (top view)

5.2. Module PCB Layout

This section depicts the inner layer of IMA3 PCB layout to enhance users' understanding of the module's design.

Top layer:

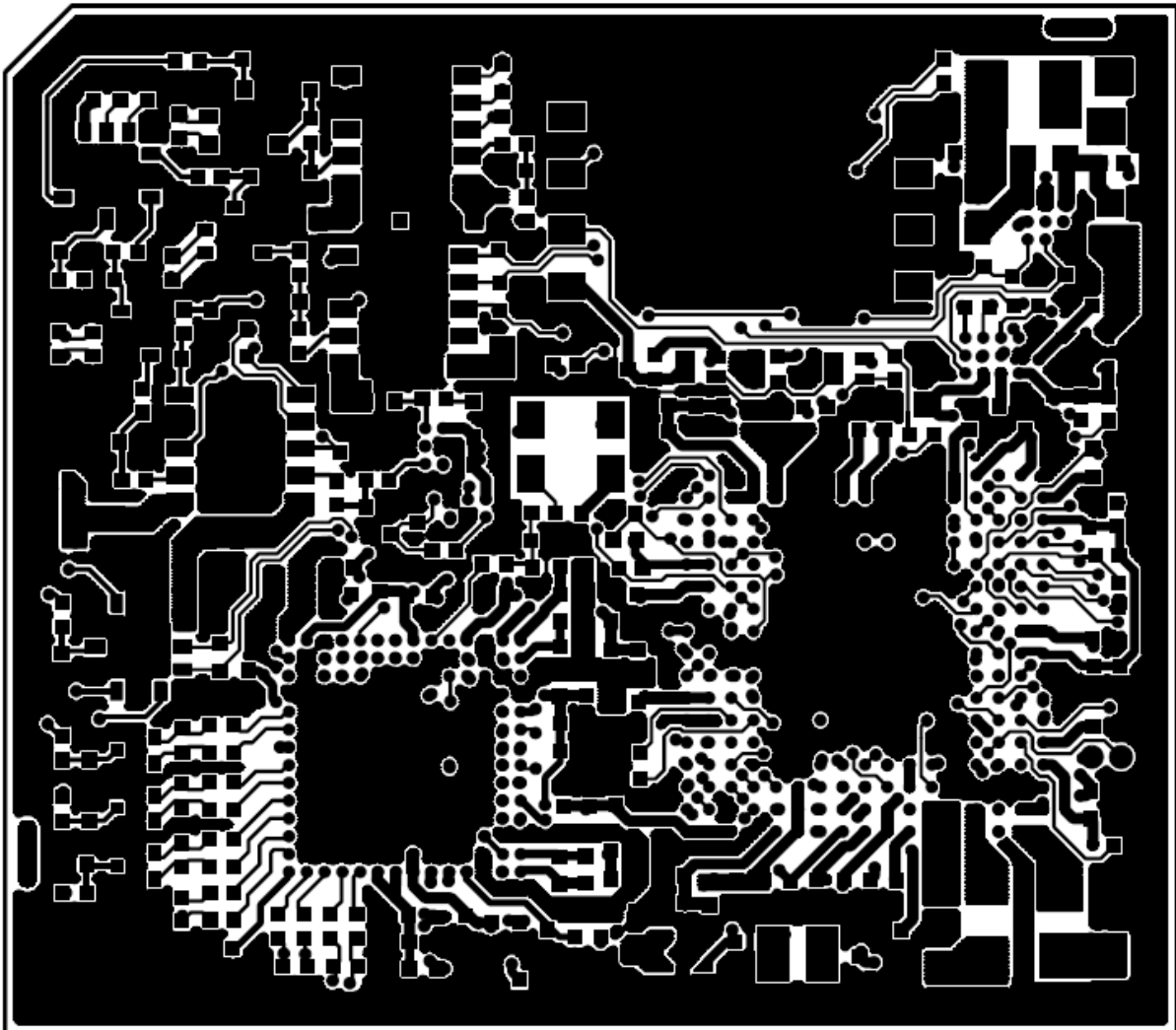


Figure 17. Top layer of IMA3 PCB layout

Bottom layer:

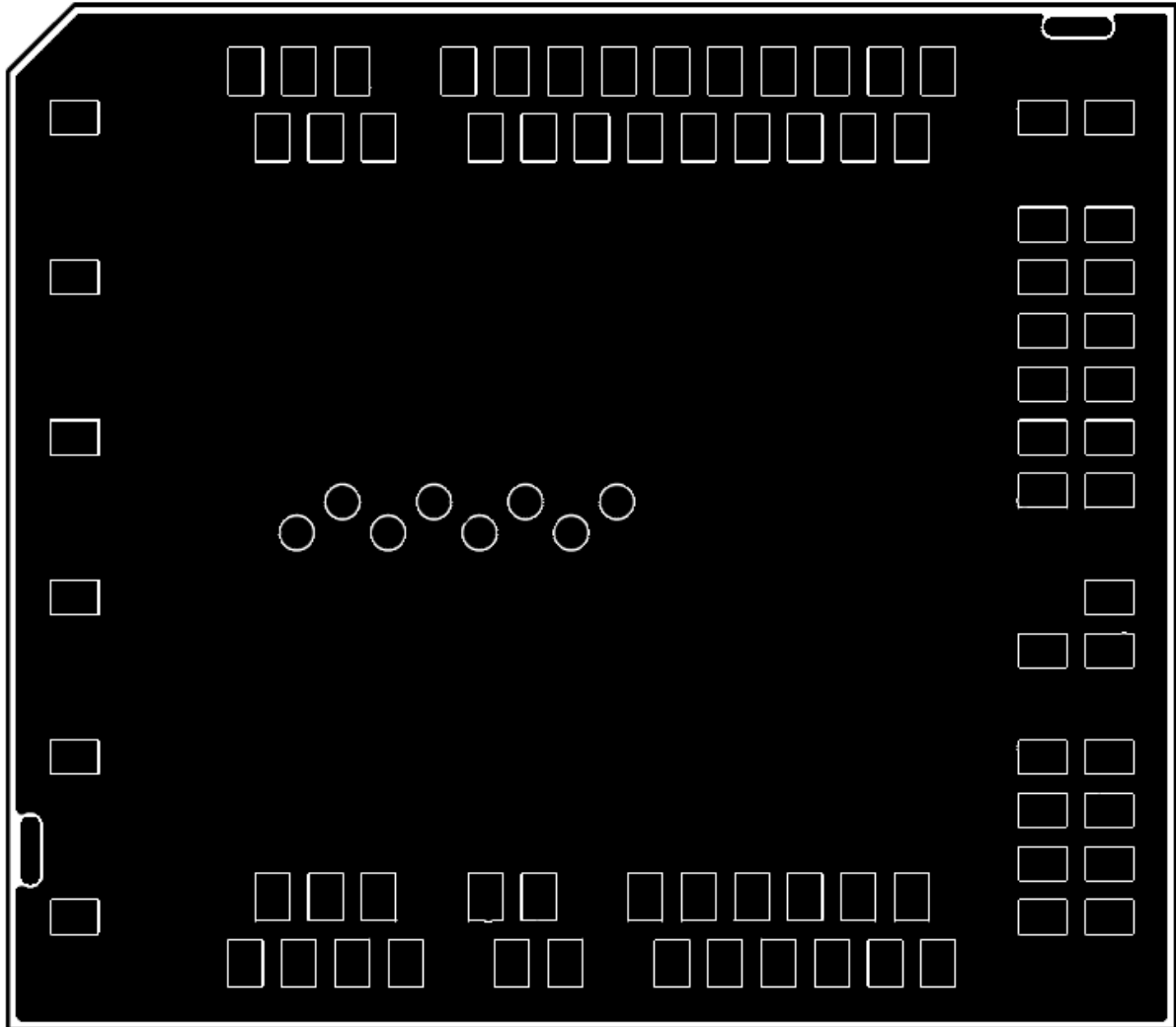


Figure 18. Bottom Layer of IMA3 PCB layout

5.3. Reflow

This section details the recommended reflow profile when the module is mounted onto other boards.

Temp. Region	1	2	3	4	5	6	7	8	9	10	11
Upper temp. region	120	170	170	170	170	190	225	225	245	250	245
Lower temp. region	120	170	170	170	170	190	225	225	245	250	245
Conveyer band speed	90 cm/minute										

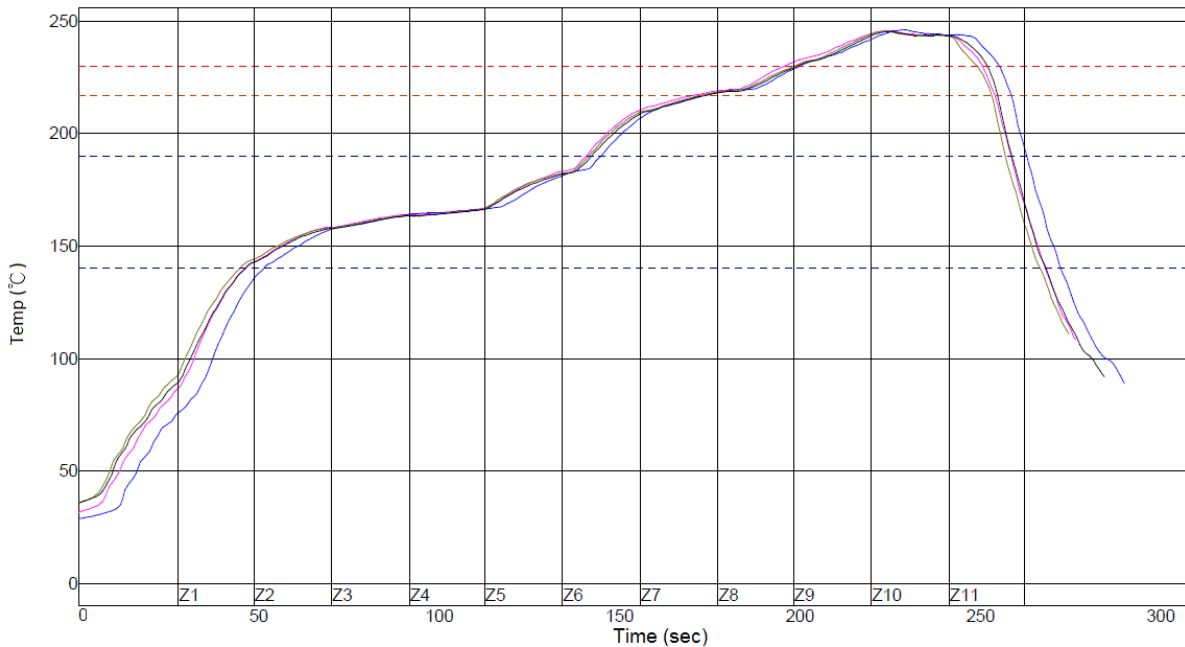


Figure 19. Reflow Profile of IMA3

Table 16. Reflow data

PWI = 60%	D31-1	D31-2	U23-3	U23-4	Temp. Difference
Preheat from 140–190°C					
	4.34	93.50	96.60	95.96	3.1
	39%	34%	52%	48%	
Melt-out Time/230°C					
	4.88	55.19	50.65	52.55	4.54
	49%	52%	6%	26%	

Max Temp				
45.73	246.01	245.56	245.38	0.63
57%	60%	56%	54%	
Total Time/217°C				
3.45	84.37	80.45	80.82	3.92
-6%	-3%	-18%	-17%	
Gradient1 (100–150°C)				
2.27	2.31	2.22	2.22	0.09
52%	54%	48%	48%	

Table 17. Process limit

Solder Paste	Lead-free		
	Min.	Max.	Unit
Profile feature			
Gradient1 (Target = 1.5) (100 °C–150 °C) (Time period = 20 s)	0	3	°C/sec
Preheat time from 140 °C to 190 °C	70	105	sec
Time maintained above 230 °C	40	60	sec
Peak package body temperature	230	250	°C
Time maintained above 217 °C	60	110	sec

5.4. Labeling



Figure 20. Label form

5.5. Thermal considerations

Ambient operating temperature: $-25\text{ }^{\circ}\text{C}$ to $+75\text{ }^{\circ}\text{C}$

($-20\text{ }^{\circ}\text{C}$ to $+60\text{ }^{\circ}\text{C}$ fully compliant with 3GPP; $-25\text{ }^{\circ}\text{C}$ to $+75\text{ }^{\circ}\text{C}$ functional work)

Ambient storage temperature: $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

The case temperature of module shielding cover must be $< 85\text{ }^{\circ}\text{C}$ when integrated to prevent damage.

Design points used to improve the thermal performance:

- It's better to add a naked copper area onto IMA3 module back side of the PCB. If the thermal performance becomes an issue in the customer's product, add thermal solutions for improvement such as a thermal pad or a heat sink.
- It's recommended to have a thermal pad or a heat sink on shielding cover to help transfer heat.
- If systems with IMA3 module embedded intend to work under ambient temperatures as low as -40°C , it's suggested that:
 1. SIM Card need to be well arranged to make sure it is functional at the condition of ambient temperature as low as -40°C .
 2. Adding heating circuit on board design, the circuit mainly consists of temperature sensing unit, heating element and control unit.

6. Regulatory and Industry Approvals

6.1. Certification testing

PTCRB, FCC and AT&T TA

6.2. Safety and hazards

Be sure the use of this product is allowed in the country and in the environment required.

The use of this product may be dangerous and must be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, and aircraft
- Where there is a risk of explosion such as gasoline stations and oil refineries

It is the responsibility of the user to comply with his or her country's regulations and the specific environmental regulations.

Do not disassemble the product; any mark of tampering will compromise the warranty's validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product must be supplied with a stabilized voltage source, and the wiring must conform to the security and fire-prevention regulations.

This product must be handled with care; avoid any contact with the pins because electrostatic discharge may damage the product. Same caution must be taken regarding the SIM card; carefully check the instructions for its use. Do not insert or remove the SIM when the product is in power-saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care must be taken for the external components of the module as well as for project or installation issues—there may be a risk of disturbing the GSM network or external devices or of having an impact on device security. If you have any doubts, please refer to the technical documentation and the relevant regulations in force.

Every module must be equipped with a proper antenna with specific characteristics. The antenna must be installed with care in order to avoid any interference with other electronic devices.

7. Packaging

The IMA3 modules are delivered in tape and reel.

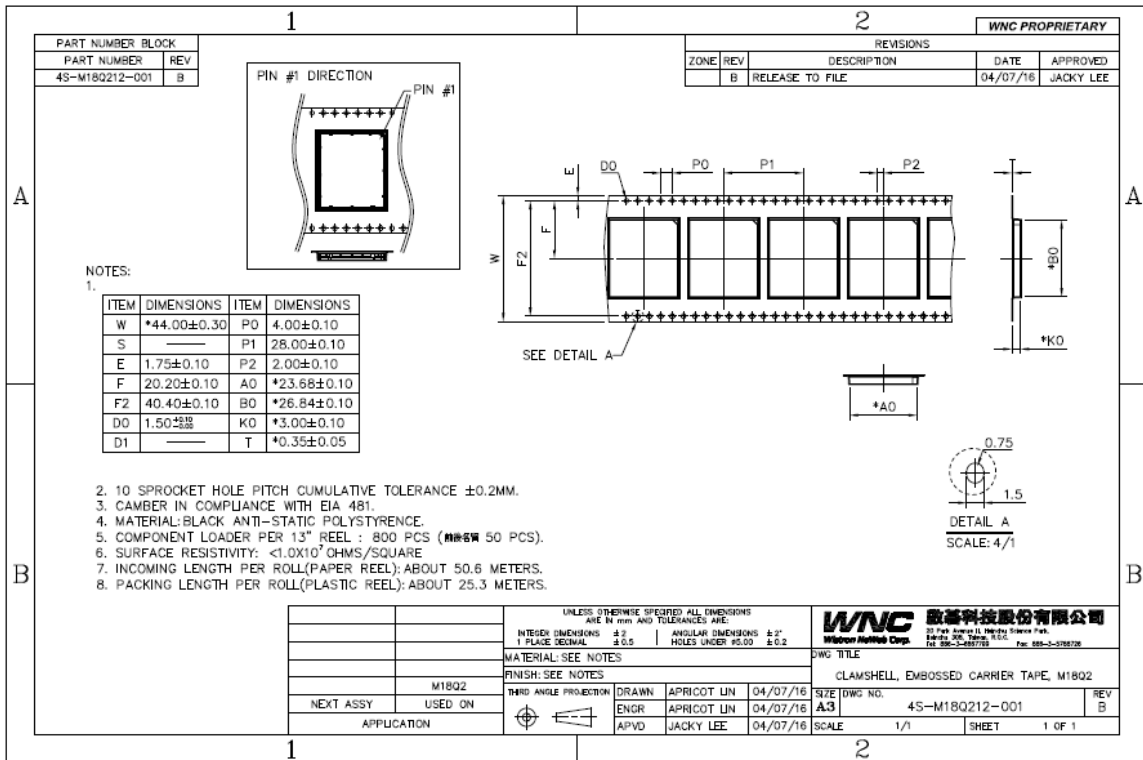


Figure 21. Packing-Tape

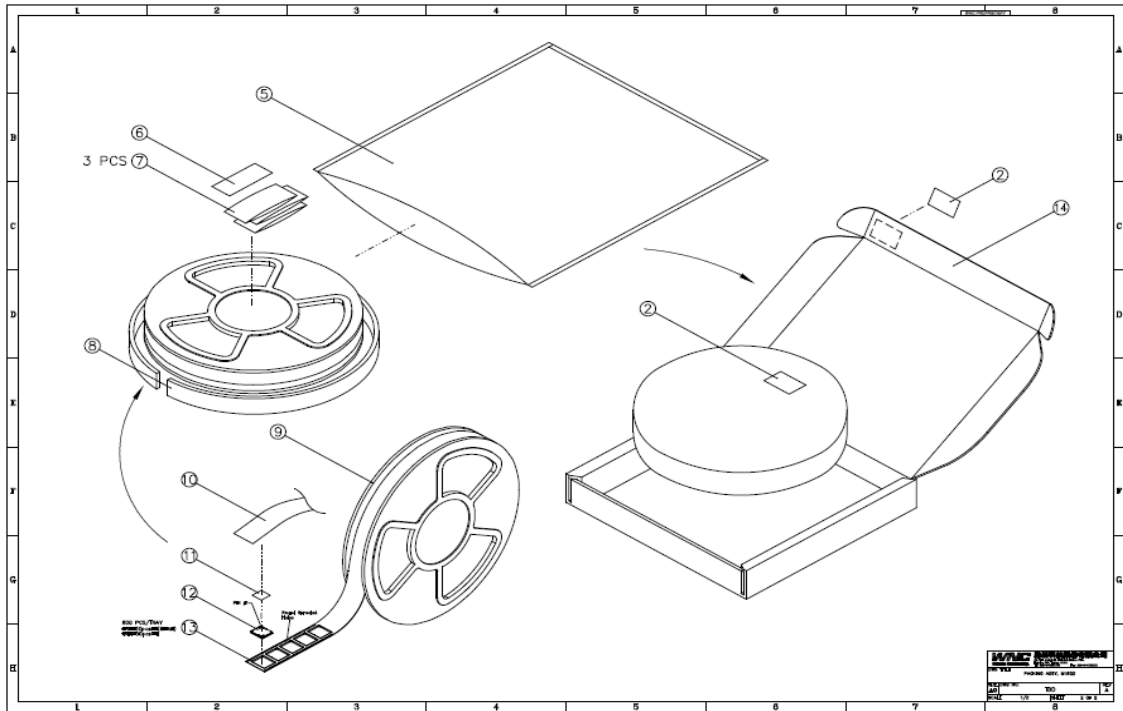


Figure 22. Packing—reel

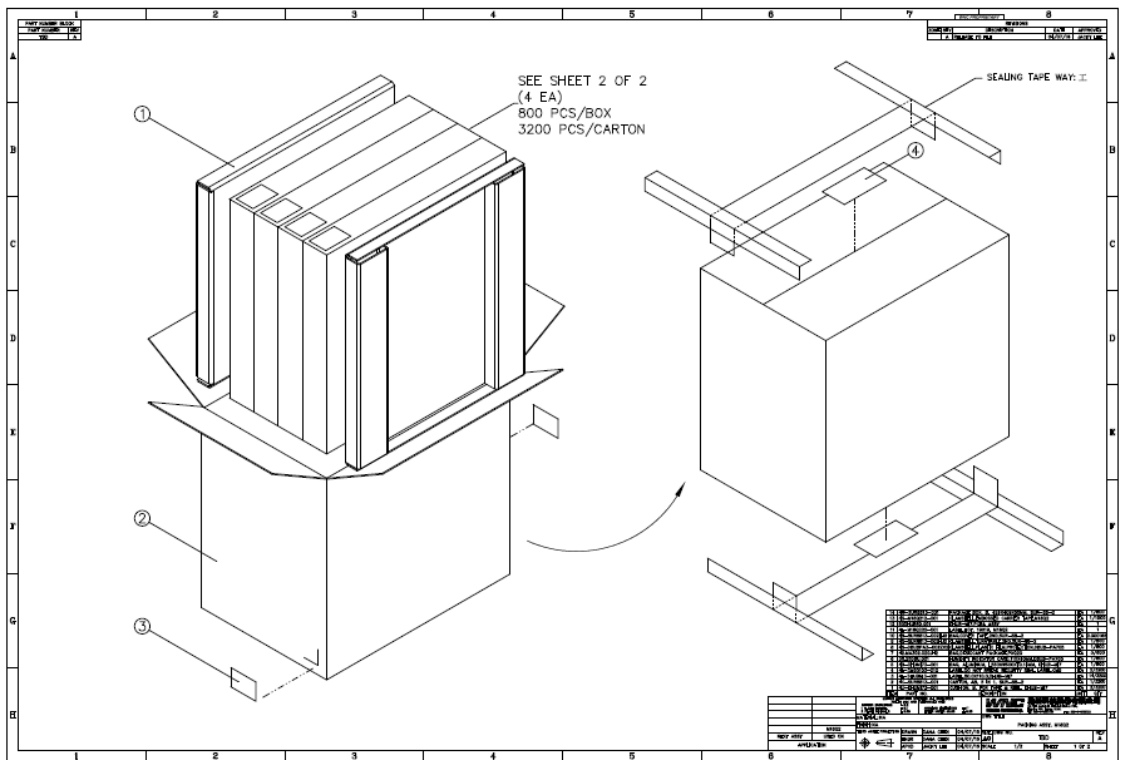


Figure 23. Packing—carton

8. Safety Recommendation

Be sure the use of this product is allowed in the country and in the environment required.

The use of this product may be dangerous and must be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, and aircraft
- Where there is a risk of explosion such as gasoline stations and oil refineries

It is the responsibility of the user to comply with the his or her country's regulations and the specific environmental regulations.

Do not disassemble the product; any mark of tampering will compromise the warranty's validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product must be supplied with a stabilized voltage source, and the wiring must conform to the security and fire-prevention regulations.

This product must be handled with care; avoid any contact with the pins because electrostatic discharge may damage the product. Same caution must be taken regarding the SIM card; carefully check the instructions for its use. Do not insert or remove the SIM when the product is in power-saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care must be taken for the external components of the module as well as for project or installation issues—there may be a risk of disturbing the GSM network or external devices or of having an impact on device security. If you have any doubts, please refer to the technical documentation and the relevant regulations in force.

Every module must be equipped with a proper antenna with specific characteristics. The antenna must be installed with care in order to avoid any interference with other electronic devices.

9. Appendix

In order to describe more detailed about the I/O default setting while entering Sleep or Hibernation is as below table.

Table 18. I/O default setting table

Pin No.	Signal Name	Type	Default setting in Normal mode	Default Setting while entering Sleep or Hibernation
15	RF_1	AI/AO	-	-
21	RF_2	AI	-	-
46	PCM_SYNC/GPIO46	DI/DO	PD	PD
47	PCM_IN/GPIO47	DI	PU	PU
48	PCM_OUT/GPIO48	DO	PU	PU
49	PCM_CLK/GPIO49	DO	PD	PD
52	GPIO01	DI/DO	PD	PD
53	GPIO02	DI/DO	PD	PD
54	GPIO03	DI/DO	PD	PD
55	GPIO04	DI/DO	PD	PD
60	I2C_SDA	DI/DO	PU	PU
61	I2C_SCL	DO	PU	PU
80	UART1_CTS (UART1)	DI	PD	PU
81	UART1_RTS (UART1)	DO	PD	NP
82	UART1_RX (UART1)	DI	PU	PU
83	UART1_TX (UART1)	DO	PU	PU
86	USB_Dp	DI/DO	-	-
87	GPIO87	DI/DO	PD	PD
88	USB_Dn	DI/DO	-	-
93	GPIO93	DI/DO	PU	PU
94	GPIO94	DI/DO	PD	PD
95	GPIO95	DI/DO	PD	PD
96	GPIO96	DI/DO	PD	PD
97	GPIO97	DI/DO	PU	PU

106	UART2_RX (UART2)	DI	PU	PU
107	UART2_TX (UART2)	DO	PU	PU
122	ADC	AI	PU	PU
125	SPI_MOSI	DO	PU	PU
126	SPI_MISO	DI	PU	PU
127	SPI_EN	DO	PD	PU
128	SPI_CLK	DO	PD	PD
129	GPIO05	DI/DO	PD	PD
130	GPIO06	DI/DO	PD	PD
131	GPIO07	DI/DO	PD	PD
132	GPIO08	DI/DO	PD	PD
134	UIM_DATA	DI/DO	PU	PU
135	UIM_CLK	DO	PU	NP
136	UIM_RESET	DO	PU	NP
137	UIM_DETECT	DI/DO	PU	NP
141	WWAN_STATE	DO	PD	PD
142	POWER_ON	DI	PD	PD
143	WAKEUP_OUT	DO	PD	PD
144	WAKEUP_IN	DI	PU	PD
145	RESET	DI	PU	PU
201	JTAG_TCK	DI	PD	PD
202	JTAG_TDI	DI	PD	PD
203	JTAG_TDO	DO	PU	PU
204	JTAG_TMS	DI	PD	PD
205	JTAG_TRST_N	DI	PD	PD