Wistron NeWeb Corp.

UMC-MT2731C
Product Specification

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1 General features

UMC-MT2731C is the 254-pin contacting LGA type NAD(Network Access Device) suitable for automotive applications based on its LTE/WCDMA/GSM communication features. For the worldwide market, WNC has three regional variants that have dedicated RAT supporting band designed as below
NA for North America region
EU for Europe region
ROW means Rest-of-World to cover countries that out of NA and EU region

1.1 Regional variant

RAT\Variant	EU	NA
GSM/EDGE/GPRS	900 and 1800	850 and 1900
WCDMA	Not Supported	Not Supported
LTE Low Band	Band8, 20 and 28	Band26(5) ,12(17),B14
LTE Middle Band	Band1 and 3	Band25(2) and 66(4)
LTE High Band	Band7	Band7

1.2 Performance key features

Key Features\Variant	EU	NA
M/N	UMC-MT2731CDJ	UMC-MT2731CBN
CPU/GPU	MTK/MT2731V/COA	MTK/MT2731V/COA
RF IC	MTK/MT6177AW/COC	MTK/MT6177AW/COC
Power Management	MTK/MT6389V/COA	MTK/MT6389V/COA
Primary Antenna	GSM/LTE; transmitting and reviving	GSM/LTE; transmitting and reviving
Diversity Antenna	LTE; receiving only	LTE; receiving only
Maximum Data Rate	LTE Category 6	LTE Category 6
LTE Downlink CA(Intra)	CA_1-1, CA_3-3 and CA_7-7	CA_2-2, CA_4-4 and CA_7-7
LTE Downlink CA(Inter)	Not Supported	Not Supported
LTE Uplink CA	Not Supported	Not Supported
GNSS L1	Not Supported	Not Supported
LTE Power Class	3	3

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1.3 Interface

1.3.1 Signal interface

UMC-MT2731C has signal interfaces as showed as below table. Developer could use these interfaces to communicate with NAD or debugging

Interface	Amount	Description
USB 3.1	1 set	USB 3.1 supports the device mode only
USB 2.0 OTG	1 set	support the device or the host mode
I2C	1 set	for I2C communication
I2S	1 set	for the digital audio interface
Audio(analog)	2 sets	for the analog audio interface; consisting of two audio DACs with Mono data stream and two line-out drivers
UART	4 sets	2 sets with CTS/RTS pin
MSDC	3 sets	1 set with 8-bit data lines, dedicated for eMMC; the other 2 sets with 4-bit data lines
JTAG	1 set	for the firmware upgrade and the debugging
SPI	1 set	support IN and OUT, MASTER and SLAVE mode. 3.3V IO
SIM	2 sets	SIM interface(Due to SOC limit,only support DSSS with inserting one SIM once)
ADC	4 pins	ADC channel with 12-bit resolution

1.3.2 GPIO

Interface	Description
GPIO(1.8V)	18 pins
GPIO(3.3V)	23 pins

1.3.3 Antenna interface

Interface	Description
Primary Antenna	1 pin for LTE/WCDMA/GSM primary transmitting and receiving
Diversity Antenna	1 pin for LTE and WCDMA diversity receiving

1.3.4 Power input interface

Interface	Description
VSYS	2 pins. NAD main supply voltage source
VBUS	1 pin. 5.0V input for USB detection (typ 5V, max:10.5V)

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1.3.5 Power output interface

Interface	Description
VEMC_PMU	1 pin. 3.0V output, max current 800mA. For eMMC
VIO33_PMU	1 pin. 3.3V output, max current 100mA. For I/O or sensors
VCN33_PMU	1 pin. 3.3V output, max current 70mA. For Connectivity
VIO18_PMU	1 pin. 1.8V output, max current 200mA. For I/O or sensors
VCN18_PMU	1 pin. 1.8V output, max current 450mA. For Connectivity
VSIM1_PMU	1 pin. 1.86V output, max current 140mA. As SIM1 supply-feed
VSIM2_PMU	1 pin. 1.86V output, max current 140mA.

1.4 Operation condition

Parameter	Minimum	Typical	Maximum	Unit
Storage Temperature Range	-40	-	85	°C
3GPP RF Performance Temperature Range	-20	-	70	°C
Operating Temperature Range	-40	-	85	°C
Power Supply Voltage(VSYS)	3.8	4	4.2	V
ESD Voltage(Human Body Model)	-	-	2000	V
ESD Voltage(Charge Device Model)	-	-	500	V
Operation Humidity	0	-	95	%RH
Current Consumption				
Sleep(Airplane/Flight/Suspended mode)	-	2.11		mA
GSM standby 1.18 sec	-	3.50		mA
WCDMA standby 2.56 sec	-	3.32		mA
LTE FDD CDRX standby(10-MHz/320-ms)	-	3.14		mA
GSM talk 11-dBm; no DTX, P-GSM	-	159.42		mA
WCDMA talk 5-dBm; IMT	-	216.72		mA
VoLTE FDD(40-ms DRX cycle/0-dBm)	-	280		mA
LTE Cat 4(150/50-Mbps, 5-dBm, Band7)	-	348.62		mA
LTE Cat 6(300/50-Mbps,5-dBm, Band7)	-	368		mA

1.5 Mechanical specification

Parameter	Min	Typ.	Max	Unit
Length	36.7	36.8	37.05	MM
Width	41.9	42	42.25	MM
Height(with shielding case)	2.93	3.23	3.53	MM
Weight(with shielding case)	9	10	11	g
Module co-planarity	0	-	100	UM

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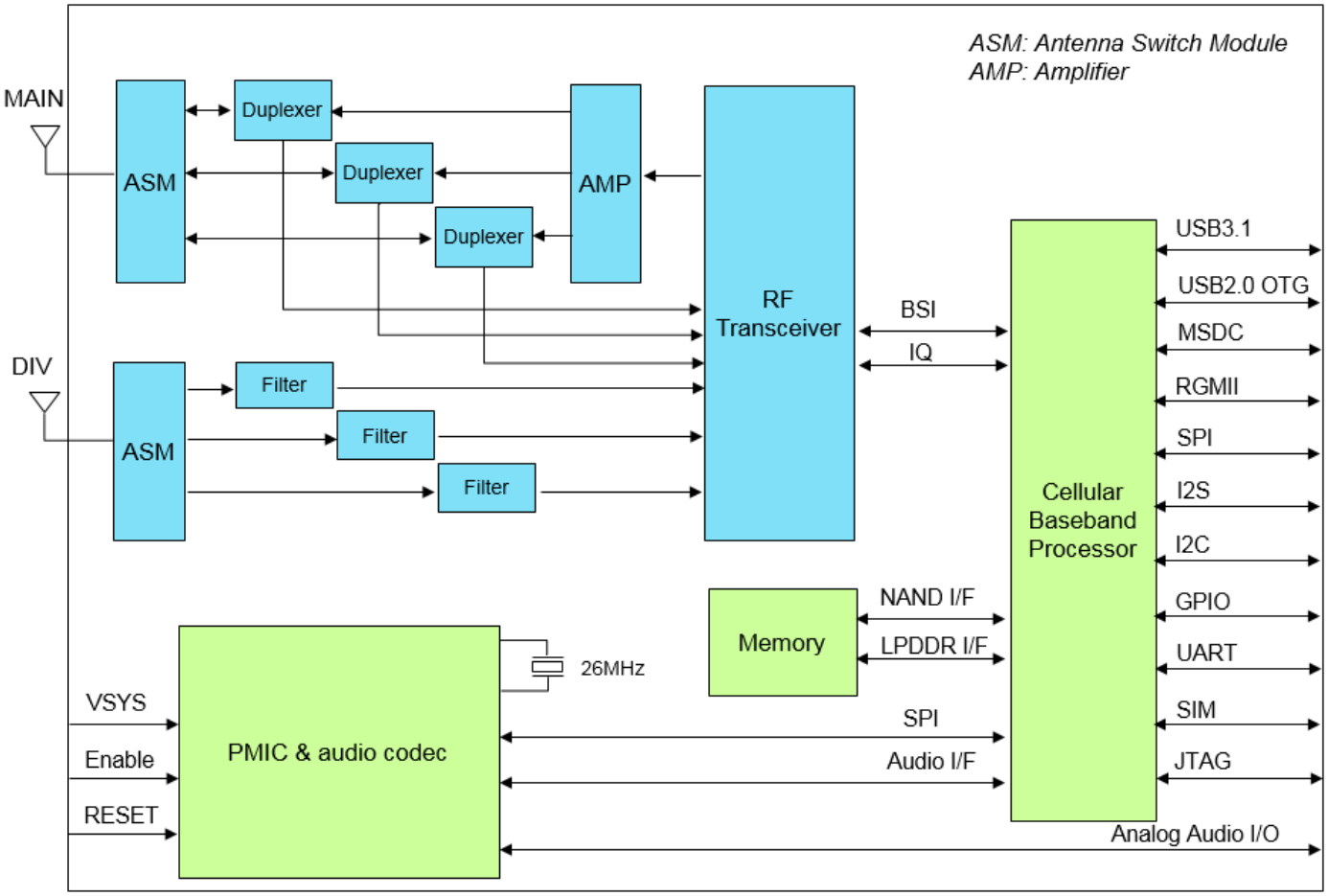
2 Block diagram

2.1 UMC-MT2731C block diagram



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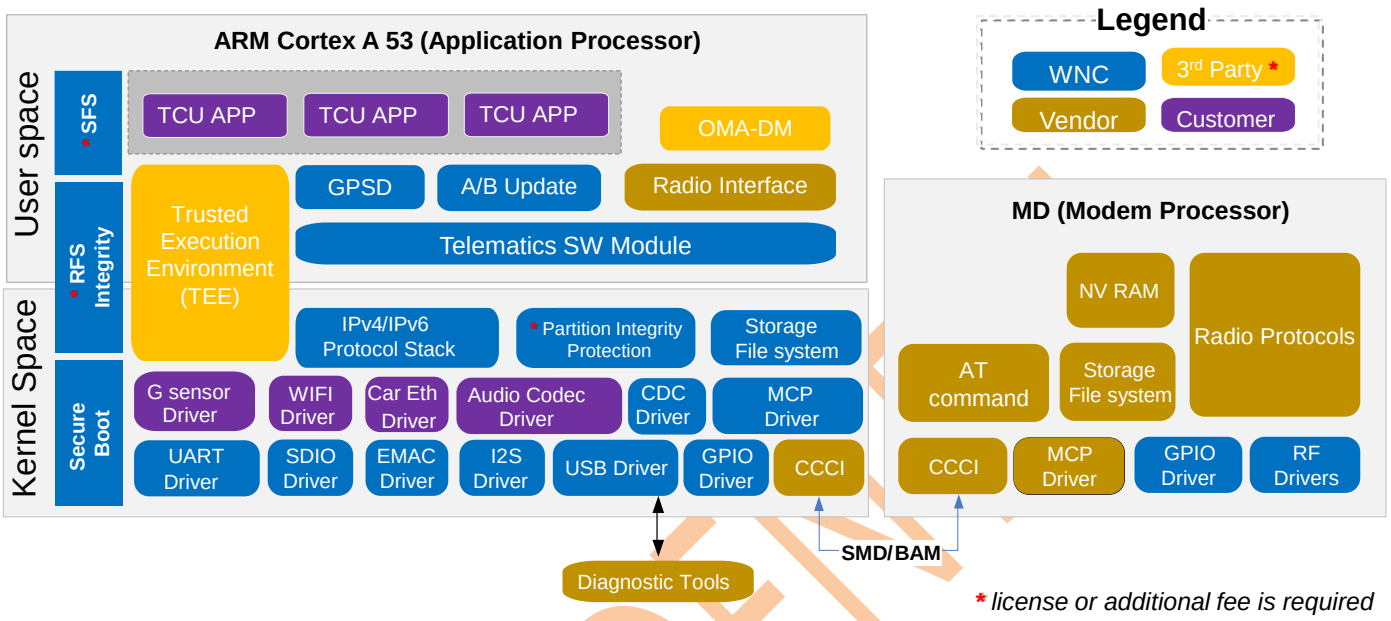
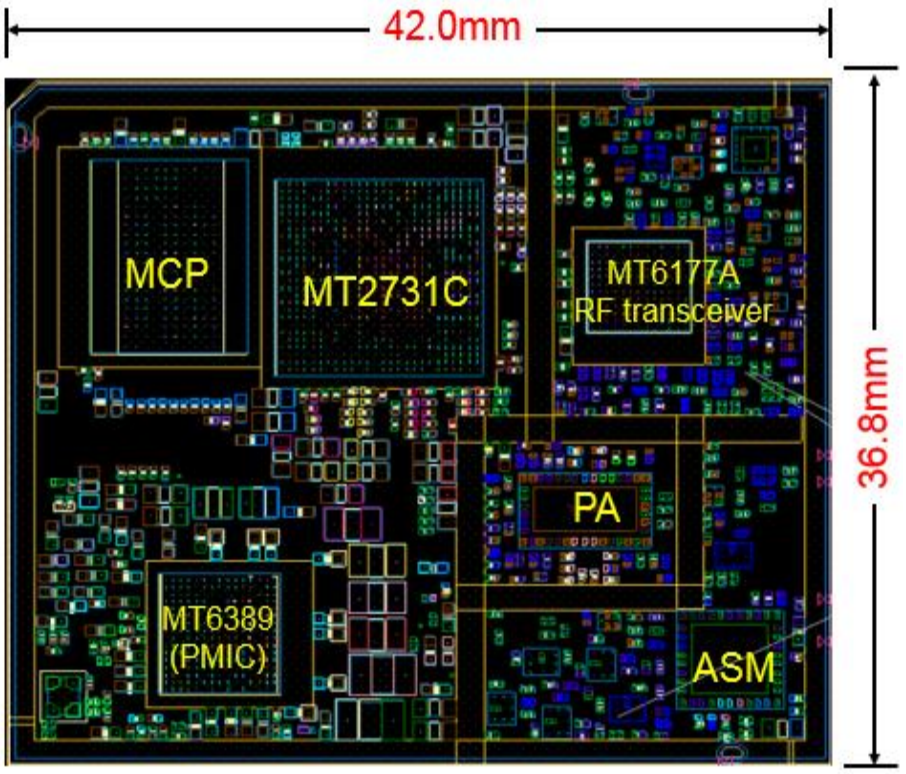
2.2 Software stack

Figure shows the software stack on MTK/MT2731 platform working on LINUX operation system which Kernel version is 4.14. For telephony, NAD supports not only voice calls but also SMS over CS and IMS



3 Board placement

3.1 Top side



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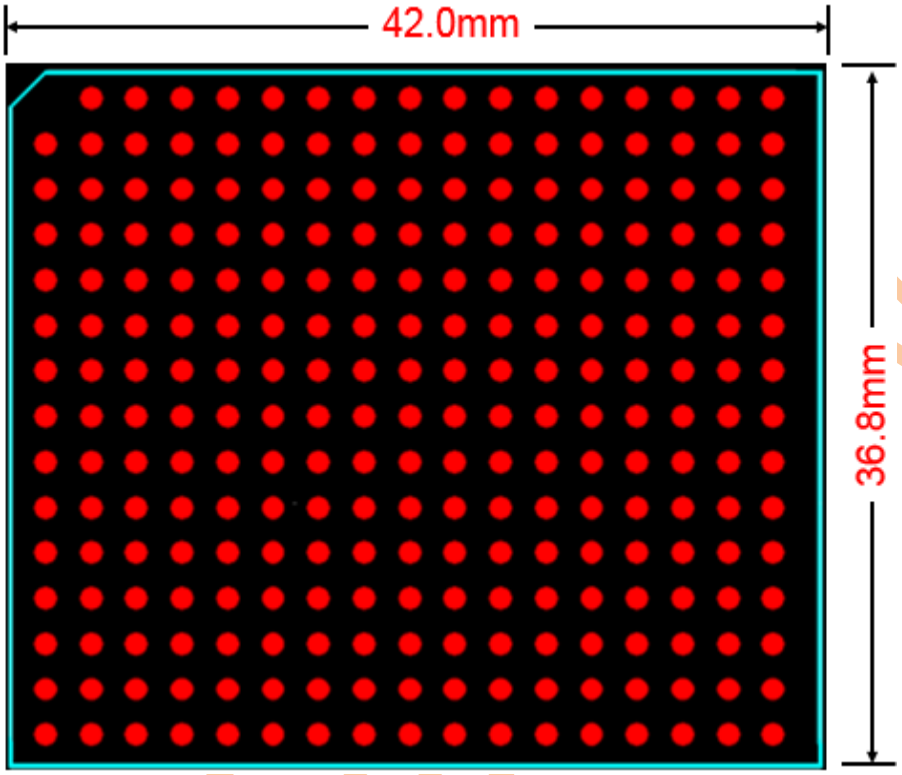
3.2 Bottom side

(Top to Bottom View)Round pads of LGA contacting



3.3 Pin diagram

Top to Bottom View(X-ray View)

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A		GPIO46_1V8	GND	SS_USB_TXP	SS_USB_TXN	SS_USB_RXN	SS_USB_RXP	GND	USB_DM_P1	USB_DP_P1	KPCOL0	IDDIG	I2S0_MCK	GND	GPIO13_3V3	GPIO1_1V8	GPIO15_3V3	A
B	MSDC0_RSTB	MSDC0_DSL	GPIO45_1V8	GPIO44_1V8	NC	NC	GND	USB_DM_P0	USB_DP_P0	GND	GPIO43_3V3	GPIO28_1V8	URTS2	UCTS2	GPIO14_3V3	GND	GND	B
C	MSDC0_DAT7	MSDC0_CLK	GND	I2S0_DI	MSDC2_CLK	MSDC2_DAT0	MSDC2_DAT3	MSDC2_DSL	GND	PCM_OUT	PCM_CLK	PCM_SYNC	URXD2	UTXD2	SPI_CLK_3V3	GND	ANT_DRX	C
D	MSDC0_DAT5	MSDC0_CMD	UTXD0	URXD0	MSDC2_CMD	MSDC2_DAT2	GND	MSDC1_DAT1	MSDC1_DAT3	SDA0	PCM_IN	GND	GND	GND	GPIO0_1V8	GND	GND	D
E	MSDC0_DAT6	MSDC0_DAT2	GPIO18_1V8	GPIO19_1V8	MSDC2_DAT1	TEMP_URXD	TEMP_UTXD	MSDC1_CMD	MSDC1_DAT0	GND	SCL0	GND	GND	GND	GND	META_MODE	GPIO8_1V8	E
F	MSDC0_DAT0	MSDC0_DAT3	I2S0_BCK	I2S0_LRCK	I2S0_DO	AGPS_SYNC	GND	GND	MSDC1_DAT2	MSDC1_CLK	LTE_COEX_TX_1V8	LTE_COEX_RX_1V8	GND	GND	GND	SPI1_A_CS1A	SPI1_A_MO	F
G	GND	MSDC0_DAT1	MSDC0_DAT4	GND	GPIO132_3V3	GND	GND	GND	GPIO11_1V8	GPIO10_1V8	GND	GPIO2_1V8	GPIO9_1V8	GND	JTMS	JTRSTB	SPI1_A_MI	G
H	GPIO119_3V3	GPIO117_3V3	GPIO124_3V3	GPIO129_3V3	GPIO130_3V3	GND	SYSRSTB	GND	GPIO12_1V8	GPIO90_1V8	GND	GND	GND	JTDI	JTDO	JTCK	GND	H
J	GPIO118_3V3	GPIO127_3V3	GPIO116_3V3	GPIO128_3V3	GPIO133_3V3	GPIO123_3V3	GND	GND	GPIO88_1V8	GPIO87_1V8	GND	GND	GND	GND	GND	GND	GND	J
K	VEMC_PMU	GND	GND	GPIO122_3V3	GPIO126_3V3	GPIO121_3V3	GPIO131_3V3	GND	GND	GPIO89_1V8	GND	GND	GND	GND	GND	AUXADC_VIN2	GND	K
L	GND	VIO33_PMU	VSIM1_PMU	VBUS	GPIO125_3V3	GPIO120_3V3	GND	GPI146_3V3	GND	GND	GND	GND	GND	GND	GND	GND	GND	L
M	VCN33_PMU	VSIM2_PMU	VRTC28	GND	GND	GND	WATCHDOG	PMIC_STATUS_B	GND	GND	GND	GND	GND	GND	GND	GND	GND	M
N	VIO18_PMU	AUDIO_IN2_P	GND	GND	GND	GND	SRCLKENA0	GND	GND	SIM2_SIO	GND	UTXD1	GND	GND	GND	GND	ANT_PTRX	N
P	AUDIO_IN1_N	AUDIO_IN2_N	AUDIO_OUT2_N	AUDIO_OUT2_P	GND	PMIC_ENB	PMIC_RESET_B	GND	SIM2_SCLK	SIM2_SRST	URXD1	UCTS1	GND	GND	GND	GND	GND	P
Q	AUDIO_IN1_P	AUDIO_OUT1_N	AUDIO_OUT1_P	VCN18_PMU	GND	VSYS	VSYS	GND	SIM1_SIO	SIM1_SCLK	SIM1_SRST	URTS1	RTC_CLK	AUXADC_VIN4	AUXADC_VIN6	AUXADC_VIN8	GND	Q
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

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3.4 Pin definition table

NC: No Connection
PD: Pull Down
PU: Pull Up

NOTE1 All unused pins should be assigned as “No Connection” on the application board
NOTE2 Internal pull-up/pull-up resistor of GPIO pins in MT2731
Type1 I/O：Internal resistance could be 3 options (10k-OHM, 50K-OHM, and 10K-OHM||50K-OHM) so far for GPIO30~36, GPIO59~64,GPIO110~115, GPIO134~145.
Type2 I/O：75K-OHM is a typical value (in the range of 40K-OHM~190K-OHM) for others I/O that cannot be configured to different resistance.

NOTE(*) In the specified software(Part#: 53tbc), NAD pin#L8 is no longer being a GPI pin as default and configured as ”MCU_RESET_B” to support following reset function
This pin is triggered high to close application software firstly, and then to do the reset of PMIC for rebooting NAD after the power-off/-on sequence

NAD Pin#	Symbol Name	Power Domain	Voltage	Internal Pull State	MT2731 Pin-out	GPIO	Description
A2	GPIO46_1V8	DVDD18	1.8V	PD	F22	GPIO46	
A3	GND				n/a		
A4	SS_USB_TXP	AVDD18_PCIE	1.8V		D26		SS-USB interface signal
A5	SS_USB_TXN	AVDD18_PCIE	1.8V		D25		SS-USB interface signal
A6	SS_USB_RXN	AVDD18_PCIE	1.8V		G25		SS-USB interface signal
A7	SS_USB_RXP	AVDD18_PCIE	1.8V		G26		SS-USB interface signal
A8	GND				n/a		
A9	USB_DM_P1	AVDD33_USB	3.3V		J25		USB 2.0 differential pair signal
A10	USB_DP_P1	AVDD33_USB	3.3V		J24		USB 2.0 differential pair signal
A11	KPCOL0	DVDD18	1.8V	PU	AD23	GPIO58	Pull this pin low to force NAD being USB Download Mode for the software upgrade
A12	IDDIG	DVDD18	1.8V	PD	P26	GPIO25	ID pin of USB 2.0 OTG interface
A13	I2S0_MCK	DVDD18	1.8V	PD	N26	GPIO24	I2S interface signal
A14	GND				n/a		
A15	GPIO13_3V3	DVDD28	3.3V	PD	AA24	GPIO13	
A16	GPIO1_1V8	DVDD18	1.8V	PD	M26	GPIO1	
A17	GPIO15_3V3	DVDD28	3.3V	PD	AB24	GPIO15	
B1	MSDC0_RSTB	DVDD18	1.8V	PU	G3	GPIO140	8-bits SDIO for eMMC
B2	MSDC0_DSL	DVDD18	1.8V	PD	F5	GPIO137	8-bits SDIO for eMMC
B3	GPIO45_1V8	DVDD18	1.8V	PD	G23	GPIO45	
B4	GPIO44_1V8	DVDD18	1.8V	PD	G22	GPIO44	
B5	NC	AVDD18_PCIE	1.8V		E24		

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B6	NC	AVDD18_PCIE	1.8V		F24		
B7	GND				n/a		
B8	USB_DM_P0	AVDD33_USB	3.3V		K26		USB 2.0 OTG differential pair signal
B9	USB_DP_P0	AVDD33_USB	3.3V		K25		USB 2.0 OTG differential pair signal
B10	GND				n/a		
B11	GPIO43_3V3	DVDD28	3.3V	PD	Y24	GPIO43	
B12	GPIO28_1V8	DVDD18	1.8V	PD	P25	GPIO28	
B13	URTS2	DVDD28	3.3V	PD	AA22	GPIO49	UART interface signal
B14	UCTS2	DVDD28	3.3V	PD	AA23	GPIO47	UART interface signal
B15	GPIO14_3V3	DVDD28	3.3V	PD	AB25	GPIO14	
B16	GND				n/a		
B17	GND				n/a		
C1	MSDC0_DAT7	DVDD18	1.8V	PU	J2	GPIO136	8-bits SDIO for eMMC
C2	MSDC0_CLK	DVDD18	1.8V	PD	H6	GPIO138	8-bits SDIO for eMMC
C3	GND				n/a		
C4	I2S0_DI	DVDD18	1.8V	PD	N25	GPIO22	I2S interface signal
C5	MSDC2_CLK	DVDD18	1.8V	PD	R25	GPIO31	4-bits SDIO
C6	MSDC2_DAT0	DVDD18	1.8V	PD	U24	GPIO36	4-bits SDIO
C7	MSDC2_DAT3	DVDD18	1.8V	PD	V26	GPIO33	4-bits SDIO
C8	MSDC2_DSL	DVDD18	1.8V	PD	R24	GPIO30	4-bits SDIO
C9	GND				n/a		
C10	PCM_OUT	DVDD28	3.3V	PU	Y25	GPIO40	Reserved interface for MT6630
C11	PCM_CLK	DVDD28	3.3V	PU	Y23	GPIO37	Reserved interface for MT6630
C12	PCM_SYNC	DVDD28	3.3V	PU	W23	GPIO38	Reserved interface for MT6630
C13	URXD2	DVDD28	3.3V	PD	AC23	GPIO48	UART interface signal
C14	UTXD2	DVDD28	3.3V	PD	AB22	GPIO50	UART interface signal
C15	SPI_CLK_3V3	DVDD28	3.3V	PD	AC25	GPIO7	SPI interface signal
C16	GND				n/a		
C17	ANT_DRX						RF diversity antenna port
D1	MSDC0_DAT5	DVDD18	1.8V	PU	F2	GPIO135	8-bits SDIO for eMMC
D2	MSDC0_CMD	DVDD18	1.8V	PU	H5	GPIO142	8-bits SDIO for eMMC
D3	UTXD0	DVDD18	1.8V	PU	L24	GPIO17	UART interface signal
D4	URXD0	DVDD18	1.8V	PU	L23	GPIO16	UART interface signal
D5	MSDC2_CMD	DVDD18	1.8V	PD	T24	GPIO32	4-bits SDIO
D6	MSDC2_DAT2	DVDD18	1.8V	PD	V25	GPIO34	4-bits SDIO
D7	GND				n/a		
D8	MSDC1_DAT1	DVDD18	1.8V	PD	AC19	GPIO62	4-bits SDIO
D9	MSDC1_DAT3	DVDD18	1.8V	PD	AF20	GPIO60	4-bits SDIO
D10	SDA0	DVDD28	3.3V	PU	Y22	GPIO41	I2C interface signal
D11	PCM_IN	DVDD28	3.3V	PU	Y26	GPIO39	Reserved interface for MT6630
D12	GND				n/a		

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D13	GND				n/a		
D14	GND				n/a		
D15	GPIO0_1V8	DVDD18	1.8V	PU	M25	GPIO0	
D16	GND				n/a		
D17	GND				n/a		
E1	MSDC0_DAT6	DVDD18	1.8V	PU	H1	GPIO134	8-bits SDIO for eMMC
E2	MSDC0_DAT2	DVDD18	1.8V	PU	H2	GPIO143	8-bits SDIO for eMMC
E3	GPIO18_1V8	DVDD18	1.8V	PD	M24	GPIO18	
E4	GPIO19_1V8	DVDD18	1.8V	PD	M23	GPIO19	
E5	MSDC2_DAT1	DVDD18	1.8V	PD	U25	GPIO35	4-bits SDIO
E6	TEMP_URXD	DVDD18	1.8V	PD	T22	GPIO27	UART interface signal
E7	TEMP_UTXD	DVDD18	1.8V	PD	T21	GPIO26	UART interface signal
E8	MSDC1_CMD	DVDD18	1.8V	PD	AD20	GPIO59	4-bits SDIO
E9	MSDC1_DAT0	DVDD18	1.8V	PD	AD19	GPIO63	4-bits SDIO
E10	GND				n/a		
E11	SCL0	DVDD28	3.3V	PU	W21	GPIO42	I2C interface signal
E12	GND				n/a		
E13	GND				n/a		
E14	GND				n/a		
E15	GND				n/a		
E16	META_MODE	DVDD18	1.8V	PD	AE23	GPIO3	Before and after NAD power-on-booting/rebooting, pull this pin low to force NAD being META Mode for connecting META tool
E17	GPIO8_1V8	DVDD18	1.8V	PD	AF23	GPIO8	
F1	MSDC0_DAT0	DVDD18	1.8V	PU	F1	GPIO141	8-bits SDIO for eMMC
F2	MSDC0_DAT3	DVDD18	1.8V	PU	F4	GPIO139	8-bits SDIO for eMMC
F3	I2S0_BCK	DVDD18	1.8V	PD	P23	GPIO20	I2S interface signal
F4	I2S0_LRCK	DVDD18	1.8V	PD	N24	GPIO21	I2S interface signal
F5	I2S0_DO	DVDD18	1.8V	PD	N23	GPIO23	I2S interface signal
F6	AGPS_SYNC	DVDD18	1.8V	PD	R23	GPIO29	Reserved interface for MT6630
F7	GND				n/a		
F8	GND				n/a		
F9	MSDC1_DAT2	DVDD18	1.8V	PD	AE20	GPIO61	4-bits SDIO
F10	MSDC1_CLK	DVDD18	1.8V	PD	AE19	GPIO64	4-bits SDIO
F11	LTE_COEX_TX_1V8	DVDD18	1.8V	PD	V23	GPIO56	Reserved interface for IDC connection of MT6630
F12	LTE_COEX_RX_1V8	DVDD18	1.8V	PD	V22	GPIO57	Reserved interface for IDC connection of MT6630
F13	GND				n/a		
F14	GND				n/a		
F15	GND				n/a		

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F16	SPI1_A_CS1A	DVDD28	3.3V	PD	AC26	GPIO6	SPI interface signal
F17	SPI1_A_MO	DVDD28	3.3V	PD	AD25	GPIO5	SPI interface signal
G1	GND				n/a		
G2	MSDC0_DAT1	DVDD18	1.8V	PU	G2	GPIO145	8-bits SDIO for eMMC
G3	MSDC0_DAT4	DVDD18	1.8V	PU	F3	GPIO144	8-bits SDIO for eMMC
G4	GND				n/a		
G5	GPIO132_3V3	DVDD28	3.3V	PD	L2	GPIO132	
G6	GND				n/a		
G7	GND				n/a		
G8	GND				n/a		
G9	GPIO11_1V8	DVDD18	1.8V	PD	AB2	GPIO11	
G10	GPIO10_1V8	DVDD18	1.8V	PD	AC4	GPIO10	
G11	GND				n/a		
G12	GPIO2_1V8	DVDD18	1.8V	PD	V21	GPIO2	
G13	GPIO9_1V8	DVDD18	1.8V	PD	AE18	GPIO9	
G14	GND				n/a		
G15	JTMS	DVDD18	1.8V	PD	AE25	GPIO51	JTAG debugging interface
G16	JTRSTB	DVDD18	1.8V	PD	AC24	GPIO55	JTAG debugging interface
G17	SPI1_A_MI	DVDD28	3.3V	PD	AD26	GPIO4	SPI interface signal
H1	GPIO119_3V3	DVDD28	3.3V	PD	N5	GPIO119	
H2	GPIO117_3V3	DVDD28	3.3V	PD	M4	GPIO117	
H3	GPIO124_3V3	DVDD28	3.3V	PD	L4	GPIO124	
H4	GPIO129_3V3	DVDD28	3.3V	PD	L3	GPIO129	
H5	GPIO130_3V3	DVDD28	3.3V	PD	M2	GPIO130	
H6	GND				n/a		
H7	SYSRSTB		0 to 1.98V		PMIC		Pull this pin low to reset NAD
H8	GND				n/a		
H9	GPIO12_1V8	DVDD18	1.8V	PD	Y5	GPIO12	
H10	GPIO90_1V8	DVDD18	1.8V	PD	AE4	GPIO90	
H11	GND				n/a		
H12	GND				n/a		
H13	GND				n/a		
H14	JTDI	DVDD18	1.8V	PD	AE24	GPIO53	JTAG debugging interface
H15	JTDO	DVDD18	1.8V	PD	AF24	GPIO54	JTAG debugging interface
H16	JTCK	DVDD18	1.8V	PD	AD24	GPIO52	JTAG debugging interface
H17	GND				n/a		
J1	GPIO118_3V3	DVDD28	3.3V	PD	N4	GPIO118	
J2	GPIO127_3V3	DVDD28	3.3V	PD	N3	GPIO127	
J3	GPIO116_3V3	DVDD28	3.3V	PD	M1	GPIO116	
J4	GPIO128_3V3	DVDD28	3.3V	PD	K3	GPIO128	

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J5	GPIO133_3V3	DVDD28	3.3V	PD	K2	GPIO133	
J6	GPIO123_3V3	DVDD28	3.3V	PD	P1	GPIO123	
J7	GND				n/a		
J8	GND				n/a		
J9	GPIO88_1V8	DVDD18	1.8V	PD	AB5	GPIO88	
J10	GPIO87_1V8	DVDD18	1.8V	PD	AB6	GPIO87	
J11	GND				n/a		
J12	GND				n/a		
J13	GND				n/a		
J14	GND				n/a		
J15	GND				n/a		
J16	GND				n/a		
J17	GND				n/a		
K1	VEMC_PMU		3.0V		PMIC		3.0-Voltage source of the external eMMC; the maximum supply current is 0.8A
K2	GND				n/a		
K3	GND				n/a		
K4	GPIO122_3V3	DVDD28	3.3V	PD	P2	GPIO122	
K5	GPIO126_3V3	DVDD28	3.3V	PD	P3	GPIO126	
K6	GPIO121_3V3	DVDD28	3.3V	PD	R2	GPIO121	
K7	GPIO131_3V3	DVDD28	3.3V	PD	R3	GPIO131	
K8	GND				n/a		
K9	GND				n/a		
K10	GPIO89_1V8	DVDD18	1.8V	PD	AF4	GPIO89	
K11	GND				n/a		
K12	GND				n/a		
K13	GND				n/a		
K14	GND				n/a		
K15	GND				n/a		
K16	AUXADC_VIN2		0 to 1.98V		PMIC		PMIC ADC input with 12-bit A-to-D resolution
K17	GND				n/a		
L1	GND				n/a		
L2	VIO33_PMU		3.3V		PMIC		3.3-Voltage output source; the maximum supply current is 300-mA
L3	VSIM1_PMU		1.8V		PMIC		1.8-Volatge source of SIM1; the maximum supply current is 140-mA
L4	VBUS				PMIC		PMIC input pin for USB detection. In Sleep Mode, VBUS should be disconnected with NAD
L5	GPIO125_3V3	DVDD28	3.3V	PD	P5	GPIO125	
L6	GPIO120_3V3	DVDD28	3.3V	PD	R4	GPIO120	
L7	GND				n/a		

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L8	GPI146_3V3	DVDD28	3.3V	PD	T3	GPIO146	This pin only offers the input function and is not able to be configured as the output pin
L8*	MCU_RESET_B	DVDD28	3.3V	PD	T3	GPIO146	This pin is triggered low to close application software firstly, and then to do the reset of PMIC for rebooting NAD after the power-off/-on sequence
L9	GND				n/a		
L10	GND				n/a		
L11	GND				n/a		
L12	GND				n/a		
L13	GND				n/a		
L14	GND				n/a		
L15	GND				n/a		
L16	GND				n/a		
L17	GND				n/a		
M1	VCN33_PMU		3.3V		PMIC		3.3-Voltage output source reserved for MT6630; the maximum supply current is 70-mA
M2	VSIM2_PMU		1.8V		PMIC		1.8-Volatge source of SIM2; the maximum supply current is 140-mA
M3	VRTC28		2.8V		PMIC		2.8-Voltage source of RTC; the maximum supply current is 2-mA
M4	GND				n/a		
M5	GND				n/a		
M6	GND				n/a		
M7	WATCHDOG	DVDD18	1.8V	PU	AD4	GPIO92	WATCHDOG trigger signal generated from MT2731
M8	PMIC_STATUS_B		0 to 5V		PMIC		When NAD system completed the booting up, PMIC will pull this pin low not only to inform MT2731 that PMIC is ready, but also as the outgoing status pin reporting NAD booting is ended This pin would be also connected to VSYS with the external pull-up resistor of 100K-OHM
M9	GND				n/a		
M10	GND				n/a		
M11	GND				n/a		
M12	GND				n/a		
M13	GND				n/a		
M14	GND				n/a		
M15	GND				n/a		
M16	GND				n/a		
M17	GND				n/a		
N1	VIO18_PMU		1.8V		PMIC		1.8-Voltage output source; the maximum supply current is 1000-mA

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N2	AUDIO_IN2_P		-1.5 to 1.5V		PMIC		Analog AUDIO Channel2 differential input pair(P/N); the minimum impedance loading at input is 7K-OHM
N3	GND				n/a		
N4	GND				n/a		
N5	GND				n/a		
N6	GND				n/a		
N7	SRCLKENA0	DVDD18	1.8V	PU	AA1	GPIO104	NAD status indicator; the state of HIGH for Normal Mode, as well as LOW for Sleep/Low Power Mode
N8	GND				n/a		
N9	GND				n/a		
N10	SIM2_SIO	DVDD28_SIM2	3.3V	PU	U1	GPIO10	SIM2 interface signal
N11	GND				n/a		
N12	UTXD1	DVDD18	1.8V	PD	AE3	GPIO93	UART interface signal
N13	GND				n/a		
N14	GND				n/a		
N15	GND				n/a		
N16	GND				n/a		
N17	ANT_PTRX						RF primary antenna port
P1	AUDIO_IN1_N		-1.5 to 1.5V		PMIC		Analog AUDIO Channel1 differential input pair(P/N); the minimum impedance loading at input is 7K-OHM
P2	AUDIO_IN2_N		-1.5 to 1.5V		PMIC		Analog AUDIO Channel2 differential input pair(P/N); the minimum impedance loading at input is 7K-OHM
P3	AUDIO_OUT2_N		-1.98V to 1.98V		PMIC		Analog AUDIO Channel2 differential output pair(P/N); the output loading is 10K-OHM w/ 1.58Vrms
P4	AUDIO_OUT2_P		-1.98V to 1.98V		PMIC		Analog AUDIO Channel2 differential output pair(P/N); the output loading is 10K-OHM w/ 1.58Vrms
P5	GND				PMIC		
P6	PMIC_ENB		0 to 5V		PMIC		Pull this pin low to power NAD off
P7	PMIC_RESET_B		0 to 5V		PMIC		Hardware reset, to pull this pin low to trigger the reset of PMIC for rebooting NAD after the power-off/-on sequence
P8	GND				n/a		
P9	SIM2_SCLK	DVDD28_SIM2	3.3V	PD	U2	GPIO112	SIM2 interface signal
P10	SIM2_SRST	DVDD28_SIM2	3.3V	PD	V2	GPIO111	SIM2 interface signal
P11	URXD1	DVDD18	1.8V	PD	AF2	GPIO94	UART interface signal
P12	UCTS1	DVDD18	1.8V	PD	AF3	GPIO95	UART interface signal
P13	GND				n/a		
P14	GND				n/a		
P15	GND				n/a		

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P16	GND				n/a		
P17	GND				n/a		
Q1	AUDIO_IN1_P		-1.5 to 1.5V		PMIC		Analog AUDIO Channel1 differential input pair(P/N); the minimum impedance loading at input is 7K-OHM
Q2	AUDIO_OUT1_N		-1.98V to 1.98V		PMIC		Analog AUDIO Channel1 differential output pair(P/N); the output loading is 10K-OHM w/ 1.58Vrms
Q3	AUDIO_OUT1_P		-1.98V to 1.98V		PMIC		Analog AUDIO Channel1 differential output pair(P/N); the output loading is 10K-OHM w/ 1.58Vrms
Q4	VCN18_PMU		1.8V		PMIC		1.8-Voltage output source reserved for MT6630; the maximum supply current is 450-mA
Q5	GND				n/a		
Q6	VSYS		4V		PMIC		System supply-feed power of NAD
Q7	VSYS		4V		PMIC		
Q8	GND				n/a		
Q9	SIM1_SIO	DVDD28_SIM1	3.3V	PU	U4	GPIO113	SIM1 interface signal
Q10	SIM1_SCLK	DVDD28_SIM1	3.3V	PD	V4	GPIO115	SIM1 interface signal
Q11	SIM1_SRST	DVDD28_SIM1	3.3V	PD	V3	GPIO114	SIM1 interface signal
Q12	URTS1	DVDD18	1.8V	PD	AE2	GPIO96	UART interface signal
Q13	RTC_CLK		0 to 1.98V		PMIC		32-KHz clock signal generated from PMIC
Q14	AUXADC_VIN4		0 to 1.98V		PMIC		PMIC ADC input with 12-bit A-to-D resolution
Q15	AUXADC_VIN6		0 to 1.98V		PMIC		PMIC ADC input with 12-bit A-to-D resolution
Q16	AUXADC_VIN8		0 to 1.98V		PMIC		PMIC ADC input with 12-bit A-to-D resolution
Q17	GND				n/a		

3.5 GPIO table

Table below shows available GPIO pins in the default software setting and internally pulled-down in the device. 1.8V GPIO pins support the interrupt to wake NAD system up, and EINT0 to 15 also supports the hardware de-bounce to filter the mechanical bounce noise

NAD Pin#	Symbol Name	GPIO	Power Domain	Voltage	MT2731 Pin-out	Description
D15	GPIO0_1V8	EINT0	DVDD18	1.8V	M25	Support Wakeup and Hardware De-bounce
A16	GPIO1_1V8	EINT1	DVDD18	1.8V	M26	Support Wakeup and Hardware De-bounce
G12	GPIO2_1V8	EINT2	DVDD18	1.8V	V21	Support Wakeup and Hardware De-bounce
E17	GPIO8_1V8	EINT8	DVDD18	1.8V	AF23	Support Wakeup and Hardware De-bounce
G13	GPIO9_1V8	EINT9	DVDD18	1.8V	AE18	Support Wakeup and Hardware De-bounce

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G10	GPIO10_1V8	EINT10	DVDD18	1.8V	AC4	Support Wakeup and Hardware De-bounce
G9	GPIO11_1V8	EINT11	DVDD18	1.8V	AB2	Support Wakeup and Hardware De-bounce
H9	GPIO12_1V8	EINT12	DVDD18	1.8V	Y5	Support Wakeup and Hardware De-bounce
E3	GPIO18_1V8	EINT18	DVDD18	1.8V	M24	Support Wakeup
E4	GPIO19_1V8	EINT19	DVDD18	1.8V	M23	Support Wakeup
B12	GPIO28_1V8	EINT28	DVDD18	1.8V	P25	Support Wakeup
B4	GPIO44_1V8	EINT44	DVDD18	1.8V	G22	Support Wakeup
B3	GPIO45_1V8	EINT45	DVDD18	1.8V	G23	Support Wakeup
A2	GPIO46_1V8	EINT46	DVDD18	1.8V	F22	Support Wakeup
J10	GPIO87_1V8	EINT87	DVDD18	1.8V	AB6	Support Wakeup
J9	GPIO88_1V8	EINT88	DVDD18	1.8V	AB5	Support Wakeup
K10	GPIO89_1V8	EINT89	DVDD18	1.8V	AF4	Support Wakeup
H10	GPIO90_1V8	EINT90	DVDD18	1.8V	AE4	Support Wakeup
A15	GPIO13_3V3	EINT13	DVDD28	3.3V	AA24	Support Wakeup and Hardware De-bounce
B15	GPIO14_3V3	EINT14	DVDD28	3.3V	AB25	Support Wakeup and Hardware De-bounce
A17	GPIO15_3V3	EINT15	DVDD28	3.3V	AB24	Support Wakeup and Hardware De-bounce
B11	GPIO43_3V3	EINT43	DVDD28	3.3V	Y24	
J3	GPIO116_3V3	EINT116	DVDD28	3.3V	M1	
H2	GPIO117_3V3	EINT117	DVDD28	3.3V	M4	
J1	GPIO118_3V3	EINT118	DVDD28	3.3V	N4	
H1	GPIO119_3V3	EINT119	DVDD28	3.3V	N5	
L6	GPIO120_3V3	EINT120	DVDD28	3.3V	R4	
K6	GPIO121_3V3	EINT121	DVDD28	3.3V	R2	
K4	GPIO122_3V3	EINT122	DVDD28	3.3V	P2	
J6	GPIO123_3V3	EINT123	DVDD28	3.3V	P1	
H3	GPIO124_3V3	EINT124	DVDD28	3.3V	L4	
L5	GPIO125_3V3	EINT125	DVDD28	3.3V	P5	
K5	GPIO126_3V3	EINT126	DVDD28	3.3V	P3	
J2	GPIO127_3V3	EINT127	DVDD28	3.3V	N3	
J4	GPIO128_3V3	EINT128	DVDD28	3.3V	K3	
H4	GPIO129_3V3	EINT129	DVDD28	3.3V	L3	
H5	GPIO130_3V3	EINT130	DVDD28	3.3V	M2	
K7	GPIO131_3V3	EINT131	DVDD28	3.3V	R3	
G5	GPIO132_3V3	EINT132	DVDD28	3.3V	L2	
J5	GPIO133_3V3	EINT133	DVDD28	3.3V	K2	
L8	GPI146_3V3	EINT146	DVDD28	3.3V	T3	This pin only offers the input function and is not able to be configured as the output pin

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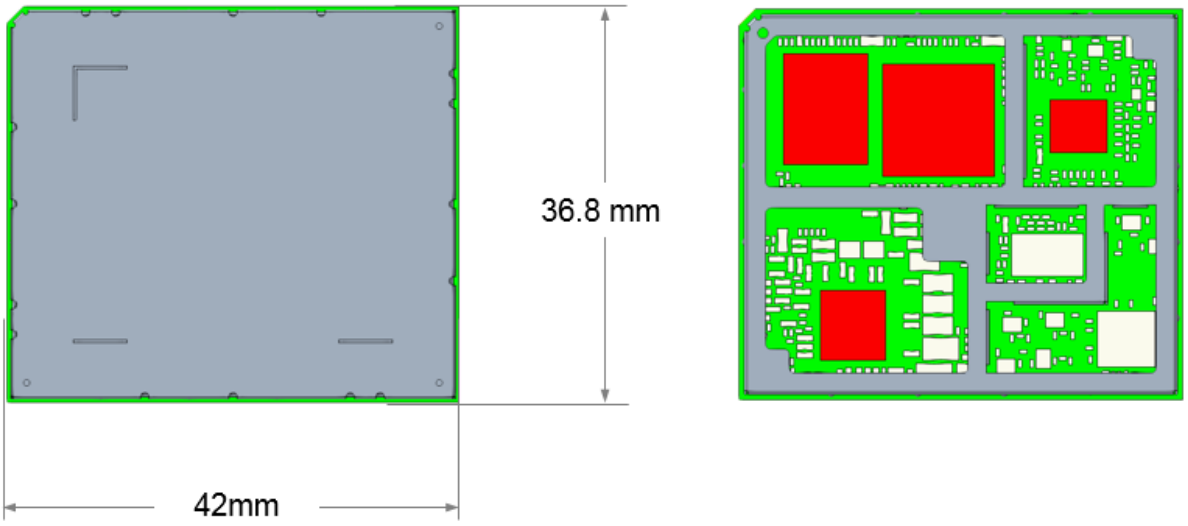
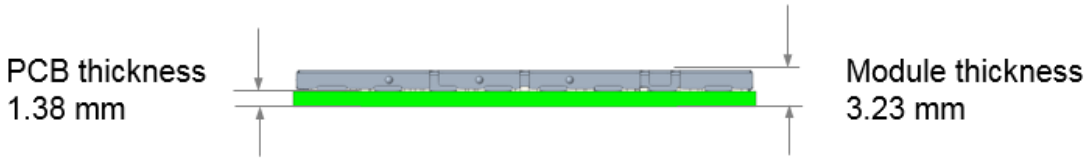
4 Mechanical design

4.1 Shielding case design





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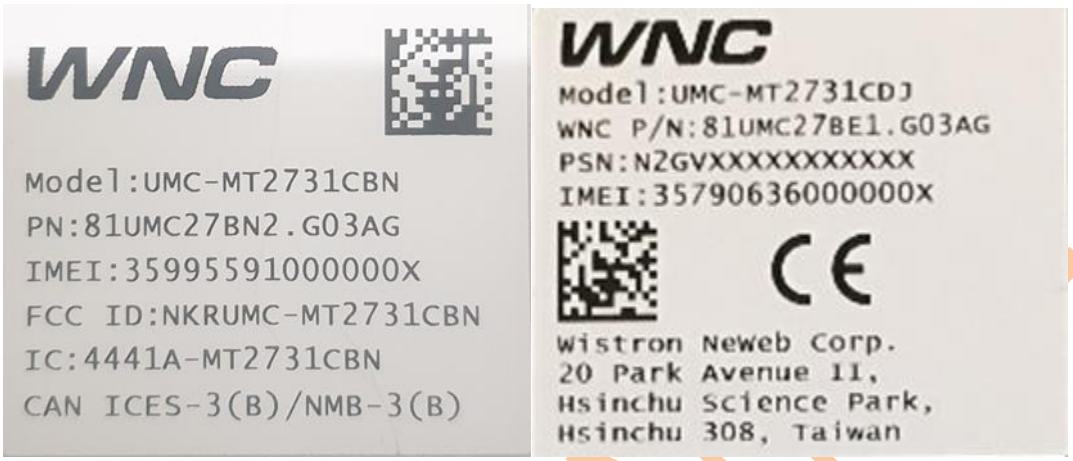
4.2 Label information

This label is applied to UMC-MT2731C NAD shielding case top. It specifies the label outline with the content format as below



4.3 NAD land pattern

1.36-MM is the original NAD bottom side copper pad diameter size. It implemented the solder mask to cover these LGA pads; thus, SMD(Solder Mask Define) round pad diameter is 1.20-MM

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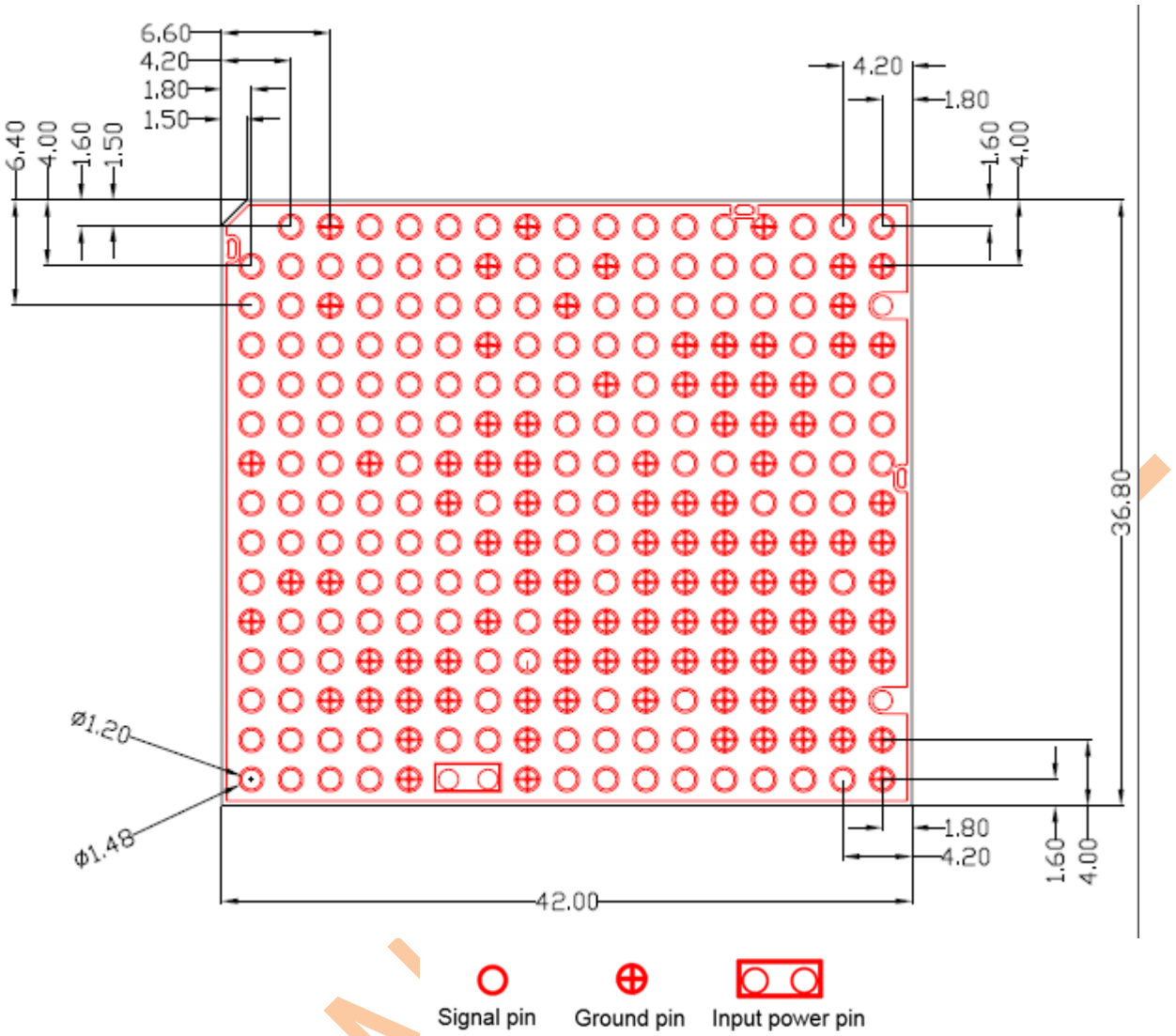

4.4 Stencil opening

Following chart is the recommendation for the stencil opening design
NOTE: The final design open window diagram will be updated after the reliability tests completed

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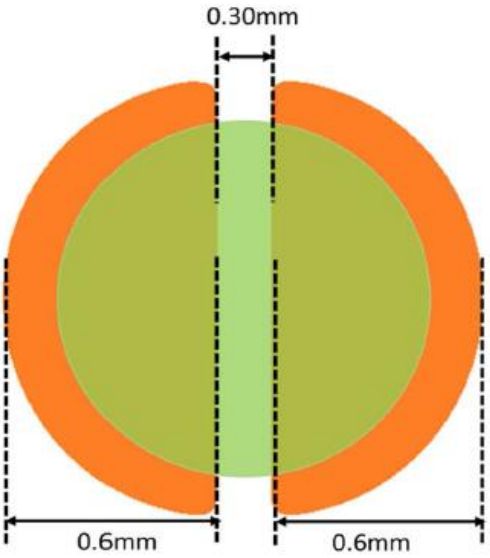
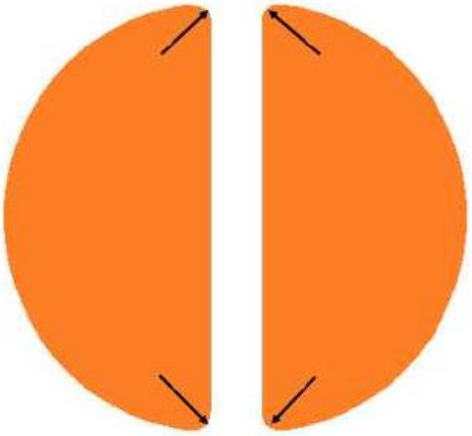


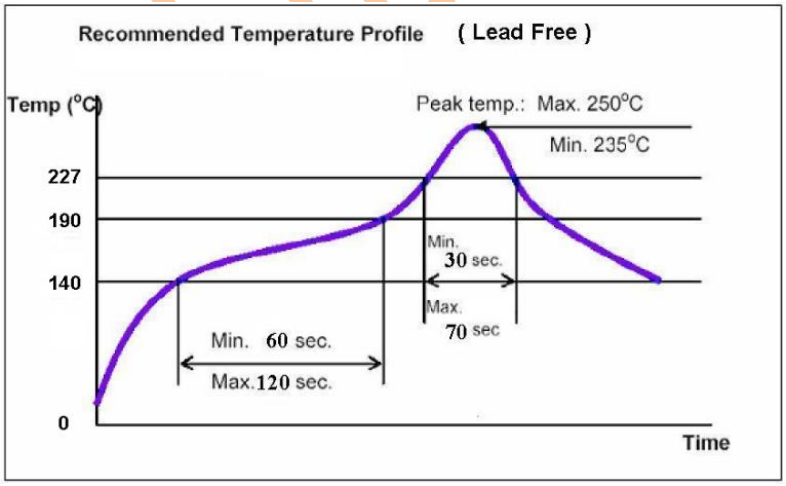


*Orange color: stencil aperture

Thickness of stencil: 0.12mm

Solder Paste Recommendation: SAC305 Alloy

4.5 Reflow profile



Profile Feature	Parameters
Peak Temperature	235 to 250°C
Reflow Zone(Above 227°C or 230°C)	30 to 70 Seconds
Preheat Zone(140 to 190°C)	60 to 120 Seconds

4.6 Moisture sensitivity level

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UMC-MT2731C complies IPC/JEDEC J-STD-020 Standard MSL 3

4.7 ESD

It strongly recommends Developer to place ESD suppression components on the interconnection signal traces between NAD bottom pads and the application board for preventing NAD being suffered ESD events with the voltage strength over the requirement defined in the table as below

Specification/Requirements	Contact Discharge
Human Body Model(HBM)	2000 Voltages
Charge Device Model(CDM)	500 Voltages

4.8 Packaging

The single-feed tape carrier for MT2731C is illustrated in Figure as shown in below. The figure also shows the proper part orientation. The tape width is 56 mm and the module is placed on the tape with a 56 mm pitch. The packing length per reel is 10.6 meters and each reel contains 100 pcs modules.

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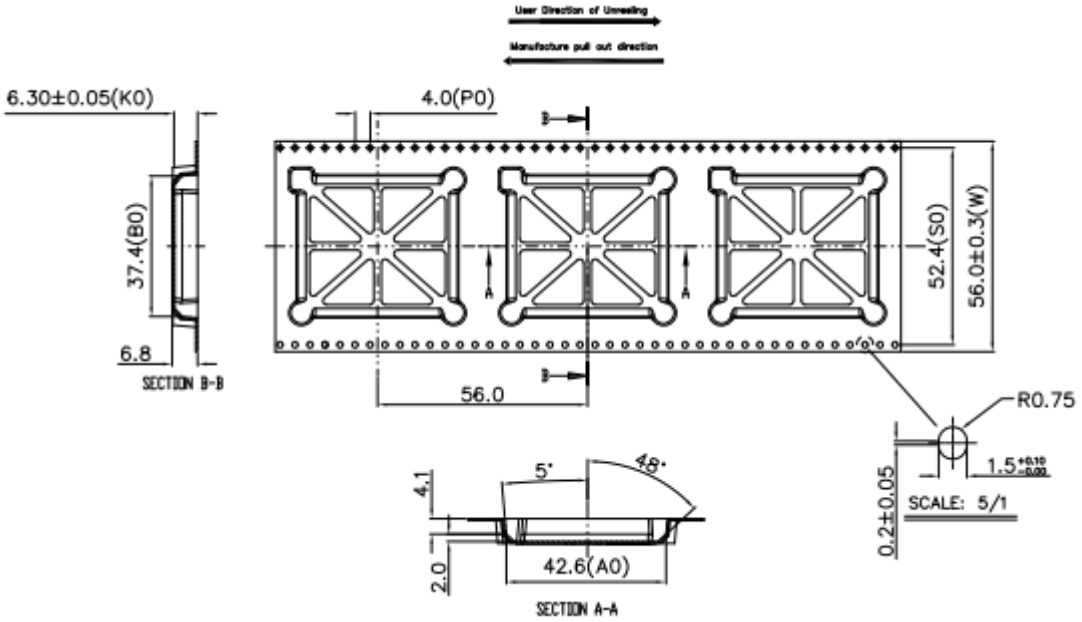
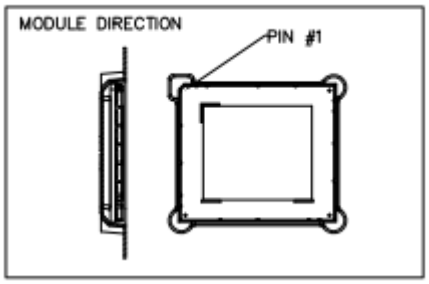
W	56.00±0.30	P2	2.00±0.15
S0	52.40±0.10	A0	42.60±0.15
E1	1.75±0.10	A1	——
F	26.20±0.15	B0	37.40±0.15
D0	1.50 +0.10	B1	——
D1	——	K0	7.0±0.15
P1	56.00±0.10	K1	——
P0	4.00±0.10	T	0.50±0.05

1. CAMBER IN COMPLIANCE WITH EIA 481.
2. MATERIAL: PS BLACK
3. SURFACE RESISTIVITY: 10^{5}~10^{9} OHMS/SQUARE
4. PACKING LENGTH PER ROLL : 8.4 METERS.
5. VENDOR SHIPPING LENGTH PER ROLL : 25.2 METERS.
6. COMPONENT POCKETS PER 13" REEL : 100 PCS
   (TOTAL POCKETS PER 13" REEL: 150PCS
   EMPTY POCKET IN FRONT OF REEL: 20PCS
   EMPTY POCKET IN BACK OF REEL: 20PCS
   BUFFER POCKET:10PCS)





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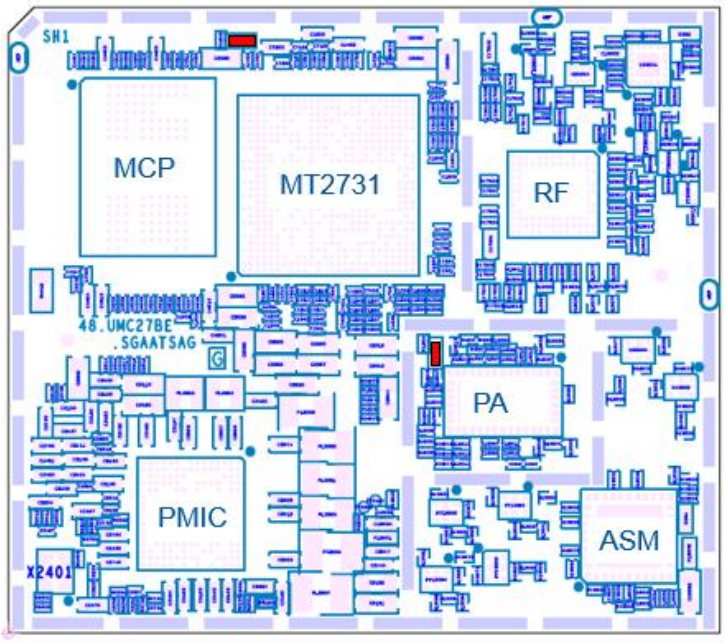
5 Thermal design

5.1 Thermal sensor

(1)There are four temperature sensors embedded in MT2731 device package. Developer could read temperature value inside MT2731 by the software command. When the package temperature reached the threshold point, MT2731 will trigger itself resetting for the over-heating protection

(2)MT2731 could get thermal information from two on board thermistors and monitor components' temperature near these two thermistor locations



Thermistor: to detect PCB temperature

(3)Developer could connect four outgoing general purpose ADC interfaces, named as AUXADC_VIN2, AUXADC_VIN3, AUXADC_VIN4 and AUXADC_VIN5, of NAD for monitoring hotspots' temperature on the application board

5.2 Software thermal mitigation

UMC-MT2731C has software approaches for the thermal mitigation. When the temperature reached the defined threshold point, LINUX kernel will control the system power by holding processors and RF power amplifier current consumption. This will make UMC-MT2731C work safely under the critical and concerned temperature condition

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6 RF specification

6.1 UMC-MT2731C

6.1.1 Maximum output power

Note(*): The minimum data in the table is following 3GPP standard

	Specification (Band/Uplink Frequency)	Minimum	Typical	Maximum	Unit
LTE	Band1(1920 - 1980 MHz)	20.3*	23	24	dBm
	Band2(1850 - 1910 MHz)	20.3*	23	24	dBm
	Band3(1710 - 1785 MHz)	20.3*	23	24	dBm
	Band4(1710 - 1755 MHz)	20.3*	23	24	dBm
	Band5(824 - 849 MHz)	20.3*	23	24	dBm
	Band7(2500 - 2570 MHz)	20.3*	23	24	dBm
	Band8(880 - 915 MHz)	20.3*	23	24	dBm
	Band12(699 - 716 MHz)	20.3*	23	24	dBm
	Band17(704 - 716 MHz)	20.3*	23	24	dBm
	Band14(788 – 798 MHz)	20.3*	23	24	dBm
	Band18(815 - 830 MHz)	20.3*	23	24	dBm
	Band19(830 – 845 MHz)	20.3*	23	24	dBm
	Band20(832 – 862 MHz)	20.3*	23	24	dBm
	Band25(1850 - 1915 MHz)	20.3*	23	24	dBm
	Band26(814 - 849 MHz)	20.3*	23	24	dBm
	Band28(703 - 748 MHz)	20.3*	23	24	dBm
	Band38(2570 - 2620 MHz)	20.3*	23	24	dBm
	Band39(1880 - 1920 MHz)	20.3*	23	24	dBm
	Band40(2300 - 2400 MHz)	20.3*	23	24	dBm
	Band41(2496 - 2690 MHz)	20.3*	23	24	dBm
	Band66(1710 - 1780 MHz)	20.3*	23	24	dBm
WCDMA	Band1(1920 - 1980 MHz)	20.3*	23	24	dBm
	Band5(824 - 849 MHz)	20.3*	23	24	dBm
	Band8(880 - 915 MHz)	20.3*	23	24	dBm
GSM (GMSK)	850(824 - 849 MHz)	31	33	35	dBm
	900(880 - 915 MHz)	31	33	35	dBm
	1800(1710 - 1785 MHz)	28	30	32	dBm
	1900(1850 - 1910 MHz)	28	29.5	30	dBm
GSM (8-PSK)	850(824 - 849 MHz)	25	27	29	dBm
	900(880 - 915 MHz)	25	27	29	dBm
	1800(1710 - 1785 MHz)	24	26	28	dBm
	1900(1850 - 1910 MHz)	24	26	28	dBm

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6.1.2 Sensitivity limit

	Specification (Band/Downlink Frequency)	Typical	Unit
LTE	Band1(2110 - 2170 MHz)	-96.3	dBm
10-MHz BW	Band2(1930 - 1990 MHz)	-94.3	dBm
QPSK	Band3(1805 - 1880 MHz)	-93.3	dBm
	Band4(2110 - 2155 MHz)	-96.3	dBm
	Band5(869 - 894 MHz)	-94.3	dBm
	Band7(2620 - 2690 MHz)	-94.3	dBm
	Band8(925 - 960 MHz)	-93.3	dBm
	Band12(729 - 746 MHz)	-93.3	dBm
	Band17(734 - 746 MHz)	-93.3	dBm
	Band14(758 - 768 MHz)	-93.3	dBm
	Band18(860 - 875 MHz)	-96.3	dBm
	Band19(875 – 890 MHz)	-96.3	dBm
	Band20(791 – 821 MHz)	-93.3	dBm
	Band25(1930 - 1995 MHz)	-92.8	dBm
	Band26(859 - 894 MHz)	-93.8	dBm
	Band28(758 - 803 MHz)	-94.8	dBm
	Band38(2570 - 2620 MHz)	-96.3	dBm
	Band39(1880 - 1920 MHz)	-96.3	dBm
	Band40(2300 - 2400 MHz)	-96.3	dBm
	Band41(2496 - 2690 MHz)	-94.3	dBm
	Band66(2110 - 2200 MHz)	-95.8	dBm
WCDMA	Band1(2110 - 2170 MHz)	-106	dBm
	Band5(869 - 894 MHz)	-104	dBm
	Band8(925 - 960 MHz)	-103	dBm
GSM	850(869 - 894 MHz)	-102	dBm
	900(925 - 960 MHz)	-102	dBm
	1800(1805 - 1880 MHz)	-102	dBm
	1900(1930 - 1990 MHz)	-102	dBm

7 Evaluation Kit

WNC provides EVK built with UMC-MT2731 EU PoC. User could use this EVK to verify basic functions or develop applications on MT2731 platform. Following is EVK block diagram

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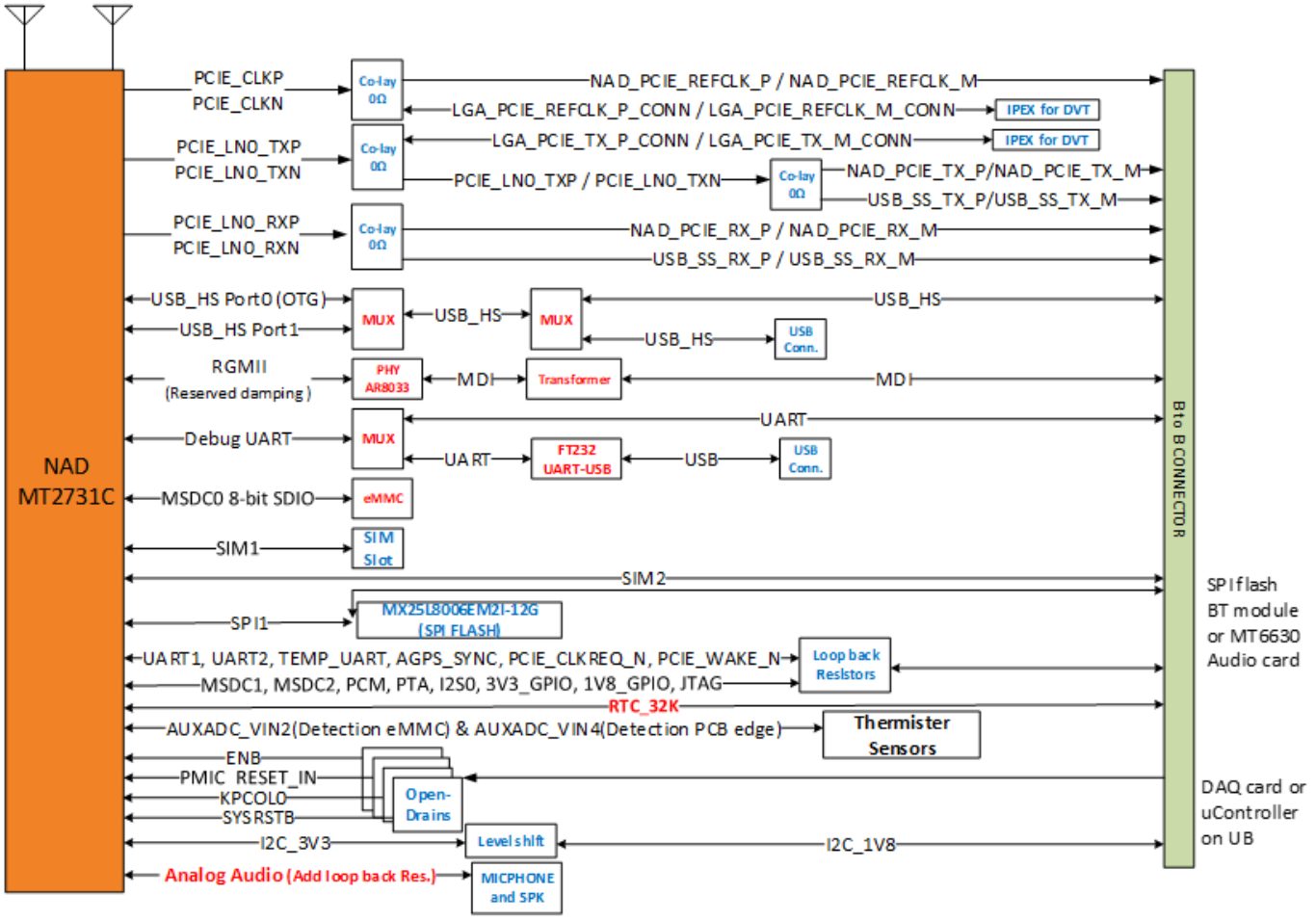

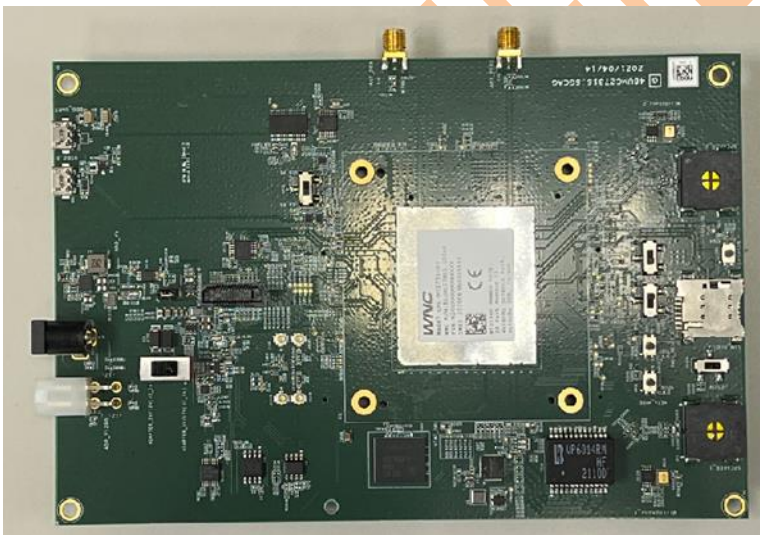

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8 Design application notes

This section describes how to connect UMC-MT2731C NAD to the circuitry on the application board, and notes that system developers should pay attention to in their design stage

8.1 Power trace

On VSYS power traces from the application board to UMC-MT2731C, to place the de-coupling capacitors, 10-uF or 22-uF, near by the input of NAD as close as possible. Recommended width of VSYS trace is at least wider than 80-mil

8.2 Power ON/OFF/Suspend and Reset

8.2.1 Power ON

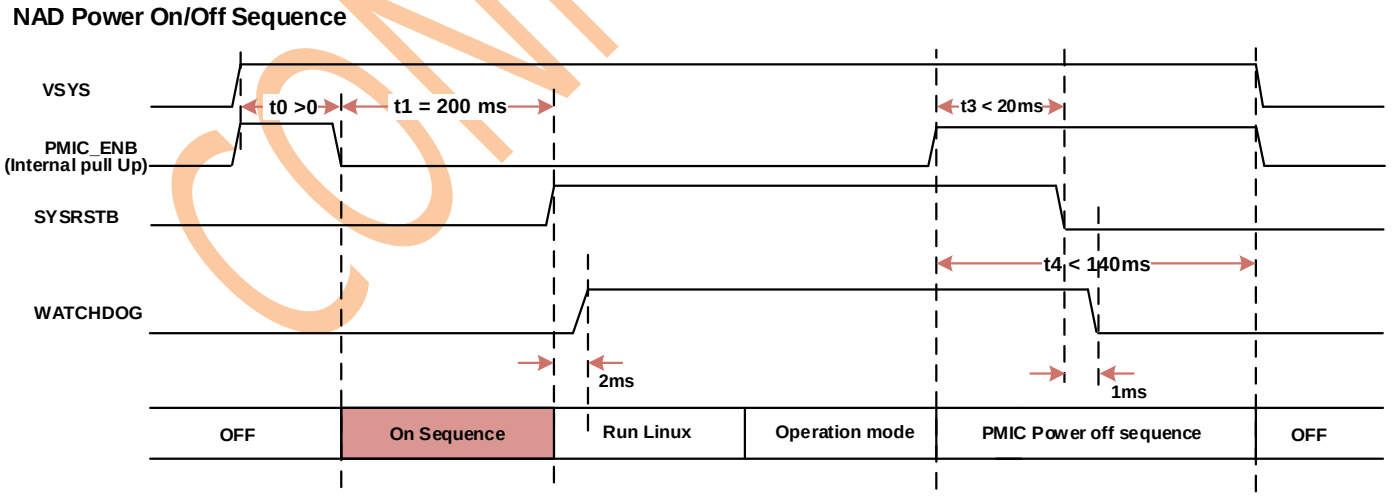
After supplying VSYS, to pull PMIC_ENB LOW to power NAD on

8.2.2 Power OFF

Pull PMIC_ENB HIGH to power NAD off. Powering off sequence requires at least 140-ms

8.2.3 Reset

(1) To pull PMIC_RESET_B LOW at least 200-ms for rebooting NAD the with completed power sequence
(2) Alternative approach is pulling SYSRSTB LOW to reset NAD without resetting the power ON/OFF sequence. This is only for the debugging



NAD Pad#	NAD Pad Name	Pin Function Description
Q6/Q7	VSYS	System supply-feed power of NAD

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P6	PMIC_ENB	Pull this pin low to power NAD off
P7	PMIC_RESET_B	Pull this pin low to trigger the reset of PMIC
H7	SYSRSTB	Pull this pin low to reset NAD without resetting the power ON/OFF sequence of PMIC

8.3 USB3.1 Gen.1

8.3.1 Layout

The total routing length of SS-USB signal traces should be less than 4500-mil and designed with 90-OHM line impedance on the application board, and the difference length of differential pair signals shall be kept within 5-mil

8.3.2 Using USB2.0

User could use USB 2.0 only. In this case, all SS-USB pins(A4, A5, A6 and A7) should be configured as No Connection(NC)

NAD Pad#	NAD Pad Name	Pin Function Description
A4	SSUSB_TXP	SS-USB interface signal
A5	SSUSB_TXN	SS-USB interface signal
A6	SSUSB_RXN	SS-USB interface signal
A7	SSUSB_RXP	SS-USB interface signal
A9	USB_DM_P1	USB 2.0 differential pair signal
A10	USB_DP_P1	USB 2.0 differential pair signal

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8.4 USB2.0 OTG

The total routing length of HS-USB signal traces should be less than 7500-mil and designed with 90-OHM line impedance on the application board, and the difference length of differential pair signals shall be kept within 40-mil

NAD Pad#	NAD Pad Name	Pin Function Description
B8	USB_DM_P0	USB 2.0 OTG differential pair signal
B9	USB_DP_P0	USB 2.0 OTG differential pair signal
A12	IDDIG	ID pin of USB 2.0 OTG interface

8.5 I2C

I2C is internally pulled-up by 3.3V with 4.7K-OHM resistor. Push-pull is recommended for high speed mode. Open-drain is recommended for standard, fast and fast plus mode

NAD Pad#	Pin Function Description	GPIO Name	I/O Type
E11	SCL0	GPIO42	Push-pull / Open-drain
D10	SDA0	GPIO41	Push-pull / Open-drain

8.6 I2S

Signal voltage level is required 1.8-Volatge

Interface	Function	Mode	Sampling Rate/Bit Resolution
I2S	IN & OUT	MASTER or SLAVE configured by the software	MASTER: up to 192-KHz, 24-bit SLAVE: up to 96-KHz, 24bit

8.7 MSDC

8.7.1 Layout

The total routing length of eMMC signal traces should be less than 1000-mil and the difference length of MSDC signals shall be kept within 10-mil on the application board. Developer could use VEMC_PMU and VIO18_PMU as the power supply of eMMC device

8.7.2 MSDC interface

MSDC0 has the independent power domain and is dedicated for eMMC device on the application board. MSDC1/2 is reserved for SDIO interface applications excluded SD-Card

Interface	Function	Standard

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MSDC0	eMMC	eMMC 5.0
MSDC1	Reserved	SDIO 3.0
MSDC2	Reserved for MT6630	SDIO 3.0

8.8 SPI

8.8.1 Layout

The total routing length of SPI signal traces should be less than 5000-mil and well-shielded by the nearby grounding in the same layer or neighborhood layers on the application board; furthermore, keeping SPI routing far away from noises source(such as VBUS, the bucking switching nodes and clock signals) is necessary

8.8.2 Application

SPI supports MASTER or SLAVE mode which is configured by the software

8.9 SIM

8.9.1 Layout

VSIM1_PMU/VSIM2_PMU is the power supply-feed for SIM1/SIM2 on the application board, and able to be configured as 1.8- or 3.3-Volatge level; the default setting is 1.8-Volatge. Both SIM1_SCLK and SIM2_SCLK is recommended to be shielded by the grounding

8.10 RF antenna port

Preventing the coplanar grounding being quite close 50-OHM RF transmission lines shall be considered by Developer when you do RF trace design connected to RF antenna pads of UMC-MT2731C on the application board. It is better to have the keep-out gap which is 3 to 5 times of top layer RF trace width between these RF lines and the grounding
Meanwhile, it is also important to reserve the pi-matching circuit design close to NAD antenna out pads as possible
Avoid making RF layout trace of the primary antenna port cross the diversity antenna trace, and then this would cause the poor antenna isolation to impact RF performance of the application board

8.10.1 Antenna detection

Following concept schematic diagram is a design example to build the antenna detection circuit by using NAD AUXADC pin of AUXADC_VIN2 for monitoring NAD ANT_PTRX connection status with the external passive antenna shunted with a grounded inductor. In this diagram

DC block: to play the role of isolating the detection signal with Antenna matching possibly consisted of the grounded matching elements
RF block: to prevent RF signals being fed into the antenna detection circuitry

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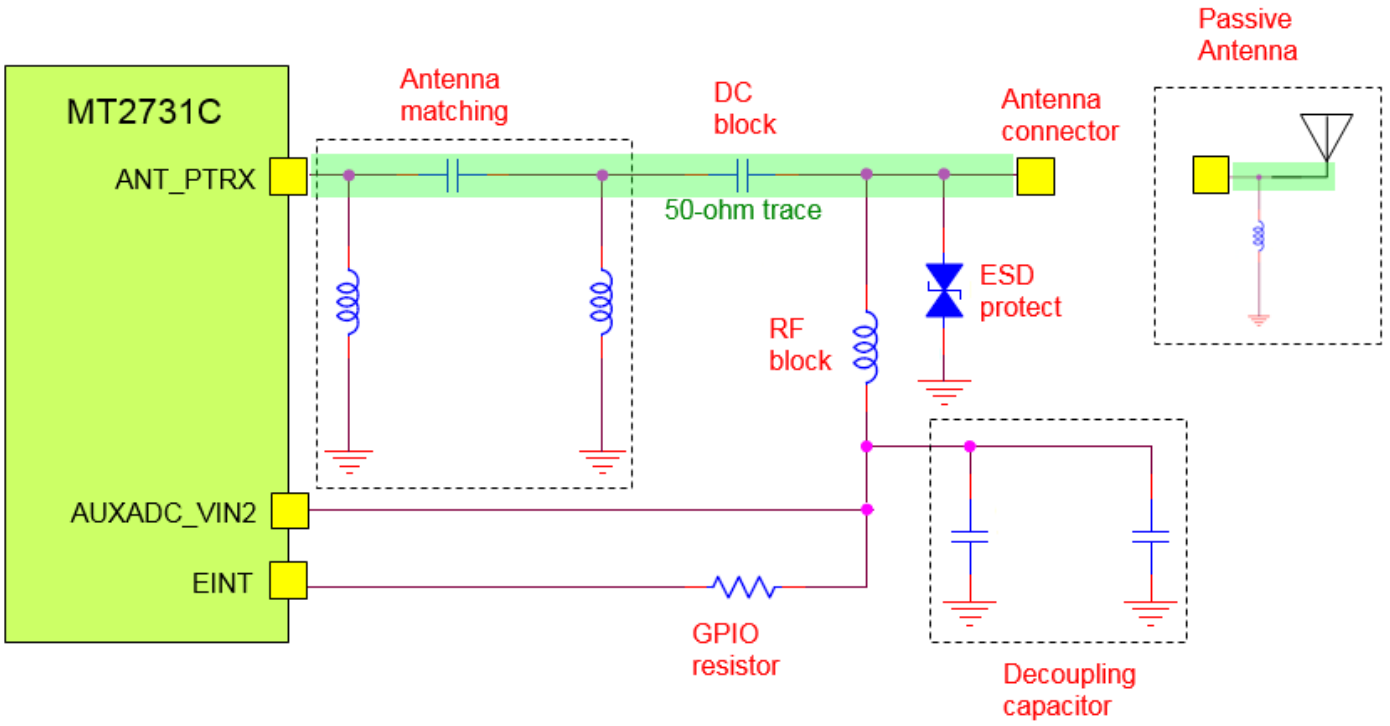
GPIO resistor: to limit the current draw when the external antenna is connected

Connected Case: NAD EINT pin would continuously send out the detection signal of the static high state; if the external antenna is well-attached with the application board, the software reading value of AUXADC_VIN2 is kept as static zero-Voltage

Disconnected Case: If any broken events happened on RF path between the external antenna and NAD ANT_PTRX, AUXADC_VIN2 would read a high state voltage level generated by NAD EINT port



8.10.2 Antenna Isolation

Due to B14 2nd harmonic fall into GPS in-band, it causes GPS performance degradation. To reduce performance degradation, enough isolation between WWAN ANT and GPS ANT is necessary. About MT2731C NA SKU, the suggest isolation should be more than 28dB.

8.11 KPCOL0

Pull KPCOL0 LOW to force NAD being USB Download Mode for user updating NAD software
*Note: Can be customized

8.12 IDDIG

This pin is used as USB 2.0 OTG ID pin

8.13 WATCHDOG

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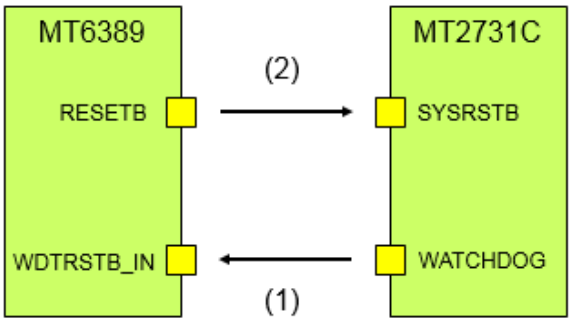
WATCHDOG is a 1.8-Voltage level signal generated from MT2731 and then received by PMIC. In normal cases, MT2731 keeps WATCHDOG as the high state; in case of the low state event happened, a NAD resetting reaction steps would be performed between MT2731 and PMIC and defined as below

(1) If MT2731 is malfunctioning, WATCHDOG would become the low state, as well as WDTRSTB_IN of PMIC. Then, PMIC starts itself reset
(2) After the reset of PMIC is finished, PMIC sent RESETB of the low state to SYSRSTB of MT2731. Then, MT2731 also starts itself reset procedure



*Note:This function work automatic internally, customer don't need to do anything to control it.

8.14 SRCLKENA0

NAD status indicator generated from MT2731; the state of high(1.8-Voltage) for Normal Mode, as well as low(0-Voltage) for Sleep/Low Power Mode
*Note: Can be customized

8.15 RTC_CLK

32-KHz clock signal generated from PMIC is able to be the synchronized signal source for other functional blocks on the application board

8.16 Thermal

It is recommended to reserve contact ground area as broad as possible on TCU. By widening contact ground area, the heat generated by module will be dissipated more efficiently. Green rectangular area is reference area for ground contact

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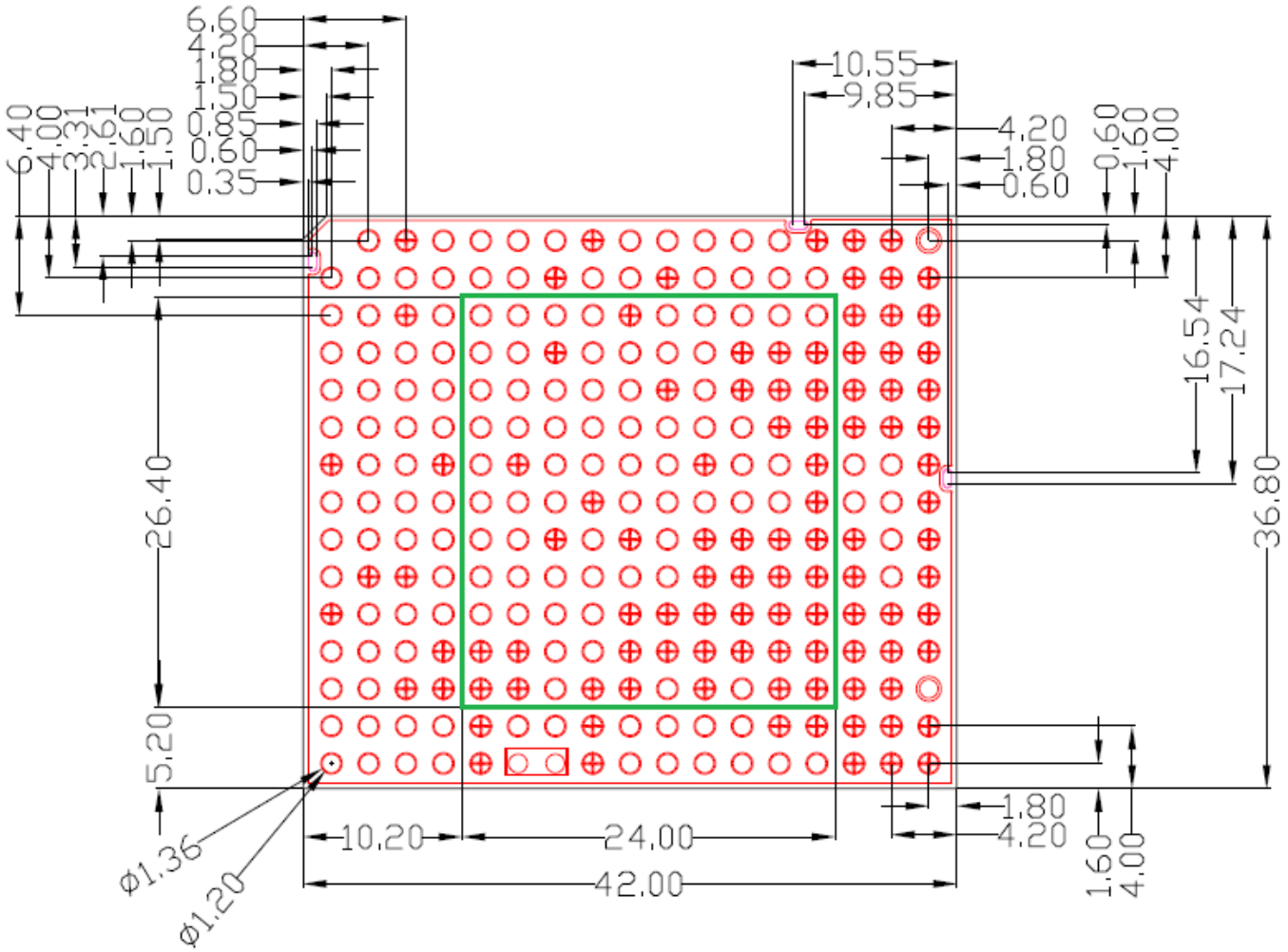

9 Abbreviation

Acronym	Definition
ADC	Analog Digital Converter
CAT	Category
CHN	China
codec	Compress Decompress
CS	Circuit Switch
DC	Direct Current
DL	Down Link
DMIPS	Dhrystone Million Instructions executed Per Second
e-call	Emergency Call

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EDGE	Enhanced Data Rate for GSM Evolution
EINT	External Interrupt Input
eMMC	Embedded Multi Media Card
ESD	Electro Static Discharge
EU	Europe
GMII	Gigabit Media Independent Interface
GND	Ground
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
I/O	Input / Output
I2C	Inter-integrated circuit
I2S	Inter-IC sound
IMS	IP Multimedia Subsystem
IP	Internet Protocol
JTAG	Joint Test Action Group
LPDDR	Low Power Double Data Rate
LTE	Long Term Evolution
Mbps	Megabit per second
MCP	Multi-Chip Package
MII	Media Independent Interface
mil	1/1000 inch
MSDC	Mass Storage Device Class
MT6630	MTK chip has Bluetooth, WLAN, GNSS function
NA	North America
NAD	Networking Access Device
OSS	Open Source Software
OTG	On The Go
PCB	Printed Circuit Board

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PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PD	Pull Down
PMIC	Power management integrated circuit
PU	Pull Up
RF	Radio Frequency
RFFE	RF Front End
RGMII	Reduced Gigabit Media Independent Interface
ROW	Rest Of World
RTC	Real Time Clock
RX	Receive
SDIO	Secure Digital Input/Output
SIM	Subscriber Identification Module
SKU	Stock Keeping Unit
SPI	Serial Peripheral interface
TX	Transmit
UART	Universal Asynchronous Receiver and Transmitter
UIM	User identity module
UL	Up Link
UMTS	Universal mobile telecommunications system
USB	Universal Serial Bus
WCDMA	Wide-band Code Division Multiple Access
DSSS	Dual SIM single standby

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10. Warning statement

Federal Communication Commission Interference Statement:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

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This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 27, 22, 24, 90

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not applicable.

2.5 Trace antenna designs

Refer to “Operational Description Antenna trace”
Please contact the module supplier

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

Antenna Type	Dipole
Antenna connector	SMA

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: “Contains FCC ID: NKRUMC-MT2731CBN”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

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IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

Industry Canada statement:

This device complies with ISED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with greater than 25cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé à plus de 25 cm entre le radiateur et votre corps.

This device is intended only for OEM integrators under the following conditions

1) The antenna must be installed and operated with greater than 25 cm between the antenna and users
2) The transmitter module may not be co-located with any other transmitter or antenna.
3) Module approval valid only when the module is installed in the tested host or compatible series of host which have similar RF exposure characteristic with equal or larger antenna separation distance.

As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

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Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes:
1) L'antenne doit être installé et exploité avec plus de 25 cm entre l'antenne et les utilisateurs
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.
3) Approbation du Module valable que lorsque le module est installé dans l'hôte testé ou de la série de l'hôte compatible qui ont même caractéristique de l'exposition aux RF avec la distance égale ou supérieure séparation antenne.

Tant que les 3 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE
In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE
Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed and operated with greater than 25cm between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 4441A-MT2731CBN”.

Plaque signalétique du produit final
Ce module émetteur est autorisé uniquement pour une utilisation dans un appareil où l’antenne peut être installée et utilisée à plus de 25 cm entre l’antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 4441A-MT2731CBN ".

Manual Information To the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final
L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel

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DETACHABLE ANTENNA USAGE

This radio transmitter [IC: 4441A-MT2731CBN] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio [IC: 4441A-MT2731CBN] a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.

Manufacturer	Model	Antenna Type	MaxGain (dBi)	Impedance (Ω)
WNC	SMA	Dipole	2.15	50

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