WLAN/BT **System Integration Manual**	**Model Name:** **UMW-WBT,** **CWM-01**	**Issue Date:** **2011/05/05**
	Project Code:	**Rev Date:** **2011/12/27**
	Base Model:	**Rev:2**

Revision History

Rev.	History	Date	Author
1	- Initial version	2011/05/05	Shukai Hsu HT Liao Hauson Chen Chris WJ Huang
2	1. Frequency range is changed to 2400-2483.5Mhz 2. FCC channels revised to be ch1 – ch11 3. Power value is revised: WIFI: 15+/-1.5dBm BT: class 1 -	2011/12/27	Shukai
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1. Introduction

This document specifies the mechanical and electrical specifications for the 802.11b/g WiFi and Bluetooth 3.0 module. Continuing a tradition of design ingenuity and development, Wistron NeWeb Corporation (WNC) presents a standard modular solution for WiFi and Bluetooth technology to comply with OEM industrial requirements in vehicles. The module provides 802.11 b/g WLAN and Bluetooth 3.0 functions by using a single chipset solution. Utilizing the module, radio manufacturers are enabled to create feature rich ready design without the additional burden to redesign the WiFi and Bluetooth functions.

For the remainder of the document, the host design that shall integrate the module shall be referred to as the application. The application shall be the controlling host entity with respect to the module.

This document also provides hardware design instruction and production setup information.

1.1 Product Overview

This document specifies the 802.11b/g + Bluetooth Module. The specification covers overall dimensions, general module construction, connector interface footprints, and mechanical and electrical characteristics of the WNC's 802.11b/g + Bluetooth module. This module was built by using Marvell's 88W8688 chipset.

Host Interface:
WLAN: SDIO
Bluetooth: SDIO/high speed UART

802.11b/g :
Frequency band:

- B Mode: 2.400~2.4835 GHz
- G Mode: 2.400~2.4835 GHz

Channel Spacing:
B / G Mode: 5MHz

Modulation:

- B Mode: DSSS with DBPSK, DQPSK, and CCK
- G Mode: OFDM with BPSK, QPSK, QAM, and 16/64QAM

Channels Support:

- B Mode: CH1 – CH13 (ETSI)/CH1-CH11 (FCC)/CH1-CH14 (Japan)
- G Mode: CH1 – CH13 (ETSI)/CH1-CH11 (FCC)/CH1-CH14 (Japan)

RF output Power:

- B Mode: 16.30 dBm @ 1,2, 5.5, and 11Mbps
- G Mode: 23.55 dBm @ 6, 9, 12, 18, 24, 36,48 and 54Mbps

Sensitivity:

- B Mode: –88dBm at 1Mbps
  –87dBm at 2Mbps
  –84dBm at 5.5Mbps
  –80dBm at 11Mbps
- G Mode: –82dBm at 6Mbps
  –81dBm at 9Mbps
  –79dBm at 12Mbps
  –77dBm at 18Mbps
  –74dBm at 24Mbps
  –70dBm at 36Mbps
  –66dBm at 48Mbps
  –65dBm at 54Mbps

Media Access Protocol: CSMA/CA

802.11b data rates of 1, 2, 5.5 and 11 Mbps
802.11g data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission
802.11e Quality of service (QoS)
802.11h transmit power control
802.11j channels (Japan)
802.11s mesh networking

Encryption:

- AEC-CCMP
- WPA encryption
- WEP 64- and 128-bit encryption with hardware TKIP processing
- IPSEC security acceleration in hardware

Bluetooth
Fully compliant with Bluetooth 2.1+EDR, 3.0
Carrier frequency: 2400MHz to 2483.5MHz (79 channels)
RF Output Power: 6.35dBm Class 1

Rx Sensitivity
-82.4 dBm (typ.) for GFSK @ BER = 0.1%,1Mpbs
-89.8 dBm (typ.) for π/4-DQPSK @ BER = 0.1%,2Mpbs
-89.8 dBm (typ.) for 8-DPSK @ BER = 0.1%,3Mpbs

1.3 Standard Bluetooth Profiles

The standard Bluetooth profile is as Table 1-2. Additional profiles other than lists are supported by 3’rd party.

Operating System	Bluetooth Profile
Linux-BlueZ	GAP
	SDP
	GOEP
	A2DP
	HID
	HSP
	PAN
	OPP
	SPP
Windows Mobile	SDP
	A2DP
	HID
	HSP

Table 1-1 Standard Bluetooth Profiles

1.4 Temperature Parameter

Operating temperature range:
- Low ambient temperature: -40ºC
- High case temperature: +85ºC

Storage temperature range:
- Low temperature: -40ºC
- High temperature: +85ºC

1.5 Module Pin Out

The module is designed as 54 pin solder joint module for SMT process. The pin-out is illustrated in the figure 1-2.

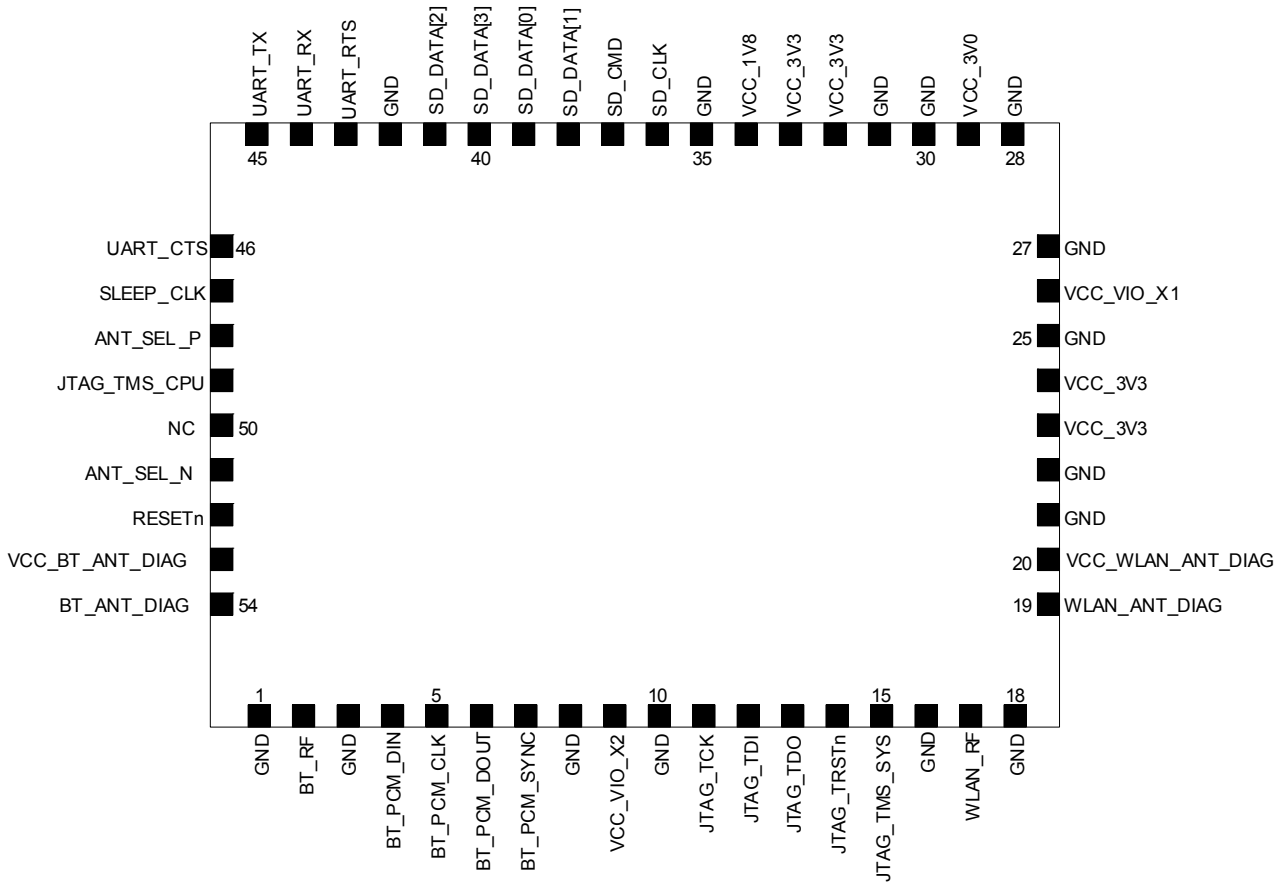


Figure 1-2 Pin out of 802.11b/g + Bluetooth module

The pin definition is shown in the following table 1-2.

Pin #	Signal Name	I/O	Signal Description	Signal Characteristics
SDIO Interface				
36	SD_CLK	I/O	SDIO clock	
37	SD_CMD	I/O	SDIO command line	
39	SD_DAT_0	I/O	SDIO data line bit 0	
38	SD_DAT_1	I/O	SDIO data line bit 1	
41	SD_DAT_2	I/O	SDIO data line bit 2	
40	SD_DAT_3	I/O	SDIO data line bit 3	
UART Interface				
45	TXD	O	UART serial data output	
44	RXD	I	UART serial data input	
46	CTS	I	UART Clear to send signal	
43	RTS	O	UART Ready to send signal	
WLAN and Bluetooth RF Interface				

17	WLAN_RF	I/O	WLAN antenna in/out	
2	BT_RF	I/O	Bluetooth antenna in/out	
Audio Interface – PCM/I2S				
5	BT_PCM_CLK/I2S_BCLK	I/O	PCM clock / I2S audio bit clock	
7	BT_PCM_SYNC/I2S_LRCLK	I/O	PCM sync pulse / I2S left/right clock	
4	BT_PCM_DIN/I2S_DIN	I	PCM data input / I2S data input (for recording)	
6	BT_PCM_DOUT/I2S_DOUT	O	PCM data output / I2S data output (for playback)	
Control & Power Interface				
52	RESET#	I	Reset signal	Active low
47	SLEEP_CLK	I	Sleep clock	
Coexistence				
48	ANT_SEL_P	O	Differential Antenna Select Positive output	
49	JTAG_TMS_CPU	I	JTAG Test Mode Select (Selects the internal CPU JTAG controller)	
50	NC			
51	ANT_SEL_P	O	Differential Antenna Select Negative output	
Antenna Diagnosis				
53	VCC_BT_ANT_DIAG	I	External power for BT antenna diagnosis	
54	BT_ANT_DIAG	O	BT antenna diagnosis output	
20	VCC_WLAN_ANT_DIAG	I	External power for WLAN antenna diagnosis	
19	WLAN_ANT_DIAG	O	WLAN antenna diagnosis output	
Joint Test Action Group (JTAG) and Test Interface				
11	JTAG_TCK	I	JTAG Tset Clock	
12	JTAG_TDI	I	JTAG Tset Data Input	
13	JTAG_TDO	O	JTAG Test Data Output	
14	JTAG_TRSTn	I	JTAG Test Reset	Active low
15	JTAG_TMS_SYS	I	JTAG Test Mode Select (Selects the System JTAG controller)	
Power & Ground				
23, 24, 32, 33,	VCC_3V3	PI	3.3V power input	3.3V +/- 1.5V is required.
29	VCC_3V0	PO	3.0V monitoring output	

34	VCC_1V8	PO	1.8V monitoring output	
26	VCC_VIO_X1	PI	1.8/3.3V Host Interface Supply	For SDIO, UART interface
9	VCC_VIO_X2	PI	3.3V Digital Interface supply	For PCM interface
1, 3, 8, 10, 16, 18, 21, 22, 25, 27, 28, 30, 31, 35, 42	GND	P	Ground	

Table 1-2 Pin Out Definition

1.6 Power management

Module supply (VCC_3V3)
802.11b/g + Bluetooth modules must be supplied through VCC_3V3 pin by a DC power supply. Voltages must be stable, due to the surging consumption profile of the WiFi/BT system.

Name	Description	Remarks
VCC_3V3	Module Supply	Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided has to be always above the minimum limit of the operating range. Consider that there are large current spike in WIFI or BT connected mode.
VCC_IO_X1, VCC_IO_X2	I/O Supply	Clean and stable supply is required: low ripple and low voltage drop must be guaranteed. Voltage provided has to be always above the minimum limit of the operating range.
GND	Ground	GND pins are internally connected but good (low impedance) external ground can improve RF performances. All GND pins must be externally connected to ground.

Operating condition

Symbol	Parameter	Condition	Min	Typ	Max	Units
VCC_3V3	Module power supply		2.97	3.3	3.63	V
VIO_X1	Host interface digital I/O power supply		1.62	1.8	1.98	V
			2.97	3.3	3.63	V
VIO_X2	Digital I/O power supply		2.97	3.3	3.63	V
VCC_3V0	1.8V internal voltage supply		2.9	3.0	3.1	V
VCC_1V8	1.8V internal voltage supply		1.7	1.8	1.9	V
TA	Ambient operating temperature		-40		85	℃
TJ	Maximum junction temperature				125	℃

1.7 RF connection

The RF pin has 50 Ω nominal impedance and must be connected to the antenna through a 50 Ω transmission line to allow transmission and reception of radio frequency (RF) signals in the WIFI and BT operating bands.

Name	Description	Remarks
WLAN_RF	WLAN antenna in/out	50 nominal impedance.
BT_RF	Bluetooth antenna in/out	50 nominal impedance.

RF port ESD rating is *+/-8kV* (contact discharge). A higher protection level could be required if the line is externally accessible on the application board. Note that antenna detection functionality will be not provided implementing for ESD protection on the ANT port.

Choose an antenna with optimal radiating characteristics for the best electrical performance and overall module functionality. An internal antenna, integrated on the application board, or an external antenna, connected to the application board through a proper 50 Ω connector, can be used.

2. Interfaces

This chapter describes the interfaces on the WLAN/BT modules: SDIO, UART, PCM, JTAG, Antenna diagnosis.

2.1 SDIO Interface

The module supports a SDIO device interface that conforms to the industry standard SDIO full speed card specification and allows a host controller using the SDIO bus protocol to access the WLAN and/or Bluetooth device. This device also supports high speed mode as defined in SDIO 1.2 specification.

The SDIO interface supports dual function operations, for WLAN and Bluetooth. Dual functionality allows the use of independent client drivers for WALN and/or Bluetooth on the host platform. Since these functions share the same physical interface, an arbitration scheme is required in the SDIO bus driver on the host platform.

The SDIO interface supports SPI, 1-bit SDIO, 4-bit SDIO transfer modes at the full clock range of 0 to 50MHz.

2.1.1 SDIO Interface Signal Description

Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 4-bit mode: Command/Response SDIO 1-bit mode: Command line SDIO SPI mode: Data in
SD_DAT_0	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data out
SD_DAT_1	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT_2	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] SDIO 1-bit mode: Read Wait (optional) SDIO SPI mode: Reserved

SD_DAT_3	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (Negative true)

2.1.2 SDIO Connection/Function

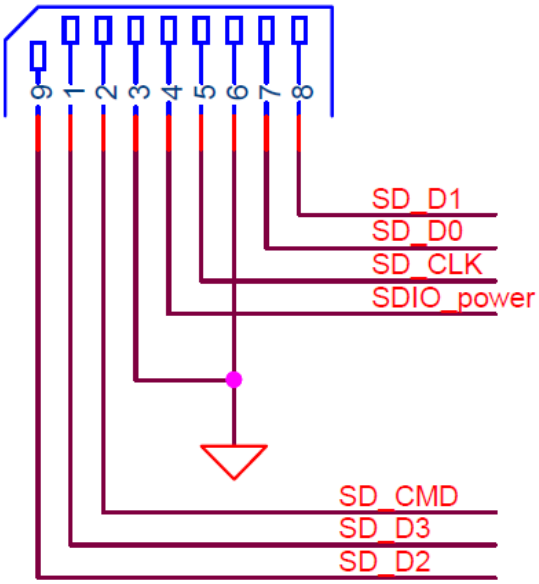


Figure 1.1 SDIO Physical Connection – 4 bit mode

Note: In 4-bit SDIO mode, data is transferred on all 4 data pins (DAT [3:0]), and the interrupt pin is not available for exclusive use as it is utilized as a data transfer line. Thus, if the interrupt function is required, a special timing is required to provide interrupts. The 4-bit SDIO mode provides the highest data transfer possible, up to 100 Mbps.

2.2 UART Interface

The module supports a high speed UART interface, compliant to the industry standard 16550 specification. High speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.

2.2.1 Signal Behavior

TXD

Serial data output to the peripheral device.

RXD

Serial data input from to peripheral device.

CTS

Clear-to-Send input from the peripheral device.

RTS

Request-to-Send output to the peripheral device.

2.3 Digital Audio Interface

Digital audio interfaces include PCM for voice application and I2S for digital stereo applications. PCM and I2S interface share the same pins.

Voice interface supports.

Hardware support for continual transmission and reception of PCM data without processor overhead.

Standard PCM clock rates from 64KHz to 2.048MHz with multi-slot handshake and synchronization.

PCM encoding/decoding support of A-law, μ-law, and linear voice.

Stereo audio interface supports.

Standard record and playback for I2S, left-justified, and right-justified serial interfaces.

Playback in IEC60958 Compatible Audio Codec Interface.

Master and slave mode for I2S, MSB, and LSB audio interfaces.

Slave mode with option to use asynchronous internal CLK.

Slave mode with optional slower synchronous CLK input from host to save power.

2.3.1 BT_PCM_SYNC/I2S_LRCLK

PCM mode: BT_PCM_SYNC, input/output (output if PCM initiator, input if PCM target)

Stereo audio mode: I2S_LRCLK

Master mode: output

Slave mode: input

2.3.2 BT_PCM_CLK/I2S_BCLK

PCM mode: BT_PCM_CLK, input/output (output if PCM initiator, input if PCM target)

Stereo audio mode: I2S_BCLK

Master mode: output

Slave mode: input

2.3.3 BT_PCM_DOUT/I2S_DOUT

PCM mode: BT_PCM_DOUT, output

Stereo audio mode: I2S _DOUT, output

2.3.4 BT_PCM_DIN/I2S_DIN

PCM mode: BT_PCM_DIN, input

Stereo audio mode: I2S_DIN, input

2.4 RESET#

Reset signal, active low. The module is reset and the module begins the boot sequence when RESET# input pin transitions from low to high.

2.5 SLEEP_CLK

SLEEP_CLK, clock input for external sleep clock. The sleep clock is used by the PMU during power save modes.

2.6 Joint Test Action Group (JTAG) and Test Interface

JTAG is reserved for SW debug and failure analysis.

JTAG Interface Signal Description

Pin Name	Type	Description
TCK	I	JTAG Test Clock Input
TDI	I	JTAG Test Data Input
TDO	O	JTAG Test Data Output
TRSTn	I/O	JTAG Test Reset (active low)
TMS_CPU	I	JTAG Test Mode Select Selects the internal CPU JTAG controller
TMS_SYS	I	JTAG Test Mode Select Selects the System JTAG controller

2.7 Antenna Diagnosis

If an external antenna equipped a 50Kohm from its RF cable core to GND, then this antenna diagnosis can check whether the antenna is plugged well or not.

2.7.1 VCC_BT_ANT_DIAG and BT_ANT_DIAG

If an external antenna equipped a 50Kohm from its RF cable core to GND and a voltage V_1 is applied to VCC_BT_ANT_DIAG, then BT_ANT_DIAG can be read as $V_1/2$ if the connection of antenna and module is good.

2.7.2 VCC_WLAN_ANT_DIAG and WLAN_ANT_DIAG

If an external antenna equipped a 50Kohm from its RF cable core to GND and a voltage V_2 is applied to VCC_WLAN_ANT_DIAG, then WLAN_ANT_DIAG can be read as $V_2/2$ if the connection of antenna and module is good.

3. Design-In

3.1 Design-in checklist
This section provides a design-in checklist.

3.1.1 Schematic checklist
The following are the most important points for a simple schematic check:

- ☐ DC supply must provide a nominal voltage (3.3V) at VCC_3V3 pins above the minimum normal operating range limit.
- ☐ DC supply must provide a nominal voltage (3.3V) at VCC_VIO_X2 pins above the minimum normal operating range limit.
- ☐ DC supply must provide a nominal voltage (3.3V or 1.8V) at VCC_VIO_X1 pins above the minimum normal operating range limit.
- ☐ DC supply must be capable to provide 0.5A current bursts with maximum 200 mV voltage drop at VCC_3V3 pins.
- ☐ DC supply must be capable to provide 0.1A current bursts with maximum 200 mV voltage drop at VCC_VIO_X2 pins.
- ☐ DC supply must be capable to provide 0.1A current bursts with maximum 100 mV voltage drop at VCC_VIO_X1 pins.
- ☐ VCC_3V3 supply should be clean, with very low ripple/noise (less than 200mV_{pp}): suggested passive filtering parts can be inserted.
- ☐ VCC_VIO_X1 supply should be clean, with very low ripple/noise (less than 100mV_{pp}): suggested passive filtering parts can be inserted.
- ☐ VCC_VIO_X2 supply should be clean, with very low ripple/noise (less than 200mV_{pp}): suggested passive filtering parts can be inserted.
- ☐ Connect only one DC supply to VCC_3V3: different DC supply systems are mutually exclusive.
- ☐ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☐ Check UART signals direction.
- ☐ Check the digital audio interface specifications to connect a proper device.
- ☐ To avoid an increase of module current consumption in power down mode, any external signals connected to the module digital pins (UART, PCM, SDIO interface) must be set low or tri-stated when the module is in power down mode.
- ☐ Any external signal connected to the digital audio interface must be tri-stated when the module is in power down mode and must be tri-stated during the module power-on sequence (at least for 1500 ms after the start-up event).
- ☐ Provide proper precautions for ESD immunity as required on the application board.
- ☐ All the not used pins can be left floating on the application board.

3.1.2 Layout checklist

The following are the most important points for a simple layout check:

- ☐ Check 50 Ω impedance of ANT line (WLAN_RF, BT_RF).
- ☐ Follow the recommendations of the antenna producer for correct antenna installation and deployment.
- ☐ Ensure no coupling occurs with other noisy or sensitive signals.
- ☐ VCC line (VCC_3V3, VCC_VIO_X1, VCC_VIO_X2)should be wide and short.
- ☐ Route VCC supply line away from sensitive analog signals.
- ☐ Ensure proper grounding.
- ☐ Optimize placement for minimum length of RF line and closer path from DC source for VCC.

3.2 Design Guidelines for Layout

The following design guidelines must be met for optimal integration of WLAN+BT modules on the final application board.

3.2.1 Layout guidelines per pin function

This section groups the module pins by signal function and provides a ranking of importance in layout design.

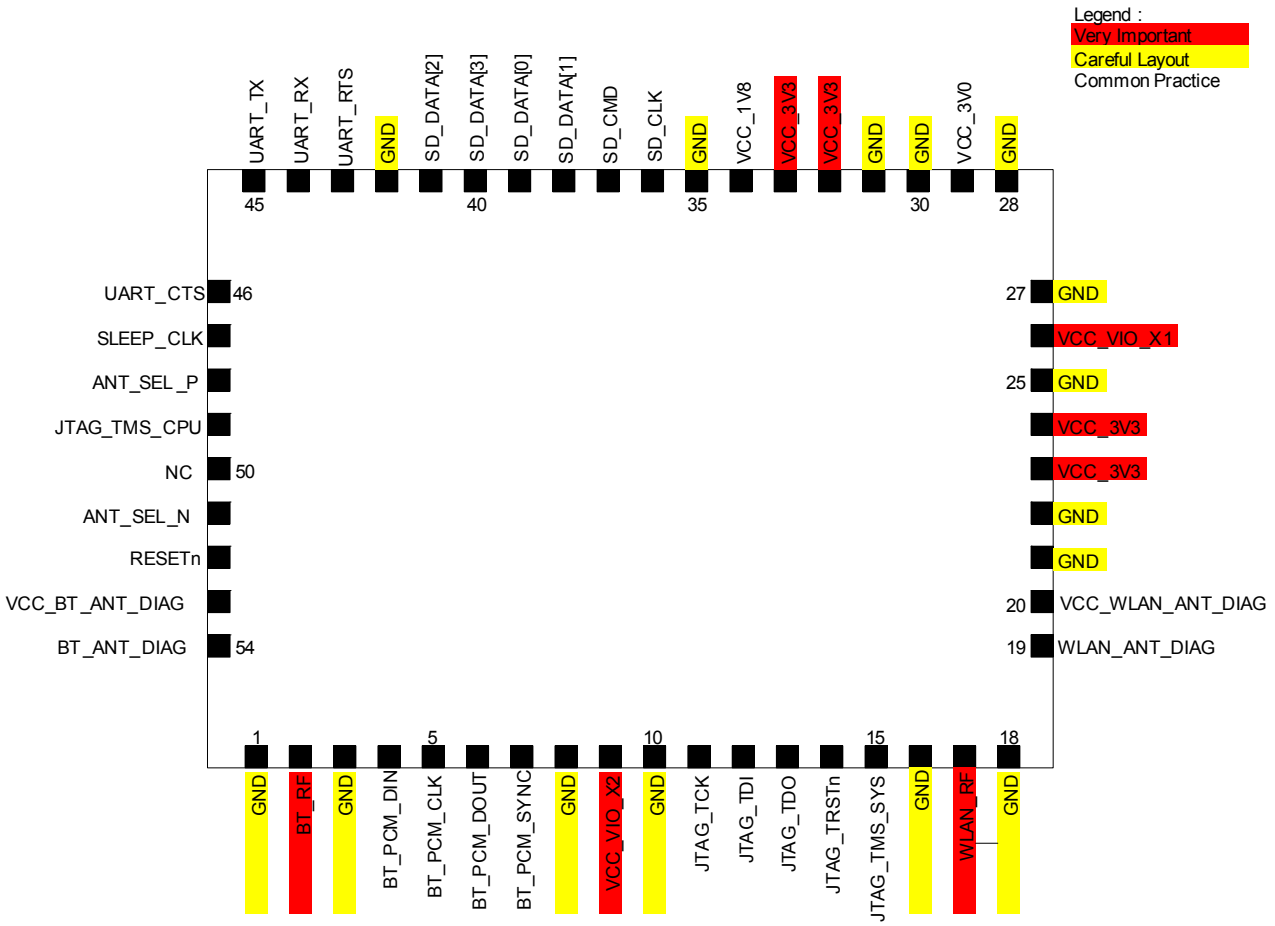


Figure 3-1: Module pin-out with highlighted functions

Rank	Function	Pin(s)	Layout	Remarks
1st	RF in/out	BT_RF WLAN_RF	Very Important	Design for 50 ohm characteristic impedance
2nd	DC Supply	VCC_3V3 VCC_VIO_X1 VCC_VIO_X2	Very Important	VCC lines should be short and wide. Route away from sensitive analog signals.
3rd	Ground	GND	Careful Layout	provide proper grounding.
4th	Digital Pins:		Common Practice	Follow common practice rules for digital pin routing.
	SDIO interface	SD_CLK, SD_CMD, SD_DAT_0, SD_DAT_1, SD_DAT_2, SD_DAT_3		
	UART	TXD, RXD, CTS, RTS		
	Digital Audio	BT_PCM_DIN, BT_PCM_SYNC, BT_PCM_CLK, BT_PCM_DOUT		
	RESET	RESET#		
	Sleep Clock	SLEEP_CLK		
	Antenna Detection	VCC_BT_ANT_DIAG, BT_ANT_DIAG, VCC_WLAN_ANT_DIAG, WLAN_ANT_DIAG		
	Antenna Select	ANT_SEL_P, ANT_SEL_N		
	JTAG	JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TRSTn, JTAG_TMS_SYS, JTAG_TMS_CPU		

Table 3-1: Pin list in order of decreasing importance for layout design

3.2.1.1 RF I/O connection

The RF antenna connection pin BT_RF & WLAN_RF are very critical in layout design. The PCB line must be designed to provide 50 Ω characteristic impedance and minimum loss up to radiating element.

- Provide proper transition between the BT_RF & WLAN_RF pads to application board PCB.
- Increase GND keep-out (i.e. clearance) for BT_RF & WLAN_RF pins to at least 250 µm up to adjacent pads metal definition and up to 250 µm on the area below the Data Module, as described in Figure XXX.
- The transmission line up to antenna connector or pad may be a micro strip or a stripline. In any

case must be designed to achieve 50 Ω characteristic impedance.

- Microstrip lines are usually easier to implement and the reduced number of layer transitions up to antenna connector simplifies the design and diminishes reflection losses. However, the electromagnetic field extends to the free air interface above the stripline and may interact with other circuitry.
- Buried stripline exhibits better shielding to incoming and generated interferences. Therefore are preferred for sensitive application. In case a stripline is implemented, carefully check that the via pad-stack does not couple with other signals on the crossed and adjacent layers.
- Minimize the transmission line length; the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- The transmission line should not have abrupt change to thickness and spacing to GND, but must be uniform and routed as smoothly as possible.
- The transmission line must be routed in a section of the PCB where minimal interference from noise sources can be expected.
- Route ANT line far from other sensitive circuits as it is a source of electromagnetic interference.
- Avoid coupling with VCC routing and analog audio lines.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer.
- Add GND vias around transmission line.
- Ensure no other signals are routed parallel to transmission line, or that other signals cross on adjacent metal layer If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the trace width of the micro strip, use the “Coplanar Waveguide” model for 50 Ω characteristic impedance calculation.
- Don’t route microstrip line below discrete component or other mechanics placed on top layer.
- When terminating transmission line on antenna connector (or antenna pad) it is very important to strictly follow the connector manufacturer’s recommended layout.
- GND layer under RF connectors and close to buried vias should be cut out in order to remove stray capacitance and thus keep the RF line 50 Ω. In most cases the large active pad of the integrated antenna or antenna connector needs to have a GND keep-out (i.e. clearance) at least on first inner layer to reduce parasitic capacitance to ground. Note that the layout recommendation is not always available from connector manufacturer: e.g. the classical SMA Pin-Through-Hole needs to have GND cleared on all the layers around the central pin up to annular pads of the four GND posts. Check 50 Ω impedance of ANT line.

3.2.1.2 Main DC supply connection

The DC supply of WLAN/BT modules is very important for the overall performance and functionality of the integrated product.

- VCC connection may carry a maximum burst current in the order of 0.5 A. Therefore, it is typically implemented as a wide PCB line with short routing from DC supply (DC-DC regulator, battery pack, etc)
- Each voltage drop in the DC supply track will restrict the operating margin at the main DC source output. Therefore, the PCB connection has to exhibit a minimum or zero voltage drop. Avoid any series component with Equivalent Series Resistance (ESR) greater than a few mΩ.
- Given the large burst current, VCC line is a source of disturbance for other signals. Therefore route VCC through a PCB area separated from sensitive analog signals. Typically it is good practice to interpose at least one layer of PCB ground between VCC track and other signal routing.
- The VCC supply current supply flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.

- A tank capacitor with low ESR is often used to smooth current spikes. This is most effective when placed as close as possible to VCC. From main DC source, first connect the capacitor and then VCC. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the VCC track length. Otherwise consider using separate capacitors for DC-DC converter and WLAN/BT module tank capacitor.
- VCC_3V3 is directly connected to the RF power amplifier. Add capacitor in the pF range from VCC to GND along the supply path.
- Since VCC_3V3 is directly connected to RF Power Amplifier, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is especially seen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to WLAN/BT module in the worst case.
- The large current generates a magnetic field that is not well isolated by PCB ground layers and which may interact with other analog modules (e.g. VCO) even if placed on opposite side of PCB. In this case route VCC away from other sensitive functional units.
- If VCC is protected by transient voltage suppressor / reverse polarity protection diode to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward WLAN/BT module, preferably closer to the DC source (otherwise functionality may be compromised).

3.2.1.3 Module grounding

Good connection of the module with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues.

- Connect each GND pin with application board solid GND layer. It is strongly recommended that each GND pad surrounding VCC and ANT pins have one or more dedicated via down to application board solid ground layer.
- If the application board is a multilayer PCB, then it is required to tight together each GND area with complete via stack down to main board ground layer.
- It is recommended to implement one layer of the application board as ground plane.
- Good grounding of GND pads will also ensure thermal heat sink.

3.2.1.4 Digital pins

- External Reset (RESET#): input for external reset, a logic low voltage will reset the module. RESET# have to be asserted before VCC is powered ON, and the de-assertion of RESET# needs at least 1ms delay after VCC is powered and stable.
- SDIO (SD_CLK, SD_CMD, SD_DAT_0, SD_DAT_1, SD_DAT_2, SD_DAT_3): the SDIO layout may be critical if the application processor is placed far away from WLAN/BT module or in close vicinity of RF antenna. In the first case the long connection may radiate higher harmonic of digital data. In the second case the same harmonics may be picked up and create self-interference that can reduce the sensitivity of WLAN/BT Receiver channels whose carrier frequency is coincident with harmonic frequencies. In the later case using RF bypass capacitors on the digital line will mitigate the problem.
- Digital Audio (BT_PCM_CLK, BT_PCM_SYNC, BT_PCM_DIN, BT_PCM_DOUT): the PCM interface requires the same consideration regarding electro-magnetic interference as the SDIO. Keep the traces short and avoid coupling with RF line or sensitive analog inputs.
- UART (TXD, RXD, CTS, RTS): the serial interface require the same consideration regarding electro-magnetic interference as for SDIO. Keep the traces short and avoid coupling with RF line or sensitive analog inputs.
- JTAG (JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TRSTn, JTAG_TMS_SYS, JTAG_TMS_CPU): the debug

interface require the same consideration regarding electro-magnetic interference as for SDIO. Keep the traces short and avoid coupling with RF line or sensitive analog inputs.

3.2.2 Footprint and paste mask

Figure 3-2 and Figure 3-3 describe the footprint and provide recommendations for the stencil for WLAN/BT modules. These are recommendations only and not specifications.

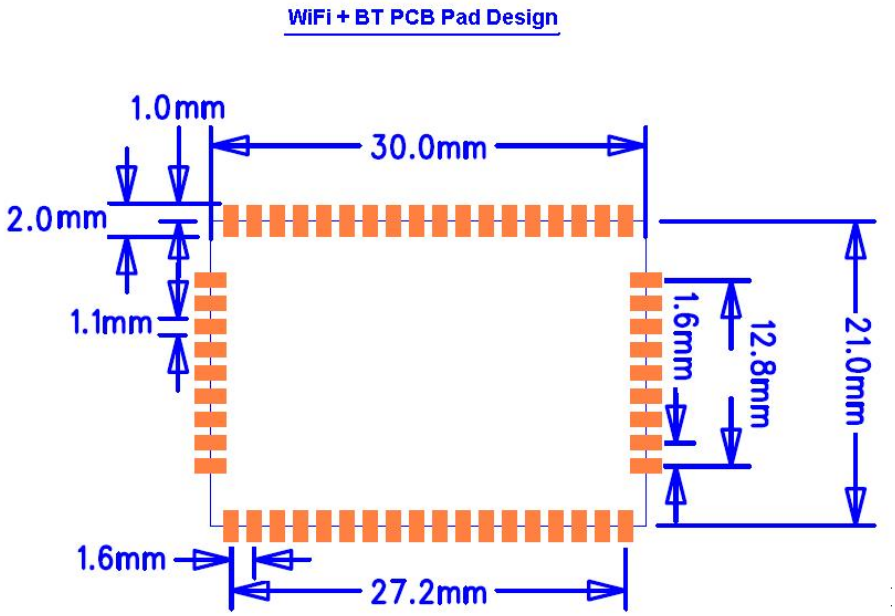


Figure 3-2: WLAN/BT modules pad design

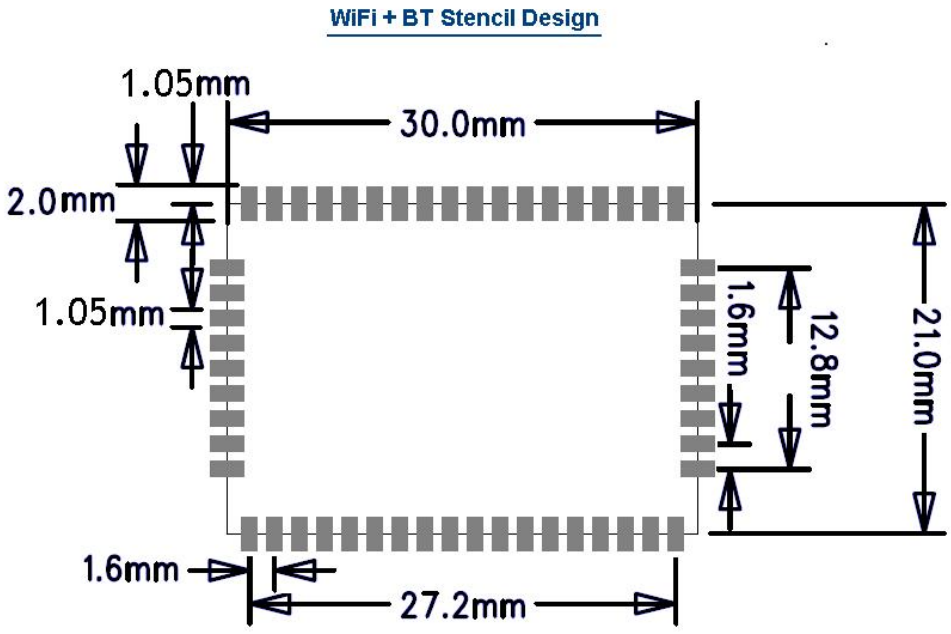


Figure 3-3: WLAN/BT modules stencil design

- The paste mask outline needs to be considered when defining the minimal distance to the next component.
- The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

3.2.3 Placement

Optimize placement for minimum length of RF line and closer path from DC source for VCC.

3.3 Module thermal consideration

The temperature increase of the main chip 88w8688, PA LX5511 and LDO MAX4835 on a WLAN/BT module mounted on a 168 x 46.45 x 1.3 mm FR4 PCB with a high coverage of copper (e.g. the EVK-G25H evaluation kit) in still air conditions are less than 28℃, 25℃, 25℃ respectively. This is based on a worse case with full continuous WLAN TX mode.

This temperature increase will be different than the one provided if the module is mounted on a PCB with different size and characteristics.

3.4 Antenna guidelines

Antenna characteristics are essential for good functionality of the module. The radiating performance of antennas has direct impact on the reliability of connection over the Air Interface. Bad termination of ANT can result in poor performance of the module.

The following parameters should be checked: Item Recommendations

Item	Recommendations
Impedance	50 Ω nominal characteristic impedance
Frequency	WIFI: 2400MHz ~ 2483.5 MHz
	BT: 2400MHz ~ 2483.5MHz
V.S.W.R	<2:1 recommended
Return Loss	S_{11}<-10 dB recommended, S_{11}<-8 dB acceptable
Gain	<3dBi

Table 3-2: General recommendation for antenna

Antennas are typically available as:

- Linear monopole: typical for fixed application. The antenna extends mostly as a linear element with a dimension comparable to lambda/4 of the lowest frequency of the operating band. Magnetic base may be available. Cable or direct RF connectors are common options. The integration normally requires the fulfillment of some minimum guidelines suggested by antenna manufacturer.
- Patch-like antenna: better suited for integration in compact designs. They are mostly custom designs where the exact definition of the PCB and product mechanical design is fundamental for tuning of antenna characteristics.

For integration observe these recommendations:

- Ensure 50 Ω antenna termination, minimize the V.S.W.R. or return loss, as this will optimize the electrical performance of the module.
- Select antenna with best radiating performance.
- If a cable is used to connect the antenna radiating element to application board, select a short cable with minimum insertion loss. The higher the additional insertion loss due to low quality or long cable, the lower the connectivity.
- Follow the recommendations of the antenna manufacturer for correct installation and deployment.
- Do not include antenna within closed metal case.
- Do not place antenna in close vicinity to end user since the emitted radiation in human tissue is limited by S.A.R. regulatory requirements.
- Do not use directivity antenna since the electromagnetic field radiation intensity is limited in some countries.
- Take care of interaction between co-located RF systems since the WIFI/BT transmitted power may interact or disturb the performance of companion systems.

- Place antenna far from sensitive analog systems or employ countermeasures to reduce electromagnetic compatibility issues that may arise.

3.4.1 Antenna termination

WLAN/BT modules are designed to work on a 50 Ω load. However, real antennas have no perfect 50 Ω load on all the supported frequency bands. To reduce as much as possible performance degradation due to antenna mismatch, the following requirements should be met:

- Measure the antenna termination with a network analyzer: connect the antenna through a coaxial cable to the measurement device, the $|S_{11}|$ indicates which portion of the power is delivered to antenna and which portion is reflected by the antenna back to the module output.
- A good antenna should have a $|S_{11}|$ below -10 dB over the entire frequency band. Due to miniaturization, mechanical constraints and other design issues, this value will not be achieved. A value of $|S_{11}|$ of about -8 dB is acceptable.

3.4.2 Antenna diagnosis functionality

The internal antenna diagnosis circuit is based on ADC measurement at ANT_DIAG pin: the RF port is DC coupled to the ADC unit in the application processor which injects a DC voltage (3.3V) on VCC_ANT_DIAG and measures the resulting DC voltage to evaluate the resistance from ANT pad to GND.

The antenna detection is performed by the measurement of the resistance from ANT pad to GND. To achieve good antenna detection functionality, use an RF antenna with built-in resistor from ANT signal to GND, or implement an equivalent solution with a circuit between the antenna cable connection and the radiating element.

Please note that the DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit Figure 53, the measured DC resistance will be always on the extreme of measurement range (respectively open or short), and there will be no mean to distinguish from defect on antenna path with similar characteristic (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

It is recommended to use an antenna with a built-in diagnostic resistor of 51kΩ to assure good antenna detection functionality and to avoid a reduction of module RF performances.

4. Handling and Soldering

4.1 Packaging, shipping, storage and moisture preconditioning

Handling Requirements

DO NOT TOUCH ANY PIN OF WIFI MODULE WHILE ASSEMBLYING.

Moisture preconditioning

This WLAN/BT module meets MSL3. Please follow J-STD-033B to handle this module.

4.2 Soldering Requirements

4.2.1 Soldering Iron Soldering

Solder Temperature: 350^{o}C
Immersion Duration: 2 ~ 3 seconds

4.2.2 Reflow Profile

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.
Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes."

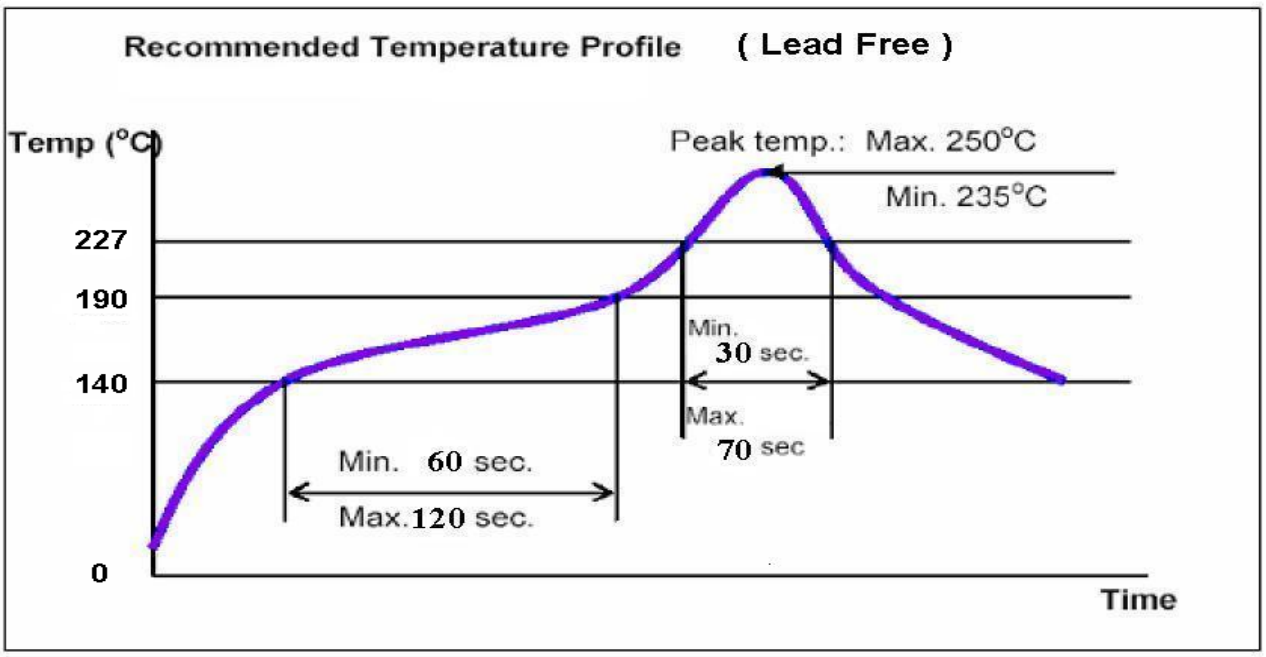
Preheat Phase
Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.
Temperature rise rate: max 3°C/s If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
Preheat Time: 60 ~ 120 sec If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.

End Temperature: 140 ~ 190°C If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ Reflow Phase
The temperature rises above the liquids temperature of 227°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.
Limit time above 227°C liquids temperature: 30 ~ 70 sec

Peak reflow temperature: 235 ~ 250°C

Cooling Phase
A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.
Temperature fall rate: max 4°C / s



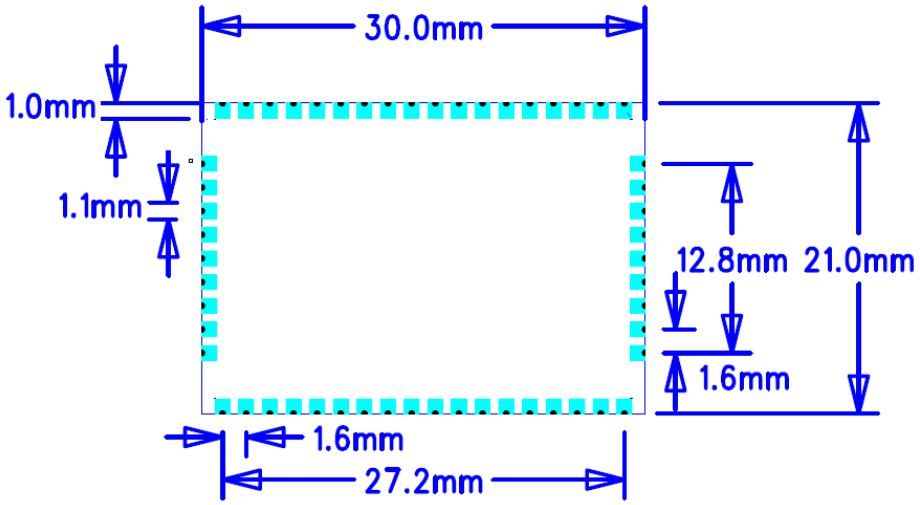
Peak Temperature : 235 ~ 250°C
Reflow Zone (above 227°C or 230°C) : 30 ~ 70 sec.
Preheat Zone (140 ~ 190°C) : 60 ~ 120 sec.

4.2.3 Soldering Paste
Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.
Soldering Paste: ACS-SN100C-MA1
Alloy specification: Sn-0.7Cu-0.05Ni+Ge (99.2% Tin / 0.7 % Copper / 0.05% Nickel / Germanium)
Melting Temperature: 227°C
Stencil Thickness: 120 µm for base boards
The final choice of the soldering paste depends on the approved manufacturing procedures.

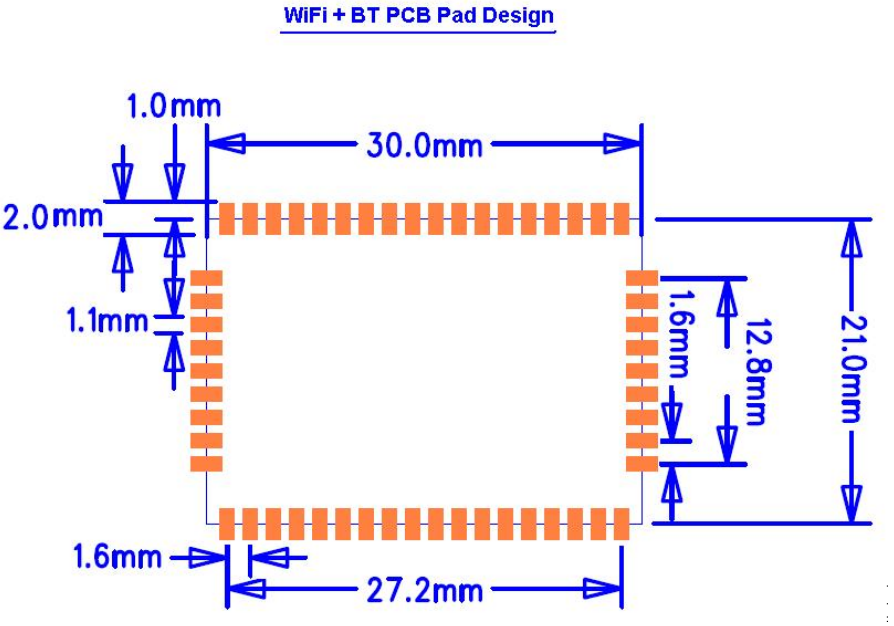
The quality of the solder joints on the connectors (’half vias’) should meet the appropriate IPC specification.

4.2.4 PCB Layout Footprint Design

4.2.4.1 Module Dimensions



4.2.4.2 PCB Layout Pad Design

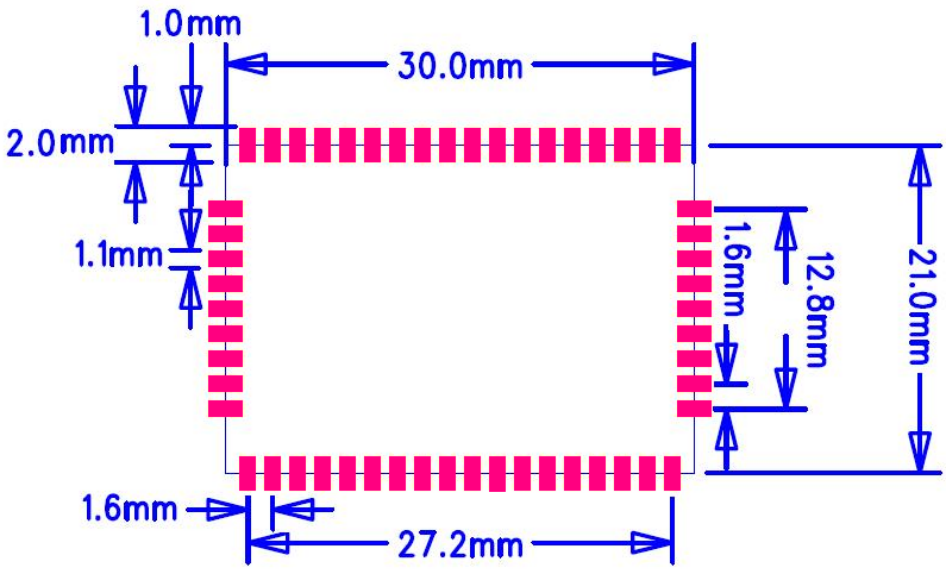


4.2.4.3 Stencil Design

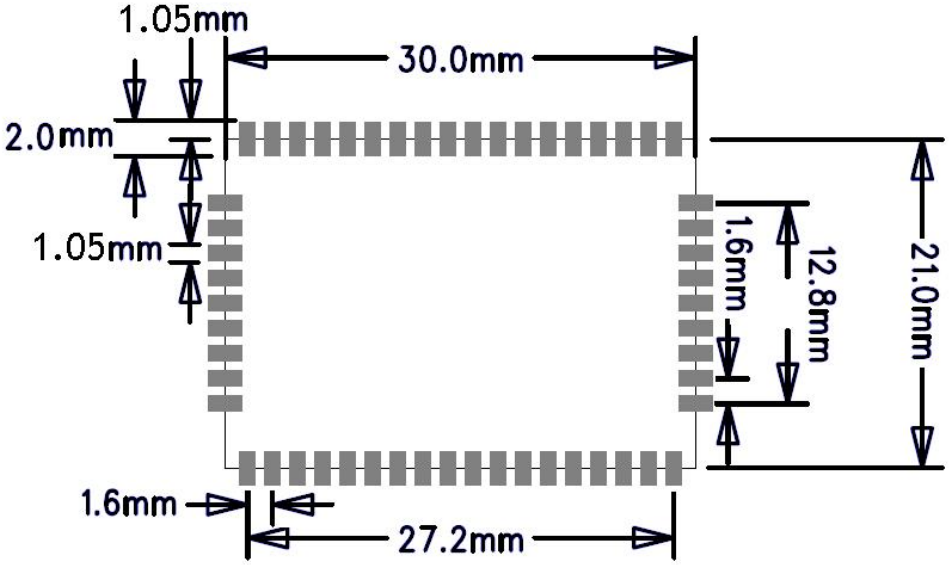
Stencil thickness : 0.10mm ~ 0.15mm.

Solder paste thickness : 0.12mm ~ 0.18mm

WiFi + BT PCB Pad Design



WiFi + BT Stencil Design



5 Product Testing

5.1 Production test

WNC focuses on high quality for its products. All units produced are fully tested. Defective units are analyzed in detail to improve the production quality.
This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Measurement of voltages and currents
- Measurement of RF characteristics
- Test at temperature 75℃ for 30 minutes

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For product available in the USA/Canada market, only channel 1~11 can be operated. Selection of other channels is not possible.

This device and its antenna(s) must not be co-located or operation in conjunction with any other antenna or transmitter.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTE:

This module is intended for OEM integrator. The OEM integrator is still responsible for the FCC compliance requirement of the end product, which integrates this module.

20cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the FCC radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's

authority to operate this equipment. If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: NKRUWMWBT-CWM01". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.