Section 4.0 Theory

4.1 General

The NAT Transceivers are a GE (General Electric) RANGR™ radio converted for use with aircraft power and audio requirements. The conversions completed by NAT make the transceivers compatible with typical aircraft requirements.

Parts of the original GE Maintenance Manuals have been included in this section to provide the most complete manual possible. There are two seperate GE manuals. The first to be included pertains to the VHF Low band transceivers (NT30 series), and the second pertains to the VHF High band transceivers (NT136/150 series). Most aspects of the transceiver remain the same as designed and therefore, the original GE manual will provide the majority of the required information.

Changes, deletions, and/or additions are included in this section and should be consulted to determine if the information given in the original manual is applicable. Do not confuse these changes to the original GE manual with amendments to the NAT service manual that may be issued in the future.

For system block diagrams to help understand the theory, refer to Section 6.2 pages D2 to D7.

4.2 GE Manual Additions

4.2.1 PA Board

The PA board contains the RF output stage, output low-pass filter, switching power supply, and antenna relay circuits.

RF input drive is obtained from the Exciter via a plug-in co-ax cable adjacent to the RF power module (HC1). The power module amplifies the 400 mW input to 1 or 10 Watts. It is capable of amplifying greater than 10 Watts, but the driver voltage will approach and finally exceed recommended levels and may destroy the power module.

The RF output is coupled through a co-ax feedline to the directional coupler, which provides leveling information as well as fault protection. Then it is routed through stripline connections to the transmit relay and output low-pass filter.

A DC signal developed from the directional coupler is used by the power control circuit to adjust the DC bias on pin 2 of HC1. This in turn varies the resulting RF output power. By adjusting this bias, 1 Watt and 10 Watt outputs are obtained, as well as

power leveling over the bandwidth of the radio.

4.2.2 Transmitter Power Level Adjust

IC202 samples the DC voltage produced by the directional coupler, and amplifies it to a usable level at all RF power settings. This is then combined with the transmit interlock voltage provided by TR8, and used to provide a variable DC level to pin 2 of HC1. This varying DC level changes the resulting RF output power of the power hybrid circuit, and allows simple remote adjustment.

IC203 interfaces a logic command from the control head to the level control circuit formed by IC102 so that either a high (10 W) or low (1 W) RF level can be remotely selected. Latitude of setting is allowed in this circuit in both high and low power modes, but, the maximum output is limited by HC1 parameters and input drive. This will not normally exceed 16 W under any condition.

4.2.3 28V DC Power Distribution And Conversion (NT136/NT150)

+28V DC and airframe ground enter the radio through the airframe connector (P101), and are routed to the NT150-1 Power Supply card located in the transmitter compartment. After transient protection and filtering, DC is applied to the regulator (U101) via the MOSFET (Q101).

The voltage regulator/converter (U101) with its associated bypass capacitors, catch diode (D102), storage inductor (L102) and reservoir capacitor (C112), provide DC-to-DC voltage down-conversion. The output level is set by R105 to 13.0 VDC. Filtering of the low voltage DC is provided by a follow-on filter consisting of L103, C113, C114 and associated components. These reduce the switching artifacts from the DC-to-DC converter, and provide filtered DC to the transceiver.

4.2.4 28V DC Power Distribution And Conversion (NT30A/B)

+28V DC and airframe ground enter the radio through the airframe connector (P101), and are routed to the NT30-1 Power Supply module located adjacent to the Receiver Board. After transient protection and filtering, DC is applied to the switch mode regulator (U1) via the MOSFET (Q1).

The voltage regulator/converter (U1) with its associated bypass capacitors, catch diode (D4), storage inductor (L2) and reservoir capacitors (C11, C12), provide DC-to-DC voltage down-conversion. The output level is set by R9 to 13.0 VDC. Filtering of the low voltage DC is provided by a follow-on filter consisting of L3, C13, C14 and FL2. These reduce the switching artifacts from the DC-to-DC converter, and provide filtered DC to the transceiver.

For diagnostic purposes, there are two BIT (Built-In Test) LEDs on the NT30-1 module. The green LED (D7) verifies +28V power is reaching regulator U1, confirms operation of the series pass MOSFET (Q1), and the POWER KEY line. The orange LED (D8) verifies that output voltage is present.

4.2.5 Sidetone Circuit

During aircraft transmissions, a replica of the transmit audio is normally echoed back to the pilot (sidetone) to indicate that the radio is functional. In the NT series transceivers, a signal is taken from the first microphone amplifier and TX enable logic and routed to the audio output stage to produce this signal. The level of this signal is adjustable to allow for specific aircraft requirements (Sidetone Adjust). The sidetone level is set to 25 mW into 600 ohms and is independent of the receive level regardless of external control head level settings.

4.2.6 Headphone Circuit

The output stage of the transceiver provides a high level output in a floating bridge configuration. This is used to drive a speaker or transformer coupled output for isolation. The transformer coupled output is capable of driving either 150 or 600 ohm lines. RV602 is factory set to provide 200 mW into 600 ohms.

4.3 GE Manual Changes/Deletions

Page No.	Column	Para.	Beginning	Action	Change...	To...
C2	left	6	NOTE	Ignore		
C7	left	4	The audio...	Change	10-Watts	4-W.
C7	left	4	The audio...	Change	...a 4 ohm	an 8Ω
C19	left	1	The PA...	Ignore		
C19	left	7-11	The power...	Ignore		
C19	right	1-3	The power...	Ignore		
C19	right	8	When the...	Ignore		
C20	left	1-8	If the...	Ignore		
C20	right	1,2	The 12..	Ignore		

Section 4.0 ends after GE Maunual inserts.

MAINTENANCE MANUAL

FCC ID: GOLNT030

29-50 MHz BOARD ASSEMBLIES

TABLE OF CONTENTS

DESCRIPTION

The System Control board for RANGR provides all functions necessary for two-way communications. This board is controlled by the control unit.

The System Control board interconnects with the power/control cable from the control unit.

The System Control board contains the audio circuitry, microcomputer, EEPROM and voltage regulators. The micro-computer controls all system functions, supplies frequency data to the frequency synthesizer, and tone/code data to the Channel Guard.

In addition to the normal radio functions, the microcomputer contains self-diagnostic maintenance routines to aid in troubleshooting the radio. Included are an internal test of the microcomputer and input/output tests to assure proper operation of the data port and data bus. Details and procedures are included in the Service Section of this manual.

The system control and interface circuits consist of the microcomputer, electrically eraseable PROM, interface circuits for voltage shifting and protection, and a watchdog timer. The EEPROM gives the user the capability to program the radio's personality as desired. The EEPROM contains the receive and transmit frequency data, Channel Guard tone frequencies/digital codes and the CCT delay on a per-channel basis.

NOTE

The EEPROM may be programmed serially through the front connector using the General Electric Universal Radio Programmer Model TQ2310.

CIRCUIT ANALYSIS

SYSTEM CONTROL BOARD

MICROCOMPUTER AND CONTROL

The microcomputer interfaces with the control unit through J701/J702 and responds to all user commands and control functions originating from the control unit. It provides the transmit and receive data to the frequency synthesizer, switching information for tone and digital Channel Guard, and provides the carrier control timer (CCT) function when the radio is in the transmit mode.

When the microphone is keyed, the $\overline{\text{PTT}}$ line from the control unit goes low. This low is applied to the microcomputer through buffer TR702 and inverter TR703. TR702 is controlled by ignition switch A+. The ignition switch must be on and A+ applied to the base of TR702. TR702 must be turned on to permit keying of the transmitter. When Channel Guard is present, the release of the PTT signal is delayed by the microcomputer for approximately 160 milliseconds to eliminate any squelch tail.

The microcomputer immediately closes the antenna relay switch by applying a low level to $\overline{\text{DPTT}}$ at IC702-28. The microcomputer then delays 15 milliseconds before transmit 9V is switched on by applying a low level to $\overline{\text{TX ENB}}$ at IC702-32. This is done to guarantee that the antenna relay contacts are closed before the transmitter is energized. Once $\overline{\text{DPTT}}$ is low, the receive audio is muted. Buffers TR705 and TR704 provide $\overline{\text{DPTT}}$ to the audio control circuits, and antenna relay. IC704-B provides the DPTT signal to the Tx/Rx VCO's and the audio processor.

The $\overline{\text{TX ENB}}$ line is controlled by microcomputer port 1, bit 5 (IC702-32) through inverter TR712 and buffer TR711. A low level on IC702-32 turns TR712 off, allowing the base of TR711 to rise. TR711 turns on, and applies A- to the $\overline{\text{TX ENB}}$ line. Inverter TR710 is also turned on during this time to inhibit the alert tone PTT.

CHANNEL SELECTION

The microcomputer and EEPROM provide the radio with up to 16 independent transmit and receive frequencies. Each time the PTT switch is operated the microcomputer transfers channel data from the EEPROM and converts it to frequency data assigned to the selected channel. The frequency data is then loaded serially into the frequency synthesizer.

The microcomputer continually monitors the status of tri-state buffers IC703A-D. These buffers are periodically turned off by a positive 5 volt, one millisecond pulse from IC702-36. At the same time PROM power switch TR708 is turned on and applies +5 VDC to the EEPROM. When the buffers are turned on, channel select data is loaded into input/output ports of the microcomputer through ports P20-P23. Power is then applied to the EEPROM and the tri-state buffers are turned off. The microcomputer converts the channel select data into address information, accesses the EEPROM, and receives the frequency data stored in the addressed location. This data then passes through the I/O ports of the EEPROM and P20-P23 of the microcomputer. The conversion process is repeated eight times in rapid succession (eight locations are required for each channel) and the data loaded serially into the frequency synthesizer over the clock and data lines. This data also includes Channel Guard information, if present, and carrier control timer information on a per-channel basis. A 4-millisecond channel change pulse from port P16 of the microcomputer is also sent to the frequency synthesizer to speed up channel acquisition.

WATCHDOG TIMER

The watchdog timer, consisting of a digital counter IC701-A and TR701, monitors the operation of the microcomputer. IC701-A generates a reset pulse in the unlikely condition that the microcomputer goes awry and does not execute the software properly.

A 6 MHz crystal X701 steps the microcomputer through the software. As programmed in software a random pulse appears at IC702-35 and is applied to the base of inverter TR701 momentarily turning it on and inhibiting any reset pulse from timer IC701-A. A discharging circuit consisting of R710 and C705 forces the microcomputer to toggle IC702-A. If the timer does not receive any inputs for a specified period of time, TR701 turns off and IC701-A times out and applies a reset pulse to pin 4 of the microcomputer. The watchdog reset will normally restore the microcomputer to normal operation so that only one pulse will occur. In the event the microcomputer is not restored to normal operation, a 6 Hz square wave will appear on the reset line and the indicator CD711 (normally unlit) will turn on.

ADVANCE CHANGE PULSE

The advance change pulse is received from connector J702 and applied to the microcomputer interrupt port IC702-6 through inverter TR707. The advance change pulse is important in radios equipped with PSLM. When a call is received on a priority channel the advance change pulse interrupts the microcomputer, forcing it to service immediately the I/O circuits. The tri-state buffers are turned on and new channel select information read in.

CARRIER CONTROL TIMER

The carrier control timer function is executed by the microcomputer under software control on a per-channel basis. When the programmed time has elapsed an alert tone is generated from P13 (IC702-30) on the microcomputer, applied to the audio PA and heard on the speaker. The CCT may be programmed for 1 or 2 minutes or disabled (programmed for no CCT).

VOLTAGE TRANSLATION

Inverter buffers IC704D-G, translate the 5 VDC levels required by the microcomputer to the +9 VDC level used by the frequency synthesizer. Inverter TR709 restores the proper polarity to the clock.

FREQUENCY SEGMENT CONTROL

To achieve rapid wideband VCO tuning extending over the 29-42 MHz range or the 35-50 MHz range, each Bandsplit is divided into four frequency segments.

By selecting one segment the operating frequency spread of the VCO is limited and frequency lock time reduced. Each segment is identified by two bits on a per-channel basis and programmed into the EEPROM. Capacitors are switched in and out of the VCO tank circuit to set the VCO tuning range to cover the correct frequency segment.

The frequency segment control circuit consists of a dual "D"-type flipflop operating under control of the microcomputer. The four frequency segment identification bits appear on the channel change and data lines and fed to dual "D" FF IC705. At the appropriate time the microcomputer applies the enable signal to clock the new segment data change through the FF. The output of the FF's is a binary expression identifying the frequency segment selected. Table 1 identifies the binary expression and the selected frequency segment.

The output of the frequency segment control circuit is applied to the modulation level control and the frequency segment selector circuits.

★

	SEGMENT	FREQUENCY SPLIT (MHz)	FF OUTPUT				GROUNDED MODULATION RESISTOR
			IC705-1 (INPUT TR216)	IC705-2 (INPUT TR217)	IC705-13 (INPUT TR218)	IC705-12 (INPUT TR219)	
29-42MHz	1	29-32	0	1	0	1	NONE
	2	32-35	0	1	1	0	R275
	3	35-38.5	1	0	0	1	R276, R296
	4	38.5-42	1	0	1	0	R275, R276 R281, R296
35-50MHz	1	35-38.5	0	1	0	1	NONE
	2	38.5-42	0	1	1	0	R275
	3	42-46	1	0	0	1	R276, R296
	4	46-50	1	0	1	0	R275, R276 R281, R296

TABLE 1 - Frequency Segment Selection

TX AUDIO PROCESSOR

The audio processor provides audio pre-emphasis with amplitude limiting and post limter filtering and a total gain of approximately 24 dB. Approximately 27 dB gain is provided by IC607A, 4 dB by IC607B and -7 dB by R666, R667.

The 9 Volt regulator IC606 powers the audio processor and applies regulated 9 volts to a voltage divider consisting of R665, R668 and symmetry control, RV603. The +4.5 V output from the voltage divider establishes the operating reference point for operational amplifiers IC607A and IC607B. C636 provides an AC ground at the summing input of both operational amplifiers.

When the input signal to IC607A-2 is of a magnitude such that the amplifier output at IC607A-1 does not exceed 5 volts P-P, the amplifier provides a nominal 27 dB gain. When the audio signal level at IC607A-1 exceeds 5 volts P-P, the amplifier gain is reduced to 1. This limits the audio amplitude at IC607A-1 to 6 volts P-P.

Resistors R662, R663 and C633 comprise the audio pre-emphasis network that enhances the signal-to-noise ratio. R663 and C633 control the pre-emphasis curve below limiting. R662 and C663 control the cut-off point for high frequency pre-emphasis. As high frequencies are attenuated, the gain of IC607 is increased.

Audio from the microphone is coupled to the audio processor through R662 and C633.

The amplified output of IC607A is coupled through R666, C633, R669, R670, R671 and bilateral switch IC608C to a second operational amplifier IC607B. The bilateral switch is controlled by the DPTT line so that Tx audio is transmitted only when the PTT switch is pressed. IC607B provides a signal gain of approximately 4 dB.

The Channel Guard tone input is applied to bilateral switch IC608C controlled by the DPTT line. The CG tone then modulates the reference oscillator and VCO on the synthesizer board.

A post-limiter filter consisting of IC607B, R669-R671, R687, C689 and C640 provides 12 dB per octave roll-off. R666 and C637 provide an additional 6 dB per octave roll-off for a total of 18 dB. The output of the post-limiter filter is coupled through the VG (Voice Guard) unit or directly to the synthesizer Tx MOD.

TX enable switch IC608-D shorts out operational amplifier IC607-B when the radio is in the receive mode. The TX ENABLE signal is generated by the microcomputer when the PTT switch is operated and is less than 2.7 VDC in the receive mode.

RX AUDIO

Received audio from the FM detector is applied to the input of audio pre-amplifier IC603-A. The audio output level of the audio preamplifier is adjusted by Volume/Squelch HI level control RV602 for 300 millivolts RMS. The audio of 300 millivolts RMS is applied to the audio preamplifier (IC603-B) through the Tone Reject filter (HC603). When VG is opptionally added, this audio is applied to VG (Voice Guard) circuit (IC611, HC603). Audio output from the VG circuit is applied to Tone Reject filter (HC605) through pins J606-2 & 3. The audio is then applied to the volume and squelch controls in the control unit through connector J701-10.

Audio is returned on the VOL ARM through J701-18 and applied to audio gate (bilateral switch) IC601-B. The audio gate is controlled by DPTT (delayed Push-To-Talk) and PA KEY/CCT PA ENB and is turned on when the control input (pin 5) exceeds 7 VDC. The gate is turned off when the control input is less than 2 volts. Receipt of an on-frequency signal (if present) with

sufficient signal-to-noise level and the correct Channel Guard frequency will cause the audio control circuit to apply +9 volts to IC601-B turning the audio gate on.

Audio from the audio gate is applied to the de-emphasis network consisting of a low-pass filter and a high-pass filter.

The low-pass filter provides a 6 dB per octave roll-off between 300 and 3000 Hz. The high-pass filter attenuates frequencies below 300 Hz.

The audio output from the de-emphasis network is applied to the non-inverting input of the audio power amplifier. The audio power amplifier consists of IC602, and associated circuitry, and provides 10-watts (6.3 VRMS across a 4 ohm load) of audio output power at terminals J702-20 and 22. The gain of IC602 is determined by the value of R622.

SQUELCH CIRCUITS

The squelch circuit(HC601)monitors noise on the SQ ARM output line and allows the receiver to be unmuted when an on-frequency signal reduces the noise level below the squelch threshold setting.

The 300 millivolt output of the audio preamplifier is applied to the squelch circuit through the variable squelch control in the control unit. The squelch control sets the noise threshold level required to operate the squelch circuit. When the noise falls below the threshold level, the receiver is unmuted.

The squelch circuit(HC601) consists of a high-pass filter, an averaging detector, DC amplifier, and a Schmitt trigger shown in Figure 1. The high-pass filter consisting of HC601-A, removes all voice signals from the SQ ARM output and couples noise to HC601-B.

Noise in the 6-8 kHz range is applied to the averaging detector consisting of HC601-B. The noise is rectified and filtered to provide an average DC output level proportional to the noise input. The DC output level is adjusted by RV601.

The average DC level is amplified by HC601-C to a level ranging from 0 to 6.0 VDC, and applied to the non-inverting input of the Schmitt trigger, HC601-D. The inverting input of HC601-D is referenced to 4.5 VDC. IC603-C provides the stable 4.5 VDC reference voltage.

When the DC level exceeds 4.5 VDC, Schmitt trigger HC601-D switches and provides a positive voltage to the CAS (Carrier Activity Sensor) and RUS (Receiver Unsquelched Sensor) control transistors in the audio control circuits. The Schmitt trigger will remain on until the threshold level falls below approximately 4.3 VDC. This difference in voltage between the firing point and turn-off point provides sufficient hysterisis to eliminate "bubbling" -- i.e., noise popping in the speaker. The "bubbling" would normally be caused by transitional changes in the DC level around the reference point which allows the receiver to be unmuted.

When an on-frequency signal is received, there will be little or no noise present at the squelch input. This results in an absence of voltage at the output of the squelch circuit Schmitt trigger, allowing the receiver to be unmuted.

AUDIO CONTROL

The audio control circuits shown by Figure 2 control the operation of the audio gate (IC601-B) and the final audio PA and consist of TR601-605, inverter IC601-A and associated circuitry. The audio control circuit inputs consist of $\overline{\text{DPTT}}$ (Delayed Push-To-Talk), $\overline{\text{RX MUTE}}$ (Receiver Mute), PA KEY/CCT PA $\overline{\text{ENB}}$ (Public Address Key/Carrier Control Timer Public Address Enable), and the output of the squelch circuit.

When an on-frequency signal with the correct Channel Guard Tone is received, CAS control transistor TR601 and RUS control transistor TR602 are turned off by the absence of a positive voltage at their bases. The CAS line from the collector of TR601 rises to +9 VDC and is supplied to J701-14.

The collector of RUS Transistor TR602 also rises to +9 VDC and turns on inverter IC601-A. A- is then applied to the base of inverter TR603, turning it off and allowing its collector to go high. The positive voltage on the collector is applied to audio gate IC601-B, turning it on. TR604 is biased on but has no effect on audio switches TR605. The base of the transistor is connected to the output of audio control switch IC601A-2 which is at A-. Therefore TR605 turns off, allowing input audio to the PA which feed audio power to the speaker.

When the microphone is keyed, the $\overline{\text{DPTT}}$ input is low. This low is applied to audio gate IC601-B through CD603B, turning IC601-B off. It is also applied to audio control switch IC601-A (through CD603A) turning it off. TR603 is also off and TR604, TR605 are on. TR605 shorts out the audio input to the audio PA IC602.

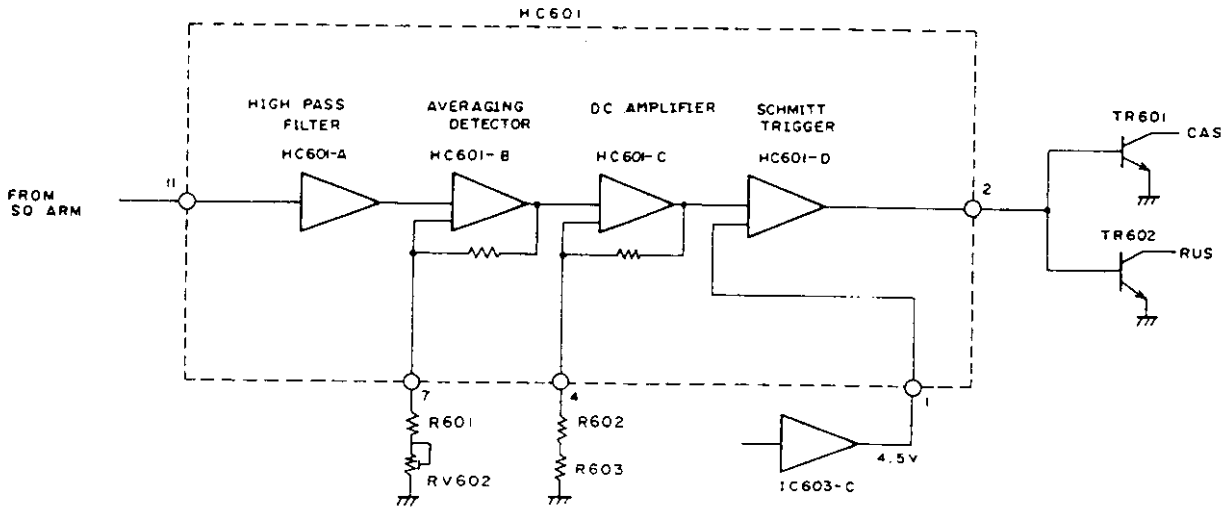

Figure 1 - Squelch circuits (HC601)

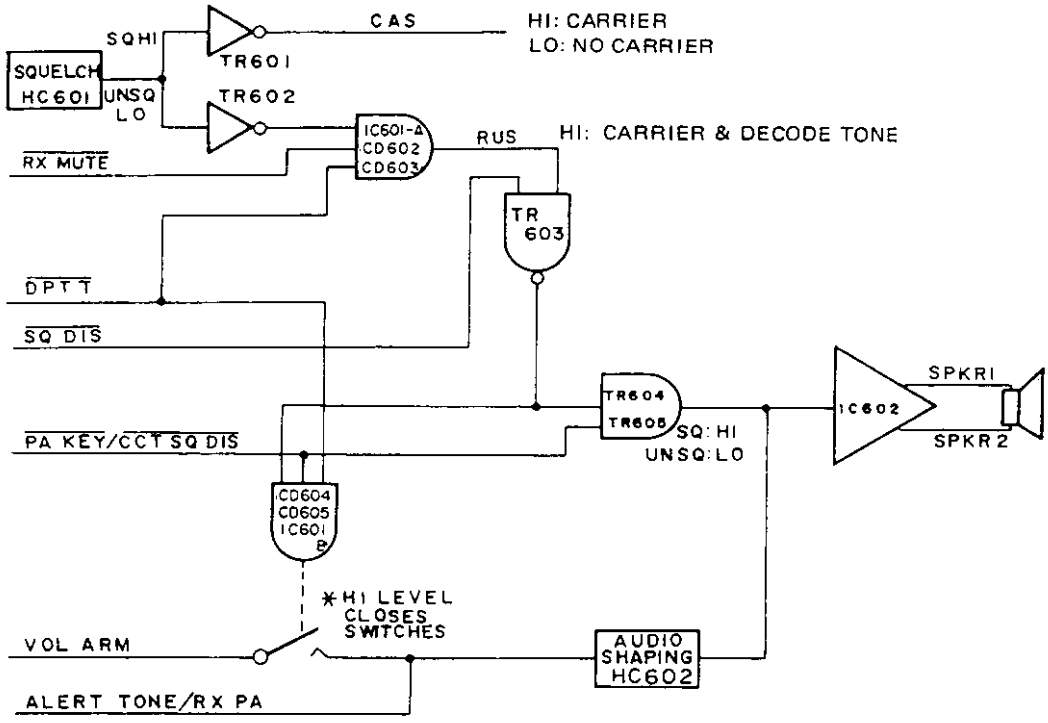

Figure 2 - Audio Control Circuit

POWER DISTRIBUTION

Battery supply A+ enters the radio through the front connector at J801-19. A- enters through J801. Figure 3 is a block diagram of the power distribution system. Two heavy connections are provided for transmit A+ and transmit A- and connect to two busses. The busses are connected to the PA through a special feedthrough arrangement. A second set of wires is routed through the control unit and supplies power to the audio amplifier and all other radio circuitry.

CAUTION

The CMOS Integrated Circuit devices used in this equipment can be destroyed by static discharges. Before handling one of these devices, the serviceman should discharge himself by touching the case of a bench test instrument that has a 3-prong power cord connected to an outlet with a known good earth ground. When soldering or desoldering a CMOS device, the soldering iron should also have a 3-prong power cord connected to an outlet with a known good earth ground. A battery-operated soldering iron may be used in place of the regular soldering iron.

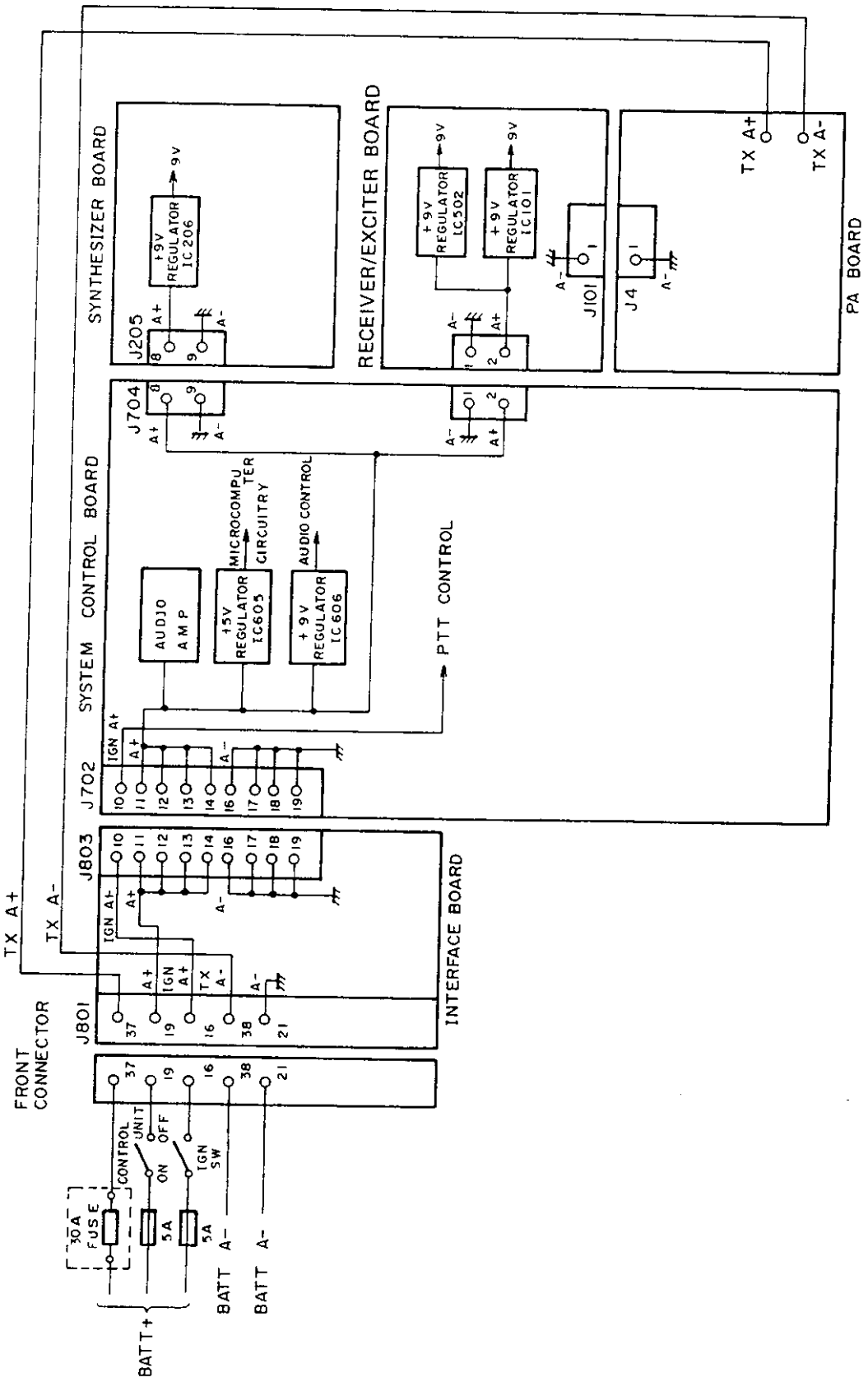

Figure 3- Power Distribution

CHANNEL GUARD

Channel Guard provides a means of restricting calls to specific radios through the use of a continuous-tone or digitally-coded squelch system (CTCSS or CDCSS). Tone frequencies range from 67 Hz to 210.7 Hz, 33 standard tones and 83 unique digital codes are available. These tones/codes are identified in Tables 2 and 3.

STANDARD TONE FREQUENCIES Hz				
67.0	88.5	107.2	131.8	167.9
71.9	91.5	110.9	136.5	173.8
74.4	94.8	114.8	141.3	179.9
77.0	97.4	118.8	146.2	186.2
79.7	100.0	123.0	151.4	192.8
82.5	103.5	127.3	156.7	203.5
85.4			162.2	210.7

TABLE 2 - Channel Guard Tone Frequencies

PRIMARY CODE	EQUIVALENT CODE	PRIMARY CODE	EQUIVALENT CODE	PRIMARY CODE	EQUIVALENT CODE
023	340, 766	205	135, 610	464	237,642, 772
025		223	350, 475, 750	465	056, 656
026	566	226	104, 557	466	144, 666
031	374, 643	243	267, 342	503	157, 312
032		244	176, 417	506	224, 313, 574
043	355	245	370, 554	516	067, 720
047	375, 707	251	236, 704, 742	532	161, 345
051	520, 771	261	227, 567	546	317, 614, 751
054	405, 675	263	213, 136	565	307, 362
065	301	265	171, 426	606	153, 630
071	603, 717, 746	271	427, 510, 762	612	254, 314, 706
072	470, 701	306	147, 303, 761	624	075, 501
073	640	311	330, 456, 561	627	037, 560
074	360, 721	315	321, 673	631 745	231, 504, 636
114	327, 615	331	372, 507	632	123, 657
115	534, 674	343	324, 570	654	163, 460, 607
116	060, 737	346	616, 635, 724	662 444	363, 436, 443,
125	172	351	353, 435	664	344, 471, 715
131	572, 702	364	130, 641	703	150, 256
132	605, 634, 714	365	107	712	136, 502
134	273	371	217, 453, 530	723	235, 611, 671
143	333	411	117, 756	731	447, 473, 474
152	366, 415	412	127, 411, 711		744
155	233, 660	413	133, 620	732	164, 207
156	517, 741	423 713	234, 563, 621	734	066
162	416, 553	431	262, 316, 730	743	312, 515, 663
165	354	432	276, 326	754	076, 203
172	057	445	222, 457, 575		
174	142, 270				

TABLE 3 - Primary and Equivalent Digital Codes (Octal)

★

The Channel Guard encode and decode functions are implemented in the microcomputer under software control. The microcomputer provides digital and/or tone Channel Guard with Squelch Tail Elimination (STE).

If the radio is in the receive mode, the Channel Guard tone/code is hard limited and inputted into the microcomputer through IC702-29 (LIM CG Tone Decode). If the correct tone code is present, the receiver is opened by the RX MUTE line. If the radio is in the transmit mode, the microcomputer generates the Channel Guard tone using WALSH BIT 1 and WALSH BIT 2. Those outputs are summed together and filtered on the System Control board to generate a smooth sinewave for tone Channel Guard or a digital waveform for digital Channel Guard.

The Channel Guard contains a summing amplifier IC604-A 8-pole active voice reject filter HC604 limiter IC604-C and tone/code reject filter HC603. A Channel Guard disable circuit TR606 allows the Channel Guard encode to be disabled. The Channel Guard decoder can be disabled at the microcomputer.

The microcomputer selects the assigned Channel Guard encode code/tone information from the EEPROM memory for each channel, transmit and receive, and generates the Channel Guard signal.

The output of audio preamplifier IC603-A is applied to the summing amplifier through bilateral switches IC601-C and D. In the encode mode DPTT is high applying A- from IC601-D to the control input of IC601-C turning it off and preventing any input from the output of audio preamplifier IC603-A from interfering with the encoding signal.

The output of summing amplifier IC604-A is applied to buffer/amplifier IC604-B through a two-pole active voice reject filter HC604. The active filter shunts all frequencies above 300 Hz to ground, thereby preventing those frequencies from interfering with the encoded signal. The output of IC604-B is the assigned CG tone or digital signal. This signal is applied to the REF MOD line through CG deviation control RV604 and IC609. Channel Guard deviation is set for 0.75 kHz.

In the decode mode DPTT is low, turning bilateral switch IC601-D off, allowing the 9 V filtered supply to turn IC601-C on. The output of audio preamplifier IC603-A is then applied to the summing amplifier IC604-A through bilateral switch IC601-C. This signal is amplified and filtered by IC604A,B and HC604, so that only the CG signal (if present) is applied to hard limiter IC604-C. The CG signal is squared up for comparison by the microcomputer to determine if the CG signal is correct. If the microcomputer determines the CG signal to be correct, RX Mute transistor TR713, is turned off, applying +9 VDC to the RX MUTE line to open the receiver.

The Channel Guard Disable(CG DSBL) line has a double function. It can disable the encode or the decode CG function. The encode function is disabled by applying +19 V or more to J701-2. This will turn on TR606 and shunt the Channel Guard tone/code to ground while the decode function is disabled within the microcomputer software. To disable the decoder, ground the CG DSBL line at J701-2. The microcomputer will detect that the line is low, turn off TR713 and force the RX MUTE line high. The decode filter/limiter circuit is not affected, it continues to operate. The detection software also does not stop working. This allows the off-hook STE to function. When the CG DSBL line is pulled high (9.0 VDC) the microcomputer does not sense any changes. It is buffered by protection diode CD710. Channel Guard disable transistor TR606 will turn on when the CG DSBL line goes above 17 V and shorts the output of the filter to ground. This will prevent any signal from going out on CG HI and will also disable the decoder since no limited CG tone will

go to the microcomputer. The receiver will be muted since no CG is decoded. Disabling the decoder this way will never allow the audio to open up, while taking the radio off hook (pulling $\overline{\text{CG DSBL}}$ low) will always make the radio open up. Turning CG Disable transistor TR606 on causes the DC bias to change. It will take 2 or 3 seconds for the bias to restore itself after the encoder is disabled.

The Squelch Tail Elimination (STE) eliminates squelch tails when the radio is on-hook or off-hook. When Channel Guard is disabled (off-hook), the decoder is still looking at the received signal. The $\overline{\text{RX MUTE}}$ line is high, as would normally be expected. The Channel Guard decoder is looking for the STE burst (phase reversal in tone Channel Guard, STE tone in Digital Channel Guard). If an STE burst is detected, the $\overline{\text{RX MUTE}}$ line will go low for about 200 ms. This will prevent the squelch tail from being heard. After 200 ms, the $\overline{\text{RX MUTE}}$ line will go high again; by now the transmission has ended and the squelch will hold the audio closed. The off-hook STE does not affect the operation of the Channel Guard while on-hook. Another way of looking at it: the radio will go quiet for 200 ms any time STE is detected. If it was on-hook it will stay quiet after the 200 ms, if it was off-hook it will revert to noise squelch operation.

In some instances it is necesssary to invert the polarity of the digital Channel Guard signal to enhance system compatability. Inverted polarity normally results in a wrong code or one that cannot be used. When this occurs, move P603 connected between J604-2, 3 to J603-2,3. The encode DCG codes may be inverted by reprogramming the EEPROM.

FREQUENCY SYNTHESIZER BOARD

The frequency synthesizer receives clock, data, and control information from the microcomputer and from this generates the Tx/Rx RF frequencies. It also provides frequency lock status to the microcomputer. It consists of synthesizer chip IC201, low- and high-current buffers, loop filter, Tx & Rx voltage-controlled oscillators (VCO's), feedback amplifiers, the dual- modulus prescaler, and the reference oscillator. The VCO's are locked to the reference oscillator by a single direct-divide synthesis loop consisting of the feedback buffer, prescaler, and synthesizer. The TX VCO operates over a frequency range of 29 MHz to 50 MHz. The RX VCO operates over the range 49.8 to 70.8 MHz.

REFERENCE OSCILLATOR

The TCXO is enclosed in an RF of a 5 PPM TCXO (Temperature Compensated Crystal Oscillator). The standard reference oscillator frequency is 13.2 MHz.

The TCXO is enclosed in an RF shielded can. Access to the oscillator trimmer is made through a hole in the top of the can. The TCXO is compensated by an internal temperature-compensator circuit for both low and high temperatures. With no additional compensation the oscillators will provide 5 PPM stability from -30°C to +60°C.

CAUTION

TCXOs are individually compensated at the factory and cannot be repaired in the field. Any attempt to repair or change the frequency of a TCXO will void the warranty.

SYNTHESIZER

Synthesizer IC201 contains a programmable reference oscillator divider (÷ R), phase detector, and programmable VCO dividers (÷N, A). The reference frequency, 13.2 MHz from the reference oscillator is divided by a fixed integer number to obtain a 5 kHz channel reference for the synthesizer.
This divide value can be changed by PROM programming. The internal phase detector compares the output of the reference divider with the output of the internal ÷N, A counter. The ÷N, A counter receives as its input the VCO frequency divided by the dual-modulus prescaler and programmed by the microcomputer. This comparison results in a ± error voltage when the phases differ and a constant output voltage when the phase-detector inputs compare in frequency and phase.

If a phase error is detected an error voltage is developed and applied to the VCO DC offset and high current buffers and loop-filter to reset the VCO frequency. The count of the ÷N, A counters is controlled by the frequency data received on the clock and data lines from the microcomputer. Thus, when a different channel is selected or when changing to the transmit or receive mode an error voltage is generated and appears at the phase-detector output, APD OUT causing the phase-locked loop to acquire the new frequency.

The enable pulse from the microcomputer enables the synthesizer and allows frequency data to be internally stored.

EQUALIZER

The equalizer consisting of IC209-A, R216, R219 and C2120 receives transmit audio from Loop Mod adjuster RV201. The output of the equalizer is summed with the output signal from the phase detector by adder IC209-B.

DC OFFSET AND HIGH CURRENT BUFFERS

DC offset buffer TR201, TR205 and diode CD202 receive the error voltage from the synthesizer and increase this level by 1.8 VDC to extend the operating range of the high-current buffers. When the PLL is off-frequency due to a channel change or frequency drift, the error voltage from the synthesizer(APD) rises or falls, turning TR201 either on or off. This transistor TR201 controls the DC offset buffer TR205. R207, CD202 and TR205 complete a high-current rapid-charge or -discharge path for C207-C209.

As the error voltage decreases, TR201, TR205 and CD202 turn on completing a discharge path for C207 to C209. When the error voltage goes positive TR201, TR205 and CD202 are turned off, allowing C207 to C209 to charge through R207. IC204 is turned on for four milliseconds when a channel is changed in receive. The time is 20 milliseconds when in transmit and when changing from transmit to receive.

LOOP FILTER

The loop-filter consists of R209-R211, and C207-209. This filter controls the bandwidth and stability of the synthesizer loop. Bilateral switch IC204 is controlled by the 4 millisecond, 9 volt channel-change pulse. When the channel-change pulse is present, the bilateral switch shorts out the low-pass filter, greatly increasing the loop bandwidth to achieve the 4-millisecond channel acquisition time required for dual priority scan. The low-pass filter removes noise and other extraneous signals internal to the synthesizer chip.

The output of the filter is applied to the varicaps in the transmit and receive VCO's to adjust and maintain the VCO frequency.

The use of two VCO's allows rapid independent selection of transmit and receive frequencies across the frequency split.

RECEIVER VOLTAGE CONTROLLED OSCILLATOR

The receiver VCO consists of a low-noise JFET oscillator, TR210, followed by high-gain buffer TR211. TR211 prevents external loading and provides power gain. The VCO is a Colpitts oscillator with the various varactors, capacitors and coil forming the tank circuit.

The VCO is switched on and off under control of the DPTT line. When the DPTT line is low, the Receiver VCO is turned on (TR213 is off, TR212 is on). Oscillator output is typically +10 dBm. The output is applied to the feedback buffer for VCO frequency control and as the Rx/Ex injection frequency to the receiver 1st mixer through L.O. buffers TR402, TR403 on the RX board. The Rx VCO also uses a high-Q resonator coil to achieve superior noise performance. The VCO operates over a frequency range of 49.8 to 70.8 MHz. The VCO voltage need only be set once at the highest frequency of the band split, after which it will operate over the entire split with no more tuning.

TRANMITTER VOLTAGE CONTROLLED OSCILLATOR

The transmit VCO is basically the same as the receiver VCO. The wideband VCO allows frequency separation of 13 MHz or 15 MHz as determined by the bandsplit the radio is operating on, 29-42 MHz or 35-50 MHz. The varactors in conjunction with the frequency segment selector circuitry (TR216 - TR219, TR227, TR228, TR230 and pin diodes CD217, CD218 and CD221) provide a voltage-controlled adjustment range that extends across the entire frequency split.

VCO control switch TR222 turns the Transmit VCO on when DPTT is high.

FEEDBACK BUFFER

The buffered outputs of the Rx VCO and Tx VCO, from TR211 and TR221 respectively, are supplied to the feedback buffer amplifiers TR206 and TR207. This, in turn drives the dual-modulus prescaler IC202. The buffered VCO outputs also drive the synthesizer output buffer IC208, which provides the common Receiver/Exciter Injection drive.

DUAL-MODULUS PRESCALER

The dual-modulus prescaler completes the PLL feedback path from the synthesizer to loop filter, to the VCO's and feedback buffers and then back to the synthesizer through the prescaler. The prescaler divides the VCO frequency by 64 or 65 under control of M CONT from the synthesizer. The output of the prescaler is applied to the synthesizer where it is divided down to 5 kHz by an internal ÷ N, A counter and compared in frequency and phase with the divided-down frequency from the reference oscillator. The result of this comparison is the error voltage used to maintain frequency lock. The ÷ N, a counter is controlled by data received from the microcomputer. Depending on the operating frequency, the DC voltage at TP201 should be within the range 3.5 to 7.5 VDC when the PLL is locked.

LOCK DETECT

The lock-detect circuit consists of comparator IC203, diodes CD203 and CD204, and reference oscillator mute switch TR208 and TR209. It is used to quickly synchronize the phase relation of the divided-down VCO frequency and the reference oscillator if the loop loses lock. It also provides a fast lock-detect signal to the microcomputer to turn on the out-of-lock indicator. If a large change in frequency is required, the ramp capacitor output (C_R) of the synthesizer may increase to near 7.5 VDC and cause the comparator output to decrease. This decrease in voltage turns TR209 off and allows TR208 to be turned on by the

positive LD line from the synthesizer. Thus TR208 disables the reference oscillator and allows the PLL loop to be brought back to synchronization rapidly.

If a large frequency error exists, the LD positive lead from the synthesizer will carry negative spikes to the microcomputer through CD204 to activate the lock indicator circuit. Pulse shaper IC701 is a one-shot multivibrator which increases the pulse width to span 1 computer cycle. TR209 is turned on, keeping TR208 off thereby preventing TR208 from muting the reference oscillator.

MODULATION LEVEL CONTROL

The modulation level control circuit automatically sets the Tx audio level applied to the transmit VCO modulator CD212 through VCO deviation adjust control RV202. The modulation level control circuit consists of IC205, R274 - R282, varactor CD212, C245 and bypass capacitors C247 and C248. The modulation level is controlled by turning bilateral switches IC205 on or off (under control of IC705) to include attenuators R275, R276 and R281 in the circuit. R274, R275, R276 and R281 form an adjustable voltage divider to change the modulation level as required. Table 1 also identifies the resistor (if applicable) used for each frequency segment.

FREQUENCY SEGMENT SELECTOR

The frequency-segment selector switches capacitance in and out of the Tx and Rx VCO tank circuits to select the frequency segment containing the selected channel. The frequency segment selector consists of TR216 - TR219, TR227, TR228, TR230, CD209, CD210, CD217, CD218, CD220 and CD221 and operates under control of the microcomputer through FF's IC705A & B. Capacitors (C224, C227, C252, C255, C291 and C294) are selected or deselected for operation in a given segment. Table 4 identifies the circuit conditions existing for selection of each segment and the capacitors used.

Reverse bias to turn off the pin-diodes is provided by the +8 V filtered supply through R232, R234 and R286. Forward bias for the diodes and current for the switching transistors are provided by the +8 V supply though R231, R233 and R285. When segment 3 is selected, TR216, TR219 and TR227 are turned on. In the Tx VCO diodes CD217 and CD221 are reverse biased and CD218 is turned on. Capacitors C251 and C293 are effectively isolated from ground by L218 and L225 respectively and C254 is connected to ground via CD218 and TR219.

Similarly in the RX VCO C223 and C290 are isolated from ground, and C226 is grounded via CD210 and TR219.

Operation of the radio over the frequency ranges 29-42 MHz or 35-50 MHz is determined by the group number of the synthesizer board. Each frequency split is divided into four operating segments varying from 3 to 4 MHz wide.

SEGMENT	TRANSISTOR SWITCH*							PIN DIOES						GROUNDED CAPACITORS
	TR216	TR217	TR218	TR219	TR227	TR228	TR230	CD209	CD210	CD217	CD218	CD220	CD221	
1	0	1	0	1	0	1	1	ON	ON	ON	ON	ON	ON	ALL
2	0	1	1	0	1	0	0	ON	OFF	ON	OFF	OFF	OFF	C223 C251
3	1	0	0	1	1	0	0	OFF	ON	OFF	ON	OFF	OFF	C226 C254
4	1	0	1	0	1	0	0	OFF	OFF	OFF	OFF	OFF	OFF	NONE

* '1' indicates transistor is turned on.

TABLE 4 - Capacitor Selection

PA BOARD

The four power amplifiers covering the frequency ranges of 29-42 MHz and 35-50 MHz and power levels of 60 W and 110 W, are very similar in construction and operation. The only differeces are in the transistor types and some component values. The following description applies to all four versions.

The PA assembly uses a driver and three RF power transistors to provide rated output power. The output power is adjustable over a range of 55 to 110 watts and 30 to 60 watts for the two power versions. Five transistors are used in the power control circuit.

Supply voltage for the PA is provided by power leads from the System Interface Board to J3 (A+) and (A-) on the PA board. Diode CD11 will cause the main fuse in the fuse assembly to blow if the polarity of the power leads is reversed. CD10 is a surge protector to suppress voltage surges on the power leads.

RF AMPLIFIERS

The Exciter output is coupled through coaxial cable P1 to the PA input. The RF is coupled through an attenuator pad (R1-R3), impedance matching transformer T1 and frequency compensator C2 and R4 to the base of pre-driver TR1. L1, CD1, and R6 set the bias voltage for TR1. C3, R6 and R36 provide negative feedback to improve the stability of TR1. Collector voltage on pre-driver TR1 is controlled by the Power Control Circuit and is applied trough a decoupling network which consists of C5, C6 and C58.

The output of TR1 is coupled to the base of amplifier TR2 through impedance-matching transformer T2 and frequency compensator C8, R34 and R35. C7 provide matching between T2 and the base of TR2. C11 and R9 provide negative feedback and R8 improves the stability of TR2.

Collector voltage to driver TR2 is supplied through a decoupling network consisting of C13 to C15 and L13.

The RF output from TR2 passes through impedance-matching transformer T3 and matching element C12. (Note: This is a 50 ohm point and may be used for checking power levels). From C16, RF passes through stabilizing resistors R10 and R11 and matching element C17 to input of 4:1 transformer T4.

The Power Amplifier, consisting of TR3, TR4, T4 and T5 is a class-C push-pull power amplifier. T4 provides impedance-matching and power splitting to the bases of TR3 and TR4. C18 and C19 provide matching elements to T4. R12 and R13 provide the base loading to TR3 and TR4. C21, C24, R14 and R15 are negative feedback elements to improve the stability of TR3 and TR4, T5 provides impedance-matching and power combining for the collectors of TR3 and TR4. C26 and C27 provide matching elements to T4. C22 and C23 provide matching elements to the collector of TR3 and TR4.

Operating voltage for the power amplifier is supplied from the DC input through T5 and decoupling network consisting of C28 to C30 and L2.

The output of the power amplifier passes through T5 to the LPF network consisting of C31 to C33 and L4. (Note: This is a 50 ohm point and may be used for checking power levels.) The RF power passes through 50 ohm microstrip Z2 and Z3, directional coupler T6 and associated components and transmit/receive relay K1 to the low-pass filter.

The relay is energized by D9V from the System Control Receiver/Exciter Board.

POWER CONTROL CIRCUIT

The power control circuit provides closed-loop RF power leveling and power turndown when it senses high VSWR load conditions.

When the transmitter is keyed, TX9V turns on and supplies current to DC Amplifier, which provides a constant control reference voltage.

TR5 to TR8 serve as DC amplifiers to supply voltage to the collector of TR1. The setting of RV1 determines the current supplied to the base of TR5. As the detected RF power increases, the current to the base of TR5 increases causing TR5 to pull current away from the base of TR8. This cuts back the drive to TR8 and in turn TR7, which reduces the voltage at the collector of TR1, decreasing RF output power.

RF power is sensed by directional coupler T6 and its associated elements. Forward power is sensed by CD3 and reflected power by CD2. Forward power is determined by the setting of RV1. CD4 to CD7 set the level of reflected RF power at which the control circuit reduces the RF output.

Thermal protection is provided by R30 (posistor) and its associated elements. R30 is thermally connected to the body of TR4. As the temperature of TR4 rises above 90°C, the resistance of R30 increases, and TR6 turns ON. This diverts emitter current from TR5 to R25, which lowers the voltage at the collector of TR1, reducing the power output.

CAUTION

Do not operate the transmitter at levels higher than rated output. Operating at higher than rated output will shorten the life of the RF power transistors.

RECEIVER/EXCITER BOARD

EXCITER CIRCUIT

The Exciter consists of a broadband negative feedback amplifier stage operating over a frequency range of 29-50 MHz.

An attenuator pad R138 and R139 at the input of the exciter provides a constant load for the injection amplifier and attenuates the signal from the injection amplifier to approximately +13 dBm. The exciter amplifies the +13 dBm signal from the injection amplifier to provide 100 mW to the power amplifier.

The Tx injection signal input from the injection amplifier is applied to the base of amplifier TR104 through an attenuator pad and impedance matching components L117 and C169. The impedance matching network matches the injection amplifier output to the base of TR104. R140, R141 and CD105 set the bias voltage for the TR104. C172 provides noise decoupling. L117 consists of broadband transformer (4:1 impedance ratio). R142 and C170 provide negative feedback to improve the stability of TR104.

The 100 mW output of TR104 is coupled to the power amplifier board through low-pass filter consisting of C174, C175, C176, L119 and output connector J102. Collector voltage for TR104 is supplied by Tx 9 V through Tx switch TR107. +9 V is regulated from the A+ to 9 VDC by IC502. When $\overline{\text{TX ENBL}}$ goes high (receive mode) TR107 is turned off.

Service Note

The output RF level can be measured by connecting a 50-ohm dummy load to J102, feeding a +3 dBm signal to P402 (135-174 MHz) and grounding the $\overline{\text{TX ENBL}}$ line.

RECEIVER CIRCUIT

The FM dual-conversion, superheterodyne receiver is designed for operation in the 29-42/35-50 MHz frequency ranges. A regulated 9.0 volts is provided to all receiver stages except the audio PA IC, which operates from the switched A+ supply.

The receiver has intermediate frequencies of 20.8 MHz and 455 kHz. Adjacent channel selectivity is obtained by using two band-pass filters: a 20.8 MHz crystal filter and a 455 kHz ceramic filter.

All of the receiver circuitry except the synthesizer, audio preamp, audio PA, and squelch circuit is mounted on the Receiver/Exciter board. The receiver consists of:

- Front End and Mixer
- 20.8 MHz 1st IF, 455 kHz 2nd IF and FM Detector
- Audio PA
- Squelch

RECEIVER FRONT END

An RF signal from the antenna is coupled through the low-pass filter, antenna relay, and band-pass filter to the input of RF amplifier TR401. The output of TR401 is coupled through low-pass filter and high-pass filters to the input of 1st mixer HC401. Front-end selectivity is provided by these band-pass, low-pass and high-pass filters.

RECEIVER INJECTION

Receiver RF injection (49.8-62.8 or 55.8-70.8 MHz) from the synthesizer VCO is applied to amplifier TR402 through P402. The input level at P402 will be between 0.5 and 1.0 milliwatts. The output of amplifier TR402 is coupled to the input of amplifier TR403. The output of amplifier TR403 is filtered by a band pass filter. This filter is tuned to pass frequencies in the 49.8-70.8 MHz passband.

1st MIXER

The first mixer is a double-balanced diode mixer (HC401) that converts a signal in 29-42 or 35-50 MHz range to the 20.8 MHz first IF frequency.

In the mixer stage, RF from the front-end RF filter is applied to one input of the mixer. Injection voltage from the amplifier stages is applied to the other input of the mixer. The 20.8 MHz 1st IF output signal is coupled from the output of HC401 through C501 to the source input of IF AMPL TR501. TR501 are a JFET amplifier/buffer stage. The output of the JFET buffer is coupled through C502 to the optional noise blanker (W402 removed) or through impedance matching networks L505, L506 and associated circuitry (bypassing IF blanking FETs TR502 and TR503) to a 4-pole XTAL band-pass filter.

1st IF

The highly-selective Crystal filter consisting of FL501-1 and FL501-2 provides the first portion of the receiver IF selectivity. The output of the filter is coupled through impedance-matching network L507, C514 and C515 to the 1st IF amplifier TR504. The amplifier provides approximately 20 dB of IF gain. The output of TR504 is coupled through an impedance-matching network L508 to a 2-pole XTAL bnad-pass filter. The output of the XTAL band-pass filter is coupled through an impedance matching network L509 to the input of IC501. Diodes CD501 provides limiting for the 20.8 MHz IF signal (1.4Vp-p) to prevent high level overload of IC501.

2nd IF and DETECTOR

IC501 and associated circuitry comprise the 2nd oscillator/mixer, IF amplifier and FM detector. The 20.8 MHz IF input is applied to pin 18 of IC501 and mixed with a 20.345 MHz frequency supplied by crystal oscillator X501. Low-side injection is used. The output of the internal mixer is amplified and applied to a 6-pole ceramic filter, FL503 which provides the 455 kHz selectivity. The output of the 455 kHz filter is reapplied to IC501-5. The 2nd IF signal is amplified and limited. L510 shifts the IF signal by 90° and reapplies it to the internal FM detector. The FM detector compares the shifted IF signal to the internal IF signal to recover the audio modulation. The audio output of IC501 is applied to the System Control board.

GE Mobile Communications

General Electric Company
Lynchburg, Virginia 24502

Printed in Japan