dresden elektronik

User Manual
Radio Modules

deRFmega128-22M00
deRFmega128-22M10
deRFmega128-22M12

deRFmega256-23M00
deRFmega256-23M10
deRFmega256-23M12

Document Version V1.3
2013-06-10

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Document history

Date	Version	Description
2012-10-15	1.0	Initial version
2012-11-30	1.1	Update technical data • TX_PWR register settings • Sensitivity Update signal description
2013-01-22	1.2	RFOUT pin description on deRFmega128-22M12 more precisely specified Update duty cycle limit Addition of deRFmega256-23M00, -23M10, -23M12
2013-06-10	1.3	Update duty cycle requirements Addition of reference design for deRFmega256-23M12 Update FCC section

Abbreviations

Abbreviation	Description
IEEE 802.15.4	IEEE 802.15.4 standard, applicable to low-rate Wireless Personal Area Networks (WPAN)
6LoWPAN	IPv6 over Low Power Wireless Personal Area Networks
ADC	Analog to Digital Converter
CE	Consumer Electronics
EMI	Electromagnetic Interference
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
GPIO	Generals Purpose Input Output
JTAG	Joint Test Action Group, digital interface for debugging of embedded devices, also known as IEEE 1149.1 standard interface
ISA SP100	International Society of Automation, the Committee establishes standards and related technical information for implementing wireless systems.
ISP	In-System-Programming
LGA	Land Grid Array, a type of surface-mount packaging for integrated circuits
LNA	Low Noise Amplifier
MAC	Medium (Media) Access Control
MCU, µC	Microcontroller Unit
PA	Power Amplifier
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RF	Radio Frequency
R&TTE	Radio and Telecommunications Terminal Equipment (Directive of the European Union)
SPI	Serial Peripheral Interface
TWI	Two-Wire Serial Interface
U[S]ART	Universal [Synchronous/]Asynchronous Receiver Transmitter
USB	Universal Serial Bus
ZigBee	Low-cost, low-power wireless mesh network standard. The ZigBee Alliance is a group of companies that maintain and publish the ZigBee standard.

1. Overview

The tiny radio module series by dresden elektronik combines Atmel's 8-bit AVR single chip ATmega128RFA1 and ATmega256RFR2 with a small footprint. Six different module types are available providing different features for the custom application.

The deRFmega128-22M00 and deRFmega256-23M00 have an onboard chip antenna to establish a ready-to-use device. No additional and expensive RF designs are necessary. This module is full compliant to all EU and US regulatory requirements.

The deRFmega128-22M10 and deRFmega256-23M10 have the smallest form factor of all module types. The customer is free to design his own antenna, coaxial output or front-end; but it is also possible to use one of the dresden elektronik's certified and documented RF designs.

The deRFmega128-22M12 and deRFmega256-23M12 have an onboard front-end feature including LNA and PA with 20 dB gain. Furthermore it supports antenna diversity by a direct connection of two antennas or coaxial connectors. All necessary RF parts and switches are integrated. This module type combined with the small form factor is the optimal solution between range extension and space for mounting on PCB.

2. Applications

The main applications for the radio modules are:

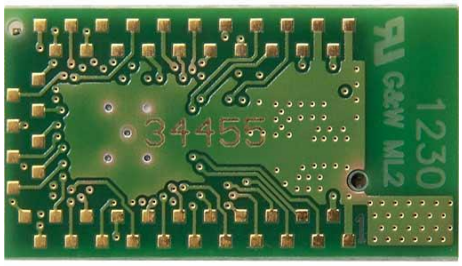
- 2.4 GHz IEEE 802.15.4
- ZigBee PRO
- ZigBee RF4CE
- ZigBee IP
- 6LoWPAN
- ISA SP100
- Wireless Sensor Networks
- Industrial and home controlling/monitoring
- Smart Metering

3. Features

3.1. deRFmega128-22M00

The radio module deRFmega128-22M00 offers the following features:

- Tiny size: 23.6 x 13.2 x 3.0 mm
- 51 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Onboard 32.768 kHz crystal (Deep-Sleep clock) and
- 16 MHz crystal



- Application interfaces:
  2x UART, 1x TWI, 1x ADC
- GPIO interface
- Debug/Programming interfaces:
  1x SPI, 1x JTAG, 1x ISP
- Onboard 2.4 GHz chip antenna
- Certification: CE, FCC

Figure 1 shows the block diagram of the radio module deRFmega128-22M00.

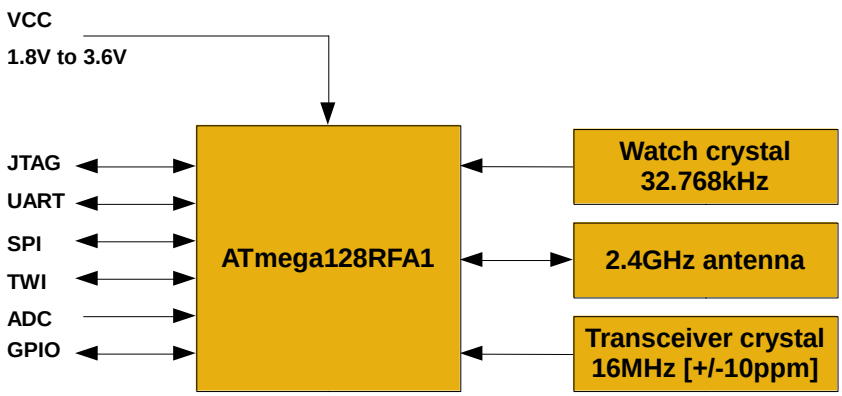
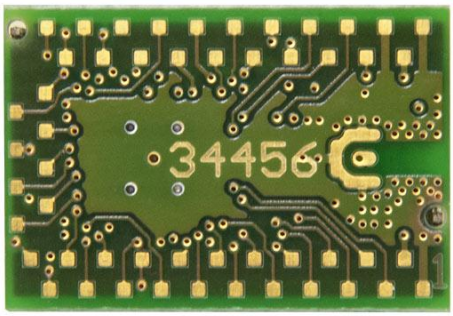


Figure 1: Block diagram deRFmega128-22M00

3.2. deRFmega128-22M10

The radio module deRFmega128-22M10 offers the following features:

- Tiny size: 19.0 x 13.2 x 3.0 mm
- 55 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Onboard 32.768 kHz crystal (Deep-Sleep clock) and
- 16 MHz crystal



- Application interfaces:
  2x UART, 1x TWI, 1x ADC
- GPIO interface
- Debug/Programming interfaces:
  1x SPI, 1x JTAG, 1x ISP
- Solderable 2.4 GHz RF output pads (1x RFOUT, 3x RFGND)
- Certification: CE, FCC pending

Figure 2 shows the block diagram of the radio module deRFmega128-22M10.

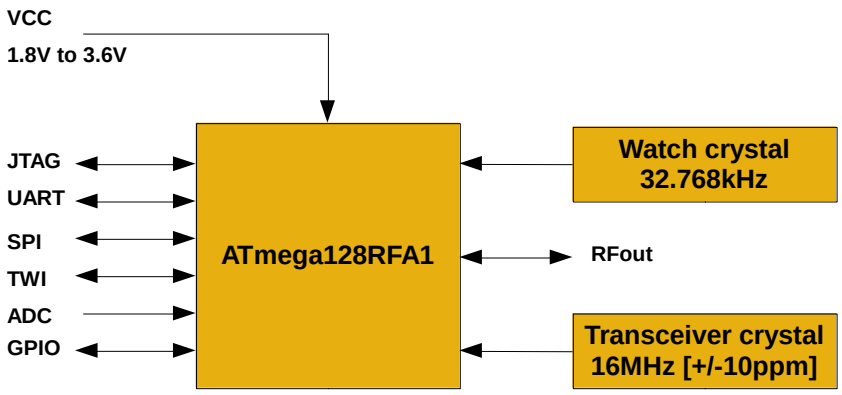
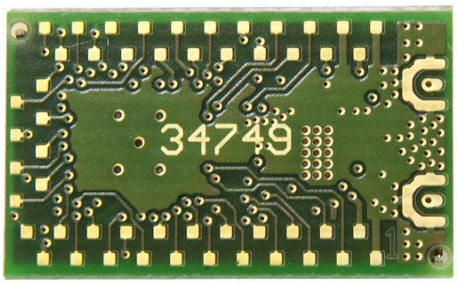


Figure 2: Block diagram deRFmega128-22M10

3.3. deRFmega128-22M12

The radio module deRFmega128-22M12 offers the following features:

- Tiny size: 21.5 x 13.2 x 3.0 mm
- 59 LGA pads 0.6 x 0.6 mm
- Supply voltage 2.0 V to 3.6 V
- Antenna diversity support
- RF shielding
- Onboard 32.768 kHz crystal (Deep-Sleep clock) and
- 16 MHz crystal



- Application interfaces: 2x UART, 1x TWI
- GPIO interface
- Debug/Programming interfaces: 1x SPI, 1x JTAG, 1x ISP
- 2.4 GHz front-end module with internal 20 dB PA and LNA
- Solderable 2.4 GHz RF output pad (2x RFOUT, 6x RFGND)
- Certification: CE, FCC pending

Figure 3 shows the block diagram of the radio module deRFmega128-22M12.

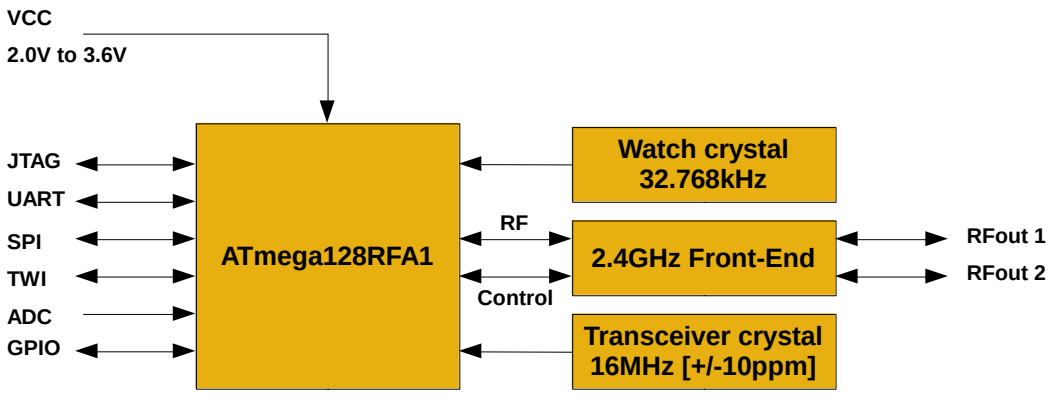
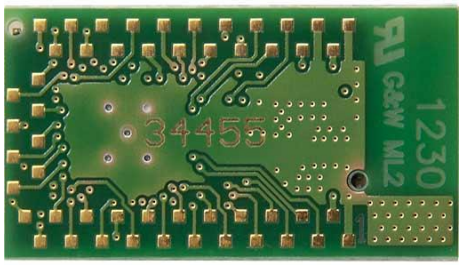


Figure 3: Block diagram deRFmega128-22M12

3.4. deRFmega256-23M00

The radio module deRFmega256-23M00 offers the following features:

- Tiny size: 23.6 x 13.2 x 3.0 mm
- 51 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Onboard 32.768 kHz crystal (Deep-Sleep clock) and
- 16 MHz crystal



- Application interfaces:
  2x UART, 1x TWI, 1x ADC
- GPIO interface
- Debug/Programming interfaces:
  1x SPI, 1x JTAG, 1x ISP
- Onboard 2.4 GHz chip antenna
- Certification: CE, FCC pending

Figure 4 shows the block diagram of the radio module deRFmega256-23M00.

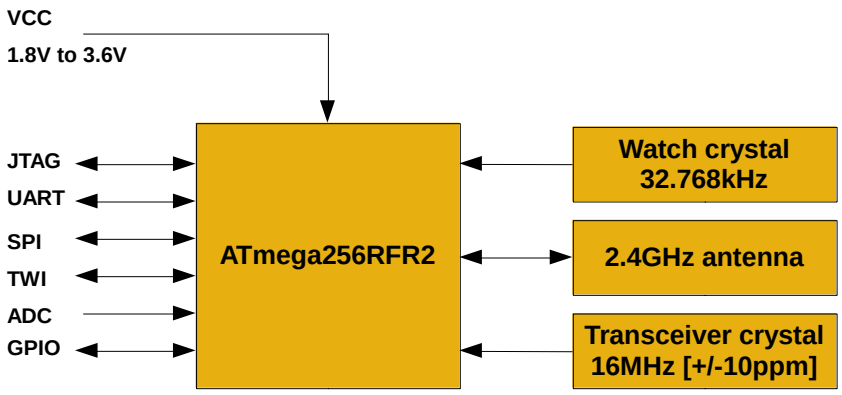
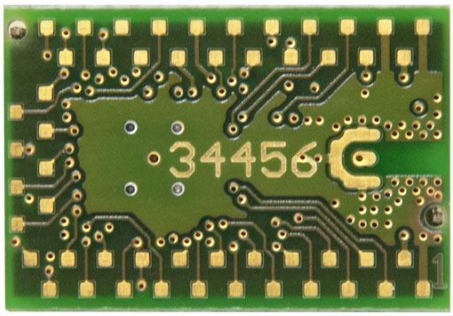


Figure 4: Block diagram deRFmega256-23M00

3.5. deRFmega256-23M10

The radio module deRFmega256-23M10 offers the following features:

- Tiny size: 19.0 x 13.2 x 3.0 mm
- 55 LGA pads 0.6 x 0.6 mm
- Supply voltage 1.8 V to 3.6 V
- RF shielding
- Onboard 32.768 kHz crystal (Deep-Sleep clock) and
- 16 MHz crystal



- Application interfaces:
  2x UART, 1x TWI, 1x ADC
- GPIO interface
- Debug/Programming interfaces:
  1x SPI, 1x JTAG, 1x ISP
- Solderable 2.4 GHz RF output pads (1x RFOUT, 3x RFGND)
- Certification: CE, FCC pending

Figure 5 shows the block diagram of the radio module deRFmega256-23M10.

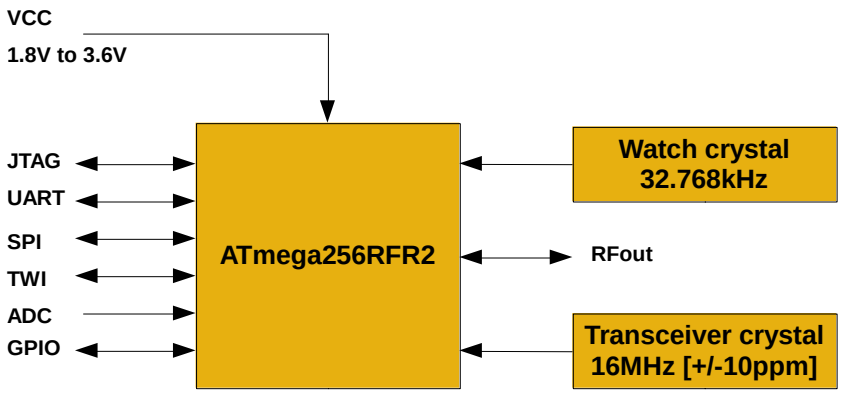
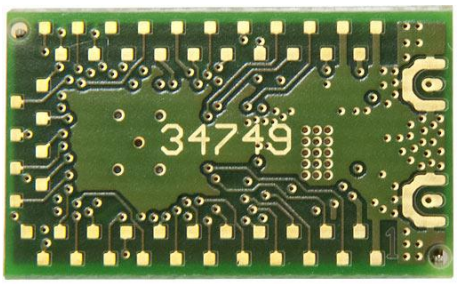


Figure 5: Block diagram deRFmega256-23M10

3.6. deRFmega256-23M12

The radio module deRFmega256-23M12 offers the following features:

- Tiny size: 21.5 x 13.2 x 3.0 mm
- 59 LGA pads 0.6 x 0.6 mm
- Supply voltage 2.0 V to 3.6 V
- Antenna diversity support
- RF shielding
- Onboard 32.768 kHz crystal (Deep-Sleep clock) and
- 16 MHz crystal



- Application interfaces: 2x UART, 1x TWI
- GPIO interface
- Debug/Programming interfaces: 1x SPI, 1x JTAG, 1x ISP
- 2.4 GHz front-end module with internal 20 dB PA and LNA
- Solderable 2.4 GHz RF output pad (2x RFOUT, 6x RFGND)
- Certification: CE, FCC pending

Figure 6 shows the block diagram of the radio module deRFmega256-23M12.

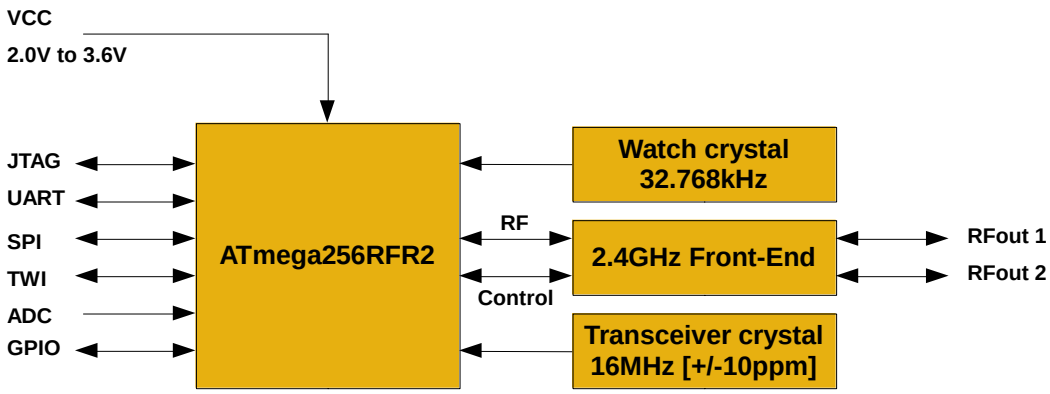


Figure 6: Block diagram deRFmega256-23M12

4. Technical data

Table 4-1: Mechanical data

Mechanical	
Radio modules	
Size (L x W x H)	23.6 x 13.2 x 3.0 mm (for 22M00 and 23M00)
	19.0 x 13.2 x 3.0 mm (for 22M10 and 23M10)
	21.5 x 13.2 x 3.0 mm (for 22M12 and 23M12)
Pads	
Type	LGA
Pitch	1.60 mm
Pad size	0.6 x 0.6 mm

Table 4-2: Temperature range

Temperature range					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Operating temperature range	T_{work}	-40		+85	°C
Humidity		25		80	% r.H.
Storage temperature range	$T_{storage}$	-40		+125	°C

Table 4-3: Electrical characteristics for deRFmega128 series

Electrical characteristics					
deRFmega128-22M00 and deRFmega128-22M10					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage	VCC	1.8	3.3	3.6	V
Current consumption	I_{TXon} (TX_PWR = +3 dBm)	17.8	18.1	18.2	mA
	I_{Txon} (TX_PWR = 0 dBm)	16.2	16.4	16.5	mA
	I_{Txon} (TX_PWR = -17 dBm)	12.5	12.7	12.7	mA
	I_{RXon}	17.5	17.6	17.7	mA
	I_{Idle} (Txoff, MCK = 8MHz)	4.7	4.8	4.8	mA
	I_{Sleep} (depends on Sleep Mode)		<1		µA

deRFmega128-22M12					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage	VCC	2.0	3.3	3.6	V
Current consumption	I_{TXon} (TX_PWR = +20 dBm)	119.4	197.7	205.2	mA
	I_{TXon} (TX_PWR = +4 dBm)	27.0	46.1	46.7	mA
	I_{RXon}	19.8	22.5	22.8	mA
	I_{Idle} (Txoff, MCK = 8 MHz)	5.2	5.4	5.6	mA
	I_{Sleep} (depends on Sleep Mode)		<1		µA

Table 4-4: Electrical characteristics for deRFmega256 series

Electrical					
deRFmega256-23M00 and deRFmega256-23M10					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage	VCC	1.8	3.3	3.6	V
Current consumption	I_{TXon} (TX_PWR = +3.5 dBm)	18.2	18.8	19.1	mA
	I_{TXon} (TX_PWR = +0.5 dBm)	16.3	16.5	16.7	mA
	I_{TXon} (TX_PWR = -16.5 dBm)	11.2	11.8	12.1	mA
	I_{RXon}	15.9	16.3	16.5	mA
	I_{RXon} (RPC mode)	10.4	10.7	11.0	mA
	I_{Idle} (Txoff, MCK = 8MHz)	4.3	4.8	5.1	mA
	I_{Sleep} (depends on Sleep Mode)		<2		µA
deRFmega256-23M12					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage	VCC	2.0	3.3	3.6	V
Current consumption	I_{TXon} (TX_PWR = +20 dBm)	139.6	232.5	243.5	mA
	I_{TXon} (TX_PWR = +4 dBm)	27.7	48.8	49.7	mA
	I_{RXon}	19.0	22.4	22.3	mA
	I_{RXon} (RPC mode)	13.5	16.7	18.0	mA
	I_{Idle} (Txoff, MCK = 8 MHz)	4.6	5.1	5.4	mA
	I_{Sleep} (depends on Sleep Mode)		<2		µA

Table 4-5: Quartz crystal properties

Quartz crystal					
	Parameter	*Min*	*Typ*	*Max*	*Unit*
Watch crystal	Frequency		32.768		kHz
	Frequency tolerance		+/-20		ppm
Transceiver crystal	Frequency		16.000		MHz
	Frequency tolerance		+/-10		ppm

Table 4-6: Radio data of deRFmega128-22M00 and deRFmega128-22M10

Radio 2.4 GHz (Supply voltage VCC = 3.3V)					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
Antenna	Type		Chip ceramic		
	Gain		-0.7		dBi
	Diversity		No		
RF Pad	Impedance		50		Ω
Range	Line of sight		TBD		m
Frequency range[1]	PHY_CC_CCA = 0x0B...0x1A	2405		2480	MHz
Channels	PHY_CC_CCA = 0x0B...0x1A		16		
Transmitting power conducted	TX_PWR = 0x00 VCC = 3.3V	2.3		2.9	dBm
Receiver sensitivity	Data Rate = 250 kBit/s Data Rate = 500 kBit/s Data Rate = 1000 kBit/s Data Rate = 2000 kBit/s		-98 -94 -91 >-80		dBm dBm dBm dBm
Data rate (gross)	TRX_CTRL_2 = 0x00 TRX_CTRL_2 = 0x01 TRX_CTRL_2 = 0x02 TRX_CTRL_2 = 0x03		250 500 1000 2000		kBit/s kBit/s kBit/s kBit/s
EVM	conducted	6.5	7.5	10.5	%

[1] Operating the transmitter at channel 11 to 25 requires a duty cycle ≤35% and channel 26 requires a duty cycle ≤15% to fulfil all requirements according to FCC Part 15 Subpart C § 15.209.

Table 4-7: Radio data of deRFmega128-22M12

Radio (Supply voltage VCC = 3.3V)					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
RF pad	Impedance		50		Ω
	Diversity		Yes		
Range			TBD		m
Frequency range		2405		2480	MHz
Channels			16		
Transmitting power conducted[2,3]	TX_PWR = 0x00 VCC = 3.3V	21.4	21.9	22.4	dBm
Receiver sensitivity	Data Rate = 250 kBit/s Data Rate = 500 kBit/s Data Rate = 1000 kBit/s Data Rate = 2000 kBit/s		-105 -100 -98 -91		dBm dBm dBm dBm
Data rate (gross)	TRX_CTRL_2 = 0x00 TRX_CTRL_2 = 0x01 TRX_CTRL_2 = 0x02 TRX_CTRL_2 = 0x03		250 500 1000 2000		kBit/s kBit/s kBit/s kBit/s
EVM	conducted	6.5	7.5	9.5	%

Table 4-8: Radio data of deRFmega256-23M00 and deRFmega256-23M10

Radio 2.4 GHz (Supply voltage VCC = 3.3V)[4]					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
Antenna	Type		Chip ceramic		
	Gain		-0.7		dBi
	Diversity		No		
RF Pad	Impedance		50		Ω
Range	Line of sight		TBD		m
Frequency range[5]	PHY_CC_CCA = 0x0B...0x1A	2405		2480	MHz

[2] Only applicable for EU: The maximum allowed TX_PWR register setting of deRFmega128-22M12 is TX_PWR = 0x0E. According to EN 300 328 clause 4.3.1 the maximum transmit power is restricted to a limit of +10dBm.
[3] Only applicable for US: Operating the transmitter at channel 11, 12, 13, 23, 24, 25 and 26 requires to ensure a reduced output power and/or duty cycle limit to fulfil all requirements according to FCC Part 15 Subpart C § 15.209. See chapter 4.3.
[4] Values are not validated.

	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
Channels	PHY_CC_CCA = 0x0B...0x1A		16		
Transmitting power conducted	TX_PWR = 0x00 VCC = 3.3V	3.6	3.7	3.8	dBm
Receiver sensitivity	Data Rate = 250 kBit/s Data Rate = 500 kBit/s Data Rate = 1000 kBit/s Data Rate = 2000 kBit/s		-99 -95 -93 -87		dBm dBm dBm dBm
Data rate (gross)	TRX_CTRL_2 = 0x00 TRX_CTRL_2 = 0x01 TRX_CTRL_2 = 0x02 TRX_CTRL_2 = 0x03		250 500 1000 2000		kBit/s kBit/s kBit/s kBit/s
EVM	conducted		~8		%

Table 4-9: Radio data of deRFmega256-23M12

Radio (Supply voltage VCC = 3.3V)[6]					
	Parameter / feature	*Min*	*Typ*	*Max*	*Unit*
RF pad	Impedance		50		Ω
	Diversity		Yes		
Range			TBD		m
Frequency range		2405		2480	MHz
Channels			16		
Transmitting power conducted[7,8]	TX_PWR = 0x00 VCC = 3.3V	22.2	22.5	22.8	dBm
Receiver sensitivity	Data Rate = 250 kBit/s Data Rate = 500 kBit/s Data Rate = 1000 kBit/s Data Rate = 2000 kBit/s		-105 -101 -99 -94		dBm dBm dBm dBm

[5] Operating the transmitter at channel 26 requires a duty cycle ≤25% to fulfil all requirements according to FCC Part 15 Subpart C § 15.209.
[6] Values are not validated.
[7] Only applicable for EU: The maximum allowed TX_PWR register setting of deRFmega128-22M12 is TX_PWR = 0x0E. According to EN 300 328 clause 4.3.1 the maximum transmit power is restricted to a limit of +10dBm.
[8] Only applicable for US: Operating the transmitter at channel 11, 12, 13, 23, 24, 25 and 26 requires to ensure a reduced output power and/or duty cycle limit to fulfil all requirements according to FCC Part 15 Subpart C § 15.209. See chapter 4.3.

Data rate (gross)	TRX_CTRL_2 = 0x00 TRX_CTRL_2 = 0x01 TRX_CTRL_2 = 0x02 TRX_CTRL_2 = 0x03		250 500 1000 2000		kBit/s kBit/s kBit/s kBit/s
EVM	conducted		~7		%

4.1. TX Power register settings for deRFmega128-22M00 and 22M10

The diagrams in **Figure 7** and **Figure 8** are showing the current consumption and conducted output power during transmission depending on the TX_PWR register setting. The values are valid for deRFmega128-22M00 and 22M10.

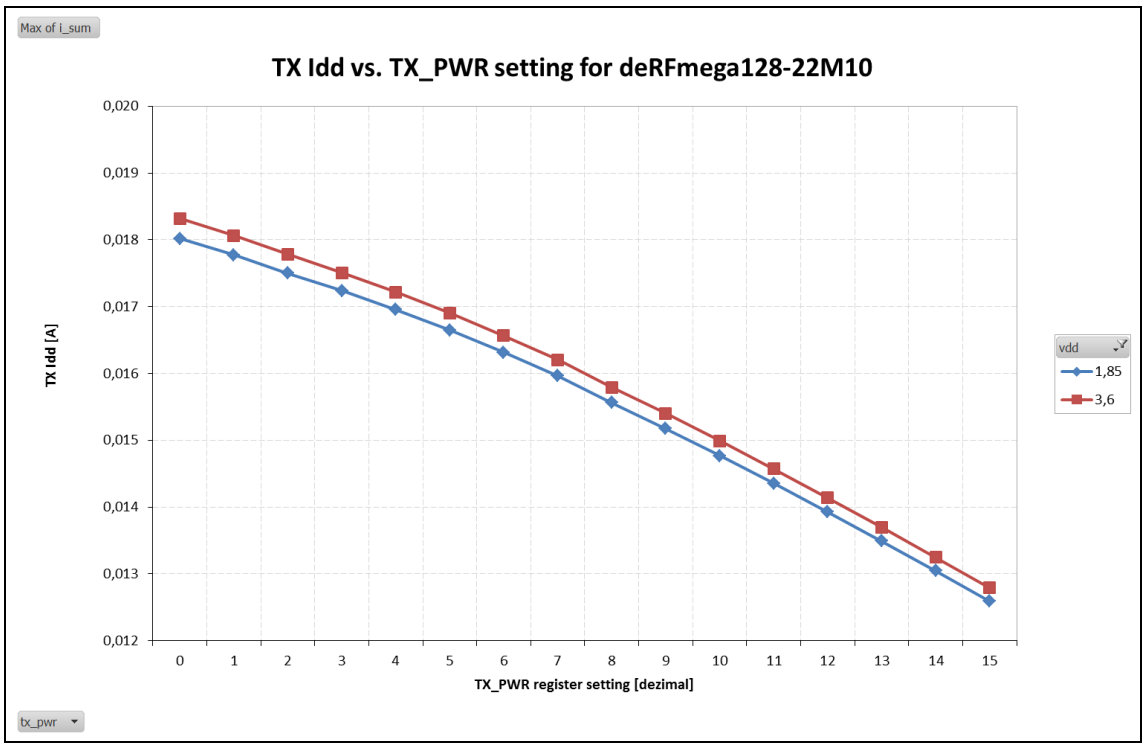


Figure 7: TX Idd vs. TX_PWR for deRFmega128-22M00 / 22M10

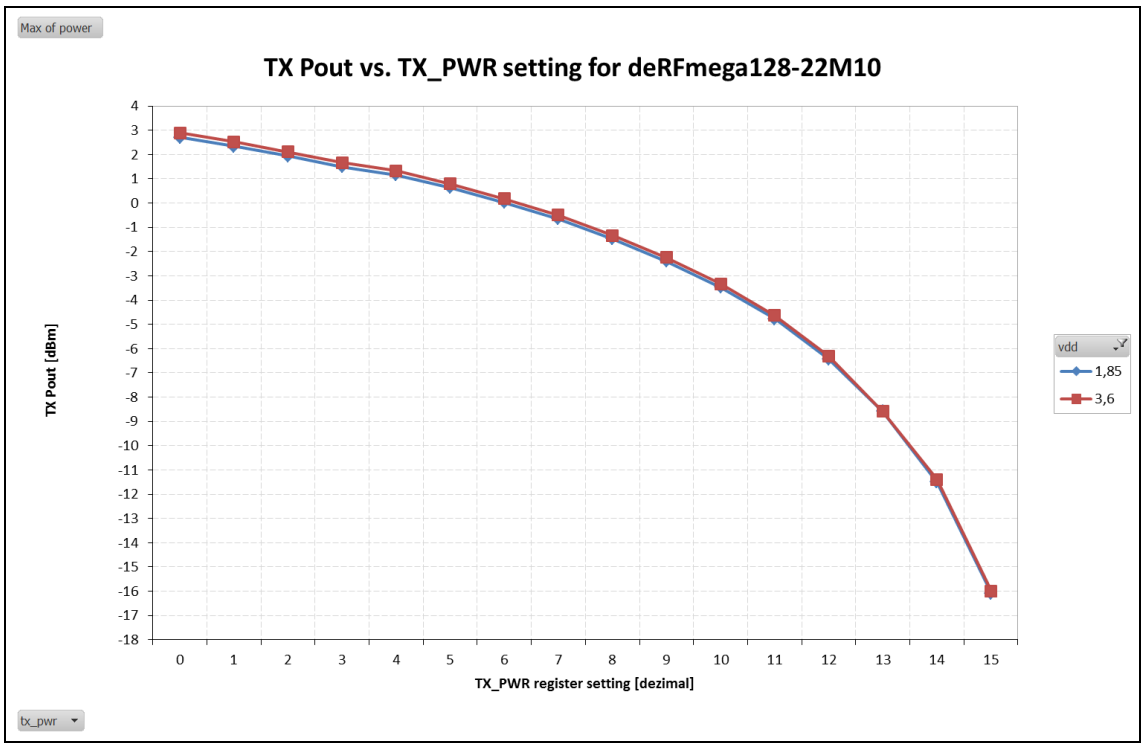


Figure 8: TX Pout vs. TX_PWR for deRFmega128-22M00 / 22M10

4.2. TX Power register settings for deRFmega128-22M12

The diagrams in **Figure 9** and **Figure 10** showing the current consumption and conducted output power during transmission depending on the TX_PWR register setting. The values are valid for deRFmega128-22M12.

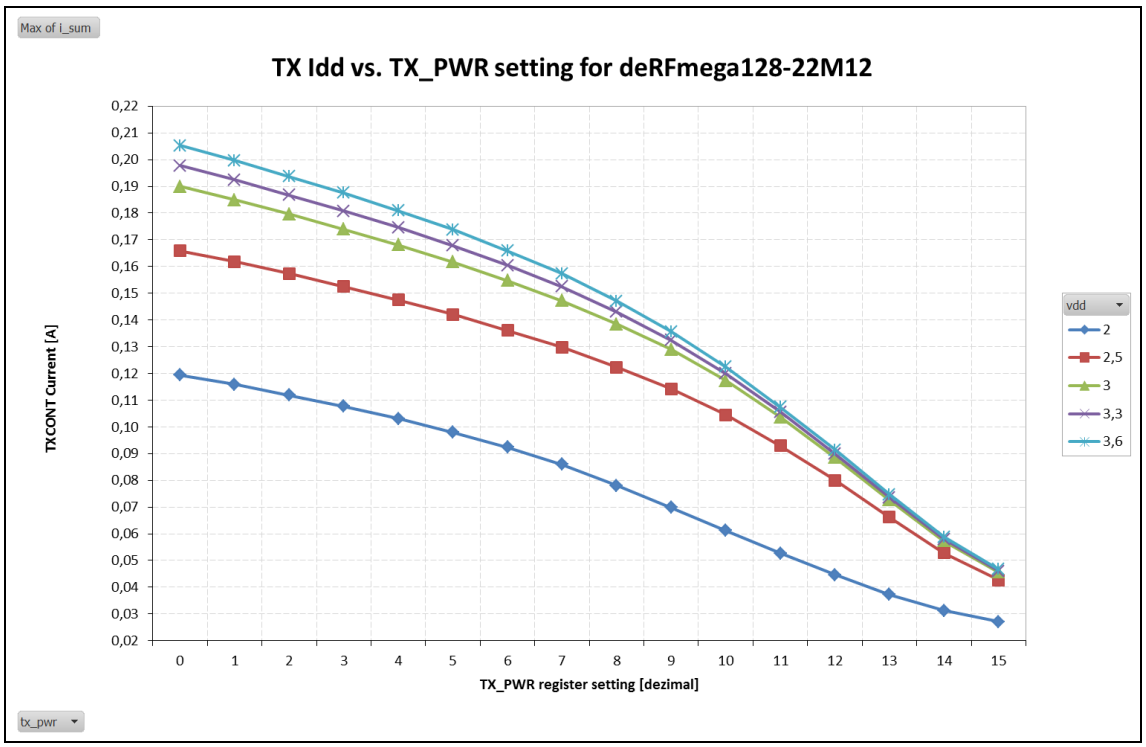


Figure 9: TX Idd vs. TX_PWR for deRFmega128-22M12

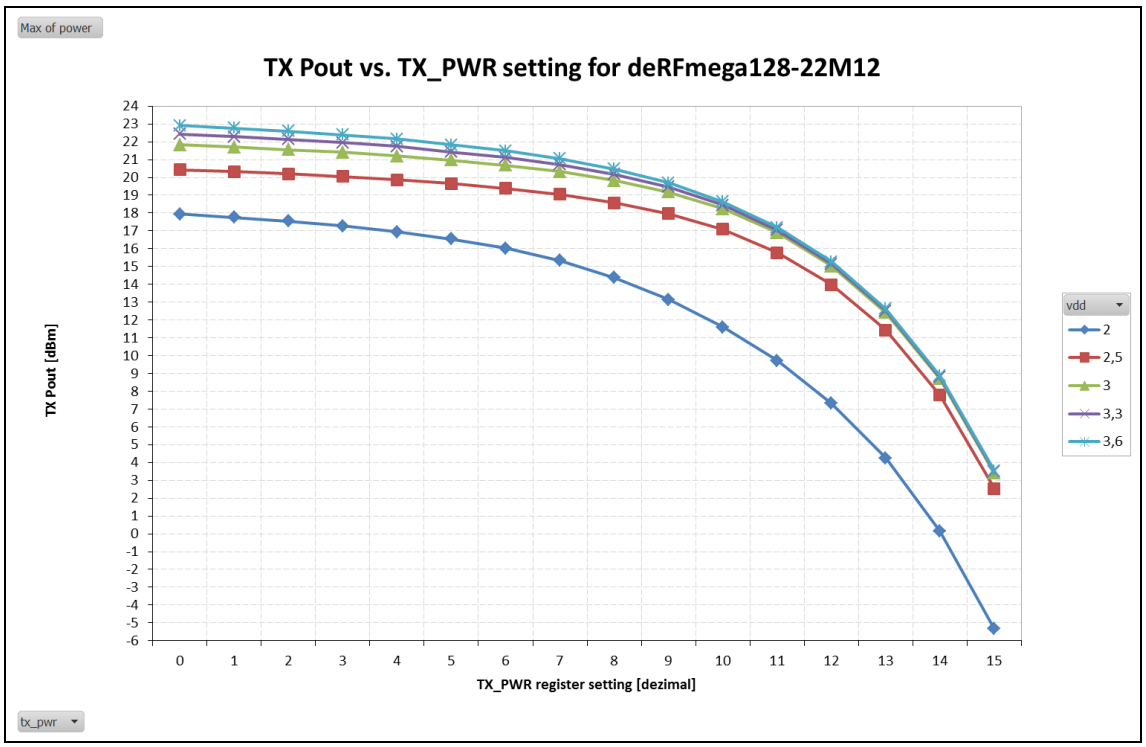


Figure 10: TX Pout vs. TX_PWR for deRFmega128-22M12

4.3. TX Power register settings for deRFmega256-23M00 and 23M10

The diagrams in **Figure 11** and **Figure 12** are showing the current consumption and conducted output power during transmission depending on the TX_PWR register setting. The values are valid for deRFmega256-23M00 and 23M10.

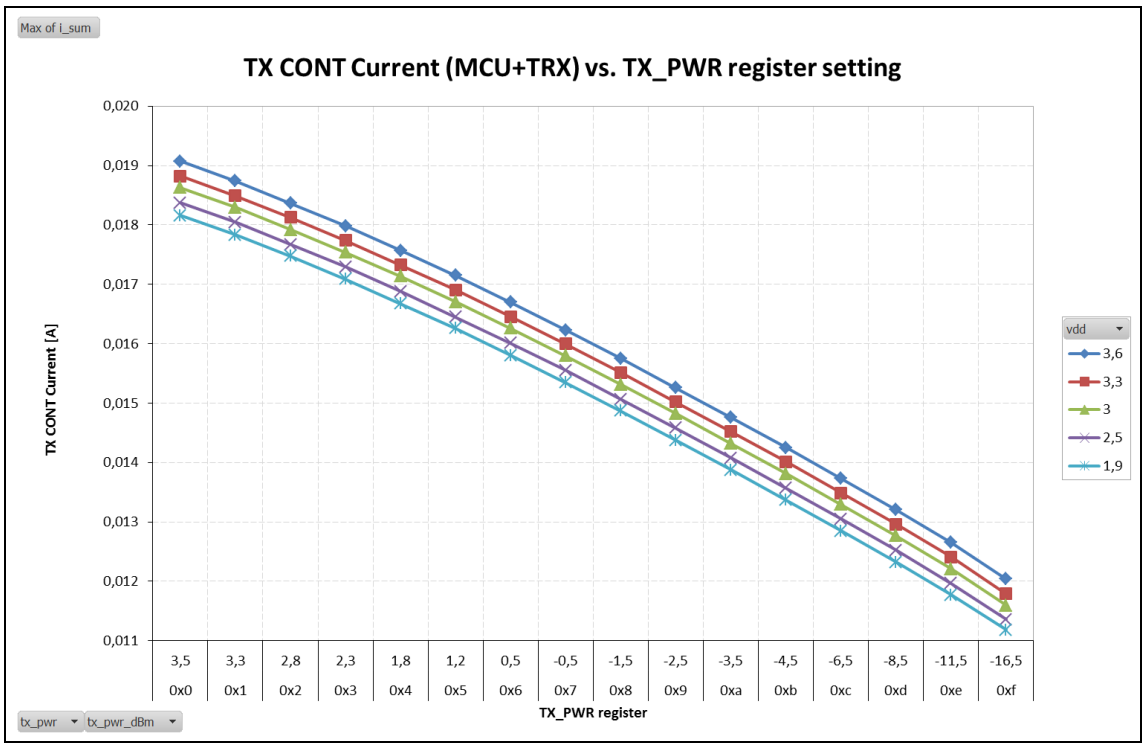


Figure 11: TX Idd vs. TX_PWR for deRFmega256-23M00 / 23M10

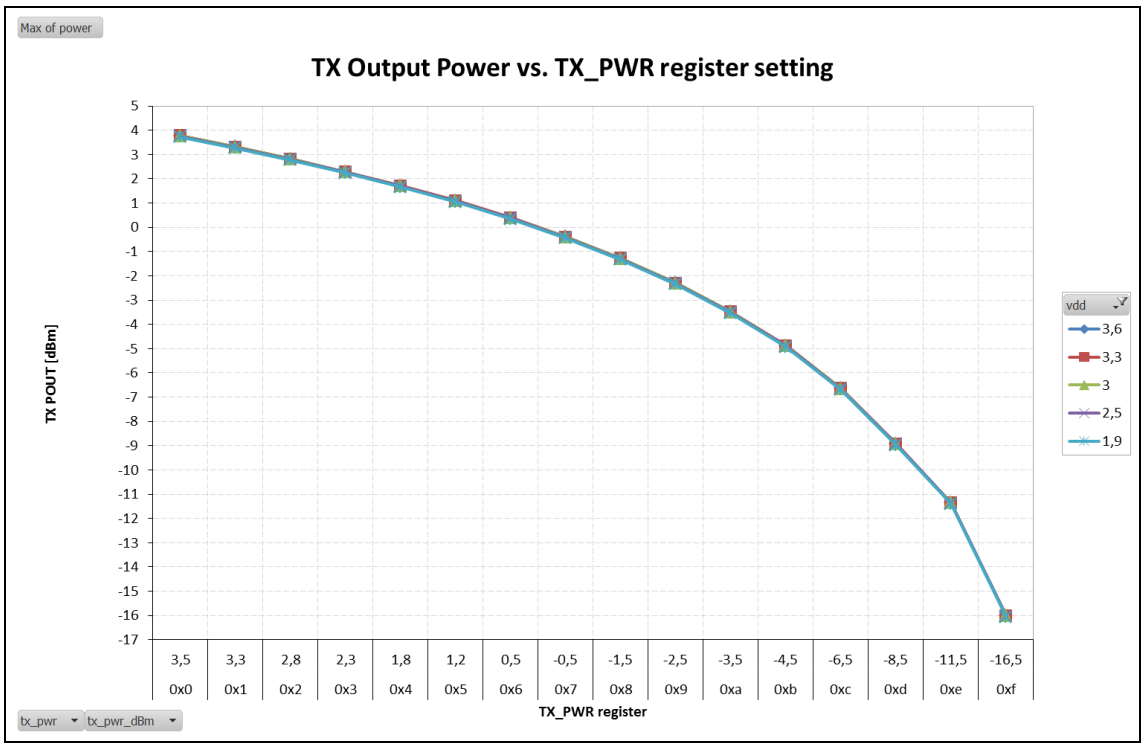


Figure 12: TX Pout vs. TX_PWR for deRFmega256-23M00 / 23M10

4.4. TX Power register settings for deRFmega256-23M12

The diagrams in **Figure 13** and **Figure 14** showing the current consumption and conducted output power during transmission depending on the TX_PWR register setting. The values are valid for deRFmega256-23M12.

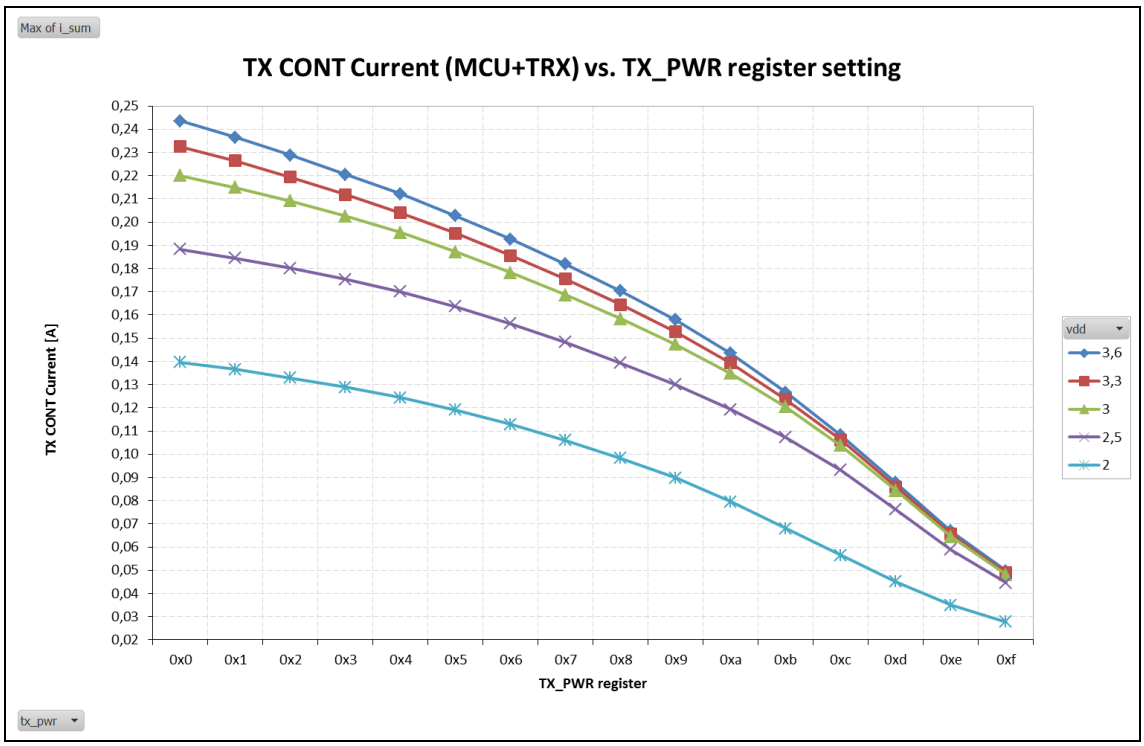


Figure 13: TX Idd vs. TX_PWR for deRFmega256-23M12

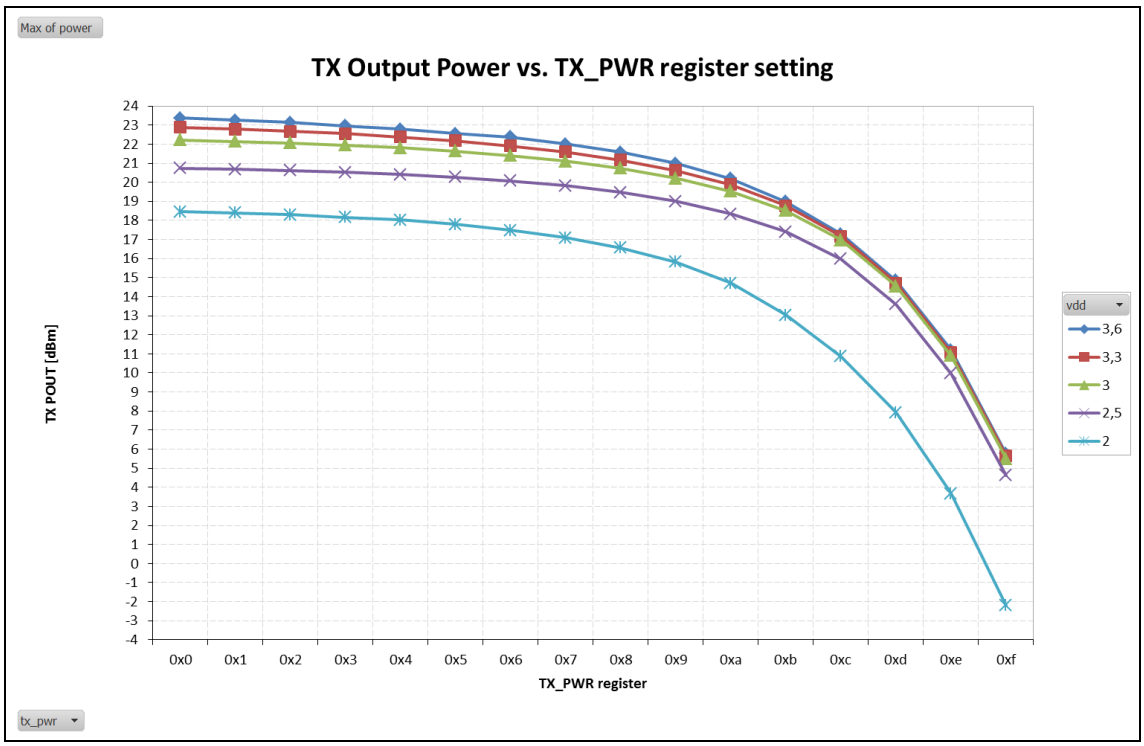


Figure 14: TX Pout vs. TX_PWR for deRFmega256-23M12

4.5. Output power and duty cycle settings for power amplified radio modules

The radio modules deRFmega128-22M12 and deRFmega256-23M12 are able to provide an output power greater than 20dBm. Table 4-10 defines the necessary power settings of the TX_PWR register **[1]** and **[2]**, which must be set to fulfill all national requirements of Europe (EN 300 328) and USA (CFR 47 Ch. I FCC Part 15). The duty cycle defines the relationship between the radio-on time and the period of 100ms.

Table 4-10: power table for deRFmega128-22M12

Device	deRFmega128-22M12				deRFmega256-23M12			
Channel	ETSI		FCC		ETSI		FCC	
	TX_PWR [hex]	Duty Cycle [%]	TX_PWR [hex]	Duty Cycle [%]	TX_PWR [hex]	Duty Cycle [%]	TX_PWR [hex]	Duty Cycle [%]
11	0xE	100	0xB	100	0xF	100	0xD	100
12	0xE	100	0x2	100	0xF	100	0x8	100
13	0xE	100	0x1	100	0xF	100	0x4	100
14	0xE	100	0x0	100	0xF	100	0x4	100
15	0xE	100	0x0	100	0xF	100	0x4	100
16	0xE	100	0x0	100	0xF	100	0x4	100
17	0xE	100	0x0	100	0xF	100	0x4	100
18	0xE	100	0x0	100	0xF	100	0x4	100
19	0xE	100	0x0	100	0xF	100	0x4	100
20	0xE	100	0x0	100	0xF	100	0x4	100
21	0xE	100	0x0	100	0xF	100	0x4	100
22	0xE	100	0x0	100	0xF	100	0x4	100
23	0xE	100	0x6	100	0xF	100	0xA	100
24	0xE	100	0xD	100	0xF	100	0xD	100
25	0xE	100	0xF	100	0xF	100	0xF	100
26	0xE	100	0xF	25	0xF	100	0xF	25

5. Mechanical size

The following section show the mechanical dimensions of the different radio modules. All distances are given in millimeters.

5.1. deRFmega128-22M00 and deRFmega256-23M00

The module has a size of 23.6 x 13.2 mm and a height of 3.0 mm. The LGA pads are arranged in a double row design. **Figure 15** shows the details from top view.

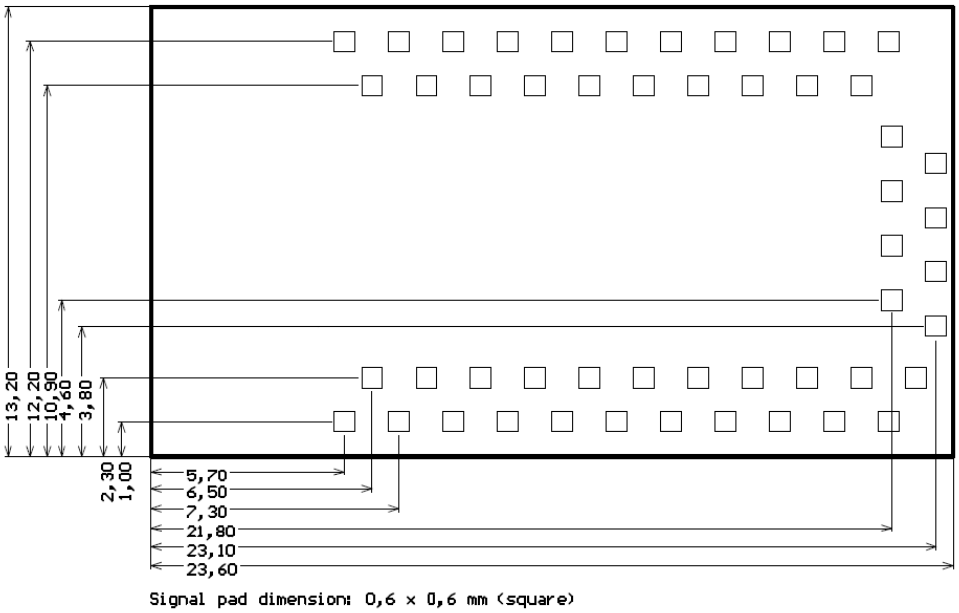


Figure 15: Module dimension and signal pads geometry (top view)

5.2. deRFmega128-22M10 and deRFmega256-23M10

The module has a size of 19.0 x 13.2 mm and a height of 3.0 mm. The LGA pads are arranged in a double row design. The RF pads consist of three ground pads and one signal pad. **Figure 16** and **Figure 17** shows the details from top view.

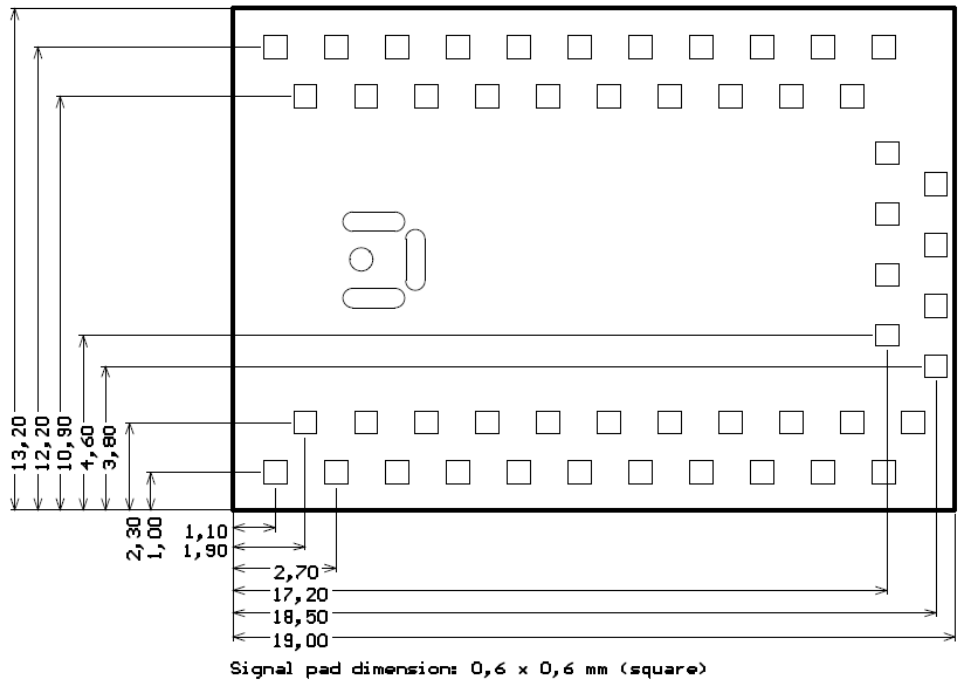


Figure 16: Module dimension and signal pad geometry (top view)

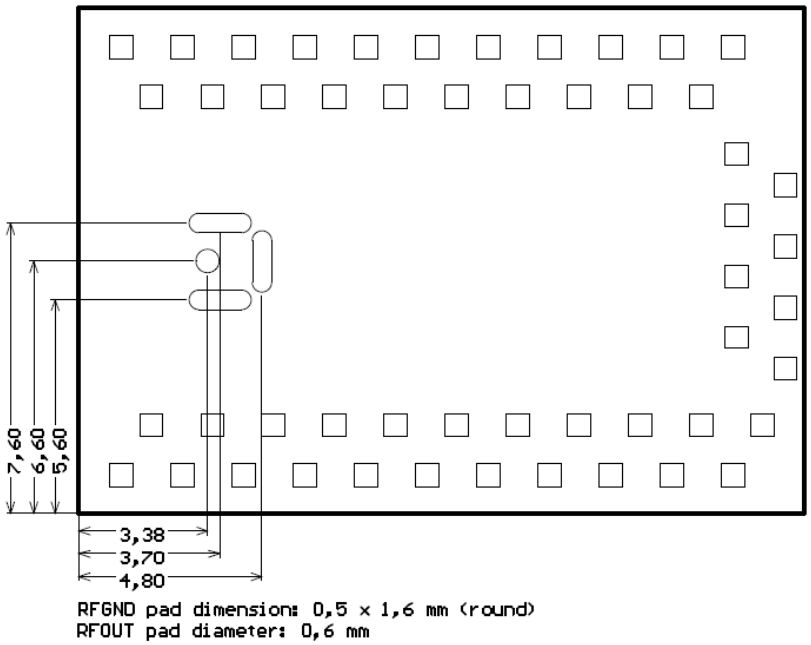


Figure 17: RF pad geometry (top view)

5.3. deRFmega128-22M12 and deRFmega256-23M12

The module has a size of 21.5 x 13.2 mm and a height of 3.0 mm. The LGA pads are designed in a zigzag structure. The RF pads consist of six ground pads and two signal pads. **Figure 18** and **Figure 19** show the details from top view.

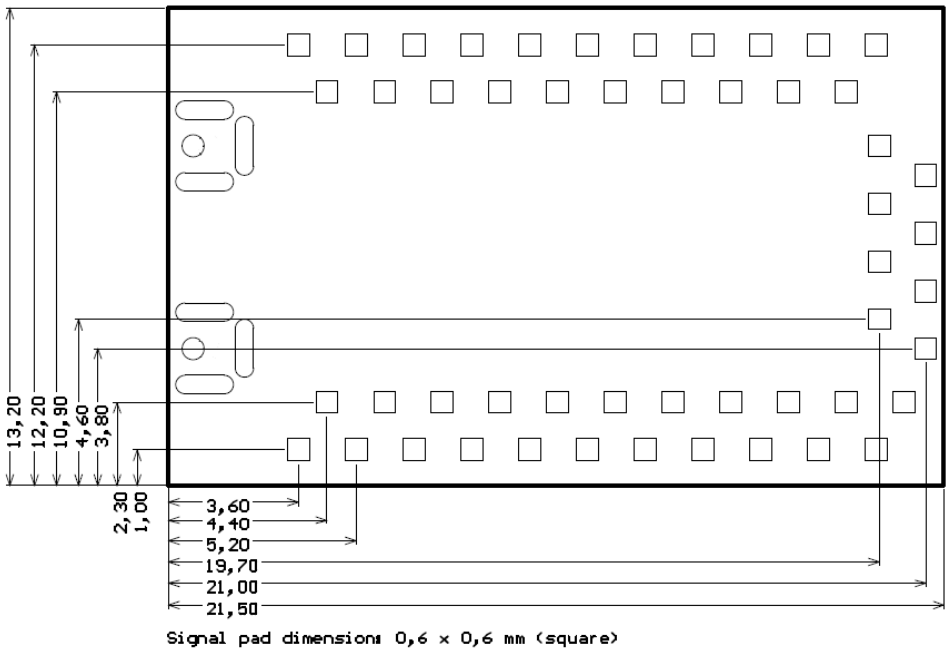


Figure 18: Module dimension and signal pad geometry (top view)

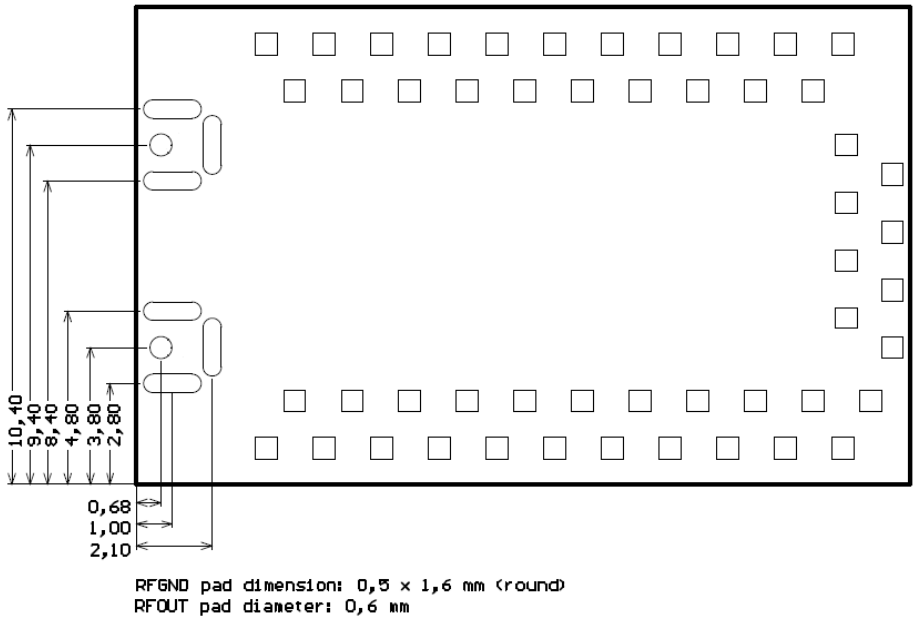


Figure 19: RF pad geometry de (top view)

6. Soldering profile

Table 6-1 shows the recommended soldering profile for the radio modules.

Table 6-1: Soldering Profile

Profile Feature	Values
Average-Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	180 s max
Temperature Maintained Above 217°C	60 s to 150 s
Time within 5°C of Actual Peak Temperature	20 s to 40 s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25°C to Peak Temperature	8 min max

Figure 20 shows a recorded soldering profile for a radio module. The blue colored line illustrates a temperature sensor placed next to the soldering contacts of the radio module. The pink line shows the set temperatures depending on the zone within the reflow soldering machine.

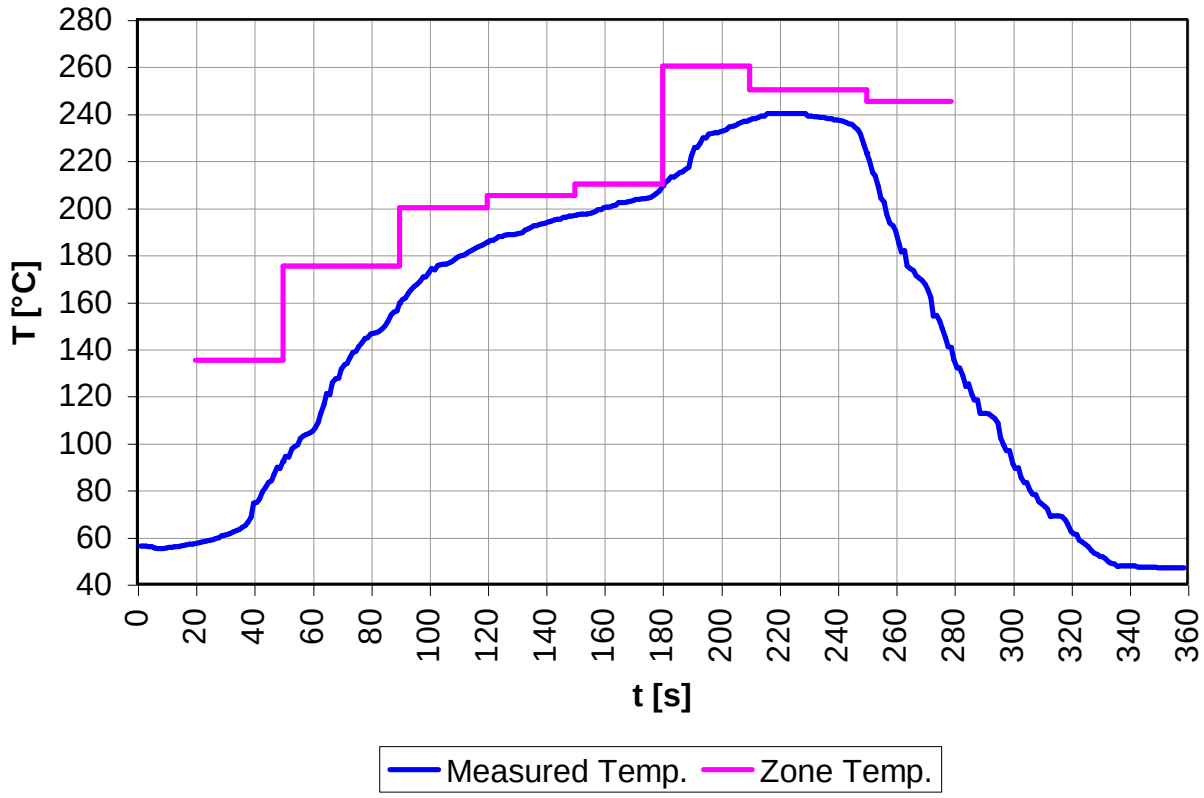


Figure 20: Recorded soldering profile

A solder process without supply of nitrogen causes a discoloration of the metal RF-shielding. It is possible that the placed label shrinks due the reflow process.

7. Pin assignment

The LGA pads provide all signals to the customer: power supply, peripheral, programming, debugging, tracing, analog measurement, external front-end control, antenna diversity control and free programmable ports. All provided signals except VCC, DGND, RSTN, RSTON, AREF, AVDDOUT and CLKI are free programmable port pins (GPIO).

7.1. Signals of deRFmega128-22M00 and deRFmega256-23M00

The radio modules deRFmega128-22M00 and deRFmega256-23M00 have 51 LGA pads. The '1' marking is shown in **Figure 22**. Consider that the pin numbering in **Figure 23** is shown from top view. All available LGA pads are listed in **Table 7-1**.

Figure 21: deRFmega128-22M00 (top view)

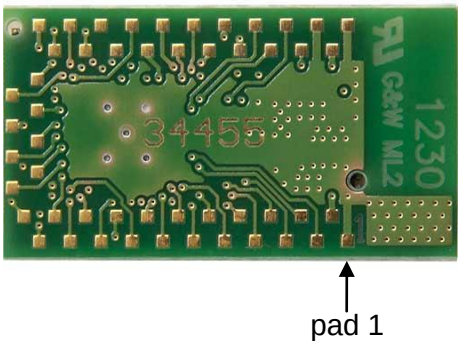


Figure 22: deRFmega128-22M00 (bottom view)

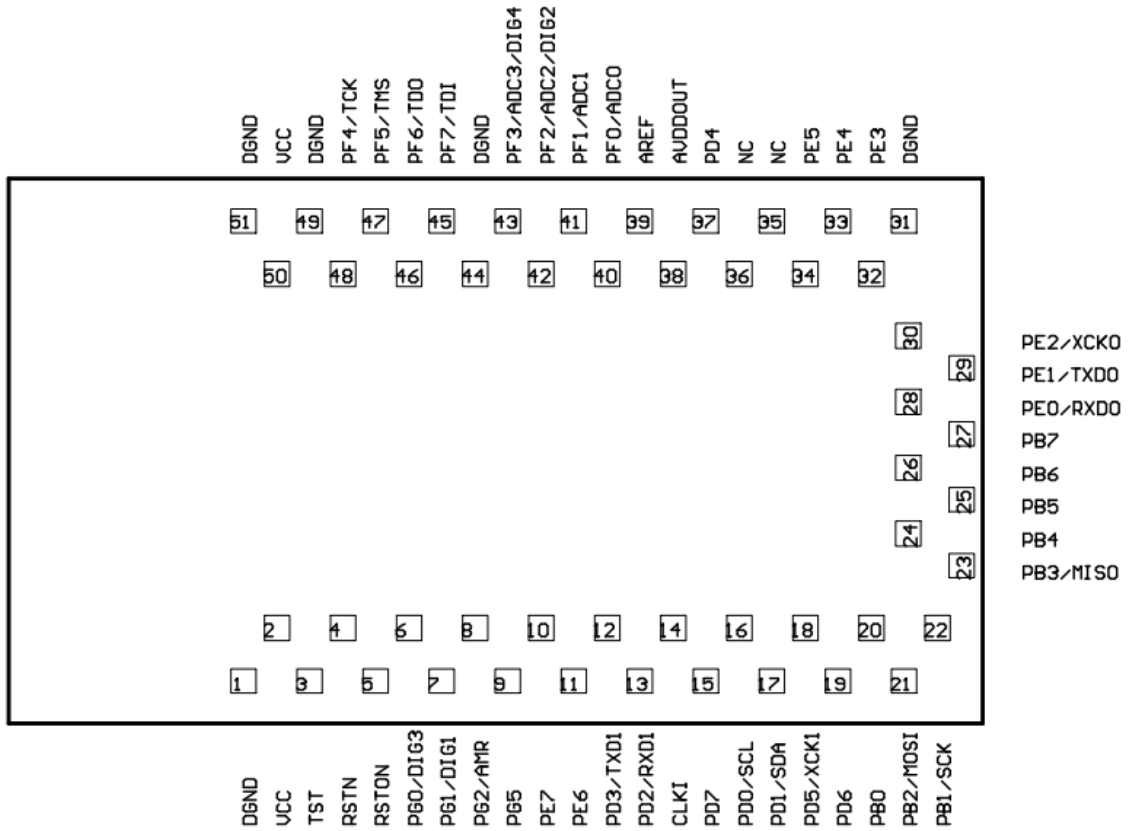


Figure 23: Pad numbering and signal names (top view)

Table 7-1: I/O port pin to LGA pad mapping for deRFmega128-22M00 and deRFmega256-23M00

I/O port pin mapping						
LGA Pad	*MCU Pin*	*Primary function*	*Alternate functions*			*Comments*
		GND				
2	-	VCC				1.8 V to 3.6 V
3	11	TST				**Must be connected to GND!**
4	12	RSTN				Reset
5	13	RSTON				Reset output
6	14	PG0		DIG3		
7	15	PG1		DIG1		
8	16	PG2	AMR			
9	19	PG5	OC0B			
10	53	PE7	ICP3	INT7	CLKO	
11	52	PE6	T3	INT6		Timer3
12	28	PD3	TXD1	INT3		UART1
13	27	PD2	RXD1	INT2		UART1
14	33	CLKI				External clock input
15	32	PD7		T0		
16	25	PD0	SCL	INT0		TWI
17	26	PD1	SDA	INT1		TWI
18	30	PD5		XCK1		
19	31	PD6		T1		Timer1
20	36	PB0	SS		PCINT0	SPI
21	38	PB2	MOSI	PDI	PCINT2	SPI, ISP
22	37	PB1	SCK		PCINT1	SPI
23	39	PB3	MISO	PDO	PCINT3	SPI, ISP
24	40	PB4		OC2A	PCINT4	
25	41	PB5		OC1A	PCINT5	
26	42	PB6		OC1B	PCINT6	
27	43	PB7	OC0A	OC1C	PCINT7	
28	46	PE0	RXD0		PCINT8	UART0
29	47	PE1	TXD0			UART0
30	48	PE2	XCK0	AIN0		UART0
31	-	GND				

32	49	PE3	OC3A	AIN1		
33	5	PE4	OC3B	INT4		
34	51	PE5	OC3C	INT5		
35	-	NC				Leave unconnected
36	-	NC				Leave unconnected
37	29	PD4		ICP1		
38	60	AVDDOUT				**Leave unconnected if unused (1.8V TRX Voltage Output)** Internal 1uF capacitor
39	62	AREF				No internal capacitor assambled
40	63	PF0	ADC0			ADC
41	64	PF1	ADC1			ADC
42	1	PF2	ADC2	DIG2		ADC
43	2	PF3	ADC3	DIG4		
44	-	GND				
45	6	PF7	ADC7		TDI	JTAG
46	5	PF6	ADC6		TDO	JTAG
47	4	PF5	ADC5		TMS	JTAG
48	3	PF4	ADC4		TCK	JTAG
49	-	GND				
50	-	VCC				1.8 V to 3.6 V
51	-	GND				

Note: PG4/TOSC1 and PG3/TOSC2 are connected to a 32.768 kHz crystal internally.

7.2. Signals of deRFmega128-22M10 and deRFmega256-23M10

The radio modules deRFmega128-22M10 and deRFmega256-23M10 have 55 LGA pads. The '1' marking is shown in **Figure 25**. Consider that the pin numbering in **Figure 26** is shown from top view. All LGA pads are listed in **Table 7-2**.

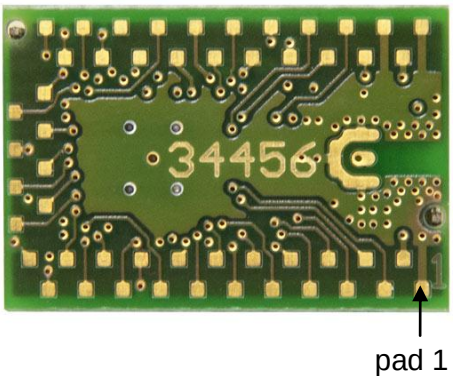


Figure 24: deRFmega128-22M10 (top view) **Figure 25: deRFmega128-22M10 (bottom view)**

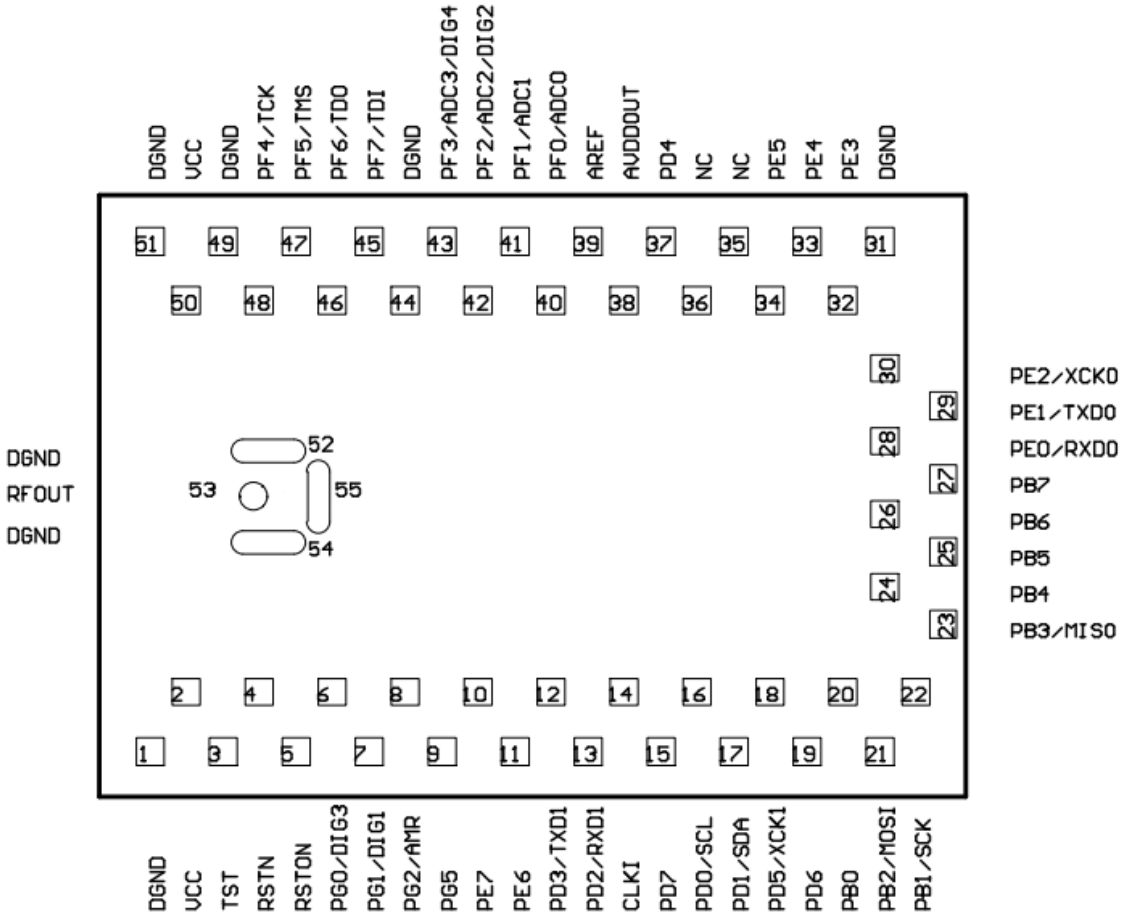


Figure 26: Pad numbering and signal names (top view)

Table 7-2: I/O port pin to LGA pad mapping for deRFmega128-22M10 and deRFmega256-23M10

I/O port pin mapping						
LGA Pad	*MCU Pin*	*Primary function*	*Alternate functions*			*Comments*
1	-	GND				
2	-	VCC				1.8 V to 3.6 V
3	11	TST				**Must be connected to GND!**
4	12	RSTN				Reset
5	13	RSTON				Reset output
6	14	PG0		DIG3		External Front-End control
7	15	PG1		DIG1		External diversity control
8	16	PG2	AMR			
9	19	PG5	OC0B			
10	53	PE7	ICP3	INT7	CLKO	
11	52	PE6	T3	INT6		Timer3
12	28	PD3	TXD1	INT3		UART1
13	27	PD2	RXD1	INT2		UART1
14	33	CLKI				External clock input
15	32	PD7		T0		
16	25	PD0	SCL	INT0		TWI
17	26	PD1	SDA	INT1		TWI
18	30	PD5		XCK1		
19	31	PD6		T1		Timer1
20	36	PB0	SS		PCINT0	SPI
21	38	PB2	MOSI	PDI	PCINT2	SPI, ISP
22	37	PB1	SCK		PCINT1	SPI
23	39	PB3	MISO	PDO	PCINT3	SPI, ISP
24	40	PB4		OC2A	PCINT4	
25	41	PB5		OC1A	PCINT5	
26	42	PB6		OC1B	PCINT6	
27	43	PB7	OC0A	OC1C	PCINT7	
28	46	PE0	RXD0		PCINT8	UART0
29	47	PE1	TXD0			UART0
30	48	PE2	XCK0	AIN0		UART0
31	-	GND				

32	49	PE3	OC3A	AIN1		
33	5	PE4	OC3B	INT4		
34	51	PE5	OC3C	INT5		
35	-	NC				Leave unconnected
36	-	NC				Leave unconnected
37	29	PD4		ICP1		
38	60	AVDDOUT				**Leave unconnected if unused (1.8V TRX Voltage Output)** Internal 1uF capacitor
39	62	AREF				No internal capacitor assambled
40	63	PF0	ADC0			ADC
41	64	PF1	ADC1			ADC
42	1	PF2	ADC2	DIG2		ADC
43	2	PF3	ADC3	DIG4		External Front-End control
44	-	GND				
45	6	PF7	ADC7		TDI	JTAG
46	5	PF6	ADC6		TDO	JTAG
47	4	PF5	ADC5		TMS	JTAG
48	3	PF4	ADC4		TCK	JTAG
49	-	GND				
50	-	VCC				1.8 V to 3.6 V
51	-	GND				
52	-	RFGND				
53	-	RFOUT				50 Ω impedance
54	-	RFGND				
55	-	RFGND				

Note: PG4/TOSC1 and PG3/TOSC2 are internally connected to a 32.768 kHz crystal.

7.2.1. External front-end and antenna diversity control

The radio modules deRFmega128-22M10 and deRFmega256-23M10 offer the possibility to control external front-end components and to support antenna diversity. **Table 7-3** and **Table 7-4** show the logic values of the control signals. A logic '0' is specified with a voltage level of 0 V to 0.3 V. A logic '1' is specified with a value of VCC - 0.3 V to 3.6 V.

An application circuit is shown in **Section 10.5**.

Antenna Diversity
The antenna diversity algorithm is enabled with setting bit ANT_DIV_EN=1 in the ANT_DIV register. The external control of RF switches must be enabled by bit ANT_EXT_SW_EN of the same register. This action will configure the pins DIG1 and DIG2 as outputs. Both pins are used to feed the RF switch signal and its inverse to the differential inputs of the RF switch. Please refer to ATmega128RFA1 **[1]** and ATmega256RFR2 **[2]** datasheet to get information to all register settings.

Table 7-3: Antenna diversity control

Mode description	PG1/DIG1	PF2/DIG2
TRX off Sleep mode	Disable register bit ANT_EXT_SW_EN and set port pins DIG1 and DIG2 to output low via I/O port control registers. This action could reduce the power consumption of an external RF switch.	
ANT0	1	0
ANT1	0	1

Front-End
The control of front-end components can be realized with the signals DIG3 and DIG4. The function will be enabled with bit PA_EXT_EN of register TRX_CTRL_1 which configures both pins as outputs. While transmission is turned off DIG3 is set to '0' and DIG4 is set to '1'. When the transceiver starts transmission the polarity will be changed. Both pins can be used to control PA, LNA and RF switches. Please refer to ATmega128RFA1 **[1]** and ATmega256RFR2 **[2]** datasheet to get information to all register settings.

Table 7-4: Front-end control

	PG0/DIG3	PF3/DIG4
TRX off Sleep mode	Disable register bit PA_EXT_EN and set port pins DIG3 and DIG4 to output low via I/O port control registers. This action may reduce the power consumption of external front-end devices.	
TRX off	0	1
TRX on	1	0

Sleep mode
To optimize the power consumption of external front-end components, it is possible to use a dedicated GPIO to set the PA into sleep mode, if applicable or to switch an additionally MOSFET, which supplies the PA.

7.3. Signals of deRFmega128-22M12 and deRFmega256-23M12

The radio modules deRFmega128-22M12 and deRFmega256-23M12 have 59 LGA pads. The '1' marking is shown in **Figure 28**. Consider that the pin numbering in **Figure 29** is shown from top view. All LGA pads are listed in **Table 7-5**.

Figure 27: deRFmega128-22M12 (top view)

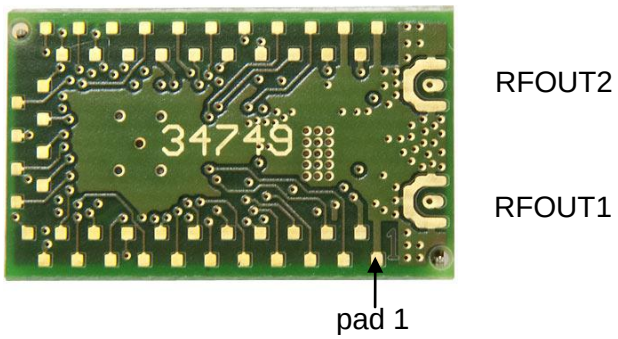


Figure 28: deRFmega128-22M12 (bottom view)

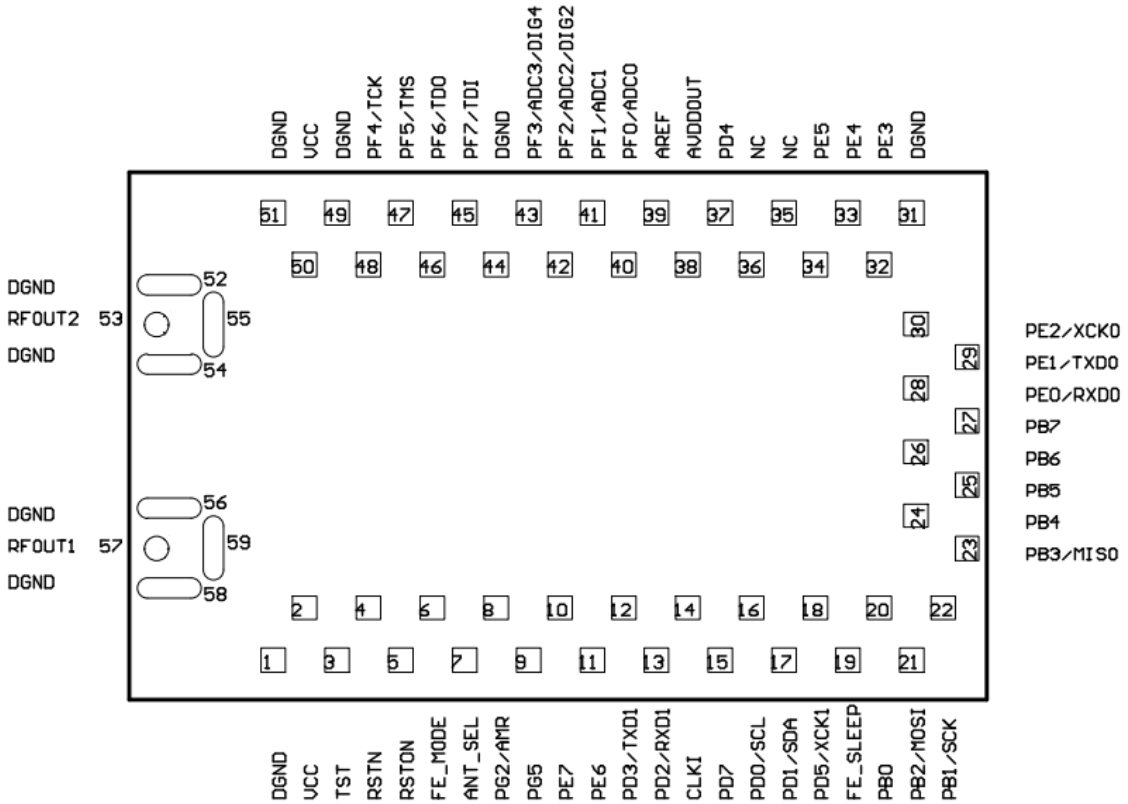


Figure 29: Pad numbering and signal names (top view)

Table 7-5: I/O port pin to LGA pad mapping for deRFmega128-22M12 and deRFmega256-23M12

I/O port pin mapping						
LGA Pad	*MCU Pin*	*Primary function*	*Alternate functions*			*Comments*
1	-	GND				
2	-	VCC				2.0 V to 3.6 V
3	11	TST				**Must be connected to GND!**
4	12	RSTN				Reset
5	13	RSTON				Reset output
6	14	PG0		DIG3		**Leave unconnected** Internal connected to PA-CTX[9]
7	15	PG1		DIG1		**Leave unconnected** Internal connected to PA-ANTSEL[9]
8	16	PG2	AMR			
9	19	PG5	OC0B			
10	53	PE7	ICP3	INT7	CLKO	
11	52	PE6	T3	INT6		Timer3
12	28	PD3	TXD1	INT3		UART1
13	27	PD2	RXD1	INT2		UART1
14	33	CLKI				External clock input
15	32	PD7		T0		
16	25	PD0	SCL	INT0		TWI
17	26	PD1	SDA	INT1		TWI
18	30	PD5		XCK1		
19	31	PD6		T1		**Leave unconnected** Internal connected to PA-CSD[9]
20	36	PB0	SS		PCINT0	SPI
21	38	PB2	MOSI	PDI	PCINT2	SPI, ISP
22	37	PB1	SCK		PCINT1	SPI
23	39	PB3	MISO	PDO	PCINT3	SPI, ISP
24	40	PB4		OC2A	PCINT4	
25	41	PB5		OC1A	PCINT5	
26	42	PB6		OC1B	PCINT6	
27	43	PB7	OC0A	OC1C	PCINT7	
28	46	PE0	RXD0		PCINT8	UART0

[9] See Section 7.3.1

29	47	PE1	TXD0			UART0
30	48	PE2	XCK0	AIN0		UART0
31	-	GND				
32	49	PE3	OC3A	AIN1		
33	5	PE4	OC3B	INT4		
34	51	PE5	OC3C	INT5		
35	-	NC				Leave unconnected
36	-	NC				Leave unconnected
37	29	PD4		ICP1		
38	60	AVDDOUT				**Leave unconnected if unused (1.8V TRX Voltage Output)** Internal 1uF capacitor
39	62	AREF				No internal capacitor assambled
40	63	PF0	ADC0			ADC
41	64	PF1	ADC1			ADC
42	1	PF2	ADC2	DIG2		**Leave unconnected**
43	2	PF3	ADC3	DIG4		**Leave unconnected**
44	-	GND				
45	6	PF7	ADC7		TDI	JTAG
46	5	PF6	ADC6		TDO	JTAG
47	4	PF5	ADC5		TMS	JTAG
48	3	PF4	ADC4		TCK	JTAG
49	-	GND				
50	-	VCC				2.0 V to 3.6 V
51	-	GND				
52	-	RFGND				
53	-	RFOUT2				50 Ω impedance*****
54	-	RFGND				
55	-	RFGND				
56	-	RFGND				
57	-	RFOUT1				50 Ω impedance*****
58	-	RFGND				
59	-	RFGND				

Note: PG4/TOSC1 and PG3/TOSC2 are internally connected to a 32.768 kHz crystal.

***) If one of both RFOUT pads of the radio modules deRFmega128-22M12 / 23M12 is unused, it must be terminated with 50 ohms to ground. This action ensures the proper function of the internal power amplifier and will reduce the power consumption.**

7.3.1. Internal front-end control

The front-end of deRFmega128-22M12 and deRFmega256-23M12 have an internal PA for transmit and a LNA for receive mode. An additionally antenna diversity feature is usable to select the antenna with the best link budget. The front-end control includes three MCU port pins (**Figure 30**). They are used to choose the TX/RX antenna, de-/activate transmit and receive mode and de-/activate the sleep mode. **Table 7-6** and **Table 7-7** show the logic values. A logic '0' is specified with a voltage level of 0 V to 0.3 V. A logic '1' is specified with a value of VCC - 0.3 V to 3.6 V. The control signals DIG1, DIG3 and PD6 are available on the LGA pins.

Table 7-6: Front-end control of TX/RX and sleep mode

Mode description	PG1/DIG1	PD6/T1	PG0/DIG3
	PA_ANT SEL	PA_CSD	PA_CTX
All off (sleep mode)	X	0	0
RX LNA mode	X	1	0
TX mode	X	1	1

Table 7-7: Front-end control of TX/RX antenna

Mode description	PG1/DIG1	PD6/T1	PG0/DIG3
	PA_ANT SEL	PA_CSD	PA_CTX
RFOUT1 port enabled	0	X	X
RFOUT2 port enabled	1	X	X

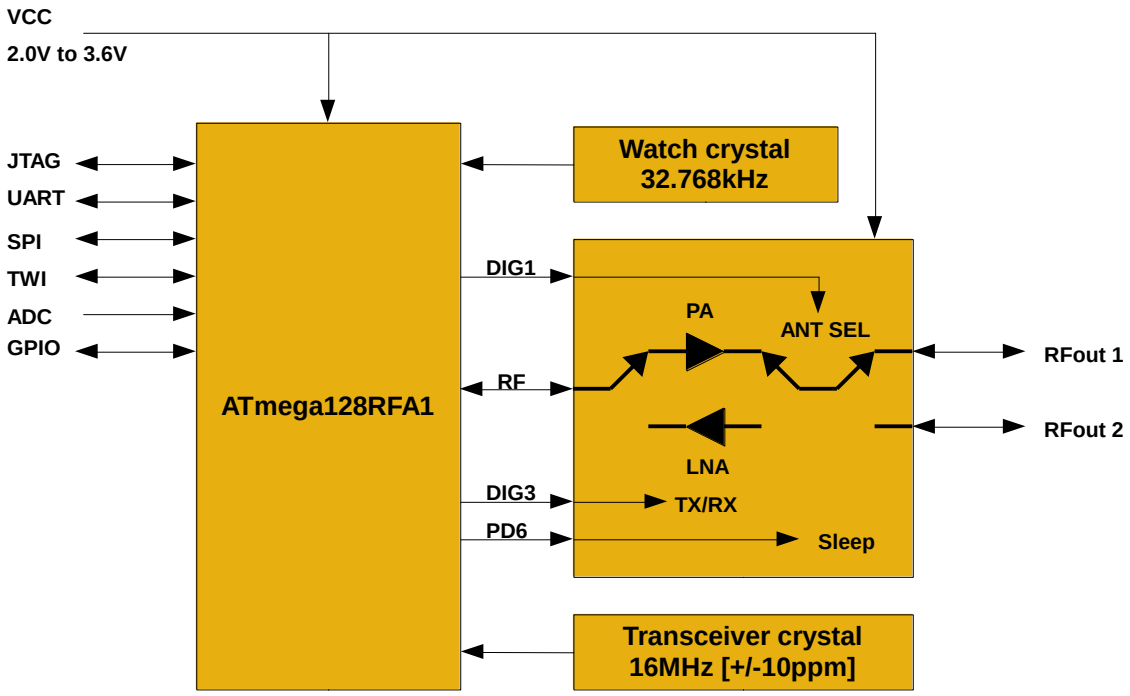


Figure 30: Block diagram of front-end functionality and control

Note: Do not leave any unused RFOUT pad unterminated!
Leave pins DIG1, DIG2, DIG3, DIG4 and PD6 unconnected to ensure the proper front-end functionality!

7.4. Signal description

The available signals are described in **Table 7-8**. Please refer to ATmega128RFA1 **[1]** and ATmega256RFR2 **[2]** datasheet for more information of all dedicated signals.

Table 7-8: Signal description list

Signal name	Function	Type	Active Level	Comments
Power				
VCC	Voltage Regulator Power Supply Input	Power		
GND		Ground		
Clocks and Oscillators				
CLKI	External Clock Input	Input		
CLKO	Divided System Clock Output	Output		
JTAG				
TCK	Test Clock	Input		No pull-up resistor on module
TDI	Test Data In	Input		No pull-up resistor on module
TDO	Test Data Out	Output		
TDM	Test Mode Select	Input		No pull-up resistor on module
Serial Programming				
PDI	Data Input	Input		
PDO	Data Output	Output		
SCK	Serial Clock	Input		
Reset				
RSTN	Microcontroller Reset	I/O	Low	Pull-Up resistor[10]
USART				
TXD0 – TXD1	Transmit Data			
RXD0 – RXD1	Receive Data			
XCK0 – XCK1	Serial Clock			
Timer/Counter and PWM Controller				
OC0A-OC3A	Output Compare and PWM Output A for Timer/Counter 0 to 3			
OC0B-OC3B	Output Compare and PWM Output B for Timer/Counter 0 to 3			

[10] Internal MCU Pull-up resistor

OC0C-OC3C	Output Compare and PWM Output C for Timer/Counter 0 to 3			
T0, T1, T3	Timer/Counter 0,1,3 Clock Input	Input		
ICP1 ICP3	Timer/Counter Input Capture Trigger 1 and 3	Input		
Interrupt				
PCINT0 - PCINT7	Pin Change Interrupt Source 0 to 7	Output		
INT0 – INT7	External Interrupt Input 0 to7	Input		
SPI				
MISO	SPI Master In/Slave Out	I/O		
MOSI	SPI Master Out/Slave In	I/O		
SCK	SPI Bus Serial Clock	I/O		
SSN	SPI Slave Port Select	I/O		
Two-Wire-Interface				
SDA	Two-Wire Serial Interface Data	I/O		No pull-up resistor[11]
SCL	Two-Wire Serial Interface Clock	I/O		No pull-up resistor[11]
Analog-to-Digital Converter				
ADC0 – ADC7	Analog to Digital Converter Channel 0 to 7	Analog		
AREF	Analog Reference	Analog		
AVDDOUT	1.8V Regulated Analog Supply Voltage Output from Transceiver	Analog		
Analog Comparator				
AIN0	Analog Comparator Positive Input	Analog		
AIN1	Analog Comparator Negative Input	Analog		
Radio Transceiver				
DIG1/DIG2	Antenna Diversity Control Output	Output		Set to output by register command
DIG3/DIG4	External Front-End control	Output		

[11] External 4k7 pull-up resistors necessary for proper Two-Wire-Interface functionality

8. PCB design

The PCB design of a radio module base board is important for a proper performance of peripherals and the radio. The next subsections give design hints to create a custom base board.

8.1. Technology

The described design has the main goal to use standard PCB technology to reduce the costs and cover a wider application range.

Design parameters

- 150 µm manufacturing process
- 4 layer PCB with FR4 Prepreg
- No via plugging
- Via hole size: 0.2 mm
- Via diameter: 0.6 mm

8.2. Base board footprint

The footprint for a custom base board depends on the radio module used. The mechanical dimensions are shown in **Section 5**. The following part describes an example to design a base board.

Properties of stencil and solder paste

- Stencil = 130 µm thickness
- Lead free solder paste (particle size from 20 to 38 µm)

Properties of signal pads

- Signal pad dimension = 0.6 x 0.6 mm (rectangular, red)
- Signal pad cut-out on stencil = 0.6 x 0.6 mm (rectangular, grey)
- Clearance to solder stop = 0.1 mm (purple)

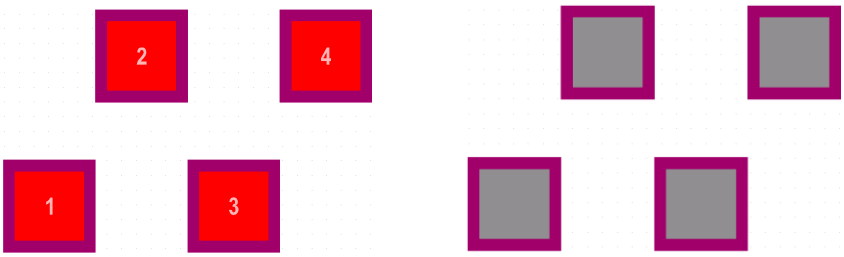


Figure 31: Signal pad footprint design

Properties of RF pads

- RF ground pad dimension = 1.6 x 0.5 mm (round, red)
- RF ground pad cut-out on stencil = 1.3 x 0.2 mm (round, grey)
- RF signal-out pad dimension = 0.6 x 0.6 mm (round, red)
- RF signal-out pad cut-out on stencil = 0.6 x 0.6 mm (round, grey)
- Clearance to solder stop = 0.1 mm (purple)

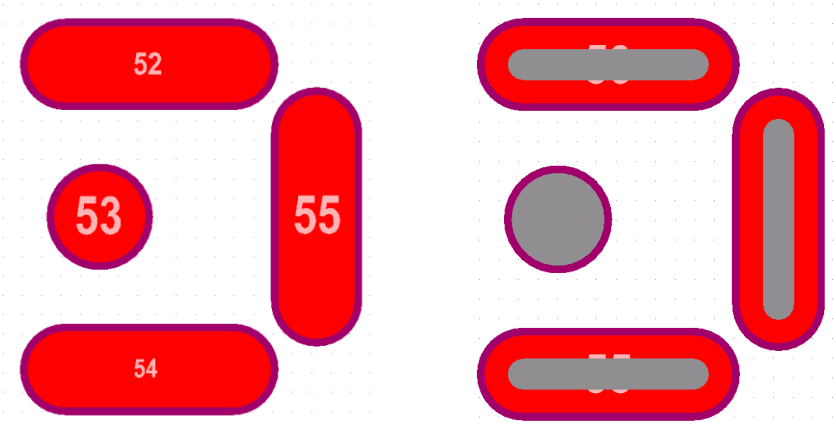


Figure 32: RF pad footprint design (top view)

8.2.1. Footprint of deRFmega128-22M00 and deRFmega256-23M00

Figure 33 shows an exemplary base board footprint for deRFmega128-22M00 and deRFmega256-23M00. Only the top layer (red) is visible. The mid and bottom layers are hidden. The rectangular signal pad copper area (red, not visible) and the paste dimension (grey) have the same size of 0.6 x 0.6 mm. The solder stop clearance (purple) has a value of 0.1 mm. Do not place copper on any other area among the entire module. Solder stop could be used everywhere.

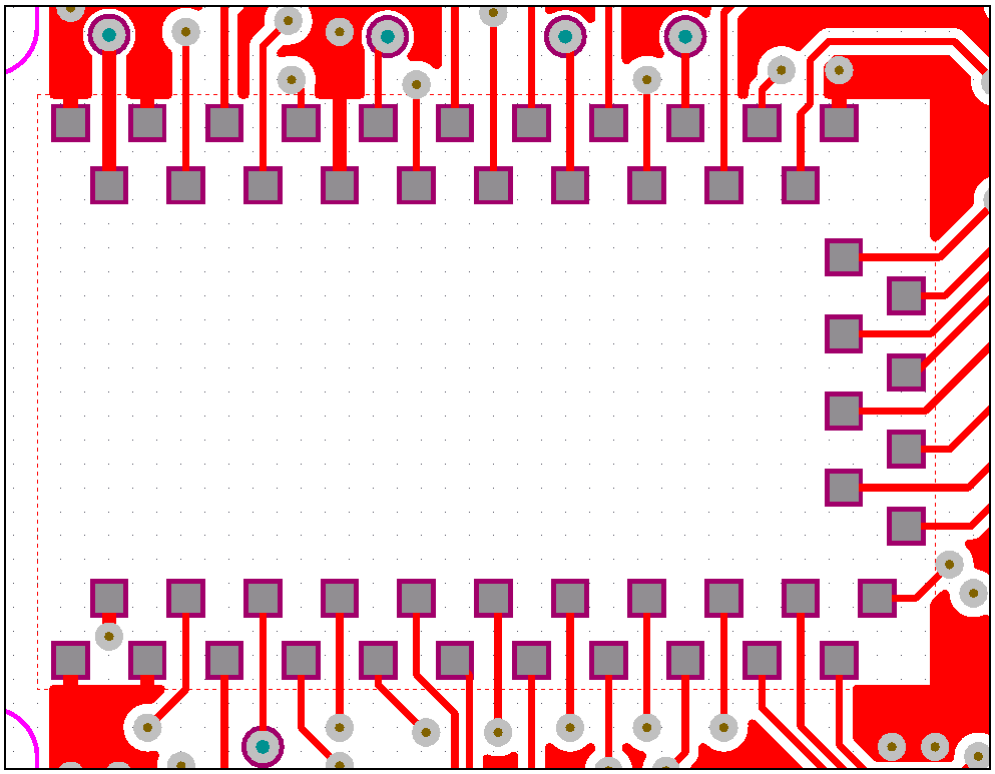


Figure 33: Exemplary base board footprint for 22M00 / 23M00 (top view)

8.2.2. Footprint of deRFmega128-22M10 and deRfmega256-23M10

The exemplary base board footprint for deRFmega128-22M10 and deRFmega256-23M10 is shown in **Figure 34**. The top layer (red) is visible, the mid and bottom layers are hidden. The rectangular signal pad copper area (red, not visible) and the paste dimension (grey) have the same size of 0.6 x 0.6 mm. The solder stop clearance (purple) has a value of 0.1 mm.

The RF ground pads are connected to each other and to the board ground to ensure a proper ground area. For the most applications it is not necessary to separate the RF ground from system ground. The RF ground area in **Figure 34** has a vertical dimension of 3.8 mm. The ground vias are not plugged. In this area are no other radio module signals. An unintentional short-circuit is therefore accepted. Do not place copper on any other area among the entire module. Solder stop could be used everywhere.

The RF trace design depends on the used base board and is described detailed in **Section 8.5.**

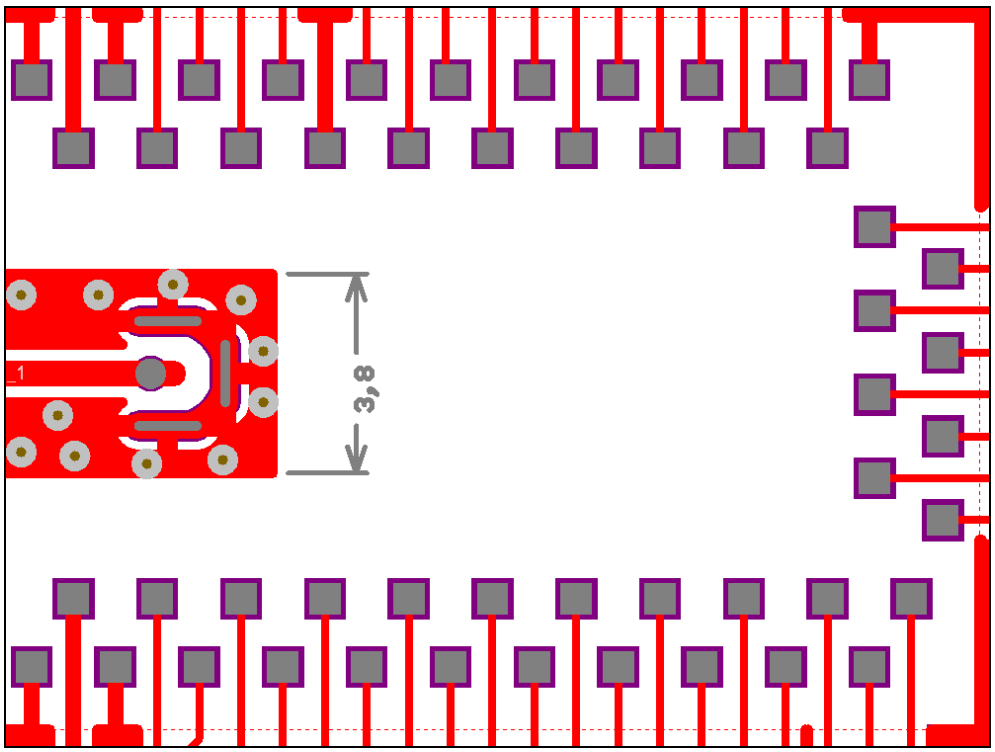


Figure 34: Exemplary base board footprint for 22M10 /23M10 (top view)

8.2.3. Footprint of deRFmega128-22M12 and deRFmega256-23M12

Figure 35 shows an exemplary base board footprint for deRFmega128-22M12 and deRFmega256-23M12. Only the top layer (red) is visible. The mid and bottom layers are hidden. The pad copper area (red, not visible) and the paste dimension (grey) have the same size of 0.6 x 0.6 mm. The solder stop clearance (purple) has a value of 0.1 mm.

The RF ground pads are connected to each other and to the board ground to ensure a proper ground area. For the most applications it is not necessary to separate the RF ground from system ground. The RF ground area in **Figure 35** has a vertical dimension of 9.4 mm. The ground vias are not plugged. In this area are no other radio module signals. An unintentional short-circuit is therefore accepted. Do not place copper on any other area among the entire module. Solder stop could be used everywhere.

The RF trace design depends on the used base board and is described detailed **Section 8.5.**

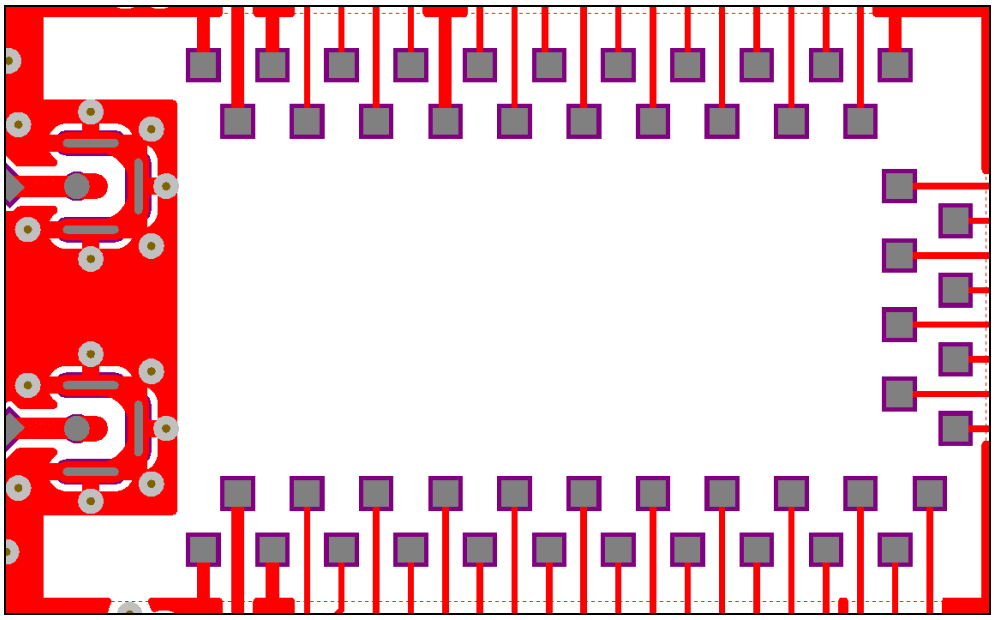


Figure 35: Exemplary base board footprint for 22M12 / 23M12 (top view)

8.3. Ground plane

The performance of RF applications mainly depends on the ground plane design. The often used chip ceramic antennas are very tiny, but they need a proper ground plane to establish a good radiation pattern. Every board design is different and cannot easily be compared to each other. Some practical notes for the ground plane design are described below:

- Regard to the design guideline of the antenna manufacturer
- Use closed ground planes on the PCB edges on top and bottom layer
- Connect the ground planes with lots of vias. Place it inside the PCB like a chessboard and on the edges very closely.

8.4. Layers

The use of 2 or 4 layer boards have advantages and disadvantages for the design of a custom base board.

Table 8-1: 2 and 4 layer board properties in comparison

2 Layer board	4 Layer board
(-) only 2 layers available for routing the traces and design a proper ground area	**(+)** 4 layers available for routing the traces and design a proper ground area
(-) only 1 layer available for routing the traces under the module	**(+)** 3 layers available for routing the traces under the module
(-) no separate VCC plane usable	**(+)** separate VCC plane usable
(+) cheaper than 4 layers	**(-)** more expensive than 2 layers

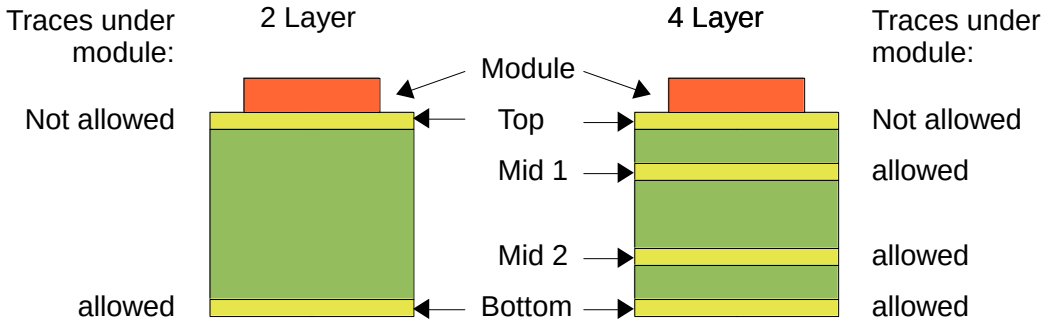


Figure 36: Layer design of 2 and 4 layer boards

8.5. Traces

Common signal traces should be designed with these guidelines:

- Traces on top layer are not allowed under the module (see **Figure 36**)
- Traces on mid layers and bottom layers are allowed (see **Figure 36**)
- Route traces straight away from module (see **Figure 33**)
- Do not use heat traps of components directly on the RF trace
- Do not use 90 degree corners. Better is 45 degree or rounded corners.

The trace design for RF signals has a lot of more important points to regard. It defines the trace impedance and therefore the signal reflection and transmission. The most commonly used RF trace designs are Microstrip and Grounded Coplanar Wave Guide (GCPW). The dimension of the trace is depending on the used PCB material, the height of the material to the next ground plane, a PCB with or without a ground plane, the trace width and for GCPW the gap to the top ground plane. The calculation is not trivial, therefore specific literature and web content is available (see **[3]**)

The reference plane to the GCPW should always be a ground area, that means the bottom layer for a 2 layer design and mid layer 1 for a 4 layer design (see **Figure 37**). Furthermore, it is important to use a PCB material with a known layer stack and relative permittivity. Small differences in the material thickness have a great influence on the trace impedance, especially on 4 layer designs.

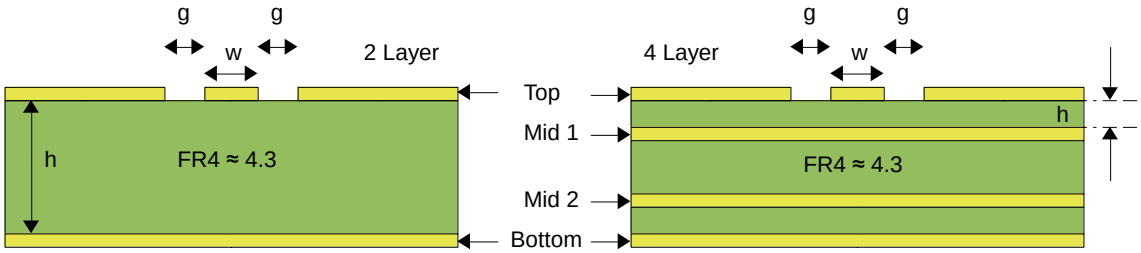


Figure 37: GCPW trace design

8.6. Placement on the PCB

The PCB design of the radio module base board and placement affects the radio characteristic. The radio module with chip antenna should be placed at the edge or side of a base board. The chip antenna should be directed to PCB side.

Figure 38: Placing at the edge

Figure 39: Placing at the center edge

Do not place the chip antenna radio module within the base board. This will effect a very poor radio performance. Instead radio modules with RF pads could be placed everywhere on the PCB. But it should be enough space for routing a RF trace to a coaxial connector or to an onboard antenna.

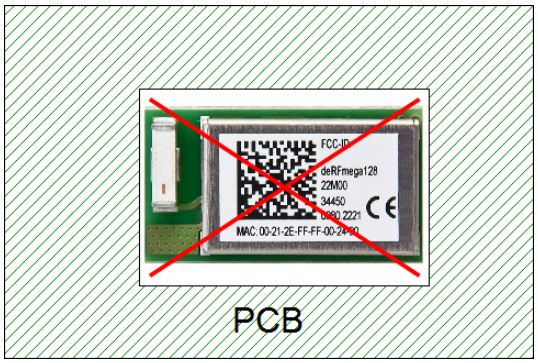


Figure 40: Placing in the center with antenna

Figure 41: Placing in the center with RF pad

Do not place ground areas below the radio module (see **Section 8.4**) and near the chip antenna.

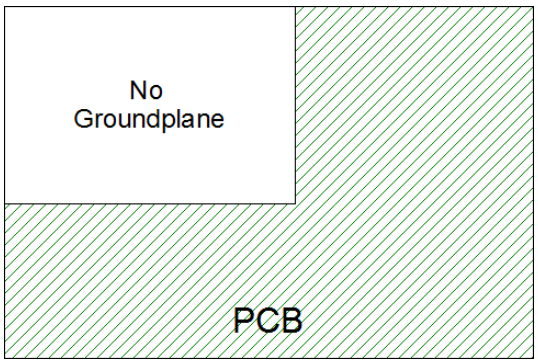


Figure 42: No ground plane under the module

8.7. Reference Design for deRFmega256-23M12

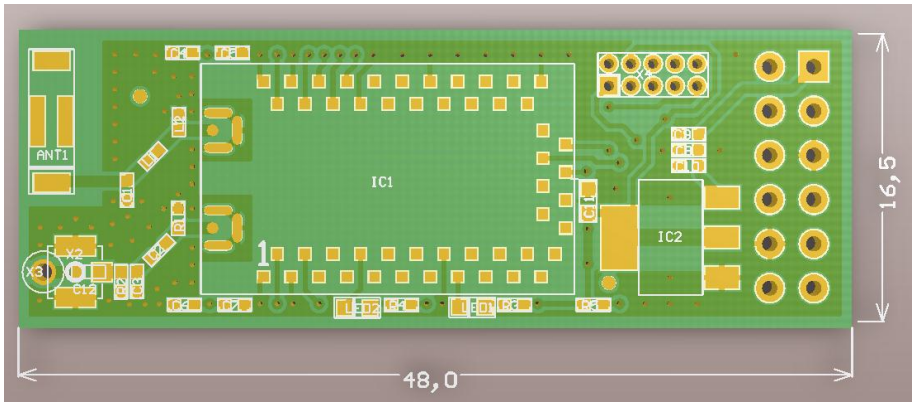
8.7.1. Overview

A reference design allows for a fast design-in of radio modules. Following its recommendations the most RF issues become subsidiary. Even with less or no RF experience it will be possible to get an optimal RF performance of a custom design.

This reference design description must be respected for the use of deRFmega256-23M12 in the United States and to fulfil the requirements of FCC regulations according to the 'Transmitter Module Equipment Authorization Guide' [10]. See chapter 14.1 for further notes of FCC compliance. If the reference design will be integrated into a custom design, it will fulfil the FCC requirements too.

The radio module deRFmega256-23M12 was measured and certified on the reference design board named RaspBee (see Figure 43). Further information on this device can be found in chapter 16. All following design descriptions are based on RaspBee.

Figure 43: Reference design board (RaspBee)

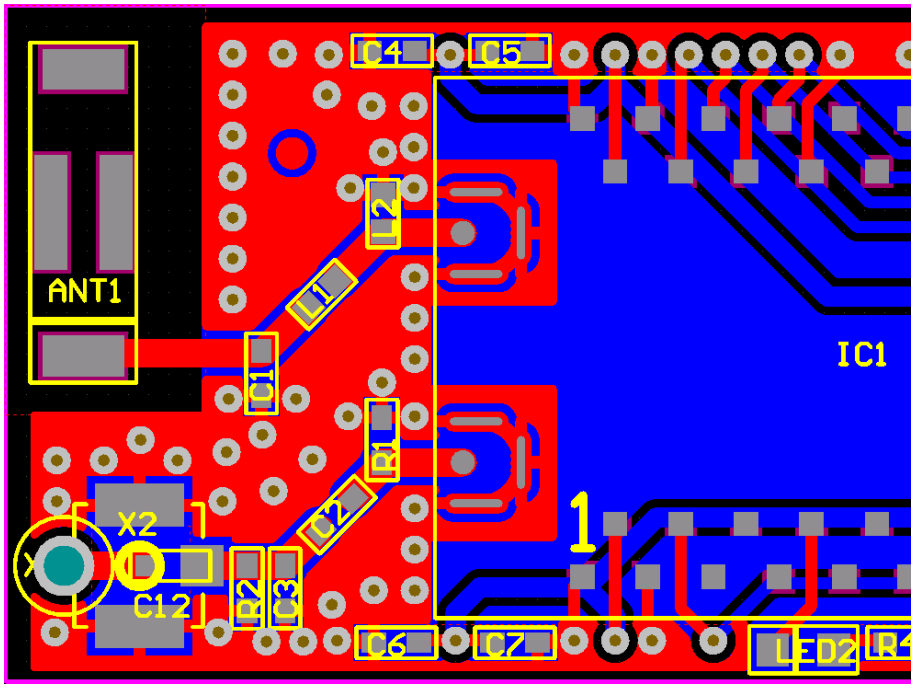


The design guide allows it to create a base board according to the reference board PCB properties. To fulfil the above-mentioned FCC requirements, the RF area of a custom PCB must have the same (design) properties. Any deviation from the reference design will result in a loss of FCC certification of the radio module and the custom design, unless the individual design will be certified again. However re-certification is possible and may be performed as Permissive Change Class II [11]. A partial re-measurement of RF properties is necessary.

> **Note:**
> Please get in contact with us to advise you for a custom FCC certified design. If necessary we will also provide RF part design data.. This may require signing a Non-Disclosure Agreement.

The important area of the reference design is the RF part shown in Figure 44. One RF-OUT pad of the radio module is connected to the chip-antenna and the other RF-OUT pad is connected to a coaxial connector or an optional wire-antenna. It is also permitted to use only one of the both RF outputs, if needed. In this case terminate the unused port with 50ohms to ground.

Figure 44: RF design



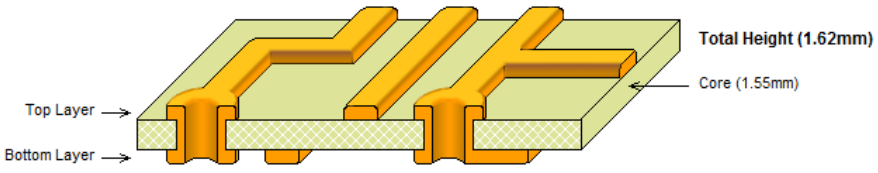
8.7.2. PCB design

The used standard technology PCB has the following properties:

- two-layer board
- board material FR4 TG 135
- dielectric constant 4.4 to 4.8 at 1 MHz
- board thickness of 1.55mm
- copper layer thickness of 35µm
- top and bottom solder
- no silk screen used

If the custom board is a multi-layer board, it is possible to leave blank all inner layers within the RF part to get a two-layer board in this area. Figure 45 shows the layer stack as presented by the PCB design tool.

Figure 45: PCB Layer stack



8.7.3. RF trace design

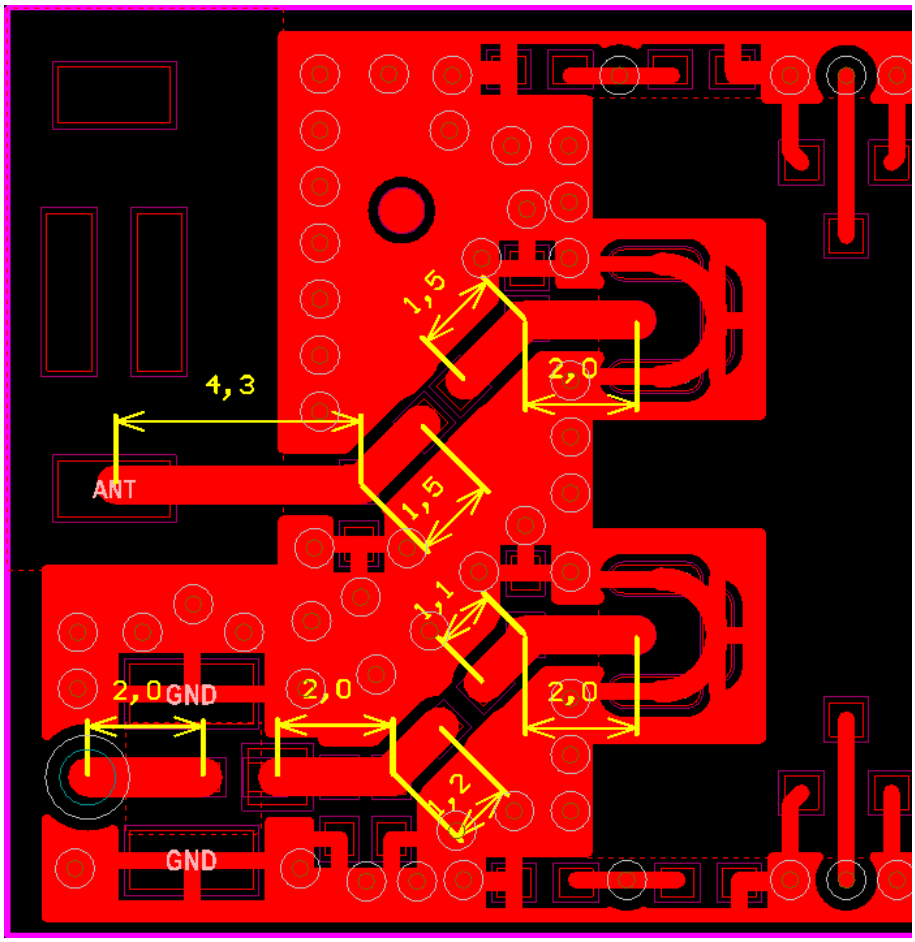
The RF trace is designed as GCPW (see chapter 8.5) with the following properties:

- GCPW width is 0.7mm
- GCPW gap is 0.2mm

Figure 46 shows the RF traces including their length. The middle traces and matching parts are routed in a 45 degree pitch. The PCB design tool defines a traces as a line with a specified width. However the traces have a round edge unlike the measurement start and end point.

If one of the RF traces will not be used, it is necessary to terminate it with 50 ohms to ground. A 49.9 ohms 0402 resistor is applicable.

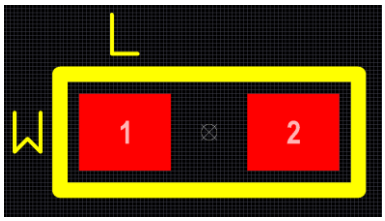
Figure 46: RF trace length



All matching parts are shown in Figure 44 and have a 0402 footprint with these dimensions:

- Pad width is 0.5mm
- Pad length is 0.6mm
- Pad center to center distance is 1.1mm

Figure 47: Pad design 0402



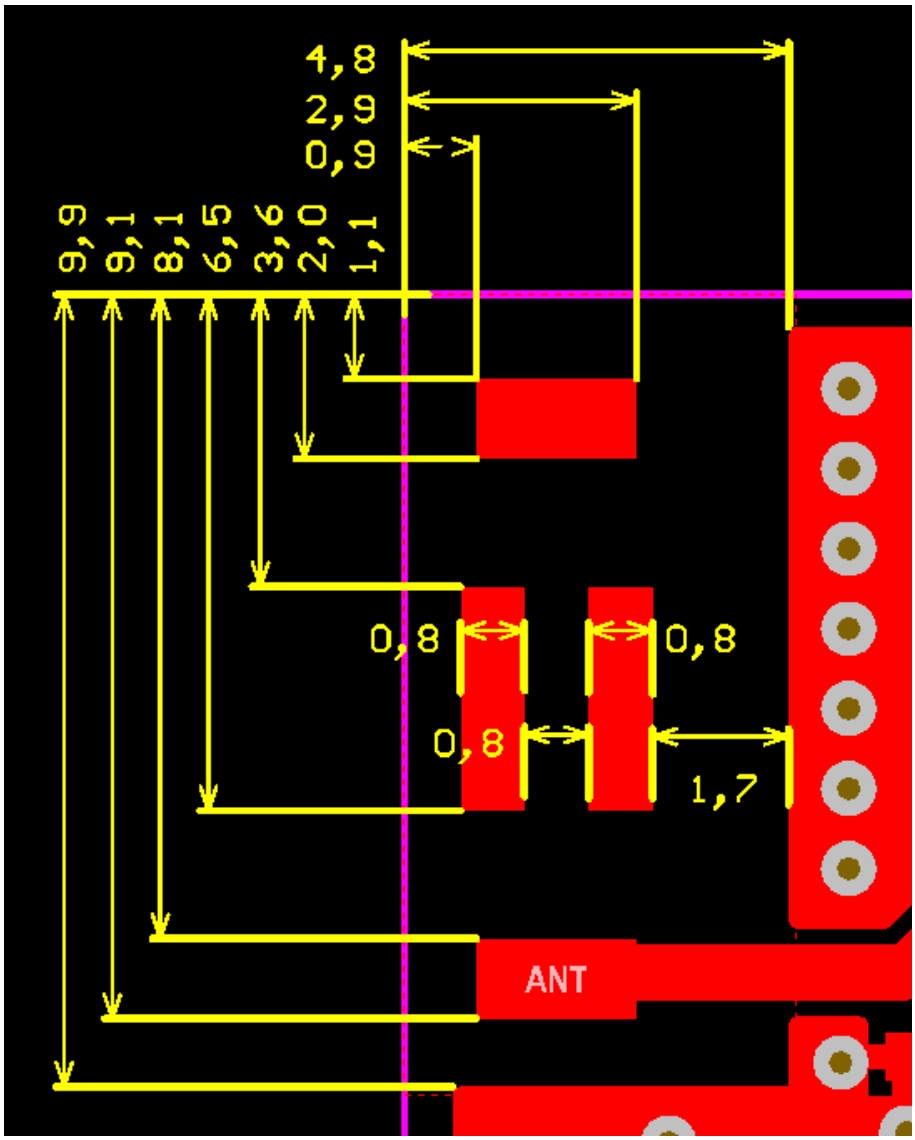
8.7.4. Chip-antenna

The used chip-antenna is optimized for being placed at the PCB edge. Its footprint dimensions are shown in Figure 48. Further details of the used antenna can be found in the manufacturer's datasheets [12]. The used antenna and all matching parts are listed in Table 8-2.

Table 8-2: BOM chip antenna

BOM – Chip antenna and matching parts				
ID	**Value**	**Order code**	**Vendor**	**Comment**
ANT1	-	2450AT43B100	Johanson Technology	
C1	-	-	-	Not assembled
C13	22pF	GRM1555C1H220JZ01D	Murata	
L2	1.5nH	HK10051N5S-T	Taiyo Yuden	

Figure 48: Chip antenna footprint



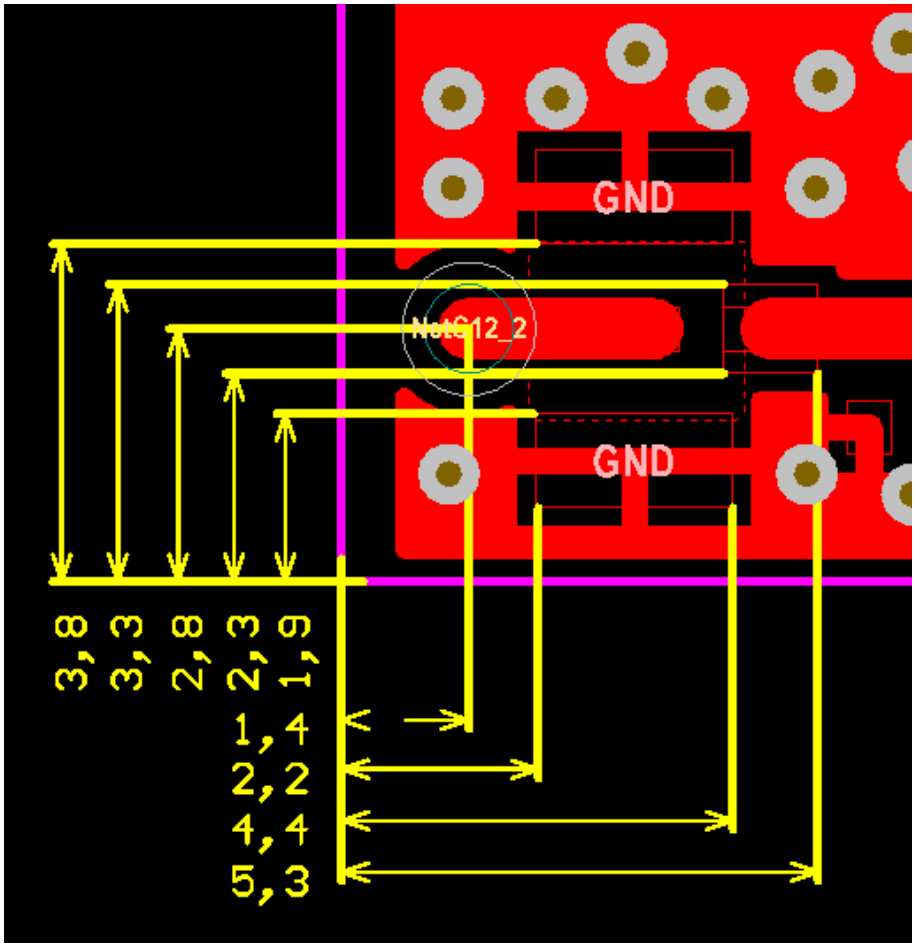
8.7.5. Coaxial connector layout

The coaxial connector allows the connection of an external antenna. It is only allowed to use the approved antennas as listed in chapter 14.3. Figure 49 shows the connector footprint dimensions. Both coaxial connector and matching parts are listed in Table 8-3.

Table 8-3: BOM coaxial connector

BOM – Coaxial connector and matching parts				
ID	**Value**	**Order code**	**Vendor**	**Comment**
X2	-	U.FL-R-SMT-1(10)	Hirose	
R1	49R9	RC1005F49R9CS	Samsung	termination resistor if coax not used, otherwise not assembled
R2	10k	RC10005F1002CS	Samsung	
C2	22pF	GRM1555C1H220JZ01D	Murata	
C3	-	-	-	Not assembled

Figure 49: Coaxial connector and wire antenna footprint



8.7.6. Ground area and vias

The ground area is important to ensure a proper RF radiation and antenna characteristic. Both ground planes on top and bottom layer (highlighted in Figure 50 and Figure 51) must be connected together with sufficient vias. The ground planes should not be separated by other signal traces.

Figure 50: Top ground

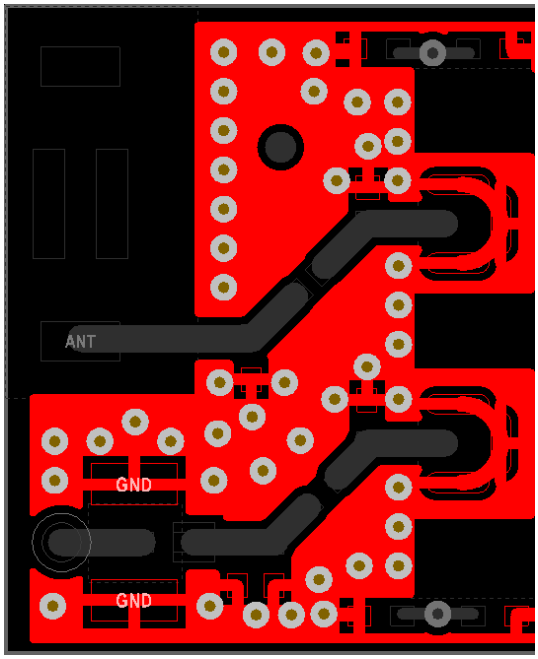
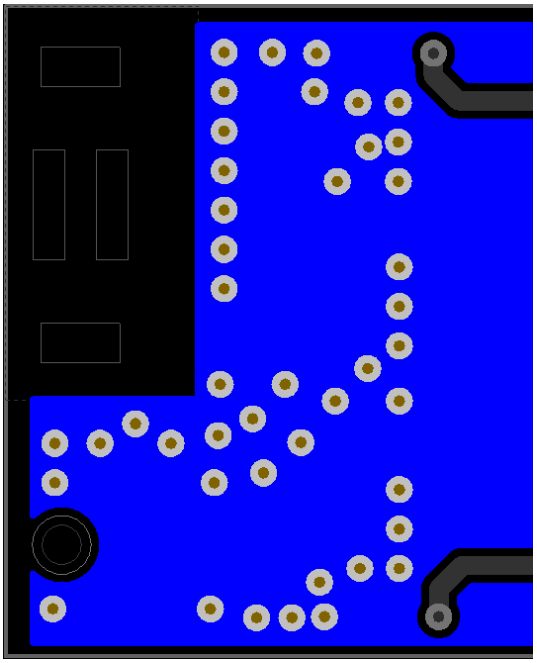


Figure 51: Bottom ground



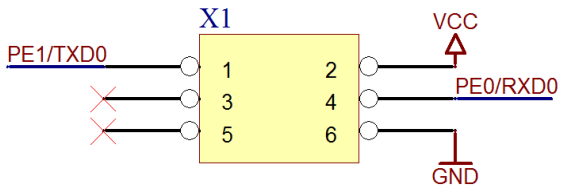
9. Clock

The radio module contains an onboard 32.768 kHz 20 ppm quartz crystal for the MCU and a 16.000 MHz 10 ppm quartz crystal for the internal transceiver. For optimum RF timing characteristics it is necessary to use a low tolerance crystal. The watch crystal clocks a timer, not the processor. The timer is intended to wake-up the processor periodically.

10. Application circuits

10.1. UART

Two U(S)ART interfaces are available on the radio modules. For communication to a host with a different supply voltage domain it is necessary to use a level-shifter. We recommend the USB level shifter by dresden elektronik. The level-shifter can be connected to the custom base board via 100 mil 2 x 3 pin header. The pin assignment should be designed as below in **Figure 52**. For an UART connection it is sufficient to use only TXD, RXD and GROUND signals.

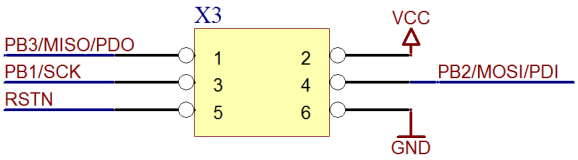


1. PE1/TXD0
2. VCC
3. Not connected
4. PE0/RXD0
5. Not connected
6. GND

Figure 52: 100 mil 2 x 3 pin header for UART0

10.2. ISP

The AVR based radio modules can be programmed via JTAG and ISP interface. For ISP connections a 100 mil 2 x 3 pin header should be used. The pin assignment is given in **Figure 53**. The MCU ATmega128RFA1 uses the ISP signals PDO and PDI on the same pins like the SPI with MISO and MOSI. We recommend the use of an 'AVR ISP programmer'.

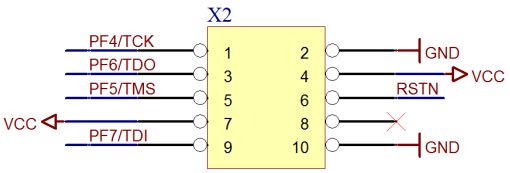


1. PB3/MISO/PDO
2. VCC
3. PB1/SCK
4. PB2/MOSI/PDI
5. RSTN
6. GND

Figure 53: 100 mil 2x3 pin header for ISP

10.3. JTAG

The AVR based radio modules can be programmed via JTAG and ISP interface. For JTAG connections a 100 mil 2 x 5 pin header should be used. The pin assignment is given in **Figure 54**. We recommend the use of 'Atmel AVR Dragon' or 'Atmel JTAG ICE mkII' programmer.



1. PF4/TCK
2. GND
3. PF6/TDO
4. VCC
5. PF5/TMS
6. RSTN
7. VCC
8. Not connected
9. PF7/TDI
10. GND

Figure 54: 100 mil 2x5 pin header for JTAG

10.4. TWI

The connection of external peripherals or sensors via Two-Wire-Interface is possible by using the TWI clock signal PD0/SCL and TWI data signal PD1/SCA. The necessary pull-up resistors must be placed externally on the base board. We recommend the use of 4.7 kΩ resistors as shown in **Figure 55**.

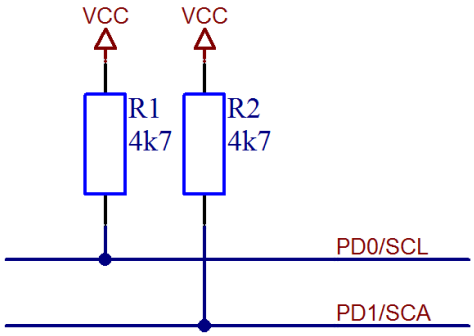


Figure 55: Two-Wire-Interface

10.5. External front-end and antenna diversity

The radio module deRFmega128-22M10 and deRFmega256-23M10 can be connected with an external front-end including power amplifier (PA) for transmission and low noise block (LNA) for receiving. **Figure 56** shows a possible design as block diagram. A custom design can contain a single PA or single LNA or a complete integrated front-end chip. It depends mainly on the application. Furthermore, it is possible to include a RF switch for driving the antenna diversity feature.

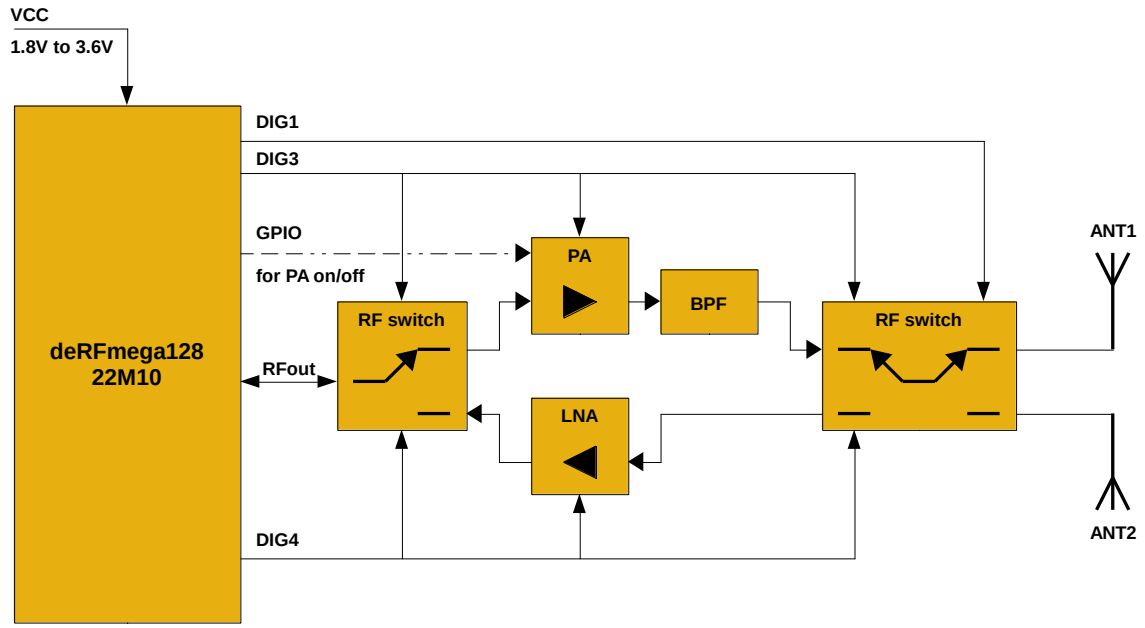


Figure 56: block diagram for external PA/LNA and antenna diversity control

Unbalanced RF output

The radio module 22M10 has a 50 Ω unbalanced RF output. For designs with external RF power amplifier a RF switch is required to separate the TX and RX path.

RF switches to PA, LNA and antenna

The switch must have 50 Ω inputs and outputs for the RF signal. The switch control could be realized with the DIG3 and DIG4 signal of the radio module. Refer to **Section 7.2.1** for detailed information.

PA

The PA has to be placed on the TX path after the RF switch. It is important to regard the PA's manufacturer datasheet and application notes, especially for designing the power supply and ground areas. A poor design could cause a very poor RF performance. For energy efficiency it is useful to activate the PA only during TX signal transmission. In this case the DIG3 signal can be used as switch for (de-)activating the PA. Some PAs have the possibility to set them into sleep state. This application can be realized via a dedicated GPIO pin. Refer to **Section 7.2.1** for more information.

BPF

The use of a band-pass filter is optional. It depends on the PA properties. Some PAs have an internal BPF and other do not have. The BPF is necessary to suppress spurious emissions of the harmonics and to be compliant with national EMI limits. It is possible to use an integrated BPF part or discrete parts. The advantage of the first variant is that the BPF characteristic is known and published in the manufacturer's datasheet.

LNA
The LNA could be used to amplify the received signal. Please regard the manufacturer's datasheet for a proper design. The control could be done by DIG4 signal. Refer to **Section 7.2.1** for more information.

RF switch for antenna diversity
The switch must have 50 Ω inputs and outputs for the RF signal. It is possible to use a separate switch with 2 inputs and 2 outputs or use another (third) switch following the switch required for the PA/LNA. Antenna diversity switching could be controlled via DIG1. Refer to **Section 7.2.1** for more information.

Certification
The customer has to ensure, that custom front-end and antenna diversity designs based on the radio module deRFmega128-22M10 or deRFmega256-23M10 will meet all national regulatory requirements of the assignment location and to have all necessary certifications, device registration or identification numbers.

For long range applications we recommend the use of the deRF-mega128-22M12 radio module which already includes PA, LNA, BPF, RF switches and antenna diversity. This module will be provided by dresden elektronik with certified reference designs for EU and US applications that meet all regulatory requirements and reduce custom design costs.

11. Programming

The programming procedures are described in the documentation Fehler! Verweisquelle konnte nicht gefunden werden., which is online available on dresden elektronik webpage. It describes the update process of the radio module, the required software and hardware for programming via JTAG and the driver installation on different operating systems.
The firmware programming of deRFmega256 radio modules is supported by Atmel Studio 6.

12. Pre-flashed firmware

Actually, the radio modules will be delivered without pre-flashed firmware.

13. Adapter boards

dresden elektronik offers these radio modules already soldered on suitable adapter boards. These boards can be plugged into dresden elektronik's development hardware platforms deRFbreakout Board, deRFnode or deRFgateway. For detailed information please refer to the datasheet **[5]**, **[6]**, **[7]** and **[8]** of the respective adapter board.

Figure 57: deRFmega128-22T00 adapter board with radio module deRFmega128-22M00 / deRFmega256-23M00

Figure 58: deRFmega128-22T02 adapter board with radio module deRFmega128-22M10 / deRFmega256-23M10

Figure 59: deRFmega128-22T13 adapter board with radio module deRFmega128-22M12 / deRFmega256-23M12

14. Radio certification

14.1. United States (FCC)

The deRFmega128-22M00, deRFmega128-22M10, deRFmega128-22M12, deRFmega256-23M00, deRFmega256-23M10 and deRFmega256-23M12 comply with the requirements of FCC part 15. The certification process for deRFmega128-22M10, deRFmega128-22M12, deRFmega256-23M00, deRFmega256-23M10 and deRFmega256-23M12 is pending.

To fulfill FCC Certification requirements, an OEM manufacturer must comply with the following regulations:

The modular transmitter must be labeled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module.

This exterior label can use wording such as the following. Any similar wording that expresses the same meaning may be used.

Sample label for radio module deRFmega128-22M00:

FCC-ID: XVV-MEGA22M00
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Sample label for radio module deRFmega256-23M12:

FCC-ID: XVV-MEGA23M12
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment.

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19). The internal / external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance. This device is approved as a mobile device with respect to RF exposure compliance, and may only be marketed to OEM installers. Use in portable exposure conditions (FCC 2.1093) requires separate equipment authorization.

Modifications not expressly approved by this company could void the user's authority to operate this equipment (FCC section 15.21).

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense (FCC section 15.105).

According to KDB 996369 the radio module deRFmega256-23M12 can only be used with a host antenna circuit trace layout design in strict compliance with the OEM instructions provided in this user manual.

14.2. European Union (ETSI)

The deRFmega128-22M00, deRFmega128-22M10, deRFmega128-22M12, deRFmega256-23M00, deRFmega256-23M10 and deRFmega256-23M12 are conform for use in European Union countries.

If the deRFmega128-22M00, deRFmega128-22M10, deRFmega128-22M12, deRFmega256-23M00, deRFmega256-23M10 and deRFmega256-23M12 modules are incorporated into a product, the manufacturer must ensure compliance of the final product to the European harmonized EMC and low-voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive.

The manufacturer must maintain a copy of the deRFmega128-22M00, deRFmega128-22M10, deRFmega128-22M12, deRFmega256-23M00, deRFmega256-23M10 and deRFmega256-23M12 modules documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a submission must be made to a notified body for compliance testing to all required standards.

The CE marking must be affixed to a visible location on the OEM product. The CE mark shall consist of the initials "CE" taking the following form:

- If the CE marking is reduced or enlarged, the proportions must be respected.
- The CE marking must have a height of at least 5 mm except where this is not possible on account of the nature of the apparatus.
- The CE marking must be affixed visibly, legibly, and indelibly.

More detailed information about CE marking requirements can be found in **[9]**.

14.3. Approved antennas

The deRFmega128-22M00 and deRFmega256-23M00 has an integrated chip antenna. The design is fully compliant with all regulations. The certification process is pending for deRFmega256-23M00.

The deRFmega128-22M10, deRFmega128-22M12 and deRFmega256-23M10 will be tested with external antennas. The approved antenna list will be updated after certification process has finished.

The deRFmega128-22M10 is compliant with the listed approved antennas in Table 14-2.

Table 14-1: Approved antenna list

Approved antenna(s) for deRFmega128-22M10				
Type	**Gain**	**Mount**	**Order code**	**Vendor**
2400 to 2500 MHz Chip ceramic antenna	+1.3dBi (peak)	SMT	2450AT43B100	Johanson Technology

The deRFmega256-23M12 is compliant with the listed approved antennas in Table 14-2.

Table 14-2: Approved antenna list

Approved antenna(s) for deRFmega256-23M12				
Type	**Gain**	**Mount**	**Order code**	**Vendor**
2400 to 2500 MHz Chip ceramic antenna	+1.3dBi (peak)	SMT	2450AT43B100	Johanson Technology
2400 to 2483.5 MHz Rubber antenna	+5dBi (peak)	RP-SMA	17013.RSMA	WiMo

According to KDB 178919 it is allowed to substitute approved antennas through equivalent antennas of the same type:

> ‘Equivalent antennas must be of the same type (e.g., yagi, dish, etc.), must be of equal or less gain than an antenna previously authorized under the same FCC ID, and must have similar in band and out-of-band characteristics (consult specification sheet for cutoff frequencies).’

15. Ordering information

The product name includes the following information:

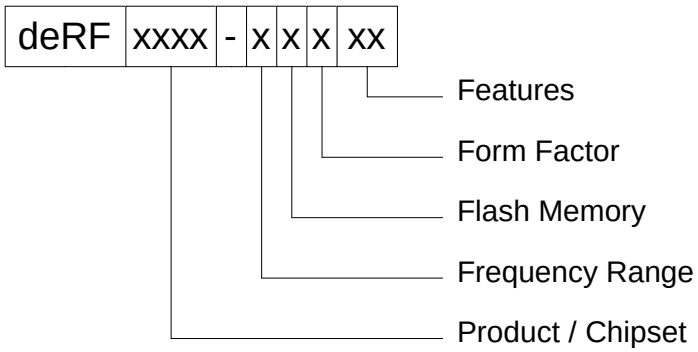


Table 15-1: Product name code

Product name code			
Information	*Code*	*Explanation*	*Comments*
Product / Chipset	mega128	ATmega128RFA1	MCU
	Mega256	ATmega256RFR2	MCU
Frequency Range	2	2.4 GHz	
Flash memory	2	128 kByte	
	3	256 kByte	
Size	M	OEM module	solderable
Features	00	chip antenna	onboard
	10	RFOUT pad	
	12	Internal front-end, Antenna diversity, 2x RFOUT pads	

Table 15-2: Ordering information

Ordering information		
Part number	*Product name*	*Comments*
BN-034491	deRFmega128-22M00	solderable radio module with onboard chip antenna, no pre-flashed firmware
BN-034492	deRFmega128-22M10	solderable radio module with RFOUT pad, no pre-flashed firmware
BN-034368	deRFmega128-22M12	solderable radio module with onboard front-end, antenna diversity RFOUT pads, no pre-flashed firmware
BN-600011	deRFmega256-23M00	solderable radio module with onboard chip antenna, no pre-flashed firmware
BN-600012	deRFmega256-23M10	solderable radio module with RFOUT pad, no pre-flashed firmware
BN-600013	deRFmega256-23M12	solderable radio module with onboard front-end, antenna diversity RFOUT pads, no pre-flashed firmware

16. Related products

RaspBee

The RaspBee is a ZigBee Light Link Addon Board for Raspberry Pi (RPi). This will enhance the application range of RPi with monitoring and controlling ZigBee networks, especially with ZigBee Light Link (ZLL) profile and ZigBee Home Automation (ZHA). ZigBee compatible end-devices and routers from a lot of manufacturers can be added into the network.

Find more information about all related products on our webpage
www.dresen-elektronik.de

17. Packaging dimension

Currently the radio modules are delivered as singular pieces with an appropriate ESD packaging. The delivery as Tape & Reel will be possible for larger amounts but is not yet available.

Further information will be described in this section as Tape & Reel delivery becomes available.

18. Revision notes

Actually, no design issues of the radio modules are known.

All errata of the AVR MCU ATmega128RFA1 are described in the datasheet **[1]**.

All errata of the AVR MCU ATmega256RFR2 are described in the datasheet **[2]**.

19. References

[1] ATmega128RFA1: 8-bit AVR Microcontroller with Low Power 2.4 GHz Transceiver for ZigBee and IEEE802.15.4; Datasheet, URL: http://www.atmel.com

[2] ATmega256RFR2: 8-bit AVR Microcontroller with Low Power 2.4 GHz Transceiver for ZigBee and IEEE802.15.4; Datasheet, URL: http://www.atmel.com

[3] AppCAD Version 3.0.2, RF & Microwave design software, Agilent Technologies; URL: http://www.hp.woodshot.com

[4] User Manual Firmware Update; URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/oem-derfmega/description/?L=0&eID=dam_frontend_push&docID=1917

[5] Datasheet adapter board 22T00 | 22T02, URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/adapter-boards-oem-modules/description/?L=1%252Fproducts%252Fusb-radio-sticks%252Fderfusb-analyzer%252F%253FL%253D1&eID=dam_frontend_push&docID=1816

[6] Datasheet adapter board 22T13, URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/adapter-boards-oem-modules/description/?L=1%252Fproducts%252Fusb-radio-sticks%252Fderfusb-analyzer%252F%253FL%253D1&eID=dam_frontend_push&docID=1818

[7] Datasheet adapter board 23T00 | 23T02, URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/adapter-boards-oem-modules/description/?L=1&eID=dam_frontend_push&docID=1859

[8] Datasheet adapter board 23T13, URL: http://www.dresden-elektronik.de/funktechnik/products/radio-modules/adapter-boards-oem-modules/description/?L=1&eID=dam_frontend_push&docID=1861

[9] Directive 1999/5/EC, European Parliament and the Council, 9 March 1999, section 12

[10] Transmitter Module Equipment Authorization Guide; 996369 D01 Module Certification Guide; FCC OET; URL: https://apps.fcc.gov/oetcf/kdb/forms/FTSSearchResultPage.cfm?id=44637&switch=P

[11] Permissive Change Policy; 178919 D01 Permissive Change Policy); FCC OET; URL: https://apps.fcc.gov/oetcf/kdb/forms/FTSSearchResultPage.cfm?id=33013&switch=P

[12] 2.4GHz Chip-Antenna 2450AT43B100 by JOHANSON TECHNOLOGY; Datasheet; URL: http://www.johansontechnology.com/datasheets/antennas/2450AT43B100.pdf

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