TN1274
Technical note

Migration differences between SPC584Bx and SPC560B64

Introduction

The SPC560B54/6x family expands the range of the SPC560B microcontroller family. It provides the scalability needed to implement platform approaches and delivers the performance required by increasingly sophisticated software architectures. The advanced and cost-efficient host processor core of the SPC560B54/6x automotive controller family complies with the Power Architecture™ embedded category, and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It also capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations. The SPC584Bx belong to a wide family of automotive microcontroller products which offers the scalability needed to implement platform approaches and delivers the performance and features required by increasingly sophisticated body applications. It is available as single or symmetrical dual core and operates at speeds of up to 180 MHz enabling the customer to adjust the performance and consumption to the application needs.

The versatile low power modes available on SPC56 body MCU have been extended with a Smart Standby Wake-up Unit reducing further the average consumption in low power conditions.

A large variety and number of communication interfaces like ISO CAN-FD, Ethernet with AVB are available as well as new features for security (HSM) and safety (ASIL-B) requirements.

This document focuses between the differences across the SPC584Bx family, and SPC560B64 family.

For the latter, we will refer to the best so far product to highlight the differences with SPC584Bx. Both devices are ASIL-B compliant.

Contents

List of tables

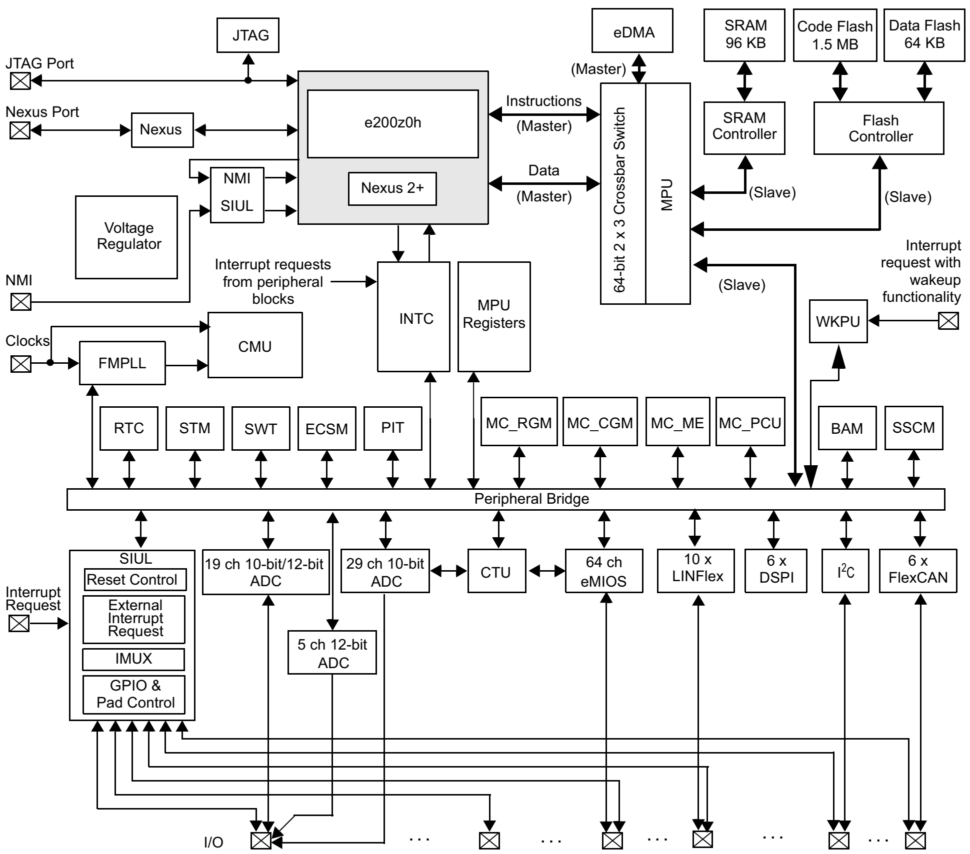
List of figures

1 Block diagrams

1.1 Comparison between block diagrams

In *Figure 1* and *Figure 2* are reported the two block diagrams of the SPC560B64 and SPC584Bx.

Figure 1. SPC560B64 block diagram

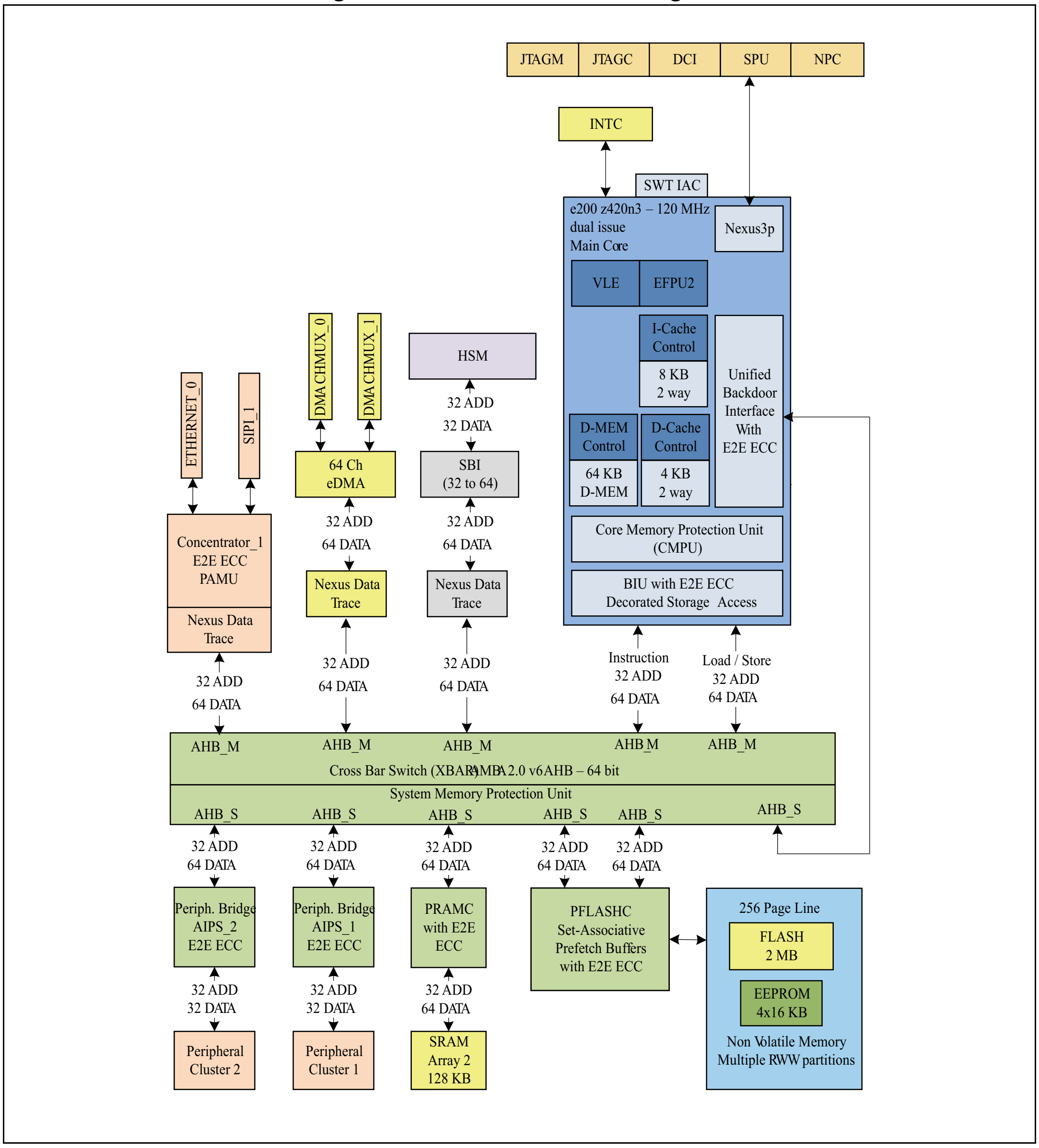


Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
ECSM	Error Correction Status Module
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
Flash	Flash memory
FlexCAN	Controller Area Network
FMPLL	Frequency-Modulated Phase-Locked Loop
GPIO	General-purpose input/output
I^2C	Inter-Integrated Circuit bus
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)

MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
MPU	Memory Protection Unit
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
VREG	Voltage regulator
WKPU	Wakeup Unit
XBAR	Crossbar switch

Figure 2. SPC584Bx block diagram



2 Overview

2.1 Features

Table 1 shows an overview of the features set of the two products. A more detailed description of the differences between the two devices and of the migration from SPC560B64 to SPC584Bx is given in the next sections.

Table 1. Overview of main features and differences

Features	SPC584Bx	SPC560B64
Core/Platform		
Core number	1xz4	1xz0
Core 0	Z420n3	Z0
Core MPU	24 regions/core	8 regions/core
System MPU	24 regions/xbar	8 regions
Memory		
Ram size	64K	96K
Standby ram (max/min)	64K/8K	32K/8K
Code Flash	2M (2 x RWW partition)	1.5M
Data Flash	64K (4x16K)	64K (4x16K)
I/O		
I/O state during and out of reset	High-Z	High-Z
Debug		
LFast	1 x JTAG	1 x JTAG
Trace interface	Nexus	Nexus
Class	3+	1 (2+ for LBGA208)
Clock		
Max Freq.	120MHz	64MHz
Clock source (fast)	IRCOSC / XOSC / PLLx	IRCOSC / XOSC / PLLx
Clock source (slow)	SIRC/SXOSC	SIRC/SXOSC
System		
INT_CTLR	1 x INTC	1 x INTC
DMA	1 x 16ch	1x16ch
STM	1	1
PIT	6	8
Communication I/F		
LIN	14 x LinFlex	10 x LinFlex
CAN	8 x ISOMCAN-FD	6 x FlexCAN

Table 1. Overview of main features and differences (continued)

Features	SPC584Bx	SPC560B64
I2C	Yes	Yes
DSPI	7	6
Timed I/O		
eMIOS	2 x 32ch	2 x 32ch
CTU	64ch	64ch
ADC		
SARADC (12bit)	64ch (1x 12-bit /1x 12-bit supervisor / 1x 10-bit STBY)	53 ADC (1x 10-bit/ 1x 12-bit)
Low Power		
Low Power Modes	HALT/STOP/STANDBY	HALT/STOP/STANDBY
RTC/API	1	1
SSWU	Yes	No
Safety		
ASIL level	ASIL-B	ASIL-B
FCCU	1	No
CRC	2 x 4ch	No
MBIST	On RAM and FLASH	no

2.2 Supply and packages

Table 2. Overview of supply and packages features and differences

Features	SPC584Bx	SPC560B64
Supply		
High voltage	3.3 or 5V	3.3 or 5V
Low voltage	Internal	Internal
Ballast	Internal	Internal
Package		
	QFN32 / eTQFP64 / eLQFP100	eLQFP64 / 100 / 144 / LBGA208(emulation package)
Temperature		
	-40°C +105°C/+125°C	-40°C +105°C/+125°C

3 Core/Platform

3.1 Cores

The SPC584Bx has a High performance 120 MHz e200z420 single core with:

- 32-bit Power Architecture technology CPU
- Core frequency as high as 120 MHz
- Hardware Security Module (HSM)
- Variable Length Encoding (VLE)
- Floating Point, End-to-End Error Correction

The SPC560B64 has a high-performance 64 MHz e200z0h CPU with:

- 32-bit Power Architecture® technology
- Up to 60 DMIPs operation
- Variable length encoding (VLE)

3.2 MPU (Memory Protection Unit)

The MPU sits on the slave side of the XBAR and allows highly configurable control over all master accesses to the memory.

SPC584Bx has 24 regions per core, SPC560B64 has 8 regions.

3.3 Interrupt controller (INTC)

Both devices furnishes one INTC.

INTC for SPC584Bx has the following features:

- Each peripheral interrupt source is software-steerable to processor 0
- 32 software-settable interrupt request sources
- 10-bit vector
  - Unique vector for each interrupt request source
  - Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 64 priorities
- Each interrupt source can be triggered by software
- Preemption
  - Preemptive prioritized interrupt requests to processor
  - ISR with higher priority preempts ISRs or tasks with lower priorities
  - Automatic pushing or popping of preempted priority to or from a LIFO
  - Ability to modify the ISR or task priority; modifying the priority can be used to
  - implement the Priority Ceiling Protocol for accessing shared resources
  - 3 INTC clock cycles from interrupt request into interrupt request to CPU
- Low latency
  - 3 INTC clock cycles from receipt of interrupt request from peripheral to interrupt
  - request to processor; four clock cycles from receipt of software request

INTC for SPC560B64 has the following features:

- Supports 196 peripheral and 8 software
- configurable interrupt request sources
- Unique 9-bit vector per interrupt source
- Each interrupt source can be programmed to one of 16 priorities
- Preemption
  - Preemptive prioritized interrupt requests to processor
  - ISR at a higher priority preempts ISRs or tasks at lower priorities
  - Automatic pushing or popping of preempted priority to or from a LIFO
  - Ability to modify the ISR or task priority; modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- Low latency
  - 3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

4 Memory

4.1 Ram controller

Both devices have one ram controller, the SPC584Bx one has size 64K, the SPC560B64 one has size 96K.

The difference between the two is that the SPC584Bx provides End-to-end Error Correction Code (e2eECC), instead the SPC560B64 provides traditional ECC.

This e2eECC is structurally different to traditional “ECC at memory” functionality

because it provides robust error detection capabilities from one endpoint of an information

transfer to another endpoint, with temporary information storage in one or more intermediate

components. Memory protected by ECC/EDC traditionally generates and checks additional error parity information local to the memory unit to detect or correct errors that have occurred on data stored in the memory, or both. On the other hand, e2eECC generates error protection codes at the source of data generation.

4.2 Ram size

Both devices have one ram controller, the SPC584Bx one has size 64K, the SPC560B64 one has size 96K.

Standby Ram (Max/Min) is 64K/8K for SPC584Bx series and 32K/8K for SPC560B64 series.

4.3 Flash controller

Table 3 summarizes the differences between flash controllers available in SPC584Bx and SPC560B64.

Table 3. Flash controller comparison between SPC584Bx and SPC560B64

Parameter/Feature	SPC584Bx	SPC560B64
N. of flash controller ports connected to the XBAR slave ports	2	1
AHB data bus width	64	32
Flash write data bus width	256	32

Table 3. Flash controller comparison between SPC584Bx and SPC560B64 (continued)

Parameter/Feature	SPC584Bx	SPC560B64
Flash read data bus width	64	128
Buffer	read buffering and line prefetching support via 4-entry, 2-way set associative mini-cache plus prefetch controller per AHB port to provide single-cycle “buffer hit” read response	four-entry “page” buffer, each entry containing 128 bits of data plus an associated controller which prefetches sequential lines of data from the flash memory array into the buffer (code flash) + 128-bit register which serves as a temporary page holding register and does not support any prefetching (data flash)

4.4 Code and Data Flash

Both devices provide 64k of data flash, 4x16K banks.

Table 4. Main differences between SPC584Bx and SPC560B64 Flashes

	SPC584Bx	SPC560B64
Code Flash size	2M	1.5M
Error Correction Code	Double Error Correction, Triple Error Detection	Single Error Correction (SEC), Double Error Detection (DED)
Read-While-Modify	Yes	No
Programming during Erase-Suspend	Yes	No
UTEST mode	Yes	No
Protection Strategy	Test Mode Disable	Censored Mode against piracy

5 Reset and boot modes

5.1 MC_RGM (Reset Generation Module)

The reset generation module (MC_RGM) centralizes the different reset sources and manages the reset sequence of the device. It provides a register interface and the reset sequencer.

Figure 3. SPC560B64 Reset Generation Module

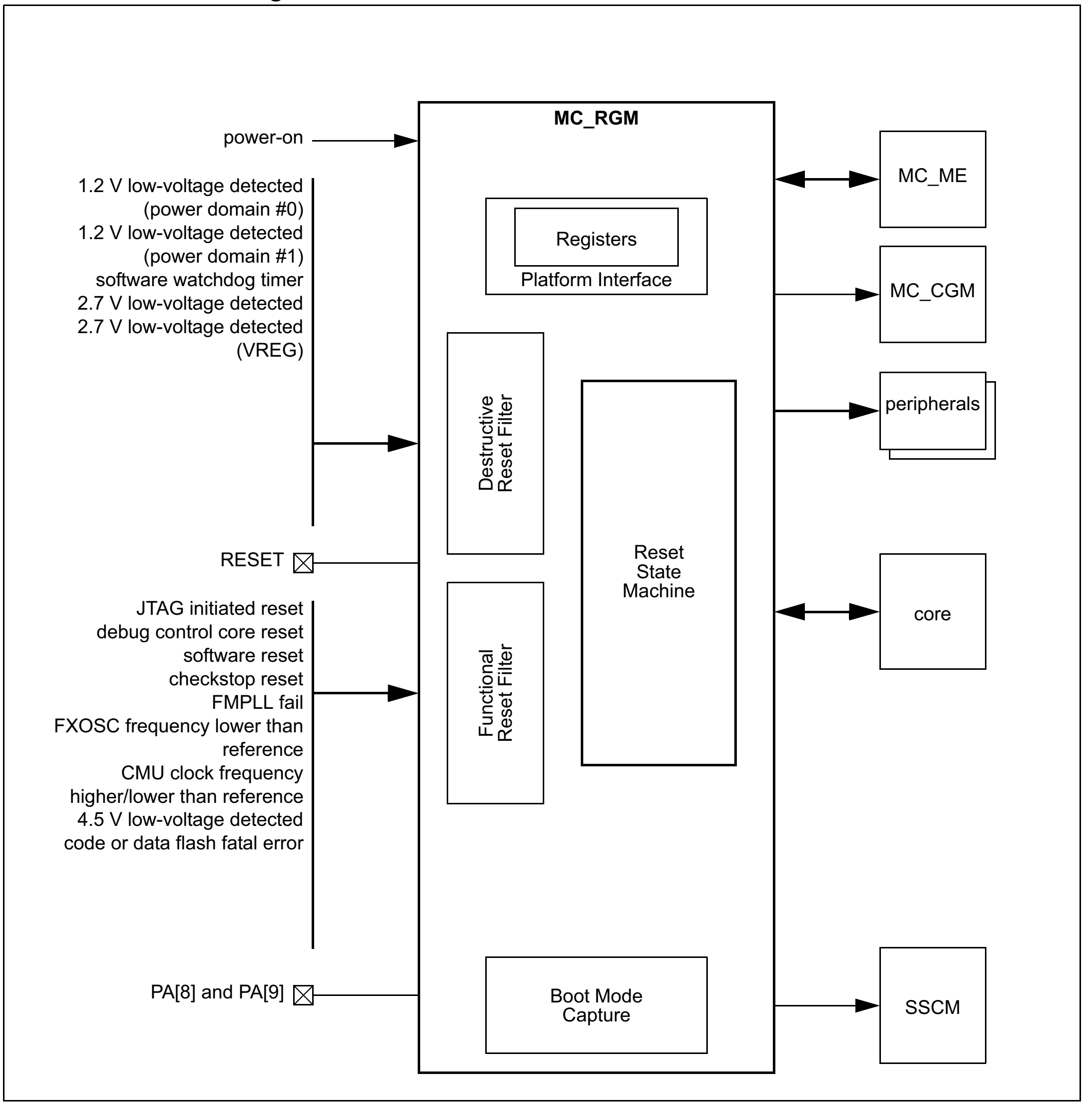
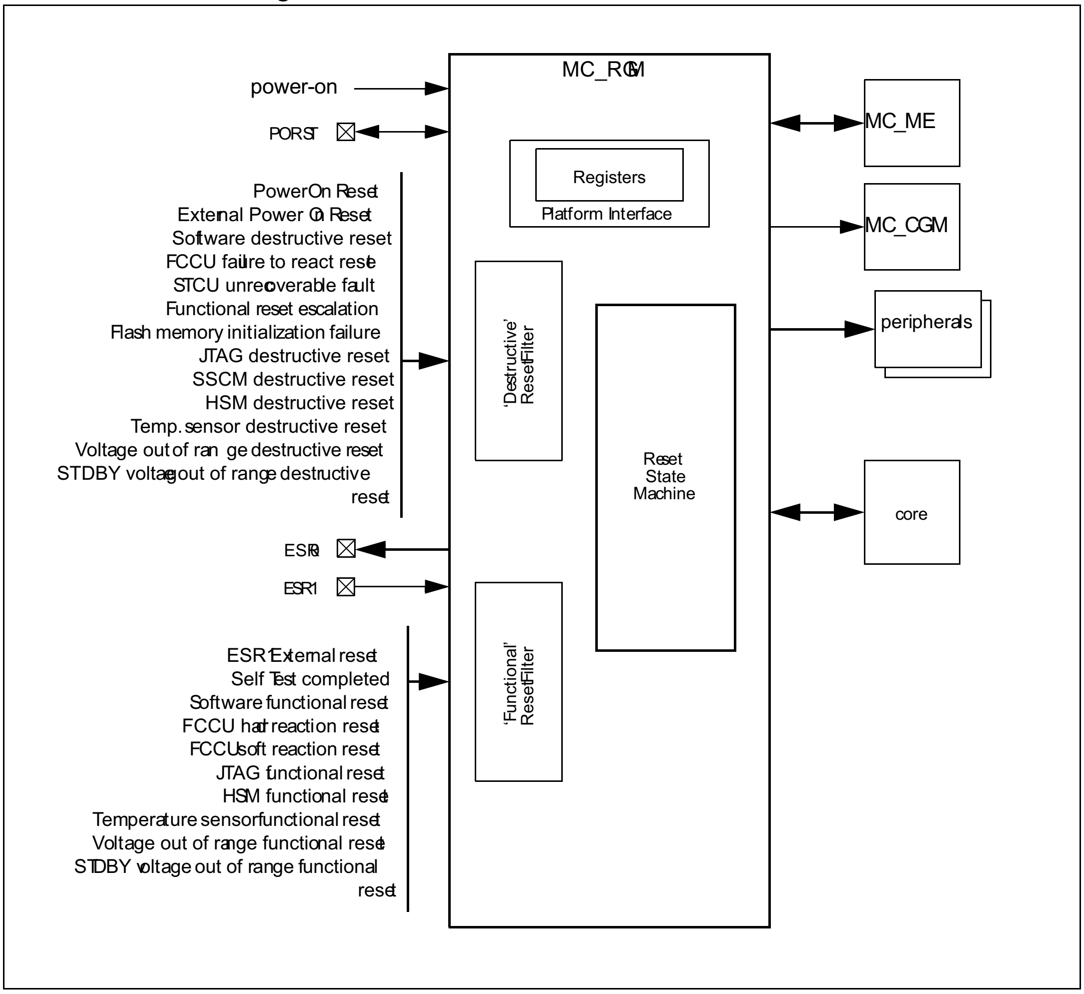


Figure 4. SPC584Bx Reset Generation Module



MC_RGM main common features:

- ‘Destructive’ resets management
- ‘Functional’ resets management
- Signaling of reset events after each reset sequence (reset status flags)
- Conversion of reset events to SAFE mode or interrupt request events (for further mode details, please see the MC_ME chapter)
- Short reset sequence configuration
- Bidirectional reset behavior configuration

SPC560B64 MC_RGM provides also:

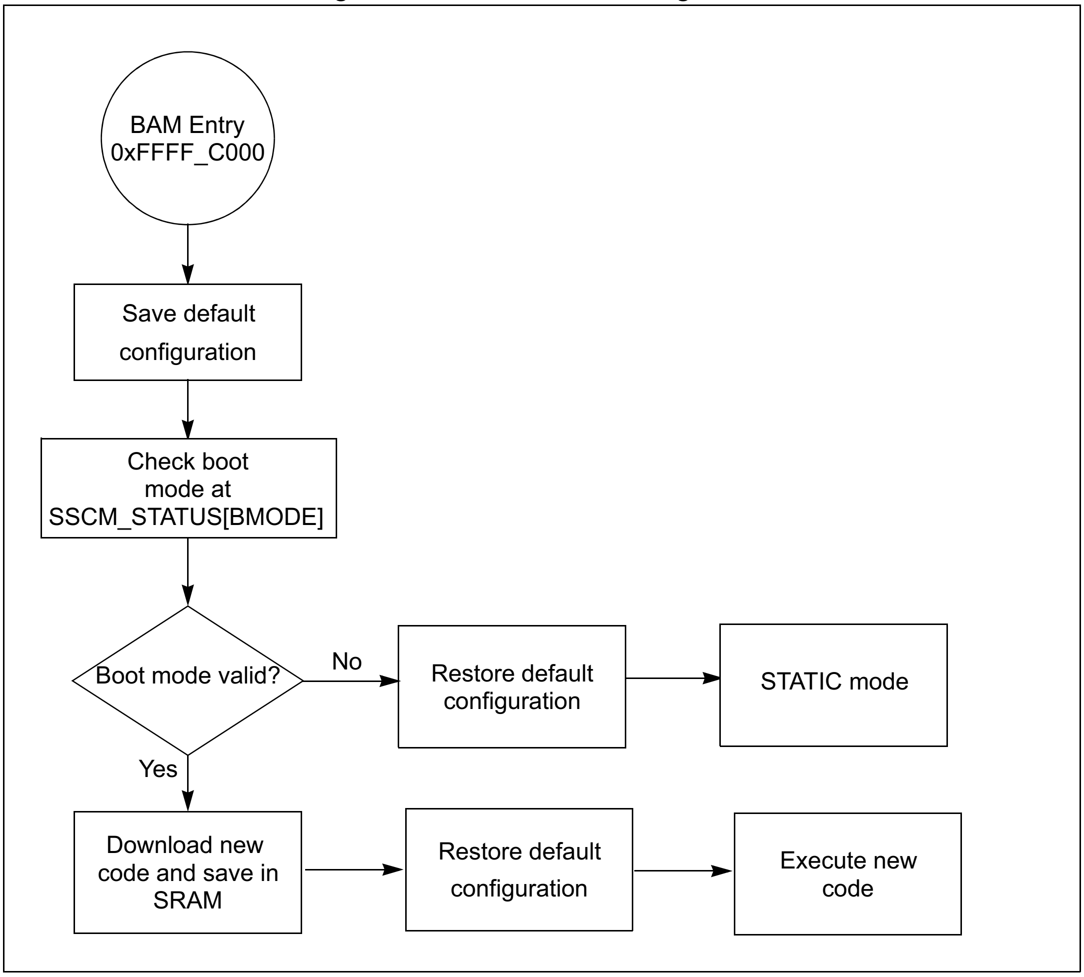
- Selection of alternate boot via the backup SRAM on STANDBY mode exit (for further mode details, please see the MC_ME chapter)
- Boot mode capture on RESET deassertion

5.2 BAM (Boot Assist Module) for SPC560B64

The BAM consists of a block of ROM at address 0xFFFF_C000 containing VLE firmware. The BAM provides two main functions:

- Manages the serial download (FlexCAN or LINFlexD protocols supported) including support for a serial password if censorship is enabled
- Places the microcontroller into static mode if flash memory boot mode is selected and a valid BOOT_ID is not located in one of the boot sectors by the SSCM

Figure 5. SPC560B64 BAM logic flow



The initial (reset) device configuration is saved including the mode and clock configuration. This means that the serial download software running in the BAM can make changes to the modes and clocking and then restore these to the default values before running the newly downloaded application code from the SRAM.

The SSCM_STATUS[BMODE] field indicates which boot mode is to be executed. This field is only updated during reset.

There are two conditions where the boot mode is not considered valid and the BAM pushes the microcontroller into static mode after restoring the default configuration:

- BMODE = 011 (flash memory boot mode). This means that the SSCM has been unable to find a valid BOOT_ID in the boot sectors so has called the BAM
- BMODE = reserved

In static mode a wait instruction is executed to halt the core.

For the FlexCAN and LINFlexD serial boot modes, the respective area of BAM code is executed to download the code to SRAM.

5.3 BAF (Boot Assist Flash) for SPC584Bx

The BAF code is programmed by ST. The two main tasks of BAF are to provide a serial

bootloader feature and to search for the application entry point. The BAF is executed via the IRCOSC as clock source.

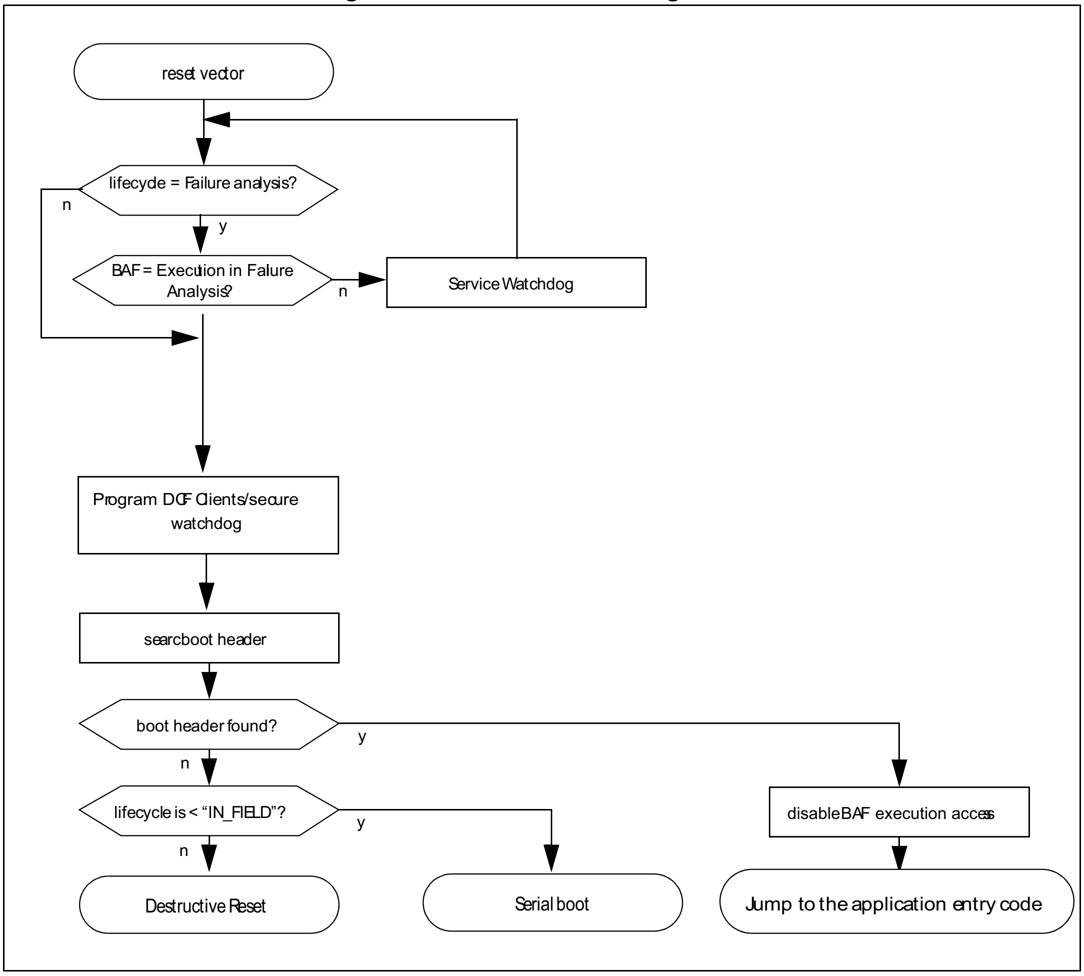
The MCU is booted through a collaboration of several blocks, hardware and firmware. The first boot phases are performed by a state machine inside the System Status and

Configuration Module (SSCM). Once completed, the SSCM sends a reset vector to the HW boot core of the device pointing into the Boot Assist Flash (BAF).

The BAF code then checks the life cycle of the device. If it is FAIL_ANALYSIS, the BAF

enters a loop in which it services the watchdog. Otherwise, it searches for a boot header and boots the application code in internal flash memory.

Figure 6. SPC584Bx BAF logic flow



6 Clocking

6.1 Clock architecture

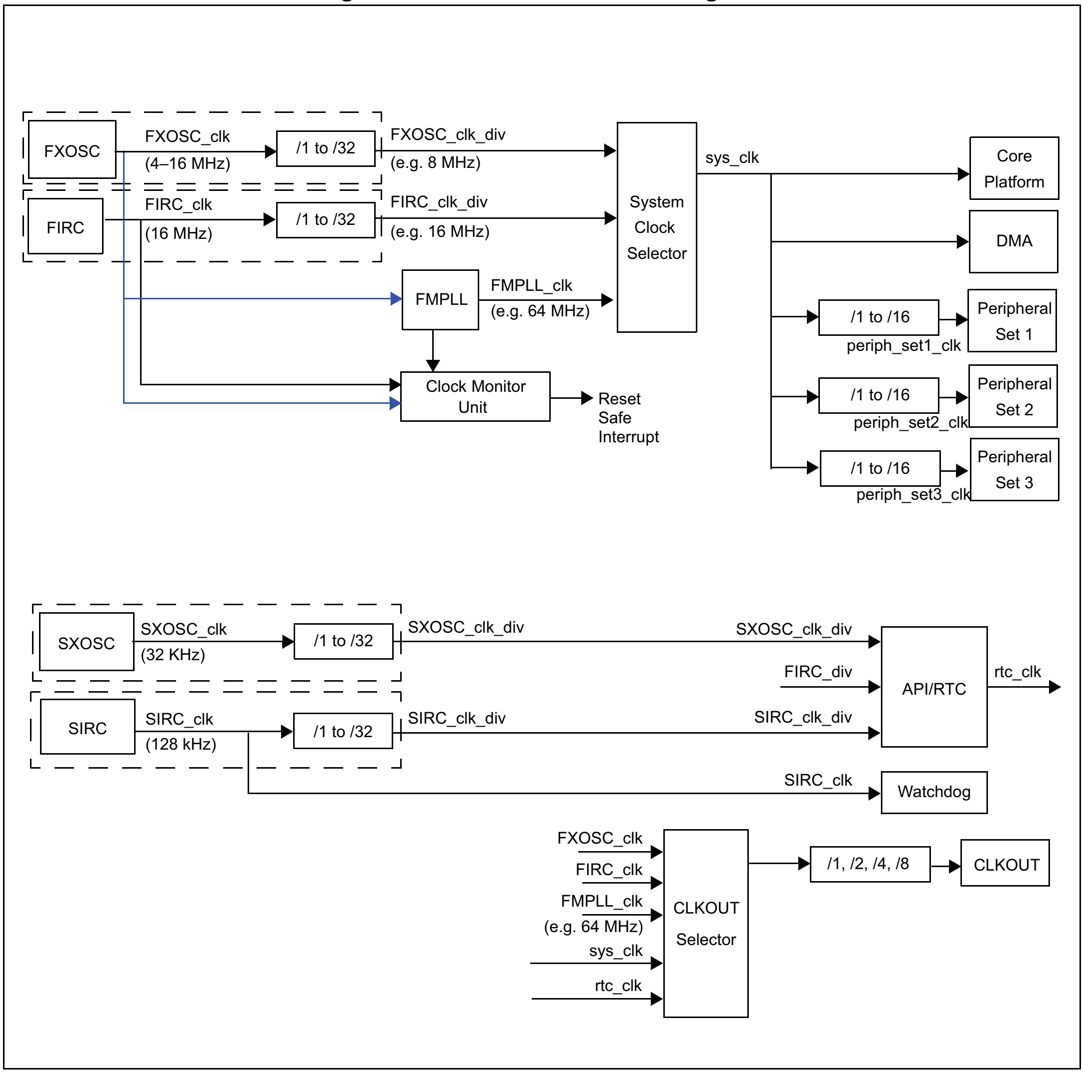
System clock for SPC560B64 is generated from three sources:

- Fast external crystal oscillator 4-16 MHz (FXOSC)
- Fast internal RC oscillator 16 MHz (FIRC)
- Frequency modulated phase locked loop (FMPLL)

Additionally, there are two low power (slow) oscillators:

- Slow internal RC oscillator 128 kHz (SIRC)
- Slow external crystal oscillator 32 KHz (SXOSC)

Figure 7. SPC560B64 clock diagram

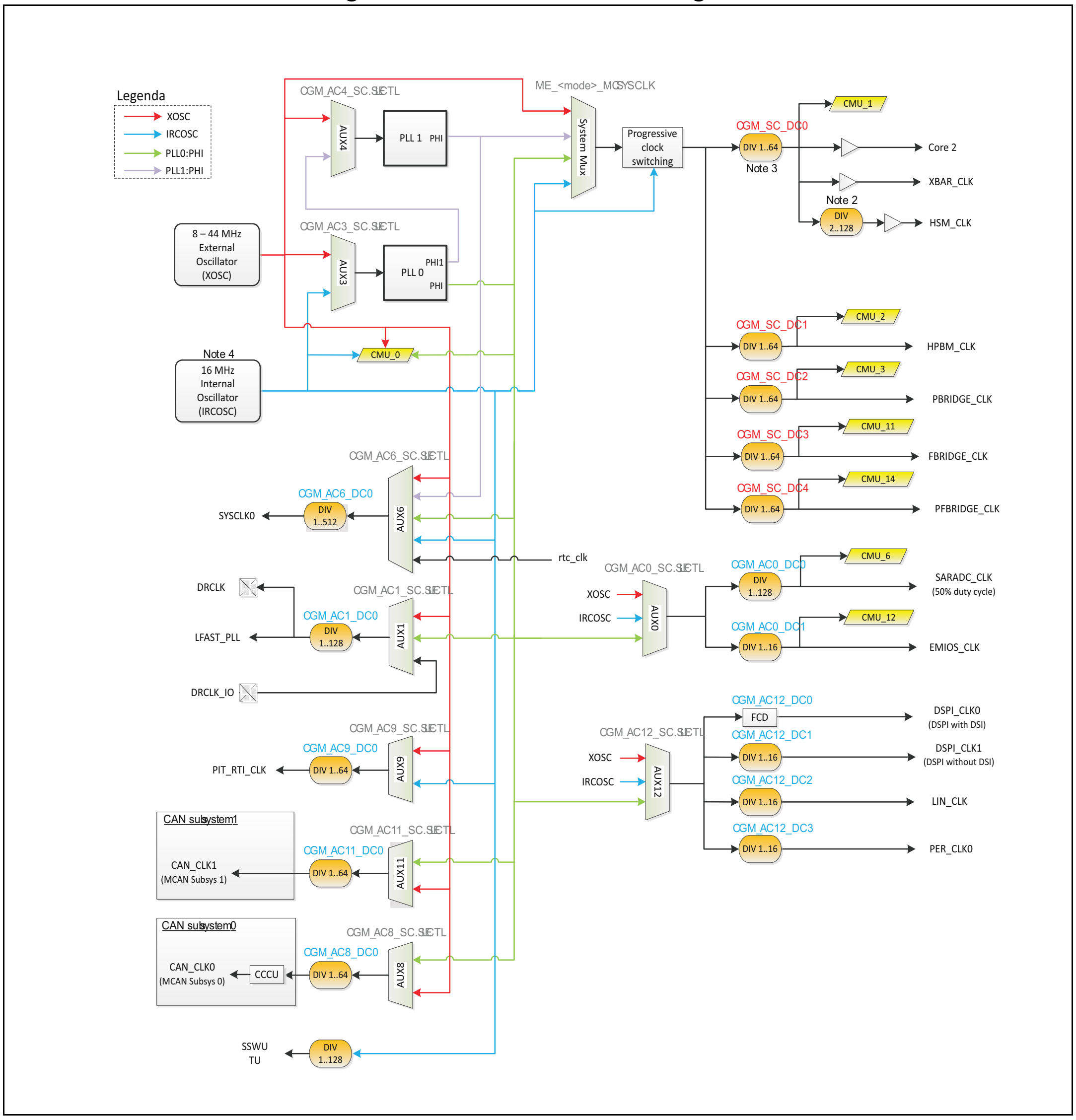


System clock for SPC584Bx is generated from three sources also:

- External oscillator/crystal (XOSC)
- Internal 16 MHz RC oscillator (IRCOSC)
- Frequency modulated phase locked loop (FMPLL)

Additionally there is the Slow internal RC oscillator 128 kHz (SIRC) as low power (slow) clock source.

Figure 8. SPC584Bx clock diagram



6.2 RTC/API (Real Time Clock / Autonomous Periodic Interrupt)

The RTC is a free running counter used for time keeping applications. The RTC may be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low power mode). The RTC also supports an autonomous periodic interrupt (API) function which can be used to generate a periodic event to the wakeup unit or an interrupt request.

Both devices have one RTC/API, with the following different features in terms of counter clock sources.

Table 5. RTC/API differences between SPC584Bx and SPC560B64 devices

	SPC584Bx	SPC560B64
N. of counter clock sources	2	2
Type of counter clock sources	LPRC prescaled by 8 (128 kHz) IRCOSC (16 MHz)	SIRC (128 kHz) SXOSC (32 KHz) FIRC (16 MHz)

7 System

7.1 STM

Both devices provide one System Timer Module, with a difference regarding the clock source in charge to drive it.

SPC584Bx STM is driven by FBRIDGE clock divided by an 8bit prescale value; SPC560B64 STM is driver by the system clock divided by an 8bit prescale clock.

Here are the full feature, common to both:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

8 Debug

8.1 Nexus interface

Both devices support Nexus interface.

SPC584Bx has a Nexus Class 3+, the SPC560B64 has a Class 1 except for LBGA208 (emulation package) which provides the Class 2+

9 Communication I/F

9.1 LIN

SPC584Bx contains 6 Linflex, SPC560B64 contains 4 LinFlex.

The first one are dma capable, the second one are not dma capable.

Table 6. Lin difference between SPC584Bx and SPC560B64 devices

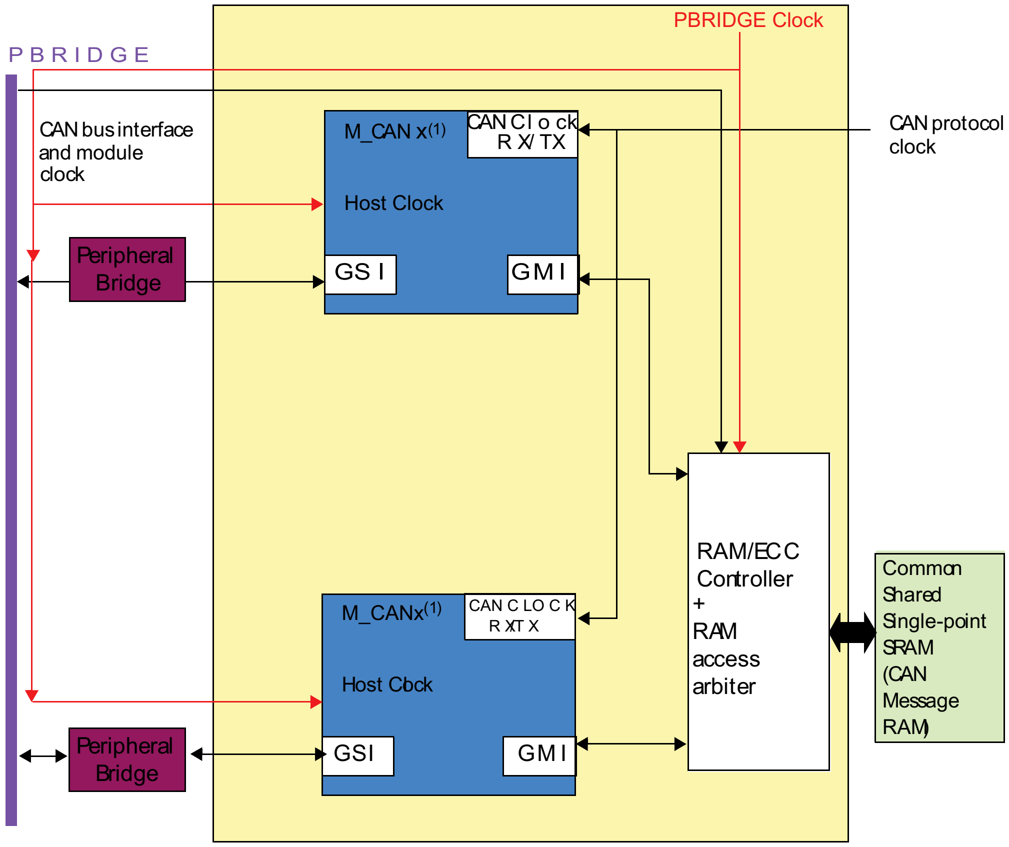
	SPC584Bx	SPC560B64
N. of Linflex	14	10
Protocol version	version 1.3, 2.0, 2.1 and 2.2	versions 1.3, 2.0, 2.1, and J2602
Timeout management	Yes	No
Separate clock for baud rate calculation	Yes	No

9.2 CAN

SPC584Bx has two CAN subsystem implemented:

- CAN Subsystem 0
- CAN Subsystem 1

Figure 9. CAN subsystem for SPC584Bx



1: Number of M_CAN nodes (M_CANx) varies per device. Please refer to Device Configuration chapter to see the number of M_CAN nodes used in the device.

Features:

The CAN subsystem consists of the following major blocks:

- Modular CAN cores: The registers of the CAN module can be accessed using the

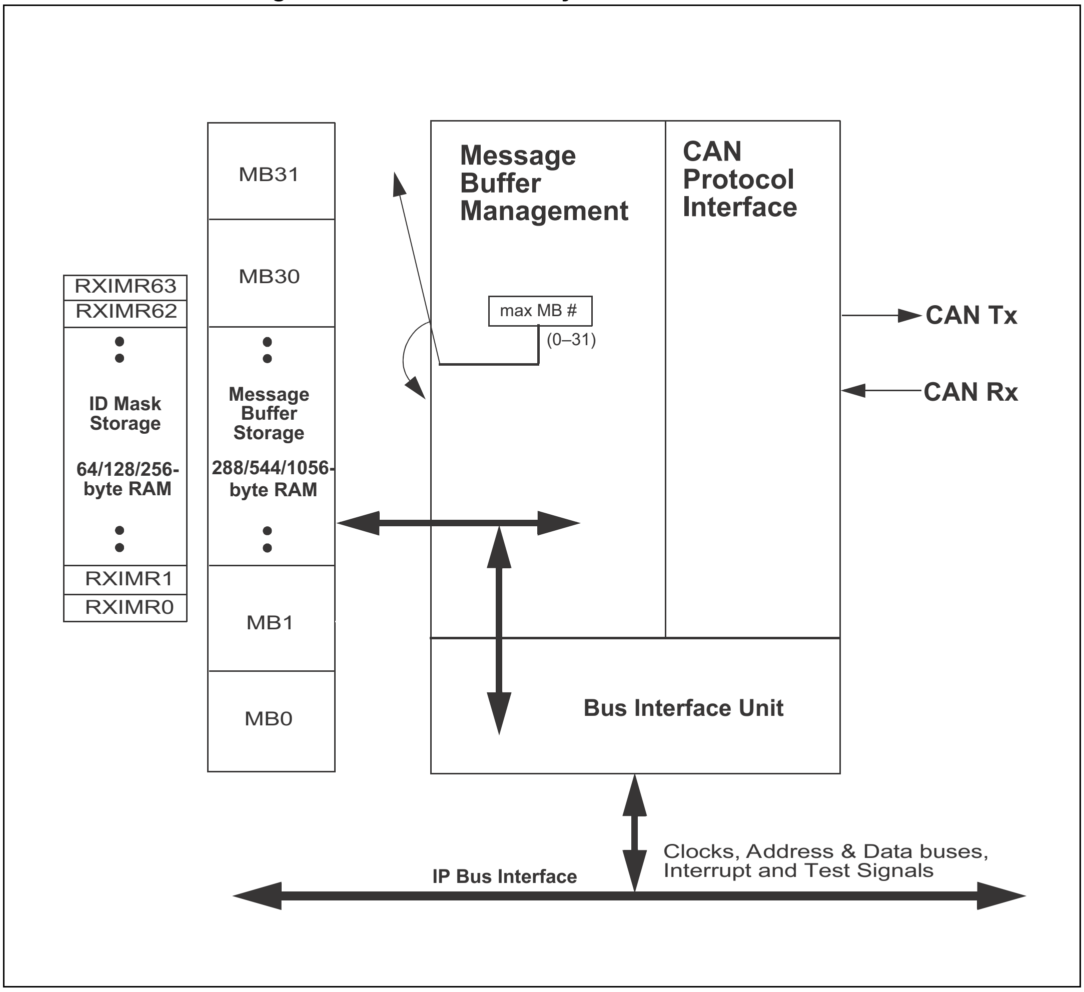
Generic Slave Interface (GSI)

- CAN-RAM arbiter
- SRAM interface and memory organization
- ECC Controller

SPC560B64 has the FlexCan implemented.

The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification.

Figure 10. FlexCAN subsystem for SPC560B64



Features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0–8 bytes data length
  - Programmable bit rate up to 1 Mbit/s
  - Content-related addressing
- Flexible Message Buffers (up to 64) of zero to eight bytes data length
- Each MB configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Includes either 1056 bytes (64 MBs) of SRAM used for MB storage
- Includes either 256 bytes (64 MBs) of SRAM used for individual Rx Mask Registers
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN version
- Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
- Unused MB and Rx Mask Register space can be used as general purpose SRAM space
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode
- Hardware cancellation on Tx message buffers

9.3 I2C

Both devices provide I2C interface, with some difference showed below by looking at the features.

- Maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF (**SPC584Bx**)
- No support for general call address (**SPC560B64**)
- Not compliant to ten-bit addressing (**SPC560B64**)

9.4 DSPI

For both devices, DSPI can operate in SPI configuration.

SPC584Bx has 7 DSPI, SPC560B64 has 6 DSPI.

Here the main differences:

- Type of transfer
  - Full-duplex, four-wire synchronous transfers (**SPC584Bx**)
  - Full-duplex, three-wire synchronous transfers (**SPC560B64**)
- Programmable transfer attributes on a per-frame basis
  - SPC584Bx
    - 8 transfer attribute registers along with 8 extended transfer attribute registers
    - serial clock with programmable polarity and phase
    - various programmable delays
    - programmable serial frame size of 4 to 64 bits, expandable by software control. SPI frames longer than 32 bits are supported using the continuous selection format
    - continuously held chip select capability
    - parity control
  - SPC560B64
    - 6 clock and transfer attribute registers
    - Serial clock with programmable polarity and phase
    - Programmable delays
      - CS to SCK delay
      - SCK to CS delay
      - Delay between frames
- Deglitching support
  - up to 128 Peripheral Chip Selects with external demultiplexer (**SPC584Bx**)
  - for up to 32 peripheral chip selects with external demultiplexer (**SPC560B64**)
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO (**SPC584Bx**):
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
  - CMD FIFO is not full (CMDFFF)
- Interrupt conditions
  - **SPC584Bx**
    - End Of Queue reached (EOQF)
    - TX FIFO is not full (TFFF)
    - Transfer of current frame Complete (TCF)
    - RX FIFO is not empty (RFDF)
    - frame received while Receive FIFO is full (RFOF)
  - **SPC560B64**
    - End of queue reached (EOQF)
    - TX FIFO is not full (TFFF)
    - Transfer of current frame complete (TCF)
    - RX FIFO is not empty (RFDF)

- FIFO overrun (attempt to transmit with an empty TX FIFO or serial frame received while RX FIFO is full) (RFOF) or (TFUF)

- Power-saving architectural features: support for stop mode (**SPC584Bx**)

10 Timed I/O

10.1 eMIOS

The eMIOS provides functionality to generate or measure time events.

Here are the main differences:

- Number of blocks
  - 2 eMIOS block with 32 channels (**SPC584Bx**)
  - 2 eMIOS blocks with 32 channels each (**SPC560B64**)
    64 channels with OPWMT, which can be connected to the CTU
    Both eMIOS blocks can be synchronized
- eMIOS block can be synchronized from outside (**SPC584Bx**)
- Flag outputs of channels 8-11 of eMIOSs are used to disable the outputs of other channels. They form the ODIS bits (**SPC584Bx**)

10.2 SCTU (Self Test Control Unit)

To handle safety features, the SPC584Bx implements a STCU (for instance memory Buily-In Self test - MBIST). SPC560B64 does not implement the STCU module.

11 Analog modules

11.1 ADC/SARADC

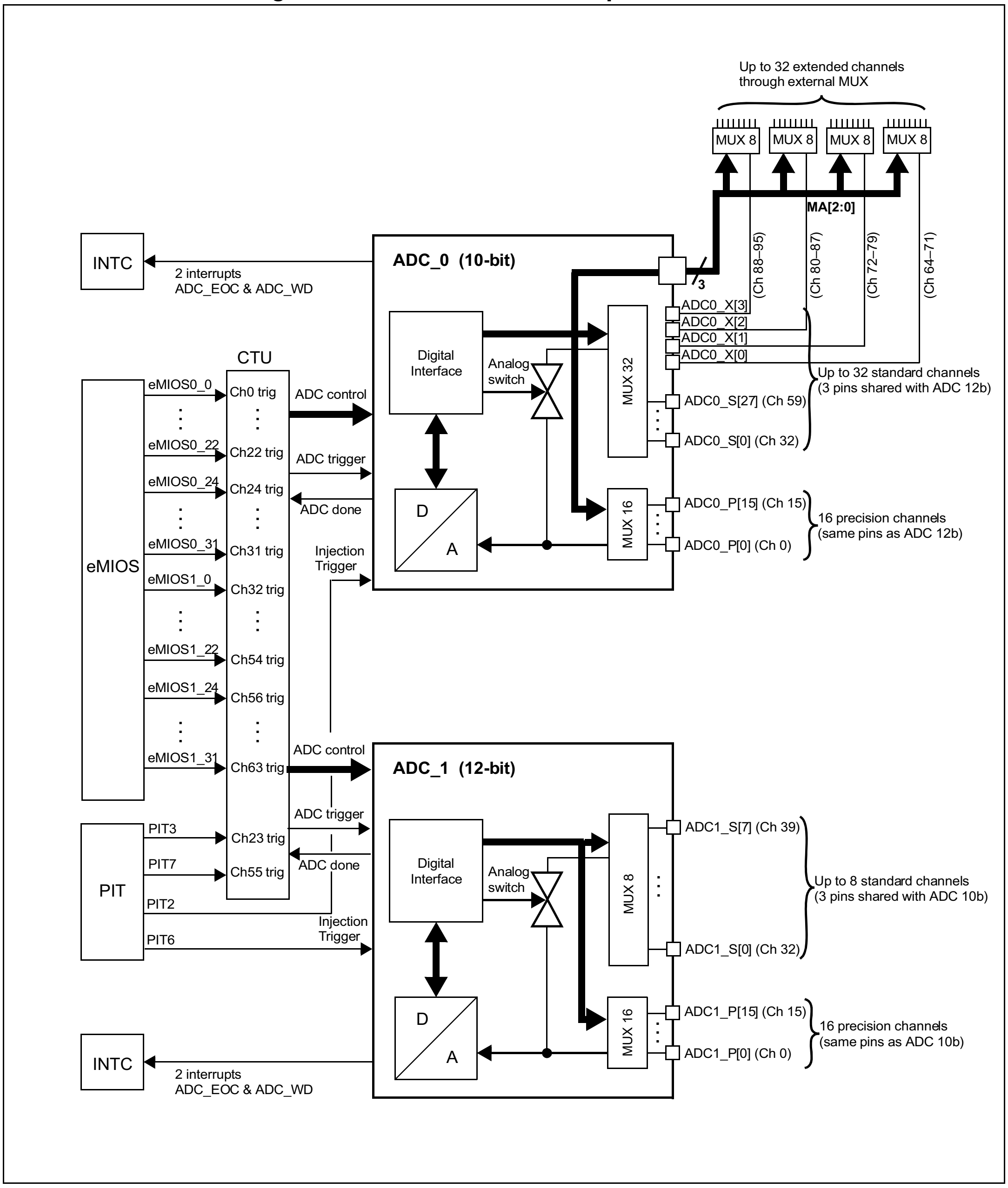
SPC584Bx provides 64 ADC channels distributed between 10bit, 12bit, stdby ADC and an independent 12 bit SARADC.

SPC560B64 provides 53 ADC channels with 10bit and 12bit resolution.

SPC560B64 ADC features:

- 2 ADC modules, (ADC_0 with 10-bit resolution and ADC_1 with 12-bit resolution)
- 0–VDD common mode conversion range
- Independent reference supplies for each ADC
- 53 single-ended input channels (depending on package type), expandable to 81 channels via external multiplexing
  - Internally multiplexed channels
    - 16 precision channels shared between 10-bit and 12-bit ADCs
    - 3 standard channels shared between 10-bit and 12-bit ADCs
    - 5 dedicated standard channels on 12-bit ADC
    - Up to 29 dedicated standard channels on 10-bit ADC
  - Externally multiplexed channels
    - Internal control to support generation of external analog multiplexer selection
    - 4 internal channels optionally used to support externally multiplexed inputs, providing transparent control for additional ADC channels
    - Each of the 4 channels supports as many as 8 externally multiplexed inputs
- 3 independently configurable sample and conversion times for high precision channels, standard precision channels and externally multiplexed channels
- Dedicated result registers available for every channel. Conversion information, such as mode of operation (normal, injected or CTU), is associated to data value.
- One Shot/Scan Modes
- Chain Injection Mode
- Conversion triggering sources:
  - Software
  - CTU
  - PIT channel 2 and 6 (for injected conversion)
- Conversion triggering support — Internal conversion triggering from periodic interrupt timer (PIT) or timed I/O module (eMIOS)
- Power-down mode for analog portion of ADC
- Supports DMA transfer of results based on the end of conversion
- 6 + 3 analog watchdogs (6 on 10-bit ADC, 3 on 12-bit ADC) with interrupt capability for continuous hardware monitoring

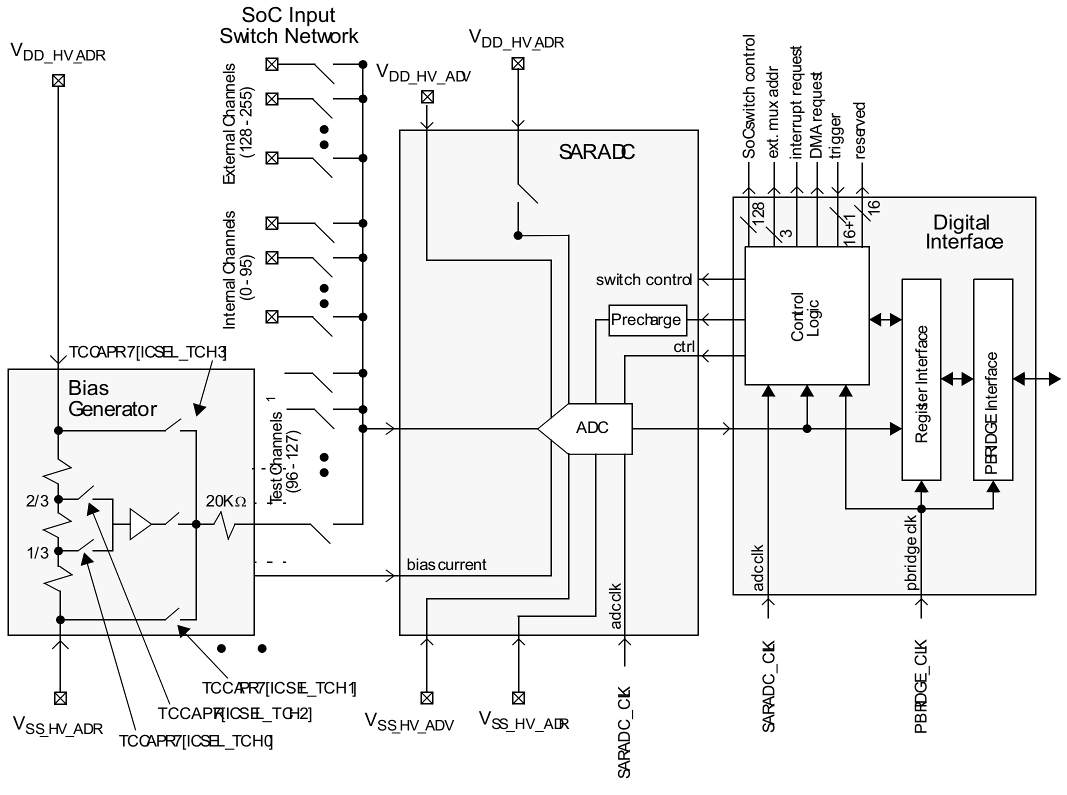
Figure 11. SPC560B64 ADC implementation



These are instead the list of the **features about SPC584Bx SARADC**, not available in SPC560B64 series:

- Selectable 10-bit or 12-bit data resolution output for 12-bit SARADC.
- Selectable 8-bit or 10-bit data resolution output for 10-bit SARADC.
- Up to 96 internal channels, 32 test channels, 128 external channels supported; variable number of analog channels of each type controlled by parameters
- 4 different conversion timing registers selectable for any channel
- Mapping of external channel to any internal channel through static programming by software
- Shorting of test channel with internal channel through static programming by software
- External decode signals (3 signals) for selection of external analog mux inputs
- Normal conversion with One Shot/Scan modes
- Injected conversion with One Shot mode
- Normal conversion with dedicated trigger input
- Injected conversion with dedicated trigger input
- 2 different abort features that allow to abort either a single channel conversion or chain conversion
- Reference selection for each channel
- Power Down Mode
- Dedicated data register for each channel, containing the following information:
  - Conversion result in one half-word:
- 10-bit or 12-bit for 12-bit SARADC.
- 8-bit or 10-bit for 10-bit SARADC.
- Status byte which provides some conversion information such as mode of operation (Normal, Injected, or CTU), data valid, data overwritten status
- Control byte for reference selection, conversion timing parameter selection
  - Configurable number of analog watchdogs.Trigger outputs on watchdog threshold crossover events
  - 2 different CTU modes (CTU Control mode and CTU Trigger mode) available when CTU feature is present in SARADC instance.
  - Interrupt/DMA support for the following conditions
- End of conversion of single channel for both normal, injected conversions
- End of conversion chain for both normal, injected conversions
- End of CTU conversion
- Watchdog thresholds crossover

Figure 12. SPC584Bx SARADC block diagram



Note: Test channels are mapped to internal analog channels via the TCCAPRn registers of SAR ADC supervisor.

12 Safety

12.1 FCCU / CRC / MBIST

These features are available on SPC584Bx only.

Appendix A Appendix A

A.1 Reference document

1. SPC584Bx Datasheet – target specification
2. SPC584Bx Reference Manual – RM0449
3. SPC560B54x, SPC560B60x, SPC56064x Datasheet – target specification
4. SPC560B64 Reference Manual – RM0037
5. Migration guide for SPC560C/B50, SPC560C/B4x with SPC560B54/6x

Revision history

Table 7. Document revision history

Date	Revision	Changes
13-Jul-2018	1	Initial release.