

ZILOG MICROPROCESSOR COMPONENTS LIBRARY

Packaged Parts

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p-cad[®]
PERSONAL CAD SYSTEMS INC.

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OVERVIEW

This manual and the two Zilog Microprocessor Packaged Parts Diskettes comprise the P-CAD Zilog Microprocessor Packaged Parts Library. The library has been developed at the request of our users, and we welcome any suggestions for improvements or additions.

The library diskettes contain the following files for use with the PC-CARDS printed circuit board (PCB) layout program:

- Component files
- Layer structure files, LAYS.PRT and LAYS.PCB
- Standard-size drawing sheet files, ASIZE.PCB through ESIZE.PCB
- ZILOG.FIL and ZILOG.LIB files

ZILOG.FIL is a sample test file used as input into PREPACK to create the binary file ZILOG.LIB that contains packaging information for PC-PACK. Both ZILOG.FIL and ZILOG.LIB contain all the components in the Zilog Microprocessor Library. Normal usage is to extract only those components used in a design and put them in a new .FIL file for input to PREPACK.

- Padstack and special symbol files (<filename>.PS and <filename>.SSF)

The padstacks and special symbol files are samples of what can be used in the PC-CARDS environment. Refer to the PC-CARDS User's Manual for more information on how to use padstacks and special symbol files.

FILE MANAGEMENT

The complete Zilog Microprocessor Parts Library includes more than 350 KB of files. If you are loading the library on the hard disk of your stand-alone computer, you should omit any of the components that you will not need in order to conserve disk space. This is especially important if you are using a 10 MB hard disk.

If your hard disk space is very limited, you may remove individual unneeded parts from the library. Each part is contained in a separate DOS file, and individual parts may

be erased using the DOS erase command. Refer to your IBM DOS Manual or the "DOS Reference" chapter included with your PC-CAPS or PC-CARDS User's Manuals for instructions on listing and erasing files.

P-CAD recommends a specific directory structure for efficient system operation. Your library parts are normally placed in a specific subdirectory to make it easy to manage these files. The directory structure is described in your P-CAD Installation Guide.

CREATING A DESIGN

To use the library in a design, run PC-CARDS. Instructions are given in the "Using PC-CARDS" chapter of your PC-CARDS User's Manual. When the menu is displayed, select FILE/LOAD and load the layer structure. You can load LAYS.PCB or one of the standard-size drawing sheet files, ASIZE.PCB through ESIZE.PCB.

Layer Structure

Two layer structure files are included with this library, LAYS.PRT and LAYS.PCB. There is no difference between LAYS.PRT and LAYS.PCB other than the active state of the layers.

The following layer structure, LAYS.PRT, is a standard P-CAD layer structure and is recommended when creating library components.

Table 1. LAYS.PRT Layer Structure

Layer	Name	Pen	Status	Use
1	PADCOM	4	ON	Graphic component pads
2	FLCOMP	4	OFF	Flash component pads
3	PADSLD	8	OFF	Graphic solder pads
4	FLSOLD	8	OFF	Flash solder pads

Table 1 Continued

Layer	Name	Pen	Status	Use
5	PADINT	9	OFF	Graphic internal pads
6	FLINT	9	OFF	Flash internal pads
7	GNDCON	10	OFF	Graphic internal ground connections
8	FLGCON	10	OFF	Flash internal ground connections
9	CLEAR	7	OFF	Graphic universal clearance
10	FLCLER	7	OFF	Flash universal clearance
11	PWRCON	13	OFF	Graphic internal power connections
12	FLPCON	13	OFF	Flash internal power connections
13	SLDMSK	14	OFF	Graphic solder mask relief
14	FLSMSK	14	OFF	Flash solder mask
15	DRILL	15	OFF	Graphic drill template
16	FLDRLL	15	OFF	Flash drill template
17	PIN	4	ABL(A)	Graphic pin connections
18	BRDOUT	12	OFF	Board outline

Table 1 Continued

Layer	Name	Pen	Status	Use
19	FLTARG	11	OFF	Flash alignment targets
20	SLKSCR	6	ABL	Silkscreen paint
21	DEVICE	5	ABL	Device names
22	ATTR	6	OFF	Attributes
23	REFDES	6	OFF	Reference designators
24	COMP	1	OFF	Component side traces
25	SOLDER	2	OFF	Solder side traces
26	INT1	3	OFF	Internal layer traces

The following layer structure, LAYS.PCB, is a standard P-CAD layer structure and is recommended when creating printed circuit board layouts.

Table 2. LAYS.PCB Layer Structure

Layer	Name	Pen	Status	Use
1	PADCOM	4	ON	Graphic component pads
2	FLCOMP	4	OFF	Flash component pads
3	PADSLD	8	OFF	Graphic solder pads
4	FLSOLD	8	OFF	Flash solder pads

Table 2 Continued

Layer	Name	Pen	Status	Use
5	PADINT	9	OFF	Graphic internal pads
6	FLINT	9	OFF	Flash internal pads
7	GNDCON	10	OFF	Graphic internal ground connections
8	FLGCON	10	OFF	Flash internal ground connections
9	CLEAR	7	OFF	Graphic universal clearance
10	FLCLER	7	OFF	Flash universal clearance
11	PWRCON	13	OFF	Graphic internal power connections
12	FLPCON	13	OFF	Flash internal power connections
13	SLDMSK	14	OFF	Graphic solder mask relief
14	FLSMSK	14	OFF	Flash solder mask
15	DRILL	15	OFF	Graphic drill template
16	FLDRLL	15	OFF	Flash drill template
17	PIN	4	ON	Graphic pin connections
18	BRDOUT	12	ON	Board outline

Table 2 Continued

Layer	Name	Pen	Status	Use
19	FLTARG	11	OFF	Flash alignment targets
20	SLKSCR	6	ON	Silkscreen paint
21	DEVICE	5	ON	Device names
22	ATTR	6	OFF	Attributes
23	REFDES	6	ON	Reference designators
24	COMP	1	ABL (A)	Component side traces
25	SOLDER	2	ABL	Solder side traces
26	INT1	3	OFF	Internal layer traces

Drawing Sheets

The standard-size drawing sheet files, ASIZE.PCB through ESIZE.PCB, were created using the LAYS.PCB layer structure. When loaded, they provide the correct layer structure for the library plus a standard-size drawing sheet border.

Components

When you have loaded the layer structure or drawing sheet file, you can enter the components, wires, text, instances, and net names. Complete instructions are given in the "Using PC-CARDS" chapter of your PC-CARDS User's Manual.

GENERAL INFORMATION

This library was created using Zilog's Component Data Book and Zilog's Microprocessor Applications Reference Book, volumes 1 and 2.

Some components come in more than one package. To

distinguish components that come in more than one package, we have used the following filename conventions:

68-pin LCC - The filename ends in L; for example:
Z8015L.PRT.

NAMING CONVENTIONS

In this library, all the signal names are drawn exactly as shown in the Zilog data manuals except where the abbreviation of the signal name is required due to the length of the name. For example, VCC STANDBY may be shortened to VCCSTBY. In addition, some names in the data sheets may contain an illegal character such as a slash (/). In such cases as these, the characters are either omitted or replaced with a dash (-). The actual signal names for the symbols are given in the pinlists in this manual.

The following signal naming conventions are used in the components library.

Table 3. Signal Naming Conventions

Signal Name	Convention
CLOCK	CLK
R/W'	R-W
BYTE/WORD'	B-W
NORMAL/SYSTEM'	N-S

FOOTPRINTS

The components in this library have been assigned footprint attributes on the ATTR layer for PC-PLACE. All DIP parts have the footprint attribute : FP=DIPxx where xx is the number of pins for that part. The Leadless Chip Carrier has a footprint attribute of : FP=LCCxx where xx is the number of pins on that package.

COMPONENT LIST BY SEQUENCE

The component filename is the component number plus the extension .PRT; for example, Z8001.PRT. "Plot Number" refers to the plots in the last section of this manual.

SYMBOL	DISK NUMBER	PLOT NUMBER
Z765	1	1
Z8001	1	1
Z8001L	1	1
Z8002	1	1
Z8003	1	1
Z8004	1	1
Z8010	1	1
Z8010L	1	1
Z8015L	1	1
Z8016	1	1
Z8030	1	1
Z8031	1	1
Z8036	1	1
Z8038	1	1
Z8060	1	2
Z8068	1	2
Z8090	1	2
Z8094	1	2
Z8108	1	2
Z8116	1	2
Z8400	1	2
Z8410	1	2
Z8420	1	2
Z8430	1	2
Z8440	1	2
Z8441	1	2
Z8442	1	2
Z8470	1	2
Z84C00	1	2
Z84C20	1	3
Z84C30	1	3
Z84C40	1	3
Z84C41	1	3
Z84C42	1	3
Z8516	1	3
Z8530	1	3
Z8531	1	3
Z8536	1	3
Z8581	1	3
Z8590	1	3
Z8594	1	3
Z8601	1	3
Z8603	1	3
Z8611	1	3

SYMBOL	DISK NUMBER	PLOT NUMBER
Z8613	1	3
Z8671	1	3
Z8681	1	3
Z8682	1	4
Z8800	1	4
Z8801	1	4
Z8810	1	4
Z8811	1	4
Z8812	1	4
Z8813	1	4
Z8820	1	4
Z8821	1	4
Z8822	1	4
Z8823	1	4
Z8830	1	4
Z8831	1	4
Z8832	1	4
Z8833	1	4

COMPONENT LIST BY FUNCTION

The component filename is the component number plus the extension .PRT; for example, the filename for Z8001 is Z8001.PRT.

CLOCK GENERATORS

Z8581 CGC clock generator and controller

COMMUNICATION DEVICES

Z8030 Z8000 Z-SCC dual channel serial communications controller
 Z8031 Z8000 Z-ASCC dual channel asynchronous serial communications controller
 Z8440 Z80 SIO/0 dual channel synchronous/asynchronous serial input/output controller
 Z84C40 Z80 CMOS SIO/0 dual channel synchronous/asynchronous serial input/output controller
 Z8441 Z80 SIO/1 dual channel synchronous/asynchronous serial input/output controller
 Z84C41 Z80 CMOS SIO/1 dual channel synchronous/asynchronous serial input/output controller
 Z8442 Z80 SIO/2 dual channel synchronous/asynchronous serial input/output controller
 Z84C42 Z80 CMOS SIO/2 dual channel synchronous/asynchronous serial input/output controller
 Z8530 SCC dual channel serial communications controller
 Z8531 ASCC dual channel asynchronous serial communications controller
 Z8470 Z80 DART dual asynchronous receiver/transmitter

COUNTER/TIMERS

Z8036 Z8000 Z-CIO counter/timer and parallel I/O unit
 Z8430 Z80 CTC four channel, counter/timer circuit
 Z84C30 Z80 CMOS CTC four channel, counter/timer circuit
 Z8536 CIO counter/timer and parallel I/O unit

DISK CONTROLLERS

Z765 FDC floppy disk controller

MEMORY MANAGEMENT

Z8010 Z8000 MMU memory management unit
 Z8010L Z8000 MMU memory management unit in a 68-pin LCC package
 Z8015L Z8000 PMMU paged memory management unit in a 68-pin LCC package
 Z8016 Z8000 Z-DTC direct memory access transfer controller
 Z8410 DMA dual port, direct memory access controller
 Z8516 DTC direct memory access transfer controller

MICROCOMPUTERS

Z8601 Z8 8-bit MCU, 2K ROM
 Z8603 Z8 Prototyping device, external 2K EPROM interface
 Z8611 Z8 8-bit MCU, 4K ROM
 Z8612 Z8 8-bit MCU, 4K external memory interface
 Z8613 Z8 Prototyping device, external 4K EPROM interface
 Z8671 Z8 8-bit MCU with BASIC/Debug interpreter
 Z8681 Z8 8-bit ROMless MCU
 Z8682 Z8 8-bit cost-effective ROMless MCU
 Z8800 Super-8 ROMless MCU
 Z8801 Super-8 ROMless MCU
 Z8810 Super-8 MCU, 4K ROM
 Z8811 Super-8 MCU, 4K ROM
 Z8812 Super-8 MCU, 4K external ROM/EPROM
 Z8813 Super-8 MCU, 4K external ROM/EPROM
 Z8820 Super-8 MCU, 8K ROM
 Z8821 Super-8 MCU, 8K ROM
 Z8822 Super-8 MCU, 8K external ROM/EPROM
 Z8823 Super-8 MCU, 8K external ROM/EPROM
 Z8830 Super-8 MCU, 16K ROM
 Z8831 Super-8 MCU, 16K ROM
 Z8832 Super-8 MCU, 16K external ROM/EPROM
 Z8833 Super-8 MCU, 16K external ROM/EPROM

MICROPROCESSORS

Z8001 Z8000 segmented CPU
 Z8001L Z8000 segmented CPU in a 68-pin LCC package
 Z8002 Z8000 nonsegmented CPU

Z8003	Z8000 segmented virtual memory processing unit
Z8004	Z8000 nonsegmented virtual memory processing unit
Z8108	Z800 high integration CPU
Z8116	Z800 high integration CPU
Z8400	Z80 CPU
Z84C00	Z80 CMOS CPU

PARALLEL I/O

Z8038	Z8000 Z-FIO FIFO input/output interface unit
Z8060	Z8000 FIFO buffer unit and Z-FIO expander
Z8420	Z80 PIO dual port, parallel input/output controller
Z84C20	Z80 CMOS PIO dual port, parallel input/output controller

PERIPHERAL CONTROLLERS

Z8090	Z8000 Z-UPC universal peripheral controller
Z8094	UPC universal peripheral controller, external RAM
Z8590	UPC universal peripheral controller
Z8594	UPC universal peripheral controller, external RAM

COMPONENT PIN SEQUENCES

The component filename is the component number plus the extension .PRT; for example Z8001.PRT.

Z765: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	RESET	15 =	DACK'	28 =	US1
2 =	RD'	16 =	TC	29 =	US0
3 =	WR'	17 =	IDX	30 =	WDA
4 =	CS'	18 =	INT	31 =	PS1
5 =	D-S	19 =	CLK	32 =	PS0
6 =	D0	20 =	[GND]	33 =	FLT-TR0
7 =	D1	21 =	WCK	34 =	WP-TS
8 =	D2	22 =	RDW	35 =	RDY
9 =	D3	23 =	RDD	36 =	HDL
10 =	D4	24 =	VCO-SYNC	37 =	FR-STP
11 =	D5	25 =	WE	38 =	LCT-DIR
12 =	D6	26 =	MFm	39 =	RW-SEEK
13 =	D7	27 =	HD	40 =	[VCC]
14 =	DRQ				

Z8001: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD0	17 =	MO'	33 =	{n/c}
2 =	AD9	18 =	MREQ'	34 =	AS'
3 =	AD10	19 =	DS'	35 =	CLK
4 =	AD11	20 =	ST3	36 =	[GND]
5 =	AD12	21 =	ST2	37 =	SN2
6 =	AD13	22 =	ST1	38 =	AD1
7 =	STOP'	23 =	ST0	39 =	AD2
8 =	MI'	24 =	SN3	40 =	AD3
9 =	AD15	25 =	SN1	41 =	AD5
10 =	AD14	26 =	SN0	42 =	SN4
11 =	[VCC]	27 =	BUSREQ'	43 =	AD4
12 =	VI'	28 =	WAIT'	44 =	AD6
13 =	NVI'	29 =	BUSACK'	45 =	AD7
14 =	SEGT'	30 =	R-W	46 =	SN5
15 =	NMI'	31 =	N-S	47 =	SN6
16 =	RESET'	32 =	B-W	48 =	AD8

Z8001L: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[GND]	24 =	MO'	47 =	B-W
2 =	[VCC]	25 =	MREQ'	48 =	{n/c}
3 =	AD0	26 =	{n/c}	49 =	AS'
4 =	AD9	27 =	{n/c}	50 =	{n/c}
5 =	AD10	28 =	{n/c}	51 =	CLK
6 =	AD11	29 =	DS'	52 =	{n/c}
7 =	AD12	30 =	ST3	53 =	[GND]
8 =	AD13	31 =	ST2	54 =	SN2
9 =	{n/c}	32 =	ST1	55 =	AD1
10 =	{n/c}	33 =	ST0	56 =	AD2
11 =	STOP'	34 =	SN3	57 =	AD3
12 =	MI'	35 =	SN1	58 =	AD5
13 =	AD15	36 =	SN0	59 =	SN4
14 =	AD14	37 =	BUSREQ'	60 =	{n/c}
15 =	[VCC]	38 =	WAIT'	61 =	{n/c}
16 =	{n/c}	39 =	BUSACK'	62 =	{n/c}
17 =	{n/c}	40 =	{n/c}	63 =	AD4
18 =	{n/c}	41 =	{n/c}	64 =	AD6
19 =	VI'	42 =	{n/c}	65 =	AD7
20 =	NVI'	43 =	{n/c}	66 =	SN5
21 =	SEGT'	44 =	{n/c}	67 =	SN6
22 =	NMI'	45 =	R-W	68 =	AD8
23 =	RESET'	46 =	N-S		

Z8002: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD9	15 =	MO'	28 =	{n/c}
2 =	AD10	16 =	MREQ'	29 =	AS'
3 =	AD11	17 =	DS'	30 =	CLK
4 =	AD12	18 =	ST3	31 =	[GND]
5 =	AD13	19 =	ST2	32 =	AD1
6 =	STOP'	20 =	ST1	33 =	AD2
7 =	MI'	21 =	ST0	34 =	AD3
8 =	AD15	22 =	BUSREQ'	35 =	AD5
9 =	AD14	23 =	WAIT'	36 =	AD4
10 =	[VCC]	24 =	BUSACK'	37 =	AD6
11 =	VI'	25 =	R-W	38 =	AD7
12 =	NVI'	26 =	N-S	39 =	AD8
13 =	NMI'	27 =	B-W	40 =	AD0
14 =	RESET'				

Z8003: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD0	17 =	MO'	33 =	ABORT'
2 =	AD9	18 =	MREQ'	34 =	AS'
3 =	AD10	19 =	DS'	35 =	CLK
4 =	AD11	20 =	ST3	36 =	[GND]
5 =	AD12	21 =	ST2	37 =	SN2
6 =	AD13	22 =	ST1	38 =	AD1
7 =	STOP'	23 =	ST0	39 =	AD2
8 =	MI'	24 =	SN3	40 =	AD3
9 =	AD15	25 =	SN1	41 =	AD5
10 =	AD14	26 =	SN0	42 =	SN4
11 =	[VCC]	27 =	BUSREQ'	43 =	AD4
12 =	VI'	28 =	WAIT'	44 =	AD6
13 =	NVI'	29 =	BUSACK'	45 =	AD7
14 =	SAT'	30 =	R-W	46 =	SN5
15 =	NMI'	31 =	N-S	47 =	SN6
16 =	RESET'	32 =	B-W	48 =	AD8

Z8004: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD9	15 =	MO'	28 =	ABORT'
2 =	AD10	16 =	MREQ'	29 =	AS'
3 =	AD11	17 =	DS'	30 =	CLK
4 =	AD12	18 =	ST3	31 =	[GND]
5 =	AD13	19 =	ST2	32 =	AD1
6 =	STOP'	20 =	ST1	33 =	AD2
7 =	MI'	21 =	ST0	34 =	AD3
8 =	AD15	22 =	BUSREQ'	35 =	AD5
9 =	AD14	23 =	WAIT'	36 =	AD4
10 =	[VCC]	24 =	BUSACK'	37 =	AD6
11 =	VI'	25 =	R-W	38 =	AD7
12 =	NVI'	26 =	N-S	39 =	AD8
13 =	NMI'	27 =	B-W	40 =	AD0
14 =	RESET'				

Z8010: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = CS'		17 = A13		33 = AD13	
2 = DMASYN		18 = A12		34 = AD12	
3 = SEGT'		19 = A11		35 = [GND]	
4 = SUP'		20 = A10		36 = CLK	
5 = RESET'		21 = A9		37 = AD11	
6 = A23		22 = A8		38 = AD10	
7 = A22		23 = {n/c}		39 = AD9	
8 = A21		24 = SN6		40 = AD8	
9 = A20		25 = SN5		41 = ST3	
10 = A19		26 = SN4		42 = ST2	
11 = [VCC]		27 = SN3		43 = ST1	
12 = A18		28 = SN2		44 = ST0	
13 = A17		29 = SN1		45 = DS'	
14 = A16		30 = SN0		46 = AS'	
15 = A15		31 = AD15		47 = R-W	
16 = A14		32 = AD14		48 = N-S	

Z8010L: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = CS'		24 = A14		47 = AD13	
2 = DMASYN		25 = A13		48 = AD12	
3 = SEGT'		26 = A12		49 = {n/c}	
4 = SUP'		27 = {n/c}		50 = {n/c}	
5 = RESET'		28 = {n/c}		51 = {n/c}	
6 = A23		29 = A11		52 = {n/c}	
7 = {n/c}		30 = A10		53 = CLK	
8 = {n/c}		31 = A9		54 = AD11	
9 = {n/c}		32 = A8		55 = AD10	
10 = {n/c}		33 = {n/c}		56 = AD9	
11 = {n/c}		34 = SN6		57 = AD8	
12 = A22		35 = SN5		58 = ST3	
13 = A21		36 = SN4		59 = ST2	
14 = A20		37 = SN3		60 = {n/c}	
15 = A19		38 = SN2		61 = {n/c}	
16 = {n/c}		39 = SN1		62 = {n/c}	
17 = [VCC]		40 = SN0		63 = ST1	
18 = {n/c}		41 = {n/c}		64 = ST0	
19 = {n/c}		42 = {n/c}		65 = DS'	
20 = A18		43 = {n/c}		66 = AS'	
21 = A17		44 = {n/c}		67 = R-W	
22 = A16		45 = AD15		68 = N-S	
23 = A15		46 = AD14			

Z8015L: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = CS'		24 = A11		47 = AD15	
2 = DMASYN		25 = A10		48 = AD14	
3 = CE'		26 = [GND]		49 = AD13	
4 = TRAP'		27 = A9		50 = AD12	
5 = SUP'		28 = A8		51 = AD11	
6 = ABORT'		29 = RSRVD		52 = AD10	
7 = RESET'		30 = SN6		53 = [GND]	
8 = {n/c}		31 = SN5		54 = CLK	
9 = {n/c}		32 = SN4		55 = AD9	
10 = A23		33 = SN3		56 = AD8	
11 = {n/c}		34 = SN2		57 = ST3	
12 = A22		35 = SN1		58 = ST2	
13 = A21		36 = SN0		59 = {n/c}	
14 = A20		37 = AD0		60 = {n/c}	
15 = A19		38 = AD1		61 = {n/c}	
16 = A18		39 = AD2		62 = {n/c}	
17 = [VCC]		40 = AD3		63 = ST1	
18 = A17		41 = AD4		64 = ST0	
19 = A16		42 = AD5		65 = DS'	
20 = A15		43 = AD6		66 = AS'	
21 = A14		44 = {n/c}		67 = R-W	
22 = A13		45 = [VCC]		68 = N-S	
23 = A12		46 = AD7			

Z8016: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = BAI'		17 = AD12		33 = ST2	
2 = BUSREQ'		18 = AD13		34 = ST3	
3 = BAO'		19 = AD14		35 = B-W	
4 = [VCC]		20 = AD15		36 = DREQ1'	
5 = AD0		21 = SN6		37 = DREQ2'	
6 = AD1		22 = SN5		38 = EOP'	
7 = AD2		23 = SN4		39 = DACK2'	
8 = AD3		24 = SN3		40 = DACK1'	
9 = AD4		25 = SN2		41 = R-W	
10 = AD5		26 = [GND]		42 = CS-WAIT'	
11 = AD6		27 = SN7-MMUS		43 = DS'	
12 = AD7		28 = SN1		44 = AS'	
13 = AD8		29 = SN0		45 = CLK	
14 = AD9		30 = N-S		46 = IEI	
15 = AD10		31 = ST0		47 = INT'	
16 = AD11		32 = ST1		48 = IEO	

Z8030: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD1	15 =	TXDA	28 =	RTXCB'
2 =	AD3	16 =	DTR-RQA'	29 =	SYNCB'
3 =	AD5	17 =	RTSA'	30 =	W-REQB'
4 =	AD7	18 =	CTSA'	31 =	[GND]
5 =	INT'	19 =	DCDA'	32 =	CS1
6 =	IEO	20 =	PCLK	33 =	CS0'
7 =	IEI	21 =	DCDB'	34 =	R-W
8 =	INTACK'	22 =	CTSB'	35 =	AS'
9 =	[VCC]	23 =	RTSB'	36 =	DS'
10 =	W-REQA'	24 =	DTR-RQB'	37 =	AD6
11 =	SYNCA'	25 =	TXDB	38 =	AD4
12 =	RTXCA'	26 =	TRXCB'	39 =	AD2
13 =	RXDA	27 =	RXDB	40 =	AD0
14 =	TRXCA'				

Z8031: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD1	15 =	TXDA	28 =	RTXCB'
2 =	AD3	16 =	DTR-RQA'	29 =	RIB'
3 =	AD5	17 =	RTSA'	30 =	W-REQB'
4 =	AD7	18 =	CTSA'	31 =	[GND]
5 =	INT'	19 =	DCDA'	32 =	CS1
6 =	IEO	20 =	PCLK	33 =	CS0'
7 =	IEI	21 =	DCDB'	34 =	R-W
8 =	INTACK'	22 =	CTSB'	35 =	AS'
9 =	[VCC]	23 =	RTSB'	36 =	DS'
10 =	W-REQA'	24 =	DTR-RQB'	37 =	AD6
11 =	RIA'	25 =	TXDB	38 =	AD4
12 =	RTXCA'	26 =	TRXCB'	39 =	AD2
13 =	RXDA	27 =	RXDB	40 =	AD0
14 =	TRXCA'				

Z8036: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD4	15 =	PB7	28 =	PA5
2 =	AD5	16 =	PCLK	29 =	PA4
3 =	AD6	17 =	IEI	30 =	PA3
4 =	AD7	18 =	IEO	31 =	PA2
5 =	DS'	19 =	PC0	32 =	PA1
6 =	R-W	20 =	PC1	33 =	PA0
7 =	[GND]	21 =	PC2	34 =	AS'
8 =	PB0	22 =	PC3	35 =	CS1
9 =	PB1	23 =	[VCC]	36 =	CS0'
10 =	PB2	24 =	INT'	37 =	AD0
11 =	PB3	25 =	INTACK'	38 =	AD1
12 =	PB4	26 =	PA7	39 =	AD2
13 =	PB5	27 =	PA6	40 =	AD3
14 =	PB6				

Z8038: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	A1	15 =	D14	28 =	D21
2 =	B1	16 =	D15	29 =	D20
3 =	C1	17 =	D16	30 =	J2
4 =	D1	18 =	D17	31 =	I2
5 =	E1	19 =	M1	32 =	H2
6 =	F1	20 =	[GND]	33 =	G2
7 =	G1	21 =	M0	34 =	F2
8 =	H1	22 =	D27	35 =	E2
9 =	I1	23 =	D26	36 =	D2
10 =	J1	24 =	D25	37 =	C2
11 =	D10	25 =	D24	38 =	B2
12 =	D11	26 =	D23	39 =	A2
13 =	D12	27 =	D22	40 =	[VCC]
14 =	D13				

Z8060: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	RFDA	11 =	D5A	20 =	D2B
2 =	ACKIA'	12 =	D6A	21 =	D1B
3 =	FULL	13 =	D7A	22 =	D0B
4 =	EMPTY	14 =	[GND]	23 =	OEB'
5 =	OEA'	15 =	D7B	24 =	DIRA-B
6 =	DOA	16 =	D6B	25 =	CLEAR'
7 =	D1A	17 =	D5B	26 =	ACKIB'
8 =	D2A	18 =	D4B	27 =	RFDB
9 =	D3A	19 =	D3B	28 =	[VCC]
10 =	D4A				

Z8068: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[GND]	15 =	MFLG'	28 =	MR-W
2 =	SP0	16 =	MP0	29 =	SDS'
3 =	SP1	17 =	MP1	30 =	SCS'
4 =	SP2	18 =	MP2	31 =	SFLG'
5 =	SP3	19 =	MP3	32 =	AUX7
6 =	AUX0	20 =	[GND]	33 =	AUX6
7 =	AUX1	21 =	MP7	34 =	AUX5
8 =	AUX2	22 =	MP6	35 =	AUX4
9 =	AUX3	23 =	MP5	36 =	SP7
10 =	AFLG'	24 =	MP4	37 =	SP6
11 =	ASTB'	25 =	MCS'	38 =	SP5
12 =	PAR'	26 =	MDS'	39 =	SP4
13 =	C-K	27 =	MAS'	40 =	[VCC]
14 =	CLK				

Z8090: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	AD5	28 =	P17
2 =	PCLK	16 =	AD4	29 =	P34
3 =	P37	17 =	AD3	30 =	P33
4 =	P30	18 =	AD2	31 =	P20
5 =	P35	19 =	AD1	32 =	P21
6 =	P32	20 =	AD0	33 =	P22
7 =	DS'	21 =	P10	34 =	P23
8 =	R-W	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
0 =	CS'	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	WAIT'	26 =	P15	39 =	P36
13 =	AD7	27 =	P16	40 =	P31
14 =	AD6				

Z8094: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	AD5	28 =	P17
2 =	PCLK	16 =	AD4	29 =	P34
3 =	P37	17 =	AD3	30 =	P33
4 =	P30	18 =	AD2	31 =	P20
5 =	P35	19 =	AD1	32 =	P21
6 =	P32	20 =	AD0	33 =	P22
7 =	DS'	21 =	P10	34 =	P23
8 =	R-W	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	CS'	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	WAIT'	26 =	P15	39 =	P36
13 =	AD7	27 =	P16	40 =	P31
14 =	AD6				

Z8108: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	A10	15 =	AS'	28 =	AD2
2 =	A11	16 =	XTAL1	29 =	AD3
3 =	A12	17 =	XTALO	30 =	[GND]
4 =	A13	18 =	CLK	31 =	AD4
5 =	A14	19 =	WAIT'	32 =	AD5
6 =	A15	20 =	BUSACK	33 =	AD6
7 =	HALT'	21 =	[VCC]	34 =	AD7
8 =	WR'	22 =	RESET'	35 =	A16
9 =	RFSH'	23 =	BUSREQ	36 =	A17
10 =	IORQ'	24 =	NMI'	37 =	A18
11 =	[GND]	25 =	INTA'	38 =	A8
12 =	M1'	26 =	AD0	39 =	A9
13 =	MREQ'	27 =	AD1	40 =	[VCC]
14 =	RD'				

Z8116: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	AD10	15 =	AS'	28 =	AD2
2 =	AD11	16 =	XTAL1	29 =	AD3
3 =	AD12	17 =	XTALO	30 =	[GND]
4 =	AD13	18 =	CLK	31 =	AD4
5 =	AD14	19 =	WAIT'	32 =	AD5
6 =	AD15	20 =	BUSACK'	33 =	AD6
7 =	B-W	21 =	[VCC]	34 =	AD7
8 =	R-W	22 =	RESET'	35 =	A16
9 =	ST0	23 =	BUSREQ'	36 =	A17
10 =	ST1	24 =	NMI'	37 =	A18
11 =	[GND]	25 =	INTA'	38 =	AD8
12 =	ST2	26 =	AD0	39 =	AD9
13 =	ST3	27 =	AD1	40 =	[VCC]
14 =	DS'				

Z8400: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	A11	15 =	D1	28 =	RFSH'
2 =	A12	16 =	INT'	29 =	[GND]
3 =	A13	17 =	NMI'	30 =	A0
4 =	A14	18 =	HALT'	31 =	A1
5 =	A15	19 =	MREQ'	32 =	A2
6 =	CLK	20 =	IORQ'	33 =	A3
7 =	D4	21 =	RD'	34 =	A4
8 =	D3	22 =	WR'	35 =	A5
9 =	D5	23 =	BUSACK'	36 =	A6
10 =	D6	24 =	WAIT'	37 =	A7
11 =	[VCC]	25 =	BUSREQ'	38 =	A8
12 =	D2	26 =	RESET'	39 =	A9
13 =	D7	27 =	M1'	40 =	A10
14 =	D0				

Z84C00: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	A11	15 =	D1	28 =	RFSH'
2 =	A12	16 =	INT'	29 =	[GND]
3 =	A13	17 =	NMI'	30 =	A0
4 =	A14	18 =	HALT'	31 =	A1
5 =	A15	19 =	MREQ'	32 =	A2
6 =	CLK	20 =	IORQ'	33 =	A3
7 =	D4	21 =	RD'	34 =	A4
8 =	D3	22 =	WR'	35 =	A5
9 =	D5	23 =	BUSACK'	36 =	A6
10 =	D6	24 =	WAIT'	37 =	A7
11 =	[VCC]	25 =	BUSREQ'	38 =	A8
12 =	D2	26 =	RESET'	39 =	A9
13 =	D7	27 =	M1'	40 =	A10
14 =	D0				

Z8410: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = A5		15 = BUSREQ'		28 = D6	
2 = A4		16 = CE-WAIT'		29 = D5	
3 = A3		17 = A15		30 = [GND]	
4 = A2		18 = A14		31 = D4	
5 = A1		19 = A13		32 = D3	
6 = A0		20 = A12		33 = D2	
7 = CLK		21 = A11		34 = D1	
8 = WR'		22 = A10		35 = D0	
9 = RD'		23 = A9		36 = IEO	
10 = IORQ'		24 = A8		37 = INT-PLS'	
11 = [VCC]		25 = RDY		38 = IEI	
12 = MREQ'		26 = M1'		39 = A7	
13 = BAO'		27 = D7		40 = A6	
14 = BAI'					

Z8420: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D2		15 = PA0		28 = PB1	
2 = D7		16 = ASTB'		29 = PB2	
3 = D6		17 = BSTB'		30 = PB3	
4 = CE'		18 = ARDY		31 = PB4	
5 = C-D		19 = D0		32 = PB5	
6 = B-A		20 = D1		33 = PB6	
7 = PA7		21 = BRDY		34 = PB7	
8 = PA6		22 = IEO		35 = RD'	
9 = PA5		23 = INT'		36 = IORQ'	
10 = PA4		24 = IEI		37 = M1'	
11 = [GND]		25 = CLK		38 = D5	
12 = PA3		26 = [VCC]		39 = D4	
13 = PA2		27 = PB0		40 = D3	
14 = PA1					

Z84C20: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D2		15 = PA0		28 = PB1	
2 = D7		16 = ASTB'		29 = PB2	
3 = D6		17 = BSTB'		30 = PB3	
4 = CE'		18 = ARDY		31 = PB4	
5 = C-D		19 = D0		32 = PB5	
6 = B-A		20 = D1		33 = PB6	
7 = PA7		21 = BRDY		34 = PB7	
8 = PA6		22 = IEO		35 = RD'	
9 = PA5		23 = INT'		36 = IORQ'	
10 = PA4		24 = IEI		37 = M1'	
11 = [GND]		25 = CLK		38 = D5	
12 = PA3		26 = [VCC]		39 = D4	
13 = PA2		27 = PB0		40 = D3	
14 = PA1					

Z84C30: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D4		11 = IEO		20 = CLK-TRG3	
2 = D5		12 = INT'		21 = CLK-TRG2	
3 = D6		13 = IEI		22 = CLK-TRG1	
4 = D7		14 = M1'		23 = CLK-TRG0	
5 = [GND]		15 = CLK		24 = [VCC]	
6 = RD'		16 = CE'		25 = D0	
7 = ZC-T00		17 = RESET'		26 = D1	
8 = ZC-T01		18 = CS0		27 = D2	
9 = ZC-T02		19 = CS1		28 = D3	
10 = IORQ'					

Z84C30: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D4		11 = IEO		20 = CLK-TRG3	
2 = D5		12 = INT'		21 = CLK-TRG2	
3 = D6		13 = IEI		22 = CLK-TRG1	
4 = D7		14 = M1'		23 = CLK-TRG0	
5 = [GND]		15 = CLK		24 = [VCC]	
6 = RD'		16 = CE'		25 = D0	
7 = ZC-T00		17 = RESET'		26 = D1	
8 = ZC-T01		18 = CS0		27 = D2	
9 = ZC-T02		19 = CS1		28 = D3	
10 = IORQ'					

Z8440: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D1		15 = TXDA		28 = RXDB	
2 = D3		16 = DTRA'		29 = SYNCB'	
3 = D5		17 = RTSA'		30 = W-RDYB'	
4 = D7		18 = CTSA'		31 = [GND]	
5 = INT'		19 = DCDA'		32 = RD'	
6 = IEI		20 = CLK		33 = C-D	
7 = IEO		21 = RESET'		34 = B-A	
8 = M1'		22 = DCDB'		35 = CE'	
9 = [VCC]		23 = CTSB'		36 = IORQ'	
10 = W-RDYA'		24 = RTSB'		37 = D6	
11 = SYNCA'		25 = DTRB'		38 = D4	
12 = RXDA		26 = TXDB		39 = D2	
13 = RXCA'		27 = RXTXCB'		40 = D0	
14 = TXCA'					

Z84C40: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D1		15 = TXDA		28 = RXDB	
2 = D3		16 = DTRA'		29 = SYNCB'	
3 = D5		17 = RTSA'		30 = W-RDYB'	
4 = D7		18 = CTSA'		31 = [GND]	
5 = INT'		19 = DCDA'		32 = RD'	
6 = IEI		20 = CLK		33 = C-D	
7 = IEO		21 = RESET'		34 = B-A	
8 = M1'		22 = DCDB'		35 = CE'	
9 = [VCC]		23 = CTSB'		36 = IORQ'	
10 = W-RDYA'		24 = RTSB'		37 = D6	
11 = SYNCA'		25 = DTRB'		38 = D4	
12 = RXDA		26 = TXDB		39 = D2	
13 = RXCA'		27 = RXTXCB'		40 = D0	
14 = TXCA'					

Z8441: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	D1	15 =	TXDA	28 =	RXDB
2 =	D3	16 =	DTRA'	29 =	SYNCB'
3 =	D5	17 =	RTSA'	30 =	W-RDYB'
4 =	D7	18 =	CTSA'	31 =	[GND]
5 =	INT'	19 =	DCDA'	32 =	RD'
6 =	IEI	20 =	CLK	33 =	C-D
7 =	IEO	21 =	RESET'	34 =	B-A
8 =	M1'	22 =	DCDB'	35 =	CE'
9 =	[VCC]	23 =	CTSB'	36 =	IORQ'
10 =	W-RDYA'	24 =	RTSB'	37 =	D6
11 =	SYNCA'	25 =	TXDB	38 =	D4
12 =	RXDA	26 =	TXCB'	39 =	D2
13 =	RXCA'	27 =	RXCB'	40 =	D0
14 =	TXCA'				

Z84C41: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	D1	15 =	TXDA	28 =	RXDB
2 =	D3	16 =	DTRA'	29 =	SYNCB'
3 =	D5	17 =	RTSA'	30 =	W-RDYB'
4 =	D7	18 =	CTSA'	31 =	[GND]
5 =	INT'	19 =	DCDA'	32 =	RD'
6 =	IEI	20 =	CLK	33 =	C-D
7 =	IEO	21 =	RESET'	34 =	B-A
8 =	M1'	22 =	DCDB'	35 =	CE'
9 =	[VCC]	23 =	CTSB'	36 =	IORQ'
10 =	W-RDYA'	24 =	RTSB'	37 =	D6
11 =	SYNCA'	25 =	TXDB	38 =	D4
12 =	RXDA	26 =	TXCB'	39 =	D2
13 =	RXCA'	27 =	RXCB'	40 =	D0
14 =	TXCA'				

Z8442: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D1		15 = TXDA		28 = RXCB'	
2 = D3		16 = DTRA'		29 = RXDB	
3 = D5		17 = RTSA'		30 = W-RDYB'	
4 = D7		18 = CTSA'		31 = [GND]	
5 = INT'		19 = DCDA'		32 = RD'	
6 = IEI		20 = CLK		33 = C-D	
7 = IEO		21 = RESET'		34 = B-A	
8 = M1'		22 = DCDB'		35 = CE'	
9 = [VCC]		23 = CTSB'		36 = IORQ'	
10 = W-RDYA'		24 = RTSB'		37 = D6	
11 = SYNCA'		25 = DTRB'		38 = D4	
12 = RXDA		26 = TXDB		39 = D2	
13 = RXCA'		27 = TXCB'		40 = D0	
14 = TXCA'					

Z84C42: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D1		15 = TXDA		28 = RXCB'	
2 = D3		16 = DTRA'		29 = RXDB	
3 = D5		17 = RTSA'		30 = W-RDYB'	
4 = D7		18 = CTSA'		31 = [GND]	
5 = INT'		19 = DCDA'		32 = RD'	
6 = IEI		20 = CLK		33 = C-D	
7 = IEO		21 = RESET'		34 = B-A	
8 = M1'		22 = DCDB'		35 = CE'	
9 = [VCC]		23 = CTSB'		36 = IORQ'	
10 = W-RDYA'		24 = RTSB'		37 = D6	
11 = SYNCA'		25 = DTRB'		38 = D4	
12 = RXDA		26 = TXDB		39 = D2	
13 = RXCA'		27 = TXCB'		40 = D0	
14 = TXCA'					

Z8470: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	D1	15 =	TXDA	28 =	RXDB
2 =	D3	16 =	DTRA'	29 =	RIB'
3 =	D5	17 =	RTSA'	30 =	W-RDYB'
4 =	D7	18 =	CTSA'	31 =	[GND]
5 =	INT'	19 =	DCDA'	32 =	RD'
6 =	IEI	20 =	CLK	33 =	C-D
7 =	IEO	21 =	RESET'	34 =	B-A
8 =	M1'	22 =	DCDB'	35 =	CE'
9 =	[VCC]	23 =	CTSB'	36 =	IORQ'
10 =	W-RDYA'	24 =	RTSB'	37 =	D6
11 =	RIA'	25 =	DTRB'	38 =	D4
12 =	RXDA	26 =	TXDB	39 =	D2
13 =	RXCA'	27 =	RXTXCB'	40 =	D0
14 =	TXCA'				

Z8516: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	INT'	17 =	AD12	33 =	TBEN'
2 =	BAI	18 =	AD13	34 =	WAIT'
3 =	BUSREQ	19 =	AD14	35 =	B-W
4 =	[VCC]	20 =	AD15	36 =	DREQ1'
5 =	AD0	21 =	A23	37 =	DREQ2'
6 =	AD1	22 =	A22	38 =	EOP'
7 =	AD2	23 =	A21	39 =	DACK2'
8 =	AD3	24 =	A20	40 =	DACK1'
9 =	AD4	25 =	A19	41 =	R-W
10 =	AD5	26 =	[GND]	42 =	CS'
11 =	AD6	27 =	A18	43 =	DS'
12 =	AD7	28 =	A17	44 =	P-D
13 =	AD8	29 =	A16	45 =	ALE
14 =	AD9	30 =	N-S	46 =	CLK
15 =	AD10	31 =	M-IO	47 =	RESET'
16 =	AD11	32 =	RBEN'	48 =	INTACK'

Z8530: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D1		15 = TXDA		28 = RTXCB'	
2 = D3		16 = DTR-RQA'		29 = SYNCB'	
3 = D5		17 = RTSA'		30 = W-REQB'	
4 = D7		18 = CTSA'		31 = [GND]	
5 = INT'		19 = DCDA'		32 = D-C	
6 = IEO		20 = PCLK		33 = CE'	
7 = IEI		21 = DCDB'		34 = A-B	
8 = INTACK'		22 = CTSB'		35 = WR'	
9 = [VCC]		23 = RTSB'		36 = RD'	
10 = W-REQA'		24 = DTR-RQB'		37 = D6	
11 = SYNCA'		25 = TXDB		38 = D4	
12 = RTXCA'		26 = TRXCB'		39 = D2	
13 = RXDA		27 = RXDB		40 = D0	
14 = TRXCA'					

Z8531: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = D1		15 = TXDA		28 = RTXCB'	
2 = D3		16 = DTR-RQA'		29 = RIB'	
3 = D5		17 = RTSA'		30 = W-REQB'	
4 = D7		18 = CTSA'		31 = [GND]	
5 = INT'		19 = DCDA'		32 = D-C	
6 = IEO		20 = PCLK		33 = CE'	
7 = IEI		21 = DCDB'		34 = A-B	
8 = INTACK'		22 = CTSB'		35 = WR'	
9 = [VCC]		23 = RTSB'		36 = RD'	
10 = W-REQA'		24 = DTR-RQB'		37 = D6	
11 = RIA'		25 = TXDB		38 = D4	
12 = RTXCA'		26 = TRXCB'		39 = D2	
13 = RXDA		27 = RXDB		40 = D0	
14 = TRXCA'					

Z8536: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	D4	15 =	PB7	28 =	PA5
2 =	D5	16 =	PCLK	29 =	PA4
3 =	D6	17 =	IEI	30 =	PA3
4 =	D7	18 =	IEO	31 =	PA2
5 =	RD'	19 =	PC0	32 =	PA1
6 =	WR'	20 =	PC1	33 =	PA0
7 =	[GND]	21 =	PC2	34 =	A0
8 =	PB0	22 =	PC3	35 =	A1
9 =	PB1	23 =	[VCC]	36 =	CE'
10 =	PB2	24 =	INT'	37 =	D0
11 =	PB3	25 =	INTACK'	38 =	D1
12 =	PB4	26 =	PA7	39 =	D2
13 =	PB5	27 =	PA6	40 =	D3
14 =	PB6				

Z8581: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	XTL1A	7 =	ADD2'	13 =	TCLK
2 =	XTL1B	8 =	STRT'	14 =	[GND]
3 =	STRH'	9 =	C0	15 =	ZCLK
4 =	INH'	10 =	C1	16 =	OSC
5 =	[VCC]	11 =	XTL2B	17 =	RSTO'
6 =	ADD1'	12 =	XTL2A	18 =	RSTI'

Z8590: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	DB5	28 =	P17
2 =	PCLK	16 =	DB4	29 =	P34
3 =	P37	17 =	DB3	30 =	P33
4 =	P30	18 =	DB2	31 =	P20
5 =	P35	19 =	DB1	32 =	P21
6 =	P32	20 =	DB0	33 =	P22
7 =	RD'	21 =	P10	34 =	P23
8 =	WR'	22 =	P11	35 =	P24
9 =	A-D	23 =	P12	36 =	P25
10 =	CS'	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	WAIT'	26 =	P15	39 =	P36
13 =	DB7	27 =	P16	40 =	P31
14 =	DB6				

Z8594: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	DB5	28 =	P17
2 =	PCLK	16 =	DB4	29 =	P34
3 =	P37	17 =	DB3	30 =	P33
4 =	P30	18 =	DB2	31 =	P20
5 =	P35	19 =	DB1	32 =	P21
6 =	P32	20 =	DB0	33 =	P22
7 =	RD'	21 =	P10	34 =	P23
8 =	WR'	22 =	P11	35 =	P24
9 =	A-D	23 =	P12	36 =	P25
10 =	CS'	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	WAIT'	26 =	P15	39 =	P36
13 =	DB7	27 =	P16	40 =	P31
14 =	DB6				

Z8601: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8603: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8611: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8613: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8671: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8681: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8682: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	[VCC]	15 =	P02	28 =	P17
2 =	XTAL2	16 =	P03	29 =	P34
3 =	XTAL1	17 =	P04	30 =	P33
4 =	P37	18 =	P05	31 =	P20
5 =	P30	19 =	P06	32 =	P21
6 =	RESET'	20 =	P07	33 =	P22
7 =	R-W	21 =	P10	34 =	P23
8 =	DS'	22 =	P11	35 =	P24
9 =	AS'	23 =	P12	36 =	P25
10 =	P35	24 =	P13	37 =	P26
11 =	[GND]	25 =	P14	38 =	P27
12 =	P32	26 =	P15	39 =	P31
13 =	P00	27 =	P16	40 =	P36
14 =	P01				

Z8800: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		17 = P47		33 = P42	
2 = P11		18 = P22		34 = [GND]	
3 = P12		19 = P32		35 = P41	
4 = P13		20 = P33		36 = P40	
5 = P14		21 = P23		37 = DS'	
6 = P15		22 = P20		38 = AS'	
7 = P16		23 = P21		39 = P35	
8 = P17		24 = P31		40 = P34	
9 = P24		25 = P30		41 = P07	
10 = P25		26 = P26		42 = P06	
11 = [VCC]		27 = P27		43 = P05	
12 = XTAL2		28 = P37		44 = P04	
13 = XTAL1		29 = P36		45 = P03	
14 = P44		30 = RESET'		46 = P02	
15 = P45		31 = R-W		47 = P01	
16 = P46		32 = P43		48 = P00	

Z8801: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		15 = P32		28 = [GND]	
2 = P11		16 = P33		29 = DS'	
3 = P12		17 = P23		30 = AS'	
4 = P13		18 = P20		31 = P35	
5 = P14		19 = P21		32 = P34	
6 = P15		20 = P31		33 = P07	
7 = P16		21 = P30		34 = P06	
8 = P17		22 = P26		35 = P05	
9 = P24		23 = P27		36 = P04	
10 = P25		24 = P37		37 = P03	
11 = [VCC]		25 = P36		38 = P02	
12 = XTAL2		26 = RESET'		39 = P01	
13 = XTAL1		27 = R-W		40 = P00	
14 = P22					

Z8810: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		17 = P47		33 = P42	
2 = P11		18 = P22		34 = [GND]	
3 = P12		19 = P32		35 = P41	
4 = P13		20 = P33		36 = P40	
5 = P14		21 = P23		37 = DS'	
6 = P15		22 = P20		38 = AS'	
7 = P16		23 = P21		39 = P35	
8 = P17		24 = P31		40 = P34	
9 = P24		25 = P30		41 = P07	
10 = P25		26 = P26		42 = P06	
11 = [VCC]		27 = P27		43 = P05	
12 = XTAL2		28 = P37		44 = P04	
13 = XTAL1		29 = P36		45 = P03	
14 = P44		30 = RESET'		46 = P02	
15 = P45		31 = R-W		47 = P01	
16 = P46		32 = P43		48 = P00	

Z8811: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		15 = P32		28 = [GND]	
2 = P11		16 = P33		29 = DS'	
3 = P12		17 = P23		30 = AS'	
4 = P13		18 = P20		31 = P35	
5 = P14		19 = P21		32 = P34	
6 = P15		20 = P31		33 = P07	
7 = P16		21 = P30		34 = P06	
8 = P17		22 = P26		35 = P05	
9 = P24		23 = P27		36 = P04	
10 = P25		24 = P37		37 = P03	
11 = [VCC]		25 = P36		38 = P02	
12 = XTAL2		26 = RESET'		39 = P01	
13 = XTAL1		27 = R-W		40 = P00	
14 = P22					

Z8812: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		17 = P47		33 = P42	
2 = P11		18 = P22		34 = [GND]	
3 = P12		19 = P32		35 = P41	
4 = P13		20 = P33		36 = P40	
5 = P14		21 = P23		37 = DS'	
6 = P15		22 = P20		38 = AS'	
7 = P16		23 = P21		39 = P35	
8 = P17		24 = P31		40 = P34	
9 = P24		25 = P30		41 = P07	
10 = P25		26 = P26		42 = P06	
11 = [VCC]		27 = P27		43 = P05	
12 = XTAL2		28 = P37		44 = P04	
13 = XTAL1		29 = P36		45 = P03	
14 = P44		30 = RESET'		46 = P02	
15 = P45		31 = R-W		47 = P01	
16 = P46		32 = P43		48 = P00	

Z8813: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		15 = P32		28 = [GND]	
2 = P11		16 = P33		29 = DS'	
3 = P12		17 = P23		30 = AS'	
4 = P13		18 = P20		31 = P35	
5 = P14		19 = P21		32 = P34	
6 = P15		20 = P31		33 = P07	
7 = P16		21 = P30		34 = P06	
8 = P17		22 = P26		35 = P05	
9 = P24		23 = P27		36 = P04	
10 = P25		24 = P37		37 = P03	
11 = [VCC]		25 = P36		38 = P02	
12 = XTAL2		26 = RESET'		39 = P01	
13 = XTAL1		27 = R-W		40 = P00	
14 = P22					

Z8820: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	P10	17 =	P47	33 =	P42
2 =	P11	18 =	P22	34 =	[GND]
3 =	P12	19 =	P32	35 =	P41
4 =	P13	20 =	P33	36 =	P40
5 =	P14	21 =	P23	37 =	DS'
6 =	P15	22 =	P20	38 =	AS'
7 =	P16	23 =	P21	39 =	P35
8 =	P17	24 =	P31	40 =	P34
9 =	P24	25 =	P30	41 =	P07
10 =	P25	26 =	P26	42 =	P06
11 =	[VCC]	27 =	P27	43 =	P05
12 =	XTAL2	28 =	P37	44 =	P04
13 =	XTAL1	29 =	P36	45 =	P03
14 =	P44	30 =	RESET'	46 =	P02
15 =	P45	31 =	R-W	47 =	P01
16 =	P46	32 =	P43	48 =	P00

Z8821: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 =	P10	15 =	P32	28 =	[GND]
2 =	P11	16 =	P33	29 =	DS'
3 =	P12	17 =	P23	30 =	AS'
4 =	P13	18 =	P20	31 =	P35
5 =	P14	19 =	P21	32 =	P34
6 =	P15	20 =	P31	33 =	P07
7 =	P16	21 =	P30	34 =	P06
8 =	P17	22 =	P26	35 =	P05
9 =	P24	23 =	P27	36 =	P04
10 =	P25	24 =	P37	37 =	P03
11 =	[VCC]	25 =	P36	38 =	P02
12 =	XTAL2	26 =	RESET'	39 =	P01
13 =	XTAL1	27 =	R-W	40 =	P00
14 =	P22				

Z8822: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		17 = P47		33 = P42	
2 = P11		18 = P22		34 = [GND]	
3 = P12		19 = P32		35 = P41	
4 = P13		20 = P33		36 = P40	
5 = P14		21 = P23		37 = DS'	
6 = P15		22 = P20		38 = AS'	
7 = P16		23 = P21		39 = P35	
8 = P17		24 = P31		40 = P34	
9 = P24		25 = P30		41 = P07	
10 = P25		26 = P26		42 = P06	
11 = [VCC]		27 = P27		43 = P05	
12 = XTAL2		28 = P37		44 = P04	
13 = XTAL1		29 = P36		45 = P03	
14 = P44		30 = RESET'		46 = P02	
15 = P45		31 = R-W		47 = P01	
16 = P46		32 = P43		48 = P00	

Z8823: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		15 = P32		28 = [GND]	
2 = P11		16 = P33		29 = DS'	
3 = P12		17 = P23		30 = AS'	
4 = P13		18 = P20		31 = P35	
5 = P14		19 = P21		32 = P34	
6 = P15		20 = P31		33 = P07	
7 = P16		21 = P30		34 = P06	
8 = P17		22 = P26		35 = P05	
9 = P24		23 = P27		36 = P04	
10 = P25		24 = P37		37 = P03	
11 = [VCC]		25 = P36		38 = P02	
12 = XTAL2		26 = RESET'		39 = P01	
13 = XTAL1		27 = R-W		40 = P00	
14 = P22					

Z8830: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		17 = P47		33 = P42	
2 = P11		18 = P22		34 = [GND]	
3 = P12		19 = P32		35 = P41	
4 = P13		20 = P33		36 = P40	
5 = P14		21 = P23		37 = DS'	
6 = P15		22 = P20		38 = AS'	
7 = P16		23 = P21		39 = P35	
8 = P17		24 = P31		40 = P34	
9 = P24		25 = P30		41 = P07	
10 = P25		26 = P26		42 = P06	
11 = [VCC]		27 = P27		43 = P05	
12 = XTAL2		28 = P37		44 = P04	
13 = XTAL1		29 = P36		45 = P03	
14 = P44		30 = RESET'		46 = P02	
15 = P45		31 = R-W		47 = P01	
16 = P46		32 = P43		48 = P00	

Z8831: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		15 = P32		28 = [GND]	
2 = P11		16 = P33		29 = DS'	
3 = P12		17 = P23		30 = AS'	
4 = P13		18 = P20		31 = P35	
5 = P14		19 = P21		32 = P34	
6 = P15		20 = P31		33 = P07	
7 = P16		21 = P30		34 = P06	
8 = P17		22 = P26		35 = P05	
9 = P24		23 = P27		36 = P04	
10 = P25		24 = P37		37 = P03	
11 = [VCC]		25 = P36		38 = P02	
12 = XTAL2		26 = RESET'		39 = P01	
13 = XTAL1		27 = R-W		40 = P00	
14 = P22					

Z8832: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		17 = P47		33 = P42	
2 = P11		18 = P22		34 = [GND]	
3 = P12		19 = P32		35 = P41	
4 = P13		20 = P33		36 = P40	
5 = P14		21 = P23		37 = DS'	
6 = P15		22 = P20		38 = AS'	
7 = P16		23 = P21		39 = P35	
8 = P17		24 = P31		40 = P34	
9 = P24		25 = P30		41 = P07	
10 = P25		26 = P26		42 = P06	
11 = [VCC]		27 = P27		43 = P05	
12 = XTAL2		28 = P37		44 = P04	
13 = XTAL1		29 = P36		45 = P03	
14 = P44		30 = RESET'		46 = P02	
15 = P45		31 = R-W		47 = P01	
16 = P46		32 = P43		48 = P00	

Z8833: NUMBER OF GATES PER PACKAGE = 1

<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>	<u>PIN</u>	<u>SIGNAL</u>
1 = P10		15 = P32		28 = [GND]	
2 = P11		16 = P33		29 = DS'	
3 = P12		17 = P23		30 = AS'	
4 = P13		18 = P20		31 = P35	
5 = P14		19 = P21		32 = P34	
6 = P15		20 = P31		33 = P07	
7 = P16		21 = P30		34 = P06	
8 = P17		22 = P26		35 = P05	
9 = P24		23 = P27		36 = P04	
10 = P25		24 = P37		37 = P03	
11 = [VCC]		25 = P36		38 = P02	
12 = XTAL2		26 = RESET'		39 = P01	
13 = XTAL1		27 = R-W		40 = P00	
14 = P22					

COMPONENT PLOTS

Plot 1

ZB010		ZB038	
ZB004		ZB036	
ZB003		ZB031	
ZB002		ZB030	
ZB001		ZB016	
ZB001		ZB015	
Z765A		ZB010	

COMPONENT PLOTS

Plot 2

ZB400 ZB0 CPU	ZB4C00 ZB0C CPU
ZB116	ZB442 ZB0 SIO/2
ZB108	ZB441 ZB0 SIO/1
ZB094	ZB440 ZB0 SIO/0
ZB090	ZB430 ZB0 CTC
ZB068	ZB420 ZB0 PIO
ZB060	ZB410 ZB0 DMA

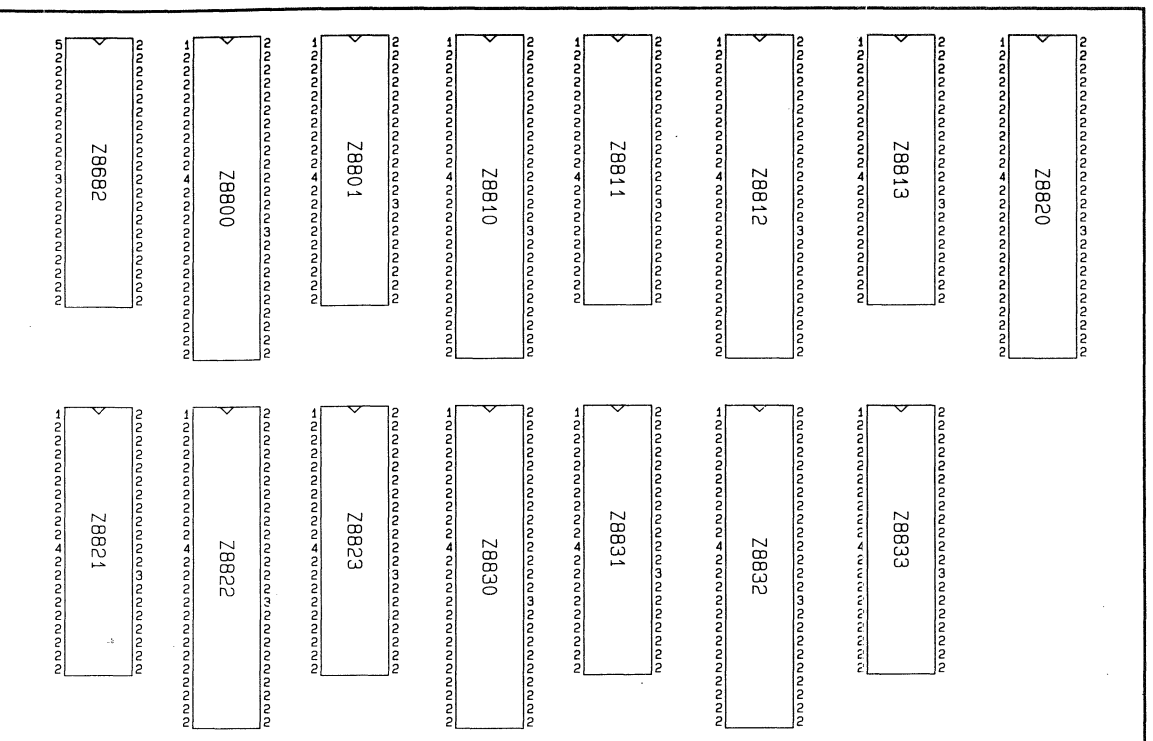
COMPONENT PLOTS

Plot 3

Z8536	Z8681
Z8531	Z8671
Z8530	Z8613
Z8516	Z8611
Z84C42 Z80C S10/2	Z8603
Z84C41 Z80C S10/1	Z8601
Z84C40 Z80C S10/0	Z8594
Z84C30 Z80C CTC	Z8590
Z84C20 Z80C PIO	Z8581

COMPONENT PLOTS

Plot 4



GERBER PHOTO PLOTTER APERTURE CHART

LAYER	TYPE 0 V50R28C.PS	TYPE 2 (N/C) 60R32C.PS	TYPE 3 (N/C) 60R32G.PS	TYPE 4 (N/C) 60R32P.PS
PADCOM	.050 Circle	.060 Circle	.060 Circle	.060 Circle
FLCOMP	Aperture 15	Aperture 9	Aperture 9	Aperture 9
PADSLD	.050 Circle	.060 Circle	.060 Circle	.060 Circle
FLSOLD	Aperture 15	Aperture 9	Aperture 9	Aperture 9
PADINT	.050 Circle	.060 Circle	.060 Circle	.060 Circle
FLINT	Aperture 15	Aperture 9	Aperture 9	Aperture 9
GNDCON	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X .100 Outer Diam	.020 Ring .060 Inner Diam
FLGCON	Aperture 8	Aperture 8	Aperture 22	Aperture 8
CLEAR	.100 Circle Solid Circle	.125 Circle Solid Circle	.125 Circle Solid Circle	.125 Circle Solid Circle
FLCLER	Aperture 20	Aperture 21	Aperture 21	Aperture 21
PWRCON	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X
FLPCON	Aperture 8	Aperture 8	Aperture 8	Aperture 22
SLDMSK	.060 Circle	.070 Circle	.070 Circle	.070 Circle
FLSMSK	Aperture 9	Aperture 11	Aperture 11	Aperture 11
DRILL	+28	+32	+32	+32
FLDRLL	Aperture 23 Text 28	Aperture 23 Text 32	Aperture 23 Text 32	Aperture 23 Text 32
PIN*	.050	.050	.050	.050

* The pin layer reflects connectivity (C) with a solid circle or no connectivity (N) with a hollow circle.

GERBER PHOTO PLOTTER APERTURE CHART (Continued)

LAYER	TYPE 1 (N/C) 60S32C.PS	TYPE 5 (N/C) 60S32P.PS	TYPE 6 (N/C) 60S32G.PS
PADCOM	.060 Square	.060 Square	.060 Square
FLCOMP	Aperture 10	Aperture 10	Aperture 10
PADSLD	.060 Square	.060 Square	.060 Square
FLSOLD	Aperture 10	Aperture 10	Aperture 10
PADINT	.060 Circle	.060 Circle	.060 Circle
FLINT	Aperture 9	Aperture 9	Aperture 9
GNDCON	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X
FLGCON	Aperture 8	Aperture 8	Aperture 22
CLEAR	.125 Circle Solid Circle	.125 Circle Solid Circle	.125 Circle Solid Circle
FLCLER	Aperture 21	Aperture 21	Aperture 21
PWRCON	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X .100 Outer Diam	.020 Ring .060 Inner Diam
FLPCON	Aperture 8	Aperture 22	Aperture 8
SLDMSK	.070 Square	.070 Square	.070 Square
FLSMSK	Aperture 12	Aperture 12	Aperture 12
DRILL	+32	+32	+32
FLDRLL	Aperture 23 Text 32	Aperture 23 Text 32	Aperture 23 Text 32
PIN*	.050	.050	.050

* The pin layer reflects connectivity (C) with a solid circle or no connectivity (N) with a hollow circle.