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DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

JULY 1985

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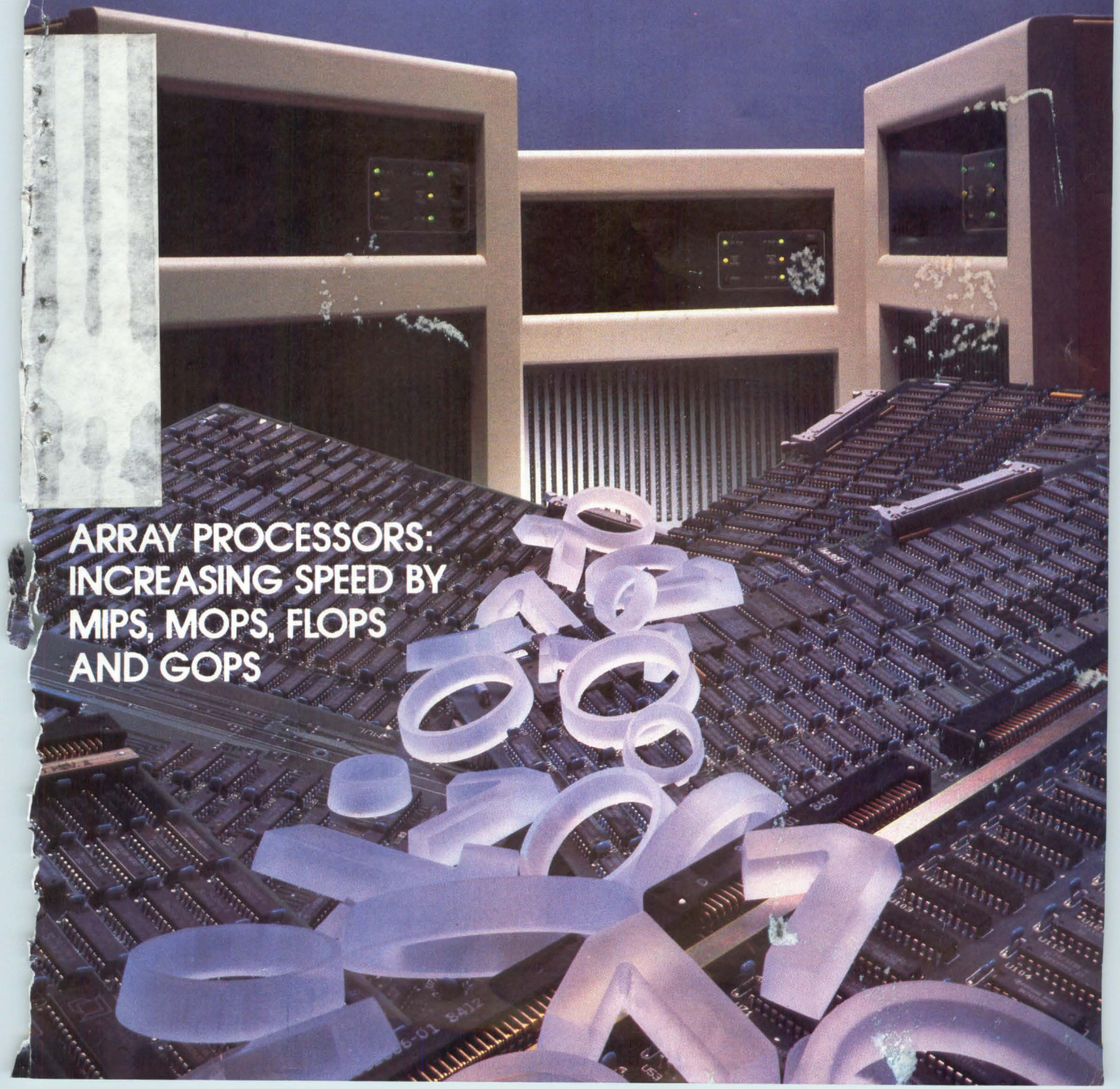
- OPENING THE SIMULATION BOTTLENECK



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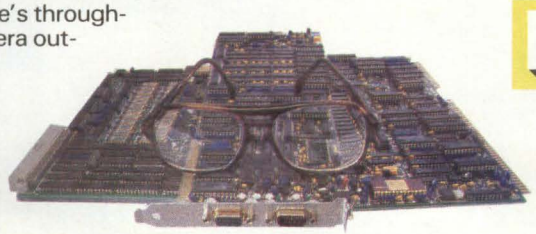

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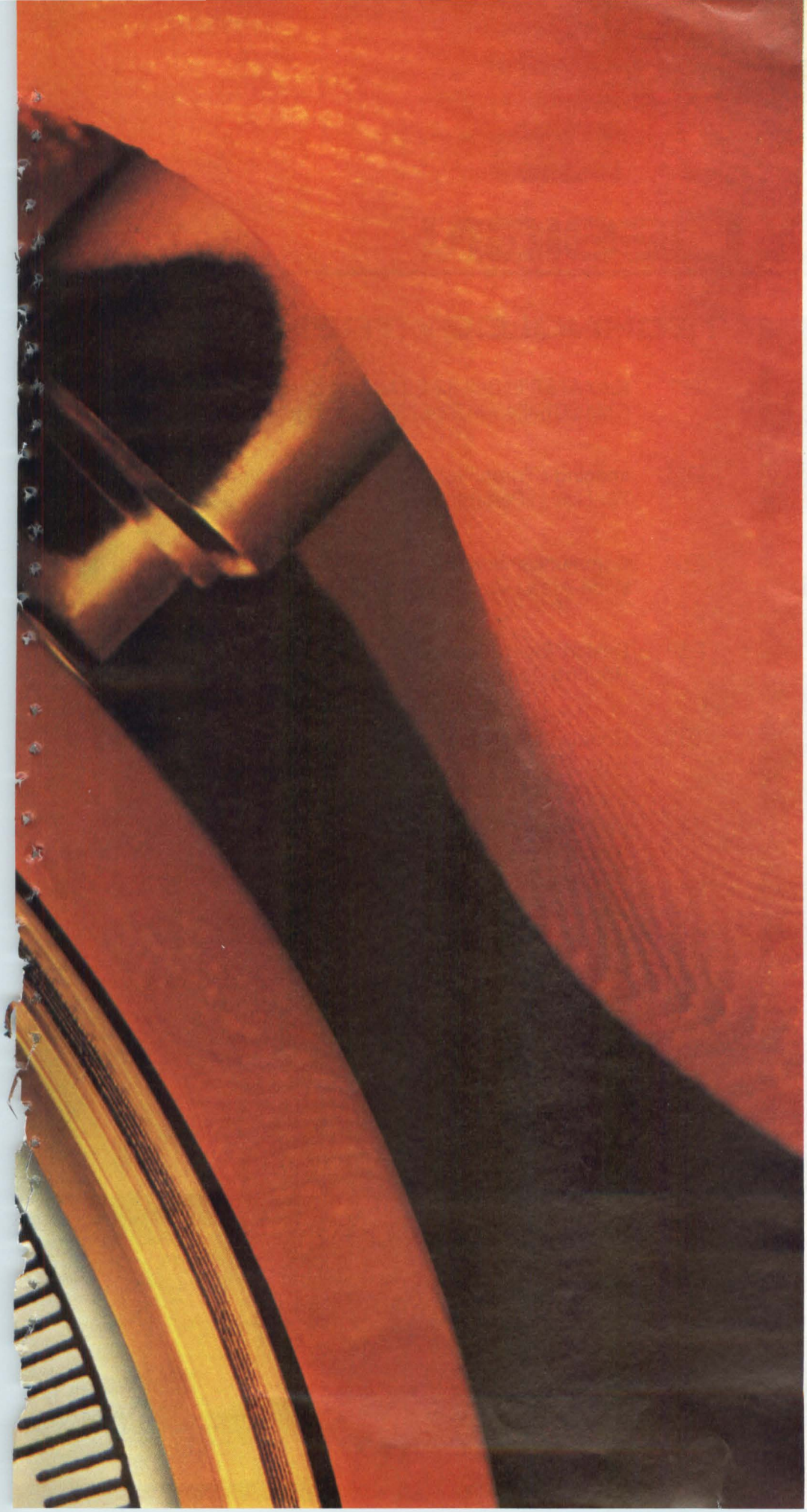

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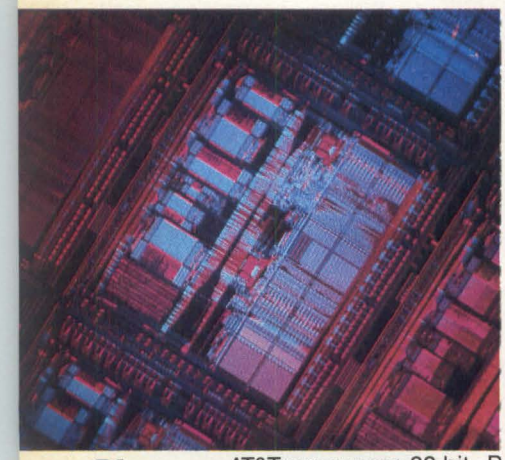

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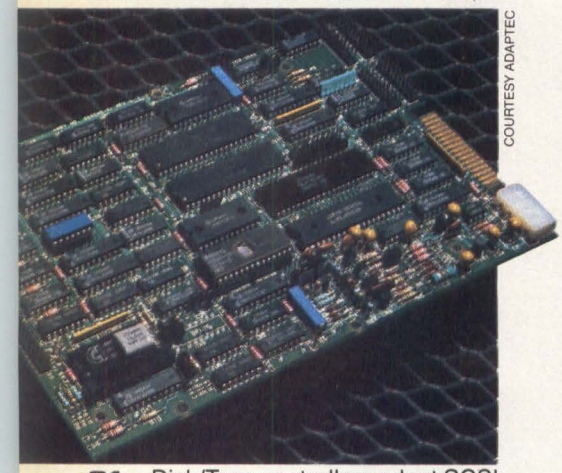

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ON THE COVER

The new generation of array processors, like the Numerix MARS 432 on the cover, is finding uses in a variety of medical, seismic, scientific and signal processing applications. The MARS 432 array processor features a 30 Mflop processor, 64 Mbytes internal memory plus application libraries and Fortran compilers. John Owens photo courtesy of Numerix Corp., 20 Ossipee Rd., Newton, MA 02164 (617) 964-2500.

Published monthly thirteen times a year with two issues in November. Subscription rates for non-qualified subscribers (US and Canada) — $40/yr; foreign — surface mail — $50/yr; airmail — $85/yr. Single copies — $4.

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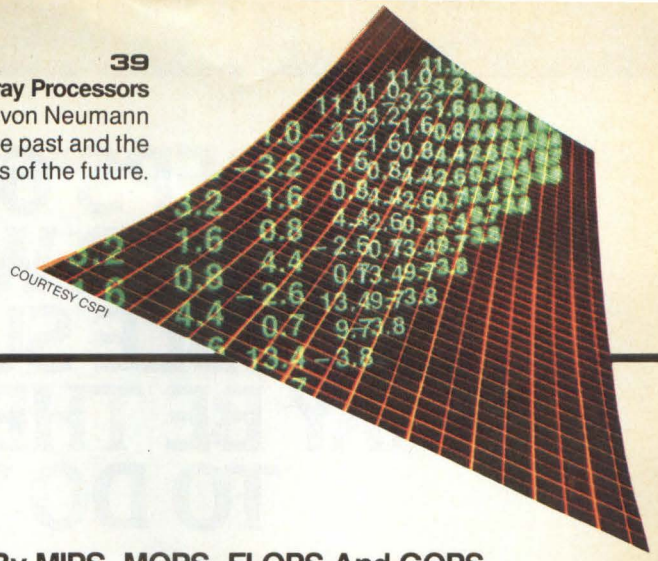
A bridge between the von Neumann architectures of the past and the SIMD/MIMD machines of the future.



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Logic simulation is a highly CPU-intensive circuit design verification task that is an essential element in the design cycle.

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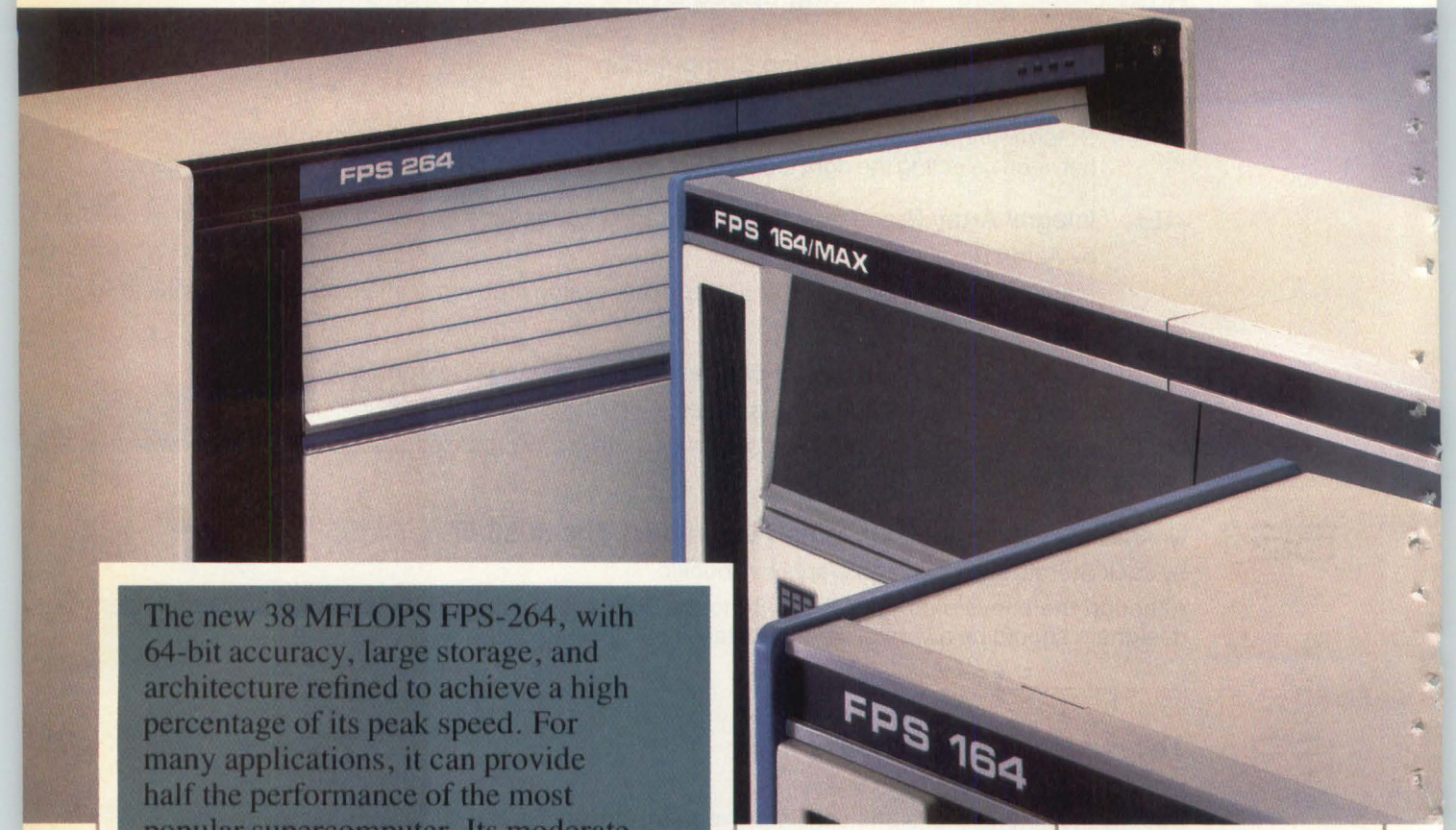

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Maximum disk storage capacity	16 Gbytes	3 Gbytes	3 Gbytes
Precision	15 decimal digits	15 decimal digits	15 decimal digits
Vector registers	4 x 2K	124 x 2K (max.)	4 x 2K
Scalar registers	64	184 (max.)	64
Host interfaces	IBM, DEC	IBM, DEC, Sperry, Apollo	
Program Development Software	FORTRAN Compiler, Overlay Linker, Assembler, Object Librarian, Interactive Debugger.		

Family Performance Measures

	FPS-264	FPS-164/MAX		FPS-164
		15 accelerators	1 accelerator	
Peak MFLOPS	38	341	33	11
Peak MOPS	190	1705	165	55
Peak MIPS (Instructions are multi-parcel)	19	5.5	5.5	5.5
Typical MFLOPS, LINPACK Benchmark	9.9	20.0	6.0	2.6
Whetstones, KWIPS (64-bit)	19,000	5440	5440	5440
1000x1000 matrix multiply, seconds	53	10	66	189
$K/MFLOPS (system price/peak speed)	$17K	$2.5K	$12K	$27K

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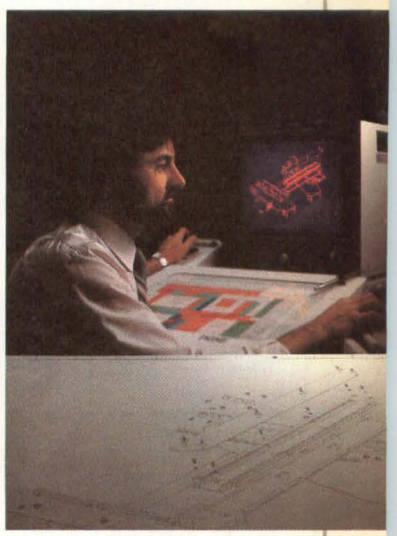

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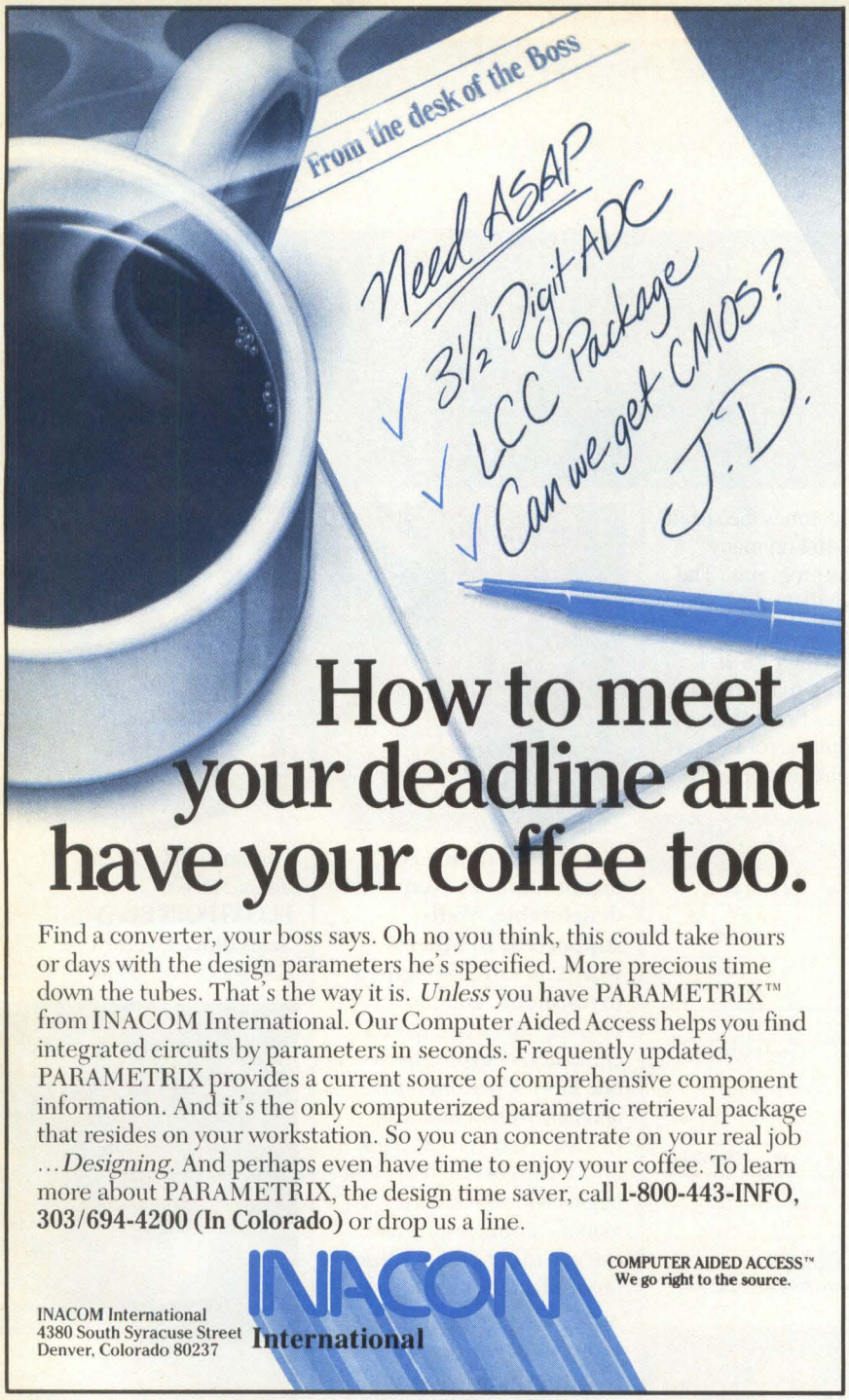

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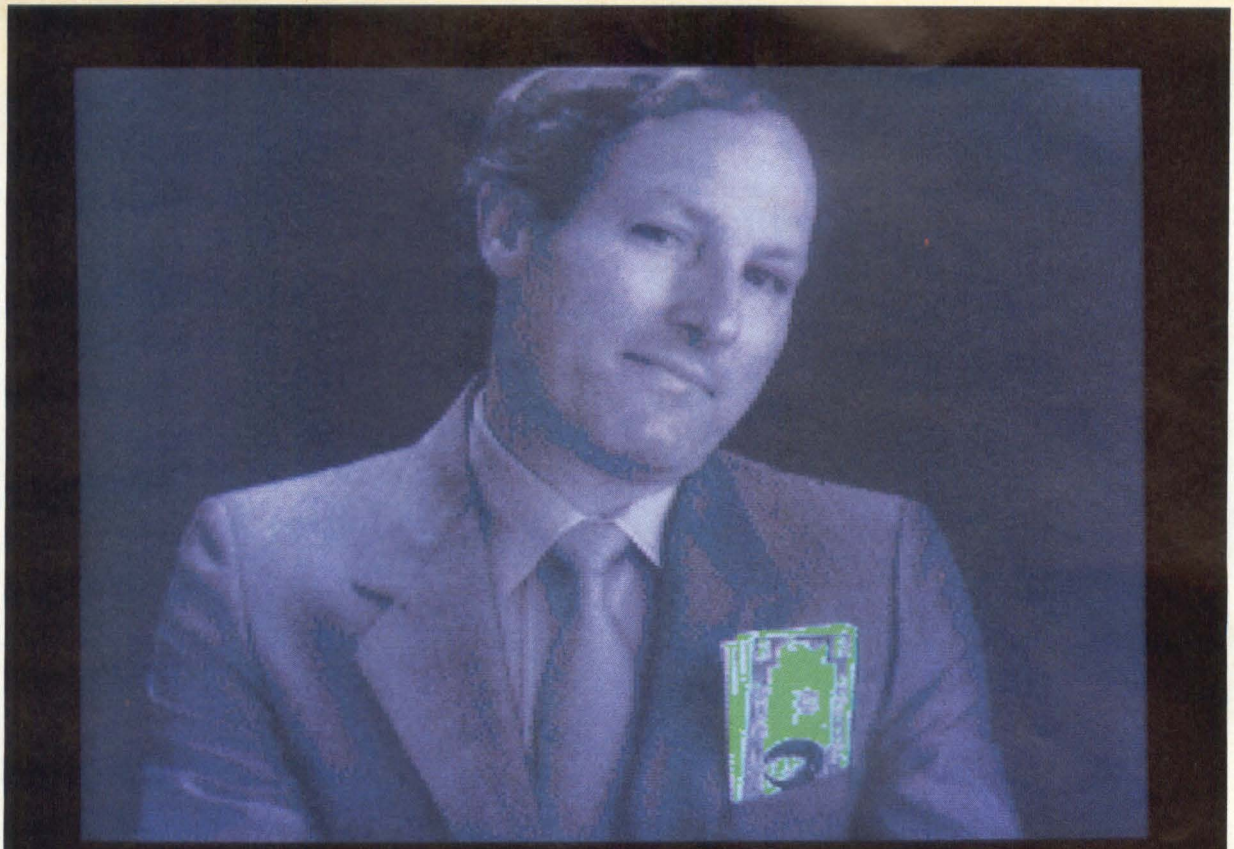

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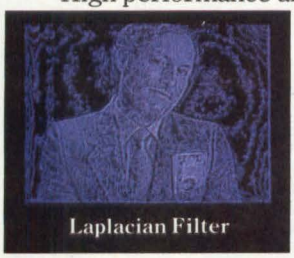

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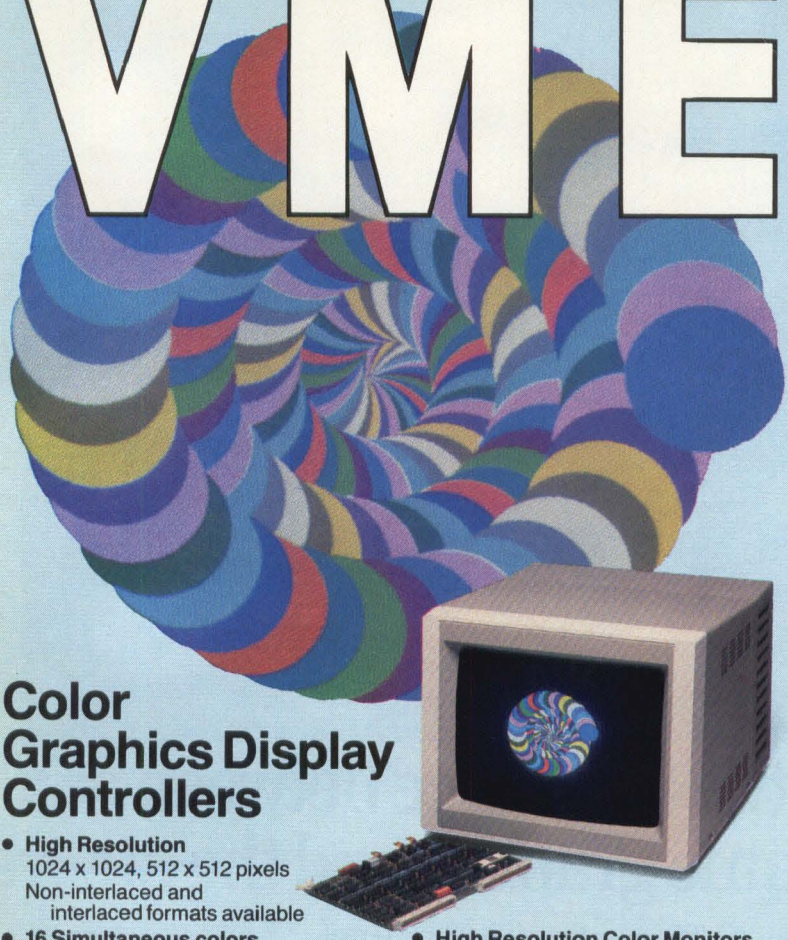

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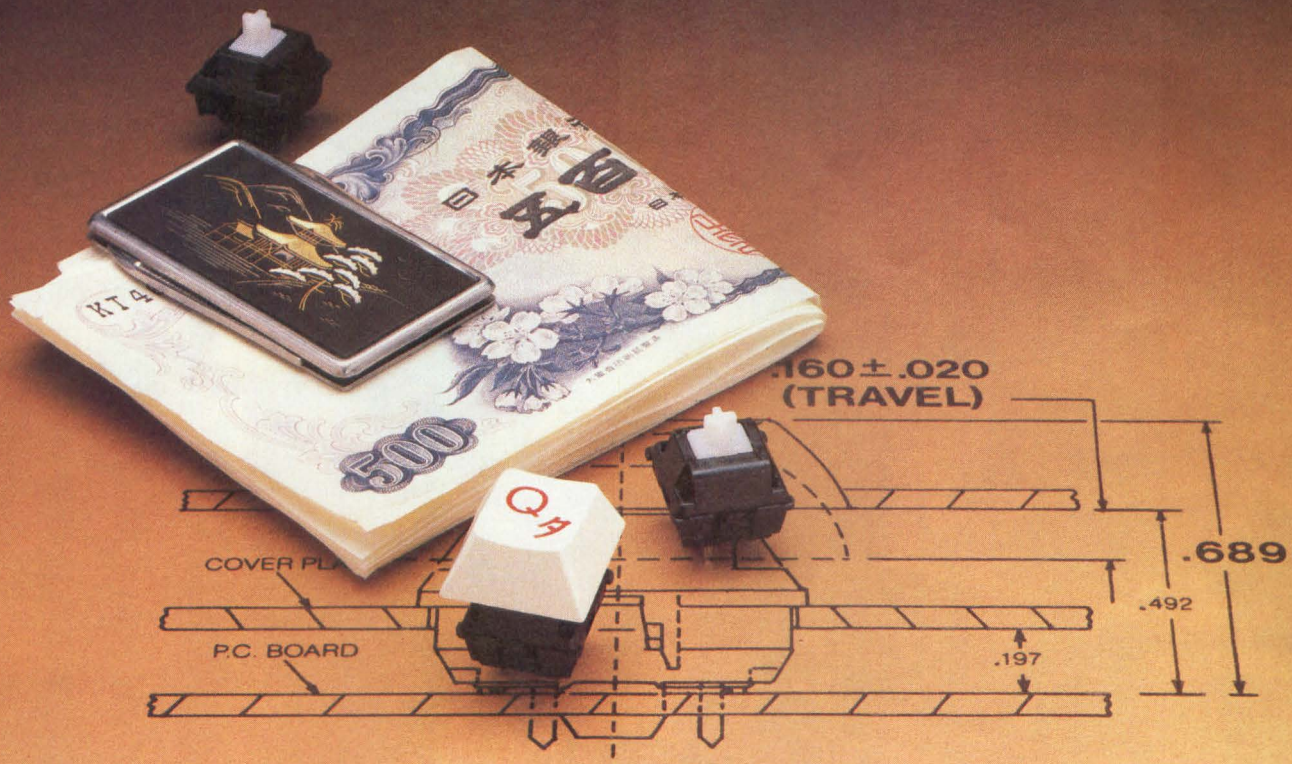
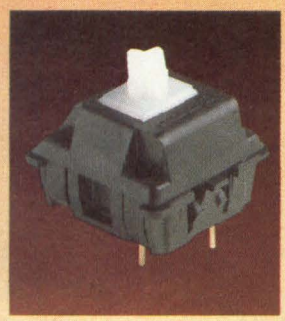


Cherry MX Keymodule: Full travel, low profile, DIN compatible. It's superior technology that brings our Far Eastern customers to Cherry. The same technology that's *available to you...off-the-shelf...at the lowest cost of any full-feature keyboard switch!*



Cherry MX technology begins with the proven gold crossbar contact concept. Continues with low profile, easy operation, clean IC logic signals and long life (20×10^6).

Linear or tactile feel, spherical or cylindrical keycaps. Options, too: LEDs, integral diode, jumpers, momentary or alternate action. As single keymodules or in standard or custom keyboards.

For application data and samples, you need only call as far east (or west) as Cherry...or contact your local stocking Cherry distributor.

CHERRY KEYMODULES

CHERRY ELECTRICAL PRODUCTS CORP. 3631 Sunset Avenue, Waukegan, IL 60087 • 1-312-578-3500

See Us At NCC/Chicago, July 15 - 18, CHERRY BOOTH 1150.

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"NO WAIT STATE"

– OF – THE – ART by FORCE COMPUTERS®

Force's "NO WAIT STATE"–OF–THE–ART CPU-4 features the 68010 at 12.5MHz with 128KBytes of SRAM for your high speed applications.

Proven speed superior in benchmarks, the CPU-4 is ideal for high performance VMEbus applications. In fact, the "NO WAIT STATE" CPU-4 holds its own against 68020 CPU products operating with several wait states!

Addition of the CPU-4 to Force's distinguished product family, designed and manufactured with years of VMEbus board engineering and production experience, assures you of a reliable, available, high performance CPU. CPU products available include:

CPU-1 Series The World's most popular and universal VMEbus CPU featuring 8/10MHz 68000, 128/512KBytes DRAM, 3 serial ports, RTC, and more. Over 6000 sold worldwide.

CPU-2 Series A highly versatile CPU incorporating the 8/10MHz 68010 with true "Dual Ported RAM" from 128KBytes up to 1MByte, multi protocol communications controller, floppy disk controller, PIT, and RTC.

CPU-3 Series The World's first UNIX* VMEbus board incorporating the 68010 CPU, 68451 MMU, and 68450 DMAC, 4 level bus arbiter, and serial I/O on one double Eurocard, 32 or 128K Bytes, zero wait state, SRAM CACHE mode operation

CPU-4 Series Additional features to those already mentioned include, a 68450 DMAC, 1 serial port, 2 parallel ports, RTC, and a floppy disk controller option.

NEW PRODUCT ADDITIONS

DRAM-E3M1+E3S3
The 1MByte DRAM master operates stand-alone or with multiple 3MByte slaves offering optimum performance in 32 bit data/32 bit address, Byte parity check environments. Typical access time is 65ns (write) and 240ns (read) with parity generation.

CMC-1
As an intelligent monochrome or color controller for raster scan terminals, this stand-alone VMEbus board offers interfaces for keyboard, lightpen, 2 serial ports and 1 Centronics parallel port.

ASCU-1/2
This new breed of high performance advanced system controller handles all exception signals on the VMEbus and contains powerful I/O devices such as a serial interface, Centronics parallel interface, 4 level bus arbiter, RTC, and GPIB interface (ASCU-2).

If the VMEbus boards you purchase aren't designed and manufactured by FORCE, chances are they aren't "NO WAIT STATE"–OF–THE–ART.

Call Force Computers today, the VMEbus specialist!

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FORCE COMPUTERS FRANCE
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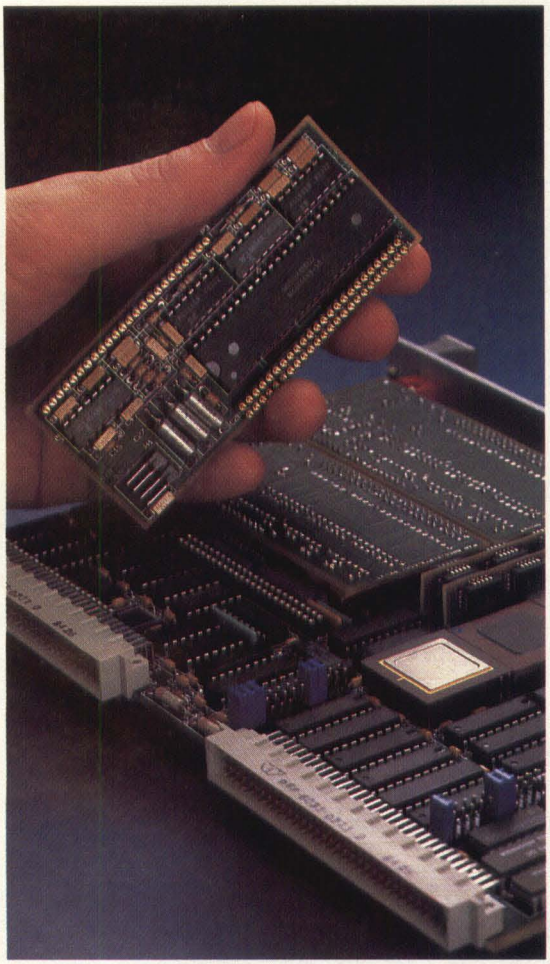
I/O WITH I.Q.



These plug-in modules make the Mostek Intelligent VMEbus board completely user-configurable.

The Mostek VMEbus Intelligent I/O board.

VMEbus has always been a smart choice for flexible system solutions. And now, Mostek has made VMEbus even smarter. By introducing the MK75804 VMEbus Intelligent I/O board.

Using the VMEbus IIO board in your system gives you a high-performance communications interface that places minimal demands on system resources. And since we designed the IIO board to accept up to three plug-in modules, it's completely user-configurable.

You can select up to six independent, full-duplex serial channels in pairs, or combinations of serial, parallel or other interfaces. Either RS232 or RS422 for serial I/O, or a Centronics-compatible printer port, or a general-purpose, 16-bit parallel I/O port.

The choice is yours. And because the IIO board incorporates a 68000 16-bit microprocessor and 128K to 512K of DRAM, it's not just smarter. It's fast also. In fact, it's capable of a transfer rate in excess of 1 Mb/s when used with our optional four-channel DMA controller. What's more, we built in a firmware monitor, an optional power-up ROM that provides download, debug and diagnostic functions.

When you add it all up, our Intelligent I/O board is easily the most flexible hardware solution available for VMEbus applications. Which is just one of the ways we show our continuing commitment to VMEbus technology.

For more information, contact Mostek Corp., 1215 W. Crosby Road, MS2205, Carrollton, Texas 75006, or call 1-800-635-0200. In Texas, 214/466-8801. In Europe, (32) 02/762.18.80. In Japan, (03) 496-4221. In the Far East (Hong Kong), 5.681.157-9.

UNITED TECHNOLOGIES MOSTEK

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EDITOR'S COMMENT

Selling Technology To The Russians

No matter how tricky the Japanese are in matters of international trade, there's no chance we'll ever go to war with them again. Where would we get parts for our Toyotas and Hondas? Where would we buy our TVs, stereo systems, VCRs, Walkmans and maybe even (God forbid) our Megabit DRAMs? Meanwhile, the Mercedes, BMWs and Porsches keep on coming from the Fatherland while the Germans rake in dollars to buy our computers and microprocessors.

Despite some inequities (big ones in the case of Japan), the international trade system has kept the world out of a major war. Our economies are so intertwined that no matter how much we disagree we don't go to war over it. There may be a lesson here that could apply to our relations with the Russians.

The major areas where we have some export trade advantage (besides food) are mostly high tech items such as jet engines, aircraft, computers and semiconductors. Yet we have a government that's afraid the Russians might gain some military advantage if they buy our electronics. It's a mistake. Missiles can be guided with relatively simple microprocessors, and those computers that the Soviets can build or purchase elsewhere are adequate for some pretty sophisticated military systems. It isn't lack of technical sophistication that holds down advances in Eastern bloc electronics; it is the lack of an entrepreneurial infrastructure. We could give them all of our latest commercially available chips and computers and by the next generation of products they would be behind again. If we sell high technology to the Russians, they must eventually become dependent upon us. Our economies could eventually become meshed to a degree that war would be unlikely.

Of course, we can't be stupid about it. We should sell them the end product, not the means to produce it. Furthermore we should insist on hard currency as a means of payment. Perhaps we should tie in other purchases with the high tech items. For example, we could make them buy a Chevy with every VAX and a PC with every 68020. Of course the Japanese could also play this game – probably even better than us. But it wouldn't hurt to have the Soviet Union overrun with VCRs and Toyotas. Consider the effect that could have on Soviet society. Could totalitarianism long exist, confronted with the anarchy of rock videos?

Our government should worry less about whether the Russians buy technology that can be openly purchased around the world. The real concern should be whether we are letting the Department of Defense hamper international trade in those very areas where we are best able to compete. Given recent revelations about spying within the Navy it would seem that the DOD's time could be better spent. Operational plans are of more value to an enemy than the latest microprocessor. The health of a high technology industry that may depend on exports for 30% to 50% of its revenue is more important than catering to the paranoia of the military establishment.

– John Bond, Editor in Chief

Zycad announces high-speed simulation for every design.

No matter what size design you're doing — LSI, VLSI, VHSIC, subsystem, or whole system — there is a Zycad logic and fault simulation engine to fit your specific design verification needs. Now Zycad offers four families of simulation engines — dedicated, special-purpose processors that accelerate the design verification process far beyond conventional simulation techniques.

Logic Evaluator®

Speed and capacity to handle virtually any design verification task.

The Logic Evaluator enables both logic and fault simulation of almost any chip, component or system at speeds up to 16 million events per second. That's faster than the most expensive supercomputers, but the Logic Evaluator costs about the same as a minicomputer. Its fully modular design makes the Logic Evaluator conveniently field upgradable to a capacity of over 1 million modeling elements.

The Logic Evaluator is the right choice for large design projects or for distributed processing among several design teams.

Fault Evaluator

High percentage fault grading of VLSI and system designs.

The Fault Evaluator is a concurrent fault simulation engine that helps design engineers develop chips and systems that are fully tested, and helps test engineers design more effective test operands. It also permits full exercising of the logic design, revealing redundant or untestable portions of a circuit or system at the design stage.

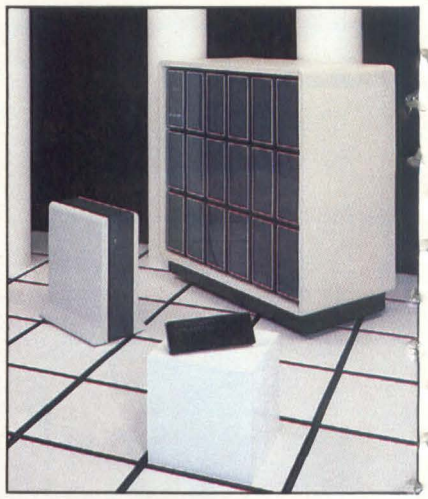
Using a proven hardware-implemented concurrent fault simulation algorithm, the Fault Evaluator lets you process fault grading runs never before possible. And develop production tests efficiently and cost-effectively. If the quality of your product is important, the Fault Evaluator is the right choice.

Expeditor 100/200™

Introducing a powerful turnkey simulation package at a low price.

The new Expeditor is a turnkey, affordably priced logic and fault simulation package that is compact enough to fit under your desk. With it, you'll be able to simulate chips, boards or entire systems up to 32,000 modeling elements at a speed of one million events per second. So logic and fault simulations that once took hours now take seconds.

Easily integrated by connecting to your small host, minicomputer or workstation network, the Expeditor turnkey package includes: ZILOS™, Zycad's user-friendly software interface, an Expeditor driver and an optional TTL library and hardware interface. The Expeditor is the right choice for an individual or multiple designers who need a turnkey simulation package with the speed and capacity to easily handle large designs.



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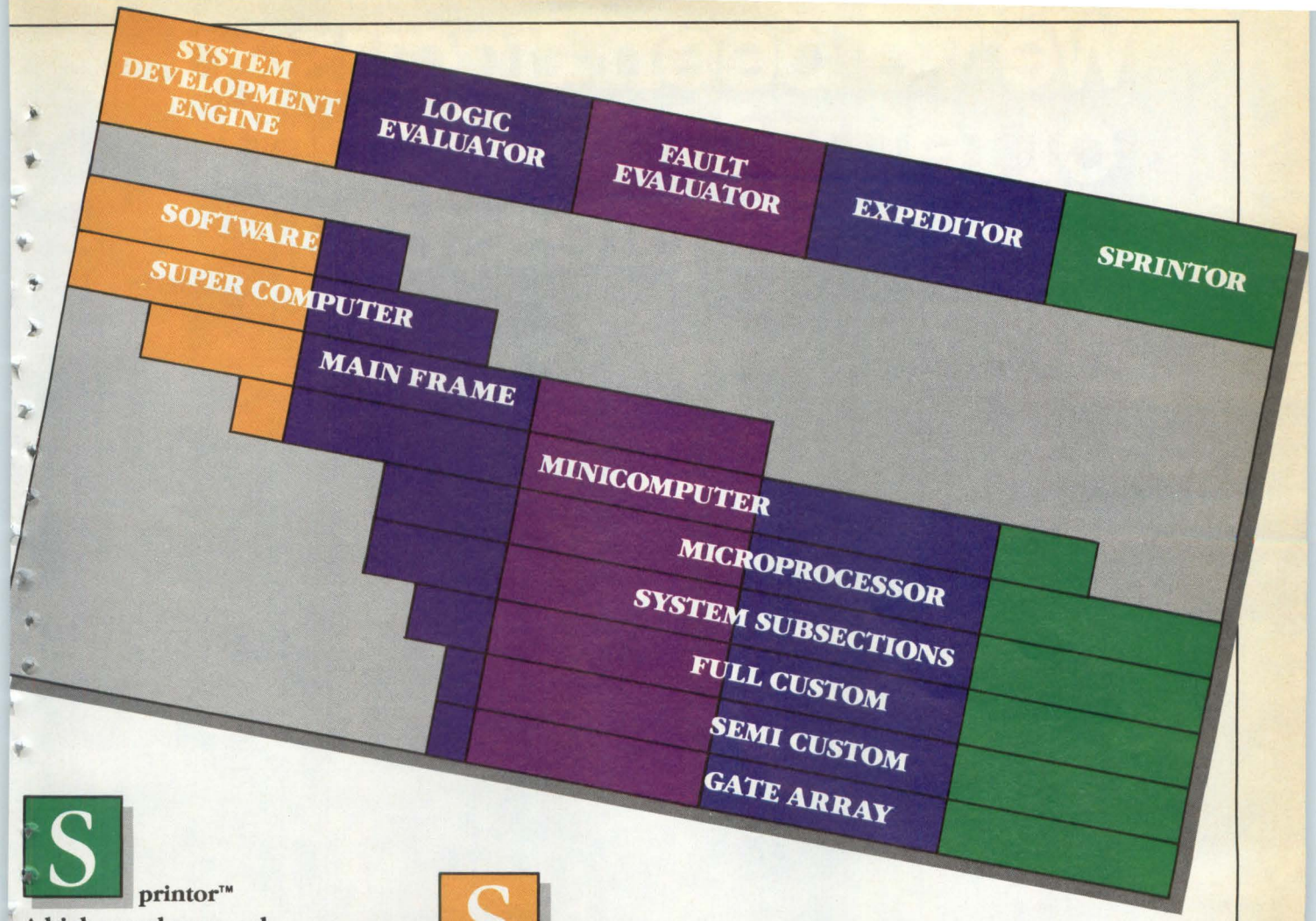

Sprintor™

A high-speed personal simulation engine with full interactivity.

The Sprintor fits into a single bus slot of a workstation, the IBM® PC/AT and MicroVAX[1]. Yet, despite its small size, the Sprintor is a powerful engine that delivers fast logic and fault simulation — up to 16,000 modeling elements at a speed of 200,000 events per second . . . perfect for chip, gate array or small system designs. And the Sprintor provides tightly coupled integration with workstation front-end software to allow full interactivity with behavioral-level language and hardware modeling systems.

For design engineers who need distributed processing capabilities plus outstanding simulation performance, all at an affordable price, the Sprintor is the right choice and will be available from workstation and PC vendors.

System Development Engine-SDE™

Breakthrough technology that makes concurrent hardware and software development practical.

Because it simulates up to 1.1 million modeling elements at over ONE BILLION events per second, the System Development Engine enables software development to begin as soon as the first functional block design is complete. A true "virtual hardware" system.

Years can be shaved off the system development cycle and the finished product can be superior to anything previously attainable. The System Development Engine is the right choice if you need to get a perfected electronic system to market years before the competition.

Now there is a Zycad logic and fault simulation engine available for virtually any design, host, designer team and budget. These engines represent the standard of the CAE industry, in terms of speed, price/performance, mean-time-between-failure (the Logic Evaluator is approaching two years), and the highest level of application engineer support. All of this has led to an installed base among the world's leading computer, telecommunications, semiconductor, defense and general electronic companies.

Call us today at (800) 631-5040 (In Minnesota call: 612-631-3175) and we'll send you complete information on any of our products. Or write us: Zycad Corporation, P.O. Box 12828, St. Paul, MN 55112.

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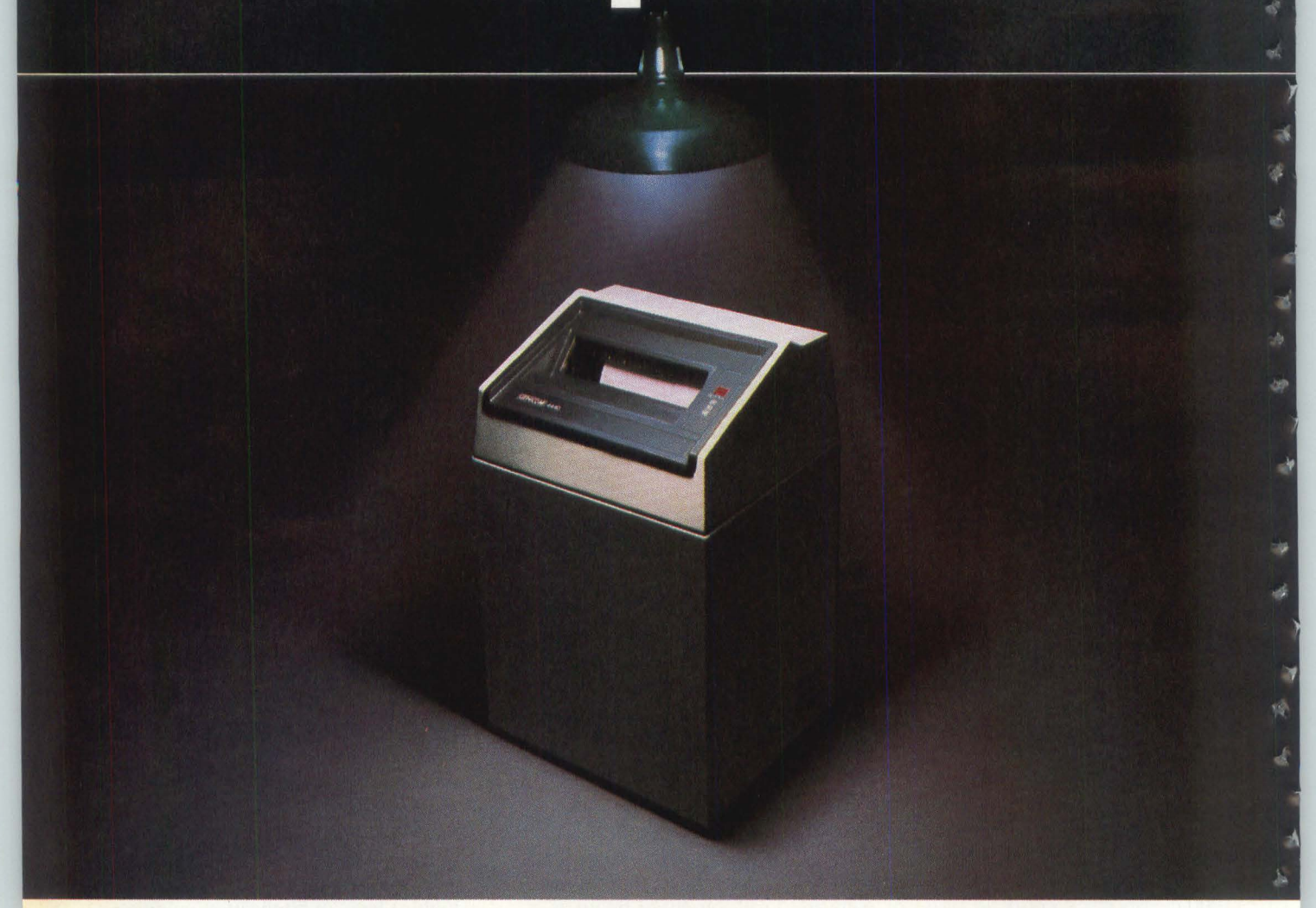
zycad™

We've been accused of refusing to break under pressure.



You Be The Judge.

In a reliability test, the Genicom 4000 line printer shuttle mechanism worked 24 hours a day non-stop for two and a half years without a failure... that's the equivalent of 20 years normal operation.

This remarkable reliability is the result of a totally new, patented resonance shuttle mechanism. It's so perfectly balanced, vibration is virtually eliminated. And the Genicom 4000 is free of those moving parts that commonly fail in other line printers. Indeed, the design is so innovative and simple, it has to be reliable.

The Genicom 4000 offers 300 or 600 lpm, data processing and letter quality printing, bar codes, 20 inch/sec paper slew, plus dual 6 pin tractors with paper reverse. But best of all, even under the pressure of extensive evaluations, it refused to break.

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HOTLINE

280 PSEC/GATE GATE ARRAY DEVELOPED Researchers from Mitsubishi reported on a 5000-gate gate array at the Custom IC Conference. Loaded delay time of 280 psec/gate is achieved with 3.28 mW power dissipation.

CRAY-2, SAID TO BE FASTEST SUPERCOMPUTER, INTRODUCED With two units shipped, Cray Research has formally introduced the Cray-2 with an OS based on UNIX System V. The liquid-cooled system is said to operate at 6-12 times the speed of the Cray-1 and requires 16 square feet of floor space.

DESIGN AND FOUNDRY SERVICES FOR ICs AVAILABLE FROM TEK IC foundry services for analog ASICs and CCDs are now available to the outside market from Tektronix Integrated Circuits Operation. CAD/CAE, E-beam lithography and bipolar ICs will also be offered on a contract basis.

JAPANESE CLAIM FASTEST AI MACHINE Researchers from NEC and the Institute for New Computer Technology report that they have built an AI computer that operates at 202 KLIPS (logical inferences per second) average.

DOCUMENT COMPANDING ON A CHIP AMD will introduce the 7970 compression/expansion processor for electronic document processing. Using CCITT-standard methods, the IC reduces bandwidth, time and storage requirements for bit-mapped 2-tone images by ratios as high as 50:1.

6 NSEC PROGRAMMABLE ARRAY LOGIC DEVICE INTRODUCED National Semiconductor has formally introduced the PL1016P8 PAL. The ECL device is said to be the fastest programmable device available, at a maximum input-to-output delay of 6 nsec, and is intended to replace multiple discrete ECL ICs.

ON-CHIP DIAGNOSTICS AGREED ON BY AMD, MMI A number of chips from MMI and AMD use a system of diagnostics on-chip that the firms have developed and are promoting as a standard.

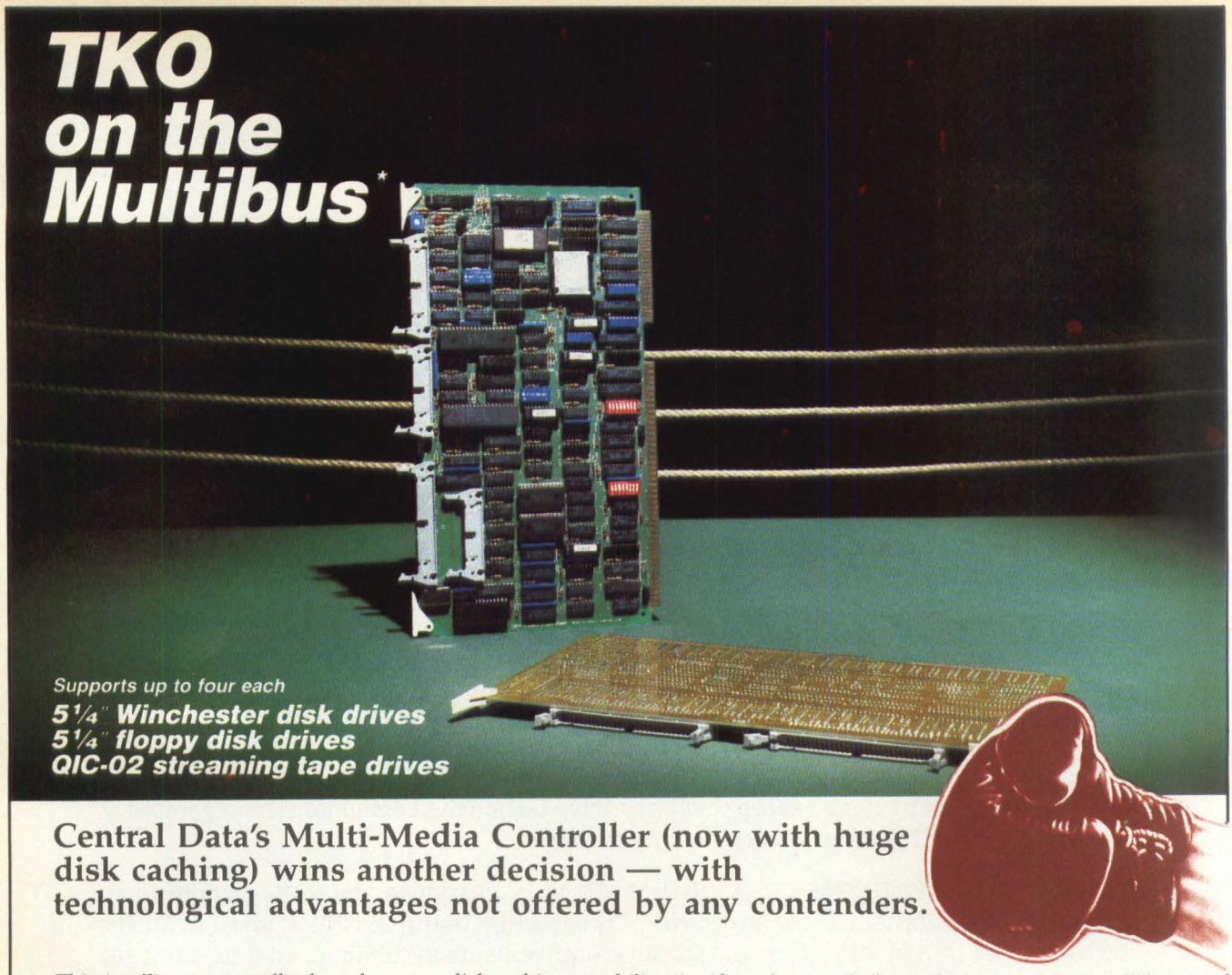
GERMAN DSP TO INCLUDE MULTIPLIER, MEMORY AND I/O PORTS The UDPI 01, a new digital signal processor from ITT Intermetall, includes a 200 nsec fixed point multiplier, on-chip data and program memory and both serial and parallel ports.

COLOR WORKSTATIONS BASED ON MICROVAX II In addition to the 32-bit MicroVAX II, DEC has announced the VAXstation 520 which features a Tektronix 4125 graphics subsystem with 1280 x 1024 pixel resolution.

DECNET TO MIGRATE TO ISO STANDARD PROTOCOLS Digital Equipment Corp. has announced that DECnet protocols will be replaced with ISO OSI international standard networking software; this will allow intervendor networks with other machines supporting ISO or MAP 802.4 hardware and software.

25 NSEC 2K x 8 PROM TO DEBUT Texas Instruments plans to introduce a 2K x 8 bipolar PROM. The TBP38S16 may be available as soon as the third quarter.

TKO on the Multibus*



Supports up to four each
5¼" Winchester disk drives
5¼" floppy disk drives
QIC-02 streaming tape drives

Central Data's Multi-Media Controller (now with huge disk caching) wins another decision — with technological advantages not offered by any contenders.

This intelligent controller board delivers all the flexibility and advanced design features you need to improve the performance of any Multibus system. It supports up to four each standard 5¼" Winchester disk drives, 5¼" floppy disk drives and QIC-02 streaming tape drives. And to allow for a huge disk cache, the board includes a versatile LBX interface.

More punch from Central Data. The board's powerful 80188 processor supports a high-speed disk cache of 128K to 8 megabytes, significantly more than any contender's. New from Central Data, this disk caching capability significantly improves throughput and performance levels for all disk drive subsystems.

Even the cache method is flexible, offering either track or sector mode by software selection. **Any** system can take advantage of this capability, including the UniPlus+* operating system offered by Central Data.

Make the winning decision. Stop sparring around with inflexible controllers — find out more about how Central Data's Multi-Media Controller can help you get the most from your Multibus system.

Call our design engineers toll-free for expert assistance with product selection and application information on this board or on our full line of quality Multibus boards.

Central Data offers a complete line of Tape and Disk Controllers. Call us for full details.

BOARD	PROCESSOR	FLOPPY	QIC-02	ST-506	RAM	EPROM	FORMER PART#
CD21/4300	80188	4–5-1/4"	4	4	6/12K	64K	B1030
CD21/4130	8085A	4–5-1/4" and 8"	—	—	12K	8K	96/6130
CD21/4120	8085A	4–5-1/4" or 8"	—	—	2K	8K	96/6120A
CD21/4055	none	4–5-1/4"	—	—	—	—	B1055
CD21/4015	none	4–8"	—	—	—	—	B1015
CD21/4029	none	—	4	—	—	—	B1026

*Multibus is a trademark of Intel Corporation.
UniPlus+ is a trademark of UniSoft Corporation.

Central Data

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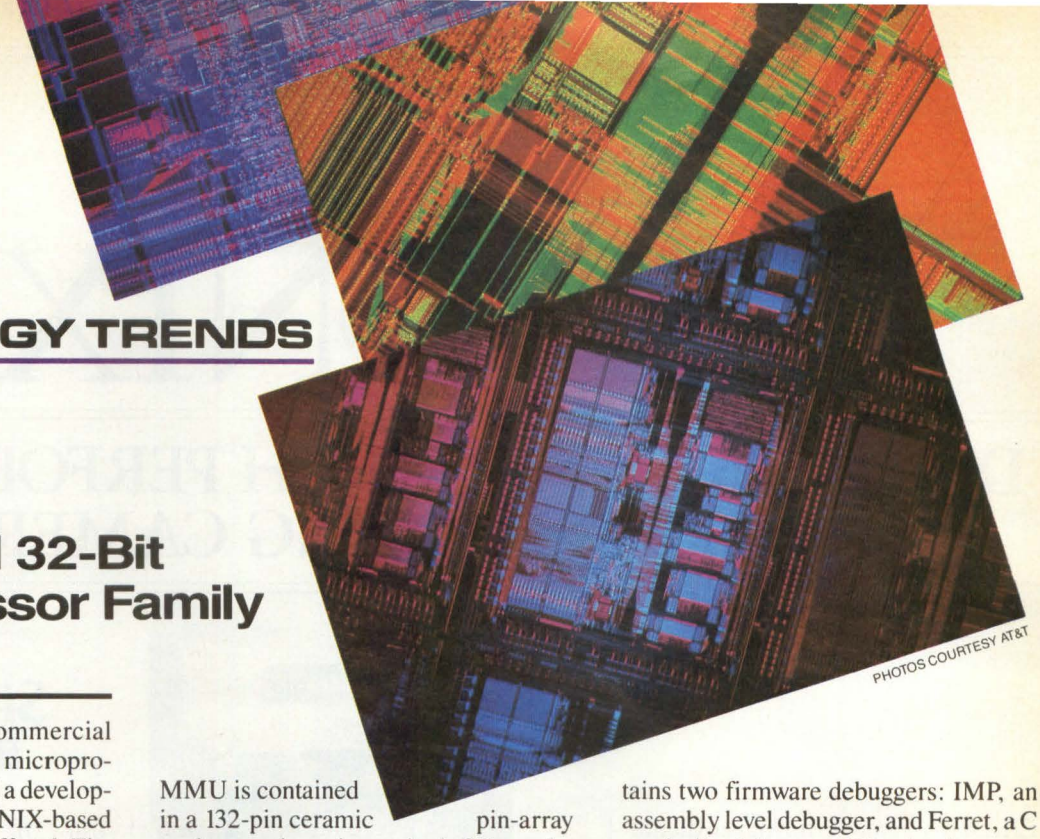
ICs

AT&T To Sell 32-Bit Microprocessor Family



PHOTOS COURTESY AT&T

AT&T has announced commercial availability of its 32-bit microprocessor chip set. Six chips and a development package consisting of UNIX-based software tools are now being offered. The announcement comes at a time when most of its competitors have already started shipping 32-bit processors. Despite the late introduction, much of the AT&T chip set is already in production.

The core of the chip set is the WE32100 microprocessor, a CMOS part housed in a 132-pin ceramic pin array. Execution speed is enhanced by an internal instruction queue and an internal instruction cache. The queue is an 8-byte FIFO that stores prefetched instructions. It is used for pipelining, enabling the microprocessor to overlap the execution of instructions while tracking each separately. The instruction cache is a 64-word on-chip cache used to increase the microprocessor's performance by reducing external memory reads for instruction fetches. When an instruction fetch from memory occurs, instruction data is placed both in the queue and in the cache. If that data is needed again it is fetched from the cache rather than from external memory, increasing the performance of the system.

The WE32100 microprocessor may be used in conjunction with the WE32101 MMU when virtual message storage is needed for a system. The MMU performs address translation by mapping virtual memory addresses to physical memory addresses. It supports both demand-paged and demand-segmented virtual memory systems and also allows the use of shared segments for intertask communication. Like the CPU, the MMU is contained in a 132-pin ceramic pin-array package and requires a single 5V supply.

For applications that require number crunching capability, AT&T also offers the WE32106 Math Acceleration Unit (MAU). Fully compatible with the proposed IEEE standard for binary floating point arithmetic, it provides single (32-bit), double (64-bit) and double-extended precision (80-bit), in addition to add, subtract, multiply, divide, remainder, square root and compare operations. Operand, result, status and command information transfers take place over a 32-bit bidirectional data bus that provides the interface to the host microprocessor. Again a CMOS part, the MAU is housed in a 100-pin package and requires a 5V supply.

To simplify system interface functions, AT&T provides the WE32105 System Interface Unit, protocol compatible with the 32100 CPU and the 32101 MMU. It provides commonly used logic and control functions such as DMA and selectable wait-state generation for a range of system applications. Implemented in CMOS, it is housed in a 100-pin ceramic pin-array package. Other support chips, such as the WE32104 DMA controller and the WE32103 dynamic RAM controller will be available late in the year.

To aid system design, AT&T also offers a development system. The main component of the system, dubbed the WE321DS, is the 321AP Microprocessor Analysis Pod. The analysis pod can emulate the CPU, MMU and clock functions in the target system under development. It contains two firmware debuggers: IMP, an assembly level debugger, and Ferret, a C symbolic debugger. The development system also includes UNIX System V-based software programs. An additional software option is available that supports logic analysis with the Hewlett-Packard 64000 logic development system.

Apart from AT&T, Motorola (Austin, TX) and National Semiconductor (Santa Clara, CA) appear to be the nearest to offering complete chip sets. Both Motorola's 68020 and the 68881 floating point unit are available now with the 68851 MMU sampling in the July/August time frame. Motorola's 68030 second generation processor may be available as soon as mid-1986. National Semiconductor's CPU, MMU and FPU are all available now in 10 MHz versions along with several support devices, such as a timing control unit, an interrupt controller and a DMA controller. A CMOS version of the 32016, the 32CT016, is expected to be available in both 6 MHz and 10 MHz versions in the third quarter. Intel (Santa Clara, CA) is expected to make a formal announcement of the long awaited iAPX386 by October.

The major market for these advanced 32-bit processors is in high-end workstations. Here, however, system builders have a lot of catching up to do, especially considering that their competitors, primarily the minicomputer houses, have the capability to introduce low-cost ($20,000) systems based on their own captive semiconductor products.

—D. Wilson

ONLY EIKONIX®

DOES SO MUCH IN HIGH PERFORMANCE DIGITAL IMAGING CAMERAS.

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EIKONIX® high-performance digital imaging cameras offer unique capabilities that clearly distinguish them from all others.

CCD or Photodiode Technology

Only EIKONIX offers a choice of high-resolution cameras employing either linear CCD (charge-coupled device) or photodiode technology. In fact, EIKONIX offers the highest-resolution CCD camera available anywhere, with up to 20 million pixels per image (4096 x 5200). You can choose the economy and low-light capabilities of a CCD camera, or the greater dynamic range of a photodiode camera, *without sacrificing high resolution.*

Color or Monochrome

Only EIKONIX has a family of high-resolution cameras available for either monochrome (256 gray-scale levels) or color (a palette of 16 million colors) applications.

More User Control

Only EIKONIX cameras use a precision stepping-motor/lead-screw/ball-slide stage mechanism, which provides precise positioning of the array and eliminates one-dimensional smearing. In addition, this mechanism allows asynchronous operation, so the user can control both scan speed and data collection rate. This eliminates the need for a separate "frame grabber" or dedicated processor, and frees the host computer for multi-tasking.

Buy Just What You Need

Only EIKONIX' broad product line lets OEMs and end users match needs precisely. Configurations range from bare-bones digital camera heads through complete image acquisition subsystems, including cameras, light sources, control electronics, imaging software, and interfaces for many widely used computers (including most DEC and Multibus-based systems).

More Applications

Only EIKONIX offers the performance and flexibility to handle the broadest range of the most demanding applications, including mapping, engineering drawing digitizing, graphic arts, CAD/CAM input, office automation, X-ray storage and analysis, textile pattern design, geological imaging, communications, animation and microscopy.

EIKONIX Know-How

Only EIKONIX digital imaging products are backed by our 17 years of experience in matching advanced electro-optical technology to a widening world of applications.

To find out what we can do to support your digital imaging applications, contact EIKONIX, 23 Crosby Drive, Bedford, MA 01730, (617) 275-5070.

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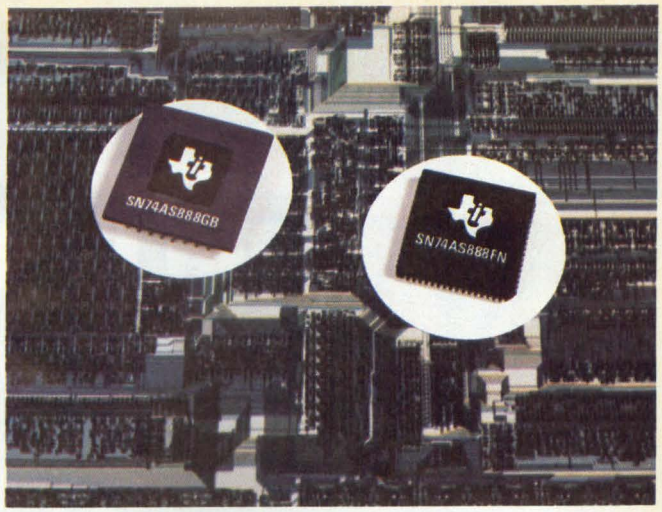


TI's SN74AS888 series of bipolar ICs uses 8-bit slices; a combination of fabrication technologies provides fast switching times and low power consumption, typically 1.1W.

Bit-Slice Chips Challenge 32-Bit Microprocessors

Despite the growing attention focused on 32-bit microprocessors, bit-slice chips offer alternative approaches. Many designers now favor segmented architectures, in contrast to the traditional universal chip approach. Functions such as graphics, memory control and I/O can be optimized if they are controlled individually. Furthermore, the architecture may be optimized for the specific application.

The performance and throughput of bit-slice devices may justify their use, in spite of higher power consumption, more packages per function and higher cost compared to microprocessors. Many of the systems that demand 32-bit performance take advantage of newer computer architectures that support pipelining and parallel processing. Additionally, newer fabrication technologies are being used for developing higher speed and lower power bit-slice devices.

Advanced Micro Devices (Sunnyvale, CA) set an industry standard with the Am2900 4-bit-slice series. The new AMD 29300 family is microcode compatible with the older 2900 series. But the 29300s are 32-bit wide chips, partitioned horizontally rather than vertically. This means that the register file is separated from the other data path elements. The chip set includes a 32-bit ALU, a 16-bit sequencer, a 64 × 18 bit register file, a 32 × 32 bit parallel multiplier and a 32-bit floating point processor. All of the chips run at a cycle time of 80 to 100 nsec. Power dissipation is high, at over 7W. Samples of the complete set are expected to be available in November.

Several companies are now offering bit-slice chips that use 8- and 16-bit vertical slices. Texas Instruments (Dallas, TX) has introduced its 8-bit-slice bipolar family, the 74AS888. For all but the year-old register file, TI's STL (Schottky transistor logic) technology is used for the family's internal logic, with interface circuitry implemented in low-power TTL. The process results in cycle times between 75 and 93 nsec. The STL gates require only a 2V power supply; the TTL section converts the signals to standard 5V levels. The combination of technologies allows the device to switch at high speeds, yet dissipate only 1.1W (typical). Enhancements incorporated in the family include floating point normalization, BCD arithmetic and CRC for data integrity. Four parts are now offered; new devices will be announced in the future.

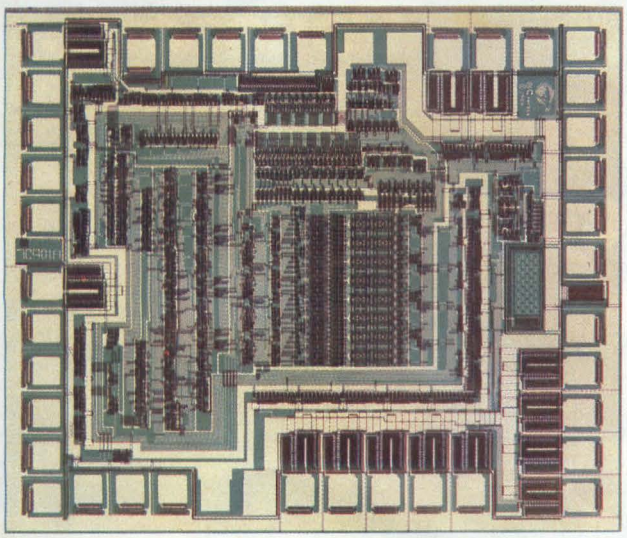
A new company riding on the popularity of the 2901 family is WaferScale Integration (San Jose, CA). The WS59016-C is comparable to an enhanced 16-bit version of the 2901. The chip is the equivalent of four 2901s and includes a carry-look-ahead similar to the 2902. WaferScale uses its standard-cell design system to enable a user to choose a cell from the cell library for specific architecture requirements. Fabricated in CMOS, the device consumes less than 1/27 the power of the 2901. Other cells in the library include common functions from the 2901 family such as a microprogram sequencer, a priority-interrupt expander and a status and shift control device.

Analog Devices (Norwood, MA) is offering bit-slice parts aimed at specific markets such as signal processing and analog-to-digital processing. The 16-bit chips are CMOS-based and have a 100 nsec cycle time. Samples are available now for its 32-bit floating point processor.

Cypress Semiconductor (Santa Clara, CA) offers 4-bit-slice CMOS parts that replace the 2901 family. The four units are expected to be faster than the bipolar version from AMD. Only one part is being sampled now. In addition to the 31 nsec cycle time, power consumption is less than one-fourth that of the AMD part.

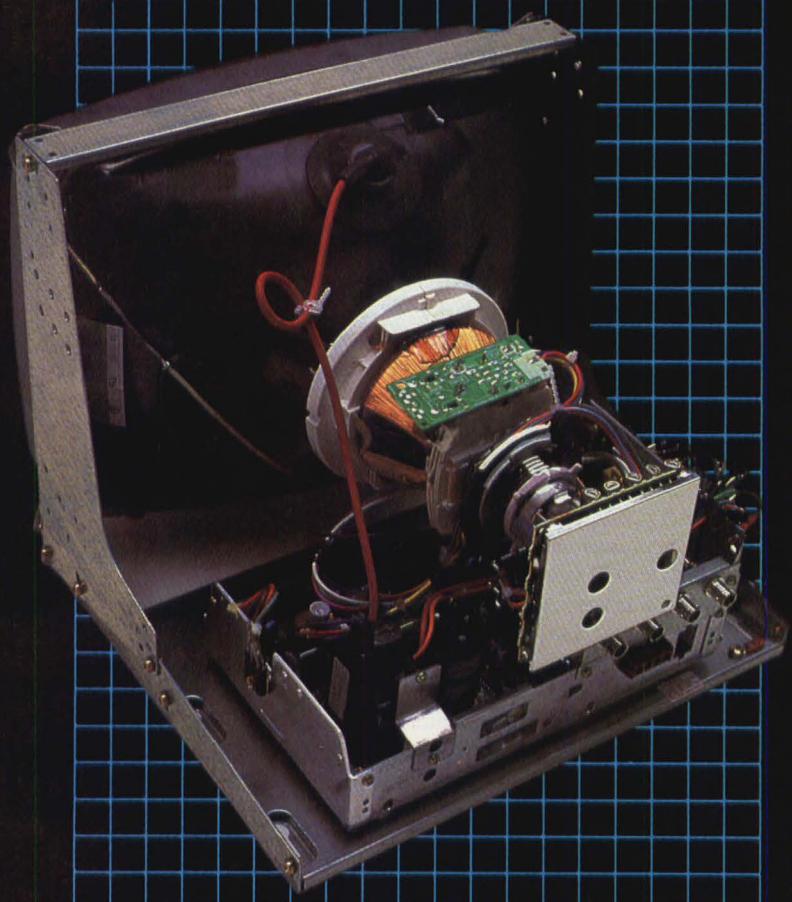
Factors in the choice between bit-slice and monolithic include cost, power consumption and speed and efficiency of microcoding. While the cost of one bit-slice part may be more than another, the real cost may be in support circuitry such as PROM or RAM. All factors must be weighed against the specific requirements and demands of the application.

—MacNicol



The 7C901 bit-slice processor from Cypress Semiconductor is faster than AMD's industry-standard 2901, with a 31 nsec cycle time.

Panasonic Data Displays



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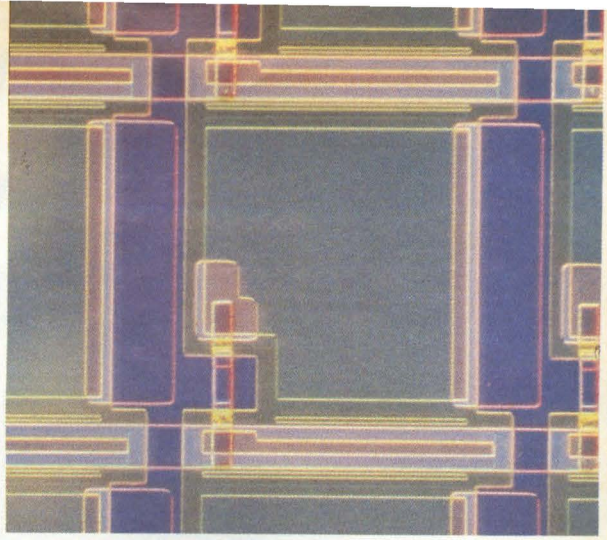

Figure 1: Microphotograph of the thin-film transistor substrate construction used in Panelvision's 640 × 400 pixel LCD.

Three Flat Panel Display Technologies Mature For Use In Portable PCs

"Full screen" flat panel displays, based not on one technology but on three very different concepts, were revealed at this year's Society for Information Display symposium in Orlando, FL. Liquid crystal, electroluminescent, and plasma gas discharge display technologies have all matured to the point where panels of 640 × 400 pixels appear technically feasible.

The significance of the full screen is that it offers display compatibility with existing personal computer equipment while the flat panel nature of the new designs brings true portability for the first time. Until now, portable terminals incorporating low-power liquid crystal displays (LCDs) have sacrificed screen size and computational ability to be able to operate from a battery.

The highest resolution on a flat panel currently used in a commercial product is 640 × 256 display elements on the LCD of the Data General/One portable computer. The LCD elements are addressed in a traditional multiplexed electrode design. This gives DG's unit, like LCD-screen portable computers from Apple, HP, Commodore, Kaypro and others, a poor screen image with low contrast and limited viewing angle.

A larger, 640 × 400 LCD panel demonstrated by Panelvision (Pittsburgh, PA), aims to overcome this problem by using active substrate addressing of the display. In this scheme, a thin-film transistor (**Figure 1**) is deposited at the site of each pixel, bringing the electronic switching needed for the display to function onto the panel itself. Most research efforts are concentrating on silicon—especially amorphous silicon—as the substrate semiconductor, but Panelvision has chosen to pursue cadmium selenide.

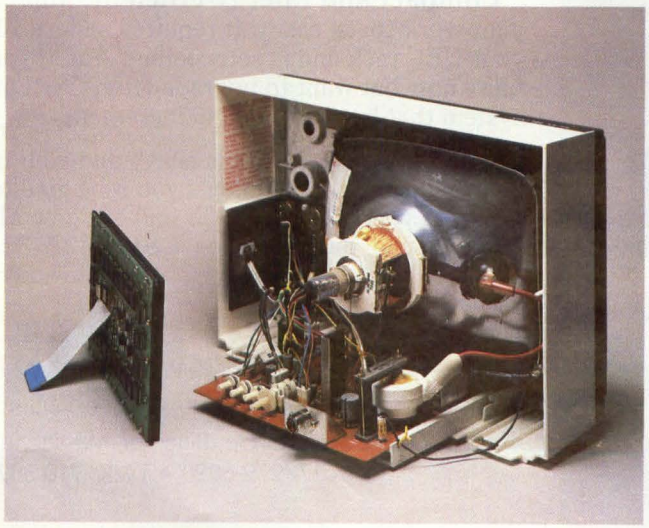

Figure 2: Planar Systems' electroluminescent display demonstrates space-saving advantages over the CRT.

Panelvision's vice president of marketing, Thomas C. Maloney, claims the new panel has a contrast ratio of 20:1 used in a back-lit, transmissive mode of display and 8:1 for reflective viewing. Large multiplexed panels like Data General's, which operate with reflected light, have contrast ratios less than 3:1, he claims.

In electroluminescence, the largest panel announced so far also made its debut at SID in the 640 × 400 resolution category. Planar Systems' (Beaverton, OR) full page panel, designated EL66610, uses AC thin-film technology (*Digital Design*, January 1985, p. 20). The display area is larger than on Planar's previous panel of 512 × 256 pixels (**Figure 2**) as a result of an improved electrical addressing configuration. The new electrode architecture has 200 row drivers and 2 sets of 640 column drivers, effectively halving the power consumption over the conventional layout.

Planar's architecture also increases the time available to charge each column electrode. The drive scheme requires a 50V modulation supply, a -160V write supply and a 190V refresh supply. Maximum modulation power consumption is claimed to be 11.5W. Custom drive circuitry is fabricated in 3μm CMOS. These circuits are surface-mounted to a two-layer PC board. Overall panel thickness is about 20 mm.

Both Panelvision and Planar expect their panels to reach the market early next year. However, plasma panels of 640 × 400 resolution are already on the market from NEC, distributed in US by World Products (Sonoma, CA) and Panasonic (Secaucus, NJ). Panasonic uses DC drive, for a panel with 155 cd/m^2 brightness and a 100:1 contrast ratio from supply voltages of 200V and 5V. NEC, which also makes a 720 × 350 pixel device, uses AC technology.

—Aldersey-Williams

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Schemes To Interconnect Networks Aid Wide-Area Data Transfer

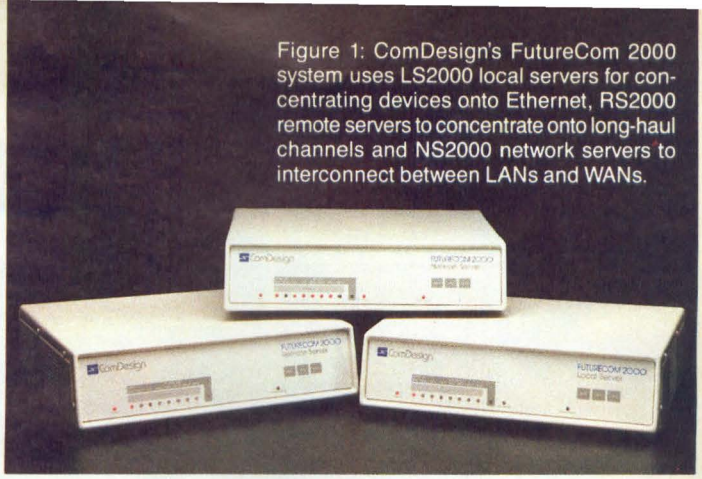

Figure 1: ComDesign's FutureCom 2000 system uses LS2000 local servers for concentrating devices onto Ethernet, RS2000 remote servers to concentrate onto long-haul channels and NS2000 network servers to interconnect between LANs and WANs.

Communication networks have sprung up in many forms to serve department needs, creating incompatibility on a larger scale. Resources on various local area networks (LANs), wide area networks (WANs) and mainframe computer networks cannot easily be shared. Network vendors may provide gateways into widely used mainframes and noncompeting networks. The need is so great that several companies with no network of their own have introduced network interconnect products.

Banyan (Westboro, MA) was out early with a virtual networking switch (see *Digital Design*, November 1984, p. 34). Since then, California Network Systems (Milpitas, CA) has announced an OEM internetworking connectivity scheme. At this year's Interface show, ComDesign (Goleta, CA) discussed the FutureCom 2000 Integrated Area Network, and Doelz Networks (Irvine, CA) presented a virtual circuit packet switch. All of these products are designed to interconnect devices on incompatible networks.

California Network Systems' initial product line provides OEMs links from other LANs into SNA. Three products provide varying performance. The first level is a software-only SNA gateway to run on a PC card, either OEM/SNA for LAN vendor configuration or SNA/3270 for IBM PC Networks. At the next level, the company offers a ComCard on the PC bus. With an 80188 on-board, it executes the gateway function considerably faster than the PC's own 8088. The NetServer box has 14 IBM PC bus slots, one for the system master, the others for ComCards or other network interface cards.

Three levels of products are also included in the FutureCom 2000 from ComDesign. They provide a local server for Ethernet that concentrates up to 32 devices onto the LAN cable, a remote server for RS-232 WANs and a Network Server that provides a gateway between Ethernets or between Ethernet and RS-232 systems (**Figure 1**).

The Banyan approach uses a central virtual circuit switch in which a front end connects to various LANs, and a back end interfaces to other Banyan servers, the public data network or a host. The 68000-based system supports Ethernet, Omninet, Pronet, RS422 and Applebus LANs and 3270 emulation. Services include file, print, backup and a naming and addressing system.

Esprit One from Doelz is also a virtual circuit switch, but it uses packets that serve as envelopes for any format of data. Data bits from each connected device are enclosed in packets standard to all Doelz concentrators and switches, with no format or protocol conversion. In combination with 68000-based hardware and a real-time OS, this provides rapid transmission and low overhead.

All of these systems except the California Network scheme, which operates around SNA, use proprietary protocols, operating systems or both. This makes writing code for a specific protocol or network configuration difficult. Other shortcomings are in scope. For example, Ethernet is the only network supported by ComDesign, and SNA the only option for California Networks. In the case of Doelz, no protocol translation is used, so the network only provides a shared medium for transmission between devices that use compatible formats.

Another method of interconnecting between networks is to use satellite channels from Vitalink (Mountain View, CA). TransLAN, marketed jointly with DEC, operates at the link level, below the higher layer protocols. This provides high throughput, but means that only like networks can be interconnected: Vitalink connects only Ethernet to Ethernet.

Network operating systems like those from Novell (Orem, UT) and Waterloo Microsystems (Waterloo, Ontario, Canada) also allow communications between separate hardware networks. This generally provides good connectivity functions. The drawbacks are that they are only for PCs, users must learn a new system and OS software must be added.

Gateways from LAN vendors are common. Although designed to heighten the market for the company's product, they are well designed to operate from that particular LAN. If connections are mainly within the LAN with only occasional need for links into other systems, they may work well.

Digital PBX systems may also interconnect various computers and networks. For example, Micom (Chatsworth, CA) has SNA and X.25 modules for the Instanet Micro600 PABX, as well as various multiplexers. The acquisition of Interlan (Boxborough, MA) suggests that a LAN interface may be forthcoming as well.

Few of the products currently available address both higher level software issues and a wide range of products. Communication software, especially between unlike machines and OSs, is complex. Now that the problem of interconnecting the various networks within one organization has been identified, the more difficult task of evaluating options must be undertaken. Universal internetworking is yet to come, but the field is opening up and the limited interfacing available may be adequate for some applications.

—Pingry

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DESIGN TOOLS

GATE ARRAY DESIGN UPDATE: Simulation And Routing Considerations

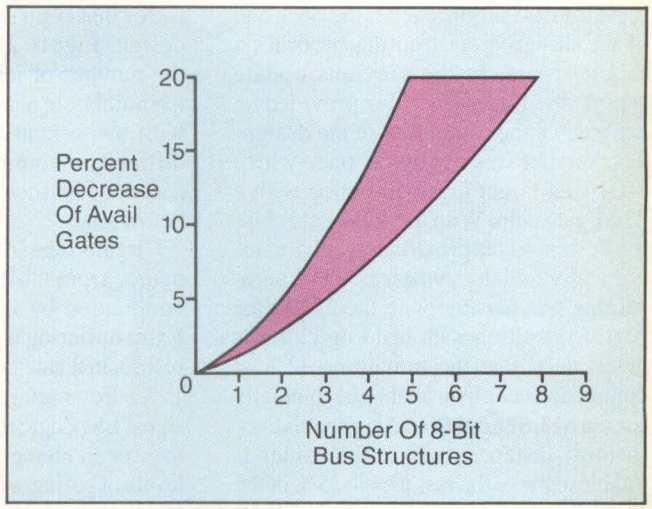

Figure 2: When routing a gate array, the number of interconnections determines whether the design can be routed on a given part. Bus structures, which consume substantial area on the chip, are often the cause of routing difficulties. The graph illustrates that as the number of buses increases, the percentage of available gates decreases.

Digital Design published a three-part series on designing a digital crosspoint switch using a CMOS gate array in January, February and March of this year. An update report was then published in May. This update report focuses on simulation procedures using Valid Logic's (San Jose, CA) Scaldsystem workstation and LSI Logic's (Milpitas, CA) Design Verifier software. Considerations surrounding the proper array choice are also explored.

As described in the May update, the Design Verifier provides the designer with statistically derived interconnect wiring delays for simulation. If the Design Verifier is not used, these delays are based on a fixed fan-out. When running the Design Verifier together with the Scaldsystem, simulation and timing analysis are performed simultaneously. When the Scaldsystem is used alone, however, the two are done independently.

Preparing and executing a simulation with the Design Verifier running on the workstation is a straightforward task. Valid's CAE software executes both batch and interactive simulations. At least one batch mode simulation is run on the workstation with the same input test vectors that are used for execution of the simulation on LSI Logic's mainframe-based LDS system. Simulation on the larger computer, done after routing, uses actual wire delays.

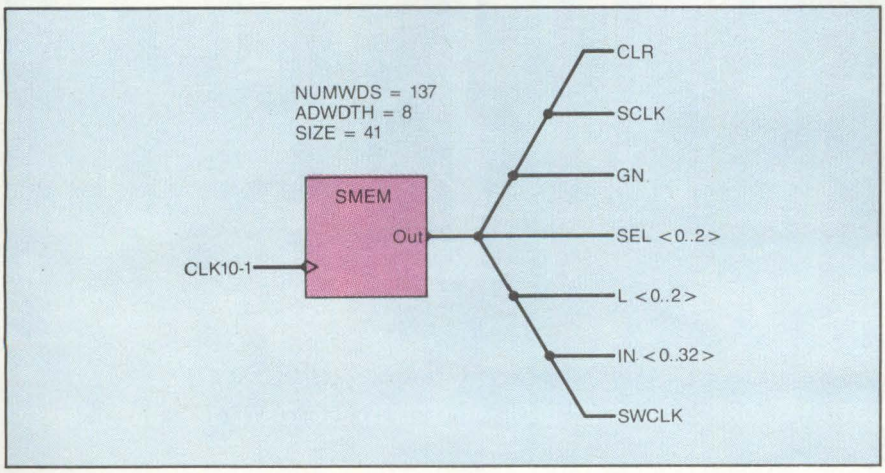

Figure 1: Running a simulation on Valid Logic's Scaldsystem and LSI Logic's Design Verifier requires the creation of an SMEM module. The SMEM module functions as a storage element for the simulation vectors. Shown is the SMEM module configured for simulation of *Digital Design*'s digital crosspoint switch. The signals found at the output of the SMEM module are the inputs to the digital crosspoint switch.

To execute a simulation, various files, including a test vector file, must be prepared. The designer must also construct an SMEM module, which functions as a RAM cell for the test vectors. The SMEM module for the digital crosspoint switch is shown in **Figure 1**. When adding the SMEM module to the design, values are first assigned to CLOCK ASSERTION (CLK), SIZE, NUMWDS and ADWDTH.

CLK defines the timing sequence for the test vectors. SIZE is calculated by adding up the number of input pins, bidirectional pins and enable signals. NUMWDS determines the total number of simulation patterns to be loaded into the RAM. ADWDTH is related to NUMWDS and defines the address width for the RAM. ADWDTH is the exponent of 2 that is equal to or greater than NUMWDS; since NUMWDS for the crosspoint switch is 137, ADWDTH is equal to 8. (If 2 were raised to the 7th power, the result would be 128, which would be unacceptable because it is less than 137.)

Configuring the SMEM module with all of the circuit input signals, bidirectional signals and enable lines is the next step. As illustrated, the CLK provides synchronization for directing test vectors from the SMEM module into the circuit. The final step is to compile a simulation file and execute the simulation.

As the design approaches the back end of the design cycle, routing becomes a crucial issue. In the previous update report, the Design Verifier provided an estimate of the routability of the design. The Verifier was run twice: once with a 1404-gate target array and once with a 2224-gate chip. With the 1404-gate chip, the design was approximately 88% automatically routable, whereas 100% autorouting was feasible with the 2224-gate part. Consulting with LSI Logic, it was determined that the remaining 12% of connections could probably be manually routed by LSI Logic's routing specialists. In most instances where the router is unable to make the last 10% to 15% of the connections automatically, LSI will attempt to manually route the signals and thus keep the design in the smallest possible array.

In general, routing is a function of the number of gates, number of nodes, chip size, average fan-out and logic organization. Number of bus structures is another factor that contributes to routability of a design. **Figure 2** shows that increasing the number of interconnects decreases the number of available gates. In designs with bus-oriented architectures, added difficulty in routing should be taken into account when determining the total number of gates.

Circuits demanding maximum performance from CMOS technology are accompanied by increased gate counts. Extra buffering is required that typically results in a gate count increase of 5% to 15%. For maximum performance designs, LSI Logic recommends using "AO" macrocell elements which perform low levels of gating with a single inversion in low fan-out circuits, keeping fan-out to a maximum of four or adding a buffer, minimizing the number of NOR gates, minimizing the number of gate inputs since two-input gates are much faster than four-input gates and using flip-flop Q outputs since they are valid before the complementary Q output.

This is the last report on *Digital Design's* gate array design project. Although we intended to fabricate the chip, Datacube's (Peabody, MA) system specification changed, changing the chip's functional requirements. The time needed for circuit alterations and additional design verification to meet the new specification cannot be justified in light of the project's purpose. Similarly, in its present configuration, there is little justification for incurring tooling and fabrication expenses.

We regret that the array will not be fabricated; however, the project overall has been a huge success. Going through the exercise of designing a gate array on a workstation has given *Digital Design* far greater insight into both CAD/CAE and semicustom technology. This added knowledge enables *Digital Design* to provide further in-depth analysis of the design issues surrounding this rapidly growing segment of design technology.

—*Collett*

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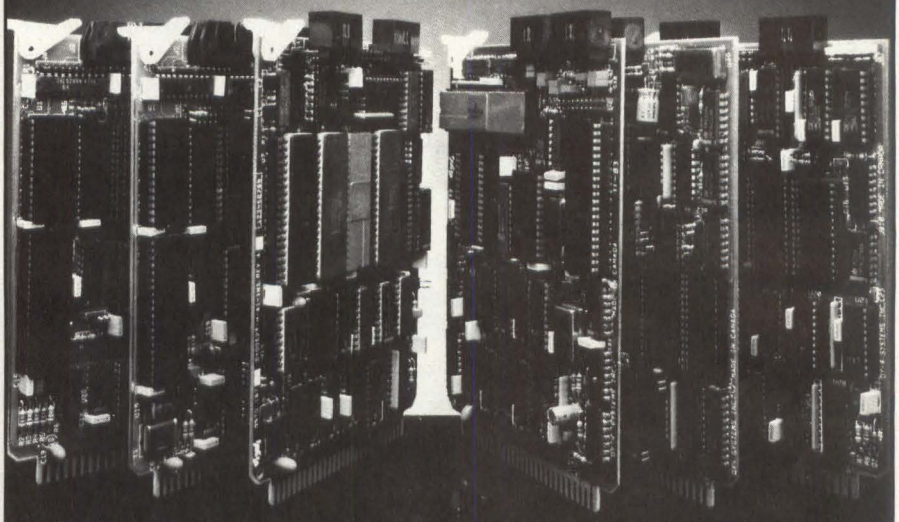

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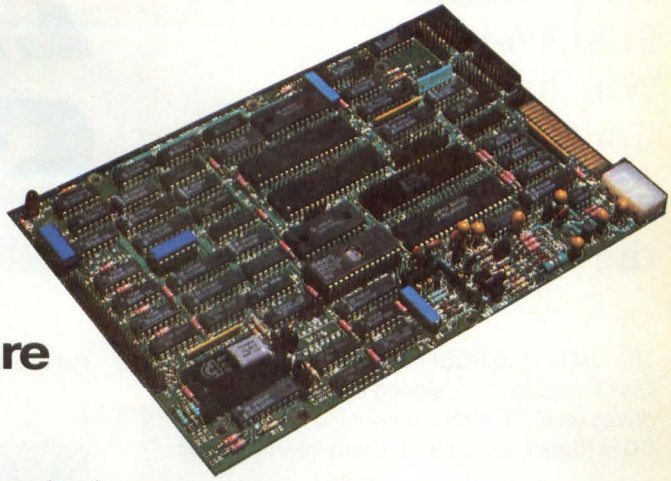
Disk/Tape Controllers Declare Independence With SCSI



By using SCSI features like device independence and auto configure, device drivers do not need to be rewritten when changing or upgrading disks. The ACB-5500 from Adaptec controls up to four ST506/ST412 Winchester disks and includes 32-bit ECC and parity checking to improve reliability of data to the system.

Increased system throughput and device independence make the Small Computer System Interface (SCSI) a desirable choice for disk and tape controllers. Moving peripherals from the system backplane to a separate I/O bus like SCSI removes a large source of bus traffic in transfers between disk and tape and the host CPU. Furthermore, it isolates host processors and operating systems from modifications in disk and tape drive configurations.

The proposed ANSI X3T9.2 standard expands the original emphasis of the Shugart Associates Systems Interface (SASI) for floppy and rigid disk drives to include other peripheral devices as well. Under either scheme, hardware host adapters translate the unique message protocol of a specific system bus (e.g., IBM PC, Multibus, VMEbus) to a common protocol understood by all SCSI devices. In addition, software commands are issued for such generic device types as disk drives, tape drives and printers. Specific device information like sector addresses is omitted. In other words, SCSI/SASI presents a logical system interface to peripherals rather than a device-level interface.

Treating peripherals as generic classes simplifies the host operating system by moving formatting, error correction, physical sector addressing and other device-specific operations to intelligent controllers. The host operating system still retains its supervisory functions such as event scheduling and interrupt handling, but users must rewrite the device drivers to eliminate commands geared to a specific controller/peripheral combination.

SCSI peripheral controllers assume responsibility for physically addressing devices; host processors select the appropriate logical device and specify the first block address as well as the number of data blocks to be transferred. Up to 64 Kbytes of data can be transferred with a single host command. Larger amounts of data from either single or multiple devices are accommodated through the use of chained commands.

With a system-level interface, designers can place the controller anywhere in their system – it no longer needs to reside on the host backplane. For example, rigid disk drives from several vendors now include SCSI controllers; tape and floppy drives will probably follow suit. Integrating a SCSI controller on the drive becomes more feasible as key functions like formatting, data separation and serial/deserialization are implemented in silicon (see *Digital Design*, June 1985, p. 32).

Many current embedded SCSI controllers require a separate board from that used for the drive electronics. A device level interface such as ST506 or SMD is also needed to translate SCSI system level commands to the control signals executed by the drive. Drive vendors using this scheme include Cynthia Peripherals (Palo Alto, CA), Fujitsu America (Sunnyvale, CA), Iomega (Salt Lake City, UT) and Shugart Associates (Sunnyvale, CA).

Applied Information Memories (Milpitas, CA) and Xebec (Sunnyvale, CA)

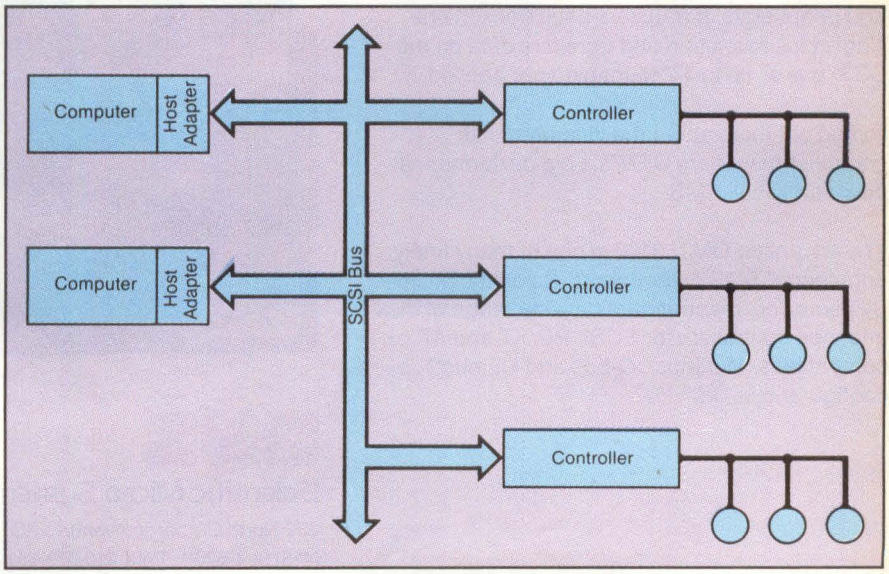


Figure 1: The SCSI bus can be described as a peer-to-peer architecture. Host adapters and controllers can assume either the role of request initiators or targets to perform operations. Up to eight host adapters and eight controllers can be attached in this manner.

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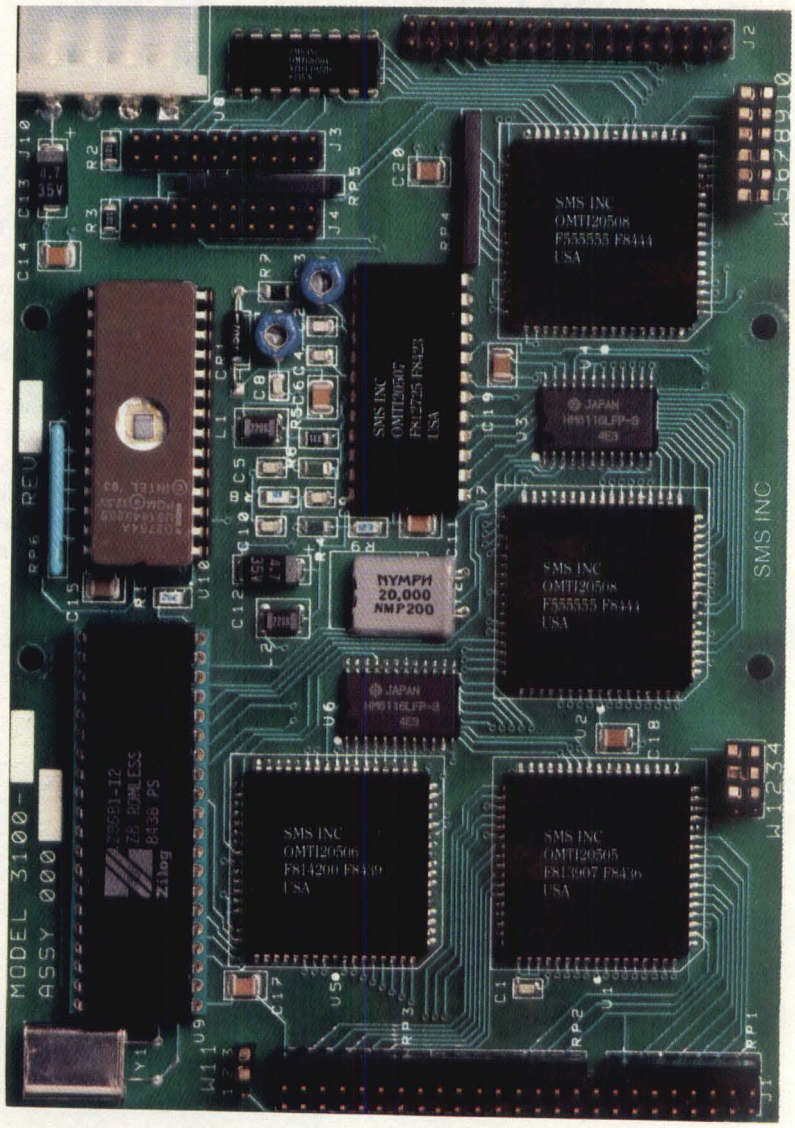

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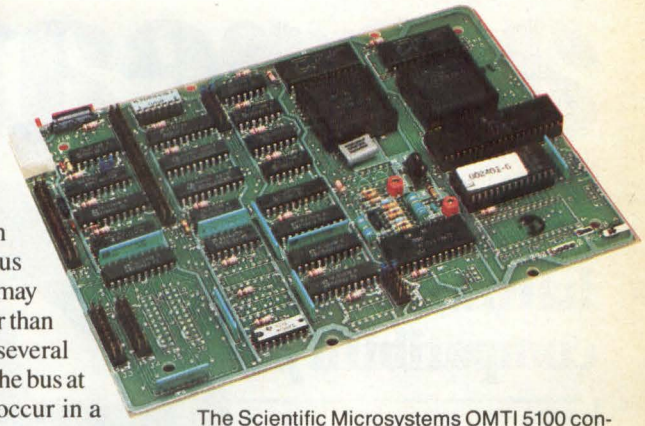

The Scientific Microsystems OMTI 5100 controller supports two fixed or removable 5¼" rigid disk drives. Non-interleaved data transfers and multisector buffering provide high throughput without overburdening the host. A VLSI chip set on OMTI SCSI controllers reduces part count on the board.

implement the SCSI controller on the same board as the disk drive electronics. Phil Devin of Xebec notes that the company needed to add a single chip for motor control to its SCSI controller to provide complete functionality. Seagate (Scotts Valley, CA) and Tandon (Chatsworth, CA) are also investigating this approach using SCSI controller chips from Western Digital (Irvine, CA).

Tape drives with embedded SCSI controllers are a ready means to back up rigid disk drives, since the interface proposal contains a COPY command that enables streaming operations without host intervention. Also, the interface has gained industry acceptance in its present SASI implementation. Tape drive manufacturers publicly supporting SCSI include Archive Corp. (Costa Mesa, CA) and Memtec Corp. (Salem, NH).

Embedded controllers work well on the SCSI bus since they can act as initiators or targets of bus transactions and thus do not rely on the host adapter to initiate each transaction like conventional standalone controller/peripheral combinations. Each controller can arbitrate with other devices for the bus, select a target (e.g., tape or cartridge disk drive) and initiate a transfer to that device.

Using such command schemes, task execution and I/O processing can occur simultaneously because host adapters can be disconnected from the SCSI bus once the host processor issues an I/O command. This frees the processor to execute other tasks. Controllers also disconnect from the bus after receiving the command from the host adapter. The SCSI bus remains free for other I/O operations until data needs to be transferred between the controller and the host adapter. Furthermore, peripherals and controllers can transfer data at 1.5 Mbytes/sec along the SCSI bus. Adequate buffering on the host adapter and the controller compensates for differing transfer rates between the SCSI bus and the system bus.

Although this scheme is more efficient than the master/slave protocol typically used on system backplane buses, it tends to move the traffic from the host bus to the SCSI bus itself. Thus, the SCSI bus may become a bottleneck rather than a solution, especially if several devices attempt to access the bus at the same time. This can occur in a multitasking SCSI environment when two or more transactions are initiated at the same time (e.g., seeking and reading from a disk while writing to tape). Several disconnect and reconnect operations can overlap as each device goes off the SCSI bus to perform internal operations and comes back on to transfer data.

Daniel Loski of Scientific Microsystems (Mountain View, CA) claims that a multifunction controller such as the OMTI 5400 is better suited for supporting multiple drives performing overlapped operations than dedicated controllers for each peripheral. A multifunction controller does not access the SCSI bus for transfers between these drives since it would not access the bus for transfers between devices attached to it, but would use internal buffers as the means of transfer. In fact, he notes that the internal buffers on a multifunction controller are much smaller than those used on dedicated controllers (8 Kbytes vs. 16 Kbytes) since information need not be stored during the arbitration and selection process.

The choice of the appropriate controller represents only half of the equation. In fact, the intelligence of the host adapter largely determines the functionality of a SCSI implementation (**Figure 1**). A simple adapter composed of discrete logic continues to place the brunt of I/O supervision on the host processor. However, this scheme provides an easy way to add controllers and peripherals into existing systems and is the most inexpensive SCSI option. In addition, system software remains largely unchanged since the SCSI bus acts as an extension of the system backplane.

However, system overhead is not reduced when simple host adapters are used with dedicated controllers. About 50% of system bus capacity is usually dedicated to servicing I/O operations, according to Loski. Minicomputers are notorious for bogging down in multitasking environments because their operating systems cannot speed data to the processor. Adaptec (Milpitas, CA), Emulex (Costa Mesa, CA) and NCR Corp. (Wichita, KS) have tackled this problem by moving I/O processing from the host operating system to the host adapter. This effectively frees 50% of the system bus for task execution.

Increasing the intelligence of the host adapter, however, also increases its cost. For example, microprocessors or high-speed discrete logic are needed to handle the arbitration and the selection/deselection protocols for multitasking (multiple device transactions on the same controller) or multithreading (multiple transactions occurring on the same SCSI bus). These costs further increase if large buffers are needed on the host adapter to streamline transfers between devices. On the other hand, Loski notes that a multifunction controller does not require such a sophisticated host adapter since the controller implements these functions on-board.

The wide range of options available within SCSI could prove daunting for even the most sophisticated designer. From embedded controllers to intelligent host adapters, users must carefully weigh the needs of their application and pick the appropriate mix to fit their budget since SCSI offers a solution for every price range.

—Aseo

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PERIPHERALS

Cartridge Disks Rediscovered

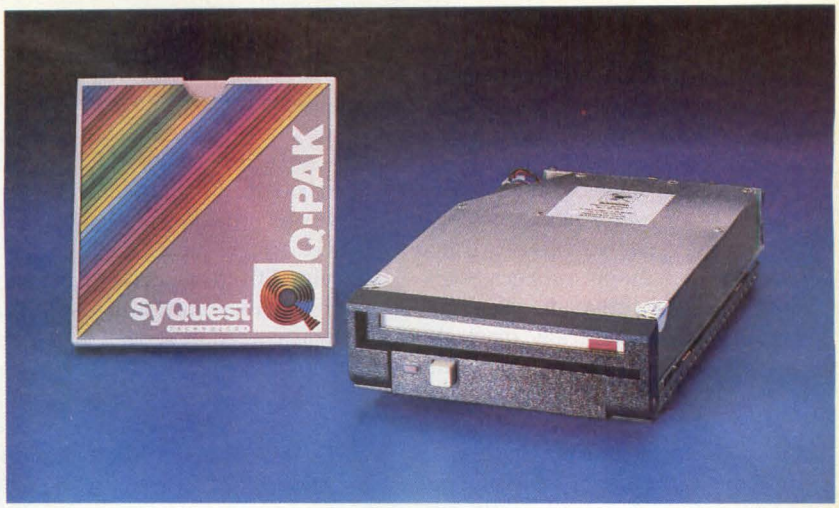

PHOTO COURTESY SYQUEST

The resurgence of the cartridge disk as a backup medium to fixed disk drives lends credence to the saying "The more things change, the more they stay the same." Originally spurned because of their relatively high cost compared to tape, cartridge disks are proving suitable for applications requiring file-oriented backup as well as immediate access to data. They have also found a place as the primary storage medium where removability serves as a security precaution.

The latest generation of cartridge drives has solved earlier problems of poor reliability and interchangeability by taking advantage of advances in media. Cartridge drive vendors have gone to standard disk interfaces, with SMD and ST506 the most common. In fact, except for their removability, these drives behave in the same manner as fixed disk drives since the same software drivers and hardware protocols are applicable to both.

The similarity in operation makes cartridge drives easier to use for file-oriented backup than tape drives. The primary drawback to tape drives is that, as serial access devices, individual files or records cannot be accessed in the same manner as on disk drives. This means that file-oriented backup and restore operations are slow, with average access times to a given sector on tape measured in seconds rather than milliseconds. Furthermore, potential users must write different device drivers and utilities to use tape drives.

Tape drives have been used for image backup, in which the contents of a fixed rigid disk drive are transferred byte for byte onto tape. This is useful when file systems are to be restored onto the same drive after a system crash. However, an image backup typically will not separate out defective sectors, so if users attempt to use an image backup to restore their files onto another disk drive, they may find that they cannot access any data since the defect map of the new drive will probably not match that of the old one. This also holds true when users attempt to transfer their files to a higher capacity drive.

Still, tape drives have the advantages of higher capacity and lower cost. A single cartridge disk can store from 5 Mbytes to over 40 Mbytes, compared to a single ¼" cartridge tape which stores 20-60 Mbytes, depending on the length used (300′ to 600′). Furthermore, only databases requiring immediate access to individual records (like medical images or circuit netlists) can justify the high cost of cartridge disks, typically $100 each. When retrieval times are less critical, ¼" cartridge tapes, at around $30 each, can be used. Users should determine which files fit the criteria mentioned above and take advantage of the benefits of both mediums.

For either backup or primary storage, cartridges provide reliability approaching that of fixed rigid drives, yet allow information to be moved from one drive to another. Cartridge disks provide a suitable alternative for applications that have outgrown the storage capacity of floppy disk drives.

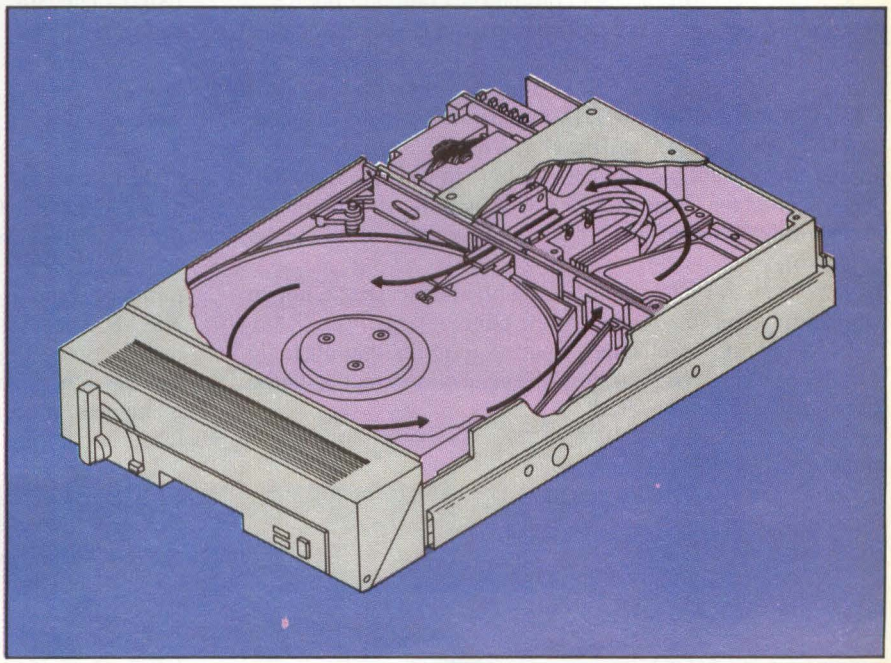

Figure 1: The disk cartridge for the Model 360 from DMA Systems undergoes a double filtration process before read/write heads are inserted. Two sets of filters clean the air as it enters and leaves the cartridge, with the disk itself acting as a centrifugal pump.

Reliability starts with the design of the cartridge itself. As with the head/disk assembly of a fixed disk drive, attempts are made to seal off outside contaminants from cartridges in a variety of ways. Two sets of filters are typically used to clean the air as it enters and leaves the cartridge (**Figure 1**). In addition, rubber gaskets are often used to form a tight seal around any areas where the cartridge meets the outside world (e.g., spindle). Because the disk itself acts as an air pump, the cartridge is also positively pressurized so that leaks do not occur along the seams.

To achieve the clean environment found inside fixed disk drives, cartridges usually go through a purge cycle prior to inserting the read/write heads. Amcodyne (Longmont, CO) and DMA Systems (Goleta, CA) slowly lower the heads to the disk surface—a practice often followed by fixed disk vendors who also use conventional oxide media. On the other hand, Micro Storage (Santa Clara, CA) and SyQuest (Fremont, CA) rely on the carbon overcoating on their plated media to resist head bouncing as the heads are lowered onto a special landing zone. Cartridge and fixed disk failure rates are nearly equal: MTBF estimates of 10,000 operating hours are common.

Beyond providing a reliable medium, disk cartridges must also be designed to be moved from one drive to another and access data accurately. To assure data interchange, vendors use self-aligning spindle mounts so that runout (or off-center effects) is minimized. In addition, Amcodyne, Century Data Systems (Anaheim, CA), DMA Systems, Micro Storage and SyQuest embed servo tracks on each disk surface to provide proper head/track alignment. Control Data (Minneapolis, MN) uses dedicated servo surfaces. As a further precaution, some drives go through a routine upon insertion of a new cartridge, trying to read the inside, middle and outside tracks of the disk.

Interchange capability also extends to the interface that is used. For 8" and larger drives, the SMD interface is preferred. SMD has the necessary signals and commands to support removability because the interface was originally designed for removable disk drives. Cartridge drives using this interface include those from Amcodyne, Century Data Systems and Control Data Corp.

However, no cartridge drive interface exists for smaller drives. In fact, the ST506 interface has had several signals redefined to support drives from DMA Systems, Micro Storage and SyQuest. These redefined signals may or may not be supported by fixed disk drive controllers. Users should work closely with the cartridge drive vendors to select controllers that support the modified signal lines as well as to make any changes needed in existing software drivers to support these changes.

Cartridge disks provide a suitable alternative to floppy disks and tapes for file backup and removable storage. However, users must gauge their applications to determine which data justifies their high cost and limited capacity. In addition, decisions about drive/controller combinations should take into consideration the level of support that the interface provides and the number of modifications to software drivers needed. —*Aseo*

LETTERS

Dear Editor:

As a manufacturer of C-44 compatible computer boards, I noted several errors in the table comparing CMOS computer buses on page 32 of your April 1985 issue [*Digital Design*, "PC Clones Challenge Role Of STD Bus," p. 30].

First, in addition to the NSC-800 and 80C85 processors, both the Motorola 146805E2 and the Harris 80C88 microprocessors are currently available on the C-44 bus. In fact, I believe that Onset Computer Corp.'s CPU-80C88 was the first commercially available board level product using the CMOS 80C88 processor.

Next, the C-44 bus supports a 20-bit address space, not an 8-bit address space as shown in the table.

Finally, the C-44 bus specification requires that all logic signals be buffered onto the bus. The table is incorrect in stating that signals are not buffered.

Sincerely,
James K. Elwell, Vice President
Quartic Systems Inc.
Salt Lake City, UT

Dear Editor:

In the April, 1985 issue of *Digital Design*, there is a tabulated comparison of CMOS buses on page 32 ["PC Clones Challenge Role Of STD Bus," p. 30]. There are several mistakes and omissions in the C-44 bus column.

1. Processor Supported—Only the NSC-800 and 80C85 are listed. The 80C88 and CMOS 6805 processors are also supported.

2. Address—The table shows 8 address bits for the C-44 bus. It has always had 16 bits for address and bits A16 through A19 were recently promulgated by the bus inventor, bringing the number of address bits up to 20. The C-44 bus is the only one of the three buses cited which carries the multiplexed data and address bits onto the bus. The other two buses carry de-multiplexed address and data on the bus.

3. Signals buffered onto the bus—The table says no. I have purchased and used two versions of Onset Computer Corp.'s NSC-800 cards and all processor output signals are buffered before going to the bus. I cannot say from personal knowledge that any other cards from Onset or any cards from any other manufacturer buffer the processor signals onto the bus, but I'll take a bet at long odds that they all do.

I have great interest in all CMOS board level products and CMOS bus architectures. I suggest that a truly comprehensive survey of low power products would be well received by us in the remote data collection and processing business.

Yours truly,
Jim Ellis
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Array Processors — Increasing Speed By MIPS, MOPS, FLOPS And GOPS

by Andrew Wilson, Sr. Technical Editor

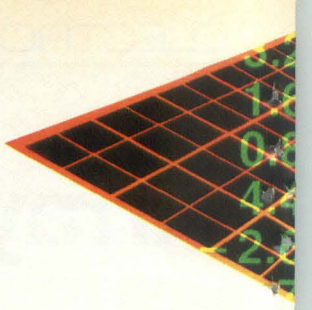
Array processors serve as a bridge between the von Neumann architectures of the past and the SIMD/MIMD architectures of the future. Acting as fast coprocessors, these machines are able to offload many of the repetitive calculations needed in scientific applications. Because of this, they have found greatest applications in image and graphics processing, finite element analysis, robotic vision systems and systems for remote sensing.

With the introduction of these machines new terminology has followed to define just how fast is fast. Manufacturers will specify performance of machines in Millions of Instructions Per Second (MIPS), Million Operations Per Second (MOPS), Floating Point Operations Per Second (FLOPS) and Giga Operations Per Second (GOPS). In bids to out-MOPS or out-FLOPS the competition, manufacturers will sometimes "benchmark" their processors on the fastest element in the system. For example, the new 29117 16-bit microprocessor from AMD (Sunnyvale, CA) features a microcycle time of 100 nsec, which transfers into a 10 MHz data rate for all instructions. Manufacturers choosing to build an array processor around the device, may then claim they have a 10 MIPS machine. Similarly, manufacturers may claim high throughputs by comparing code written in Fortran for one machine with code written in assembly language on another. Worse still, some machines are optimized for specific functions (such as one-dimensional FFTs) and perform very effectively for these functions. Thus, when benchmarked against other machines performing a very different function, they perform very badly.

To add to this confusion, the host computer-interaction must be taken into account. If, for example, an array processor is performing high-speed calculations and results need to be transferred to the host frequently, then the AP must be interrupted and the data sent over a common bus. If the bus bandwidth is small the AP will remain idle for longer than it is active, slowing system performance incredibly.

Despite this gloom and doom, many manufacturers have introduced machines which perform very effectively, using novel implementations to improve performance. For the user or potential buyer of such machines, one thing is apparent – the applications which the machine must perform must be carefully analyzed, the computationally intensive routines effectively documented and, if possible, submitted to the array processor manufacturer. In this way the user will obtain a true application specific benchmark.

In the first of three articles, Dr. Paz Kahana of CSPI (Billerica, MA) examines the concepts of computer precision in array processors – between that of 32-bit and 64-bit machines. Following this, Aaron Boxer of Masscomp (Westford, MA) shows how an array processor can be used to speed NMR imaging functions. Finally, Robert Frisch and Barry Eisenstein from Mercury Computer Systems (Lowell, MA) discuss the design of a new array processor.



Single Vs. Double Precision Computation

by Paz Y. Kahana, Ph.D., CSPI, Billerica, MA

When performing scientific or floating point oriented calculations using a digital computer, a decision must be made about the degree of precision required for the computation and the representation of the results. Often the decision is already made because of the resources available or the budgetary or the organizational concerns. However, all active buyers of scientific computing equipment make this decision during the brand selection process of the purchasing cycle.

It has become customary among scientists and engineers to specify single precision of computer word size for tasks such as FFTs, convolutions, image, and speech and signal processing. Problems involving (large) matrices, optimization algorithms and minimizations or maximizations mostly require the higher accuracy associated with double precision computer word representation.

Determining whether an application requires double or single precision involves a balance between selecting the right tool for the computation and not investing more than is necessary. Computing machines (standalone computers and attached array processors) offering double precision capability (64 bits of word size) contain more hardware logic and software and are, therefore, more expensive to develop, purchase and maintain.

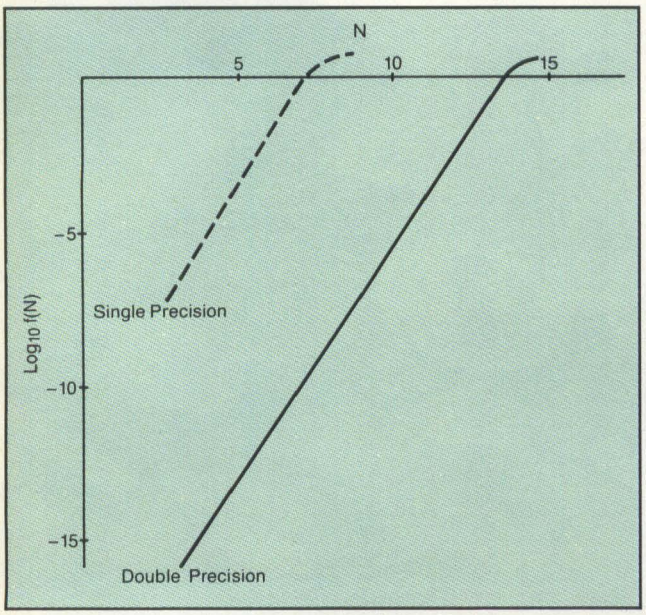


Figure 1: The function $Log_{10}F(N)$, as defined in **Equation 6**, is for various matrix sizes N. The broken line represents the results of a single precision calculation on a VAX 11/780 (32-bit word length). The solid line represents the results of a double precision calculation on the MAP-6420 array processor (64-bit word length, 56 bits of mantissa and 8 bits of exponent) from CSPI attached to the same VAX 11/780.

The general question of accuracy and precision of physical experiments can be traced to the very fundamentals of our understanding of nature. Different computer designs may affect the way the computer handles the arithmetics, round-off errors and overflow and underflow conditions.

Scientists are limited in their ability to conduct certain measurements. Such limitations can result from poorly or incompletely defined systems of reference, inaccurate measuring tools or techniques, practical considerations and even the most basic laws of nature. When developing theoretical models or other algorithms aimed at explaining and predicting experimentally observed data, it is often necessary to introduce approximations to reduce the problem to manageable size and complexity and sometimes even to obtain a solution at all.

It is likely to expect basic measurement and approximation errors in any problem even before it reaches the computer. There is nothing that can be done about this but to make sure that the situation does not get worse by the compounding of whatever errors the computer adds in the computations.

Digital computers store numbers in a fixed size computer word, particular to the computer architectural design. In all but a small number of cases, real numbers are only approximate representations to the true numbers. Errors in computer representations may result from rounding and chopping, loss of lead digits, and overflow and underflows. If X and Y are representations of X^0 and Y^0, we may define the relative errors σ and τ as

$$x = (1 + \sigma)\, x^0$$

$$y = (1 + \tau)\, y^0 \qquad \textbf{Equation 1}$$

The relative error may be positive or negative, but we assume each to be "properly bounded" for the sake of this illustration. When X and Y are multiplied, the result X*Y may be represented as

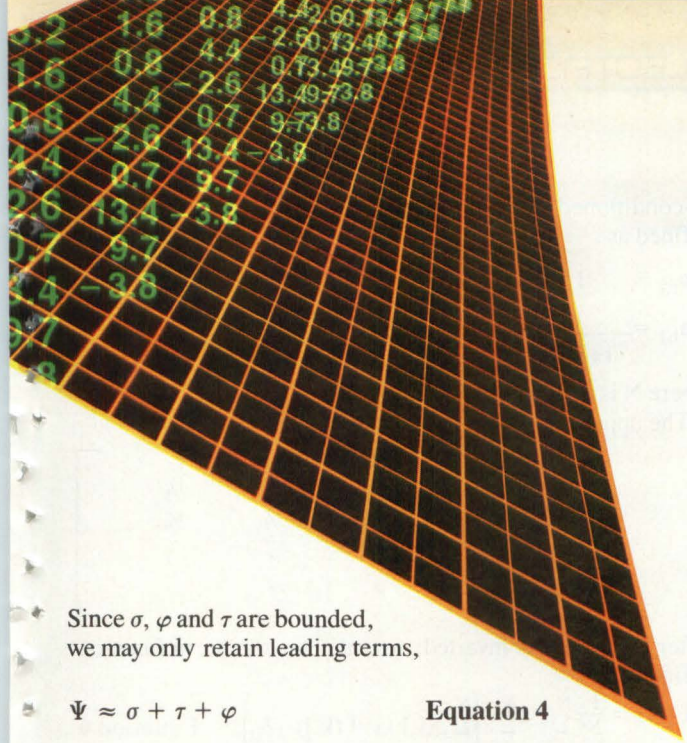
$$x * y = (1 + \varphi)\, x^0 y^0 \qquad \textbf{Equation 2}$$

where * denotes the computer product, and φ behaves similarly to τ and σ. By combining **Equation 1** and **2**, and applying proper algebra we obtain

$$x * y = (1+\Psi)x^0 y^0$$

with

$$\Psi = \sigma + \tau + \varphi + \sigma\tau + \sigma\varphi + \tau\varphi + \sigma\tau\varphi \qquad \textbf{Equation 3}$$



Since σ, φ and τ are bounded, we may only retain leading terms,

$$\Psi \approx \sigma + \tau + \varphi \qquad \textbf{Equation 4}$$

Since we do not know the signs of the individual relative errors, we must conclude that the relative error of the product is the sum of the relative errors of the product components. Of the three error sources τ and σ originate from the computer representation of X^0 and Y^0, and φ is because the computer performs X*Y and not the true product X^0Y^0.

If the algorithm used calls for a long series of repeated multiplications, it is not hard to realize that the error introduced in one cycle will continue to propagate during each iteration. For this reason it is necessary to determine the required number of significant digits and ensure that the relative error of the final result is outside the range of the desired significant digits.

Similar analysis may be performed for machine additions and subtractions, and the following results are obtained

$$x \oplus y = (1+\varphi)\,(x^0+y^0)$$

$$x \ominus y = (1+\varphi)\,(x^0-y^0)$$

where $\oplus$ and $\ominus$ are machine defined operations. If $X, Y > 0$,

$$x \oplus y = x^0 + y^0 + \sigma x^0 + \tau y^0$$

so

$$x \oplus y = (1+\Psi)\,(x^0 + y^0)$$

with

$$\Psi\,(x^0 + y^0) = \sigma x^0 + \tau y^0$$

This means that the add relative error in $X + Y$ is at most the machine relative error in one of the terms.

The subtract case is different since there is no bound for the relative error in the result because of errors in the operands. For example, consider

$$X^0 = 1.23456776 \text{ with } X^0 = 1.2345678$$

$$Y^0 = 1.23456774 \text{ with } Y^0 = 1.2345677 \qquad \textbf{Equation 5}$$

The floating point result of X^0-Y^0 is 2.00×10^{-8}, while $X-Y = 1.00 \times 10^{-7}$. As a result of the operation, the relative error grew from an order of a millionth of a percent to 400%. It was the loss of significant digit that caused this magnification in the relative error.

A sufficient theoretical background has been established to analyze the problem of accuracy in scientific and engineering computations. Error sources will originate from the fundamental uncertainties imposed by the laws of nature (such as the uncertainty principle), errors in measurement or statistical noise in data, errors due to approximations introduced into formalisms and theories to handle data and the variety of computer related errors caused when data is manipulated. The algorithm used and the way computers perform the computations (total word length, computer algebra definitions and number of bits of the mantissa and exponent) may affect the accuracy of the result. When floating point calculations are required, it is crucial to minimize computer generated errors since they are added to all the others previously introduced to the problem.

At the heart of most scientific and engineering floating point computations there are likely to be polynomial expansions, matrix algebra and eigenanalysis, numerical integration, linear tranformations as well as nonlinear integrations and transformations. Although there are many other specialized applications in use, the majority of scientific applications contain elements of the above in core solvers or as part of the calculations.

Using the simplified but important results of the relative error analysis it can be understood why matrix computations, for example, require double precision. Diagonalization of a matrix involves a total number of multiplications proportional to N^2, where N is the dimension of the matrix. For even medium matrices the error propagation may be so large that the results will not be accurate within the required number of significant digits. Optimization problems and minima and maxima problems involve subtraction of close numbers. The resulting relative error may be so large (**Equation 5**) that no logical or subsequent arithmetic operation can be meaningful in single precision. **Equation 5** will produce correct answers to 15 significant digits in double precision but will fail in single precision. Sometimes even simple function evaluation such as exp(x) or sin(x) may produce erroneous results in single precision. In these and other cases it is necessary to work in double precision.

The disciplines where such situations arise include hydrodynamics, structural and network analysis and quantum chemistry and physics, where large matrices are handled, flow analysis and reservoir modeling, where nonlinear differential equations are being solved, and chemical kinetics, scattering and reaction dynamics, where ordinary (differential) equations on motion are integrated.

By contrast, in applications such as image rotation and compression, linear transformations are applied only a few times. Error propagation is thus contained and single precision conditions will suffice.

Similarly, FFTs and convolutions are calculated by a suitable series expansion. Convergence can be tested for by making use of enough terms, and algorithms exist to ensure it. Again, single precision will provide good accuracy in such cases.

To demonstrate the difference in computational accuracy between single and double precision a simple computation was conducted, applying a commonly used problem – matrix inverse using column pivoting technique. A particular case of an

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ill-conditioned matrix was selected, that of the Hilbert matrix defined as

$$a_{i,j} = 1 \qquad (\forall j)$$

$$a_{i,j} = \frac{1}{i+j-1} \qquad (i \neq 1)$$

where N is the matrix dimension.

The upper left part of the matrix is

$$\underline{\underline{A}} = \begin{bmatrix} 1 & 1 & 1 & 1 & . \\ \frac{1}{2} & \frac{1}{3} & \frac{1}{4} & \frac{1}{5} & . \\ \frac{1}{3} & \frac{1}{4} & \frac{1}{5} & \frac{1}{6} & . \\ . & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \end{bmatrix}$$

After the matrix is inverted, we calculate the norm function defined as

$$F(N) = \frac{1}{N^2} \sum_{i=1,\ j=1,\ k=1}^{N} \left[\sum^{N} a(i,k) a^{-1}(k,j) - \delta_{ij} \right] \qquad \textbf{Equation 6}$$

This norm should vanish under ultimate precision conditions.

In **Figure 1** the behavior of $\mathrm{Log}_{10}F(N)$ is plotted as the matrix dimension N is varied for both single and double precision calculations. The broken line represents the single precision (32 bits) results on a VAX 11/780. The solid line represents the results of the same calculation performed on the MAP-6420 array processor from CSPI (Billerica, MA) attached to the same VAX 11/780 in double precision (64-bit word length, 56 bits of mantissa and 8 bits of exponent).

There is a serious lack of precision in the single precision computation even for small matrices. For larger matrices neither computation is accurate, but the double precision run provides more accurate results over a range of matrix size.

This test is particularly demanding and is not expected to be encountered often in real applications. The matrix elements become of similar numerical magnitude in the lower part of the matrix resulting in a much larger subtraction error that is added to the multiplication error, which is the underlying reason for the severe ill-conditioning of the Hilbert matrix. Whereas many matrices in science and engineering applications do not behave like this, the illustration it provides is quite revealing; not even small matrixes can always be diagonalized properly, and double precision must be used.

It is up to the user to understand the nature of the problem, the algorithm and the program used to solve it to make the decision concerning the required accuracy of the results and to determine whether single or double precision should be used. Increasing precision capability in the hardware has a direct monetary cost. Double precision can also be implemented in software but leads to series speed degradation which may be unacceptable. Despite its higher cost it is generally true that double precision capability is best implemented as a hardware feature supported by a high-level language compiler. DD

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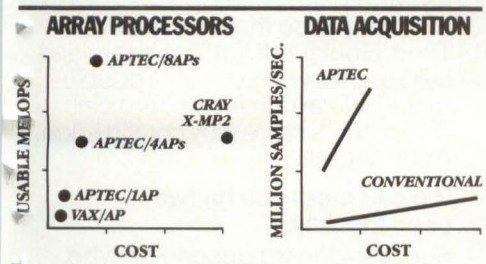

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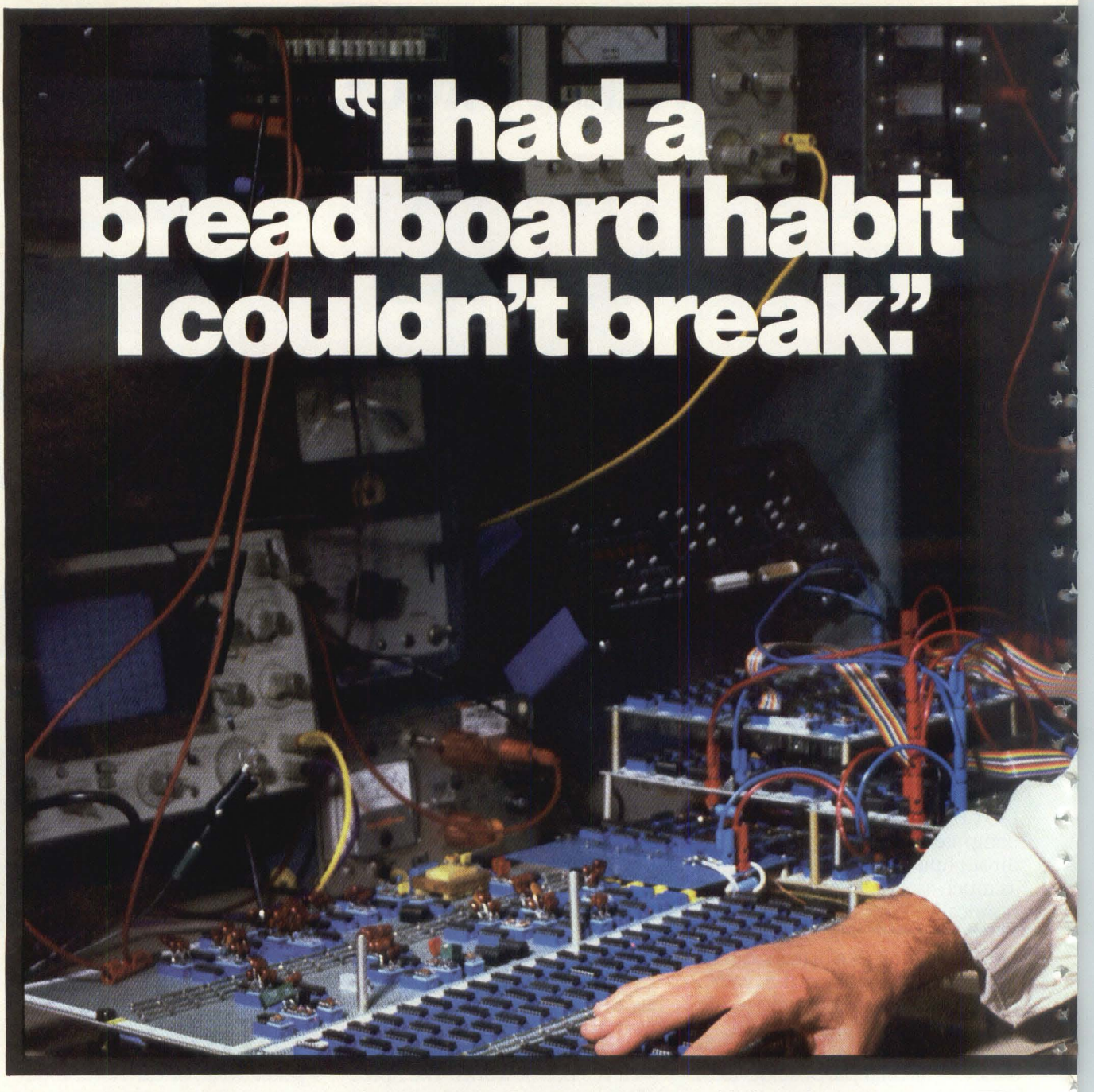

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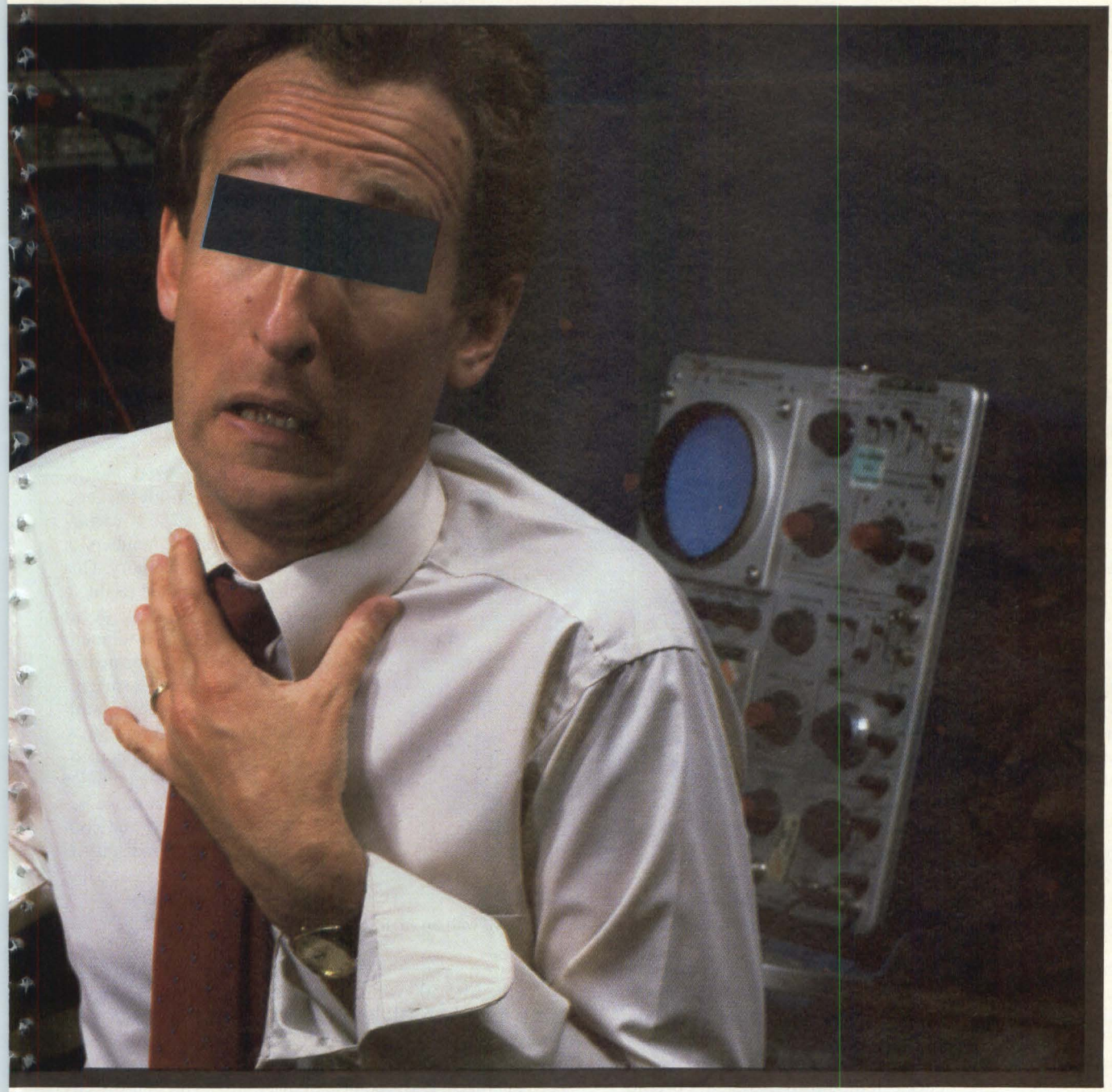

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Integral Array Processor Speeds Image Processing

by Aaron Boxer, Masscomp, Westford, MA

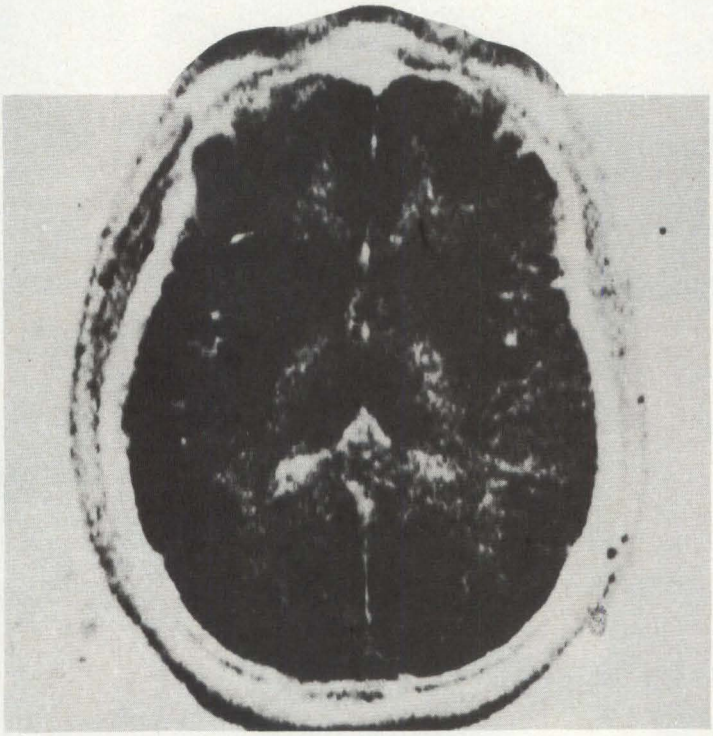

Figure 1: NMR brain scan performed on an MC-500 with an AP-501 array processor.

Array processors (APs) are designed to perform repetitive computations on regular structures of data at much higher speeds than general-purpose CPUs. They take advantage of this regular structure to perform several pipelined operations simultaneously. Many scientific computation and image processing problems can be performed significantly faster on an AP. Until recently, array processing hardware was available only on supercomputers, and access to the hardware was very expensive. Today, APs are sold as peripherals that attach to mainframe minicomputers.

These peripheral APs communicate with the host computer through standard buses such as Intel's Multibus or DEC's Unibus. These buses are not always the fastest ones in the computer system. Data sets to be operated on are often very large and transferring this data between the host memory and the AP memory can be a bottleneck in the host/AP system's overall performance.

An integral AP made by Masscomp for its MC-500 series computers solves this bus bottleneck. The AP-501 does DMA transfers on the MC-500 private CPU-memory bus which has a bandwidth of 8 Mbytes/sec. This is two to three times the speed of the Multibus and the Unibus, thus lowering the performance impact of DMA data transfers between AP memory and MC-500 main memory.

NMR Imaging

Nuclear magnetic resonance (NMR) is rapidly gaining acceptance in the medical community as a medical imaging technique. It can produce high quality images of bone and tissue without the use of X-rays. **Figure 1** shows an NMR brain scan performed on an MC-500 with an AP-501 array processor from NMR Imaging Inc. (Houston, TX). Producing this image from the input data required over six million floating point calculations.

Data is digitized into the MC-500 as 16-bit integers, arranged as a 256 × 256 array of complex numbers in the host main memory. This array is converted to single precision floating point numbers and a two-dimensional FFT is performed on the whole array. The magnitude of each complex number in the resulting 256 × 256 FFT array is computed. Finally, all the magnitudes are scaled into a range between 0 and 255 and converted to bytes for display as the pixels of an image like the one in the photo.

Data Flow

Figure 2 shows the architecture of the MC-500 with its AP and the flow of data. Analog signals from the NMR hardware are sampled by a 12-bit A/D converter. The converted data is transferred as 16-bit quantities to the host memory over the Multibus. The DACP is a high speed intelligent DMA controller that transfers the data directly from the A/D converter to MC-500 main memory. The 256 × 256 array of complex numbers occupies a total of 256 Kbytes of main memory.

The AP DMA transfers one row of 256 complex numbers at a time from main memory into AP memory over Masscomp's high speed CPU-memory bus. In the AP, the row of data is converted to single precision floating point numbers (IEEE 754 format) and a complex FFT is performed. The AP DMA transfers the result back to the host main memory on the CPU-memory bus. This process is repeated for all 256 rows of data. This first dimension of the 2D FFT produces a result array of 512 Kbytes in main memory.

The host CPU transposes rows and columns of the result in main memory before the second FFT. The AP DMA transfers a row of 256 complex single precision numbers from the transposed result array in main memory to AP memory and another

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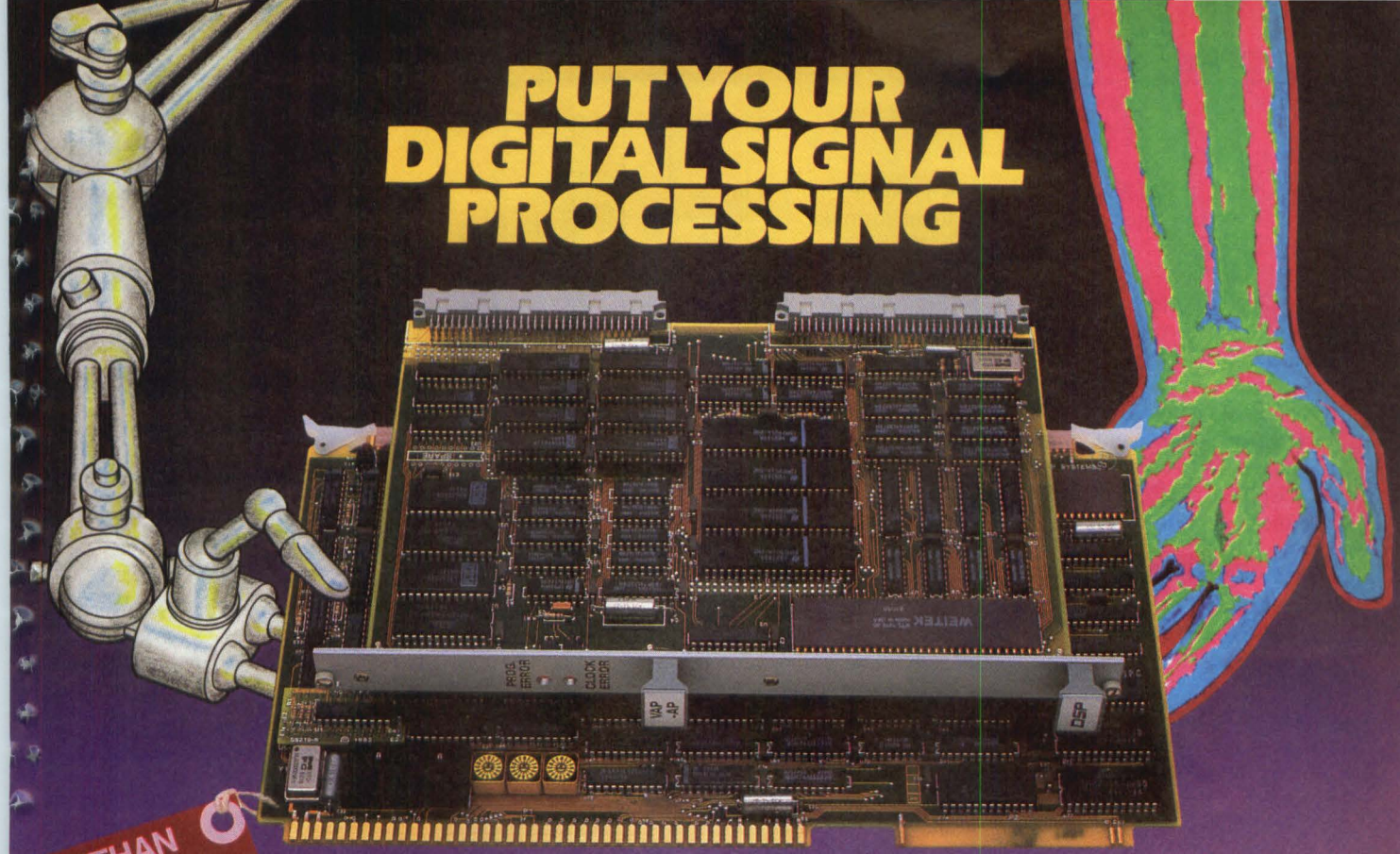

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FFT is performed. The magnitude of each complex number in the result is then calculated according to the formula:

MAG = SQRT(real[X] + imaginary [X])

where X is a complex number. The result is scaled into the range of 0 to 255 and converted to bytes before the AP DMA transfers it back to the host main memory. This process is repeated for each of the 256 rows of the transposed matrix in the host main memory.

The final result is a 256 × 256 array of bytes that is transferred from main memory over the Multibus to the raster memory of Masscomp's graphics processor (GPM). There they are displayed as a 256 × 256 array of 8-bit pixels in an image like the one in **Figure 1**.

Parallel Processing

The NMR application was described as if each step was performed sequentially. Significant performance improvements can be realized by performing several functions in parallel with the AP and the CPU.

A high degree of parallelism can be achieved by treating each row of 256 complex elements as a separate set of data. All the operations that can be performed on a row by the AP or the CPU are completed before the data is moved to the next piece of hardware. **Figure 3** represents a "snapshot" of several pieces of the first FFT in the NMR computation occurring at once.

The AP in **Figure 3** is performing DMA transfers and vector calculations simultaneously. Row 3 of the raw 16-bit integer data from main memory is being DMA transferred into the AP vector memory while the AP vector hardware is converting row 2 into floating point numbers and doing the complex FFT on it. The previously completed FFT of row 1 is also DMA transferred back to main memory.

The AP requires 1.5 msec to convert to floating point format and perform an FFT on the 256 elements in row 2. The DMA transfer from main memory of row 3 into the AP takes 0.35 msec. DMA transfer of the completed FFT of row 1 from AP memory back to main memory takes 0.4 msec. DMA hardware in the AP performs the two transfers serially rather than simultaneously. They total 0.75 msec which is less than the computation time on row 2. DMA time is not a bottleneck in the AP process since it takes less time to transfer row 1 out and row 3 in than it does to perform the computations on row 2.

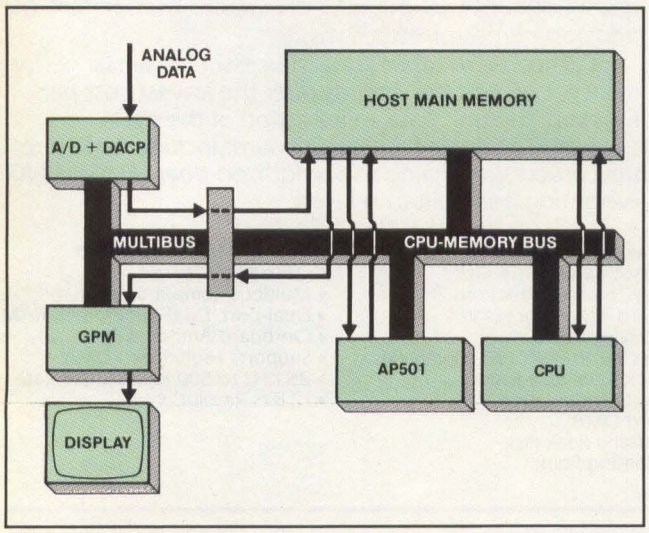

Figure 2: Data flow path for NMR imaging application.

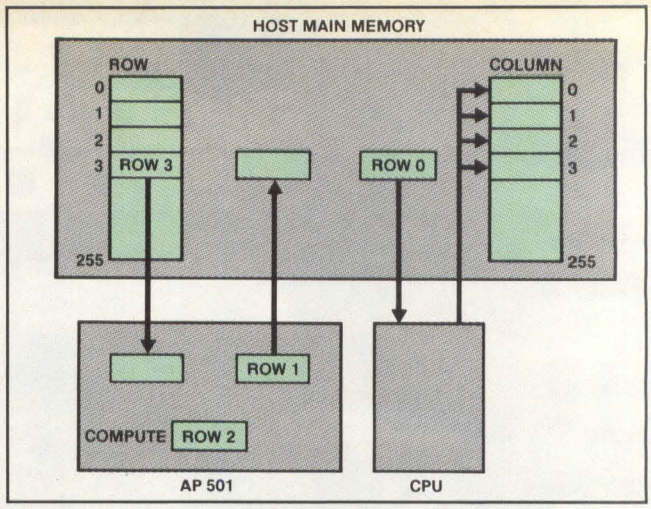

Figure 3: Parallel processing in NMR application.

The CPU transposes the FFT from row 0 in main memory into a column matrix in main memory for the next FFT concurrently with the AP activity mentioned. This takes 1.3 msec for the row of 256 complex floating point numbers. The CPU also takes 0.4 msec to issue instructions to the AP to perform the computations and the DMA transfers.

The CPU tasks take 1.7 msec which is longer than the AP tasks. The application software is designed so all the AP tasks are synchronized with the CPU. The next set of DMA transfers and AP computations do not begin until the CPU has issued the current set of AP instructions and transposed a row of FFT data. The 1.7 msec of CPU tasks is repeated 256 times for a total of 425 msec for the first FFT of the NMR imaging computation.

In the second FFT, the CPU's only task is issuing instructions to the AP. The DMA transfers between the host main memory and the memory occur simultaneously with AP computations.

Each column of 256 complex floating point elements contains all the information necessary to produce one column of 256 bytes for the final image. Therefore each column of complex data is transferred from host main memory to AP memory only once, and all the computations to produce the column of bytes are performed before returning the result to the host memory. These tasks include the second FFT, the magnitude calculation scaling to a 0 to 255 range and the conversion to bytes. All computations combined require 6.9 msec per column for a total of 1.7 sec for all 256 columns.

The 256 × 256 byte pixel array is now ready for display on the MC-500 graphics display as an image. The total time to perform the 6 million floating point computations required for the photo is 2.2 seconds.

The application described took about 90 seconds on an MC-500 without an AP. NMR Imaging Inc. added a single-board AP and partitioned the problem into parallel tasks that could be divided between the AP and the host CPU. The result was a 30 times performance improvement for about a 20% higher system price. DD

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Modular Array Processor Features Dual Processor Design

by Robert Frisch and Barry Eisenstein, Mercury Computer Systems, Lowell, MA

There are two major problems associated with array processors: lack of compute power and difficulty of use. Although some array processors (APs) offer high throughput, they require the user to program in microcode. Other APs reduce the programming task, either by providing support in a high-level language such as Fortran or by providing the customer with a library of preprogrammed functions. However, these approaches reduce the system's performance, limit its flexibility or both.

Many APs are also optimized for a single data format and a specific type of operation, such as the FFT. Such machines fall short of advertised performance in most real-world applications. More versatile designs exist, but they pay a penalty in speed, price or both. Also, most architectures are usually "closed"; that is, there is no provision for the user to customize or enhance the hardware.

Mercury Computer's ZIP 3200 AP contains two processors: a pipeline for high-speed calculations and a control processor (CP) for data management. Each processor has its own program memory and control logic, so algorithms can be run with little or no assistance from the host computer.

To reduce further the need for service from the host, the ZIP has a 128K data memory, expandable to 16 Mbytes, and I/O ports that interface directly to external devices such as A/D and D/A converters.

Using the AP in a typical system (such as the Multibus), the pipeline resides on a separate circuit board, so that the user can change the AP's data format by changing the pipeline processor.

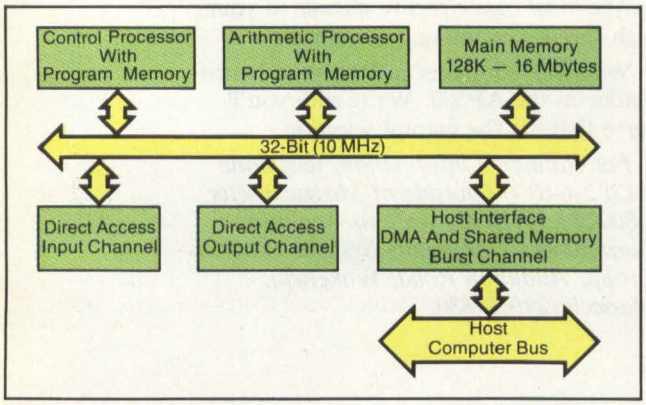

Figure 1: Main components of the ZIP array processor consist of the control processor, the main memory, the external ports and the host interface.

Currently, two pipelines are available: the fixed point 3216 and the floating point 3232. Future pipeline designs will support data formats up to 64 bits.

As **Figure 1** shows, the main components of the ZIP are the CP, pipeline, main memory, external I/O ports and host interface. All components communicate via the main ZIP bus, which is 32 bits wide and has a 100 nsec transfer time, for a throughput of up to 40 Mbytes/sec.

The CP is a general-purpose computer based on the AMD 29116 controller. It handles functions such as passing data to and from the pipeline, computing memory addresses, controlling program sequencing in the pipeline and passing data among various parts of the system.

The presence of the CP increases performance by relieving the host computer of many data management tasks. The CP's instruction set includes such operations as rotate and merge, that can be performed in 100 nsec. It has thirty-two 16-bit general registers, sixteen of which are extended by external logic to 23 bits. The CP also features a real-time clock, 11 interrupt vectors and automatic memory refresh via cycle stealing.

The CP and the pipeline have 2048 words of program memory each. The CP has the ability to load overlays, modules of program code that are kept in the ZIP main memory until they are needed. Development software includes a linking loader and run-time executive that support programs with up to 256 overlays. Thus, the ZIP can execute complex algorithms with no need for service from the host computer.

One important feature of the ZIP is how it synchronizes data flow between the two processors. The pipeline halts when its input buffer is empty or when its output buffer is full. Similarly, the CP will halt if it tries reading from an empty buffer or writing to a full one. One of the processors will resume execution when the other clears the bottleneck by reading or writing the proper buffer. This mechanism simplifies the need to measure pipeline delays to ensure that all parts of the ZIP are properly synchronized.

At the heart of the ZIP is the arithmetic pipeline processor. Two versions are currently available: the 3232 performs floating point arithmetic on 32-bit data, and the 3216 performs fixed point arithmetic on 32- or 16-bit data.

The 3232 (**Figure 2**) is based on the AMD 29325 ALU chip, which is notable for its high throughput. Its design allows the result of any calculation to be immediately available as input to the next without pipeline delays. The 29325 performs fix, addition, subtraction, multiplication and float operations, operating on data in either the IEEE standard format or in DEC

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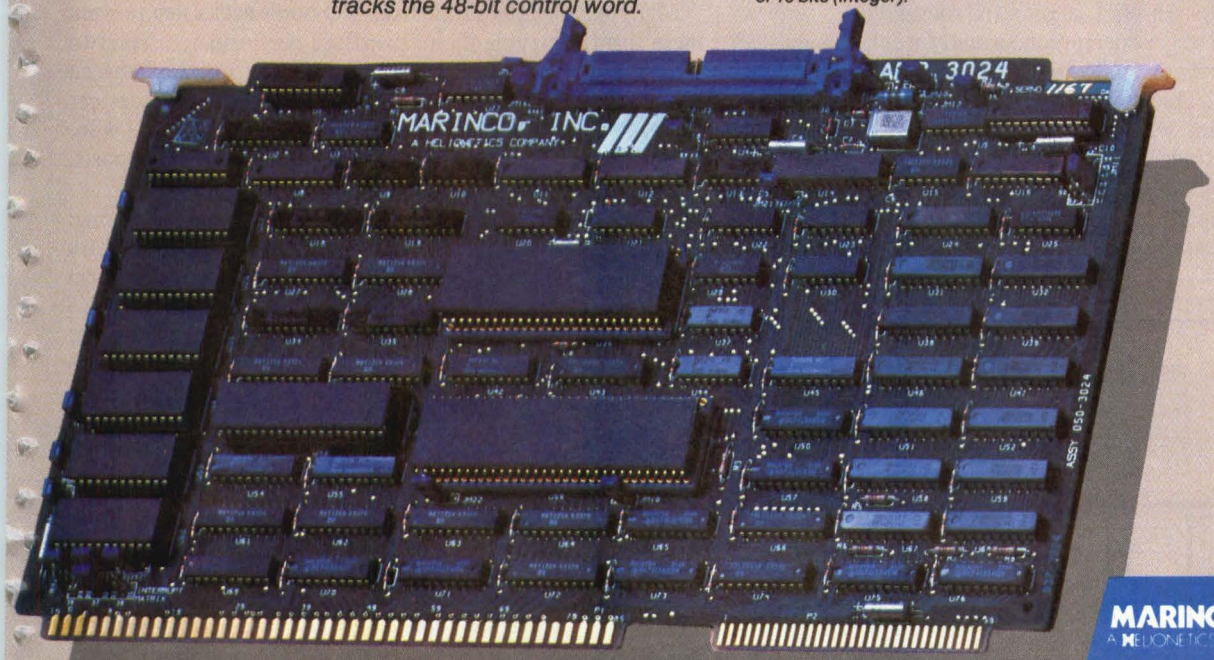
***Program Memory** 2K X 48-bits **Data Memory** 8K words **Data Word** 24 bits long, 8-bit exponent, 16-bit mantissa (floating pt.) or 16 bits (integer).*



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format. External circuitry provides logical AND and OR functions and formatting operations such as clearing and sign extension. A "subtract from 2" operation provides quick execution of the Newton-Raphson algorithm for computing reciprocals.

The power of the 29325 is augmented by the Weitek 1066 multiport register file. This device contains 32 words of RAM, a look-up table for reciprocals and square roots, three input ports and three output ports. Twenty-four words of RAM are used as input buffers, output buffers and temporary registers for intermediate results. The remaining eight words are dual-mode; they may be used either as input buffers or as temporaries.

Input buffer words are divided into two banks. While the pipeline is using one bank, the CP can load new data into the other. Words used as temporaries can always be accessed, regardless of which bank is in use. The output buffer is operated as a FIFO.

A useful feature of the pipeline is its ability to save the sign bit of any result in a status register. This bit can be used by conditional statements to provide an IF-THEN-ELSE function within the pipeline. This allows it to execute complex routines with no intervention by either the CP or the host computer.

The 3232 can process data at a rate of 8 MFLOPS. For more demanding applications, the ZIP can drive two pipelines for throughputs up to 16 MFLOPS. For the ultimate in performance, multiple ZIPs can be placed in a single host computer.

Users that do not require such high performance may prefer to use the 3216 fixed point pipeline. This unit can operate on integer or fractional data. Fractional data allows it to be used for block floating point operations, in which the CP manages the exponents.

The 3216 (**Figure 3**) has a five stage pipeline consisting of ALU, input buffers, multiplier, scaling and rounding logic and an output FIFO. All stages operate concurrently at either 20 million operations per second in 16-bit mode or 5 million per second in 32-bit mode. The pipeline can switch from one mode to the other mid-stream, with no lost cycles. This allows the programmer to freely trade precision for speed at any point in the program.

The 3216 has four accumulators for storing intermediate results. The accumulators are 48 bits wide to minimize rounding errors in long chains of calculations. Results are automatically truncated to 32 or 16 bits in the output buffer.

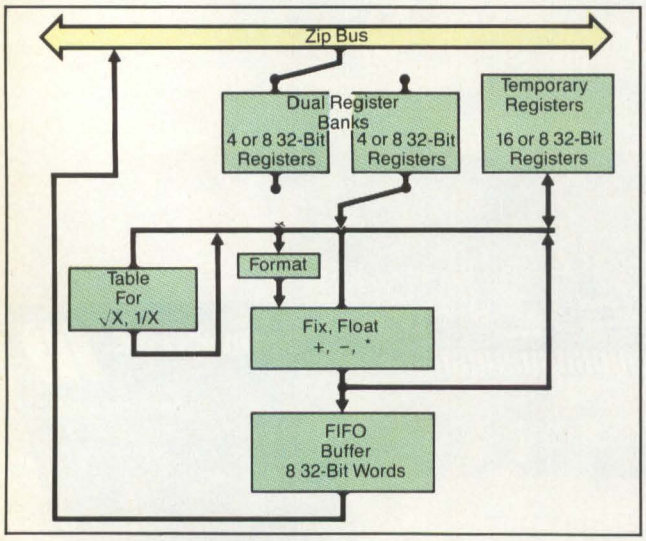

Figure 2: Arithmetic pipeline for the ZIP 3232 which can perform floating point arithmetic on 32-bit data.

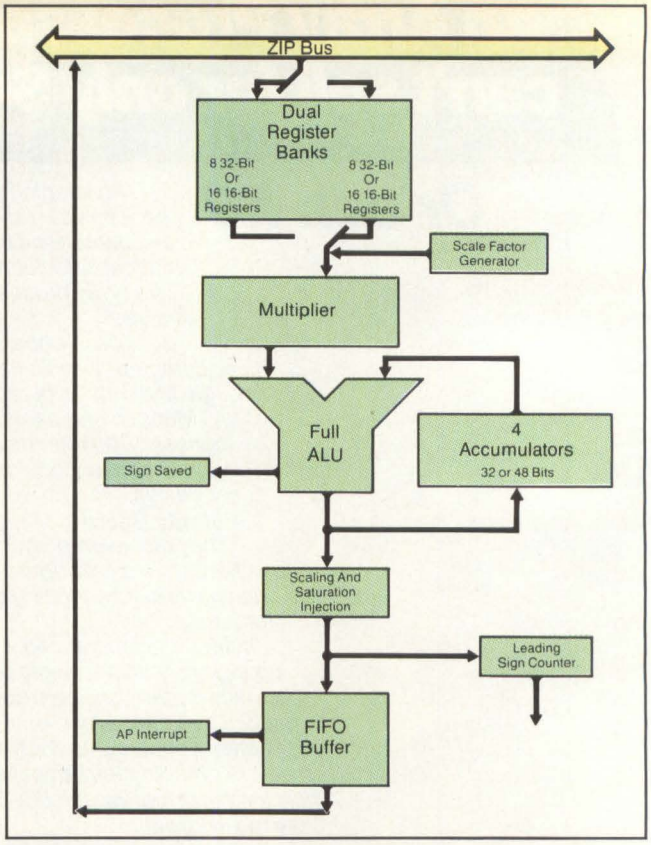

Figure 3: Arithmetic pipeline of the ZIP 3216 which can perform fixed point arithmetic on 32- or 16-bit data.

Many AP designs suffer from I/O bottlenecks that prevent them from achieving their advertised performance. The two most common places for such bottlenecks are transfers between the AP and the host and between the AP and the external devices such as A/D converters. Throughput in these two areas is increased by the ZIP's host interface and by its external I/O ports, respectively.

The host interface includes a programmable burst channel that transfers large blocks of data into or out of the ZIP with minimal overhead to both the ZIP and the host. The channel can transfer data at speeds of up to 400 nsec per word (5 Mbytes/sec), while using only 100 nsec of ZIP processing time. When two or more ZIPs are placed in a single host, they can use the burst channel to pass data among themselves with no intervention by the host.

The external ports may be configured by jumpers to function as separate 16-bit input and output ports or as a single 32-bit bidirectional port, with a throughput of up to 20 Mbytes/sec. Onboard handshaking logic provides easy interfacing to the user's devices, and each port includes four control (output) and status (input) bits, whose functions are completely user-definable. The CP's vectored interrupts assure fast response to the ports' data needs. **DD**

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Alexander Baillie
FMPS Project Manager
Canadian Astronautics Ltd.
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"We chose Canadian Astronautics and Star Technologies to provide us with the fastest processing system in the world for remote sensing image analysis involving geographic information."

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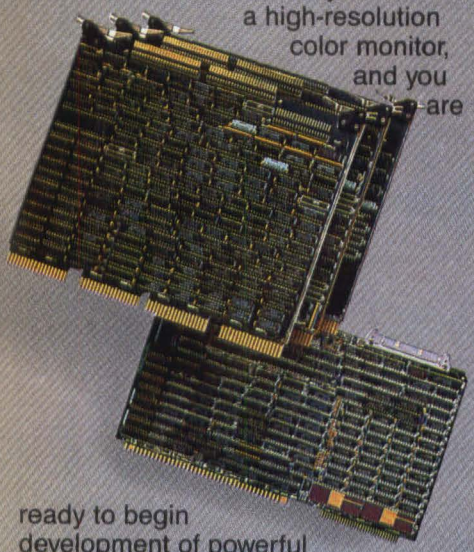

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"...drawing speeds of up to 88 million pixels per second."

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Maintaining Compatibility When Upgrading The 8086/87

by Jack Sterett, Al Brown and Gary Hornbuckle, Tektronix Inc., Wilsonville, OR

Intel's 16-bit microprocessor family provides a planned upgrade path with code-compatible processors that offer a range of performances. Two members of this family are the 8086 with its math coprocessor, the 8087, and the higher performance 80286 which has an 80287 coprocessor. Because of the use of the 8086 family in the IBM PC, there is a large software base of 8086-compatible software that system designers wish to protect when upgrading the performance of their existing product lines. This makes the 80286 a logical choice for product extensions and upgrades. Although the conversion from the 8086 to the 80286 is mostly a straightforward process, system designers should be aware of several details. Extending the Tektronix color graphics workstation product line from the 8086-based Tektronix 4110 Series to the 80286-based 4120 Series may prove valuable to others making the 8086/80286 conversion.

Tektronix' 4120 Series includes three color graphics workstations, the 4125 with high-resolution 2D capability, the 4128 with 3D wireframe and the 4129 with 3D shaded surface graphics. The 4120 Series provides improved performance over the 4110 Series both in terms of speed and graphics capabilities. The added functionality of 3D graphics necessitates a much larger firmware storage capability and higher computational performance to accomplish the more complex graphics calculations with comparable response time. A major design goal of the new series was to maintain complete upward compatibility for application programs originally targeted for the 4110 Series. Major engineering objectives for the new workstation hardware were to double the CPU performance, to double the EPROM available for software enhancements without reducing user RAM space, to open a system board slot for other options and to ensure complete application compatibility with the 4110 Series. Given these goals, the 80286/87 processor, math coprocessor combination was the logical choice for the new workstation.

The 80286 is a high-performance 16-bit microprocessor that is instruction-set compatible with its 8086 predecessor. Although the new processor operates at a higher clock rate, the two to three times performance improvement of the 80286 is due largely to improvements in the internal implementation. The 80286 microcode and internal logic is modified to allow most instructions to execute in fewer cycles than the 8086. It also enables a higher degree of pipelining. The philosophy of the 80286 is to decouple instruction execution as much as possible from external memory bus activity through instruction queues and bus output buffers. Although the 80286 offers built-in support for demand-paged virtual memory, the 4120 Series does not use this feature to maintain code compatibility with the 4110 Series.

In the 4110 Series, the CPU and memory occupy two boards. One board contains an 8086 processor, self-test EPROM, an 8087 math coprocessor, an interrupt controller, keyboard and host ports and interface logic to the system backplane bus. Graphics firmware and 32K of RAM stack space are resident on the second board. The 2732 EPROM chips provide storage for firmware up to a maximum of 128 Kbytes and stack RAM is implemented with 4116 dynamic RAM chips. As a result of the two-board packaging, the CPU is required to access memory over the system backplane bus. This bus is also shared with peripheral controllers and special-purpose graphics controllers resident on other boards. A block diagram of the 4110 Series architecture is shown in **Figure 1**.

In the 4110, the system bus is a bottleneck for two reasons: the bandwidth contention among bus controllers and data sharing. The Multibus-like system bus is controlled by an Intel 8288 bus controller and the 8289 arbitor and is totally asynchronous. Because of the handshaking protocol, a memory request cycle takes a minimum of 1.2 μsec to complete. If another bus controller has the bus, the 8086 can be held off during the other controller's activity. This is especially significant when the display controller needs the bus since it locks the bus for multiple memory cycles updating the display, keeping the 8086 from fetching instructions. Since all program instructions and stack memory are accessed over the system bus, the 8086 can become starved for instructions when bus contention is high.

The system bus is a problem, in terms of data sharing, because even to achieve a simple scheme for maintaining data integrity, the 8086 is not allowed to access critical areas of system RAM at the same time as the graphics coprocessor. As a result, the 8086 can be blocked for significant periods of time even when bus activity is low.

Using the 80286, the 80287 and some new memory parts, the two-board CPU/memory pair can be implemented on one board and can increase memory size and performance significantly (**Figure 2**). The 8288 and the 8289 parts were replaced with the 82288 and the 82289 parts to control the 4120 Series system bus. Intel's 2186 pseudostatic 8K × 8 RAM parts allowed the entire stack to be moved to the CPU card. The entire firmware space was also moved to the CPU card using 27256 EPROMs to increase memory density eightfold and to double the total size to 256 Kbytes.

To promote system throughput, an additional 82288 system bus controller is used to establish a private, local bus. This is used exclusively by the 80286 to access RAM, EPROM and I/O

devices on the CPU board, thus bypassing the system bus for instruction fetches and stack accesses, by far the most numerous processor requests. Because this is a synchronous bus, a memory fetch can be complete in only 500 nsec. Another special synchronous bus, called the RAM bus, was added to allow the 80286 on the CPU board to directly access the graphics display list memory on a separate memory board without having to use the system bus. The dual-ported display list memory is controlled by an 8207 memory controller that provides all bus control, dynamic refresh and address decoding required by 64K dynamic RAMs. Only bus buffers are required on the CPU board. The other port of the display list memory is used by the bipolar display list processor (graphics engine) to fetch the display list created by the 80286. This list is fetched, usually in blocks, via the system bus.

To insure the integrity of the display list data, software semaphores along with the 80286 "lock" instruction prefix are used to synchronize accesses from the 80286 and the graphics engine. The lock instruction causes a special signal from the 80286 to be asserted during a read, modify, write memory sequence. This signal is used to provide nondivisible access to a software semaphore that locks out the graphics engine at the other display memory port while the 80286 is updating the display list, preventing garbage data from appearing on the screen.

Communication between the 80286 and optional peripheral controllers takes place over the system bus, as in the 4110 Series. The new architecture and higher packaging density of the 4120 Series provide the extra space needed for the 3D graphics firmware enhancements while improving performance both through the inherent speed of the 80286 and the 80287 and through reduced bus contention.

Although the 80286 is designed to be code-compatible with

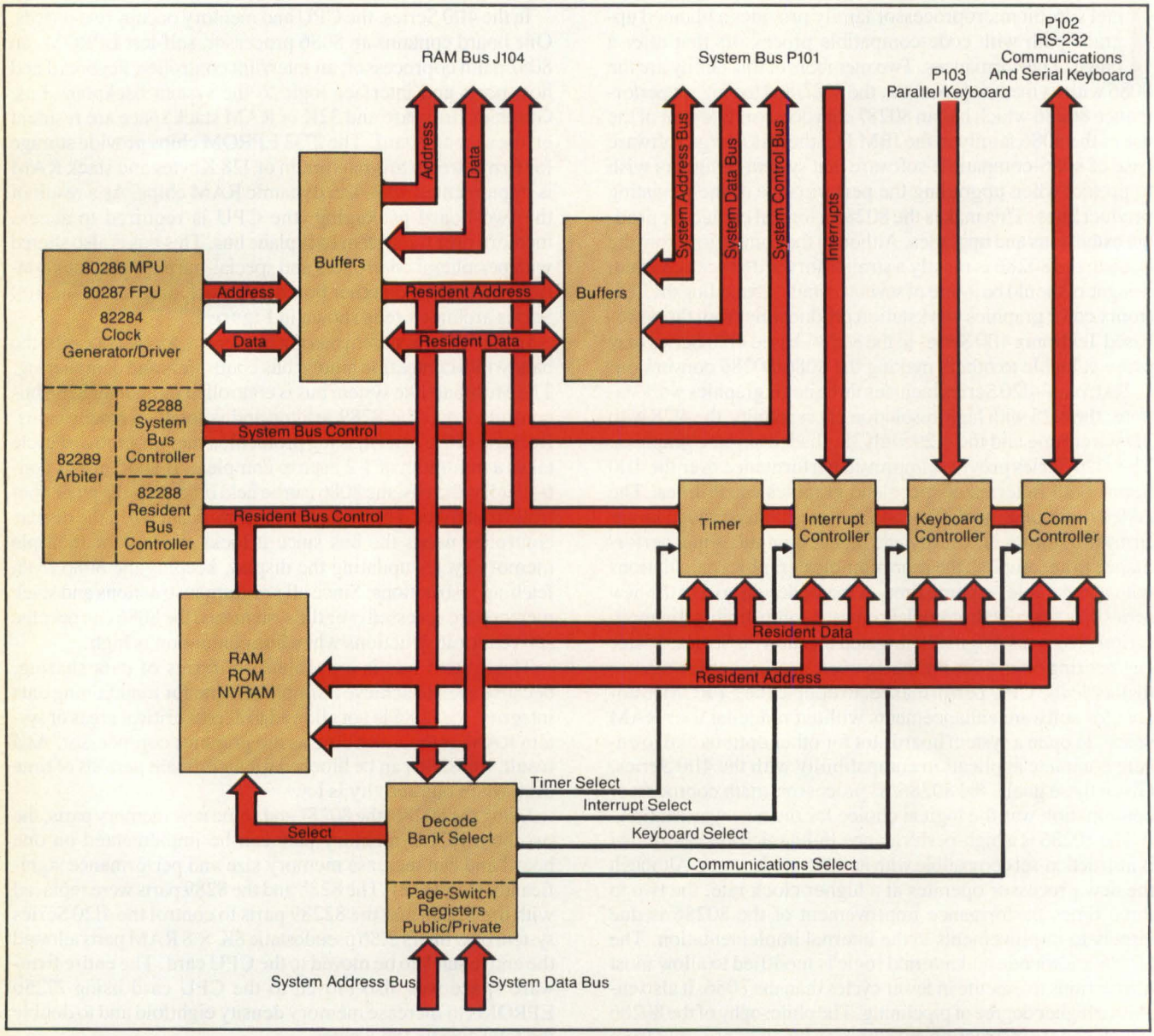
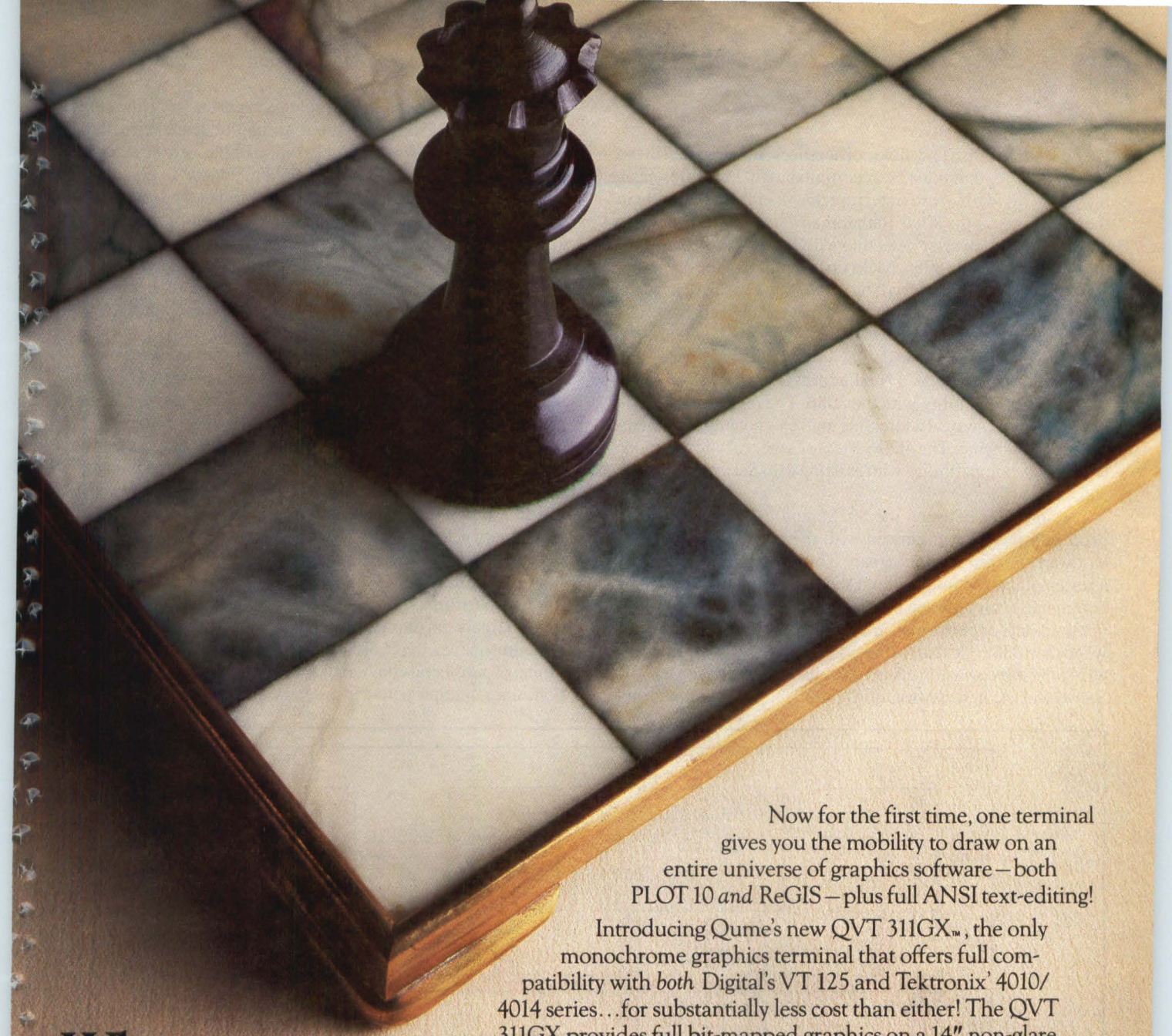


Figure 1: In the previous 4110 Series architecture, an 8086 accessed stack RAM and firmware over an external system bus shared with peripheral and graphics controllers. The asynchronous bus, implemented with the 8288 bus controller and the 8289 arbitor, required a minimum of 1.2 μsec to complete the required handshake for each bus transfer. In addition, other controllers could become the bus master, preventing the 8086 from fetching instructions for extended periods.



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the 8086, there are a few minor differences, documented in the Intel literature, that must be accommodated. The differences include a "divide-by-zero" interrupt that operates differently in the 80286 than in the 8086. Rather than generating an interrupt and continuing on after detecting a divide-by-zero condition, the 80286, unlike the 8086, backs up to the start of the offending instruction to enable a retry. The difference can result in an infinite loop if the software does not expect a subsequent execution of the division instruction.

Although the 80286 provides facilities for demand-paged virtual memory, it also has a "real address" mode that provides complete compatibility with the 8086. The real address mode has segmented physical addressing and does not impose a memory protect scheme. The 4120 Series uses the real address mode to maintain compatibility with existing 4110 Series application software.

The interface between the 80286 and the 80287 math coprocessor has been improved with the addition of two extra hardware synchronization signals. This allows the 80287 to take a series of instructions without the need to interpose FWAIT commands between each instruction as in the 8086. However, no functional or performance degradations have been detected when the 8086 code that includes the FWAIT is executed on the 80286/87. As a measure of code compatibility between the 4110 Series and the new workstations, application programs compiled with the old 8086/87 compiler also execute on the 80286/87-based 4120 Series.

Most of the compatibility problems experienced in the conversion to the 80286 were due to timing dependencies. The problems resulted from the integration of the new 80286 and its associated parts with older peripheral chips. To obtain the maximum performance, the 80286 was run at the full 6 MHz clock rate. At the same time, the peripheral chips used in the 4110 Series had to be retained to maintain application compatibility and these operate at 4.9 MHz with a separate clock. The two clocks did not present a problem as the parts are designed to be coupled asynchronously. However, each peripheral controller chip has its own inherent "recovery" time. Sending two successive commands to a peripheral chip in less than the allowed recovery time will result in erratic behavior. The time between commands is a function of the software code and the processor clock rate. Converting from the 8086 to the 80286 caused some peripheral recovery time to be violated in the prototype 4120 workstation; this violation was due to the increase in clock speed and more efficient bus transaction queuing in the 80286. Components affected included the Intel 8254 chip and the Signetics 2661 communications controller.

Recognizing the occurrence of a violation is not straightforward because the 80286 employs pipeline strategies to improve performance. This means that the instruction execution is largely decoupled from bus timing through internal instruction queues. It is not simple to determine what the output timing of peripheral commands actually is through code inspection, since multiple output instructions executed several instruc-

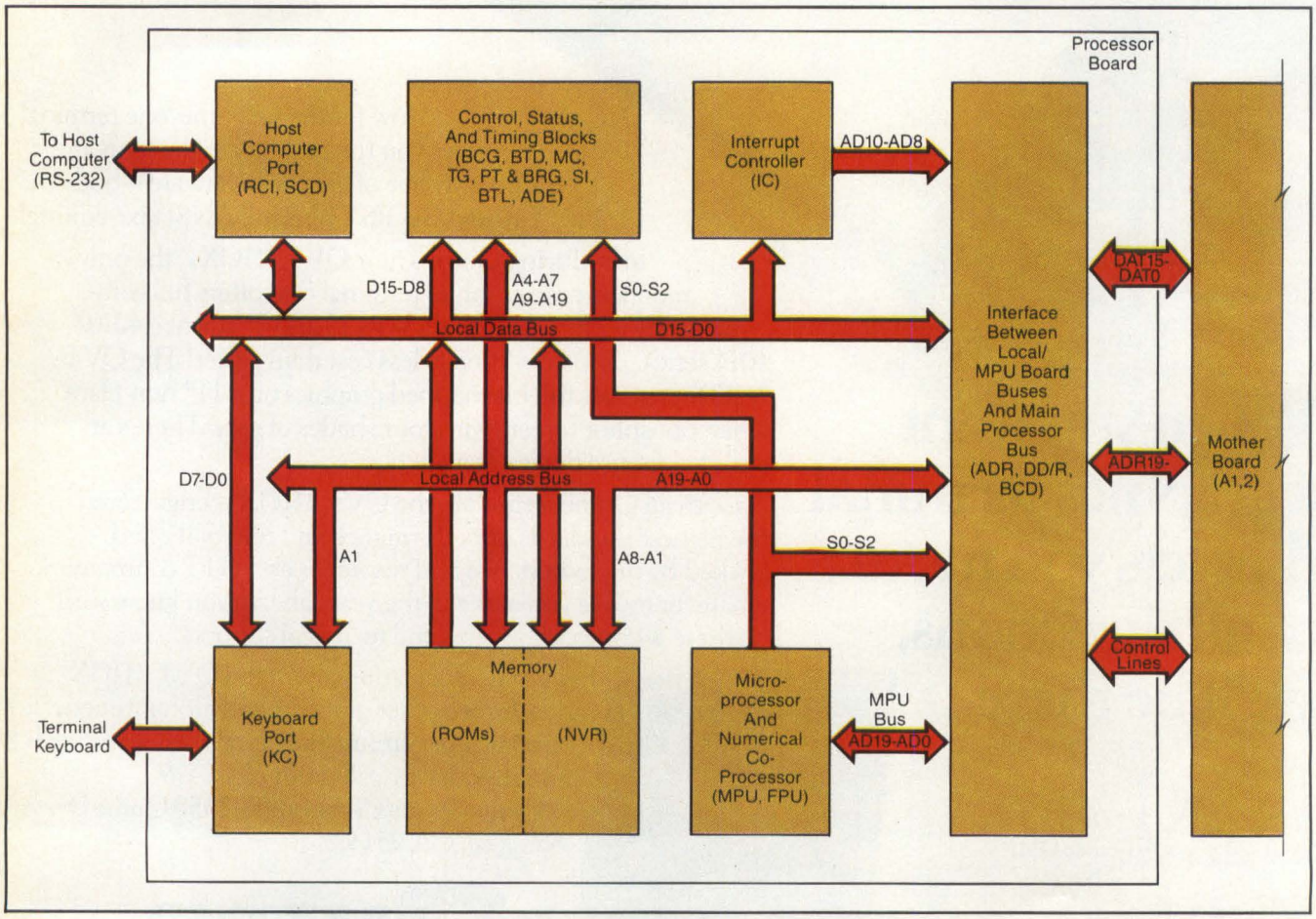

Figure 2: The new 4120 architecture brings all firmware and stack RAM onto the CPU board with the 80286 and the 80287. In addition, two private, synchronous buses were added to provide fast, unshared access to program memory, stack RAM and the graphics display list memory.

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tions apart could be queued up inside the processor to access the system bus in back-to-back requests. A simple and effective strategy to prevent violations of the peripheral timing is to follow an output instruction with a "jump to next instruction," which flushes the instruction queue, followed by the required number of "NOP" instructions to insure the minimum recovery delay. Another timing-related problem that proved difficult to detect because of its extremely intermittent nature involved the interrupt response of the 80286. Normally, if programmers want to change the interrupt mask status of an 8259A interrupt controller, they would disable the 80286 interrupt acknowledge, write to the controller and reenable interrupts. However, if there are active interrupt sources in the system when the 80286 modifies the interrupt masks, there is a finite (though very small) probability that an interrupt request will arrive after the 80286 disables interrupts but before the 8259A can respond to the new mask status. The result is a metastable state that produces a "glitch" on the 80286 interrupt input line. Under these conditions, the 8259A is not guaranteed to be stable until its "command response time" has expired, starting with the receipt of the mask command.

To insure reliable operation when there are active interrupt sources, programmers should follow this sequence when sending commands, such as interrupt mask updates, to the 8259A interrupt controller chip: 1) disable the interrupt acknowledge on the 80286, 2) write the mask to the 8259A, 3) execute a "jump to next instruction" to flush the 80286 instruction queue, followed by NOPS to establish a minimum delay equal to the controller response time (350 nsec for the 8259A) and 4) reenable interrupts on the 80286. Failure to follow this procedure allows the metastable state to affect the 80286 and cause system crashes at very infrequent, yet unacceptable intervals.

The final area of concern for any engineering team converting the 8086 to the 80286 is self-test code. Although many self-tests can, and should, be made timing independent, the very nature of seft-testing makes this impossible in some cases. To accomplish a thorough fault isolation, self-test code must get very close to the hardware, and this is when timing dependencies creep in. For example, self-test code that exercises the 4110 graphics coprocessor board exhibited timing problems when executed on the 80286. During normal operation, the graphics engine fetches display list primitives under its own control and at its own rate. However, during self-test the main CPU "spoon feeds" the graphics engine one command at a time to verify basic command execution before the engine is allowed to fetch its own commands from the display list. This primitive operation gives needed feedback to service personnel about where a failure is located. The increased speed of the 80286 over the 8086 resulted in commands being sent to the graphics engine faster than it could respond, leading to false self-test failures. Code delays were employed to eliminate the problem. Any 8086 to 80286 conversion project should expect a few of these timing-related incompatibilities to surface in the self-test code. DD

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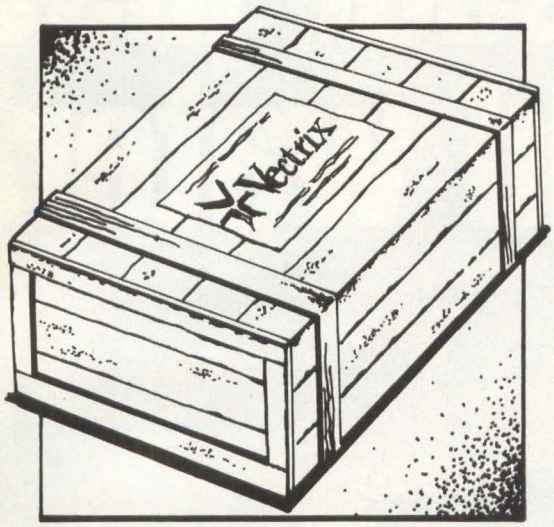

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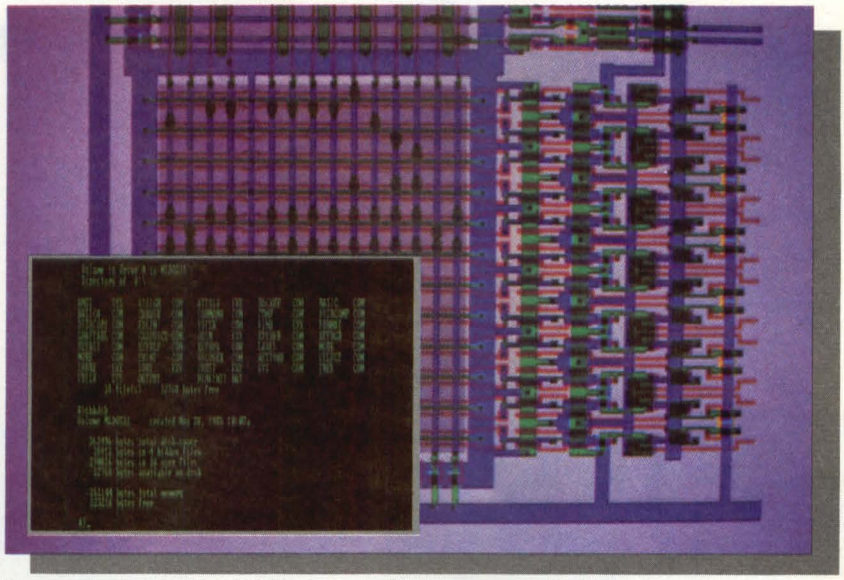

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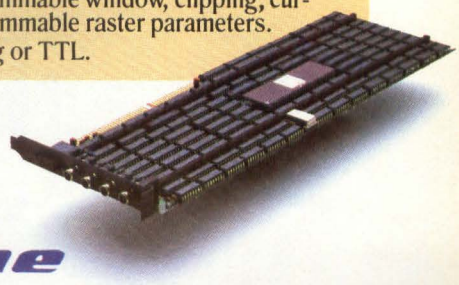

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The Future Of Flexible Disks

by Bob Hirshon, Contributing Editor

Flexible disk technology has not exactly set the world on fire over the past decade and a half. While other mass storage technologies have improved dramatically, floppy drives have made comparatively modest gains. Micro-Winchester disk drives, for example, increased in capacity from about 5 Mbytes in 1980 to over 100 Mbytes today. During the same period, floppy drives went from 400 Kbytes to 1.6 Mbytes – a far less impressive, fourfold improvement over five years. Performance improvements have been even smaller.

The flexible disk drive technology appears to lag far behind other memory technologies because of several factors, including cost, media removability and compatibility. Floppies, unlike Winchesters, are a removable, it is hoped, interchangeable, medium. Being removable, the diskettes are subject to extreme environmental stress during transport. Reliable reading of data under such conditions necessitates keeping recording parameters conservative.

In addition, interchangeability of media between drives from different manufacturers means standards must be set – a time-consuming and technology-stifling process. The process may be a matter of various manufacturers methodically ironing out

Bob Hirshon is Contributing Editor, Peripherals, for Digital Design *and a Boston-area writer specializing in science and technology.*

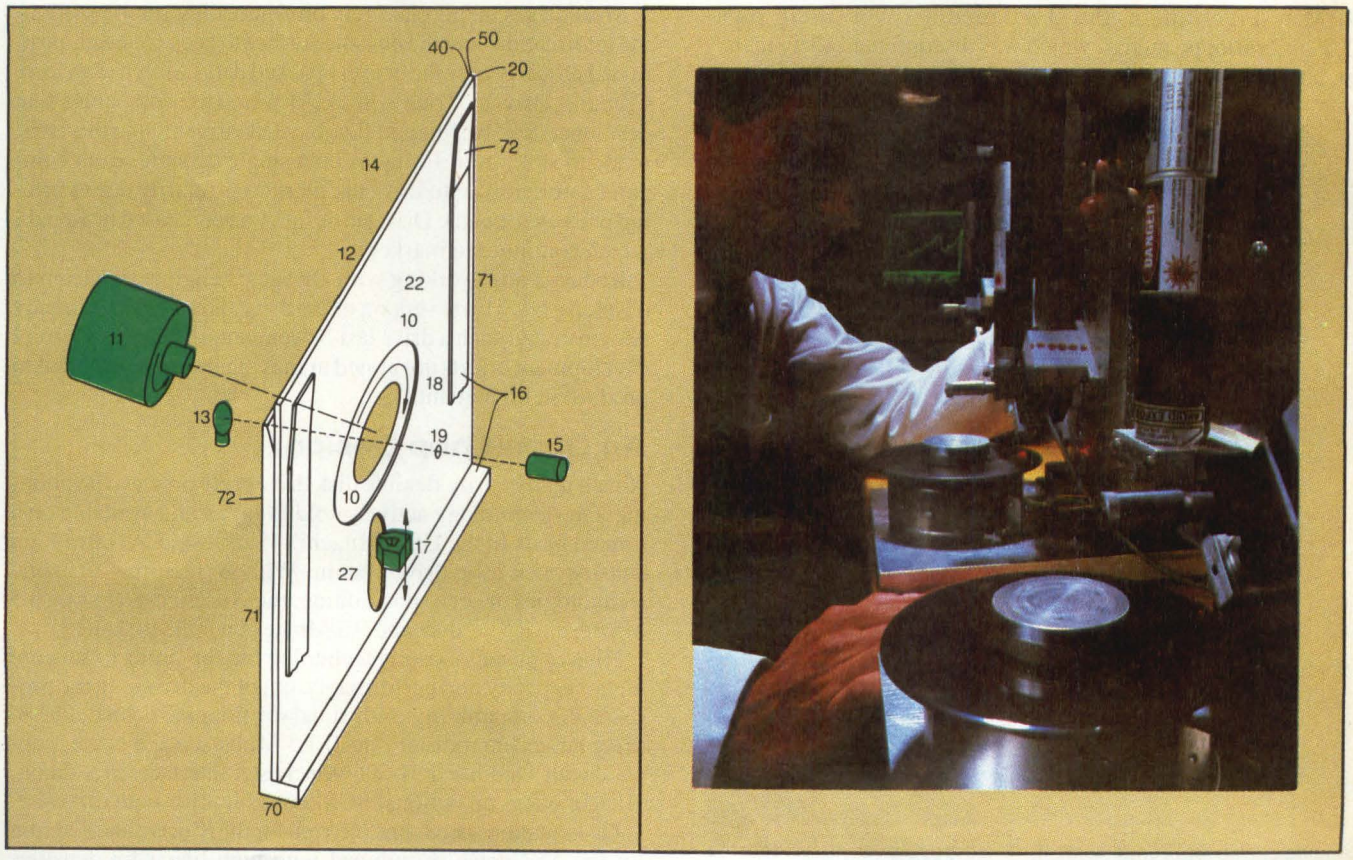

Figure 1: IBM's 1969 patent (left) for this early prototype floppy disk was one of the first applications for flexible disk media. One of the latest is 3M's stretched surface recording (SSR) consisting of flexible disk media stretched over a rigid plastic substance. Here (right) it is being examined for surface defects with a laser testing device.

specifications or it may be a case of IBM choosing a specification and the rest of the manufacturers following suit. But either way, once a standard is set, considerable inertia must be overcome before another can replace it. And the more established a standard becomes and the more software is available on that format, the more difficult it becomes to introduce a new format.

Cost is another key factor. Flexible disk drives compete in the intensely price-sensitive small computer market. This puts high-volume, low-cost production at a premium and makes performance advantages less important. So efficient has floppy drive production become that lower volume, advanced technology drives cannot compete. When 1.6-Mbyte drives sell for about $100, OEMs are not willing to spend $200 for a 3-Mbyte drive. As a result, high performance flexible disk drives have a very limited market.

Together, these factors keep the mainstream of the flexible disk industry far from the leading edge. Nonetheless, there are active efforts ongoing in the US and especially in Japan to extend the limits of flexible disk technology. Although many are limited to the laboratory or niche applications now, these technologies demonstrate the capabilities of this versatile media and indicate what we can expect from the technology in the 1990s.

Microfloppies Finally Emerge

One technology that has emerged from the laboratory to join the mainstream is the sub-4″ microfloppy. It took four years of infighting over several different media formats before the industry finally settled on a modified version of the Sony 3½″ format. IBM's selection of the 3½″ media (over their own 3.9″-microfloppy media, which was discontinued early in the standards battle) for their portable JX computers in Japan, and for another system reportedly being introduced in the US this summer, has ended the controversy for good. With Apple, Hewlett-Packard and now IBM all using the 3½″ microfloppies, lack of software – an early difficulty with the media – will cease to be a problem.

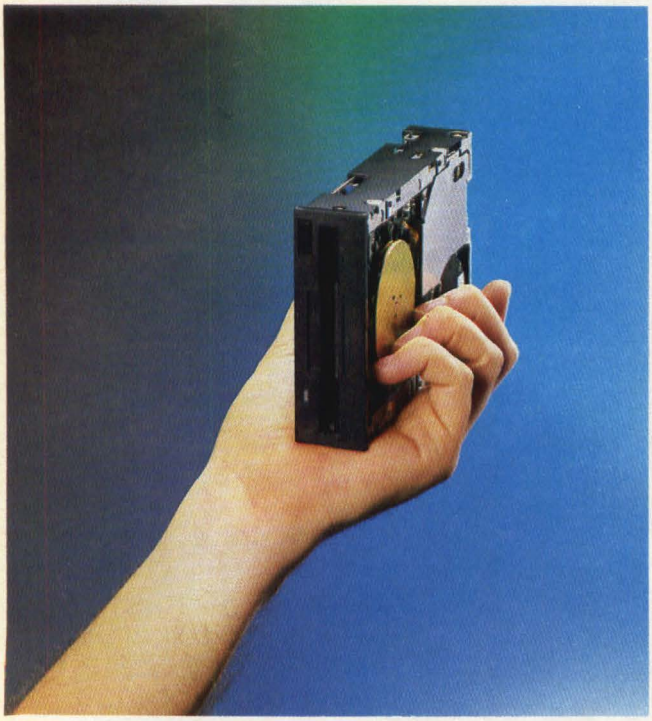

Figure 2: With IBM's endorsement, microfloppy disk drives will become increasingly popular. By 1987, the drives are expected to represent nearly one-third of all flexible disk drives shipped annually, according to Disk/Trend. (Photo courtesy Canon USA)

Microfloppies have a number of technical advantages over larger flexible disk drives, including lower power consumption, higher reliability and smaller footprint. The hard shell media offers added durability, more precise clamping (because of the addition of a metal hub) and higher resistance to anisotropic deformation and expansion from thermal and hygroscopic effects.

Current versions of microfloppy drives record at 135 tracks per inch (tpi) and about 7500 bits per inch (bpi) for a capacity of 500 Kbytes per surface. Double-sided drives storing 1 Mbyte are now available in quantity and are used in IBM's JX computer. The next stage in microfloppy development is a 1.6-Mbyte double-sided drive. Sony demonstrated such a drive two years ago, using high-coercivity media and custom-designed heads to increase bit density from 7610 bpi to 13,340 bpi. Setting standards for the 1.6-Mbyte microfloppy is the next step. Nippon Telephone and Telegraph (NTT) is currently working with several Japanese manufacturers to facilitate a 1.6-Mbyte microfloppy standard.

Servo-Positioned Floppies

A number of companies have been working toward a high-capacity, high-performance flexible disk drive. Media for these drives look like conventional floppy disks, but may have special, high-coercivity surfaces. This allows the smaller, more tightly packed bit cells to resist demagnetization and provide a sufficiently high-amplitude signal.

Most drives in this class rely on embedding servo positioning information onto the diskette surface to keep the heads positioned properly over the densely packed data. Amlyn (San Jose, CA) and Drivetec (San Jose, CA) were two companies that developed 5¼″ half-height flexible disk drives using this technique to store over 3 Mbytes on a single diskette. Both companies were forced to leave the market, primarily due to pricing pressures, but the Drivetec design was purchased by Kodak, which continues to market it.

Kodak is now working with Drivetec's engineering team to develop a 6.6-Mbyte version of the drive. Drivetec had already demonstrated such a drive last November at Comdex. Current development efforts are aimed at making the drive efficient to produce in high quantities.

An Open-Loop Design

Not all high density flexible disk drives rely on servo positioning. One technology actively sold in Japan and available on a limited basis in the US is Hitachi's (San Jose, CA) ultra-high density open-loop drive system. Without resorting to exotic technologies or servo positioning, the Hitachi drives store 6.5 Mbytes on a 5¼″ disk and 9.6 Mbytes on an 8″ diskette.

Hitachi pushes existing technology to the limits to squeeze higher capacity and performance out of the drives. In the process, all compatibility with standard floppies is lost. The 8″ drive has a data transfer rate of 1.5 Mbits/sec and comes supplied with a modified ST-506 Winchester interface. In addition, Hitachi offers an optional SCSI controller for both drives.

Disk rotation speeds are 360 rpm for the 8″ drive and 720 rpm for the 5¼″ drive. Combined with high linear bit densities (20,560 bpi for the 8″ drive and 29,560 bpi for the 5¼″ drive), this accounts for the high transfer rates. Track density is kept

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to a relatively conservative 96 tpi for the 8" drive and 125 tpi for the 5¼" drive. Thus it is the extremely high linear densities that result in the drives' large capacities.

To achieve these high bit densities, Hitachi incorporated narrow-gap manganese zinc ferrite heads, rather than conventional nickel zinc ferrite heads, to produce a stronger signal in a smaller bit cell. Maxell developed a high density media for use with the heads. Although coercivity, at 650 oersteds, is no higher than other high coercivity media, the Maxell disks have a thinner, smoother coating and have much lower anisotropy from thermal expansion. The thinner, smoother coating allows higher density recording, and the resistance to anisotropic effects allows accurate positioning of the heads over the densely packed data.

Although both drives have been shipped in quantity in Japan, Hitachi has not actively marketed them in the US. However, the company has provided samples to a number of US firms.

Vertical Recording

Vertical, or perpendicular, recording has numerous advantages over conventional, or longitudinal, recording. But the many logical advantages of the technology have thus far been unable to outweigh an equal number of practical disadvantages.

Vertical recording orients bit cells down into the disk surface, rather than orienting them end-to-end. Not only do the cells take up far less space when oriented in this manner, allowing more bits per inch, but they also respond favorably as bit density increases.

Longitudinally recorded bit cells deform and demagnetize each other as they are squeezed more tightly, since like-charged ends of bit cells are adjacent. Vertically recorded bit cells, however, have opposite-charged ends of cells adjacent to one another. These tend to attract each other and resist deformation and demagnetization.

Another advantage of perpendicular recording is the elimination of the need for increasingly thin media coatings. With longitudinal recording, smaller bit cells require thinner coatings to maintain optimal bit cell dimensions. This means the bit density of longitudinal recording is limited by how thinly diskette surfaces can be evenly coated. In addition, as diskette coatings become thinner, the signal amplitude of each bit cell decreases, making reading of the data more difficult and requiring higher coercivity media.

Vertical recording avoids these problems. Since the bit cell orientation is down into the disk, optimal bit cell dimensions are maintained without making the coating thinner. In fact, since longer bit cells are actually more desirable, thick film coating is preferable. Thus vertical recording allows high bit density with good recording characteristics that actually improve as density increases.

The advantages of vertical recording have been well-known for many years and have inspired numerous research efforts. To date, none have brought a product to market. The main difficulty is the media. The two preferred materials for perpendicular recording are cobalt chromium and barium ferrite, and each has its problems. Cobalt chromium must be sputtered onto the diskette, an expensive and time-consuming means of producing floppies. The diskette then requires some sort of lubricant or overcoat to reduce wear.

Barium ferrite does not require sputtering, but consistency has been a problem. Proper uniformity of the particles and the binder mix is especially crucial, and the material must be carefully oriented to achieve good recording characteristics.

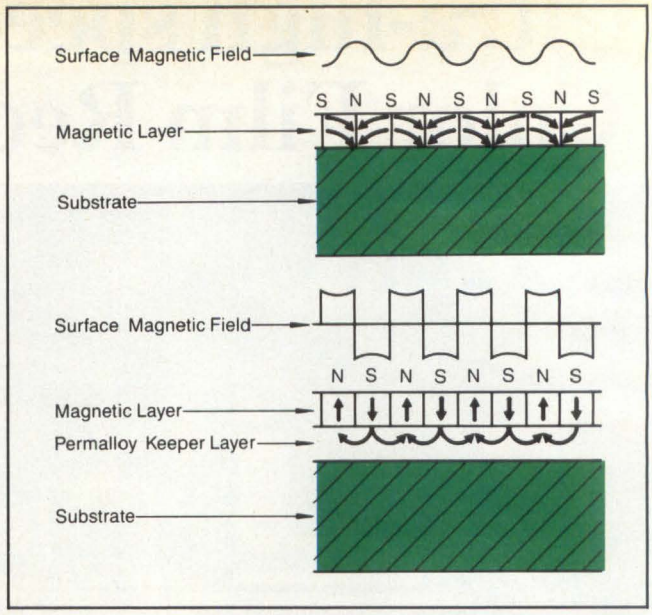

Figure 3: Conventional, longitudinal recording orients bit cells end-to-end along the length of the data track. Vertical, or perpendicular recording, orients the bit cells side-by-side down into the surface of the recording media.

Most importantly, the drives as well as the media must meet the pricing constraints of the floppy disk market. So far, the combination of technical difficulties and market concerns have prevented the introduction of a vertical recording flexible disk drive. Nontheless, Japan-based manufacturers are still actively pursuing the technology, and some have announced plans to have a product available within a year. US efforts in flexible disk vertical recording have been reduced to comparatively small groups at the larger media and drive companies.

The one company dedicated exclusively to the technology, Vertimag (Minneapolis, MN), recently was forced to lay off most of its workforce, and is now down to only 12 full-time employees. "After January, the plug was pulled by our investors," explains Nathan Curland, vice president of engineering and acting CEO for Vertimag. "We couldn't raise enough funds by private funding, so now we're trying to sell the company." Despite Vertimag's problems, Curland remains optimistic about the future of vertical recording. "Technology will march on, densities will get higher," predicts Curland, "and eventually the market will require perpendicular recording. The only question is when."

Noncontact Recording Methods

Some technologies combine elements of flexible disk recording and Winchester technology. Bernoulli drives, for example, use flexible disk media encased in a removable cartridge. As in Winchester drives, the disks spin at high speeds, and the R/W head comes close to the surface, but never actually touches it.

Bernoulli technology takes advantage of the stabilizing action of a stationary plate just underneath a spinning disk. Rather than fluttering uncontrollably, the flexible media spins smoothly over the plate, at a distance precisely determined by the speed of rotation and the physical design of both plate and media.

This media stability allows R/W heads to be 10 μin from the media. This is close enough to allow linear bit densities of up

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to 20 Kbits/in while avoiding head and media wear problems associated with conventional contact flexible disk recording.

IBM invented Bernoulli technology, but never incorporated it into a product. Iomega (Ogden, UT) developed the technology, and designed a line of 5¼" and 8" format drives around it. In addition to providing up to 10 Mbytes of removable storage on a single cartridge, the drives operate well in harsh environments and are resistant to airborne contaminants. This makes them popular for use in industrial, laboratory and military environments. Miltope (Melville, NY) makes a mil-spec version of the drive.

Ironically, Iomega's latest product is a 20-Mbyte, IBM-compatible subsystem, designed to let IBM PC/AT buyers circumvent IBM's well-publicized 20-Mbyte Winchester disk drive problems. Iomega offers free upgrade software to PC/AT buyers who purchase a stripped down, no-Winchester version of the AT, and the upgrade to a Bernoulli drive.

Stretching The Limits

Another technology that combines qualities of flexible and Winchester disk drive recording is Stretched Surface Recording (SSR). Developed by 3M (St. Paul, MN), it involves stretching flexible diskette material over a rigid circular disk between two low rims bounding the inner and outer circumference of the recording area. Stretched over the two rims, the media is taut but slightly resilient, like a drum or banjo head.

As in Bernoulli drives, the media spins rapidly, and the heads stay in close proximity to the surface, without actually touching it. Also as in Bernoulli drives, aerodynamic effects maintain the head-to-disk spacing. But in SSR, it is the dimpling effect on the surface of the disk, caused by air passing between head and disk, that creates the spacing. This space can be as small as 5 μin – half that of Bernoulli drives. Consequently, 3M engineers predict even higher capacities for their SSR disks – up to 50 Mbytes for a 5¼" disk.

3M recently ramped up production of SSR disks at its Wetherford, OK manufacturing facility. It expects the first drives using SSR to be fixed media drives and predicts they will be introduced this year, possibly at NCC. In the near future drives using removable SSR cartridges will be developed. These, 3M claims, will compete with removable Winchester cartridge drives, Iomega's Bernoulli drives and other high density floppy technologies.

Flexible Variations

Other new flexible disk developments range from slight variations on a theme to whole new applications for the media. Omek (Fremont, CA) is a small company trying to distinguish its product from a largely indistinguishable field. Its 5¼" half-height floppy drives have a unique self-testing and exercising feature that may be particularly attractive to customers who do not have their own drive test equipment. By applying jumpers to various positions on the drives' option select pins, customers can run the drives through a variety of different self-tests, the results of which are displayed by means of flashing red and green LEDs.

Another form of self-test is incorporated by Hewlett-Packard (Greely, CO) in their microfloppy drives. Their "media monitor" keeps track of disk insertions on a dedicated area of the disk and lets the user know when the disk has probably outlived its usefulness.

Unit shipments in thousands	1983 Shipments	Forecast 1984	1985	1986	1987
8 inch drives					
One side	336.4	227.9	129.7	68.7	30.9
Two sides	1,275.9	1,285.4	1,082.5	832.8	493.7
8 INCH TOTAL	1,612.3	1,513.3	1,212.2	901.5	524.6
5.25 inch drives					
One side	4,323.7	4,520.9	4,531.1	4,253.4	3,678.7
Two sides	6,165.7	10,126.5	13,412.3	15,891.8	17,681.4
5.25 INCH TOTAL	10,489.4	14,647.4	17,943.4	20,145.2	21,360.1
Microfloppy drives	438.3	1,959.0	4,168.2	6,674.5	9,711.2
TOTAL ALL DRIVES	12,540.0	18,119.7	23,313.8	27,721.2	31,595.9

Figure 4: Disk/Trend predicts rapid growth for flexible disk drives in all categories except 8" drives.

Conventional flexible disk technology is increasingly finding its way into unconventional applications. Ensoniq (Malvern, PA), for example, uses microfloppy disk drives in its Mirage Digital Sampling Keyboard, a five-octave electronic synthesizer capable of reproducing sounds stored on diskettes. Chyron (Melville, NY) uses microfloppies in its digital character generators, which create and store alphanumerics for use in videotape production. And Compusonics (Denver, CO) has patented a digital floppy-disk-based audio system that stores up to an hour of music on a 5¼" diskette.

Market Matters

Despite the many new technologies being investigated in laboratories, no one could accuse the flexible disk drive industry of being technology driven. The successful companies have not been those who introduced the latest technologies first (in fact, most of those who did are now out of business), but those who produced the greatest number of drives at the lowest cost.

The result is that virtually all flexible disk drive production is now done overseas. Even Tandon (Chatsworth, CA), the last surviving high-volume, US-based floppy drive manufacturer, produces its drives in Singapore and India. And in every category of flexible disk drives currently undergoing growth (that is, all categories excluding 8" drives), manufacturers not based in US now dominate, according to Disk/Trend (San Jose, CA). These manufacturers now account for 66% of all single-sided 5¼" drives, 54% of all double-sided drives and 97% of all microfloppy drives. In the long-term, flexible disk drive technology has substantial room for innovation. However, in the near future, market concerns will continue to dominate the industry, and improvements will be measured in dollars and cents (and yen), rather than in Mbytes and msecs. DD

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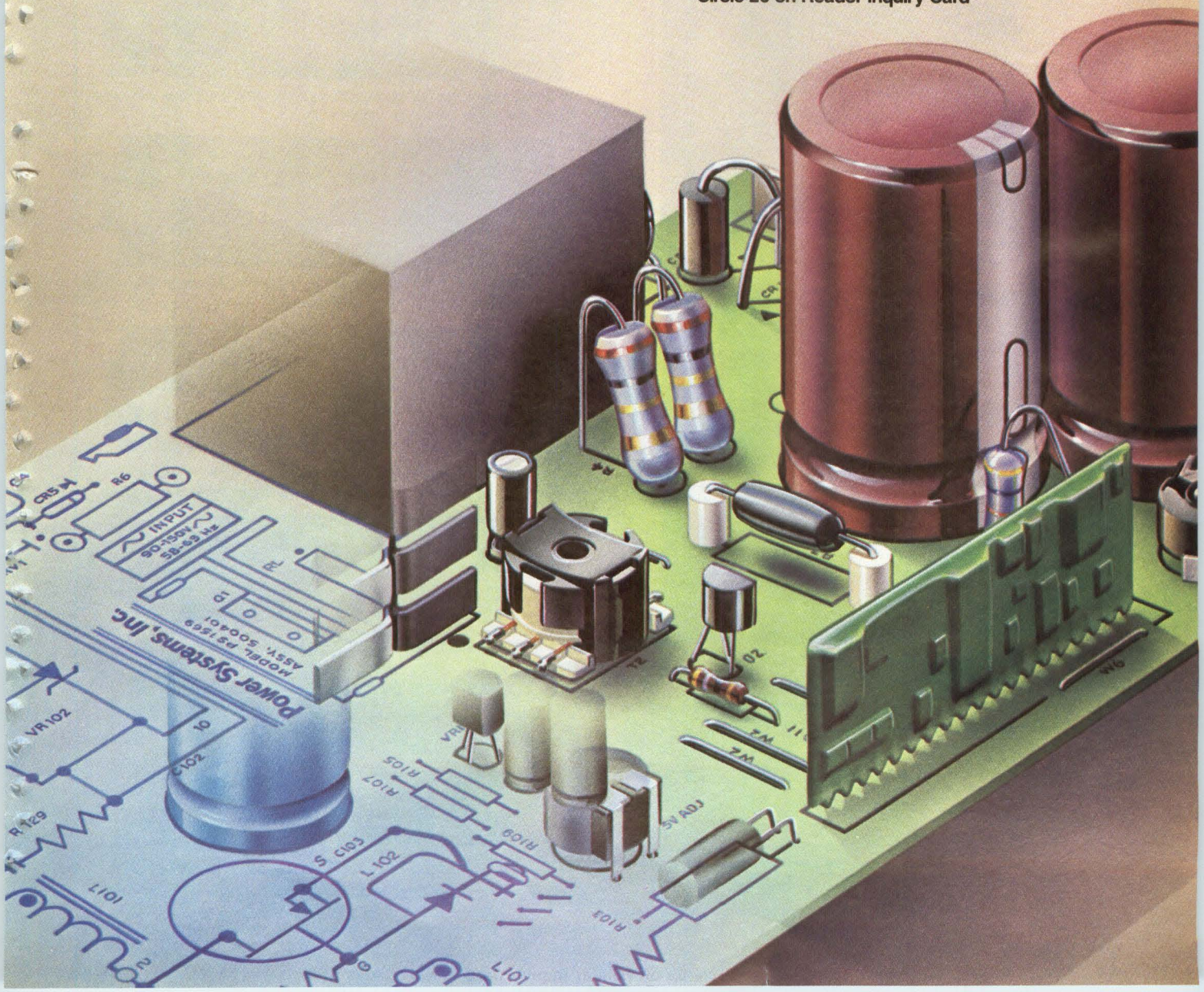

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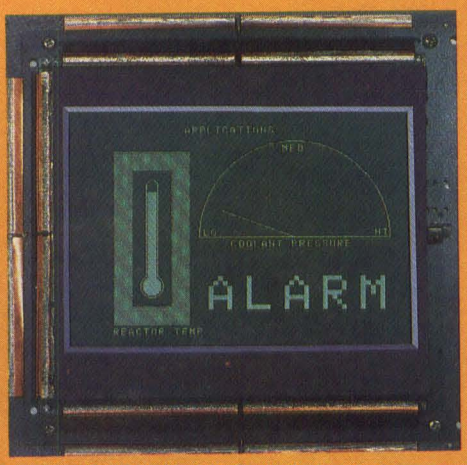

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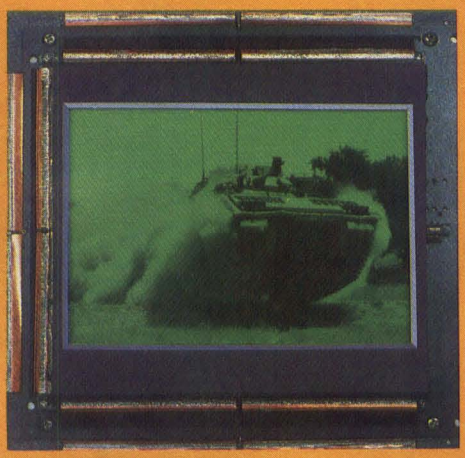

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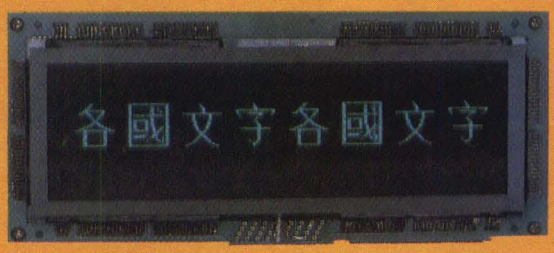

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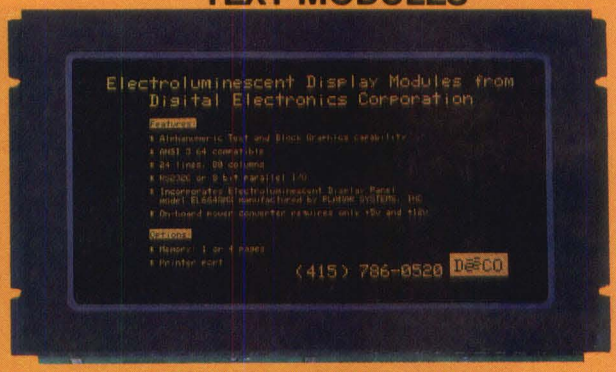

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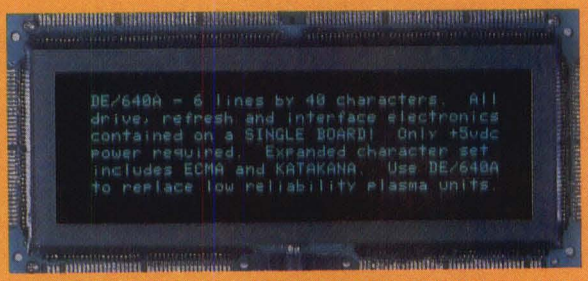

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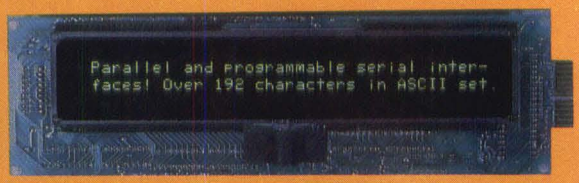

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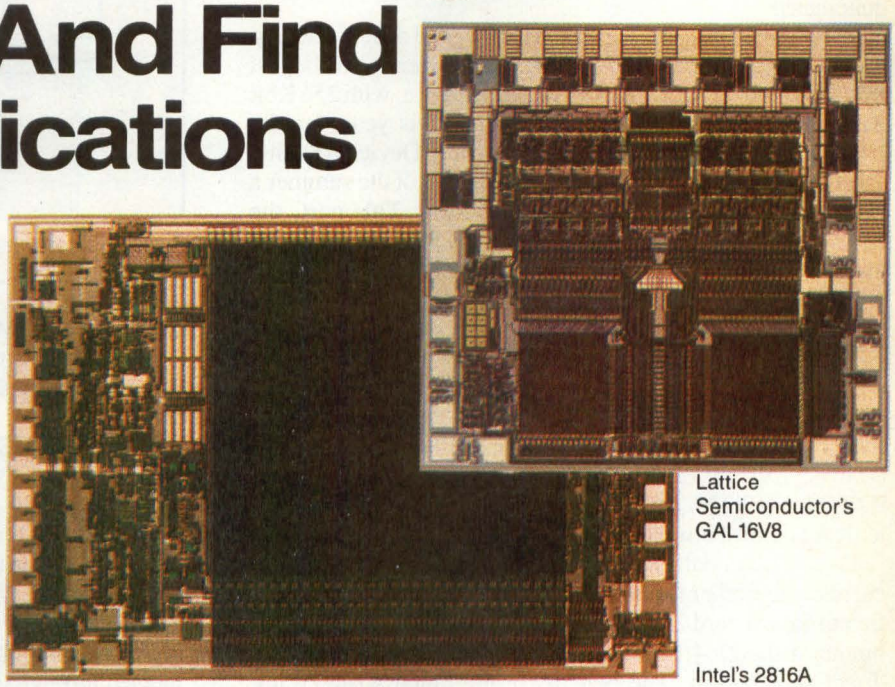

Lattice Semiconductor's GAL16V8

Intel's 2816A

by Dave Wilson, Executive Editor

During the 1970s, the EEPROM market was built exclusively around MNOS technology. The key companies were NCR and General Instrument, and the highest density device available was only 8 Kbits. The major uses were in consumer electronics such as tuners, in point-of-sales equipment to store prices or tax tables, in postage meters to store postal rates and in other look-up tables with a variety of applications.

In the early 1980s, the first parts using floating gate technology began to emerge from Intel and Xicor. In 1982, Seeq Technology began its first product shipments. Along the way, Advanced Micro Devices, Hughes, Motorola, National Semiconductor, Siemens and others independently developed their own EEPROM capabilities. One early idea regarding the position of the EEPROMs in the marketplace was that they would become a replacement for the UVEPROMs. The ability to reprogram the parts without having to remove them from a board brought obvious benefits to the designer. To date, however, the EPROM market has been relatively untouched by the EEPROM technology. This is primarily because of the radical difference in product cost between the two devices produced with the same design rules.

In introducing its new 64 Kbit EEPROMs, Hitachi (San Jose, CA) claims to have effectively solved the price problem. By using MNOS technology, Hitachi has built its devices (the HN58064P-25 and the P-30) with single-capacitor memory cells, as opposed to the three capacitor cells found in most of its competitors' devices designed with floating gate technology. Also, Hitachi has resisted the current trend toward putting a greater level of functionality on a single device. By moving some advanced features off the chip, Hitachi claims to have reduced the cost of the EEPROMs and made them available as a commodity product. Seeq Technology (San Jose, CA) offered EEPROM technology on-board its microcontroller (the 72710) as an alternative to the on-board UVEPROM. The part was unsuccessful because of the designers' unfamiliarity with the Texas Instruments instruction set and Seeq's delay in shipping the part. The EEPROM is, however, finding its way into many newer microcontrollers as a substitute for UVEPROM.

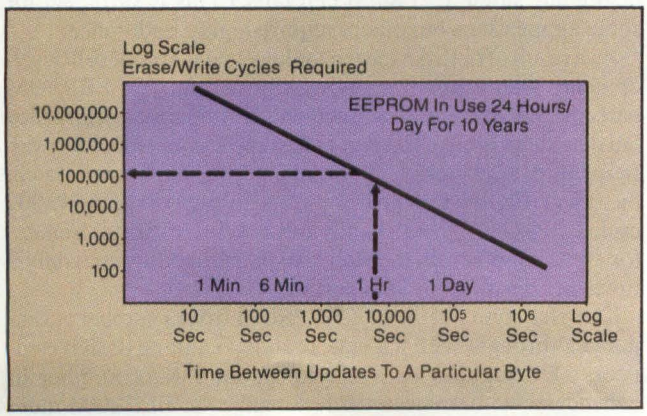

Figure 1: Required EEPROM endurance vs. time between writes.

Another application for the technology, that of EEPROMs replacing fuses in programmable array logic devices, appears to be gaining momentum. Already, Lattice Semiconductor (Portland, OR) has announced two families of reprogrammable array logic devices. These are the Lattice Reconfigurable Array Logic (RAL) device and the Generic Array Logic (GAL) device. Both combine a CMOS process with EEPROM floating gate technology. According to Lattice, this provides designers with reconfigurable logic featuring bipolar speeds (25 nsec) at significantly reduced power levels. The GAL16V8 device is a pin-for-pin replacement for any of the standard 20-pin bipolar PAL devices and can also be configured into architectures that do not exist. Each output of the GAL can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. All circuit elements in the unit come fully tested. They are erased

prior to shipment to assure a 100% programming yield. Test vectors to verify each logic pattern do not have to be generated during production testing because the programming yield is guaranteed.

In terms of density, the EEPROM has a good deal of catching up to do before it rivals the UVEPROM. Currently, the largest EE part available is the 8K × 8 (64 Kbit) device, with 256 Kbit parts promised by some suppliers later this year. On the UVEPROM side, however, Advanced Micro Devices (Sunnyvale, CA) expects to have available by the end of the summer a UV part of no less than 1 Mbit in density. This part, the AM27C1024, a 1-Mbit CMOS product, is a 5V device that features a power dissipation of 250 mW when active and 500 mW when in standby mode.

Other technologies are also continuing to challenge the EEPROM. These include the static RAM with battery backup and the shadow RAM. Two years ago Mostek (Carrolton, TX) began offering a CMOS static RAM with a built-in ten-year battery. Since then, others have jumped in. Dallas Semiconductor (Dallas, TX), for example, now offers a 64-Kbit nonvolatile RAM, the DS1225. An on-board lithium power supply and intelligent control circuitry retain data in the absence of V_{CC}.

These CMOS static RAM parts will fit into many systems that currently use other forms of nonvolatile memory because they fit into the standard 28-pin JEDEC format. They also match the pinout of the 2764 EPROM or the 2864 EEPROM to allow direct substitution. The benefits of unlimited write cycles, safeguards against corrupted data and fast read and write times (as low as 150 nsec) provide for an alternative to EEPROMs, EPROMs or shadow RAMs in some applications.

The distinction between the NVRAM and the EEPROM is that normal reading and writing occurs between the processor and the SRAM portion of the NVRAM. Writing into the EEPROM occurs only when data is to be saved, such as during a power failure. NVRAMs allow for unlimited writes and a quick store of the whole array since each system bit has a

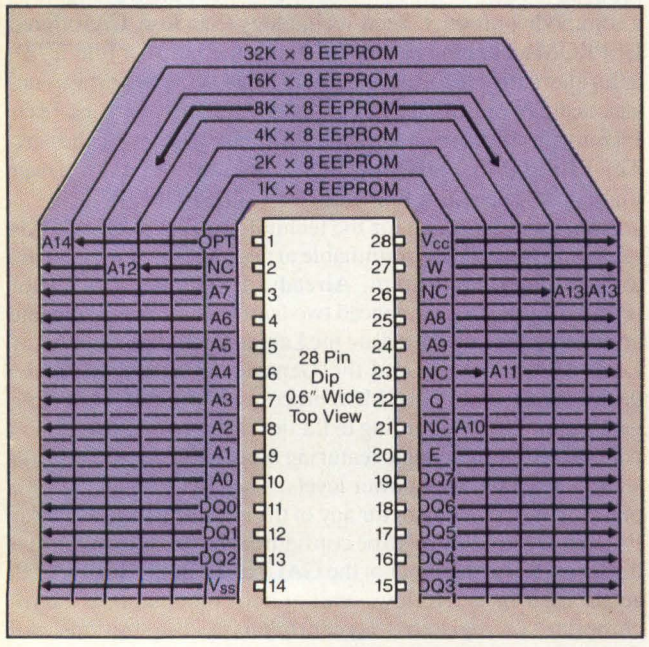

Figure 2: Evolution of the EEPROM in a 28-pin DIP.

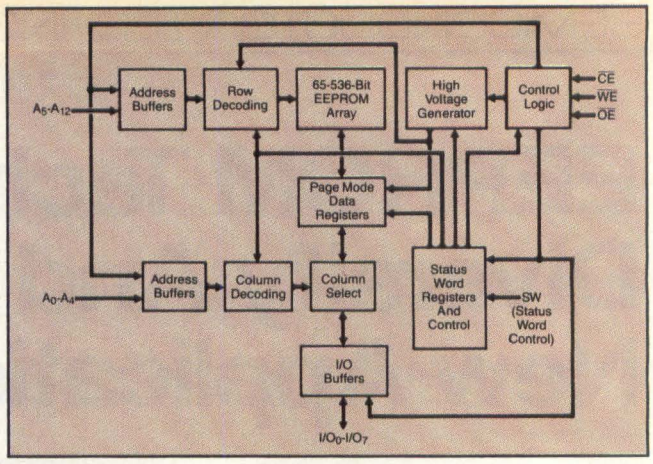

Figure 3: Block diagram of the Exel XL-48C64.

shadow EEPROM bit. At present, however, NVRAMs are not available in densities higher than 4K, and the bulk of products shipped by manufacturers still appears to be at or below the 1K level.

In the past, EEPROM access times have been around 150 nsec, and the only available nonvolatile memory with access times below 150 nsec has been the bipolar PROM. Bipolar parts, however, can only be programmed once and consume more power than their MOS counterparts. Today, it would appear that the EEPROM is catching up, in terms of access times, to the point where it may challenge the bipolar parts. Formerly, high speed alterable nonvolatile memory systems were implemented through the use of a combination of slow EEPROMs and high-speed static RAMs. Upon power up, the system would download the EEPROM content into static RAM for fast access. Recently, however, two high-speed CMOS EEPROMs, the XL46C16 (2K × 8) and the XL46C32 (4K × 8), have broken the 100 nsec barrier and offer access times of 55 nsec. With the advent of these parts from Exel (San Jose, CA), many high-speed system designers will be able to consolidate their memory architectures by replacing their redundant combinations with the new parts. Typical applications include adaptive robotics, high-speed process controllers and programmable video pattern generators. But it is not only the access time where developments in technology continue to enhance the performance of the EEPROM.

Another area of research is focusing on the increased endurance of the parts. At present, the industry standard endurance is 10,000 cycles. (Endurance is defined as the maximum number of erase/write cycles that the entire memory can withstand before any single EEPROM cell fails.) This is sufficient for some applications but others require higher endurance.

As a result of both device technology and memory cell development, Seeq Technology now offers a family of EEPROM parts that can be reprogrammed one million times before they fail data sheet limits. The part is designed for applications with frequent data alteration (i.e., data storage portion of system memory). **Figure 1** compares the one million cycle and 10,000 cycle EEPROMs. Seeq's family can be written every 6 minutes for 10 years, whereas the standard part can be written only 3 times per day for the same period.

The availability of the 64K EEPROM from a number of vendors has brought with it a new awareness among design engineers. Throughout its evolution from 16K, a number of enhancements have been made to make the EEPROM more useful to the designer. Several features are found on a variety

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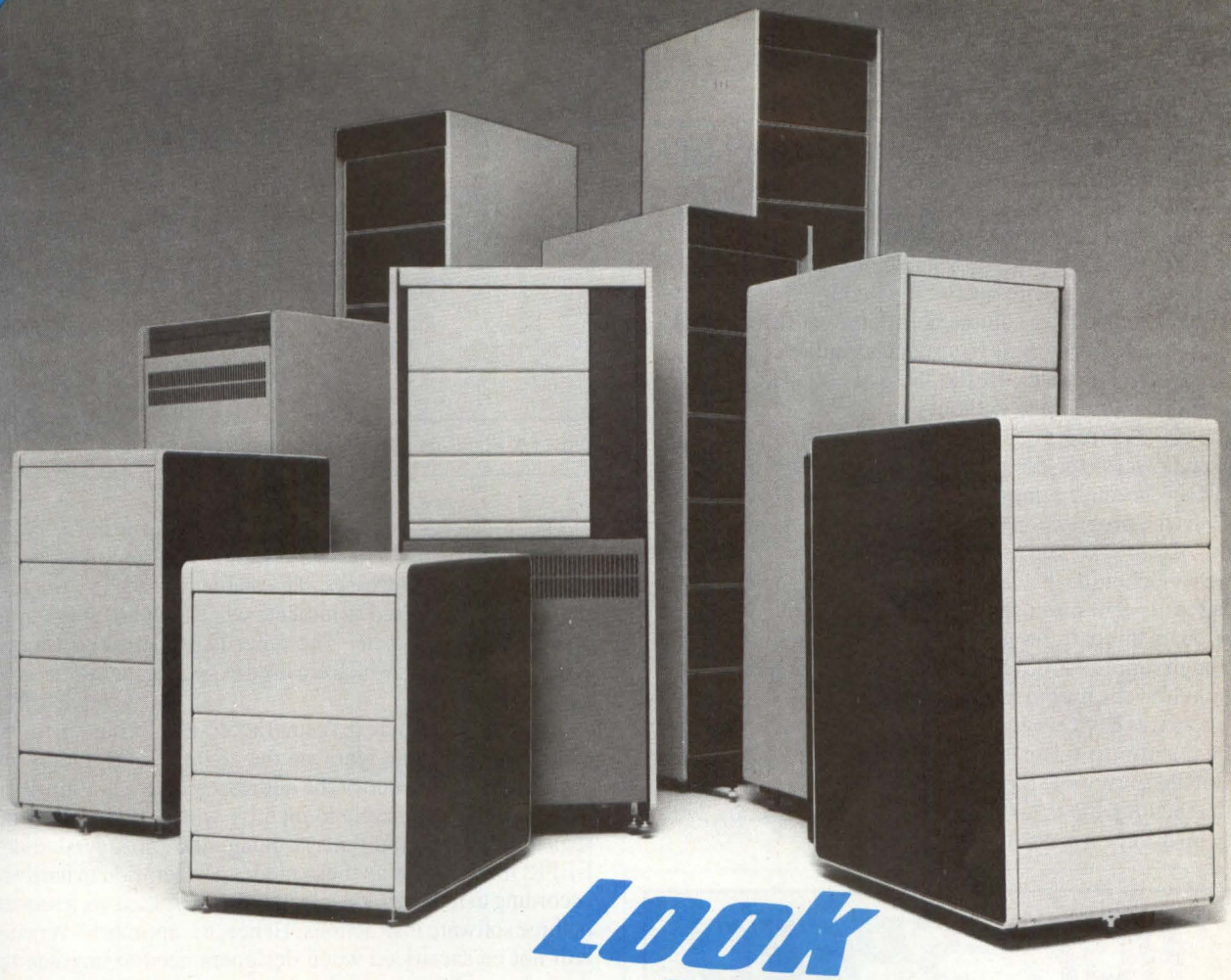
of chips as standard, including 5V programmability, on-chip address, data latches, timing circuitry, automatic erase before write and mechanisms to prevent inadvertent write cycles during power up and power down situations. Today, the 16K EEPROM is available in both 24-pin and 28-pin sockets, but only the 28-pin package will allow designers to directly upgrade from the 16K to the 64K density level in the same socket (**Figure 2**). At present, several manufacturers provide different schemes for signaling the completion of the write cycle on their 28-pin EEPROM parts. Most recommend that the designer weigh the trade offs between them before choosing the notification scheme used in their system.

The first option is to use the Ready/Busy output found on pin 1. This pin is used to notify the microprocessor in the system that a write cycle is in progress if the open drain current is low. The Ready/Busy line could be connected to an interrupt request pin of a microprocessor to interrupt the microprocessor when a write cycle is completed or to generate a status bit. If the

EEPROM CROSS REFERENCE AND SELECTION GUIDE

General Instrument	Organization	Pins	Power Supply	Format	Size	Technology
AMD						
9864 EEPROM	8K×8	28	5V	Parallel	64K	NMOS
2864A EEPROM	8K×8	28	5V	Parallel	64K	NMOS
2817A EEPROM	2K×8	28	5V	Parallel	16K	NMOS
EXEL						
XL46C16 EEPROM	2K×8	28	5V,12V	Parallel	16K	CMOS
XL2816A EEPROM	2K×8	24	5V	Parallel	16K	NMOS
XL2817A EEPROM	2K×8	28	5V	Parallel	16K	NMOS
XL2865A EEPROM	8K×8	28	5V	Parallel	64K	NMOS
XL2864A EEPROM	8K×8	28	5V	Parallel	64K	NMOS
XL48C64 EEPROM	8K×8	28	5V	Parallel	64K	CMOS
XL28C256 EEPROM	32K×8	28	5V	Parallel	256K	CMOS
General Instrument						
ER1451 EAROM	50×14	14	−30V,5V	Serial	700 bits	MNOS
ER0082 EAROM	82×1	18	−30V,5V	Parallel	82 bits	MNOS
ER1450 EAROM	50×14	14	−30V,5V	Serial	700 bits	MNOS
ER1400 EAROM	100×14	14	−30V,5V	Serial	1400 bits	MNOS
ER2051 EAROM	32×16	28	−28V,5V	Parallel	512 bits	MNOS
ER2055 EAROM	64×8	22	−28V,5V	Parallel	512 bits	MNOS
ER5901 EEPROM	128×8	24	5V	Parallel	1K	SNOS
ER5911 EEPROM	64×16 or 128×8	8	5V	Serial	1K	SNOS
ER59256 EEPROM	16×16	8	5V	Serial	256 bits	SNOS
ER3400 EAROM	1K×4	22	−30V,−12V,5V	Parallel	4K	MNOS
ER2810 EAROM	2K×4	24	−24V,−14V,5V	Parallel	8K	MNOS
PCD8572 EEPROM	128×8	8	5V	Serial	16K	SNOS
ER5904 EEPROM	512×8	24	5V	Parallel	4K	SNOS
ER5912 EEPROM	128×16 or 256×8	8	5V	Serial	2K	SNOS
PCD8582 EEPROM	256×8	8	5V	Serial	2K	SNOS
ER5902 EEPROM	256×8	24	5V	Parallel	2K	SNOS
ER5914 EEPROM	256×16 or 512×8	8	5V	Serial	4K	SNOS
HITACHI						
HN5806 EEPROM	8K×8	28	5V	Parallel	64K	MNOS
HUGHES						
H0938	2K×4	28	5V	Parallel	8K	CMOS
H3264	8K×8	28	5V	Parallel	64K	CMOS
H3108A	1K×8	24	17V	Parallel	8K	CMOS
H3104A	512×8	24	17V	Parallel	4K	CMOS
H3300	32×8	18	5V	Parallel	256 bits	CMOS
INTEL						
2816A EEPROM	2K×8	24	5V	Parallel	16K	NMOS
2817A EEPROM	2K×8	28	5V	Parallel	16K	NMOS
2864B EEPROM	8K×8	28	5V	Parallel	64K	NMOS
2004 NVRAM	512K×8	28	5V	Parallel	4K	NMOS
2001 NVRAM	128×8	18	5V	Parallel	1K	NMOS
MITSUBISHI						
M58653P	50×14	14	−30V,5V	Serial	700 bit	MNOS
M58657P	100×14	14	−30V,5V	Serial	1400 bit	MNOS
M58658P	20×16	14	−30V,5V	Serial	320 bit	MNOS
M5G1400P	100×14	14	−35V	Serial	1400 bit	MNOS
MOTOROLA						
MCM2801	16×16	14	5/25V	Serial	256 bit	FETMOS
MCM2802	32×32	14	5/25V	Serial	1024 bit	FETMOS
MCM2833	4K×8	28	5V	Parallel	32K	FETMOS
MCM2864	8K×8	28	5V	Parallel	64K	FETMOS
NCR						
52864 EEPROM	8K×8	28	5V	Parallel	64K	SNOS
52801 EEPROM	16×16	14	5V	Serial	256 bits	SNOS
52832 EEPROM	4K×8	28	5V	Parallel	32K	SNOS
59306 EEPROM	16×16	8	5V	Serial	256 bits	SNOS
59308 EEPROM	64×16	8	5V	Serial	1K	SNOS
52001 NVRAM	128×8	24	5V	Parallel	1K	SNOS
52002 NVRAM	256×8	24	5V	Parallel	2K	SNOS
52004 NVRAM	512×8	24/28	5V	Parallel	4K	SNOS
52210 NVRAM	64×4	18	5V	Parallel	256 bits	SNOS
52211 NVRAM	128×4	18	5V	Parallel	512 bits	SNOS
52212 NVRAM	256×4	18	5V	Parallel	1K	SNOS
National Semiconductor						
NMC98C64 EEPROM	8K×8	28	5V	Parallel	64K	CMOS
NMC9817 EEPROM	2K×8	28	5V	Parallel	16K	CMOS
NMC9346 EEPROM	64×16	8	5V	Serial	1K	NMOS
NMC9802 EEPROM	256×8	18	5V	Parallel	2K	NMOS
NMC9306 EEPROM	16×16	8	5V	Serial	256 bits	NMOS
NMC9816A EEPROM	2K×8	24	5V	Parallel	16K	XMOS
NMC9817A EEPROM	2K×8	28	5V	Parallel	16K	XMOS
SEEQ						
52B33 EEPROM	8K×8	28	5V	Parallel	64K	NMOS
52B13 EEPROM	2K×8	24	5V	Parallel	16K	NMOS
2816A EEPROM	2K×8	24	5V	Parallel	16K	NMOS
5516A EEPROM	2K×8	28	5V	Parallel	16K	NMOS
2817A EEPROM	2K×8	28	5V	Parallel	16K	NMOS
5517A EEPROM	2K×8	28	5V	Parallel	16K	NMOS
2864 EEPROM	8K×8	28	5V	Parallel	64K	NMOS
SGS						
M120 EEPROM	256×4	18	5V	Parallel	1K	NMOS
M9306 EEPROM	16×16	8	5V	Serial	256 bit	NMOS
XICOR						
X2404 EEPROM	512×8	8	5V	Serial	4K	NMOS
X2804A EEPROM	512×8	24	5V	Parallel	4K	NMOS
X2816A EEPROM	2K×8	24	5V	Parallel	16K	NMOS
X28C64 EEPROM	8K×8	28	5V	Parallel	64K	CMOS
X2864A EEPROM	8K×8	28	5V	Parallel	64K	NMOS
X28256 EEPROM	32K×8	28	5V	Parallel	256K	NMOS
X2816B EEPROM	2K×8	24	5V	Parallel	16K	NMOS
X2864B EEPROM	2K×8	24	5V	Parallel	64K	NMOS
X2001 NVRAM	128×8	24	5V	Parallel	1K	NMOS
X2002 NVRAM	256×8	28	5V	Parallel	2K	NMOS
X2004 NVRAM	512×8	28	5V	Parallel	4K	NMOS
X2210 NVRAM	64×4	18	5V	Parallel	256 bits	NMOS
X2210A NVRAM	14×4	18	5V	Parallel	256 bits	NMOS
X2212 NVRAM	256×4	18	5V	Parallel	1K	NMOS
X2212A NVRAM	256×4	18	5V	Parallel	1K	NMOS
X2444 NVRAM	16×16	8	5V	Serial	256 bit	NMOS



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EEPROM is in a write cycle, the Ready/Busy pin is pulled low and held low until the cycle is completed. Once completed, it is pulled high indicating that valid data may be read from the EEPROM. A second notification feature available to the user is DATA polling, in which the most significant bit of the last byte is used to let the microprocessor know that a write cycle is in progress. During a write cycle, an attempted read of the EEPROM will result in a complement of the data bit. After the completion of the write cycle, true data is available. This read/compare scheme allows the EEPROM to be polled to determine if it is still in a write cycle without any external hardware.

Some manufacturers consider the Read/Busy feature an inferior solution to the problem of write cycle completion notification. This is because tying up pin 1 for the Ready/Busy function limits the progression of the device to the 256K level in a 28-pin DIP.

Another technique that most EEPROM manufacturers may soon adopt is one proposed by Exel when it introduced its XL48C64. In this part, several special user features are accessible through simple software commands. Three unique on-chip registers allow the user to select a variety of operational modes and to monitor device status. The special functions available include a software selectable 32-byte page mode, a 5V-chip erase mode, a fast write mode that allows a 5 msec write cycle time, a read only mode for inadvertent write protection and a Ready/Busy device status indicator.

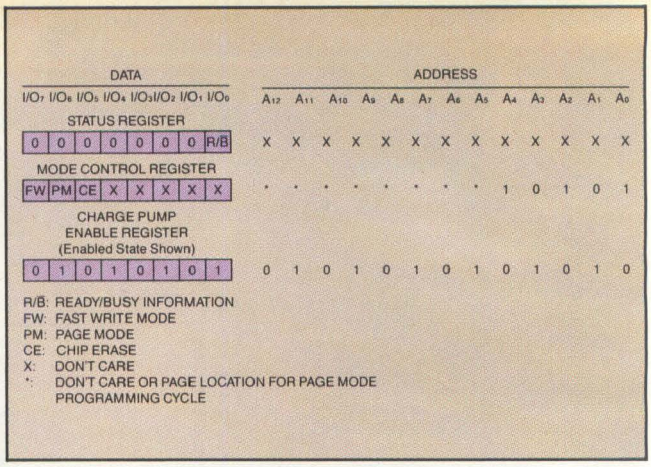

Figure 4: XL48C64 status word configuration.

The three registers are accessible whenever pin 1 SW (the Status Word) is low. These are shown in **Figure 3** along with their respective addresses. The status register is a read-only register which is used to indicate when the part is executing a nonvolatile write cycle. The other two control registers are write-only registers which are used to operate the special device modes.

The status read cycle ($\overline{SW}$ low) accesses information from the status register while ignoring the address lines. Status write cycles require that one of the addresses shown in **Figure 4** accompany the write cycle to identify which of the two control registers is to be modified. Although the 256K version of the EEPROM will give up these modes of operation in hardware, according to industry sources, it will be retained via a sequence of three software instructions. Hence, the approach's versatility will not be sacrificed when designers need to upgrade their designs to a higher density. Higher density EEPROMs will open up new applications for program storage and data table applications, such as calibration constants and configuration parameters.

Soft-key configurations in a graphics or a character-oriented terminal is an example of functions, such as protocol, screen attributes and character fonts, which can be keyed in by the user. Calibration constants can be stored in an EEPROM with a smart interface for a robot's axis of movement. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location may be stored. The EEPROM may also be used as a nonvolatile storage device inside the next generation of intelligent credit cards.

CMOS will become the preferred technology in all applications because of the reduced power requirements and the reliability of system operation. This, coupled with decreasing read and write times to the device and increasing endurance times, will continue to diversify the applications of the EEPROM.

DD

References:

1. Proceedings of the 1984 Wescon Conference.
2. Proceedings of the 1985 Electro Conference.

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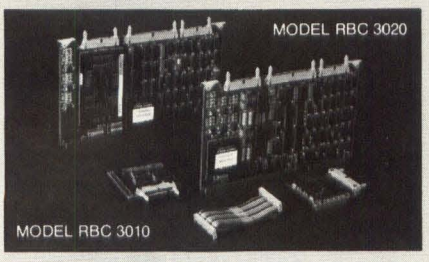

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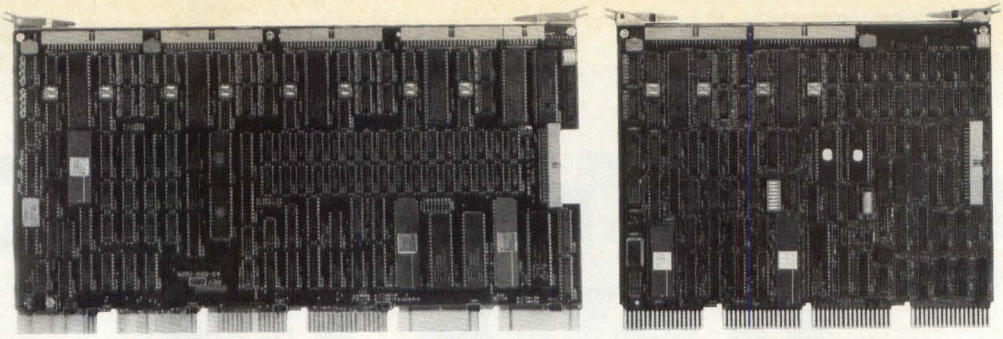

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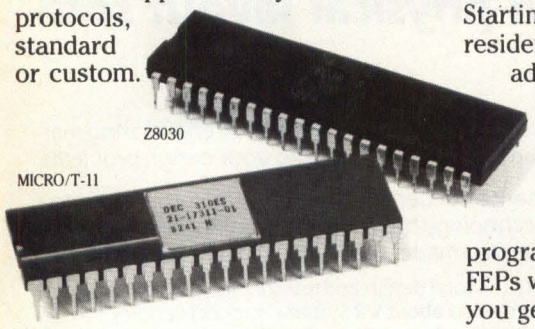

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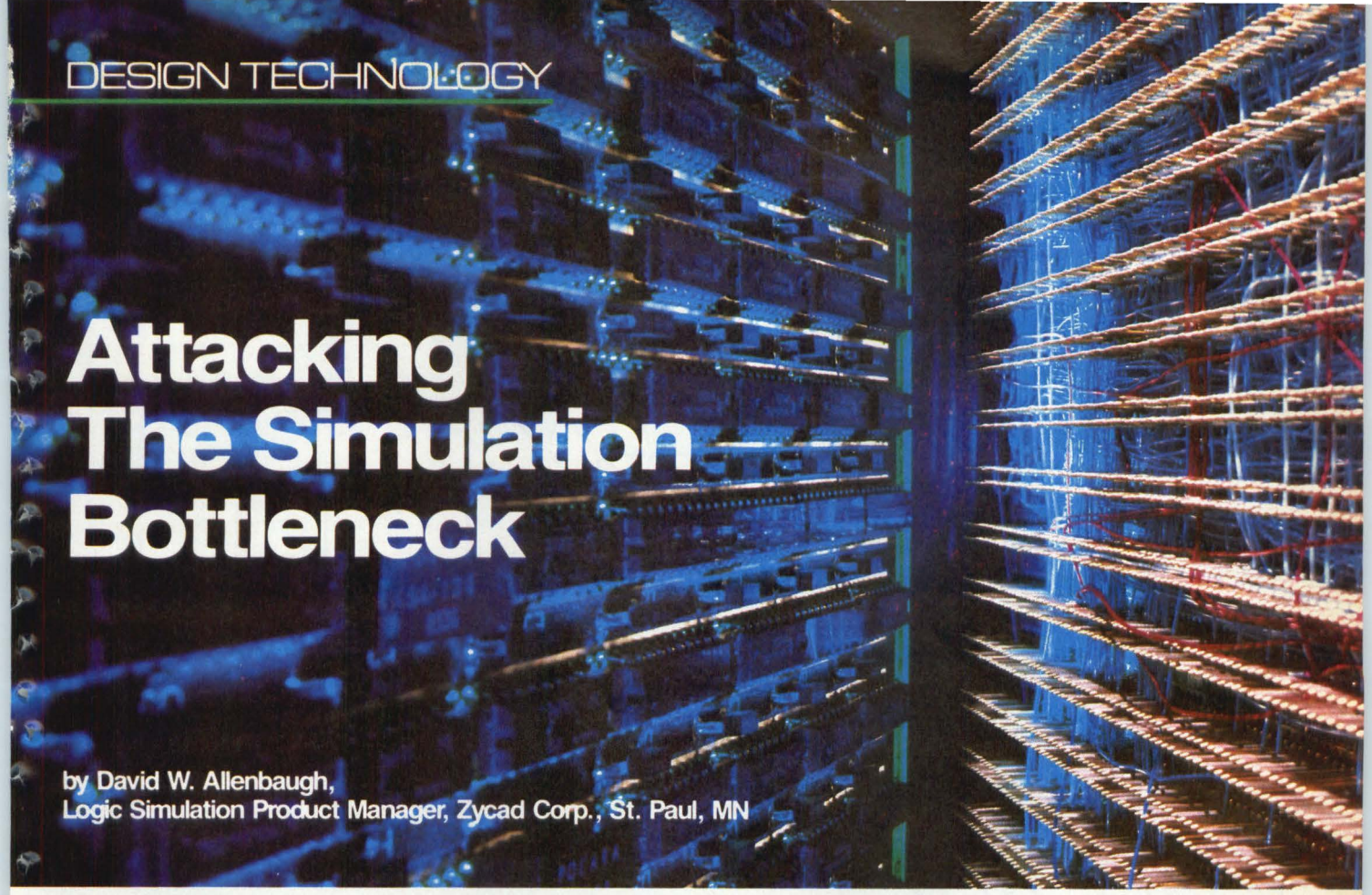
Attacking The Simulation Bottleneck

by David W. Allenbaugh,
Logic Simulation Product Manager, Zycad Corp., St. Paul, MN



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Logic simulation is a highly CPU-intensive circuit design verification task that is an essential element in the design cycle. Without logic simulation, circuit checkout and test times would be unacceptable for today's rapidly shrinking market windows. In many instances, using traditional software-based simulation techniques on LSI and VLSI designs requires an impractical amount of CPU time. A simulation demanding hundreds of hours is not unusual.

The logic simulation process can be divided into four tasks: 1) enter or define the circuit/system, 2) compile the circuit/system into a format acceptable by the simulation algorithm, 3) load the simulation algorithm and perform the simulation and 4) pass the simulation results back to the user. Prior to the introduction of hardware accelerators, executing the actual simulation proved to be the most time-consuming step. To reduce execution times, methods of improving simulation algorithms received much attention. Most attempts to increase speed focused on rewriting the algorithm in a lower level language. Although there have been some positive results, this approach has not progressed to a point where large system-level simulations or thorough regression test simulations are feasible.

An alternative way to tackle the simulation bottleneck is to implement the simulation algorithms in hardware. This approach has been taken by Zycad Corp. (St. Paul, MN) and a few other CAD/CAE companies. Zycad's solution implements an event-driven timing wheel algorithm entirely in hardware (**Figure 1**). The architecture of the hardware accelerator, or Logic Evaluator (LE), is optimized around an event driven simulation algorithm. Each of the possible 16 modules in the LE contains an independent event processing pipeline running at 1 million events/sec. There is no instruction fetching or decoding in the event processors of the LE, so the data (events) flow from place to place concurrently. Hence, the Logic Evaluator functions like a multiprocessor dataflow machine.

In its largest configuration, the system has a random access memory bandwidth of nearly 16 billion bits/sec and processes up to 16 million events/sec. Combining several supercomputer architectural features including multiple pipelines and multiple processors results in simulation performance 1000 times that of a large mainframe. Other features of the system include the following: 12-state simulation; unidirectional, bidirectional and wired gate functions; and fault simulation with timing analysis.

Aside from actual simulation speed, another potential bottleneck is the excessive time necessary to load the algorithm. The LE attaches directly to a host computer or a workstation and is loaded via a 16-bit parallel interface with transfer rates of 1 to 2 Mbytes/sec. This translates into loading 100,000 gates into the system in approximately 9 seconds.

Zycad currently provides interfaces to Apollo-based workstations, DEC's VAX, Prime's computers, Data General's MV series and IBM or IBM plug-compatible mainframe computers through a Device Attachment Control Unit (DACU). A software-based driver to interface the LE from the host is also available for each of these configurations.

Simulation Language

With the attention removed from the actual simulation process, the focus turns to the compile time. Compilation converts a design description from a text or a graphic form to an object-code format that can be loaded into the simulation algorithm. Every simulation system must go through some type of compiling process.

Zycad Intermediate Form (ZIF) is the LE's object-code for-

mat. It consists of several 16-bit binary words, taken separately or in 32-bit pairs and collected into larger structures called packets. Each packet contains a particular type of information. Several packets may perform similar functions and thus form a packet group. There are four kinds of packets: control packets, network packets, input packets and output packets.

Control packets dictate how the LE responds to and executes simulations. Network packets describe the simulation network to the LE. All gates, fan-outs and delay values are included in the network packet. Input packets target and stimulate, or both, the pins of a simulation network, and output packets contain the data returned from a simulation run. There are five types of output packets: two that output only design verification data, two reporting fault simulation information and one providing execution statistics at the end of a simulation. Dividing the LE input

(continued on p.85)

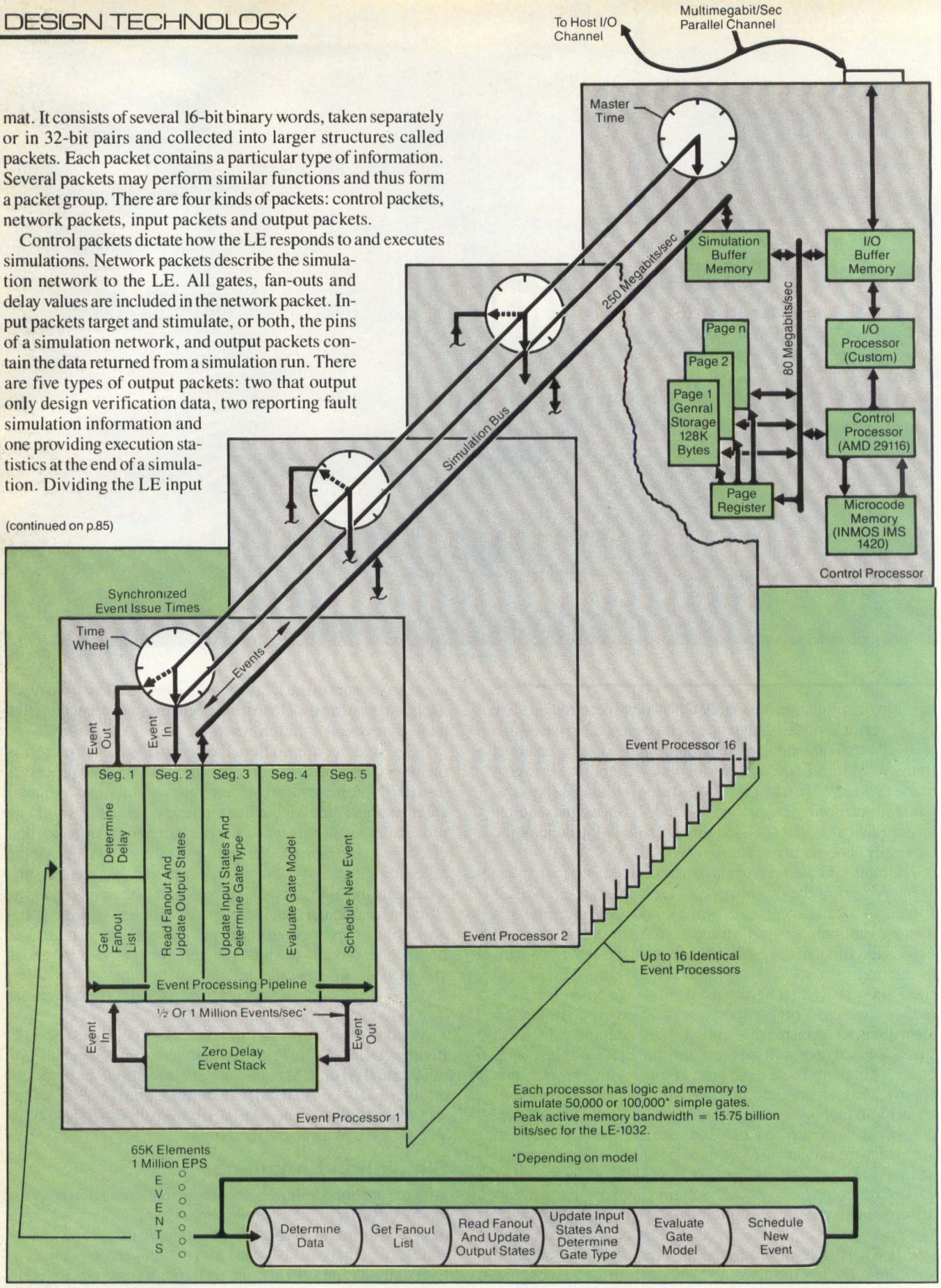

Figure 1: Zycad's Logic Evaluator drastically increases simulation speed in comparison to traditional software simulators. The architecture of the Logic Evaluator is based on an event-driven timing wheel algorithm.

(continued from page 80)

information into independent packets allows the user to send only those packets that changed from the previous run. In the typical case, a network (the largest packet) is tested with many tests and combinations of observed outputs. These runs can be made by changing only the smaller test and output packets.

A number of current LE users integrated the LE into their existing proprietary CAD systems by developing their own compilation software. Another option is to use ZILOS, Zycad's front-end software package that permits the LE to function like a virtual turnkey system. ZILOS was developed through a joint agreement between Zycad and SimuTec (Incline Village, NV). The package functions as an interface between ZIF and SimuTec's SILOS simulation description language. Simulation input data coded in SILOS may be translated to ZIF, via ZILOS, and executed on the LE.

SILOS commands can use most of the LE's capabilities through ZIF. Conversely, the LE executes most processes that can be described by SILOS commands. ZILOS provides users with the power and flexibility of a SILOS simulator along with the speed and capacity of the LE. With ZILOS, compilation of a 20,000-gate design takes about 4 minutes; 100,000 gates can be compiled in approximately 20 minutes. ZILOS is presently available for DEC's VAX and Apollo-based workstations.

Designers currently using Tegas or workstation software from Mentor Graphics (Beaverton, OR) can also integrate a Logic Evaluator into the existing environment (**Figure 2**). Two interfaces currently exist for the Mentor workstations. XSIM, an interface supplied by Mentor, allows the LE to be shared on an Apollo networking ring and makes the LE transparent to the user. Zycad offers a second interface that permits Mentor users to translate Mentor's database to the ZILOS input language. A similar translator is also available for workstations from Tektronix, CAE Systems Division (Sunnyvale, CA) and Daisy (Mountain View, CA).

On mainframe computers, Tegas is the most commonly used software simulator. A translator that converts Tegas Design Language (TDL) to ZILOS is provided by Zycad. The use of a translator is often accompanied by wasted CPU time. However, this is not the case with Zycad's Tegas-to-ZILOS translator. A benchmark comparing throughput simulation times of a 20,000-gate design on DEC's VAX/780 using Tegas and the Zycad system was recently completed. To compile and link the design using Tegas required 51.5 minutes; simulating 2000 test vectors (approximately 13 million events) took 5 hours and 52 minutes. In contrast, using ZILOS and the TDL-to-ZILOS translator, the same simulation requires 2 minutes to translate, 6 minutes for ZILOS compilation and 14 seconds for LE simulation. This yields a sixfold improvement in compilation time and a 1500-fold improvement in simulation time. Total throughput time using the Zycad system was 8 minutes and 49 seconds, compared with 6 hours and 43 minutes on the VAX/Tegas system. **Table 1** highlights several other LE benchmarks.

Software
Zilos → LE
Tegas (TDL) → ZILOS → LE

Hardware
Apollo
Data General MV Series
Digital VAX
IBM (and plug compatible)
Prime

Workstations
Mentor Graphics → XSIM → LE
→ ZILOS → LE
CAE Systems → LE
→ ZILOS → LE
Daisy → ZILOS → LE

Figure 2: When ZILOS is used as a front-end, the Logic Evalutor (LE) functions as a standalone system. However, the system readily interfaces to a wide range of hardware and software from such vendors as DEC, IBM, Daisy, Apollo and Mentor.

Impact On The Design Process

Dedicated simulation engines are causing a major change in the CAE design process. Gate-level system simulation enables complete system verification prior to committing the design to hardware. Design cycles are also shortened when a hardware accelerator is used, enabling manufacturers to make product introductions within tight market windows. Moreover, the impact of hardware accelerators will become greater as the levels of integration in VLSI-based systems continues to rise.

Because of these revolutionary new tools, there may also be a decline in the interest of behavioral-level simulation. Designers must often resort to the behavioral approach when there is insufficient CPU horsepower available to perform gate-level simulation. Machines such as the LE, however, offer the designer a tool that is thousands of times faster than anything previously available. DD

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Benchmark Description	Existing System	Zycad System	Simulation Time, Existing System	Simulation Time, Zycad System
41,000 gates 41075 ZIF elements 1643 input vectors	IBM 3083 Tegas	VAX/750 LE-1002* ZILOS	45 minutes	35.5 second
8,000 gate array 6362 ZIF elements 2770 sample times	CDC Cyber 205 Tegas	VAX/750 LE-1002 ZILOS	10.5 minutes	2 seconds
8,000 gate array 6362 ZIF elements 2770 sample times	CRAY XMP Tegas	VAX/750 LE-1002 ZILOS	3.9 minutes	2 seconds
3,000 gate array 6362 ZIF elements 2770 sample times	VAX/780 Tegas 5	VAX/750 LE-1002 ZILOS	100 minutes	2 seconds
1692 gates 8600 input vectors 2,150,000 sample times	VAX/750 Silos	VAX/750 LE-1002 ZILOS	31.7 minutes	7 seconds
751 gates: 363 conventional 114 nodes 274 bidirectional 2560 input vectors	IBM 4341 Internal	VAX/750 LE-1002	21.4 minutes	8.6 seconds

Note: The LE-1002 is Zycad's basic model.

Table 1: Examples of simulations running on some of the world's most powerful computer systems illustrates the performance of the Logic Evaluator.

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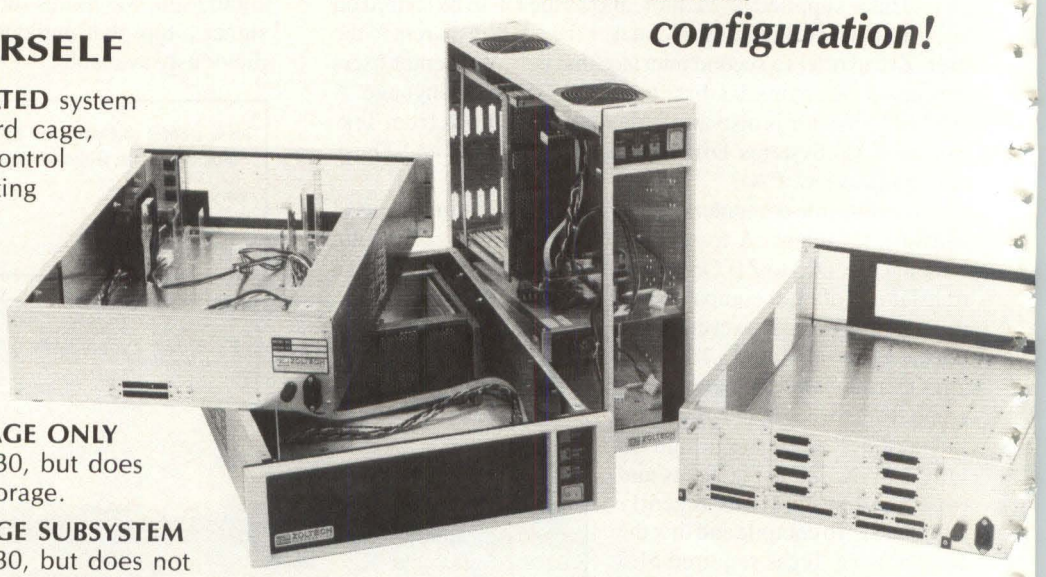

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NEW PRODUCT FOCUS

S Y S T E M S

PC/AT-Based CAE Design System

The CAE Systems Division of Tektronix (Sunnyvale, CA) has upgraded the IBM PC/AT, making it a circuit design workstation. An addition to the 6000 Series family of intelligent graphics workstations, the Tekstation AT can act as a standalone system or as a multiuser system networked through Ethernet. It supports applications ranging from CAE-based design capture, design verification and physical layout to software development under the UTek operating system. UTek, also supported by all Series 6000 products, is Tektronix's version of the Berkeley 4.2 UNIX-based operating system.

The Tekstation AT is also packaged with the CAE 2000 Designers' Database/Schematic Capture software and IDEAL logic simulator for compatibility with larger CAE-based systems. In addition to compatible application software from IBM and other third party vendors for tasks such as word processing and project planning, PC-DOS, which operates simultaneously with UTek, is supported.

In hardware, CAE Systems Division has added the National Semiconductor 32016 16-bit 10 MHz coprocessor, allowing access to 16 Mbytes of virtual memory. Disk storage is increased from 85 Mbytes expandable to 280 Mbytes. It has also added a graphics card for 720 × 704 pixel resolution and increased RAM to 2.5 Mbytes expandable to 4.5 Mbytes in standard configurations.

A file server configuration is available for about $40,000, an Ethernet interface for $1,400. Tekstation AT prices start at $25,000.

—Lamneck

Circle 234

S O F T W A R E

Hierarchical Design Review Speeds Throughput

Taking advantage of the high degree of hierarchy and redundancy in VLSI circuits, the DRACULA III layout verification package from ECAD Inc. (Santa Clara, CA) increases the throughput of existing superminicomputers or engineering workstations. As a result, users need not move to more expensive supercomputers or hardware accelerators as their circuits increase in size.

With circuit complexity increasing the IC's layout is constrained by the minimum chip area and the design rules. In fact, critical circuit paths become more important as the electrical parameters become closely related to the geometries. Unfortunately, many existing programs that check circuit layout can take several hours on a DEC VAX-11/780 to verify a 50,000-gate circuit. Such programs typically view the circuit as a flat homogeneous structure, so memory requirements increase rapidly as the size of the circuit grows, as does the processing required to verify each portion of the circuit.

However, most circuit layouts can be viewed as a collection of cells with each cell containing polygons that represent the physical location of individual elements (e.g., transistors and interconnects). Individual cells can be repeated, overlapped with other cells or combined to form larger cell structures that also can be repeated many times. This collection of individual cells and combined cells forms a hierarchical tree structure describing their geometric relationships to each other.

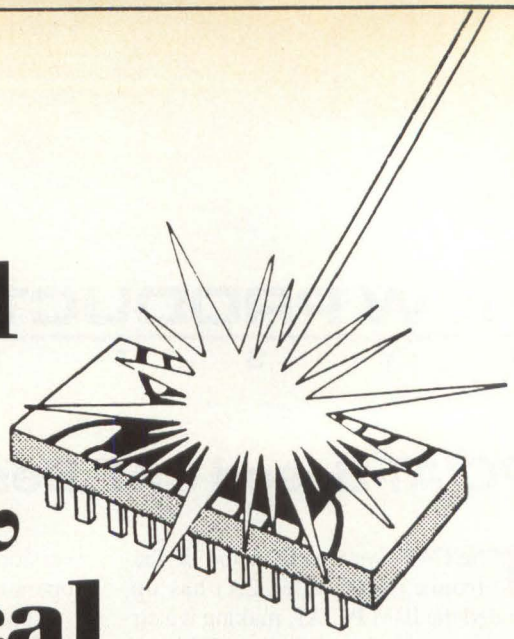
DRACULA III analyzes intercell geometric interactions within individual cells only once or analyzes the geometric interaction between a collection of cells only once. These characteristics are then stored for future reference whenever the package encounters a similar configuration. Since the netlist that describes the overall organization of the circuit is also saved, the verification process is analogous to compiling a subroutine and relinking the entire program. As a consequence, the company claims performance 4× to 10× faster than packages that do not utilize such an approach. ECAD cautions that performance gains are tempered by the size of the circuit as well as the degree of overlap allowed between cells. The hierarchical approach works best with complex circuits with a minimum of overlap between cells. Small circuits, or those with highly overlapped cell structures, work better with the flat approach, according to ECAD.

The package is available on a wide variety of minicomputers including those from Data General, Digital Equipment and Gould Computer Systems. Versions are also available for the Apollo and Sun engineering workstations.

—Aseo

Circle 233

Experimental Physicists Electronics & Electro-Optical Engineers



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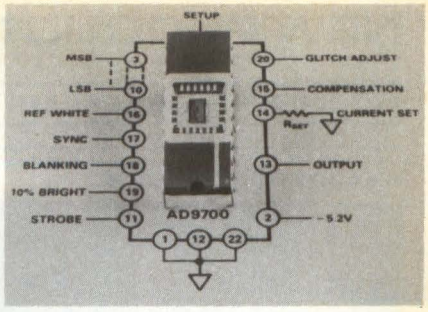


Designed to function as a building block in graphics systems, Analog Devices' (Norwood, MA) AD9700 monolithic D/A converter can accept 8 bits of digital data at update rates as high as 125 MHz, a feature important to the spatial resolution associated with raster scan systems. Equally important is the AD9700's high settling time specified at 10 nsec to 0.4% of gray scale. The ECL-compatible device is housed in a 22-pin package and operates from a single -5.2V power supply, dissipating only 650 mW. The output is quoted to develop 1V across a 75 ohm load which will drive a graphics monitor that conforms to EIA standards RS-170 and RS-343.

Eight current switches drive a precision R2R network; the AD9700's built-in bandgap reference controls the current switches and achieves temperature stability as well as a power supply rejection ratio of 0.1%/volt. The 8-bit inputs are gated through ECL registers within the device, providing data storage and minimizing glitches in the output signal. A glitch adjust pin is also supplied on the device. The rise and fall times of the AD9700 are specified at 2 nsec, achieving compatibility with high bandwidth CRTs and extending the capability for higher pixel density.

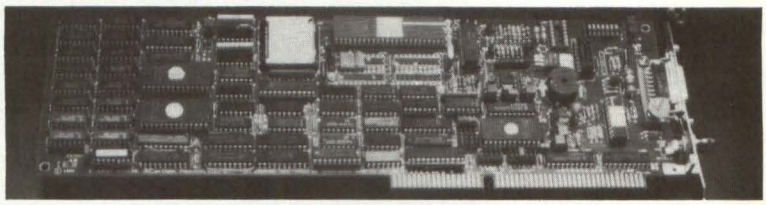
The AD9700 provides five composite function input controls: composite blanking, composite sync, reference white, 10% bright and setup, which allows control over the composite blanking level. In addition, the need for external timing circuitry to integrate sync and blanking with gray scale information is eliminated.

Five versions of the AD9700 are available. The AD9700BW (nonhermetic) and AD9700BD (hermetic) are DIP units operating over a temperature range of -25°C to +85°C; the hermetic DIP AD9700SD is for use over a range of -55°C to +125°C. The AD9700BE and AD9700SE are leadless chip carrier devices for temperature ranges of -25°C to +85°C and -55°C to +125°C, respectively. The SD and SE versions are available in military requirements.

—Lamneck

Circle 231

Ethernet PC Transceivers, Controllers Based On VLSI Chip



Three new products for the 3Com (Mountain View, CA) IEEE 802.3 EtherSeries IBM PC network have been designed with a VLSI transceiver IC developed by 3Com and Advanced Micro Devices (Sunnyvale, CA). The 3C101 transceiver connects all 802.3-compatible controllers to the Ethernet cable by a piercing tap. A half-card network controller for the PC, the 3C500B replaces the previous full-size board. The 3C505 is an intelligent controller designed to work in the AT for server functions, as well as in the PC and XT.

The 3C505 has dual bus connectors, so it can be used in an AT with full 16-bit I/O to create a communication, print or disk server. In addition to the AMD transceiver IC, the board uses an 80186 for protocol processing, an 82586 Ethernet coprocessor and 128 Kbytes of RAM, expandable to 256 Kbytes. Smaller or more lightly loaded networks can use the same card in an XT or PC. Both this board and the standard-performance 3C500B controller have two connectors, one for standard Ethernet coax and an external transceiver and one for thin (Cheapernet) cable with the transceiver on-board.

The 3C500B provides a personal computer connection to Ethernet with three VLSI chips. Integration of more transceiver functions onto the AMD chip is a major factor in packing the controller onto a half-card, which eliminates the need for a card guide at installation.

Rather than the standard 500m up to 1 km of cable can be used with the 3C101 transceiver. Designed to be fully IEEE 802.3 compatible, it taps into an Ethernet cable by piercing and operates with any make of controller. The piercing tap is not a new configuration, but eases network reconfiguration and installation.

3Com has also introduced two software packages to extend the range of EtherSeries: the Ether3270 gateway into SNA and the EtherMac products to link Macintoshes into 3Com's multifunction 3Server box. An expansion board for the 3Server provides direct connection into AppleTalk. The Port Expansion Board costs $625, the EtherShare software is $695 per server, EtherPrint is $395 per server and EtherMac software is $50 per user. Users with the $7,995 3Server can upgrade the Share and Print software for $125 each. Ether3270 is $1,595 for either PCs or the 3Server.

The piercing 3C101 tap is priced at $295, with installation toolkit and parts available. The half-card 3C500B costs $650 and the 3C505 high-performance controller, $1,095. All prices are suggested list and subject to OEM discounts.

—Pingry

Circle 230

COMPUTERS/SYSTEMS

In-Circuit Emulator

Supporting NMOS and CMOS 8088 μP up to 8 MHz, this in-circuit emulator, the SBE-88, features 5 real-time breakpoints, 64 Kbytes of mappable memory and an RS-232 interface. The SBE-88 supports the minimum and maximum modes of operation for the 8088 and provides full support for the 8087 and 8089 coprocessors. The five breakpoints allow real-time program execution until an opcode fetch occurs at a specified break address. Price is $2,495 (32K) and $2,795 (64K). **Huntsville Microsystems**, Huntsville, AL **Circle 205**

Dual-μP System

Based on the 68000 and the microEclipse processors, this dual-microprocessor system, the Desktop Generation Model 45, runs Desktop/UX, a native UNIX operating system based on System V. The dual architecture allows the microEclipse to offload I/O operations from the 68000, which is dedicated to UNIX applications. The basic configuration consists of 512 Kbytes of memory, a 15-Mbyte disk and one floppy diskette drive. Price is $750. **Data General**, Westboro, MA **Circle 152**

VME-Based 32-Bit Supermicro

Designed for harsh environments, this real-time UNIX-based 32-bit supermicrocomputer, the Universe 2400, is built around the 12.5 MHz MC68000 and the VMEbus. Its 32-bit internal datapath and 4-Kbyte cache enable the Universe 2400 to execute 1.25 MIPS with no wait-states. The 32-bit VMEbus has a bandwidth of 40M bps and optional I/O processors, each with its own MC68000. Supporting UN/System V, the firm's implementation of UNIX System V, and UNOS, the company's UNIX-compatible real-time operating system, the Universe 2400 is priced from $9,999 to $17,500. **Charles River Data Systems**, Framingham, MA **Circle 157**

Workstations For Designing, Programming, Testing Programmable Devices

Both of these workstations, the Universal Programming workstation and the Logic Programming workstation perform designing, programming and testing of over 125 programmable logic devices such as PALs and IFLs. They also perform logic reduction and device simulation and are hosted on a pretested IBM PC/XT setup with a 256-Kbyte RAM, 10-Mbyte hard disk and a monochrome display. The software includes MS-DOS 3.0, PROMlink and ABEL. The programmer is the 29B, set up as a logic programmer or as a universal PROM/logic programmer. Prices are $11,250 (Logic Prog.) and $13,750 (Universal Prog.). **Data I/O**, Redmond, WA **Circle 160**

DEC-Compatible Backplane/Mass Storage

A pair of DEC-compatible backplane/mass storage systems offer features not available with the MicroPDP-11. The Cyclone Mass storage system includes a Q-Bus backplane, mass storage controller/interface, power supply and Winchester tape and floppy drives. The controller conforms to DEC's MSCP so can be configured with the LSI-11/23 PLUS and LSI-11/73. The CSM-ST model offers 36 to 240 Mbytes of Winchester capacity and a 60 Mbyte streaming tape drive; the CSM-FL offers 36 to 88 Mbytes of hard storage and an 8" floppy drive. Price ranges from $9,400 to $21,000. **Qualogy**, San Jose, CA **Circle 155**

Computer Paint System

With a full color (24-bits/pixel) mode, this computer paint system, the ArtStar II, provides 16.7M colors. With a filtering capability to output 4,000-line resolution digital camera photos, ArtStar II's panel cell animation and multiple color cycling feature (Color Palette Movies) brings animations to the screen. Other features include antialiased drawing, 99 fonts on line, with camera font compose, pans and zooms and a pen-user interface that eliminates the use of a keyboard. Price is $94,900. **ColorGraphics Systems**, Madison, WI **Circle 161**

150 nsec Supermini

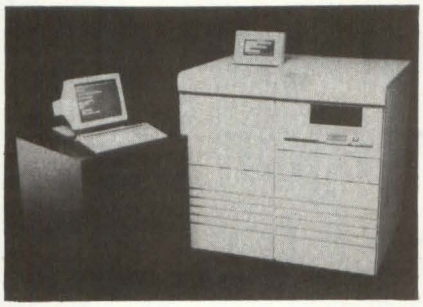
This line of 32-bit superminicomputers uses the firm's VLSI technology and 64-Kbit memory. The 9400 has a 150 nsec cycle speed and includes a 1-Mbyte 9400 processor, a 40-Mbyte Winchester drive, 3 CRTs, a 125 lpm printer and the ITX operating system. The 9400 processor module provides a micro-controlled 32-bit processor with up to 4 Mbytes of memory, up to 8 system peripherals and up to 210 RS-232 connections. Price is $67,000. **NCR**, Dayton, OH **Circle 156**

Universal Microcomputer Development System

Supporting 8-bit CMOS and single-chip microcomputers, this microcomputer development system, the SA-1000, supports Hitachi's 6301, 6305, the HSP (signal processor) 61810, and NEC's 7810/11. The unit includes a 12" CRT, two 8" floppy disk drives, an ASCII keyboard, real-time in-circuit emulation with 64 Kbytes of no-wait state RAM and

a built-in universal PROM programmer. Price is $7,995. Emulation probes are available for $2,495 to $3,245 each. **Sophia Computer Systems**, Santa Clara, CA **Circle 154**

5/7 MIPS Superminis



The HCX-7 32-bit superminicomputer features 7.1 MIPS performance in UNIX and C language environments. With an instruction set of 160 that typically requires one machine cycle of 100 nsec to execute, the HCX-7 allows up to 235 terminal connections. The H1200 superminicomputer provides 5.0 MIPS and also supplies 32-bit addressing. Supporting up to 224 interactive users, the H1200 uses 100K ECL technology. **Harris**, Ft. Lauderdale, FL **Circle 151**

Data Acquisition System

An addition to the firm's data acquisition line, the 1752A data acquisition system acquires data at 1000 readings/sec with one standard analog measurement processor. Each analog measurement processor employs a 14-bit A/D converter multiplexed to 16 differential analog measurement channels. The processor offers resolution to 124 μV in the 1V range, measurement accuracy of 0.02% and DC common mode rejection of 70 dB. The 16-bit CPU supports Macrostore floating point processor, 132K main memory, 400-Kbyte double-sided, double-density floppy disk and IEEE-488/RS-232-C interfaces. Price is $8,390. **Fluke**, Everett, WA **Circle 159**

Enhancements For Color Workstation

A graphics processor and accompanying graphics buffer have been added to improve the speed of graphics applications on the Sun-2/160 color sunstation. The graphics processor supports all of the Sun-2/160 graphics standards including the CGI standard, available with Sun System Release 2.0. With the graphics processor, the Sun-2/160 draws vectors with floating point coordinates at 1.5 MIPS, allowing for display of 40,000 2D vectors/sec and 25,000 3D vectors/sec. The shading rate of 3D polygons is 1 MIPS with polygon fill rates of up to 35 MIPS. Both the processor and the buffer list at $5,900. **Sun Microsystems**, Mountain View, CA **Circle 153**

In-Circuit Emulators For 6809/80186

Both of these in-circuit emulators, the ICD-178 for Motorola's 6809 and the ICD-278 for Intel's 80186, can operate in a standalone environment (controlled by a console terminal) or with a host computer. The ICD-178 8-bit emulator operates at 2 MHz with 64 Kbytes SRAM for downloading files, altering memory contents and loading future memory into a target system. The ICD-278 16-bit emulator operates from 8 to 12 MHz with 128 Kbytes SRAM. **Zax**, Irvine, CA **Circle 158**

PERIPHERALS

Desktop Test Head

Designed for the PC-based Dash family of electronic design tools, this functional testing subsystem, Dash-Test, verifies semicustom VLSI chips in the same system used for the chip's development. Dash-Test reveals functional differences and prototype errors by forcing identical test vectors into both the software models and hardware prototypes. For application-specific ICs and PCBs with up to 256 I/O pins, Dash-Test connects the device under test through a zero insertion force socket. It can be configured in increments of 16 up to 256 channels, enough capacity to handle multiple sets of ASICs if a given logic array cannot fit into a single package. Price is $5,000. **FutureNet**, Canoga Park, CA **Circle 169**

LAN For HP 9000 Series 500s

A full implementation of the IEEE 802.3 standards for a 10 Mbyte/sec, baseband multiple-access/collision-detection LAN, the HP 9000 LAN links HP 9000 Series 500 computers to one another and to HP 3000 computers. Offering Ethernet Version 1.0 support, the LAN consists of Network Services/9000 Series 500 software (HP 5095314) and the LAN/500 link interface card (HP 27125A). **Hewlett-Packard**, Palo Alto, CA **Circle 167**

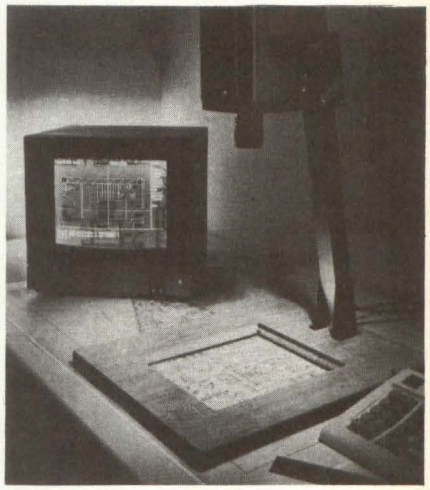
Statistical Multiplexer With Integral Modem

This 4- or 8-channel menu-driven modular multiplexer, the 7400-series statistical multiplexer, features a 2400 bps switched network internal modem option, leased-line internal modems with automatic dial back-up and restoral and an extended system control function that is accessed through a 300 bps help diagnostic modem. For leased-lines, the 7400 also offers integral 4800 and 9600 bps modems with dual-dial backup. **Racal-Vadic**, Milpitas, CA **Circle 163**

3″ Floppy Disk Drives

With storage capacities from 250 Kbytes to 1 Mbyte, these 3″ floppy disk drives (EME-102/202, EME-150/250, EME-130/230) are plug-compatible with 5¼″ floppy disk drive interfaces. Measuring 90 mm wide, 150 mm deep and 40 mm high, the drives include single-button diskette ejection/insertion and direct-drive brushless motor and a steelband. Track density of the disks is 100 or 200 tpi, rotational speed is 300 rpm and disk diameter is 3″. **Panasonic**, Secaucus, NJ **Circle 164**

Video Tracing System



Designed for microcomputer CAD systems, the video tracing system uses a video camera to project drawings onto a monitor. The CAD drawing screen is overlayed on top of the image to trace the drawing into the CAD system. The video tracing system can be used with AutoCAD and CADmaster; the basic system includes software, video camera, stand and scan synchronizer card for IBM PC, XT or AT and sells for $5,000. **Brighter Images**, Lafayette, CA **Circle 166**

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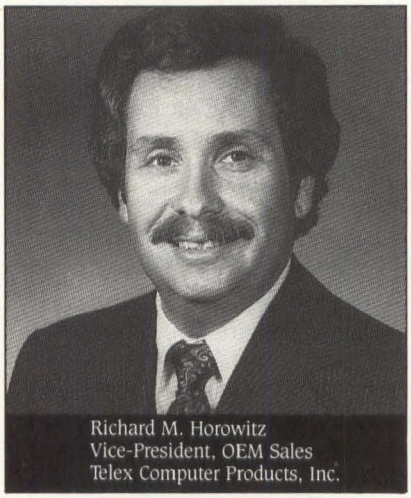

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Pen Plotters With HPGL Emulation

Designed for low-end business graphics, CAD and CAE, these two plotters, the 4550 and 4551, meet the requirements of the HPGL. Both models plot charts, graphs and drawings on paper and transparencies, and both feature removable six-pen cassettes. Ballpoint, water-based ceramic or oil-based fiber-tip pens are available in 8 to 12 colors. Both the 4550 and the 4551 contain RS-232-C Serial and Centronics Parallel interfaces. Prices are $795 (4550) and $995 (4551). **Facit,** Merrimack, NH

Circle 221

19.2 KBPS Compact Data Modem

Operating at 19.2 Kbps, the DSP 19200M Data Modem, packaged in a 12.4″ × 15.4″ × 3.5″ enclosure, features a built-in eight-port data multiplexer, comprehensive diagnostic test capabilities and error correction based on trellis coding technology. The modem operates over four-wire type 3002 leased telephone lines with DI conditioning. Price is $12,000. **NEC America**, Melville, NY

Circle 213

½″ Streaming Magnetic Tape Drive

With a 64-Kbyte cache memory and a MTBF of 7400 hours, this ½″ streaming tape drive, the DMT 2520, is ANSI/IBM-compatible. Storage capacity is 46 Mbytes at 1600 bpi, 92 Mbytes at 3200 bpi (2400′ reel) and up to 138 Mbytes at 3200 bpi (3600′ reel). Features include automatic tape loading and threading, self-diagnostics during power up and a Pertec interface. **Anritsu America**, Oakland, NJ

Circle 162

Video Display Terminal

With an 80 or 132 × 24 display, the ADM 12plus terminal is compatible with the TeleVideo 925, 950, 912 and 920 terminals, and this firm's ADM 2, ADM 12 and the ADM 31. The terminal features programmable cursor keys, a variable format display memory, variable speed vertical scrolling and horizontal scrolling. A 4-page memory option is also available to add a 158-column × 48-line memory format. Price is $745. **Lear Siegler**, Anaheim, CA

Circle 211

Speech Recognition And Touch Pad Keyboards

The Touch Pad keyboard and the Speech Recognition keyboard are two new products added to this firm's line of keyboards. The KB5153 touch pad keyboard allows information selection with a finger touch or a stylus. It provides three pointing modes including cursor key, mouse and absolute, and a function key mode. The KB5152V speech recognition keyboard is plug-compatible with the IBM PC and XT and allows use of a 160-word vocabulary of verbal commands. Speech recogntion works through the keyboard electronics so no software modifications are necessary and no PC adder board is required. The keyboard comes with complete noise canceling microphone, foot switch, vocabulary management software and user's manual. **KeyTronic**, Spokane, WA

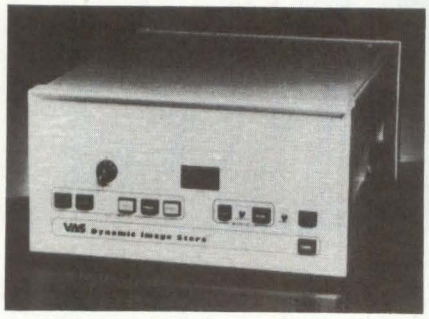
Circle 168

2400 BPS Modem

Bell 103, 212A and CCITT V.22 compatible, as well as internationally (CCITT V.22 BIS) compatible, Scholar, a 2400 bps modem, operates in sync/async mode. With auto dial and voice/data capabilities, Scholar offers modem options from the screen menu, rather than from switches. Also announced are five modular modems, additions to the DF100 Series. They operate at 300/1200, 2400, 4800 and 9600 bps. Price for Scholar is $895. The DF100 Series ranges from $595 to $3,045. **Digital Equipment Corp.**, Maynard, MA

Circle 210

Hard-Disk Video Recorder



The Dynamic Image Store (DIS) video disk recorder is designed for real-time recording on a plated hard disk. DIS provides immediate playback of up to 500 images in real time at 60 fields/sec, as well as slow motion and single-step stop action for image-by-image analysis. **Matrix Instruments**, Orangeburg, NY

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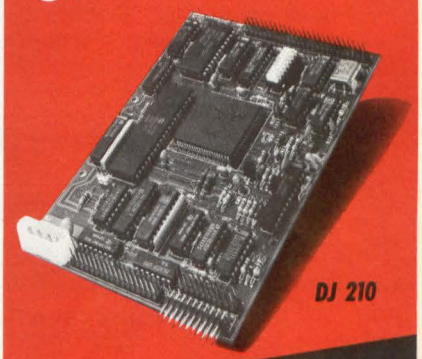

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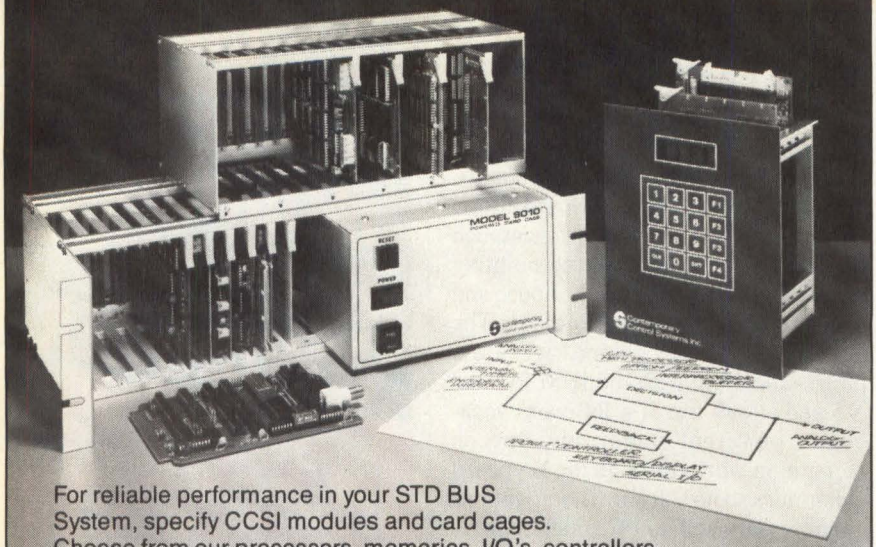

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NEW PRODUCTS

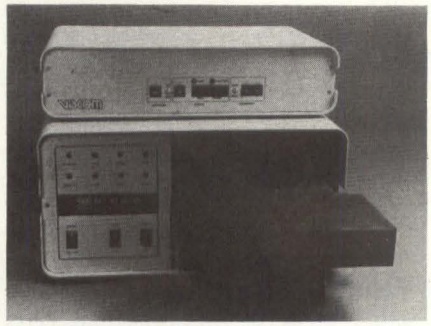
Photoplotter For Micro-Based CAD Systems

Designed for use with microcomputer-based PCB CAD systems, the FP1-1622 photoplotter interfaces directly to the computers via RS-232-C. The FP1 can create one to one precision artwork for PCBs with line width and 12 mils spacing. The plot area is a flatbed with vacuum hold down and accommodates plots of up to 15.5″ × 21.5″. Currently supported by Personal CAD Systems, the FP1-1622 photoplotter is priced at $25,000. **GTCO**, Rockville, MD **Circle 204**

3½″ Compact Winchester Drive

With a maximum unformatted storage capacity of 19.1 Mbytes, these compact 3½″ Winchester disk drives (the DK301 Series) feature high density coated recording media and a low-load head. The Series adopts the ST506/412 standard interface for 5¼″ drives, for convenient switch to 3½″. Price ranges from $750 to $920. **Hitachi,** New York, NY **Circle 206**

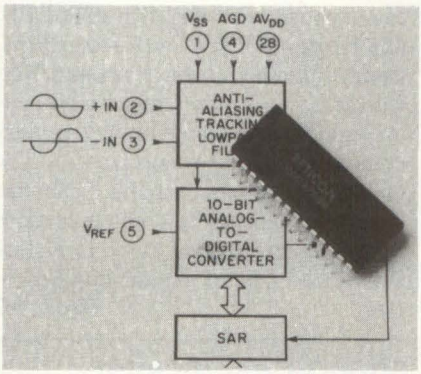
QCR Camera



Registering film within ± .0002″ without registration pins, this precision registered camera and μP controller is designed for the Matrix Instruments QCR film recorder. The Computer Guided Optical Registration (CGOR) offers automatic operation, which electronically notches the film after 36 exposures and starts a new roll count, and manual operation for shooting long rolls of film and discretionary film notching. **Viscom Optical Products**, Costa Mesa, CA **Circle 208**

COMPONENTS

10-Bit ADC Low-Pass Filter Combo



The RT5640 A/D converter with on-chip antialiasing filter works as a complete analog front end for digital signal processors. Containing a fully differential 10-bit linear A/D converter with a sampling rate varying from 20 Hz to 40 kHz, the RT5640 can achieve a user-controlled AGC function through an externally supplied reference voltage. The fully differential seventh order antialiasing filter tracks the conversion rate of the A/D converter; the filter has 0.2 dB of passband ripple and a stopband rejection of more than 60 dB. Price is $22 in 100s. **EG&G Reticon**, Sunnyvale, CA **Circle 133**

256K DRAM With Extended Page Mode

Employing triple-poly technology and laser-fuse redundancy, the MCM6256 is a 262,144-bit DRAM. Page-mode operation allows random column accesses of up to 512 bits within a selected row with page access times of 50 nsec max and page cycle times of 100 nsec max for the MCM6256-10 device. Max page access times for the MCM6256-12 are 60 nsec, and the MCM6256-15, 75 nsec. Page cycle times specify 120 nsec for the MCM6256-12 and 150 nsec for the MCM6256-15. Prices are $26-$36. **Motorola**, Austin, TX **Circle 182**

64K CHMOS EPROM For Military

A military-specified version of the earlier 64K 27C64 CHMOS EPROM, the M27C64 uses from 1/400 to ¼ the power of EPROMs based on HMOS technology, such as the M2764A. The new M27C64 is pin compatible with the M2764A and can use the same programming equipment. The M27C64 also provides radiation immunity of the M2764A because of similar geometries. Available in 250 nsec and 350 nsec versions, their prices in 1,000s are $107 and $59, respectively. **Intel**, Santa Clara, CA **Circle 181**

Controller For Group 4 Facsimile/X.25 Communications

Handling all link-level operations of the Group 4 facsimile, as well as CCITT X.25 serial data communications standard, the WD2511F MOS/LSI device is a bit-oriented controller, which automatically manages several packet buffers, acknowledges error free packets and requests packets containing errors to be retransmitted. The device also offers built-in channel DMA, zero-bit insert and delete, auto appending and testing of FCS field and TTL compatibility. **Western Digital**, Irvine, CA **Circle 177**

Three-Port Hybrid Isolation Amplifier

Combining ±2500V of transformer-coupled isolation and ±0.012% max nonlinearity, this hybrid isolation amplifier uses two internal transformers to provide three-port isolation between the input, output and power supply ports. The AD295 is available in three grades: ±0.05%, ±0.025% and ±0.012% max nonlinearity; ±450 μV/°C, ±300 μV/°C, and ±150 μV/°C max output offset voltage drift; ±10 μV/°C, ±3V/°C, ±1.5V/°C max input offset drift. Other key specs are ±1.5% typical gain accuracy, ±60ppm/°C max gain drift, ±18 mV max output offset voltage, and ±3 mV max input offset voltage. **Analog Devices**, Norwood, MA **Circle 128**

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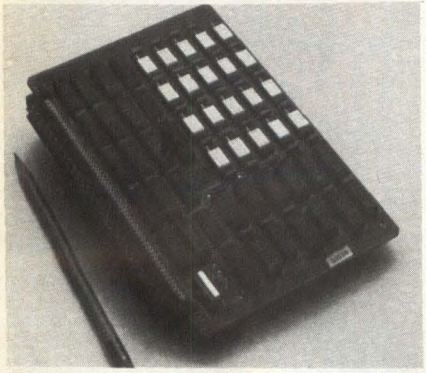
BOARDS

Graphics Display Generator



Built to MIL-E-16400 requirements, this graphics display generator, CombatView, features a graphics instruction set, a dedicated Schottky μP and a 16-bit ALU. Resolutions of either 640 × 512 or 1280 × 1024, interlaced or noninterlaced, are available. CombatView provides black and white to multicolor displays up to 64-bit planes for configuration in any military environment. **Liacom**, Marlboro, MA **Circle 147**

3-Mbyte Memory Board For PC AT

Providing up to 3 Mbytes of RAM for the IBM PC AT, the Mega Memory is a full-size printed circuit board that fits into any of the 16-bit slots of the AT. A total of 6 banks, representing 12 rows, can be populated using either 64K or 256K chips, depending on the configuration. Standard with the board are the Wait-Less Printing and Insta-Drive Software packages. Price is $395 to $5,495. **Emulex**, Costa Mesa, CA **Circle 192**

Analog Input Module

An intelligent, self-continued single-board micro system, Scadar Series 10 is complete with memory, power supply and I/O. It interfaces to IBM PCs, Intel 310/A, DEC LSI-11, PDP-11, VAX, HP-3000 and other hosts through RS-232 and TTY current loop ports. Eight differential inputs are provided, each with a detection range of ±10 VDC and overvoltage protection to ±16 VDC. Price is $2,500. **Burr-Brown**, Tucson, AZ **Circle 198**

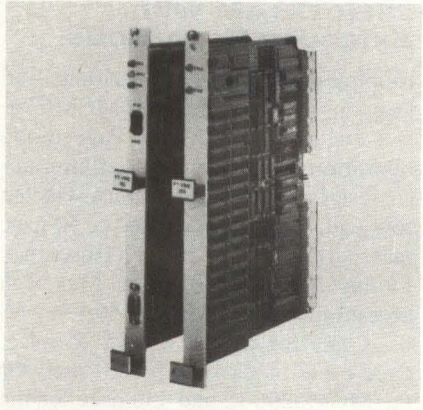
16-Bit S-100 Based Slave Processor

Designed to operate with 8- and 16-bit Master CPUs, the Super 16 Slave Processor comes with an 8 MHz 80186 CPU, 256 Kbytes of RAM and 4 serial ports. Running under Turbo DOS and Network/OS, the Super 16 features Master-to-Slave, 8-bit/16-bit memory to memory communication, I/O status port, 4K/32K of EPROM, programmable baud rate generator, sync/async communications and real-time clock. Price is $1,195. **Advanced Digital**, Huntington Beach, CA **Circle 197**

68000-Based Octal Serial Board

An addition to the firm's ModulasTen line of Multibus products, this octal serial board, the M68COM, provides eight independent full-duplex channels and contains the 16/32-bit 68000 or 68010 MPU. Running at 10 MHz with no wait states for memory reads or writes, the M68COM includes an optional 10 MHz 4-channel DMA controller. The board supports X.25, SDLC, HDLC and Bi-sync protocols. Price is $1,595. **SBE**, Concord, CA **Circle 200**

VMEbus Processor With VMX Bus Port



An enhanced version of the PT-VME100 VME processor, the PT/VME103 VME/VMX processor module uses a 10 MHz 68010 virtual memory processor in conjunction wih a 68451 MMU. Room for a second MMU is provided, and the module will support a 68881 floating point processor. Some features include conformance to the VMX Revision B specification, VMEbus 24-bit address and up to 128K ROM and 32K RAM or an additional 128K ROM on-board. **Performance Technologies**, East Rochester, NY **Circle 149**

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5¼" Floppy Controller For Multibus

Using the FD 1791 controller, this 5¼" floppy disk controller controls up to four single- or double-density floppy drives. Write data is precompensated and DMA logic is included to allow data transfers to any 16M locations in the system memory. Complete with a phase locked loop data separate and a 34-pin locking flat ribbon cable connector, its price is $280 in 100s. **Central Data**, Champaign, IL **Circle 199**

VMEbus Board Set

Centering around a cache-based M68000/M68010 CPU board, this VMEbus product line includes a system controller board, an EPROM/SRAM board and a 512 Kbyte DRAM board. The board set is packaged on the single height VME form factor. The CPU board uses a cache scheme like the M68020 and provides 1 Kbyte on-board and cache memory, and each has an 8, 10 and 12.5 MHz M68000 or M68010. Prices begin at $1,095 in 25s. **Microcosm**, Beaverton, OR **Circle 195**

IBM PC Quick Vector Processor

Built around the 68000, the QVP (Quick Vector Processor) accepts vector data as input and produces raster data to drive high resolution color film recorders and other hardcopy devices. Accepting data input coordinates in a 32,768 × 32,768 (15-bit) data space, the QVP comes with the SCODL (Scan Conversion Object Description Language). A total of 256 colors can be used in one image from a palette of 16M possible colors. **Matrix Instruments**, Orangeburg, NY **Circle 203**

68020 Supermicrocomputer On Multibus

Featuring the 68020, this 32-bit processor board, the MAP-2000, and the MB-2000 2-Mbyte companion memory board offers 32-bit supermini performance (VAX 11/780) on two boards. Using the dedicated 32-bit memory expansion bus, the MAP-2000 can access up to 8 Mbytes of memory. Additional on-board resources include up to 512 Kbytes of ROM, 128 Kbytes of zero wait state RAM, a real-time clock with battery backup, 16 levels of vectored interrupts, two RS-232 serial ports and bus interfaces to the Multibus, iLBX Bus and the 32-bit Matrox MX-bus. **Matrox**, Quebec, Canada **Circle 196**

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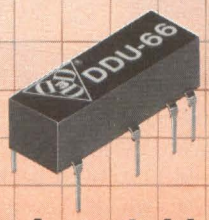

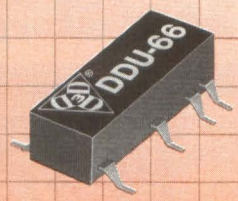

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80188-Based Multibus-Compatible SBC

Based on the 80188 CPU, operating at 8 MHz, this single-board computer has 16 JEDEC 28-pin memory sockets. 96K to 128 Kbytes of RAM are available. As a system, the MP85188 includes the 80188 CPU, clock, RAM, EPROM, EEPROM, serial I/O, parallel I/O, interrupt controller, timers, watchdog security timer, user-defined board status I/O and SBX expansion. Price is $1,495. **Burr-Brown**, Tucson, AZ **Circle 191**

IBM PC Multifunction/ Display Combo Boards

Designed as IBM PC, XT, AT and compatible enhancement boards, the Persyst Mono Combo Card and Color Combo Card achieve multifunction and display on a single board. The combo boards offer up to 384K of expanded memory. Multifunction features include a parallel printer port with bidirectional capabilities. A serial port connects to any async modem. Byte parity is provided, and the boards have switch selectable starting addresses of 128 Kbytes, 256 Kbytes and 384 Kbytes. Insta-Drive and Wait-Less Printing Software programs are included. Prices start at $520. **Emulex**, Costa Mesa, CA **Circle 201**

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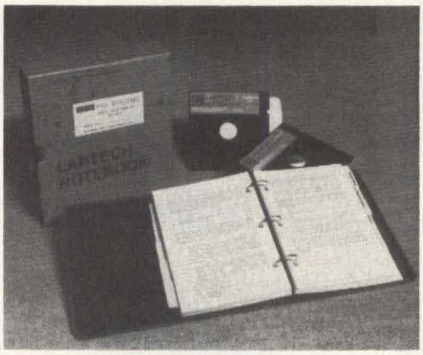
SOFTWARE

Component/Semicustom IC Libraries

These three component libraries and two semicustom IC libraries are designed to work with the firm's PCB software. They include the CMOS family components library which includes 150 standard components from Motorola's 14000 series of ICs; the μP components library containing 150 components from the Intel family of microsystem components; and the discrete device components library, drawn from various manufacturers, which has about 100 components, including resistors, capacitors, transistors and others. The semicustom IC libraries are the Motorola ALS-TTL macrocell array library and the Motorola CMOS macrocell array library. All cost $500 each. **P-CAD**, San Jose, CA **Circle 170**

Software For IBM PC Instrumentation Systems



Designed to support the PCI-4301 series single board I/O system on the IBM PC, the PC-4901-1 software package provides subroutines which allow a user to write application software in BASIC. It consists of three parts: a BASIC callable routine package, a reference table to define I/O points and an edit program to allow users to update the reference table. The reference table is used to define such things as gain, data format and engineering units for the I/O points. **Burr-Brown**, Tucson, AZ **Circle 173**

SPICE Circuit Simulator

The Simon Simulator is based on algorithms created specifically for the simulation of MOS and CMOS circuits and is not a SPICE derivative. Written originally to simulate bipolar circuits and later adapted for MOS technology like SPICE and SPICE derivative simulators, Simon can accept existing SPICE-coded network files. The company quotes the new simulator as operating as fast as 50× the speed of SPICE and guaranteed to converge the first time it is run. **ECAD**, Santa Clara, CA **Circle 172**

Turbo Pascal 3.0 With Graphics, BCD Options

Turbo Pascal 3.0 now has added graphics, optional BCD support, I/O redirection and a memory mapped editor. The Turbo Pascal language environment includes a single-pass native code compiler, full-screen editor with Wordstar-like commands, run time error checking, commented source code and a MicroCalc spreadsheet. Requiring 35 Kbytes of memory, Turbo 3.0 is available for micros running MS/DOS, PC/DOS, CP/M 80 or CP/M 86. Price is $69.95 **Borland International**, Scotts Valley, CA **Circle 171**

μP Development Tools For ULTRIX

BSO's family of μP development tools is now available for DEC's line of VAX computers operating under the ULTRIX operating system. Full support is available for the Intel 80186, 8087 and 8051, the Motorola 68000/010 and 6809 and the Zilog Z80 and Z8000. The development tools include C, Pascal and PL/M compilers, macro assemblers, symbolic debuggers and communication packages and are available under ULTRIX or UNIX 4.2. **Boston Systems Office**, Waltham, MA **Circle 217**

SDLC PC-To-PC Communications Software

Allowing IBM PCs to communicate with each other using the SNA/SDLC protocol, the Adapt SNA PCcom software package provides complete file transfer capabilities between PCs. Files on the secondary PC can be renamed or deleted remotely via the primary PC. It runs on an IBM PC, XT, AT or compatible with 128K memory, one diskette or hard disk drive, one IBM SDLC adapter card and a synchronous modem. Price is $475. **Network Software Associates**, Irvine, CA **Circle 220**

NEW PRODUCTS

Modula-2 Developers System

The Pinnacle/MOSYS Development System includes the Motorola-2 operating system and a 68000 native code compiler, a document processor, a library and utilities, and a screen editor. Standard hardware features in the developers package include 256 Kbyte RAM, a 10 Mbyte hard disk, seven serial ports and one parallel port. The Pinnacle 12 MHz 68000 executes 3 MIPS with a zero wait state RAM of up to 8 Mbytes. Price for the package is $3,995. **Pinnacle Systems**, Dallas, TX **Circle 219**

PCB Layout Software

The Auto-Router is a collection of software tools and circuit element templates that aid in the layout and trace routing of a double-sided PCB. Currently running on most MS-DOS machines, the output of the Auto-Router is a complete definition of the PCB, including silk screen and drilling patterns, as a script file to the AutoCAD mechanical drawing program. The software can route a 20″ by 20″ PCB, perform traces routed on 50 mil centers, provide for buses of variable sizes, allow for creation and use of custom parts and more. Price ranges from $995 to $1,499. **The Great Soft-Western Co.**, Denton, TX **Circle 218**

Data Security Software

Written in C for IBM PCs and compatibles, this menu-driven data security program, Comsafe-X, is designed for data communication and information management. In networks, it can communicate privately with another party, assure the authenticity of received data, create and verify electronic digital signatures, verify the source of a received message, implement an electronic mail system and protect data from disclosure. Price is $500 per user. **RSA Security,** Sunnyvale, CA **Circle 216**

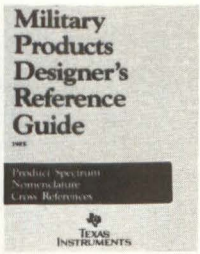
Symbolic Simulator For 8086/87/80186

A high-level language-oriented simulator for debugging and analyzing programs written for the Intel 8086/87/80186 μP SoftProbe/87 provides 8087 numerical coprocessor simulation. SoftProbe/87 can be hosted on VAX under VMS or UNIX, or any 68000-based supermicro running UNIX System III, V and BSD 4.2 operating system. Supporting Intel-compatible language processors, SoftProbe/87 accepts MCS-86 executable code module as input. License starts at $6,750. **Systems & Software**, Costa Mesa, CA **Circle 214**

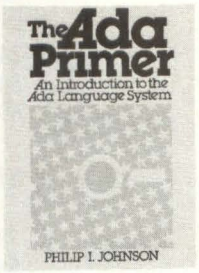
3D CAD/Drafting System

Suited for the IBM PC family, the interactive 3D CAD and drafting system, the 3-D Graphixx CADD System, is capable of 3D imaging/modeling, technical graphics, production drafting CAE, animation, slide show and more. The system includes a variety of options like 19″ color workstations and A-E size plotter support. 3-D Graphixx comes with color selection per vector, menu operations, 2D and 3D editing, graphics word processing, math function graphics generation with hidden lines removed, multilayering and auto scale/auto dimensioning. Price is $2,995 (IBM PC) and $3,995 (PC/AT). **Universal Intergraphix**, Ontario, CA **Circle 215**

NEW LITERATURE



Military Reference Guide. Over 900 devices are featured in the Military Products Designer's Reference Guide, a free 100-page manual from Texas Instruments. The guide provides four product Sections, Logic, Linear and Interface, Bipolar Memory and MOS Memory, along with a section on the SBR9989 16-bit military μP. Product descriptions for AS, ALS, CMOS and LinCMOS are included with complete graphs and charts.
Texas Instruments **Circle 261**

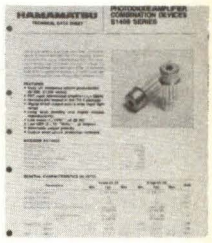


The Ada Primer. In his book, *The Ada Primer: An Introduction to the Ada Language System*, Philip I. Johnson examines Ada as a program design language that is easy to learn, lends itself to effective management and reduces costs. Assuming prior knowledge of high-level programming languages (e.g., Fortran and COBOL), Johnson introduces Ada's techniques for describing and typing data, its subprogram concepts, its approaches to parallel real-time operations and its package concept for program modules.
McGraw-Hill **Circle 256**

CRT Brochure. With descriptions of photorecording and projection CRTs and their applications, this six-page brochure from RCA Tube Operations presents technical data and schematic diagrams. Specifications include deflection angle anode voltages, electrode and grid voltages, line width, luminance and emission wavelength. Four-color charts and a CIE color designation chart are also provided.
RCA **Circle 263**

Digital Filtering Application Note. Dealing with digital filtering and two different structures of finite impulse response (FIR) digital filters, this application note from TRW LSI Products Division, *An Introduction To Two Different FIR Structures*, summarizes the tapped delay line signal flow structure for FIR filters. It also offers an alternative method: the Frequency-Sampling structure, which can be outlined in hardware time-multiplexed with Infinite Impulse Response (IIR) filters because of the similarity between the two forms.
TRW **Circle 254**

Photodiode/Amplifier Data Sheet. Hamamatsu has published a technical data sheet detailing characteristics, spectral response, specifications and operating instructions of its S1406 series photodiode/amplifier combination devices. These recently introduced devices incorporate a UV enhanced silicon photodiode chip and a FET input operational amplifier in a TO-5 package. The four-page data sheet is fully illustrated.
Hamamatsu **Circle 262**



APPGEN Software Directory. The APPGEN library of fourth generation UNIX software is covered in this Directory from Software Express. Included are 45 vertical market applications that run on the 50 machines to which the Software Express development environment is currently directed. They range from superminis like the IBM PC/AT to mainframes such as Amdahl. The Directory is $10 and will be updated quarterly.
Software Express **Circle 255**

CALENDAR

August 1-2

Integrated Logistics Support Seminar. Washington, DC. Contact: Technical Transfer Society Seminars, c/o Technology Training Corp., Dept. ILS/LSA, PO Box 3608, 3420 Kashiwa St., Torrance, CA 90510-3608. (213) 534-3922.

August 4-8

ASME International Computers In Engineering Conference. Boston, MA. Contact: Mary Benedict, American Society of Mechanical Engineers, 345 East 47th St., New York, NY 10017. (212) 705-7100.

August 5-7

The IBM PC Seminar. Washington, DC. (four other dates and locations) Contact: Data-Tech Institute, Lakeview Plaza, PO Box 2429, Clifton, NJ 07015. (201) 478-5400.

August 5-9

Fiber Optic Communication Systems Course. Santa Barbara, CA. Contact: University of California Extension, Santa Barbara, CA 93106. (805) 961-4200.

August 5-9

Contemporary Data Communication Networks: Planning, Management And Computer-Based Design Course. Ann Arbor, MI. Contact: Dixon R. Doll, Engineering Summer Conferences, 400 Chrysler Center, North Campus, University of Michigan, Ann Arbor, MI 48109. (313) 971-5234.

August 12-14

Data Communications: Network Design, Integration and Applications. Los Angeles, CA. Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

August 13-15

Computer Graphics '85 East. Boston, MA. Contact: National Computer Graphics Association, PO Box 3412, McLean, VA 22103. (800) 225-6242.

August 13-15

Systems Network Architecture And Implementation Seminar. Boston, MA. (six other dates and locations) Contact: CSI, 992 South Saratoga-Sunnyvale Rd., San Jose, CA 95129. (408) 725-1568.

August 14-16

Structured Systems Development With 4th-Generation Languages Seminar. Denver, CO. Contact: Software Institute of America Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

August 20-22

Designing With Single Chip Microcomputers Course. Boston, MA. (Chicago, IL—Oct. 15-17) Contact: Hughes Institute, PO Box 17968, Milwaukee, WI 53217-0968. (414) 271-1266.

August 21

Applied Data Communications Seminar. Chicago, IL. (several other dates and locations) Contact: UDS Representative, Instrument Dynamics, PO Box 584, Wakefield, MA 01880. (205) 837-8100, ext. 306.

August 26-28

PC FAB Expo '85 Technical Seminar And Trade Show. Boston, MA. Contact: Julia Wilson, PC FAB Expo '85/Boston, 1790 Hembree Rd., Alpharetta, GA 30201. (404) 475-1818.

September 5

15th US Invitational Computer Conference (ICC). Newton, MA. (several other dates and locations) Contact: B.J. Johnson & Assoc., 3151 Airway Ave., #C-2, Costa Mesa, CA 92626. (714) 957-0171.

September 10-12

CADCON. Boston, MA. Contact: Steve Schuldenfrei, Morgan-Grampian Exposition Group, 1050 Commonwealth Ave., Boston, MA 02215. (617) 232-EXPO.

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