Integrated Circuit Databook

PLESSEY
SEMICONDUCTORS

digital integrated circuits

NOVEMBER 1979

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

$3.00

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DEVICE TYPE

SP8000 SERIES HIGH SPEED DIVIDERS

Prescalers

SP4000 SERIES HIGH SPEED DIVIDERS

Prescalers

NOVOL

Non-Volatile Logic

Two-modulus Programmable Dividers

Modulus Extenders

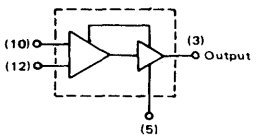
SP9000 SERIES DATA CONVERSION PRODUCTS

High Speed Comparators

technical data

VOLTAGE-CONTROLLED OSCILLATOR

SP1648



Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silcon chip. Output levels are compatible with PECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The SP1648 is used in the Phase-Locked Loop shown in Figure 9. This device may be used in many applications requiring a fixed or variable frequency clock source of high spectral purity (See figure 2).

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC

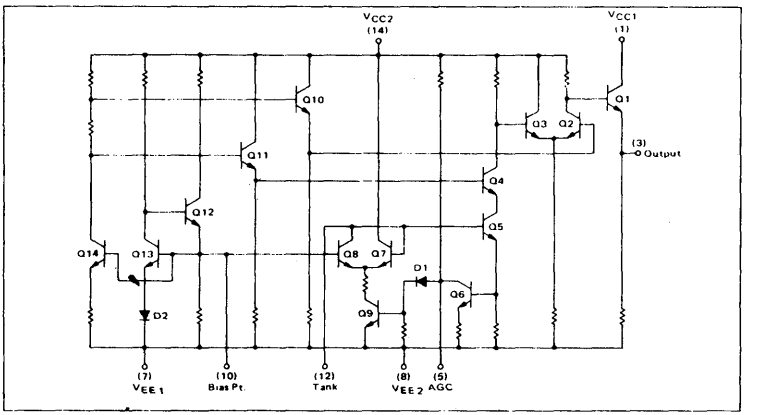
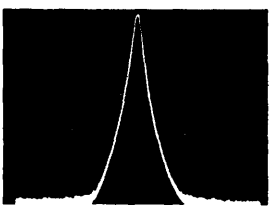
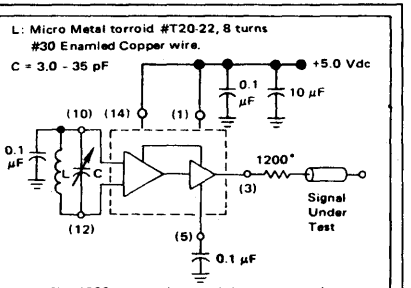


FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



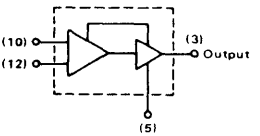
B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts



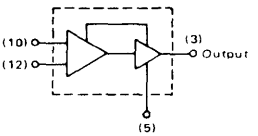
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+85°C	+1.680	+1.180	5.0	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	40	—	—	mAdc	—	—	1, 14	—	7, 8
Logic '1' Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1, 14	3	7, 8
Logic '0' Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1, 14	—	7, 8
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak to Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 3	—	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 3	—	1, 14	3	7, 8
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 3	—	1, 14	3	7, 8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 volts

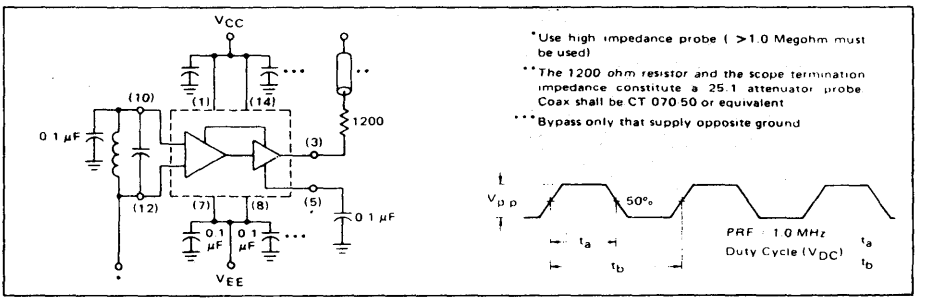


@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.300	-3.800	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.500	-4.000	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	41	—	—	mAdc	—	—	7, 8	—	1, 14
Logic '1' Output Voltage	V_{OH}	3	-1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7, 8	3	1, 14
Logic '0' Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7, 8	—	1, 14
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak to Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 3	—	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 3	—	7, 8	3	1, 14
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 3	—	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



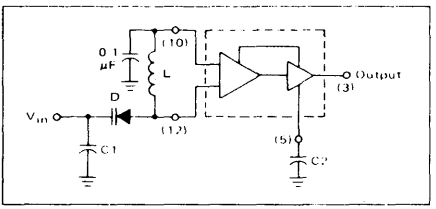
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

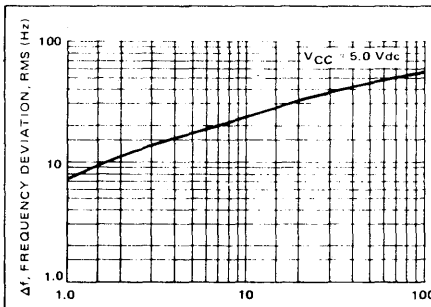
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

FIGURE 4 – THE SP1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



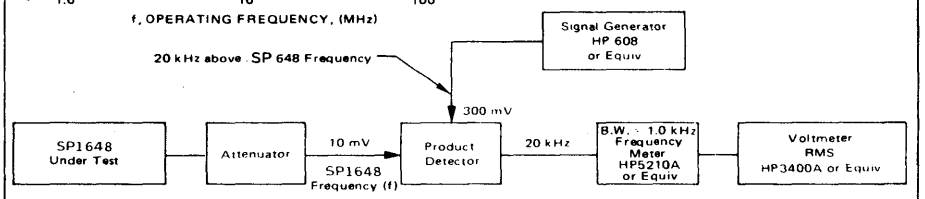
When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L µH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimized prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE
USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

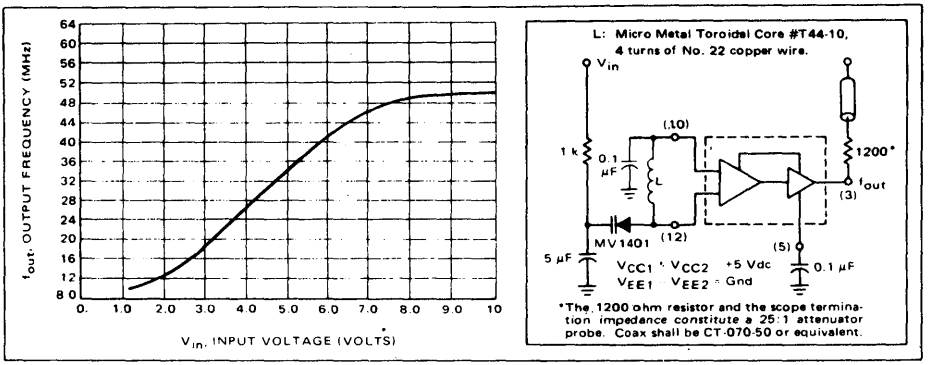


FIGURE 7

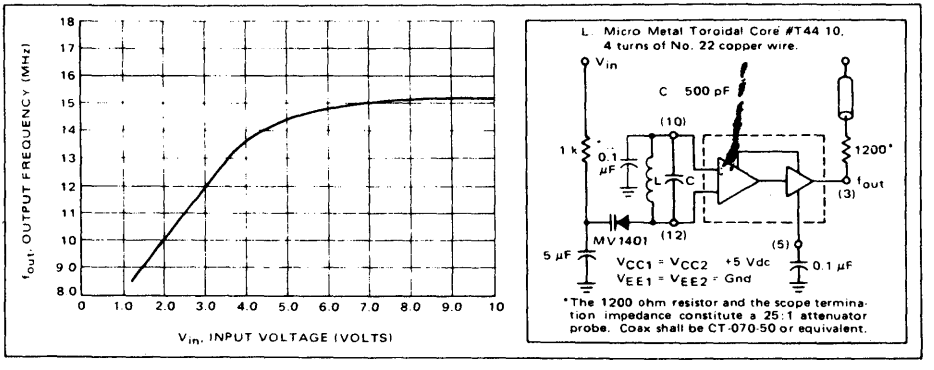
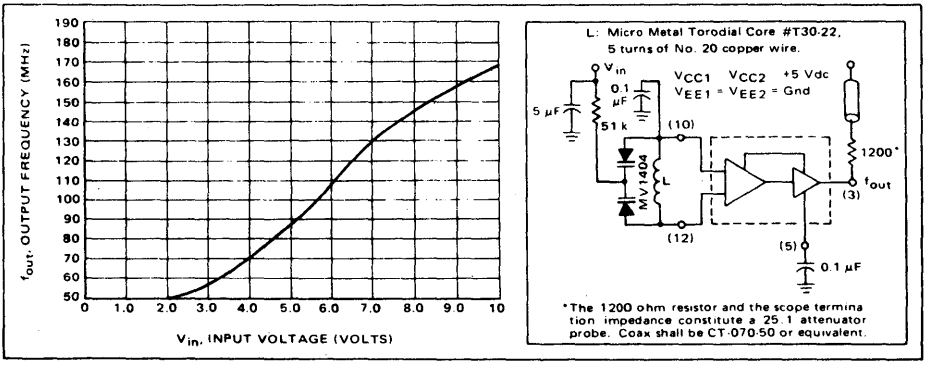


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\ (C_D\ (max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the SP1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

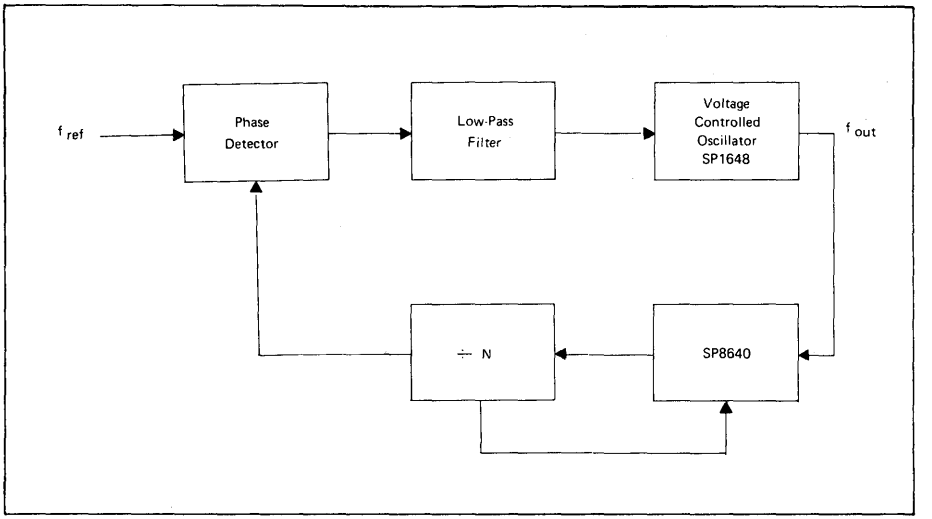


Figure 10 shows the SP1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the SP1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the SP1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the PECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

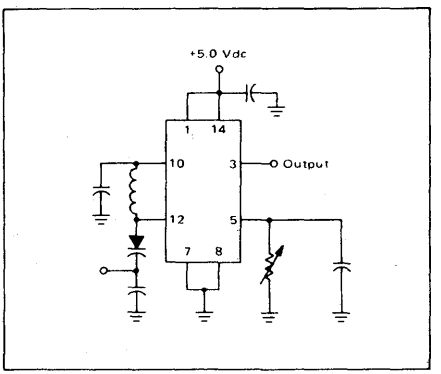


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE SP1648 (SQUARE WAVE OUTPUT)

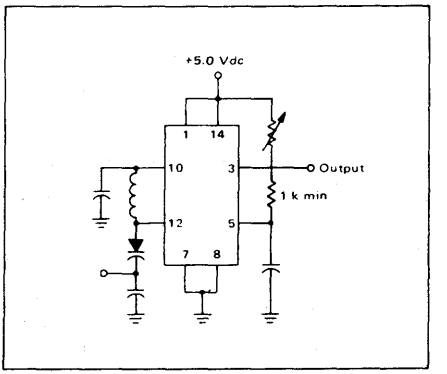


FIGURE 12 – CIRCUIT SCHEMATIC USED FOR COLLECTOR OUTPUT OPERATION

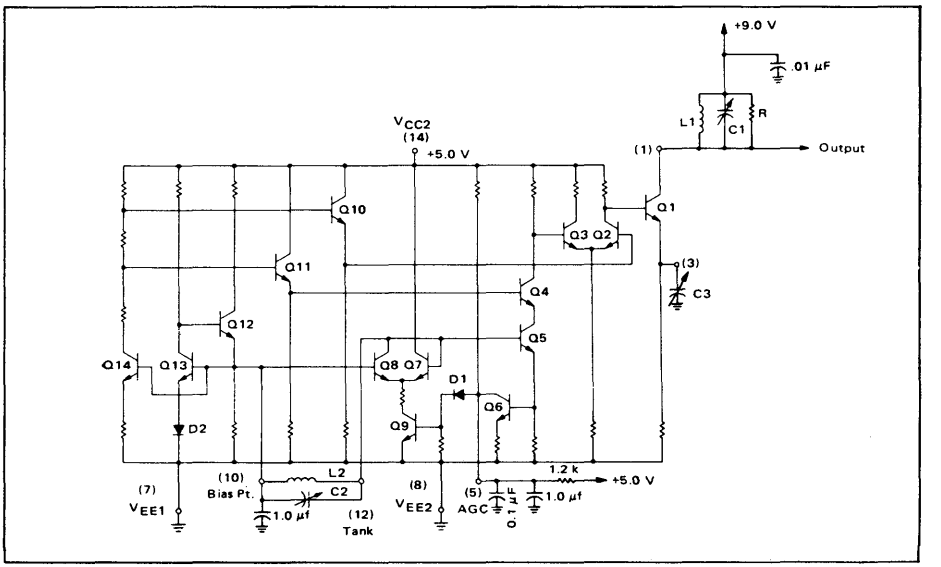


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 100 MHz
C3 = 3.0 - 35 pF
Collector Tank
L1 = 0.22 μH C1 = 1.0 - 7.0 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 11 kΩ @ 100 MHz Resonance
Oscillator Tank
L2 = 4 turns #20 AWG 3/16" ID
C2 = 1.0 - 7.0 pF

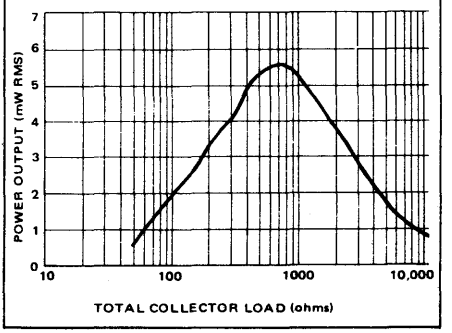
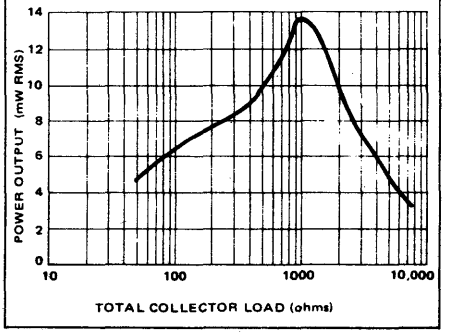


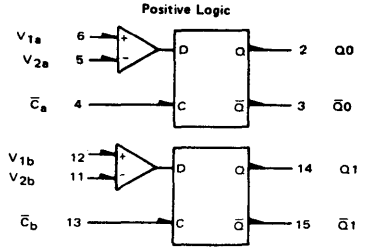
FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 10 MHz
C3 = 470 pF
Collector Tank
L1 = 2.7 μH C1 = 24 - 200 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 6.8 kΩ @ 10 MHz Resonance
Oscillator Tank
L2 = 2.7 μH
C2 = 16 - 150 pF



DUAL A/D COMPARATOR

SP1650 • SP1651



V_{CC} = +5.0 V = Pin 7,10
V_{EE} = -5.2 V = Pin 8
Gnd = Pin 1,16

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (SP1650)
  = 3.0 ns typ (SP1651)
- Input Slew Rate = 350 V/μs (SP1650)
  = 500 V/μs (SP1651)
- Differential Input Voltage:
  -5.0 V to +5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (SP1650)
  -2.5 V to +3.0 V (-30°C to +85°C) (SP1651)
- Resolution: ⩽20 mV (-30°C to +85°C)
- Drives 50 Ω lines

The **SP1650** and the **SP1651** are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The **SP1650** provides high impedance Darlington inputs, while the **SP-1651** is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from PECL III or PECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

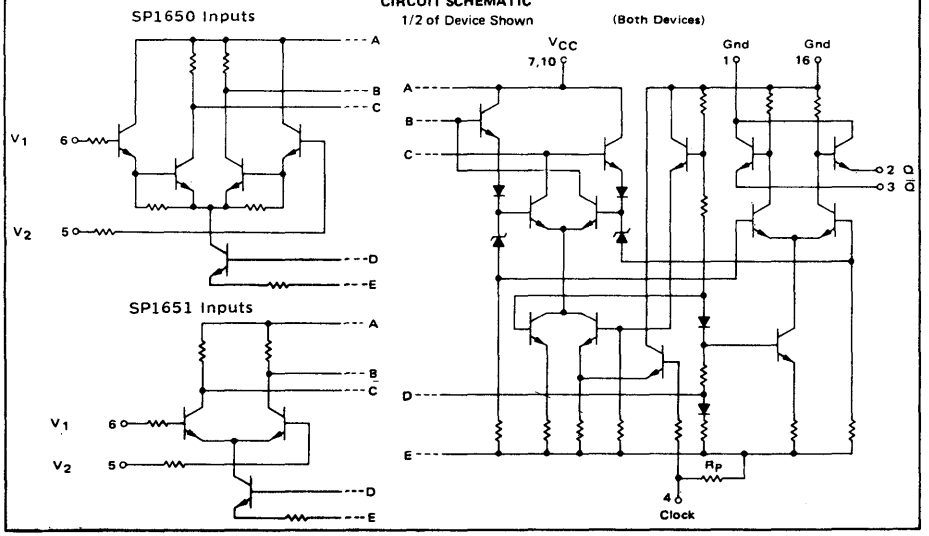
Assessment of the performance differences between the **SP1650** and the **SP1651** may be based upon the relative behaviors shown in Figures 3 and 6.

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

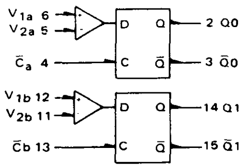
CIRCUIT SCHEMATIC
1/2 of Device Shown (Both Devices)



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB *or equivalent) or a transverse* air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

POSITIVE LOGIC



CERAMIC PACKAGE E

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
	TEST VOLTAGE VALUES (Volts)											
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10	–	–	–	25*	–	–	mAdc	–	4,13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Negative	I_E	8	–	–	–	55*	–		mAdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Input Current	I_{in}																					
SP1650		6	–	–	–	10	–		μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
SP1651		6	–	–	–	40	–		μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
SP1650		6	–		–	7	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
SP1651		6	–	–	–	10	–		μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
Input Clock Current	$I_{in}H$	4	–	–	–	350	–	–	μAdc	4	13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
	$I_{in}L$	4	–	–	0.5	–	–	–	μAdc	–	13	–	–	6,12	–	–	–	–	–	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
		2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	5,11	–	–	–	–	↓	↓	1,6,12,16
		2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	6,12	5,11	–	–	↓	↓	1,16
		2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	5,11	6,12	↓	↓	1,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	6,12	–	–	–	–	↓	↓	1,5,11,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	5,11	–	–	–	–	–	↓	↓	1,6,12,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	5,11	6,12	–	–	↓	↓	1,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	6,12	5,11	↓	↓	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	–	–	–	–	6,12	–	–	–	–	7,10	8	1,5,11,16
		2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	5,11	–	–	–	–	–	↓	↓	1,6,12,16
		2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	5,11	6,12	–	–	↓	↓	1,16
		2	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	6,12	5,11	↓	↓	1,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	6,12	–	–	–	–	–	↓	↓	1,5,11,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	5,11	–	–	–	–	↓	↓	1,6,12,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	6,12	5,11	–	–	↓	↓	1,16
		3	↓	↓	↓	↓	↓	↓	↓	↓	–	–	–	–	–	–	–	5,11	6,12	↓	↓	1,16
Logic "1" Threshold Voltage ② 1	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
2		2	↓	–	↓	–	↓	–	↓	–	↓	–	4	–	6	–	–	–	–	↓	↓	↓
3		3	↓	–	↓	–	↓	–	↓	–	↓	4	–	–	6	–	–	–	–	↓	↓	↓
4		3	↓	–	↓	–	↓	–	↓	–	↓	–	4	6	–	–	–	–	–	↓	↓	↓
Logic "0" Threshold Voltage ② 1	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
2		3	–	↓	–	↓	–	↓	↓	–	↓	–	4	–	6	–	–	–	–	↓	↓	↓
3		2	–	↓	–	↓	–	↓	↓	–	↓	4	–	–	6	–	–	–	–	↓	↓	↓
4		2	–	↓	–	↓	–	↓	↓	–	↓	–	4	6	–	–	–	–	–	↓	↓	↓

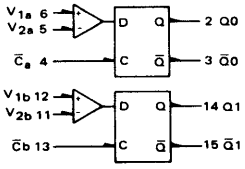
NOTES ① All data is for ½ SP1650 or SP1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired) $|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
SP1650	+3.000	+2.980	-2.500	-2.480
SP1651	+2.500	+2.480	-3.000	-2.980

SWITCHING TIMES

POSITIVE LOGIC



CERAMIC PACKAGE E

❶ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

See Figure 2

Characteristic	Symbol	Pin Under Test	SP1650/1651 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2								–	–	5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| \leq 12$ Vdc.

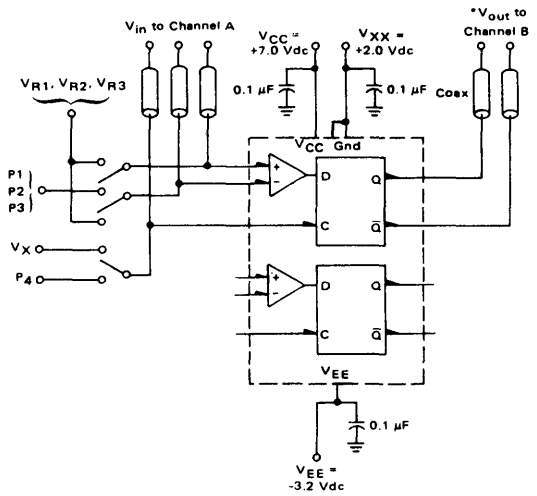
② Unused clock inputs may be tied to ground.

③ See Figure 8.

④

All Temperatures	V_{R2}	V_{R3}
SP1650	+4.900	-0.400
SP1651	+4.400	-0.900

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



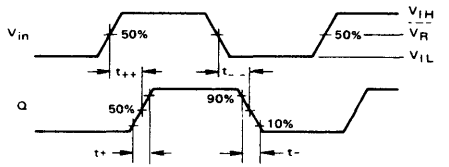
50-ohm termination to ground located in each scope channel input
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

*Complement of output under test should always be loaded with 50-ohms to ground.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

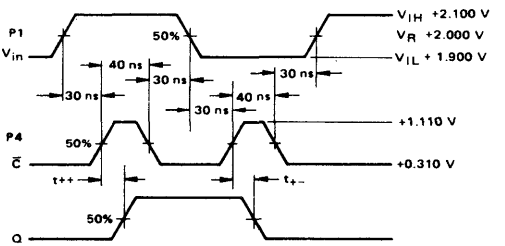


Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

TEST PULSE LEVELS

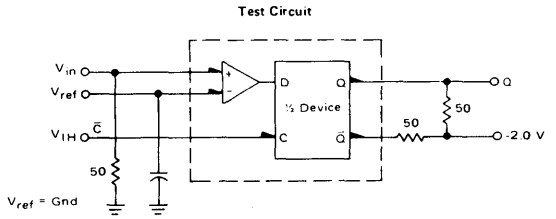
	Pulse 1		Pulse 2		Pulse 3	
	SP1650	SP1651	SP1650	SP1651	SP1650	SP1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

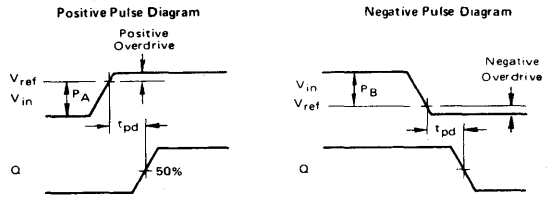
Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns.

FIGURE 3 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE





Input switching time is constant at 1.5 ns (10% to 90%).

Propagation Delay versus Pulse Amplitude

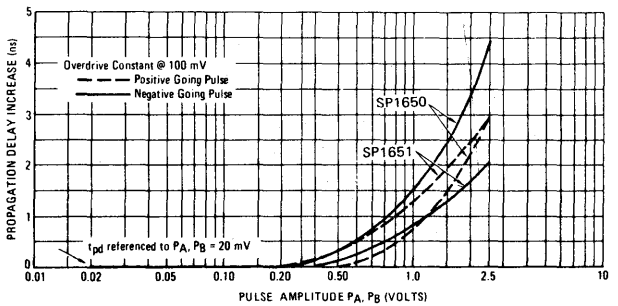


FIGURE 3 (continued)

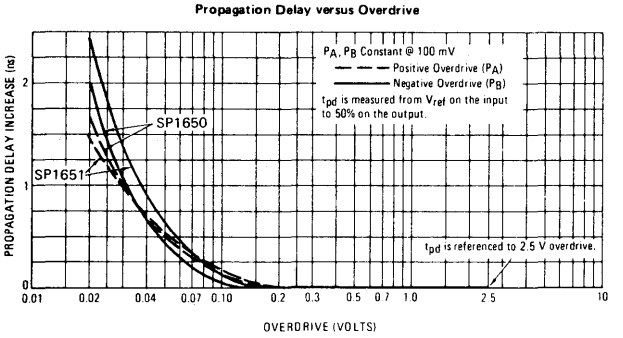


FIGURE 4 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

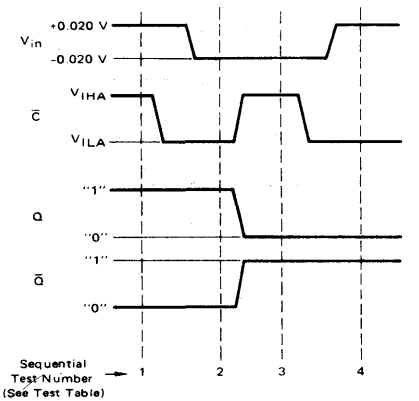
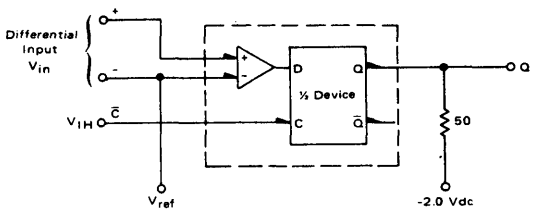


FIGURE 5 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ Vdc \leqslant V_{ref} \leqslant +2.5\ Vdc$

Typical Transfer Curves

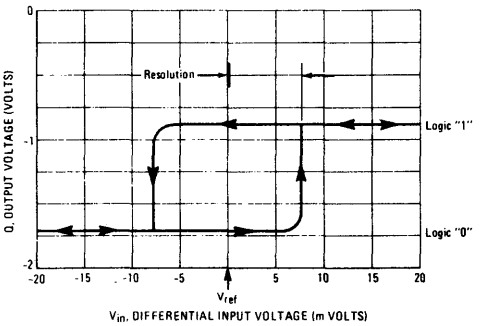
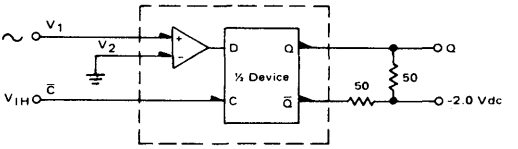
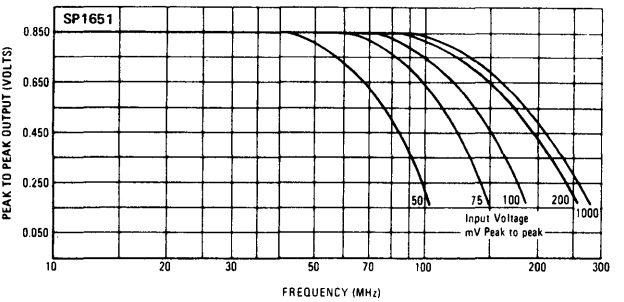


FIGURE 6 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



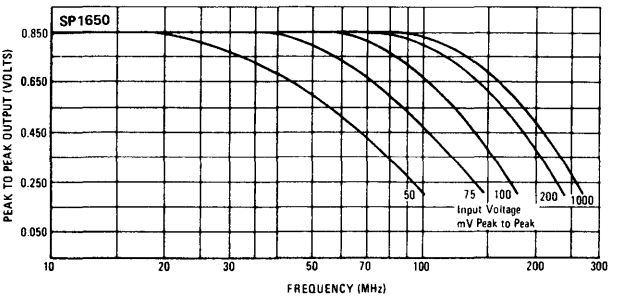
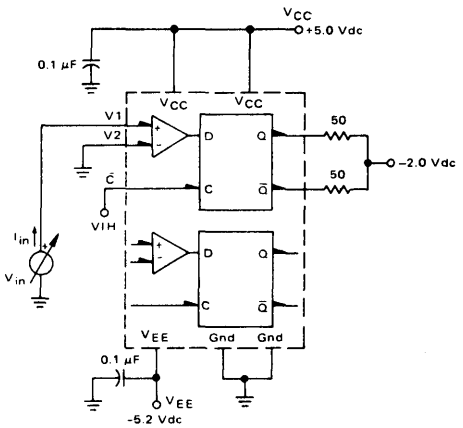
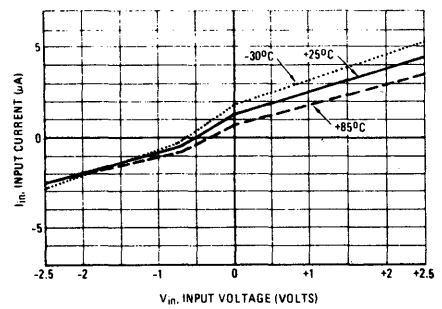


FIGURE 7 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



Typical SP1650 (Complementary Input Grounded)



Typical SP1651 (Complementary Input Grounded)

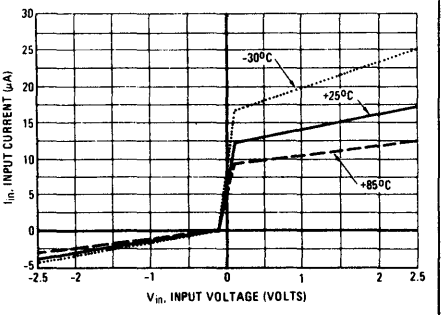
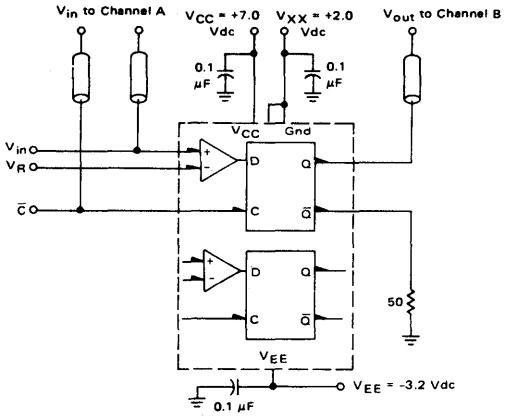


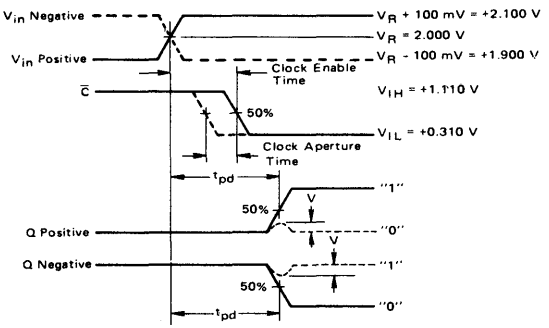
FIGURE 8 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case

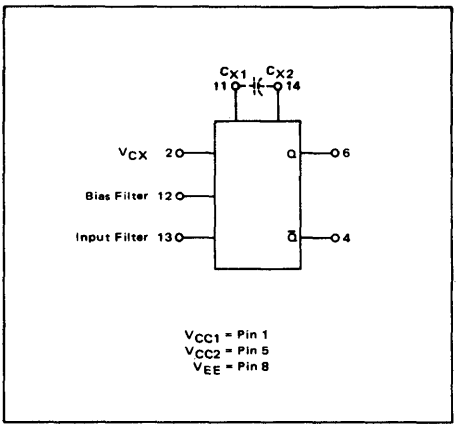


——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

VOLTAGE-CONTROLLED MULTIVIBRATOR

SP1658

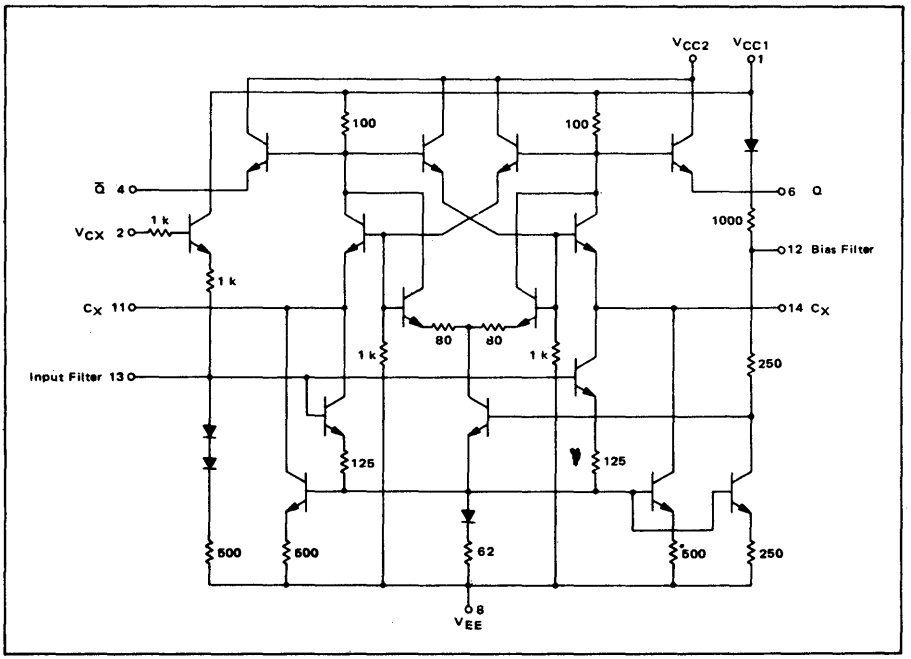


The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with PECL, III and PECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

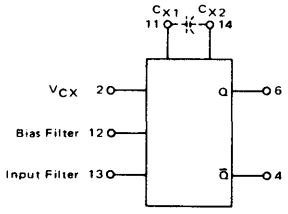
FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

CERAMIC PACKAGE E



@ Test Temperature	TEST VOLTAGE VALUES (Vdc ±1%) V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
-30°C	0.0	-2.0	-1.0	+2.0	-5.2
+25°C	0.0	-2.0	-1.0	+2.0	-5.2
+85°C	0.0	-2.0	-1.0	+2.0	-5.2

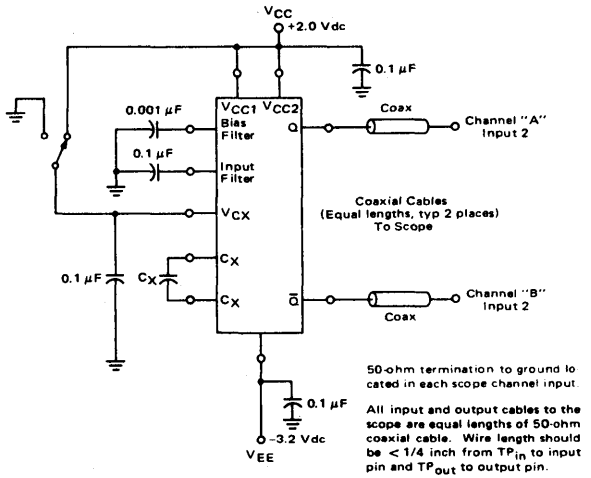
Characteristic	Symbol	Pin Under Test	SP1658 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8*	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
		8**	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
Input Current	I_{inH}	2*	–	–	–	–	350	–	–	µAdc	2	–	–	–	8	1,5
Input Leakage Current	I_{inL}	2*	–	–	0.5	–	–	–	–	µAdc	–	2	–	–	8	1,5
"Q" High Output Voltage	V_{OH}	4*	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
		6**	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
"$\overline{Q}$" Low Output Voltage	V_{OL}	4*	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
		6**	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	Gnd		V_{EE} -3.2 V	V_{CC} +2.0 V
Rise Time (10% to 90%)	t_+	6	–	2.7	–	1.6	2.7	–	3.0	ns	–	11,14	–	2	8	1,5
Fall Time (10% to 90%)	t_-	6	–	2.7	–	1.4	2.7	–	3.0	ns	–	11,14	–	2	2	1,5
Oscillator Frequency	f_{osc1}	–	130	–	130	155	175	110	–	MHz	–	11,14	–		8	1,5
	f_{osc2}	–	–	–	78	90	100	–	–	MHz	11,14	–	–		8	1,5
Tuning Ratio Test †	TR	–	–	–	3.1	4.5	--	–	–	–	11,14	–	–		8	1,5

*Germanium diode (0.4 drop) forward biased from 11 to 14 (11 ——▶|—— 14).
**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ——|◀—— 14).

†TR = $\frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\ \text{V}}$

C1 = 0.01 µF connected from pin 12 to Gnd.
C2 = 0.001 µF connected from pin 13 to Gnd.
C_{X1} = 10 pF connected from pin 11 to pin 14.
C_{X2} = 5 pF connected from pin 11 to pin 14.

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



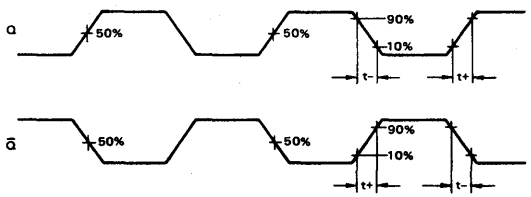


FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

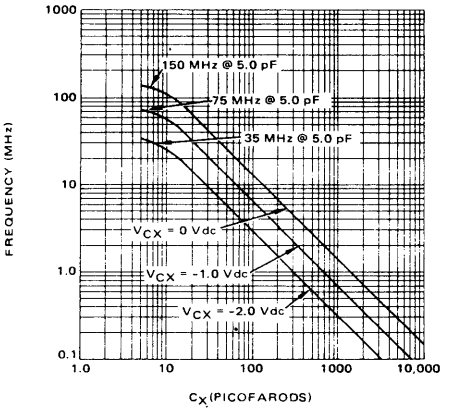


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY

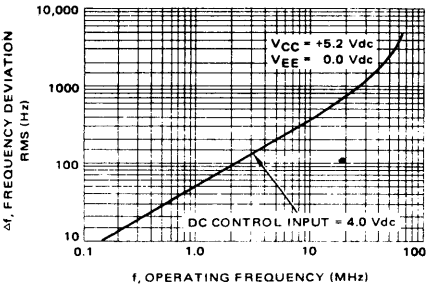
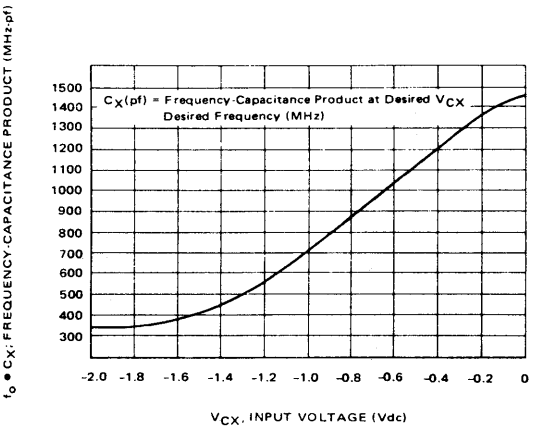


FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})

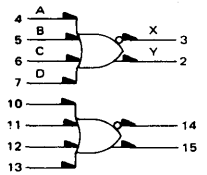


DUAL 4-INPUT GATE

SP1660

SP1660 provides simultaneous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point is always in the center of the transition region over the temperature range (-30° to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}

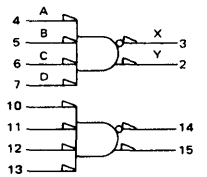
POSITIVE LOGIC



$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

NEGATIVE LOGIC

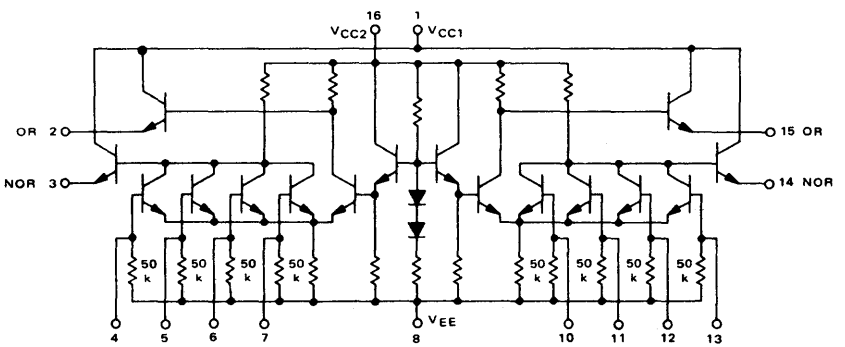


$X = \overline{A \bullet B \bullet C \bullet D}$

$Y = A \bullet B \bullet C \bullet D$

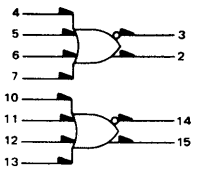
t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

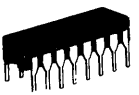
CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (LIC021 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





CERAMIC PACKAGE E

● Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
NOR Logic "1" Output Voltage	V_{OH} ●	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "0" Output Voltage	V_{OL} ●	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "1" Output Voltage	V_{OH} ●	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "0" Output Voltage	V_{OL} ●	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "1" Threshold Voltage	V_{OHA} ●	3	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic "0" Threshold Voltage	V_{OLA} ●	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic "1" Threshold Voltage	V_{OHA} ●	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic "0" Threshold Voltage	V_{OLA} ●	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9			2	–	–		
	t_{4+2+}	2	–	1.6	–	1.5	–	1.7			2	–	-		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	-		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

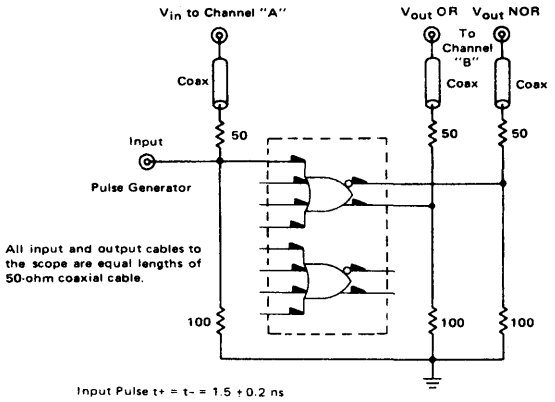
● NOTES

The electrical specifications shown above apply to the SP1660 under the following conditions:

1. The package is housed in a suitable heat sink.†
   or
2. Air is blown transversely over the package. See general information section for more details.

†A suitable heat sink is an IERC LIC21 4A2WCB or equivalent.

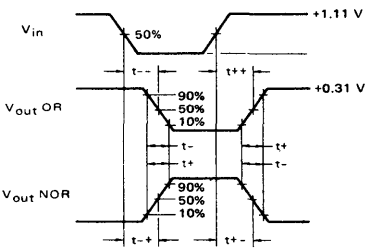
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse t+ = t- = 1.5 +0.2 ns

Unused outputs connected to a 50-ohm resistor to ground

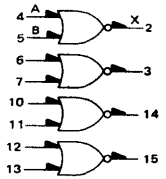
PROPAGATION DELAY



QUAD 2-INPUT "NOR" GATE

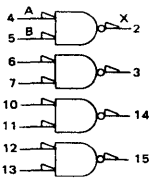
SP1662

POSITIVE LOGIC



$X = \overline{A + B}$

NEGATIVE LOGIC



$X = \overline{A \cdot B}$

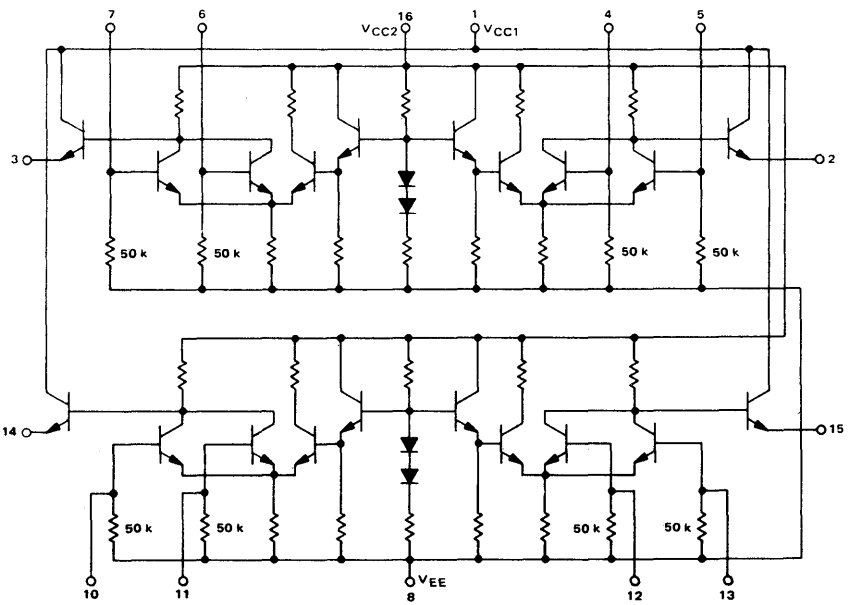
Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (-30 to +85°C).

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

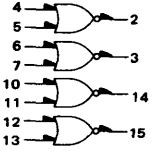
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

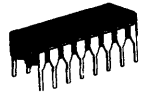
CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink(IERC-21 4 A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





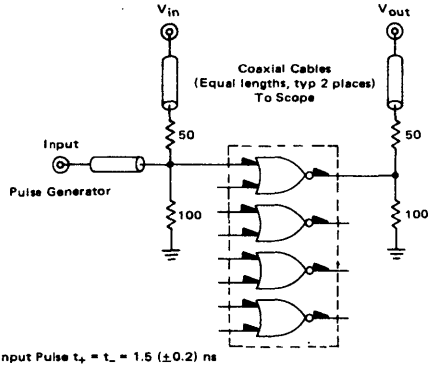
CERAMIC PACKAGE E

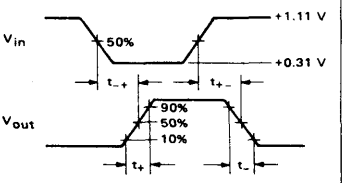
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1662 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\,H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\,L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	1.0	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	1.1	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	1.4	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	1.2	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





Input Pulse $t_+ = t_- = 1.5\ (\pm 0.2)$ ns

Unused outputs connected to a 50-ohm resistor to ground.

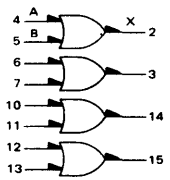
QUAD 2-INPUT "OR" GATE

SP1664

Four 2-input OR or AND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range -30 to +85°C.

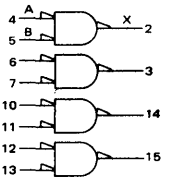
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



X = A + B

NEGATIVE LOGIC



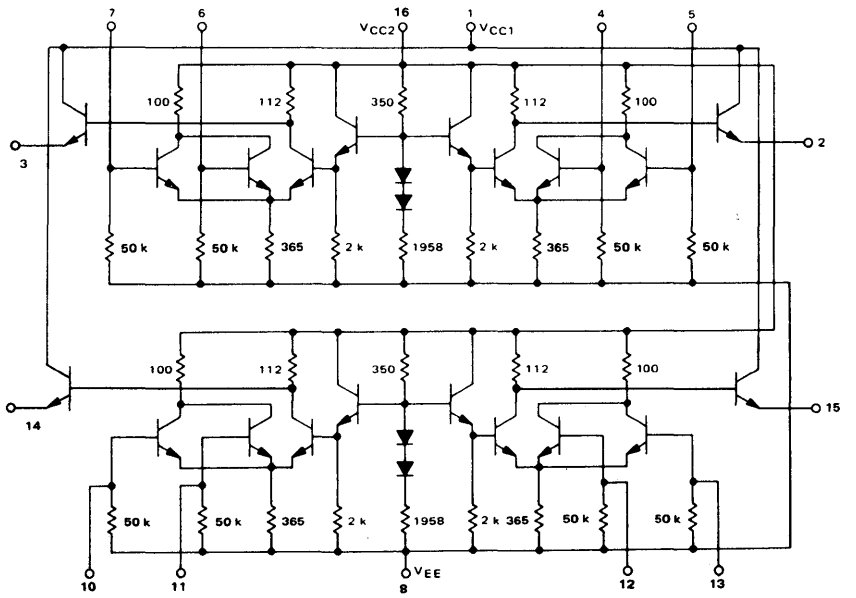
X = A • B

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

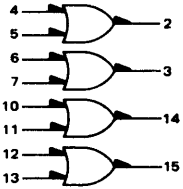
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

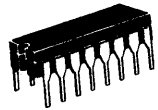
CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink(IERC-21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





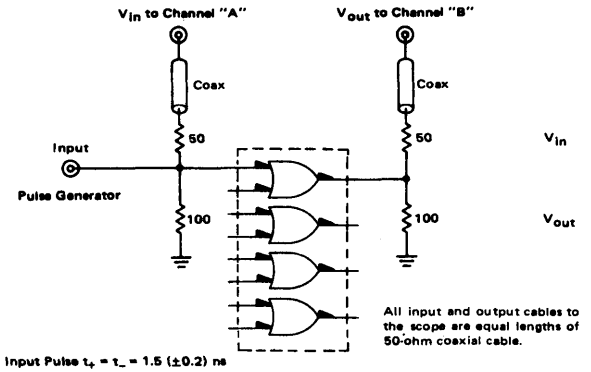
CERAMIC PACKAGE E

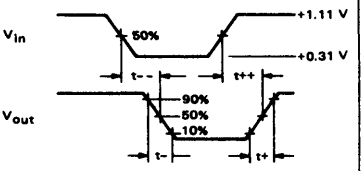
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1664 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	5	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	–	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





Input Pulse $t_+ = t_- = 1.5\ (\pm 0.2)$ ns

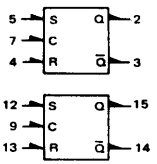
Unused outputs connected to a 50-ohm resistor to ground.

DUAL CLOCKED R-S FLIP-FLOP

SP1666

This device consists of two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage. The device is useful as a high-speed dual storage element.

POSITIVE LOGIC



t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

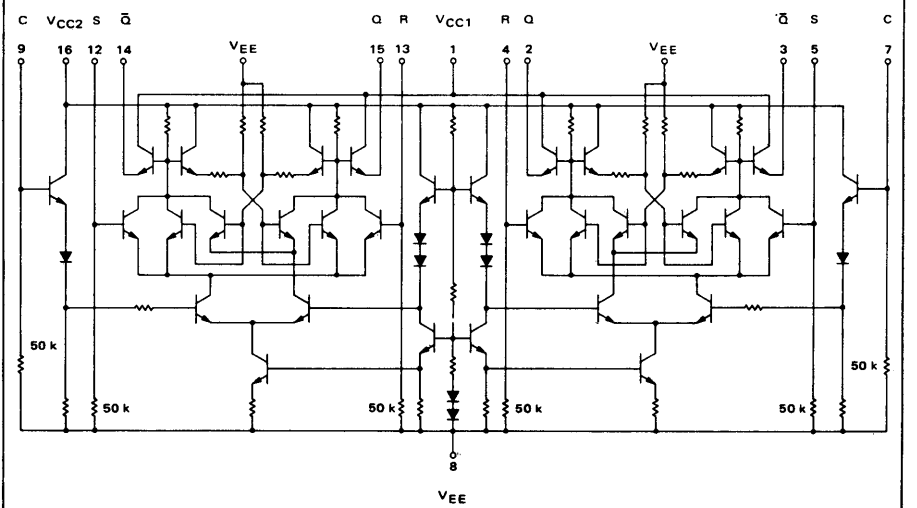
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

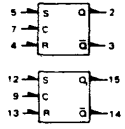
CIRCUIT SCHEMATIC

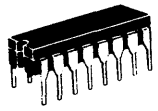


Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 21-4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





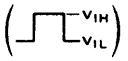
CERAMIC PACKAGE E

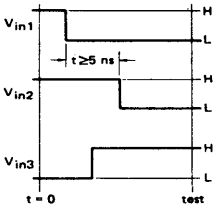
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1666 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85 Min	+85 Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	I_{inL}	12	–	–	0.500	–	–	–	µAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	µAdc	–	9,13	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	15 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q̄" Logic "1" Output Voltage	V_{OH}	14 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q̄" Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	9	–	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑤	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
"Q̄" Logic "1" Output Threshold Voltage	V_{OHA}	14 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
"Q̄" Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	9	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
[illegible]	t_{9+15-}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9-15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	15	–	–	↓	↓
	t_{9-14-}	14									14	–	–		
	t_{9+14-}	14									14	–	–		
Set Input	t_{12+15+}	15	1.0	2.5	1.0	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	↓	↓	↓	↓	↓	↓	ns	12	14	–	–	8	1,16
Reset Input	t_{13-14-}	14							ns	13	14	–	–	8	1,16
	t_{13+15+}	15							ns	13	15	–	–	8	1,16
Rise Time	t_+	14,15	0.8	2.8	0.8	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16

○ Notes appear on page following Electrical Characteristics tables

NOTES





① I_E is measured with no output pull-down resistors.

② Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

③ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

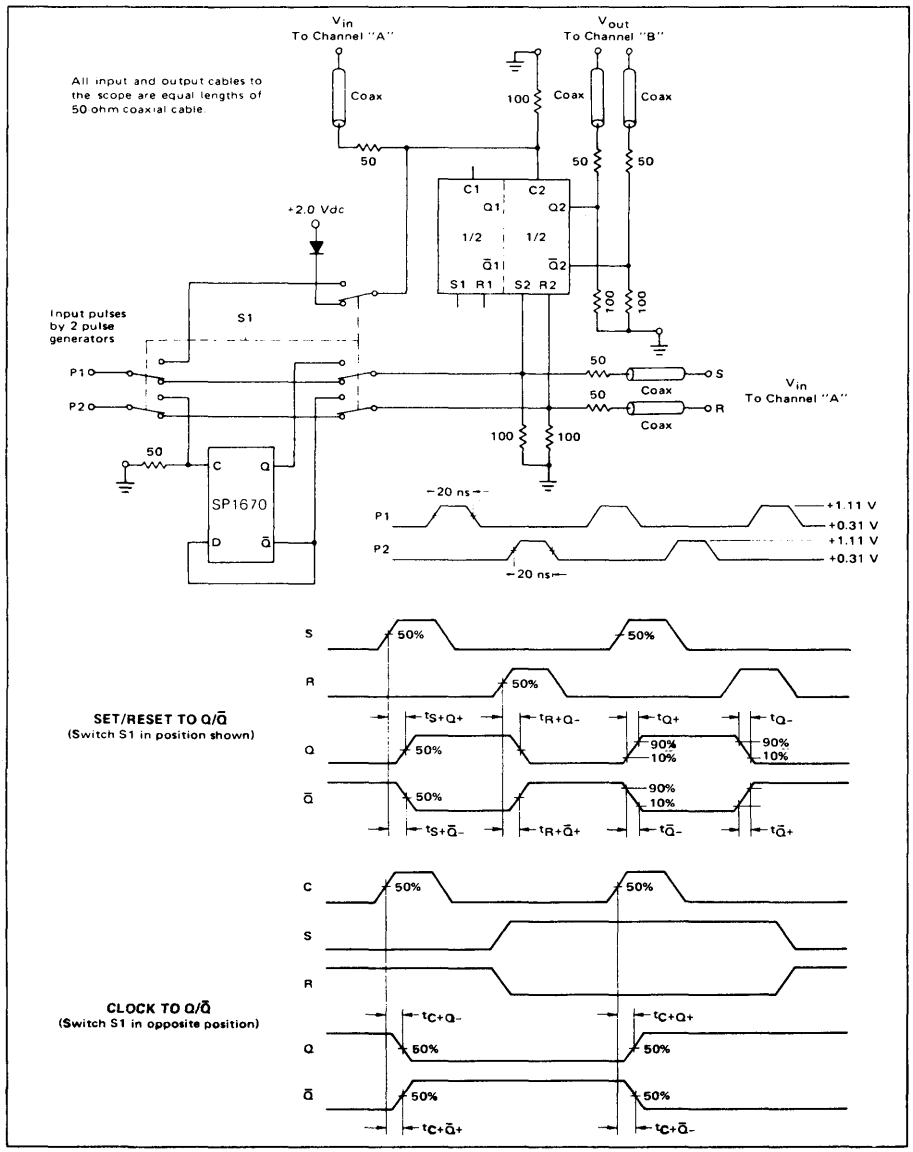
④ Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑤ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑥ Apply V_{in3} to C (V_{IH} to V_{IL})

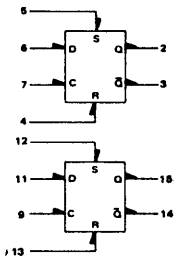
⑦ Apply V_{in3} to S (V_{IH} to V_{IL})

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



SP1668

POSITIVE LOGIC



This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

TRUTH TABLE

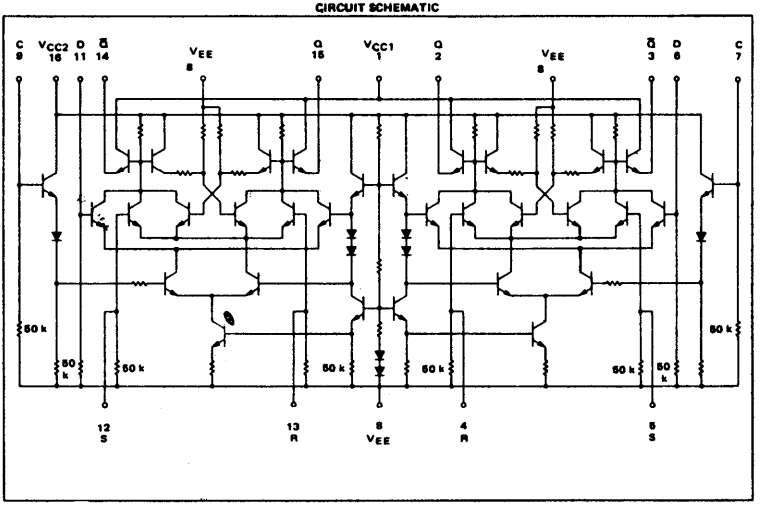
S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

**Output state not defined ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

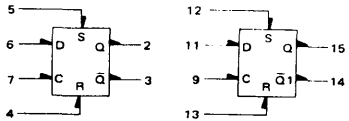
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



CERAMIC PACKAGE E

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

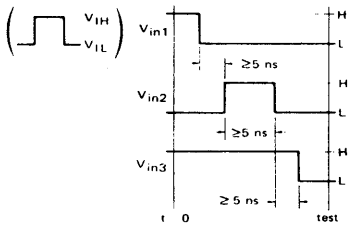
Characteristic	Symbol	Pin Under Test	SP1668 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E (Hi-Z)	1				55			mAdc	7,9				8	1,16
Input Current	I_{in} H	11,12,13②				0.370			mAdc	11,12,13				8	1,16
		9				0.225			mAdc	9				8	1,16
	I_{in} L	11,12,13②			0.500				µAdc		11,12,13			8	1,16
		9			0.500				µAdc		9			8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15③	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc		13			8	1,16
		15④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	9				8	1,16
"Q" Logic "0" Output Logic	V_{OL}	15⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc		12			8	1,16
		15⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9				8	1,16
"Q̄" Logic "1" Output Voltage	V_{OH}	14⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc		12			8	1,16
		14⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9				8	1,16
"Q̄" Logic "0" Output Voltage	V_{OL}	14③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc		13			8	1,16
		14④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9				8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15	-1.065		-0.980		-0.910		Vdc			12	13	8	1,16
		15⑦										11			
		15⑤								11		9			
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15		-1.630		-1.600		-1.555	Vdc			13	12	8	1,16
		15⑥											11		
		15③									11	9			
"Q̄" Logic "1" Output Threshold Voltage	V_{OLA}	14	-1.065		-0.980		-0.910		Vdc			13	12	8	1,16
		14⑥											11		
		14③									11	9			
"Q̄" Logic "0" Output Threshold Voltage	V_{OLA}	14		-1.630		-1.600		-1.555	Vdc			12	13	8	1,16
		14⑦										11			
		14⑤										9			
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{9+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15			8	1,16
	t_{9+15-}	15									15				
	t_{9+14-}	14									14				
	t_{9+14+}	14									14				
Rise Time	t_+	14,15	0.8	2.8	0.9	2.5	0.9	2.9	ns	9	14,15			8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15			8	1,16
Set Input	t_{12+15+}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	15			8	1,16
	t_{12+14-}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	14			8	1,16
Reset Input	t_{13+14+}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	14			8	1,16
	t_{13+15-}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	15			8	1,16

○Notes appear on page following Electrical Characteristics tables.

NOTES

① I_E is measured with no output pulldown resistors.

② Test voltage applied to pin under test.



③ Apply V_{in1} to S (V_{IH} to V_{IL}).

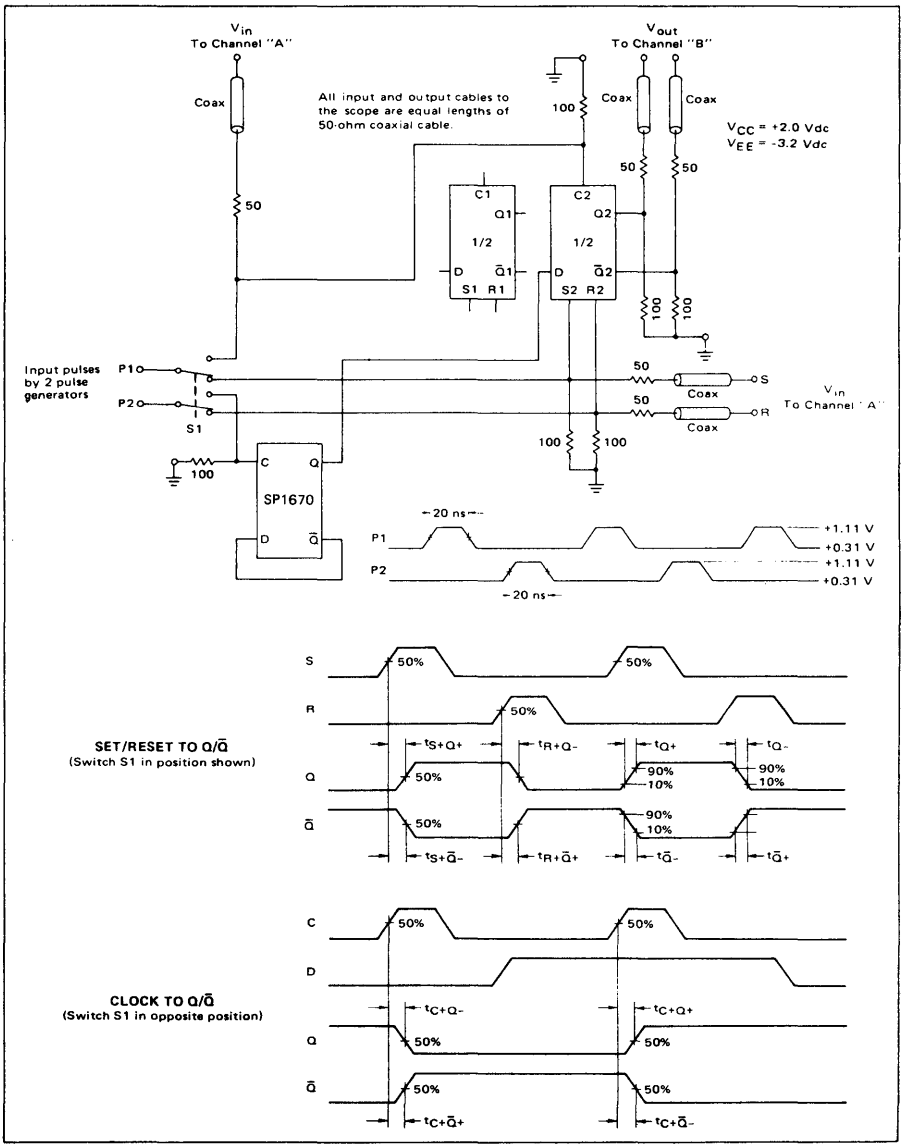
④ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})
V_{in3} to D (V_{IH} to V_{IL})

⑤ Apply V_{in1} to R (V_{IH} to V_{IL})

⑥ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

⑦ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS @ 25°C



MASTER-SLAVE
TYPE D FLIP-FLOP

SP1670

The SP1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

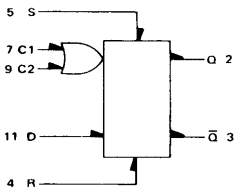
When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

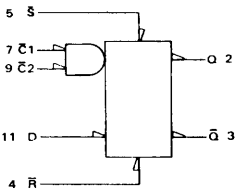
Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

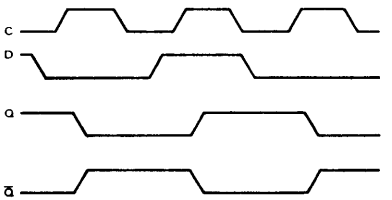
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	⌐	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	⌐	H
L	L	H	H	Q_n

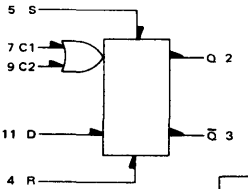
ϕ = Don't Care
ND = Not Defined
C = C1 + C2

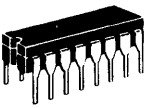
TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-7214A2WC8 or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.005	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP 1670 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11				270				11								
	$I_{in\ L}$	4			0.5				μAdc	9	4			8				1,16
		5		–				–		9	5		–		–	–	–	
		9	–	–		–	–	–		7	9		–		–	–	–	
		7	–	–		–	–	–		9	7		–		–	–	–	
		11	–	–		–				9	11	–						
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc		4,7,11			8	9	5		1,16
		3								11	5,9				7	4		
		2								11	5,7				4	9		
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11				7	5		
		2									4,7,11				5	9		
		3								11	5,9				4	7		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065		-0.980	–	-0.910	–	Vdc		4,7,11		–	8	9		5	1,16
		3		–		–		–		11	5,9				7		4	
		2		–		–		–		11	5,7				4	–	9	
		3		–		–		–		–	4,9,11				5		7	
		2		–		–		–		–	5,7	11			4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	11	5,7	–	–	8	9		4	1,16
		3									4,9,11				7		5	
		2				–				–	4,7,11				5		9	
		3				–				11	5,9	–			4		7	
		2				–				–	4,7		11		5	9	–	
		3				–				–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{7+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–			–	8	–	–	–	1,16
(See Figure 1)	t_{7-2-}	9,2								–			–		–		–	
	t_{7+3-}	9,3								–		–			–	–		
	t_{7-3+}	9,3								–		–	–		–	–		
Set to Output Delay	t_{5+2+}	5,2								–			–		–	–		
(See Figure 2)	t_{5+3-}	5,3								–		–			–	–	–	
Reset to Output Delay	t_{4+2-}	4,2								–		–			–	–	–	
(See Figure 2)	t_{4+3+}	4,3								–		–	–		–	–	–	
Output Rise Time	$t_{2+,13+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time	$t_{2-,3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
(See Figure 2)																		
Set Up Time	t_{5} "1"	2			–	0.4	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_{5} "0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time	t_{H} "1"	2	–		–	0.3	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_{H} "0"	2	–		–	0.5	–	–		–	6		–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270		300	–	270	–	MHz	–	–		–		–	–	–	–

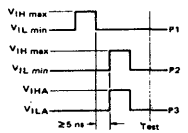


FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT

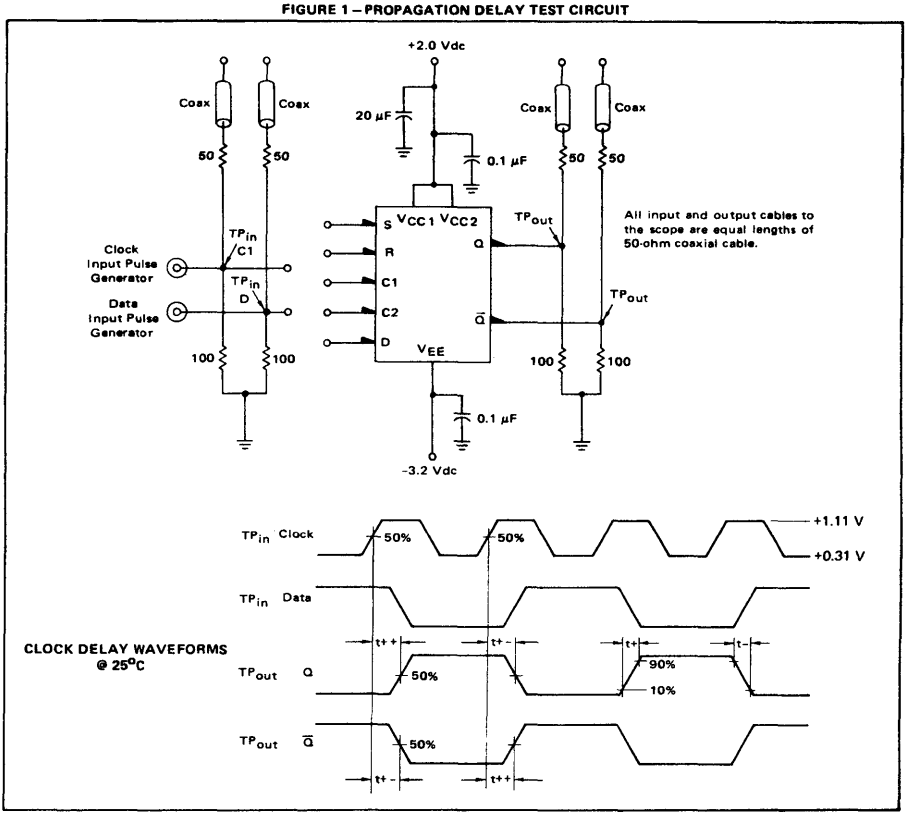


FIGURE 2 – SET-RESET DELAY WAVEFORMS @ 25°C

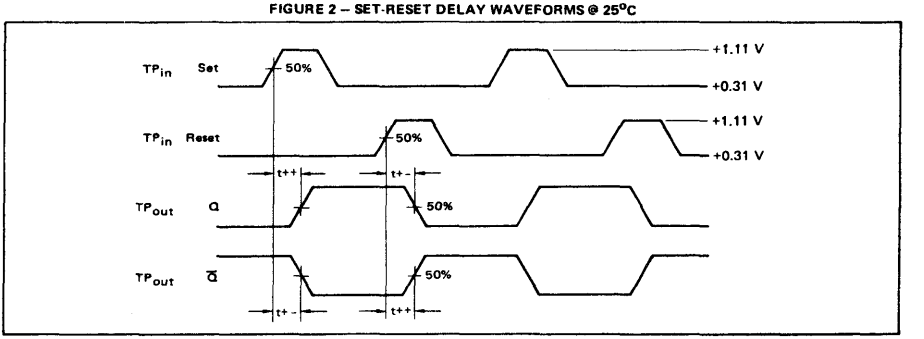
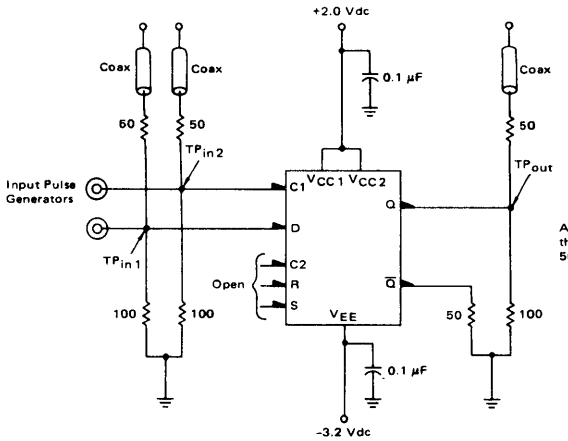
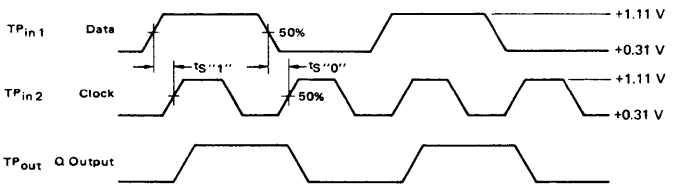


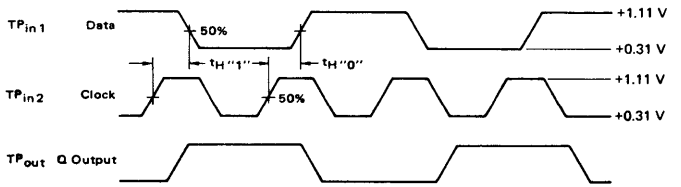
FIGURE 3 – SET UP AND HOLD TIME TEST CIRCUIT



SET UP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 4 – TOGGLE FREQUENCY TEST CIRCUIT

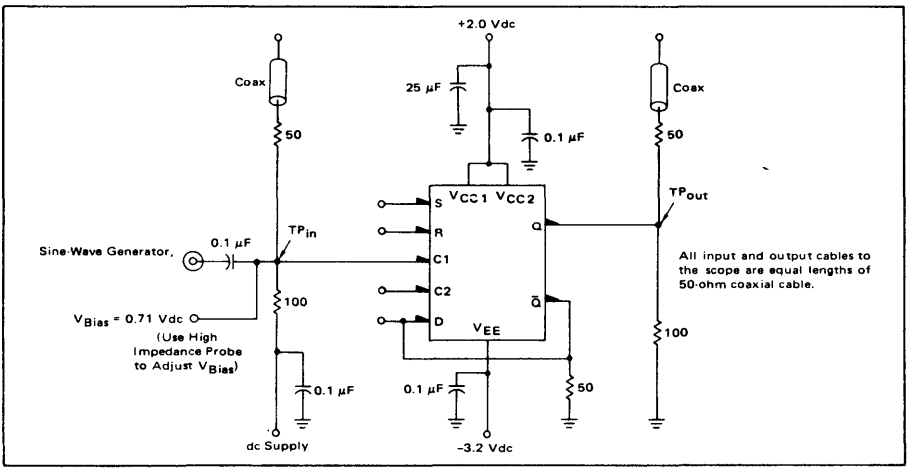


FIGURE 5 – TOGGLE FREQUENCY WAVEFORMS

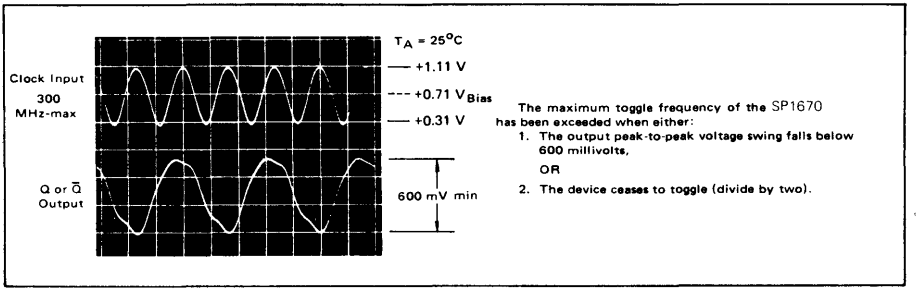


FIGURE 6 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

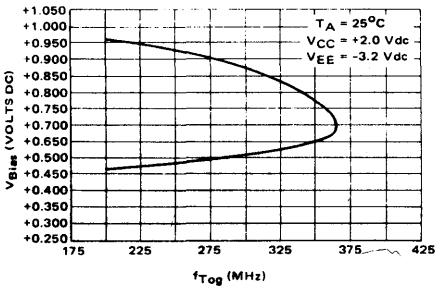
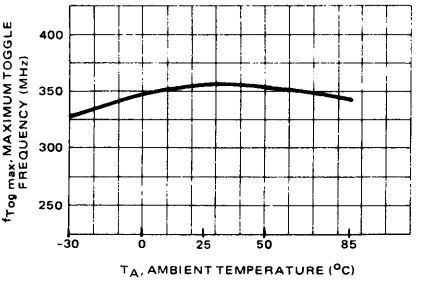


Figure 6 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal. V_{Bias} is defined by the test circuit in Figure 4, and waveform Figure 5.

Figures 8 and 9 illustrate minimum clock pulse width recommended for reliable operation of the SP1670.

FIGURE 7 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

FIGURE 8 – MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50 Ω

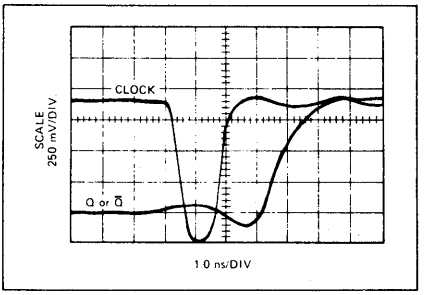
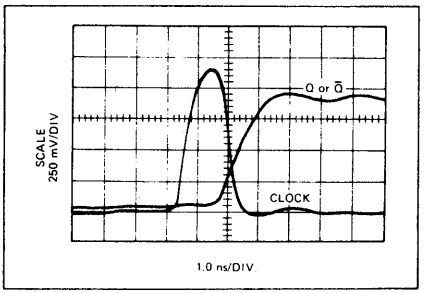


FIGURE 9 – MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50 Ω



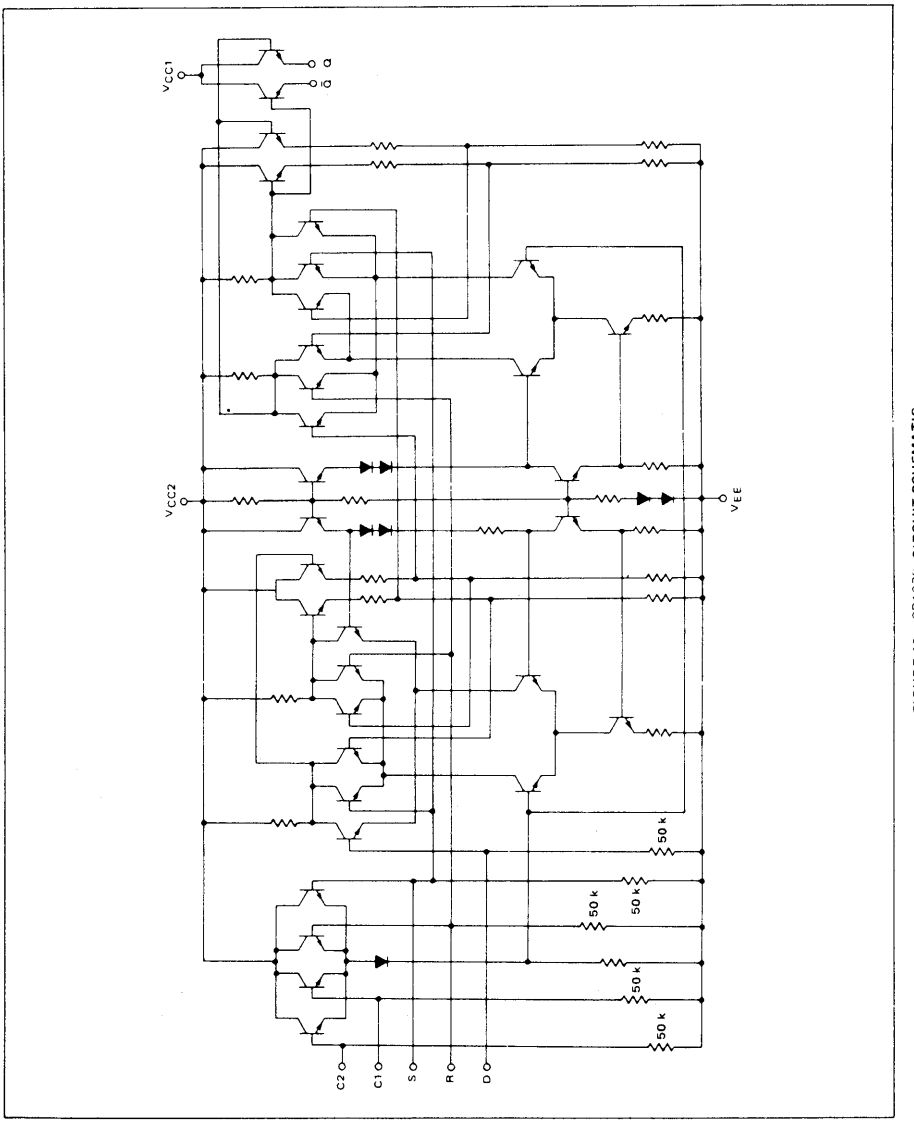
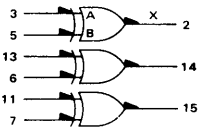


FIGURE 10 – SP1670 CIRCUIT SCHEMATIC

TRIPLE 2-INPUT
EXCLUSIVE-OR GATE

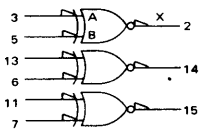
SP1672

POSITIVE LOGIC



$X = A \bullet \overline{B} + \overline{A} \bullet B$

NEGATIVE LOGIC



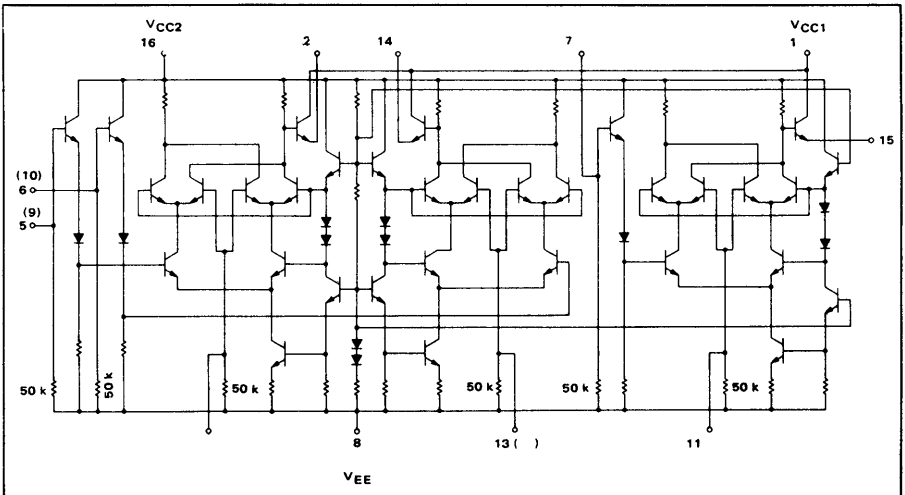
$X = A \bullet B + \overline{A} \bullet \overline{B}$

This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

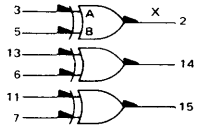
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WC8 or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



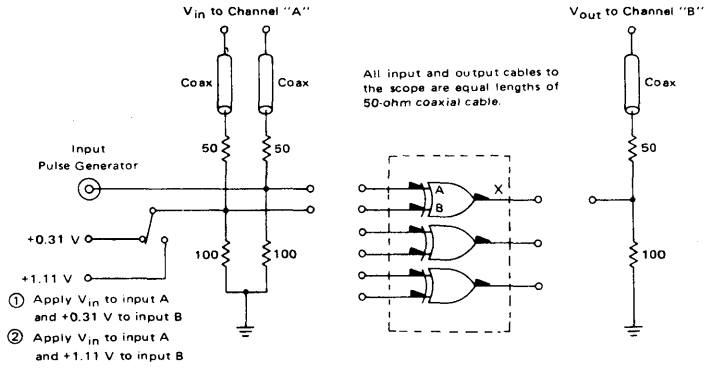
CERAMIC PACKAGE E

@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1672 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8				55	–		mAdc	All Inputs		–	–	8	1,16
Input Current	$I_{in\ H}$	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0.75 $I_{in\ H}$	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3	5	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	3	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3,5	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	3,5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3	5	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	3	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3,5	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	3,5	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max				Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{2+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

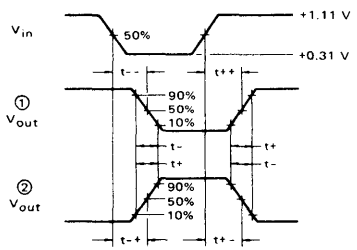
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

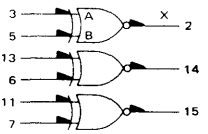
PROPAGATION DELAY



TRIPLE 2-INPUT
EXCLUSIVE-NOR GATE

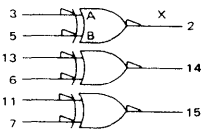
SP1674

POSITIVE LOGIC



$X = A \bullet B + \bar{A} \bullet \bar{B}$

NEGATIVE LOGIC

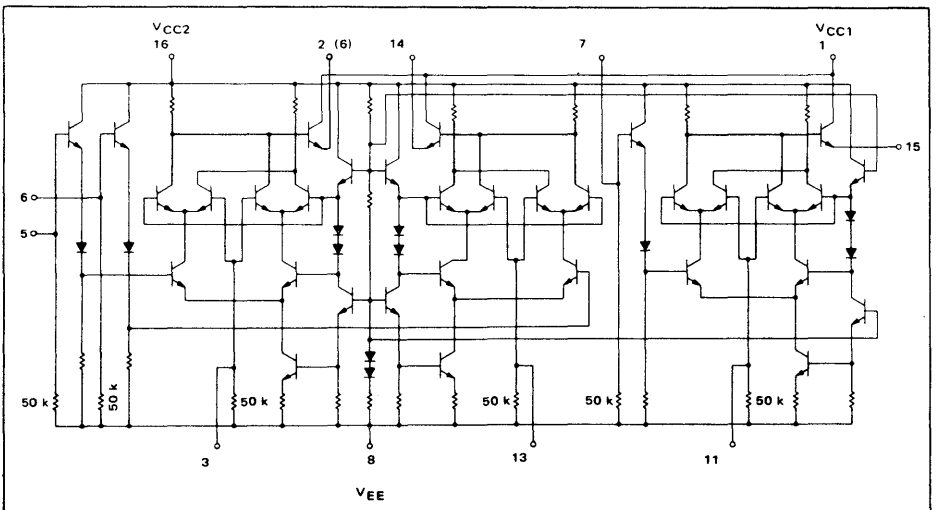


$X = \bar{A} \bullet B + A \bullet \bar{B}$

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30° to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

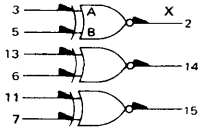
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WC8 or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



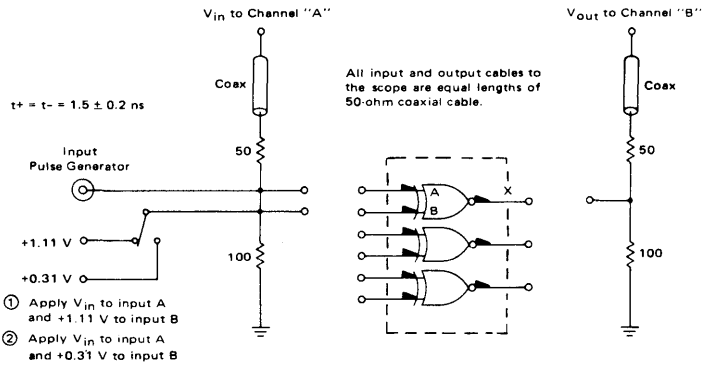
CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1674, Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	I_{inH}	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0.75 I_{inH}	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	$V_{OH\phi}$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3,5	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	$V_{OL\phi}$	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3	5	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	3	–	–	8	1,16
Logic "1" Threshold Voltage	$V_{OHA\phi}$	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3,5	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Threshold Voltage	$V_{OLA\phi}$	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3	5	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	3	8	1,16
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{6+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{6-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

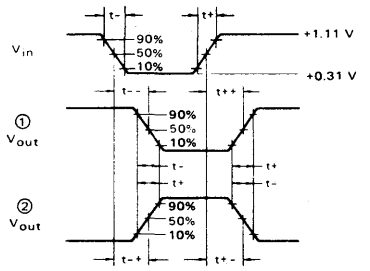
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

PROPAGATION DELAY



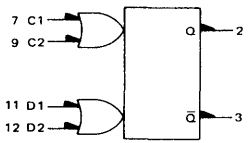
UHF PRESCALER
TYPE D FLIP-FLOP

SP1690

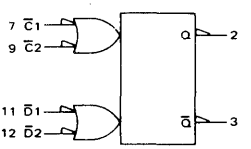
P_D = 200 mW typ/pkg (No Load)
f_{tog} = 500 MHz min

The SP1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary Q and $\overline{Q}$ outputs. It is a higher frequency replacement for the SP1670 (350 MHz) D flip-flop. There are no set or reset inputs and an extra data input is provided.

POSITIVE LOGIC

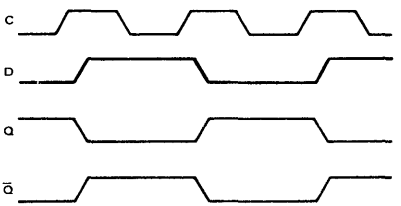


NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TIMING DIAGRAM



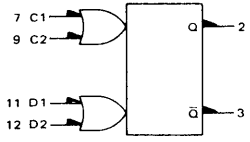
TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⌐	L	L
⌐	H	H

C = C1 + C2
D = D1 + D2
ϕ = Don't Care

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



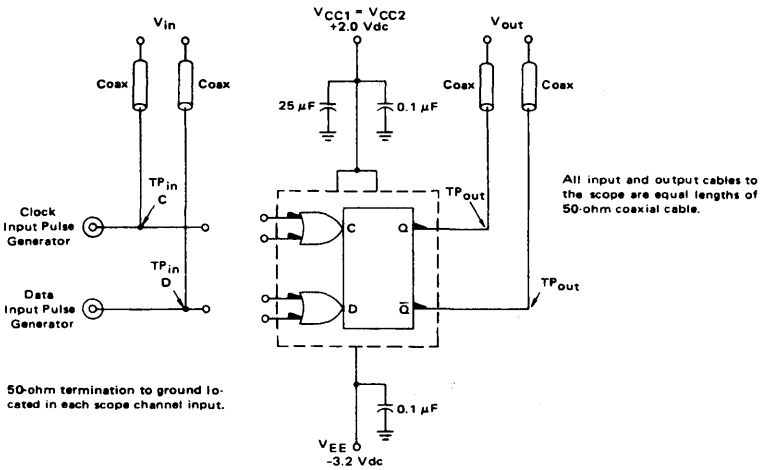
CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1690. Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P1	P2	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8				59			mAdc	7,9,11,12				8	–	–	1,16
Input Current	$I_{in\ H}$	7			–	250			µAdc	7				8	–	–	1,16
		11			–	270			µAdc	11				8	–	–	1,16
	$I_{in\ L}$	7	–		0.5	–		–	µAdc		7			8	–		1,16
		11	–		0.5	–		–	µAdc		11		–	8	–		1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	11				8	7	–	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc		11			8	7	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910		Vdc	11				8	–	7	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600		-1.555	Vdc	–	11	–	–	8	–	7	1,16
Switching Parameters					Min	Typ	Max							-3.2 Vdc			+2.0 Vdc
Clock to Output Delay (See Figure 1)	t_{7+2+}	2	–	–	–	1.5	–	–	ns	–	–	–	–	8	–	–	1,16
	t_{9+2+}		–	–	–	1.5	–	–	ns	–	–	–	–	–	–	–	
Output Rise Time	t_+		–	–	–	1.3	–	–	ns	–	–	–	–	–	–	–	
Fall Time	t_-		–	–	–	1.3	–	–	ns	–	–	–	–	–	–	–	
Setup Time (See Figure 2)	$t_{setup\ H}$		–	–	–	0.3	–	–	ns	–	–	–	–	–	–	–	
	$t_{setup\ L}$		–	–	–	0.3	–	–	ns	–	–	–	–	–	–	–	
Hold Time (See Figure 2)	$t_{hold\ H}$		–	–	–	0.2	–	–	ns	–	–	–	–	–	–	–	
	$t_{hold\ L}$		–	–	–	0.3	–	–	ns	–	–	–	–	–	–	–	
Toggle Frequency (See Figure 3)	f_{tog}	2	500	–	500	540	–	500	–	MHz	–	–	–	–	8	–	–	1,16

P1 — $V_{IH\ max}$ / $V_{IL\ min}$ P2 — $V_{IHA\ min}$ / $V_{ILA\ max}$

FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT



CLOCK DELAY WAVEFORMS @ 25°C

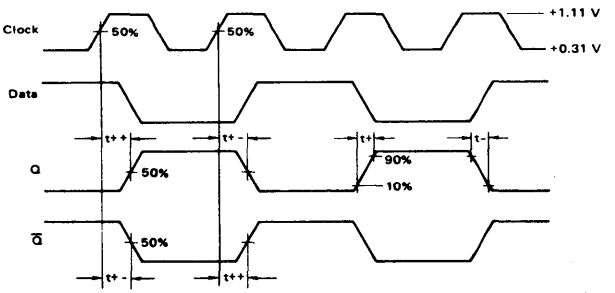
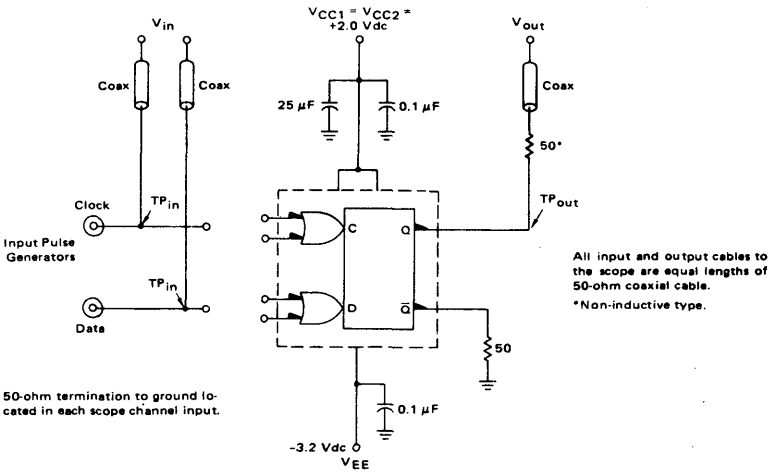
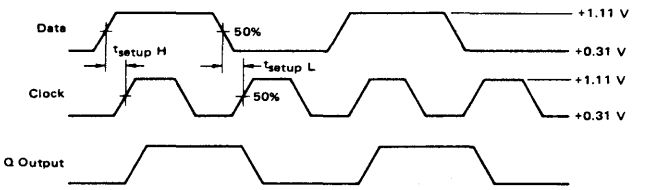


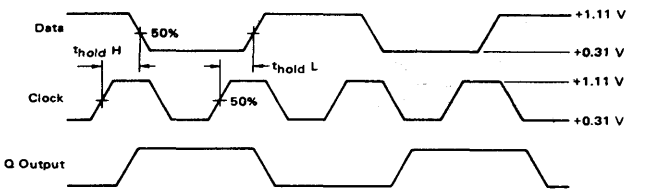
FIGURE 2 – SETUP AND HOLD TIME TEST CIRCUIT



SETUP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Setup time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 3 – TOGGLE FREQUENCY TEST CIRCUIT

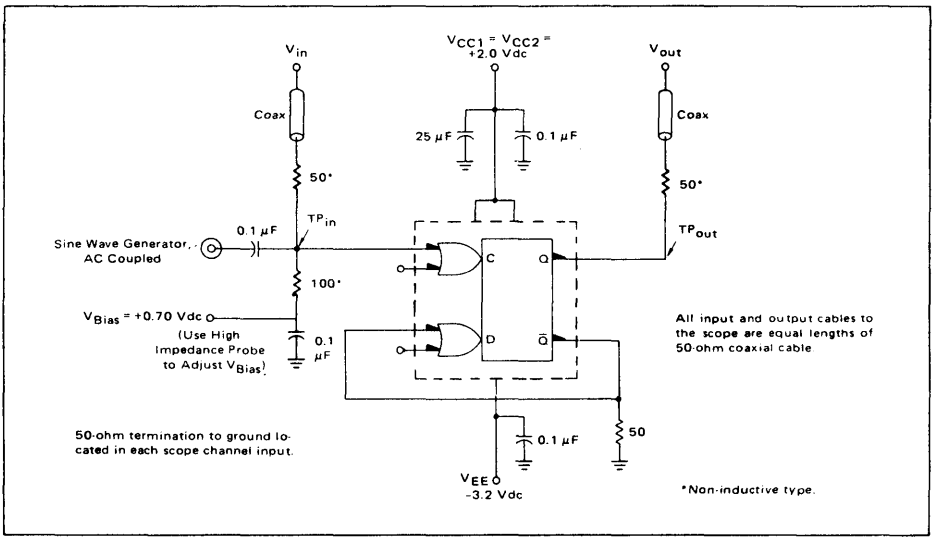
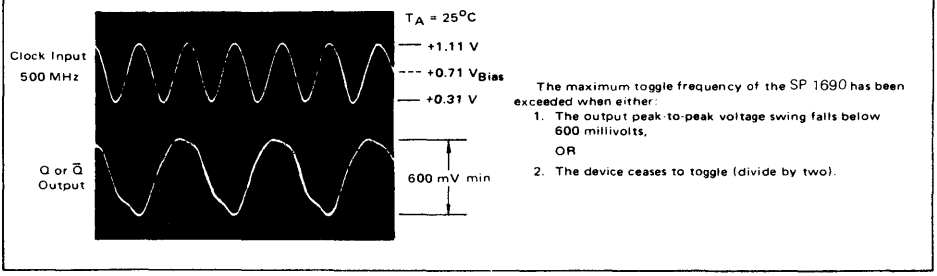


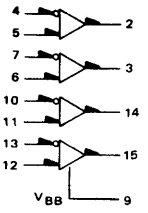
FIGURE 4 – TOGGLE FREQUENCY WAVEFORMS



QUAD LINE RECEIVER

SP1692

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.

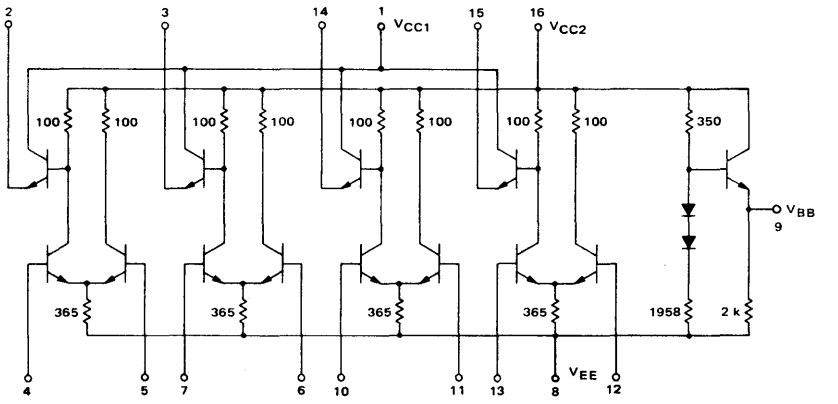


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

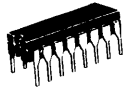
CIRCUIT SCHEMATIC



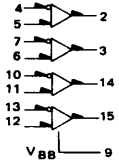
See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



CERAMIC PACKAGE E



● Test Temperature	TEST VOLTAGE VALUES						
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	
-30°C	-0.875	-1.890	-1.180	-1.515	From Pin 9	-5.2	
+25°C	-0.810	-1.850	-1.095	-1.485		-5.2	
+85°C	-0.700	-1.830	-1.025	-1.440		-5.2	

Characteristic	Symbol	Pin Under Test	SP1692 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.375	1.275	-1.35	-1.25	1.30	1.20	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out				
Propagation Delay	t_{4-2+}	2	–	1.6	–	1.5	–	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	–	1.8	–	1.7	–	1.9								
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3								
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3								

APPLICATIONS INFORMATION

The SP1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a SP1660 OR/NOR gate. The SP1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the SP1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The SP1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The SP1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

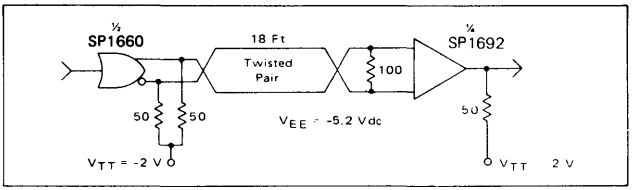


FIGURE 1 – LINE DRIVER/RECEIVER

FIGURE 2 – 400 MBS WAVEFORMS

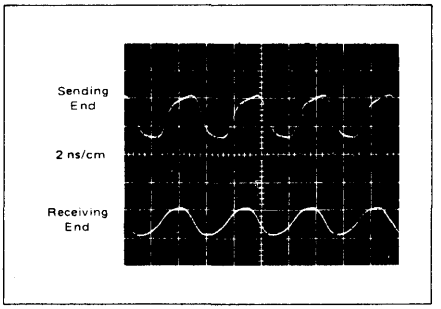
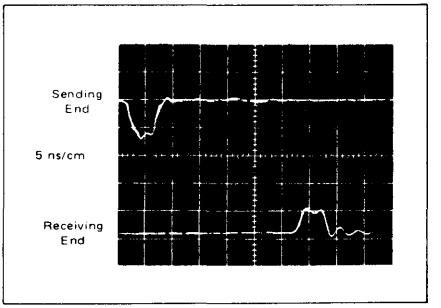


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



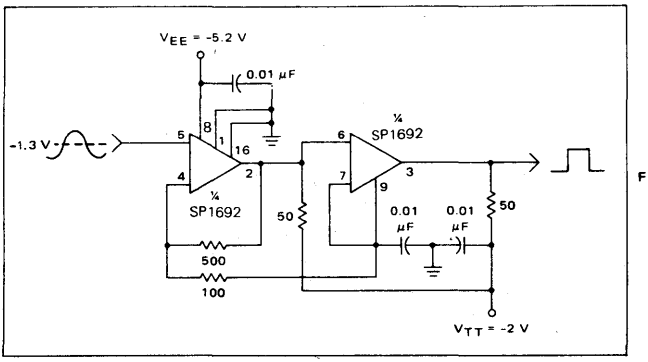


FIGURE 4 – 200 MHz SCHMITT TRIGGER

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

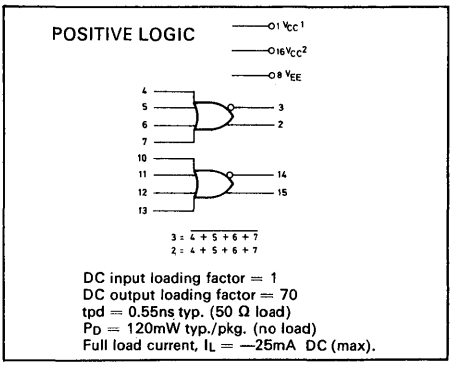
SUB-NANOSECOND LOGIC

ADVANCE INFORMATION

SP16F60

DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (—30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.



DC input loading factor = 1
DC output loading factor = 70
tpd = 0.55ns typ. (50 Ω load)
P_D = 120mW typ./pkg. (no load)
Full load current, I_L = —25mA DC (max).

Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible with SP1660

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | V_{CC} - V_{EE} |	8V
Base input voltage	OV to V_{EE}
O/P source current	<40mA
Storage temperature	—55°C to +150°C
Junction operating temperature	< +125C

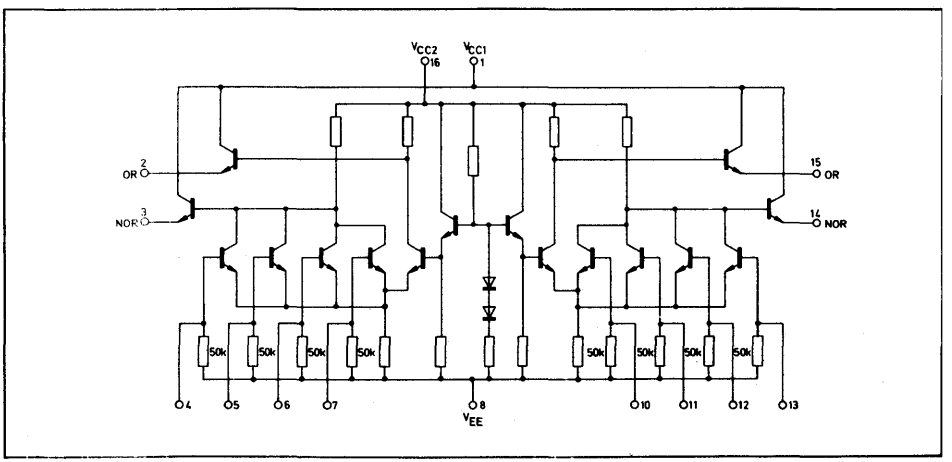


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (V)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	−0.875	−1.890	−1.180	−1.515	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+85°C	-0.700	−1.830	−1.025	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	– – – –	4 5 6 7	– – – –	– – – –	8	1,16
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4 5 6 7	– – – –	– – – –	– – – –	8	1,16
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4 5 6 7	– – – –	– – – –	– – – –	8	1,16
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	– – – –	4 5 6 7	– – – –	– – – –	8	1,16
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	– – – –	– – – –	– – – –	4 5 6 7	8	1,16
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	– – – –	– – – –	4 5 6 7	– – – –	8	1,16
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	– – – –	– – – –	4 5 6 7	– – – –	8	1,16
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	– – – –	– – – –	– – – –	4 5 6 7	8	1,16
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	–	0.55	0.8	–	–	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	–			–	–			2	–	–		
	t_{4+2+}	2	–	–			–	–			2	–	–		
	t_{4-3+}	3	–	–			–	–			3	–	–		
Rise Time 20% to 80%	t_{3+}	3	1.5	2.1	0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2+}	2	1.5	2.1	0.35	0.6	–	–	ns	4	2	–	–	8	1,16
Fall Time 20% to 80%	t_{3-}	3	1.4	2.1	0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2-}	2	1.4	2.1	0.35	0.6	–	–	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

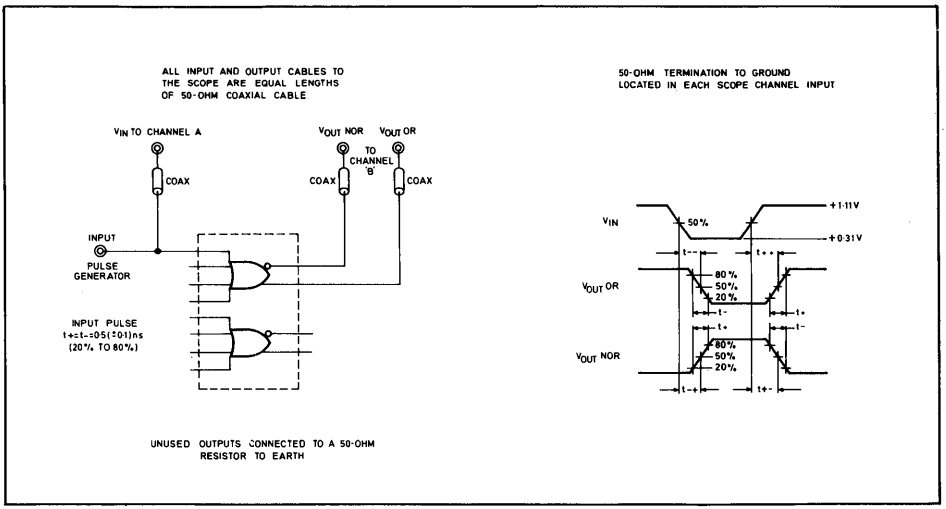


Fig. 3 Switching time test circuit and waveforms at +25°C

SP4020
VHF/UHF ÷ 64 PRESCALER

The SP4020 is an ECL divide by 64 which will operate at frequencies in excess of 950 MHz, and is intended for use as a prescaler in television receiver synthesiser tuners.

The device has a typical power dissipation of 470 mW at the nominal supply voltage of +6.8V.

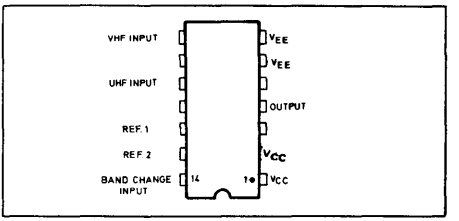


Fig. 1 Pin connections

OPERATING NOTES

Two input ports are available on this device. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring at high frequencies. Both inputs are terminated by a nominal 400Ω and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

When the device is switched to the VHF input, an input hysteresis of 50 mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF1} - V_{REF2}$

If the UHF input only is used and the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Band change input	+7.2 to −0.5V or −10mA
Output current	+30 mA to −30 mA
Operating junction temperature	+150°C
Storage Temperature	−55°C to +150°C

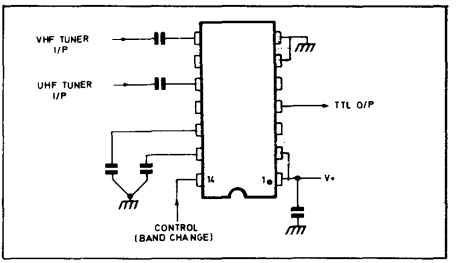
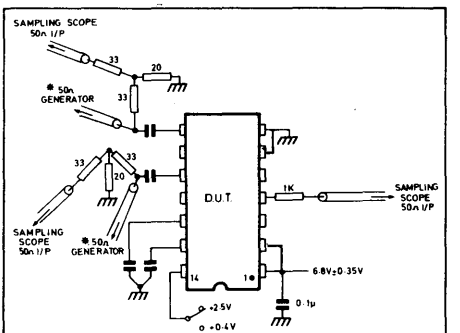


Fig. 2 Typical application



Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit.

All capacitors are 1nF unless otherwise stated.

Fig. 3 AC test circuit

FEATURES

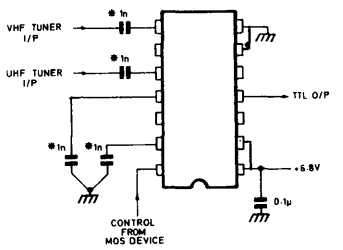
- Dual Input Ports for VHF and UHF
- Self-Biasing Clock Inputs
- Input Dynamic Range of 300mV to 900mV p-p Over Entire Frequency Range
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input
- Push – Pull TTL O/P

ELECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 68 mA typ., 90 mA max.
Temperature range: +10°C to +55°C
Clock inputs: AC coupled, self-biasing via 400Ω
Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

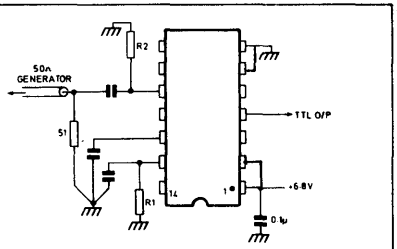
Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = +6.45V to +7.15V
Clock input voltage: 300mV to 900mV p-p
T_A: +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Inputs					
Max. I/P frequency	950	1100		MHz	UHF I/P
Min. I/P frequency		150	450	MHz	UHF I/P
Max. I/P frequency	350	1000		MHz	VHF I/P
Min. I/P frequency		40	60	MHz	VHF I/P sinewave
Band change I/P					
High level	2.5			V	
Low level			0.4	V	
Low level I/P current			−0.8	mA	at 0.4V
Max. clamp current	−3			mA	at approx. −0.7V
Output					
Low Level			0.4	V	5mA current sink
High Level	2.5	3.5	4.5		
Supply Current		68	90	mA	V_{CC} = 6.8V



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 Application circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

For 50 mV hysteresis R1 = 36kΩ R2 = ∞
For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

Fig. 5 Wideband operation

PACKAGE DETAILS

The SP4020 is packaged in 14-lead DIL.

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP 4021

UHF ÷ 64 PRESCALER

The SP4021 is an ECL divide by 64 which will operate at frequencies in excess of 950 MHz, and is intended for use as a prescaler in television receiver synthesiser tuners.

The device has a typical power dissipation of 500 mW at the nominal supply voltage of +6.8V.

OPERATING NOTES

The input is terminated by a nominal 400Ω and should be AC coupled to the signal sources. Input power to the device is terminated to ground by the decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

If the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when the clock input changes from a low to a high level.

FEATURES

- Self-Biasing Clock Input
- Input Dynamic Range of 300mV to 900mV p-p Over Entire Frequency Range
- Variable Input Hysteresis Capability for Wide Band Operation
- Push-Pull TTL O/P

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock input	2.5V p-p
Output current	+30 mA to -30 mA
Operating junction temperature	+150°C
Storage Temperature	-55°C to +150°C

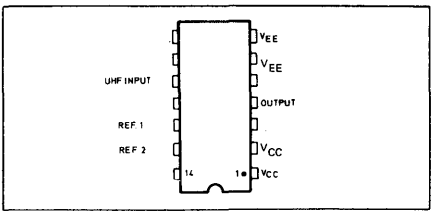


Fig. 1 – Pin connections

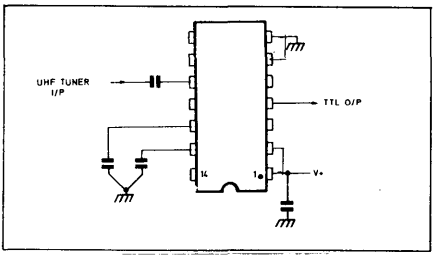
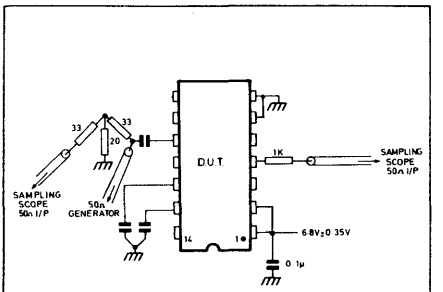


Fig. 2 – Typical application



All capacitors are 1nF unless otherwise stated.

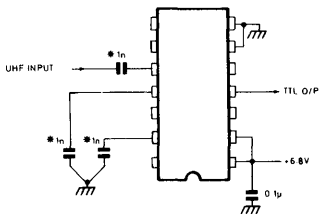
Fig. 3 – AC test circuit

ELECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 68 mA typ., 90 mA max.
Temperature range: $0^{o}C$ to + $65^{o}C$
Clock input: AC coupled, self-biasing via 400Ω
Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

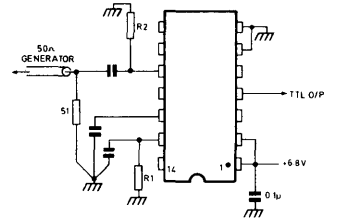
Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = +6.45V to +7.15V
T_A: $+25^{o}C$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Input					
Max. I/P frequency	950	1100		MHz	
Min, I/P frequency			100	MHz	
Sensitivity			550	mV_{p-p}	100MHz
			400	mV_{p-p}	200MHz
			350	mV_{p-p}	300MHz
			300	mV_{p-p}	500-700MHz
			400	mV_{p-p}	800MHz
			700	mV_{p-p}	950MHz
Overload Level	1.2			V_{p-p}	100MHz
Output					
Low Level			0.5	V	5mA current sink
High Level	2.5	3.5	5.0	V	-1mA
Supply Current		70	100	mA	V_{CC} = 7.15V



* Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 3 Application circuit



Capacitors are 1 nF unless otherwise stated. Values should be increased if operation below 10 MHz is desired.
For 50mV hysteresis R1 = 36kΩR2 = ∞
For 100mV hysteresis R1 = 18kΩR2 = 18kΩ

Fig. 4 Wideband operation

PACKAGE DETAILS

The SP4021 is packaged in 14-lead DIL.

SP 4040
VHF/UHF ÷ 256 PRESCALER

The SP4040 is an ECL divide by 256 which will operate at frequencies in excess of 950 MHz, and is intended for use as a prescaler in television receiver synthesiser tuners.

The device has a typical power dissipation of 470 mW at the nominal supply voltage of +6.8V.

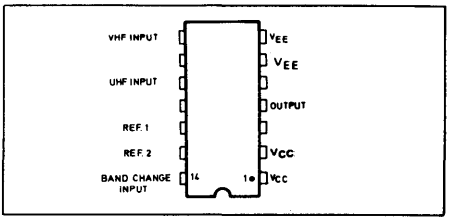


Fig. 1 Pin connections

OPERATING NOTES

Two input ports are available on this device. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring at high frequencies. Both inputs are terminated by a nominal 400Ω and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

When the device is switched to the VHF input, an input hysteresis of 50 mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF1} - V_{REF2}$

If the UHF input only is used and the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 256 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Band change input	+7.2 to −0.5V or −10mA
Output current	+30 mA to −30 mA
Operating junction temperature	+150°C
Storage Temperature	−55°C to +150°C

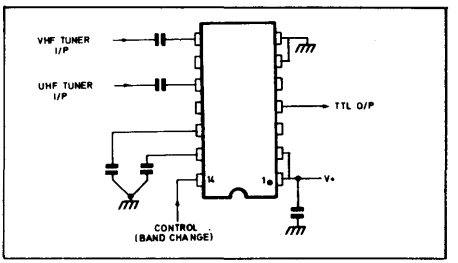
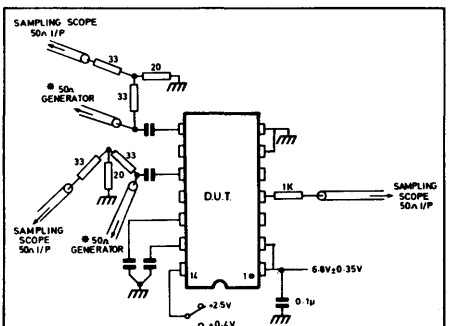


Fig. 2 Typical application



Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit.

All capacitors are 1nF unless otherwise stated.

Fig. 3 AC test circuit

FEATURES

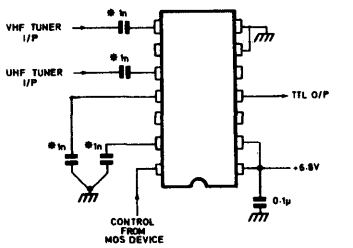
- Dual Input Ports for VHF and UHF
- Self-Biasing Clock Inputs
- Input Dynamic Range of 300mV to 900mV p-p Over Entire Frequency Range
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input
- Push – Pull TTL O/P

ELECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 68 mA typ., 90 mA max.
Temperature range: +10°C to +55°C
Clock inputs: AC coupled, self-biasing via 400Ω
Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

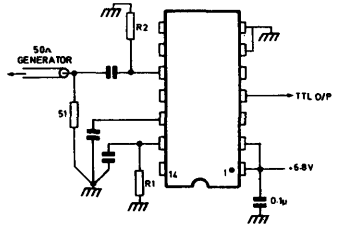
Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = +6.45V to +7.15V
Clock input voltage: 300mV to 900mV p-p
T_A: +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Inputs					
Max. I/P frequency	950	1100		MHz	UHF I/P
Min. I/P frequency		150	450	MHz	UHF I/P
Max. I/P frequency	350	1000		MHz	VHF I/P
Min. I/P frequency		40	60	MHz	VHF I/P sinewave
Band change I/P					
High level	2.5			V	
Low level			0.4	V	
Low level I/P current			−0.8	mA	at 0.4V
Max. clamp current	−3			mA	at approx. −0.7V
Output					
Low Level			0.4	V	5mA current sink
High Level	2.5	3.5	4.5		
Supply Current		68	90	mA	V_{CC} = 6.8V



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 Application circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

For 50 mV hysteresis R1 = 36kΩ R2 = ∞
For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

Fig. 5 Wideband operation

PACKAGE DETAILS

The SP4020 is packaged in 14-lead DIL.

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

SP4041

UHF ÷256 PRESCALER

The SP4041 is an ECL divide by 256 which will operate at frequencies in excess of 950 MHz, and is intended for use as a prescaler in television receiver synthesiser tuners.

The device has a typical power dissipation of 500 mW at the nominal supply voltage of +6.8V.

OPERATING NOTES

The input is terminated by a nominal 400Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

If the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 256 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when clock input changes from a low to a high level.

FEATURES

- Self-Biasing Clock Input
- Input Dynamic Range of 300mV to 900mV p-p over Entire Frequency Range
- Variable Input Hysteresis Capability for Wide Band Operation
- Push-Pull TTL O/P

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock input	2.5V p-p
Output current	+30 mA to -30 mA
Operating junction temperature	+150°C
Storage Temperature	-55°C to +150°C

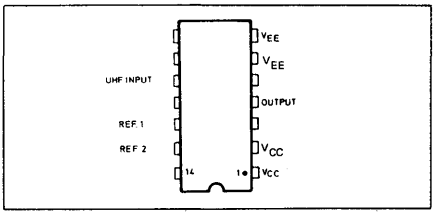


Fig. 1 – Pin connections

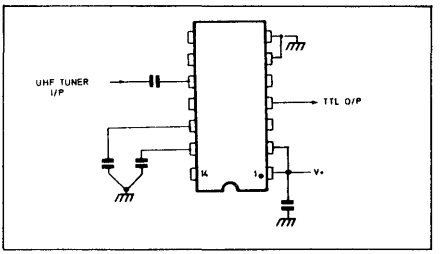


Fig. 2 – Typical application

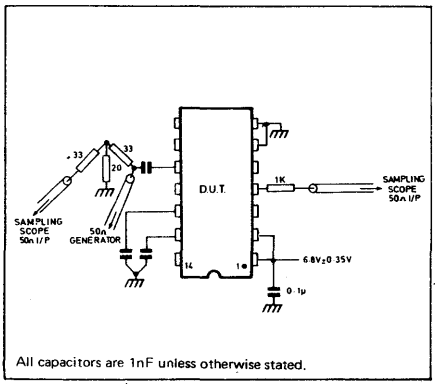


Fig. 3 – AC test circuit

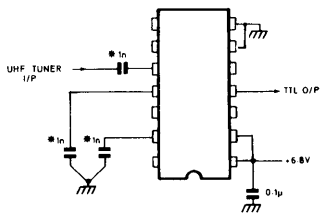
ELECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 68 mA typ., 90mA max.
Temperature range: 0°C to + 65°C.
Clock input: AC coupled, self-biasing via 400Ω
Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = +6.45V to +7.15V

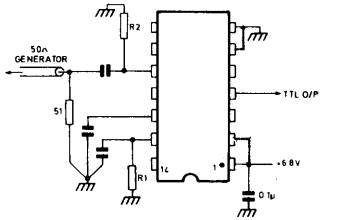
T_A: +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Input					
Max. I/P frequency	950	1100		MHz	
Min. I/P frequency			100	MHzp-p	
Sensitivity			550	mV_{p-p}	100MHz
			400	mV_{p-p}	200MHz
			350	mV_{p-p}	300MHz
			300	mV_{p-p}	500-700MHz
			400	mV_{p-p}	800MHz
			700	mV_{p-p}	950MHz
Overload Level	1.2			V p-p	100 MHz
Output					
Low Level			0.5	V	5mA current sink
High Level	2.5	3.5	5.0	V	-1mA
Supply Current		70	100	mA	V_{CC} = 7.15V



*Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 — Application circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

For 50 mV hysteresis R1 = 36kΩ R2 = ∞
For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

Fig. 5 — Wideband operation

PACKAGE DETAILS

The SP4041 is packaged in 14-lead DIL.

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

SP4140/50

VHF/UHF÷ 256 PRESCALER

The SP 4140/50 are ECL divide by 256 which will operate at frequencies in excess of 950 MHz, and are intended for use as a prescaler in television receiver synthesiser tuners.

The device has a typical power dissipation of 300 mW at the nominal supply voltage of 5.0.

OPERATING NOTES

The input is terminated by a nominal 800Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

The SP4140 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The SP4150 output is designed to provide complementary emitter follower O/Ps so that the rise time of the output can be adjusted to suit system requirements.

FEATURES

- 5.0 Volt Operation
- Self-Biasing Clock Inputs
- Input Dynamic Range of 10mV to 600mV p-p Over Entire Frequency Range
- Variable Input Hysteresis Capability for Wide Band Operation
- Complementary ECL O/P
- Push – Pull TTL O/P

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Output current	+30 mA to -30 mA
Operating junction temperature	+150°C
Storage Temperature	-55°C to +150°C

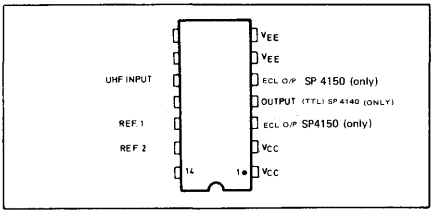


Fig. 1 – Pin connections

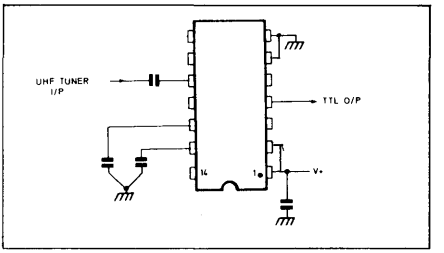


Fig. 2 – Typical appoication

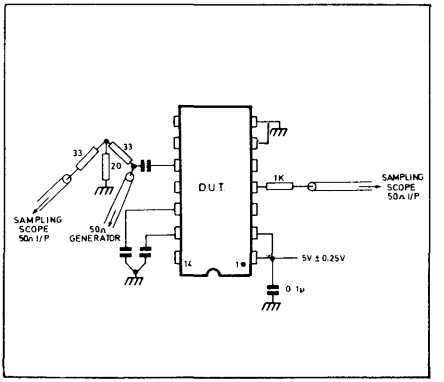


Fig. 3 – AC test circuit

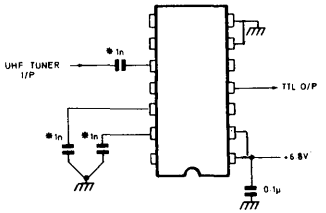
ELECTRICAL CHARACTERISTICS

Supply voltage: 5.0 ± 0.25V
Supply current: 60 mA typ.
90 mA max
Temperature range: $0^{o}C$ to $70^{o}C$
Clock inputs: AC coupled, self-biasing via 800Ω

Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = 5.0V ±0.25

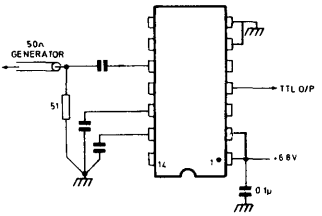
Clock input voltage: 10mV to 600mV p-p
T_{amb} $5^{o}0$ to + $70^{o}C$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Inputs					
Max. I/P frequency	950	1100		MHz	
Min. I/P frequency			80	MHz	
Output SP 4140					
Low Level	0		0.45	V	3 mA sink V_{CC} = 5.0V
High Level	3.8		4.6	V	1mA source T_{amb} $25^{o}C$
Output SP4150					
Voltage Swing	600	800		mV	No load each output
Supply Current		60	90	mA	V_{CC} = 5V



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 — Application circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

Fig. 5 — Wideband operation

PACKAGE DETAILS

The SP 4140/50 is packaged in 14-lead DIP.

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8600A&B
250MHz ÷ 4 COUNTER

The SP8600 is a fixed ratio emitter coupled logic ÷4 counter with a specified input frequency range of 5—250 MHz. The operating temperature range is pecified by the device code suffix letter: 'A' denotes -55°C to +125°C, 'B' denotes 0°C to +70°C peration,

Intended for use with an external bias arrangement nd capacitive coupling to the signal source, the ;P8600 can be either single driven, or double driven vith two complementary input signals.

The outputs are complementary free collectors that an have their load resistors taken to any bias voltage p to 12V more positive than V_{EE}.

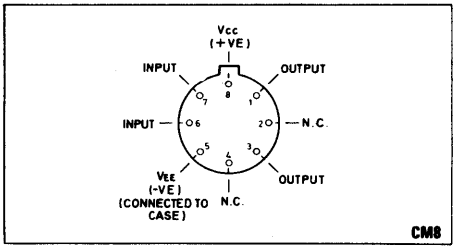


Fig. 1 Pin connections (bottom view)

FEATURES

- Low Power
- Free Collector Outputs to Interface to TTL
- 250 MHz ÷ 4 Over Full Military Temp. Range

APPLICATIONS

- Synthesizers — Mobile and Fixed
- Counters
- Timers

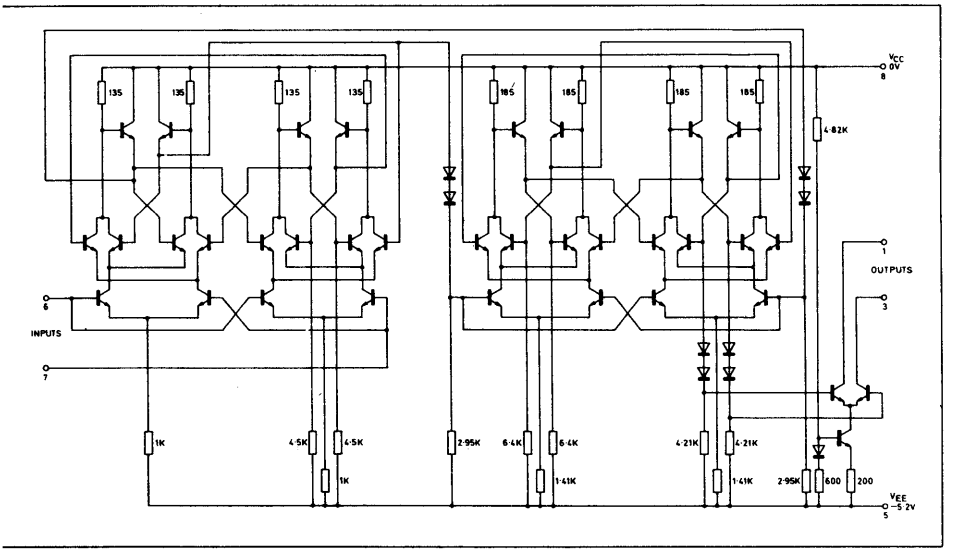


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade —55°C to +125°C
'B' grade 0°C to +70°C

Supply voltage 0V
−5.2V
Input voltage (single driven — other input decoupled to ground plane) V_{CC} 400 to 800 mV p-p
Input voltage (double complementary input drive) V_{EE} 250 to 800 mV p-p
Input bias voltage Bias chain as in test circuit (see Fig. 3 and operating notes).

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. input frequency	250	390*		MHz	Typical figure quoted at +25°C.
Min. input frequency with sinusoidal input			25	MHz	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	1.6			mA	Input f=250 MHz.
Power supply drain current		16*	25	mA	V_{EE} = −5.2V, V_{BIAS} as Fig. 3.

*At +25°C

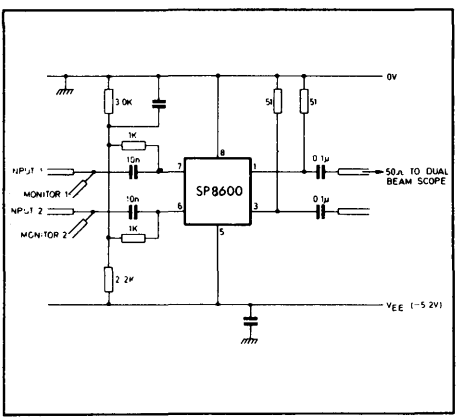


Fig. 3 Test circuit

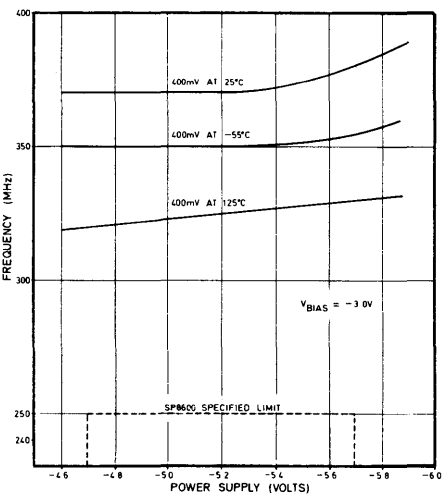


Fig. 4 Maximum input frequency v. power supply voltage (typical)

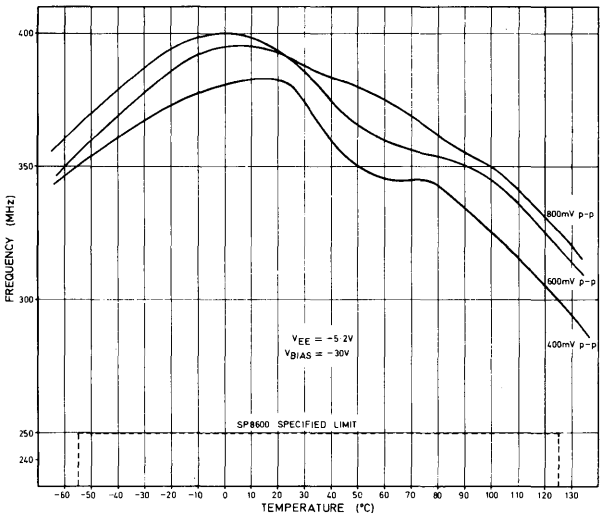


Fig. 5 Maximum input frequency v. temperature

PERATING NOTES

The circuit performance obtained from the SP8600 is timized if normal high frequency rules for circuit out are obeyed — leads should be kept short, pacitors and resistors should be of non-inductive oes, etc.

The signal source is normally AC coupled to one of e inputs or, if complementary signals are available, to th inputs. The inputs require an external bias chain set the DC potential on the inputs (see Fig. 3). No preciable change in performance is observed over a nge of DC bias from −2.5V to −3.5V.

Any tendency for the circuit to self-oscillate in the sence of input signal (or when the input signal is very all) can be overcome by offsetting the two inputs by proximately 40mV, using, for example, the bias angement shown in Fig. 6. The input wave form may sinusoidal, but below 25 MHz incorrect operation ay occur because of the limited slew rate of the out signal. A square wave input with a slew rate eater than 20V/μs ensures correct operation down DC.

The output is in the form of complementary free llectors with at least 2mA available from them. For tisfactory high frequency interfacing to ECL or hottky TTL the circuit techniques illustrated in Fig. 7 e recommended.

For maximum frequency operation, it is essential that e output load risistor values be such that the output nsistors do not saturate. If the load resistors are nnected to the 0V rail, then saturation can occur with istance values greater than 600Ω. Of course, if the ad resistors are taken to a more positive potential, en higher values can be used. N.B. If only one output used, the other output should be connected to 0V.

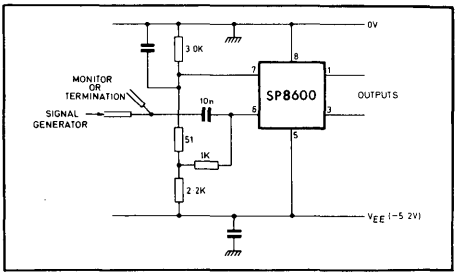


Fig. 6 Bias arrangement to prevent self-oscillation under no-signal conditions

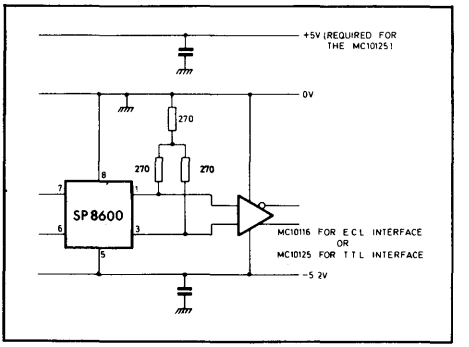


Fig. 7 ECL qnd Schottky TTL interfacing

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC}—V_{EE}	10V
Input voltage V_{IN}	Not greater than supply voltage in use
Bias voltage on o/p's V_{OUT}—V_{EE}	14V
Operating junction temperature	+175°C max.
Storage temperature	—55°C to +175°C

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SP8000 SERIES

HIGH SPEED DIVIDERS

SP8601A & B

150MHz÷4

The SP8601 is a fixed ratio emitter coupled logic ÷4 counter with a maximum specified input frequency of 150 MHz but with a typical maximum operating frequency well in excess of this (see Typical Operating Characteristics). The operating temperature range is specified by the final coding letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C.

The SP8601 can be operated with single input drive or with double, complementary, I/P drive. It can be driven with direct coupling from ECL II levels (or from an SP8602 device), or it can be capacitively coupled to the signal source if an external bias is provided.

There are complementary free collector outputs that can have their external load resistor connected to any bias up to 12 volts more positive than V_{EE}.

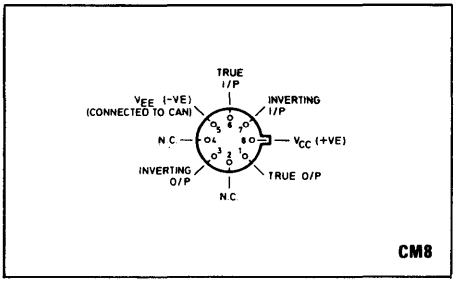


Fig. 1 Pin connections (bottom view)

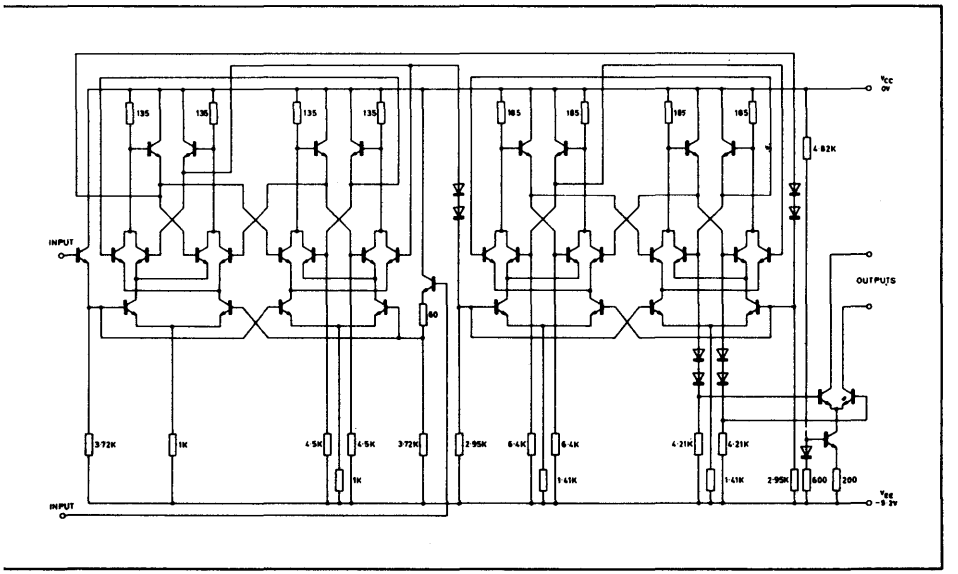


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade	−55°C to +125°C
'B' grade	0°C to +70°C
Operating supply voltage V_{CC}	0V.
V_{EE}	−5.2V ±0.25V
Input voltage (single drive — other input decoupled to ground plane)	400 to 800 mV (p-p)
Input voltage (double drive)	250 to 800 mV (p-p)
Bias voltage	Bias chain as in test circuit (see Fig. 2).

Characteristic	Value			Units	Conditions
	Min	Typ.	Max.		
Max. input frequency	150			MHz.	
Min. input freq. with sinusoidal input.			15	MHz.	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	1.6			mA	Input freq.= 150 MHz. R_{load} = 50Ω
Power supply drain current		18	25	mA	V_{EE} = −5.2V

OPERATING NOTES

Circuit performance obtained from the SP8601 is optimised if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally directly coupled into the device, which will tolerate a wide range of input bias voltages, but was designed for inputs from ECL II levels and can therefore be satisfactorily driven from SP8602 range of counters. The bias voltage on the input marginally affects the overall power consumption of the device (For typical operating characteristics with varying bias voltages see Fig. 4).

If it is not practicable to directly couple the input signal, then a bias chain similar to the one shown in Fig. 3 can be used.

The input waveform may be sinusoidal, but below about 10 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate of greater than 20 V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with 2 mA min. available from them. The output voltage swing obviously depends on the value of load resistor used and also the frequency of operation. The following table gives some typical examples of output voltage for different load resistors. With careful board layout to minimise capacitance these figures can easily be exceeded.

Min. Output Voltage	Load Resistor	Input Frequency
1.1V	1kΩ	120 MHz
320mV	200Ω	150 MHz
80mV	50Ω	180 MHz

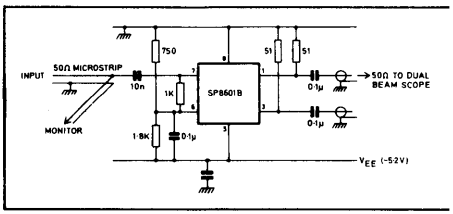
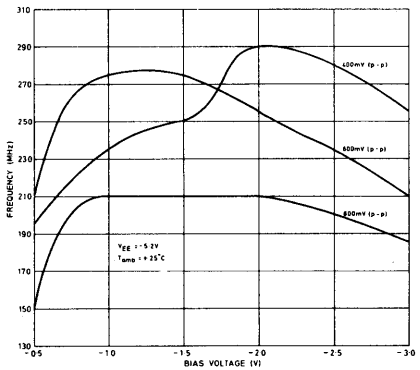


Fig. 3 Test circuit

TYPICAL OPERATING CHARACTERISTICS



NOTE: The value of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig. 4 Maximum input frequency v. bias voltage at single input drive levels of 400, 600 and 800 mV (typical device)

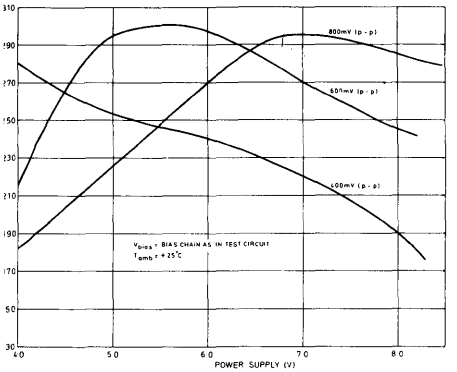


Fig. 5 Maximum frequency v. power supply voltage at single input drive levels of 400, 600 and 800 mV (typical device)

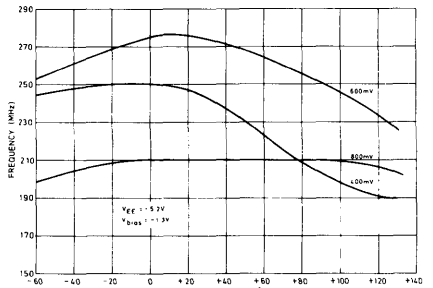


Fig. 6 Maximum input frequency v. temperature at single input drive levels of 400, 600 and 800 mV (typical device)

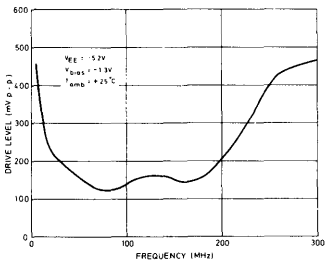


Fig. 7 Minimum single input drive level for correct operation v. input frequency (typical device)

APPLICATION NOTES

The SP8601 used with two SP8602 series ÷2 counters to give a 500 MHz divide-by-sixteen prescaler is shown in Fig. 8. Capacitors marked thus * may need to be increased in value for low frequency operation.

For correct operation when interfacing with TTL and ECL II the circuits shown in Figs. 9, 10 and 11 are recommended.

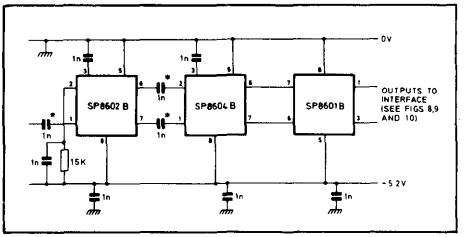


Fig. 8 Divide-by-sixteen prescaler

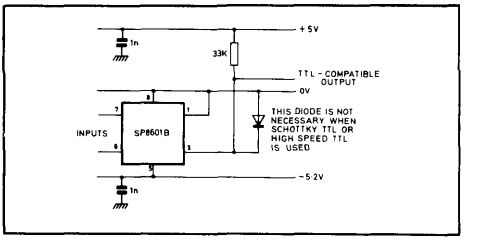


Fig. 9 TTL interface (fanout = 1 TTL gate)

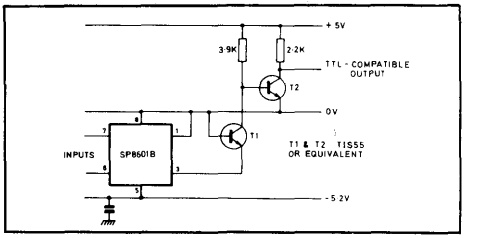


Fig. 10 High fanout TTL interface

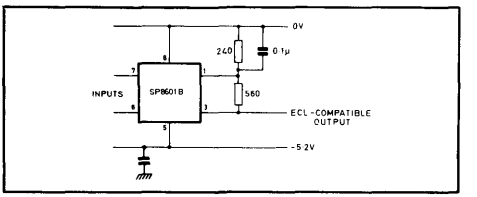


Fig. 11 ECL II interface

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	
V_{CC}—V_{EE}	10 V
Input voltage V_{in}	Not greater than the supply voltage in use
Bias voltage on outputs	
V_{out}—V_{EE}	14 V
(see Operating Notes)	
Operating junction temperature	+175°C
Storage temperature	−55°C to +175°C

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8602 A&B
500MHz÷2

The SP8602 is a fixed ratio ECL÷2 counters with maximum specified I/P frequencies of 500. MHz. The operating temperature range is specified by the final coding letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C.

The device can be operated with single input drive or with double, complementary, input drive; in both cases the input is normally capacitively coupled to the signal source. Two complementary emitter follower outputs are provided.

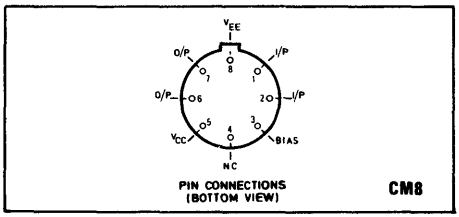


Fig. 1 Pin connections

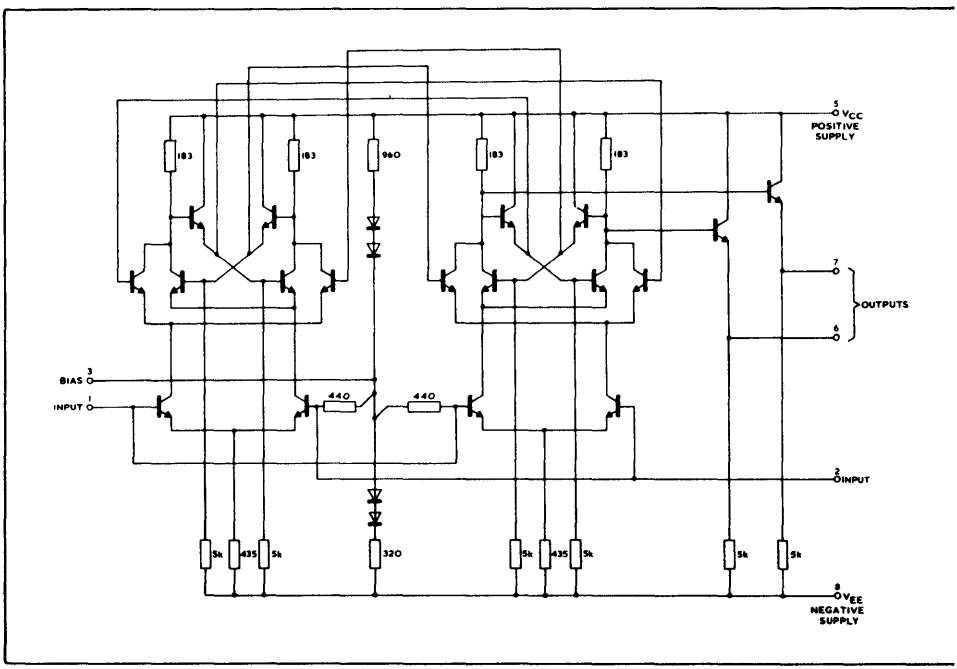


Fig. 2 Circuit diagram (all resistor values are nominal)

LECTRICAL CHARACTERISTICS

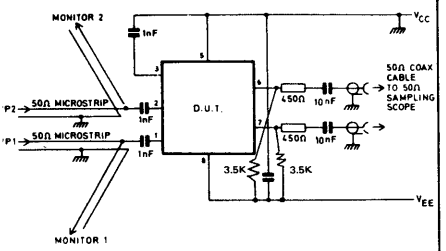
Test conditions (unless otherwise stated)

T_{amb} 'A' Grade	−55°C to +125°C
'B' Grade	0°C to +70°C
Operating supply voltage: V_{cc}	OV
V_{ee}	−5.2V± 0.25V
Input voltage (single drive- other input and bias decoupled to ground plane)	400 to 800 mV p-p
Input voltage (double drive- bias decoupled to ground plane)	250 to 800 mV p-p
Output load	500Ω and 3pF

Characteristic	Type	Value				Conditions
		Min.	Typ.	Max.	Units	
Max. input freq.	SP8602A,B.	500			MHz	V_{ee} = −5.2V
Min. input freq. with sinusoidal input			20	40	MHz	
Min. slew rate of square wave input for correct operation			30	100	V/μS	single input drive
Output voltage swing		400			mV	V_{ee} = −5.2V T_{amb} = −55°C to +70°C
Output voltage swing		350			mV	V_{ee} = −5.2V T_{amb} = +125°C I/P freq. = 500 MHz
Power supply drain current			12	20	mA	V_{ee} = −5.2V See note 1

OTES

In practice, the 3.5kΩresistors specified in the test circuit (Fig.3) are not essential; omission of these resistors will reduce the maximum pply current to 18mA.



Note: The values of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig. 3 Test circuit

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{cc} - V_{ee}$	8V
Input voltage V_{in}	Not greater than the supply voltage in use
Output current I_{out}	10 mA
Operating junction temperature	+150°C
Storage temperature range	−55°C to +150°C

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the output emitter-followers are inadvertently shorted to ground. All components used in the circuit layout should be suitable for the frequencies involved, and outside a controlled impedance environment, leads and connections should be kept short to minimise stray inductance.

The signal source is normally capacitively coupled to the input. A 1000pF capacitor is usually sufficient. If the input signal is likely to be interrupted a 15KΩ resistor should be connected between the input and the negative rail. In the single drive case it is preferable to connect the resistor to the input not in use – in the double drive case either input can be used. The addition of the input pulldown resistor causes a slight loss of input sensitivity, but it prevents circuit oscillation under no-sign conditions.

The input waveform may be sinusoidal, but belo about 40 MHz the operation of the circuit becom dependent on the slew rate of the input rather than th amplitude. A square wave input with a slew rate of mo than 100 V/μS will permit correct operation down to D(

The output voltage swing can be increased by th addition of a DC load to the output emitter follower Pulldown resistors of 1.5 K to the negative rail provide a increase of typically 25% in the output voltage swing.

APPLICATION NOTES

SP8602B interfacing to E C L 10 000 and E C L III

By increasing the output voltage swing using extern pulldown resistors (see operating notes), the SP8602B can coupled directly into an E C L III or E C L 10 000 gate, bu there is a reduction of the noise immunity. Where noi immunity is important the device can be connected to a E C L 10 000 or E C L III line receiver.

Divide-by-16 frequency scaler.

The SP8602B interfacing with the SP8601B a high-speed TTL to give a divide-by-16 frequency scal is shown in Fig. 4.

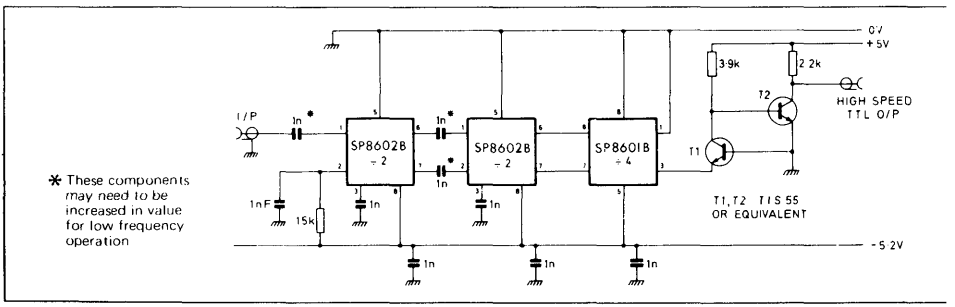


Fig. 4 Divide-by-16 frequency scaler

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8605 B & M 1.0GHz ÷ 2
SP8606 B & M 1.3GHz ÷ 2

The SP8605/6 UHF counters are fixed ratio ÷ 2 synchronous emitter coupled logic counters with, in the case of the SP8606 a maximum operating frequency in excess of 1.3GHz, over a temperature range 0° C to 70° C (B Grade) and —40° C to +85° C (M Grade). The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100-ohm lines and interfacing to ECL with the same positive supply. The SP8605/6 require supplies of 0V and —5.2V ±0.25V).

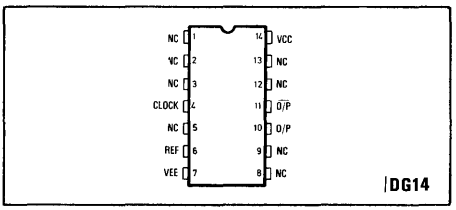


Fig. 1 Pin connections

FEATURES

- DC to 1.3GHz Operation
- 0°C to 70°C (B Grade) and —40°C to +85°C (M Grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range.
- Complementary Emitter Follower O/Ps.
- ECL III Compatible.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 10V
Input voltage	V_{INac} 2.5V p — p
Output current	15mA
Storage temperature range	—55° C to +150° C
Maximum operating junction temperature	+150° C

APPLICATIONS

- UHF Instrumentation, including Counters and Timers.
- Prescaling for UHF Synthesisers.

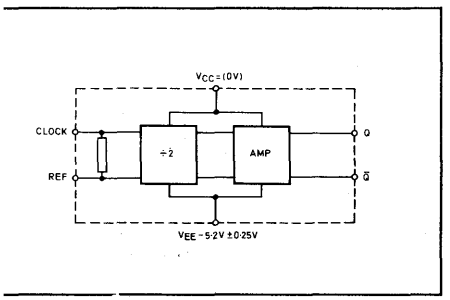


Fig. 2 Functional diagram

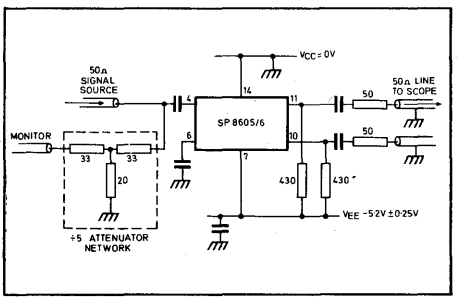


Fig. 3 Toggle frequency test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: B Grade 0° C to +70° C
M Grade −40° C to +85° C
Supply voltage V_{CC} = OV
V_{EE} = −5.2V ± 0.25 V
Input voltage 400 — 1000mV p — p

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. toggle frequency	SP8606B SP8605B	1.3 1.0			GHz GHz	
Min. toggle frequency for correct operation with sine wave input	All			150	MHz	V_{IN}=600mv to 1.0v p-p
Min. slew rate for sq. wave input to guarantee operation to 0Hz.	All			200	V//us	
Output voltage swing	All	500	600		mV	430 Ω to V_{EE}
Power supply drain current	All		70	100	mA	V_{EE}=−5.45V, No load

TOGGLE FREQUENCY TEST BOARD LAYOUT
1. All connections to the device are kept short.
2. The capacitors are leadless ceramic types.
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

OPERATING AND APPLICATION NOTE

The SP8605/6 dividers are very simple to use but normal high frequency rules should be followed for optimum performance, for example, all connections should be kept short, the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400 ohm resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane. This decoupling completes the input signal path to th device and therefore must be very low inductance fo optimum performance. The sensitivity of the device ca be increased by DC coupling the input signal abou earth (see Fig. 4).

V_{CC} − V_{EE} should be kept inside the specifie 5.2 volts ± 0.25 volts but the actual value of Vc relative to earth is not very critical and can be varie between 2.7V and 3.3V with only a small effect o performance. A Vcc of about 3.0V is the optimum fc full temperature range operation.

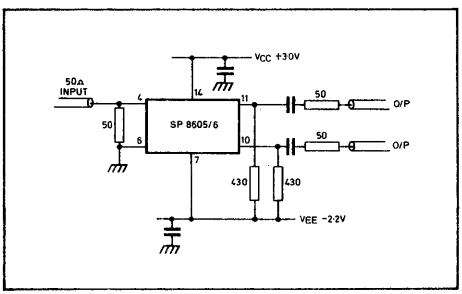


Fig. 4 Circuit for using the input signal about earth potential

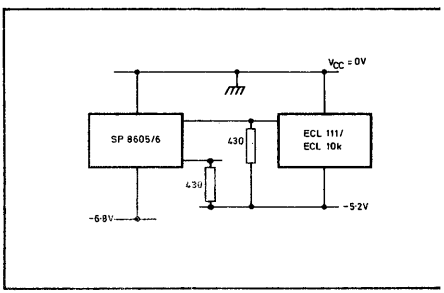


Fig. 5 Interfacing SP8605/6 series to ECL 10K and ECL III

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self oscillate with an output frequency of approximately 400MHz. This can be prevented by connecting a 10Kohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8605/6 will miscount with low frequency sinewave inputs of slow ramps. A slew rate of 200V//us or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL 10K or ECL III (See Fig. 5.). The unused output should be connected to a load resistor as shown to reduce output distortion.

The input impedance of the SP8605/6 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is generally enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The SP8605/6 can be used in instrumentation for direct counting applications up to 1.3GHz and in frequency synthesisers.

Plessey
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1641 Kaiser Avenue,
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SP8000 SERIES

HIGH-SPEED DIVIDERS

SP8607 A&B

600 MHz ÷ 2

The SP8607 is a divide-by-2 counter with a minimum guaranteed toggle frequency of 600 MHz over a 0°C to +70°C temperature range. The device is designed for capacitive coupling to the signal source to either of the two inputs and it has two complementary emitter follower outputs. Power dissipation is typically only 70mW with a 5.2V supply.

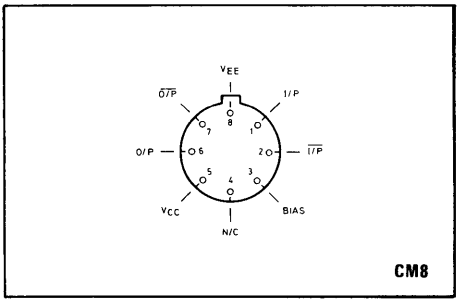

Fig.. 1 Pin connections

FEATURES

- 600 MHz Operation
- −55°C to 125°C Guaranteed for 'A' grade
- Only 70mW Dissipation at 5.2V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Connections as test circuit, Fig. 3
T_{amb}: (A grade) −55°C to +125°C
(B grade) 0°C to +70°C
Supply voltage V_{CC} = 0V
V_{EE} = −5.2V ± 0.25V
Specified input voltage range: 400 to 800mV p-p

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage $\|V_{CC} - V_{EE}\|$	8V
Input Voltage DC	≤ Supply
Input Voltage AC	2.5V p−p
Output Current	15mA
Operating Junction Temp.	+150°C
Storage Temp Range	−55°C to + 150°C

Characteristic	Value			Units	Conditions
	Min	Typ.	Max		
Max. toggle frequency	600	800		MHz	
Min. input frequency (sine wave)		50		MHz	
Min. slew rate of square wave input for correct operations to OHz		40	100	V/μs	
Output voltage swing	400			mVp-p	V_{EE} = −5.2V, f_{in} = 600 MHz
Output voltage levels					
V_{OH}		−0.75		V	f_{in} = OHz
V_{OL}		−1.5		V	
Input impedance		400		Ω	f_{in} = OHz
O/P pulldown resistors		4.0		kΩ	
Bias voltage level		−2.6		V	2.7kΩ resistor from pin 3 to V_{CC}
Power supply drain current		14	18	V	V_{EE} = −5·2V

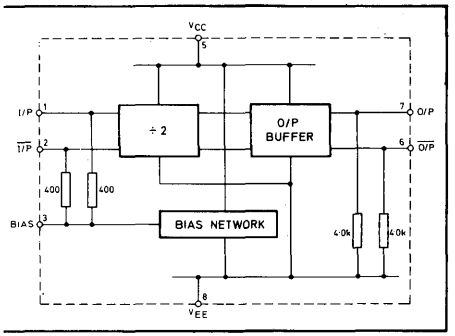

Fig. 2 SP8607 block diagram

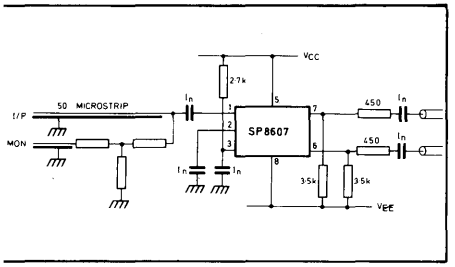

Fig. 3 Test circuit for SP8607

OPERATING NOTES

All components used with the SP8607 should be suitable for the frequencies involved, resistors and capacitors should be of low inductance types and unterminated loads should be kept short to minimise uncounted reflections. The test circuit uses positive earth because this minimises noise problems and the danger of accidently shorting the O/P transistors to a negative voltage. However, the device will operate satisfactorily and to the specification, with a negative earth provided that the positive supply is well decoupled to the UHF earth.

There are two complementary inputs connected to an internally-generated temperature-compensated bias point via two 400 ohm resistors. The signal source would normally be capacitively coupled to one of the inputs and the other should be decoupled to earth. If two complementary input signals are available (when cascading SP8607s for example) both inputs should be used

The input signal can be directly connected to the device either by using a voltage dropping network or by using split power supplies (see Fig. 4). In this mode the device is very tolerant of the actual values of V_{CC} and V_{EE} although $V_{CC} - V_{EE}$ should stay within 5.2V ± 0.25V. A 2.7kΩ resistor is connected from V_{CC} to the bias pin in the test circuit because this greatly improves the device's ability to operate with large input signals

It is important that pins 2 and 3 are decoupled by a capacitor in the range 100 – 1000pF because device sensitivity can be reduced by decoupling to a poor earth

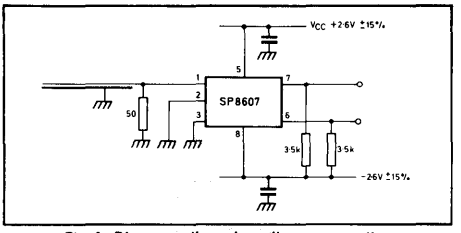

Fig. 4 Direct coupling using split power supplies

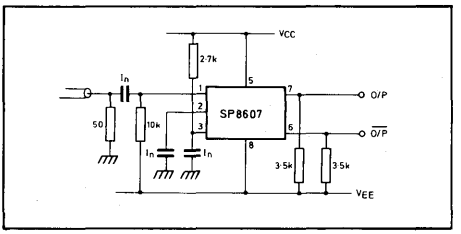

Fig. 5 SP8607 with input pulldown resistor

In the absence of an input signal, or if the input signal is of very low amplitude, the device may give an output signal of about 250 MHz. This is due to the balanced nature of the internal ÷ 2 circuit and can be stopped if required by connecting a 10 kohm resistor between the input and the negative rail. (See Fig. 5). This causes a drop in sensitivity of about 100 mV but typical devices still easily meet the 400 – 800 mV input amplitude specification. With sine wave inputs below 50MHz the SP8607 miscounts because the slew rate of the input signal is too slow. Below this frequency a square wave input is needed with a slew rate of 100V/μ or more.

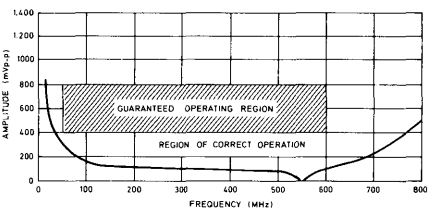

Fig. 6 Typical operating characteristic

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP8608 B & M 1.0GHz ÷ 2
SP8609 B & M 1.3GHz ÷ 2

The SP8608/9 UHF counters are fixed ratio ÷2 asynchronous emitter coupled logic counters with, in the case of the SP8609 a maximum operating frequency in excess of 1.3GHz. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100-ohm lines and interfacing to ECL with the same positive supply. The SP8608/9 require supplies of OV and —6.8V (±0.35V).

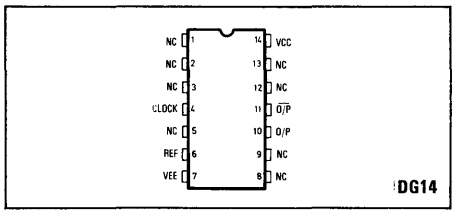

Fig. 1 Pin connections

FEATURES

- DC to 1.3GHz Operation
- 0°C to 70°C (B Grade) and —40°C to +85°C (M Grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range.
- Complementary Emitter Follower O/Ps. ECL III Compatible.

APPLICATIONS

- UHF Instrumentation, including Counters and Timers.
- Prescaling for UHF Synthesisers.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 10V
Input voltage	V_{INac} 2.5V p-p
Output current	15mA
Storage temperature range	—55° C to +150° C
Maximum operating junction temperature	+150° C

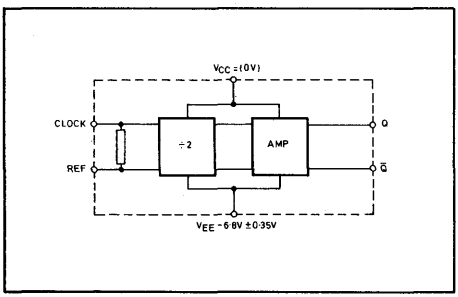

Fig. 2 Functional diagram

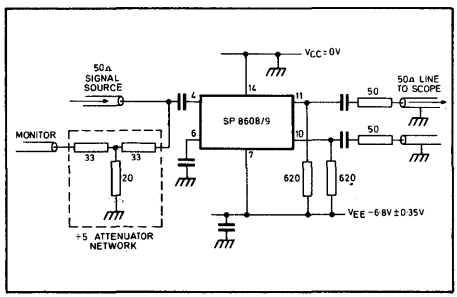

Fig. 3 Toggle frequency test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: B Grade 0° C to +70° C
M Grade −40° C to +85° C
Supply voltage V_{CC} = 0V
V_{EE} = −6.8V ±0.35V
Input voltage 400 to 1000mV p-p

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. toggle frequency	SP8608B & M SP8609B & M	1.3 1.0			GHz GHz	
Min. toggle frequency for correct operation with sine wave input	All			150	MHz	V_{IN}=600mv to 1.0v p-p
Min. slew rate for sq. wave input to guarantee operation to 0Hz.	All			200	V/µs	
Output voltage swing	All	500	600		mV	620 Ω to V_{EE}
Power supply drain current	All		70	100	mA	V_{EE}= −7.15V No load

TOGGLE FREQUENCY TEST BOARD LAYOUT
. All connections to the device are kept short.
. The capacitors are leadless ceramic types.
. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

OPERATING AND APPLICATION NOTE

The SP8608/9 dividers are very simple to use but normal high frequency rules should be followed for optimum performance, for example, all connections should be kept short, the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400 ohm resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane. This decoupling completes the input signal path to the device and therefore must be very low inductance for optimum performance. The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 4).

V_{CC} − V_{EE} should be kept inside the specified 6.8 volts ± 0.35 volts but the actual value of V_{CC} relative to earth is not very critical and can be varied between 4.2V and 5.0V with only a small effect on performance. A V_{CC} of about 4.6V is the optimum for full temperature range operation.

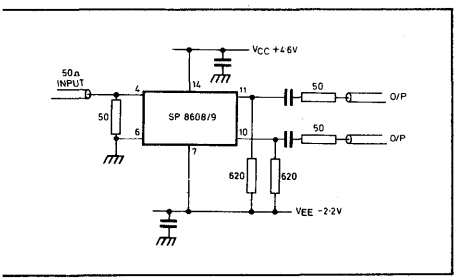

Fig. 4 Circuit for using the input signal about earth potential

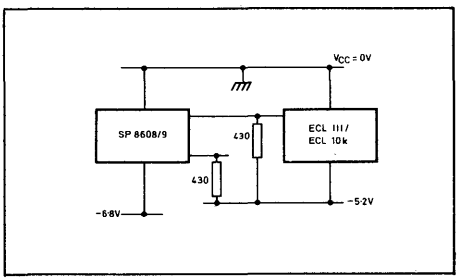

Fig. 5 Interfacing SP8608/9 series to ECL 10K and ECL III

In the absence of an input signal the devices will self oscillate with an output frequency of approximately 400MHz. This can be prevented by connecting a 10Kohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8608/9 will miscount with low frequency sinewave inputs of slow ramps. A slew rate of 200V//μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL 10K or ECL III (See Fig. 5.). The unused output should be connected to a load resistor as shown to reduce output distortion.

The input impedance of the SP8608/9 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is generally enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The SP8608/9 can be used in instrumentation for direct counting applications up to 1.3GHz and in frequency synthesisers.

Plessey Semiconductors
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Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8610B & M 1.0GHz ÷ 4
SP8611 B & M 1.5GHz ÷ 4

The SP8610/11 UHF counters are fixed ratio ÷4 asynchronous emitter coupled logic counters with, in the case of the SP8611B, a maximum operating frequency in excess of 1.5GHz over a temperature range of 0°C to +70°C. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100 Ω lines and interfacing to ECL with the same positive supply. The SP8610/11 require supplies of 0V and —5.2V (±0.25V).

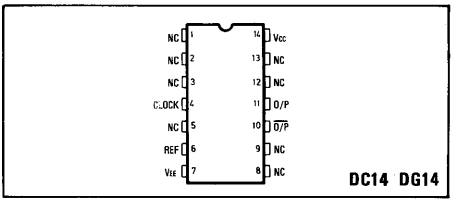

Fig. 1 Pin connections

FEATURES

- DC to 1.5GHz operation
- 0°C to +70°C (B grade) and —40°C to +85°C (M grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range
- Complementary Emitter Follower O/Ps, ECL III Compatible.

APPLICATIONS

- UHF Instrumentation, including Counters and Timers
- Prescaling for UHF Synthesisers

QUICK REFERENCE DATA

- Vcc = 0V VEE = —5.2V ± 0.25V
- Input Voltage Range 400mV to 1.0V
- Output Voltage Swing 600mV Typ.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	Vcc — VEE 10V
Input voltage	VINac 2.5V p–p
Output current	15mA
Storage temperature range	—55°C to +150°C
Maximum operating junction temperature	+150°C

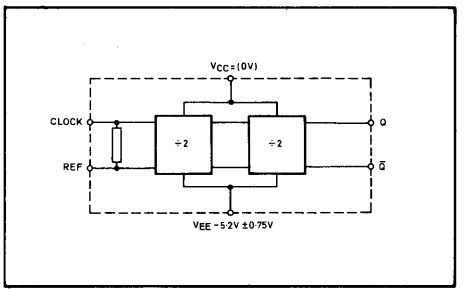

Fig. 2 Functional diagram

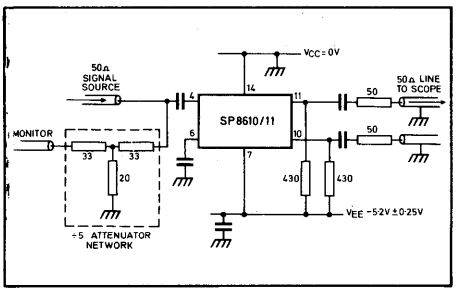

Fig. 3 Toggle frequency test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 0°C to +70°C ('B' Grade)
−40°C to +85°C ('M' Grade)
Supply voltage V_{CC}=0V
V_{EE}=5.2V±0.25V
Input voltage 400 to 1000mV

Characteristic	Type	value			Units	Conditions
		Min.	Typ.	Max.		
Max. toggle frequency	SP8611B SP8611B SP8610B	1.3 1.5 1.0			GHz GHz GHz	V_{NI}=400mV to 1V p-p V_{IN}=800mV to 1V p-p V_{IN}=400mV to 1V p-p
Min. toggle frequency for correct operation with sine wave input	All			150	MHz	V_{IN}=600mV to IV p-p
Min. slew rate for square wave input to guarantee operation to 0Hz	All			200	V/µs	
Output voltage swing	All	500	600		mV	
Power supply drain current	All		70	100	mA	V_{EE}= −5.45V No load

TOGGLE FREQUENCY TEST BOARD LAYOUT
1. All connections to the device are kept short.
2. The capacitors are leadless ceramic types.
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

OPERATING AND APPLICATION NOTE

The SP8610/11 dividers are very simple to use but normal high frequency rules should be followed for optimum performance. For example, all connections should be kept short and the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400Ω resistor connecting the input to a reference voltage; this biases the input in the centre of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the ground plane. This decoupling completes the input signal path to the device and therefore must be very low inductance for optimum performance. The sensitivity of the device can be increased by DC coupling the input signal about |ground|(see Fig. 4).|

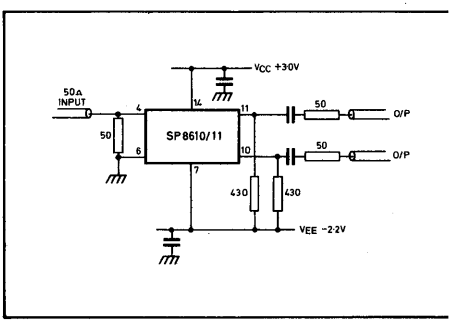

Fig. 4 Circuit for using the input signal about ground

|Vcc — Vee| should be kept inside the specified 5.2V ± 0.25V but the actual value of Vcc relative to ground is not very critical and can be varied between 2.7V and 3.3V with only a small effect on performance. A Vcc of about 3.0V is the optimum for full temperature range operation.

In the absence of an input signal both DC coupled and capacitively coupled circuits will self-oscillate with an output frequency of approximately 200MHz. This can be prevented by connecting a 10kΩ resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8610/11 will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL10K or ECL III (see Fig. 5).

The input impedance of the SP8610/11 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity. So, although it can load the signal source significantly, there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is when the input sensitivity is worst.

The SP8610/11 can be used in instrumentation for direct counting applications up to 1.5GHz and in frequency synthesisers.

In a frequency synthesiser the SP8610/11 and the SP8643 can be used together (see Fig. 6).

Fig. 5 Interfacing SP8610/11 to ECL10K and ECL III

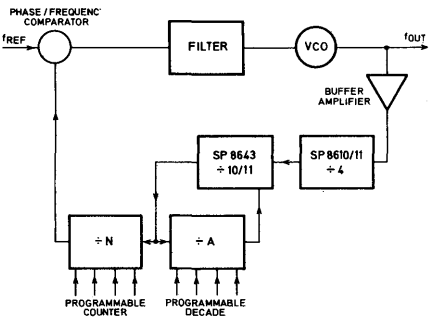

Fig.6 A 1.5GHz synthesiser loop

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8619B & M 1.5GHz ÷ 4
SP8617B & M 1.3GHz ÷ 4

The SP8619 series of UHF counters are fixed ratio ÷4 asynchronous emitter coupled logic counters with, in the case of the SP8619B a maximum operating frequency in excess of 1.5GHz. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100 ohm lines and inter facing to ECL with the same positive supply. The SP8619 series require supplies of 0V and −6.8V (± 0.35V).

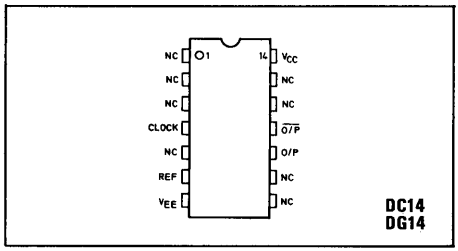

Fig. 1 Pin connections

FEATURES

- DC to 1.5GHz Operation
- 0°C to 70°C (B Grade) and −40°C to +85°C (M Grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range.
- Complementary Emitter Follower O/Ps, ECL10K and ECL111 Compatible

APPLICATIONS

- UHF Instrumentation, Including Counters and Timers
- Prescaling for UHF Synthesisers

QUICK REFERENCE DATA

- V_{CC} = 0V V_{EE} = −6.8V ± 0.35V
- Input Voltage Range 400mV to 1.2V p-p
- Temperature Range 0°C to +70°C
- Output Voltage Swing 800mV Typ.

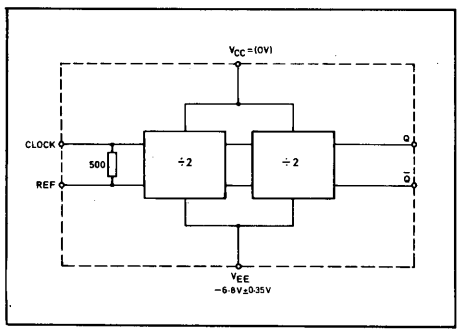

Fig. 2 Functional diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $|V_{CC} - V_{EE}|$ 10V
Input voltage V_{INac} 2.5V p-p
Output current 15mA
Storage temperature range −55°C to +150°C
Maximum operating function temperature +150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb}: B Grade 0° C to +70° C
M Grade −40° C to +85° C
Supply voltage $V_{CC} = 0V$
$V_{EE} = -6.8V \pm 0.35V$
Input voltage 400 to 1200mV p-p

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. toggle frequency	SP8619	1.5			GHz	
	SP8617	1.3			GHz	
Min. toggle frequency for correct operation with sine wave input	All			150	MHz	V_{IN} = 600mV to 1.2Vp-p
Min. toggle frequency for correct operation with sine wave input	All			100	MHz	V_{IN} = 800mV to 1.2Vp-p
Min slew rate for square wave input to guarantee operation to 0Hz	All			200	V/μs	
Output voltage swing	All	600	800		mV	
Power supply drain current	All		80	110	mA	V_{EE} = −7.15V

Toggle Frequency Test Board Layout

. All connections to the device are kept short
2. The capacitors are leadless ceramic types
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

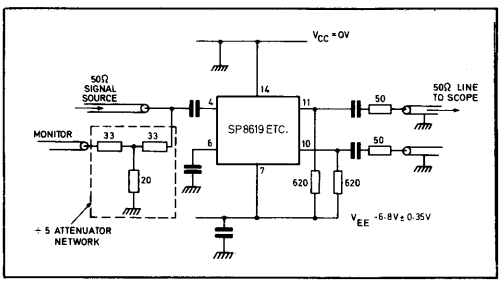

Fig. 3 Toggle frequency test circuit

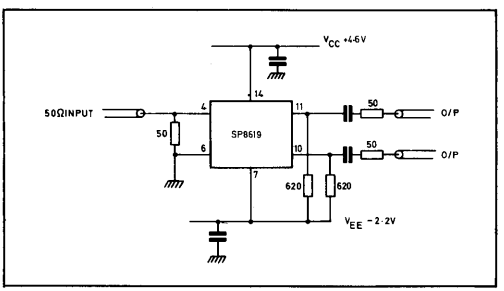

Fig. 4 Circuit for using the input signal about earth potential

OPERATING AND APPLICATION NOTE

The SP8619 series of dividers are very simple to use but normal high frequency rules should be followed for optimum performance - for example, all connections should be kept short and the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400 ohm resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane.

The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 4).

$|V_{CC} - V_{EE}|$ should be kept inside the specified 6.8V $\pm$0.35V but the actual value of V_{CC} relative to earth is not very critical and can be varied between 4.2V and 5.0V with only a small effect on performance. A V_{CC} of about 4.6V is the optimum for full temperature range operation.

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self-oscillate with an output frequency of approximately 300MHz. This can be prevented by connecting a 10k ohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8619 will miscount with low frequency sine-wave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL 10K or ECL III (see Fig. 5).

The input impedance of the SP8619 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum input signal requirement. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The SP8619 series can be used in instrumentation for direct counting applications up to 1.5GHz and in frequency synthesisers.

In a frequency synthesiser, the SP8619 and the SP8643 can be used together (see Fig. 6).

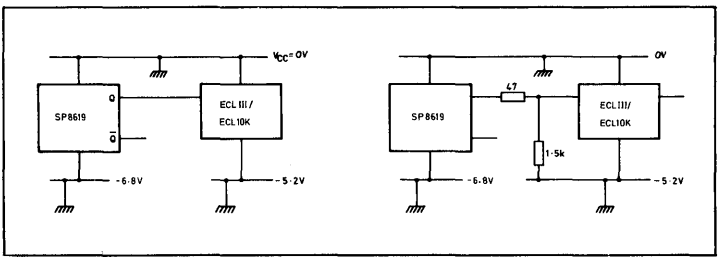

Fig. 5 Interfacing SP8619 series to ECL 10K and ECL III

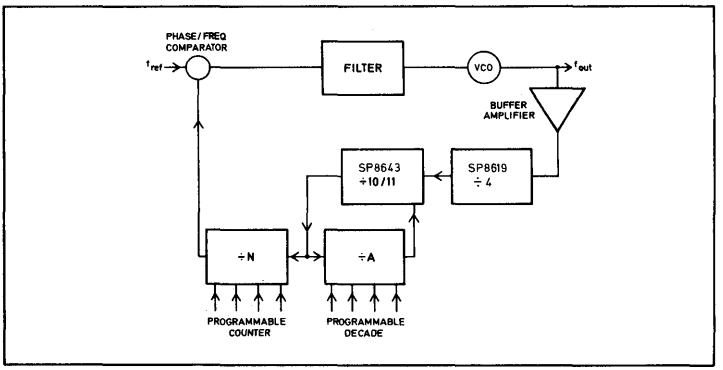

Fig. 6 A 1.5GHz synthesiser loop

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES

HIGH SPEED DIVIDERS

÷5 COUNTERS

SP8620 A&B

(400MHz)

The SP8620 is a fixed ratio emitter-coupled logic ÷5 counter with specified input frequency range of DC to 400MHz. The operating temperature is specified by the final coding letter: -55°C to +125°C ('A' grade), 0°C to +70°C 'B' grade).

The counter is normally capacitively coupled to the signal source and is specified with an input signal range of 400–800mv p-p –4dBm to +22dBm). There are two bias points in the circuit that should be capacitively decoupled to the ground plane.

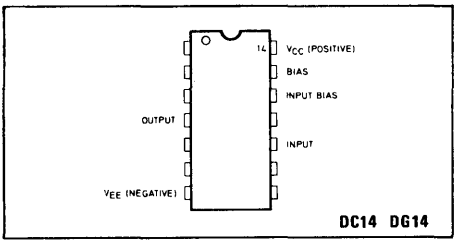

Fig.1 Pin connections (bottom view)

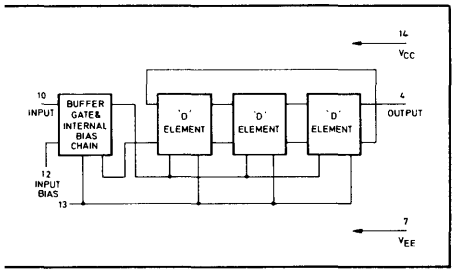

Fig.2 Circuit diagram (all resistor values are nominal)

FEATURES

- D.C. to 400MHz Operation.
- *Temperature Ranges of* –55°C to +125°C ('A' Grade), 0°C to +70°C ('B' Grade) Over Full Specified Input Range and Frequency

APPLICATIONS

- Frequency Counters and Timers
- Frequency Synthesisers

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

Tamb: 'A' grade: –55°C to +125°C
'B' grade: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{IN}	Not greater than supply
Output current I_{OUT}	15mA
Operating junction temperature	+150°C
Storage temperature	–55° to +150°C

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. input frequency	SP8620	400			MHz	
Min. input frequency with sinusoidal input			20	40	MHz	
Min. slew rate of square wave input for correct operation			30	100	V/μS	
Output voltage swing		400	800		mV	V_{EE} = –5.2V
Power supply drain current			55	70	mA	V_{EE} = –5.2V

OPERATING NOTES

It is recommended that a positive earth plane is used for the circuit layout, thus preventing damage if the output is short-circuited to earth.

The signal source is normally capacitively coupled to the input (see Fig. 3). A 1000pF capacitor is suitable at high frequencies, but if lower frequency operation is also required, say below 10MHz, then an additional capacitor should be connected in parallel. The device can be DC coupled if it is required – see Fig. 4.

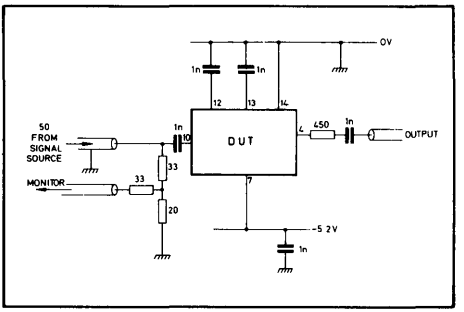

Fig.3 Test circuit

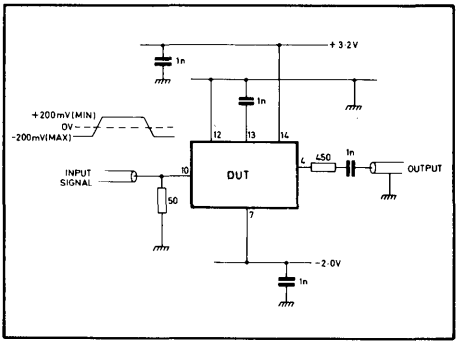

Fig.4 Divide by 16 frequency scaler

The circuit may self oscillate when there is no input signal or when the input signal is well below the specified input signal. This can be prevented by connecting a 15kΩ resistor between the input and the negative rail. This causes a loss in sensitivity of up to 100mV p-p.

The input waveform may be sinusoidal, but below about 20MHz the circuit tends to malfunction on minimum amplitude input signals and the condition becomes worse as the frequency is decreased. This is because correct operation of the circuit depends on the slew rate of the input signal. A square wave input with a slew rate greater than 100V/μS ensures correct operation down to DC.

The output swing of the devices can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5kΩ will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8620 devices to interface directly to ECL II devices with no loss in noise immunity. If the devices are required to interface to ECL III or ECL 10,000 then an interface similar to Fig. 5 should be used.

The values of the decoupling capacitors are not critical but they should be of a type suitable for the frequencies involved.

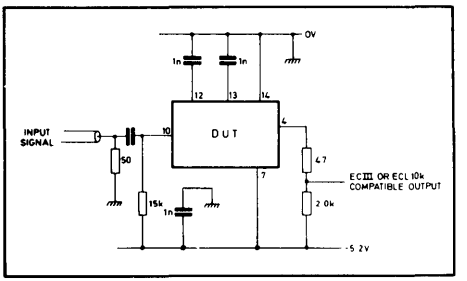

Fig. 5 Interfacing to ECL III or ECL 10,000

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Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES

HIGH SPEED DIVIDERS

SP8627 ÷ 80
SP8628 ÷ 100 (WITH RESET)
SP8629 ÷ 100

150 MHz PRESCALERS

The SP8629 is a fixed ratio ECL ÷ 100 counter with minimum guaranteed toggle frequency of 150MHz ver a −30°C to +70°C temperature range. The device an operate in the single-ended or differential input ode, and is typically capacitively coupled to the gnal source. An input amplifier is included to allow ge of extremely small amplitude high frequency signals. he output of the device is similar to Low Power chottky TTL and produces a square wave of frequency ut = $f_{in}/100$.

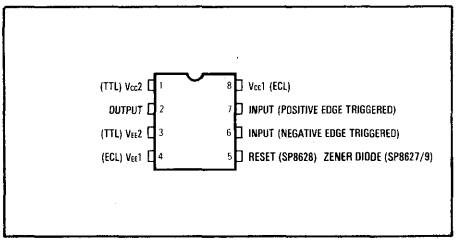

Fig. 1 Pin connections

EATURES

- Low Power 170mW typica
- High Frequency, DC to 150MHz, Small Input Amplitude
- Single Supply Operation 5.2v ± 10%
- Count Down Sequence avoids FM IF Harmonics
- ECL Dividers reduce Switching Transients
- ÷4 Reset on SP8628 Reduces Jitter on Frequency Display Systems

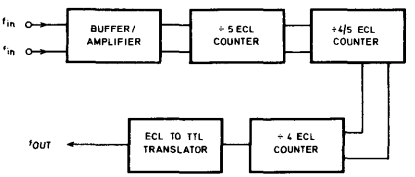

Fig. 2 SP8627/8/9 logic diagram

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

Power Supply Voltage	$\|V_{CC} - V_{EE}\|$	8V
Input Voltage	Vin (DC)	not greater than supply voltage
Output voltage	V_{OUT}	5.5V
Output current	I_{OUT}	40mA
Zener current	I_Z	20mA
Operating Junction temperature		150°C
Storage temperature range		−30°C to +85°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: + 5.2V ± 0.52V, V_{EE}: OV,
T_{amb}: 25°C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Maximum input frequency	f_{max}	150	200		MHz	V_{CC} = 5.2V, V_{IN} = 600mVp−p, single ended
Input voltage	$V_{IN}1$	200		1000	mVp−p	V_{CC} = 5.2V, single ended
Input voltage	$V_{IN}2$	100		1000	mVp−p	V_{CC} = 5.2V, differential
Minimum input frequency with sine wave	f_{sine}	10			MHz	V_{CC} = 5.2V, V_{IN} = 600mVp−p
Minimum slew rate of square wave input	dv/dt			50	V/μs	V_{CC} = 5.2V, V_{IN} = 600mVp−p
Logic 1 output voltage	V_{OH}	2.4			V	V_{CC} = Min, I_{OH} = −400/μA
		2.0			V	V_{CC} = Min, I_{OH} = −1.6mA
Output short circuit current	I_{OS}	−10		−40	mA	V_{CC} = Max
Logical 0 output voltage	V_{OL}			0.5	V	V_{CC} = Min, I_{OL} = 8mA
Supply current	I_{CC}		33	45	mA	V_{CC} = Max
Zener voltage, pin 5 (SP8627/9)	V_Z		6.3		V	I_Z = 5mA (see note 2)
Reset input voltage (SP8628)	$V_{IN(LO)}$			0.5	V	
	$V_{IN(HI)}$	2.4			V	
Reset input current (SP8628)	I_{IN}			−1.6	mA	V_{IN} = 0.5V

NOTE
All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

TYPICAL APPLICATIONS

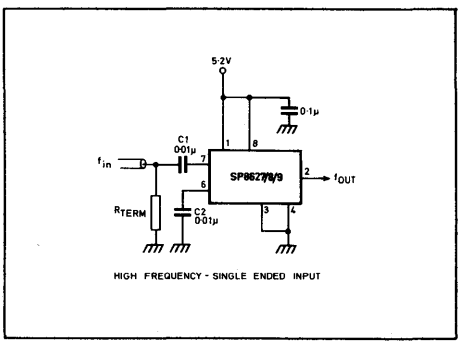

Fig. 3 High frequency, single-ended input

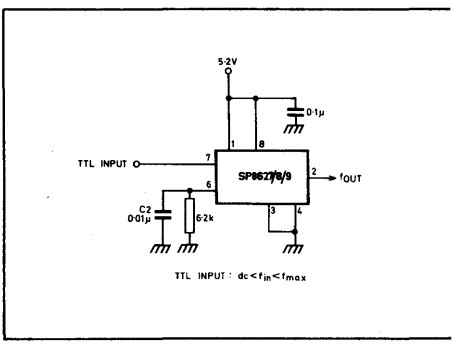

Fig. 4 TTL input (DC<f_{in}<f_{max})

)PERATING NOTES.

Two ground and two V_{CC} connections are provided, eparating the ECL stages from the TTL section, solating the noise transients inherent in the TTL tructure. In most cases, shorting the two grounds to a lood ground plane and the V_{CC}s to a wide V_{CC} bus vill provide sufficient isolation. All components used n the circuit layout should be suitable for the requencies involved and leads should be kept short to ninimise stray inductance.

The signal source is usually capacitively coupled to he input as shown in Fig. 3. In the single-ended mode a apacitor of 0.01 µF (C2) should be connected between he unused input and the ground plane to provide a lood high frequency bypass. The capacitor should be ncreased at lower frequencies. If the input is likely to ie interrupted, it may be desirable to connect a 100k Ω esistor between an input and ground. In the single nded mode it is preferable to connect the resistor to he unused input. The addition of the 100k Ω resistor auses a loss of input sensitivity, but prevents circuit scillations under no signal (open circuit) conditions.

The input waveform will normally be sinusoidal but elow 10MHz correct operation depends on the slew ate of the input signal. A slew rate of 50V/µs will nable the device to operate down to DC. The device vill operate with a TTL input signal as shown in Fig. 4 nd is DC coupled to the input.

The device can be used in phase locked loop pplications such as FM radio or other communications ands to prescale the input frequency down to a nore useable level. A digital frequency display system an also be derived separately or in conjunction with a hase locked loop, and it can extend the useful range f many inexpensive frequency counters to, typically, 00MHz

The on-chip Zener diode allows a simple stabilised ower supply to be constructed with the addition of a ew extra external components, as shown in Fig. 5, to he SP8627/9. The SP8628 has a 'reset' facility on pin 5. his input acts as a data inhibit to the final divide-by- our when a high level is applied (or the input is left pen circuit).

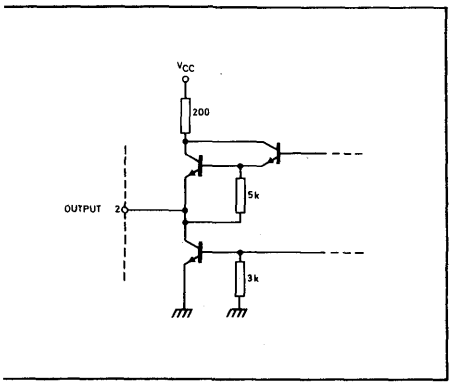

Fig. 7 Output circuit diagram

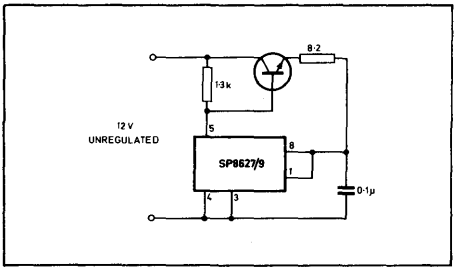

Fig. 5 Voltage regulator

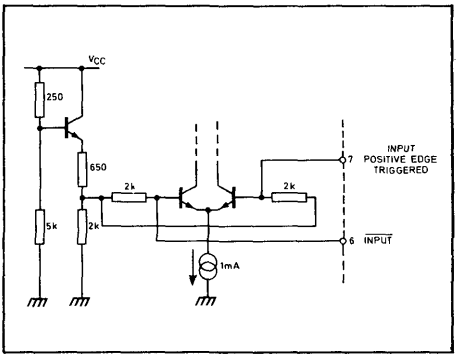

Fig. 6 Input circuit diagram

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Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8630 A&B
600MHz DECADE COUNTER

GENERAL DESCRIPTION

The SP8630 counter is a fixed ratio ÷ 10 circuit using emitter coupled logic, with maximum specified counting frequencies of 600 MHz over temperature ranges of −55°C to +125°C, 0°C to 70°C. A 6:4 mark/space square wave is provided at the emitter follower output. The input is normally single driven and capacitively coupled to the signal source. There are two bias points on the circuit which should be capacitively coupled to the ground plane.

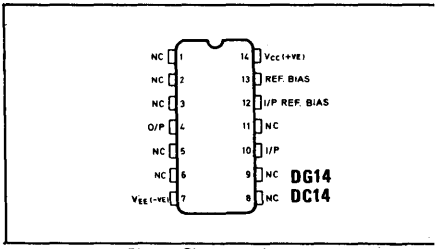
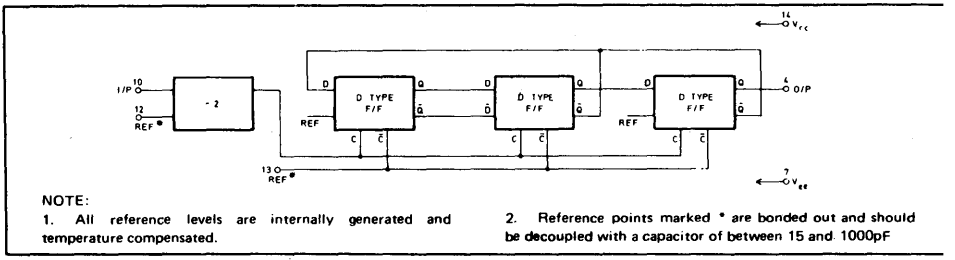


Fig. 1 Pin connections



NOTE:
1. All reference levels are internally generated and temperature compensated.
2. Reference points marked * are bonded out and should be decoupled with a capacitor of between 15 and 1000pF

Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless stated otherwise):

Tamb: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C

Operating supply voltage
V_{CC} 0V
V_{EE} −5.2V ± 0.25V
Input voltage 400 to 800 mV (p-p)
Output load 500Ω & 3pF.

NOTE: The maximum input frequency is guaranteed . V_{EE} = −5.2V. For typical operating characteristics wi power supply variations see Fig.5, which shows that t maximum operating frequency of a typical device increas with increasing power supply voltage

Characteristic	Type	Value			Units	Conditions
		Min	Typ	Max		
Max input freq.	SP8630	600			MHz	
Min input freq. with sinusoidal input			20	40	MHz	
Min. slew rate of square wave I/P for correct operation			30	100	V/μs	
Output voltage swing		400	600		mV	V_{EE} = −5.2V
Power supply drain current			70	95	mA	V_{EE} = −5.2V

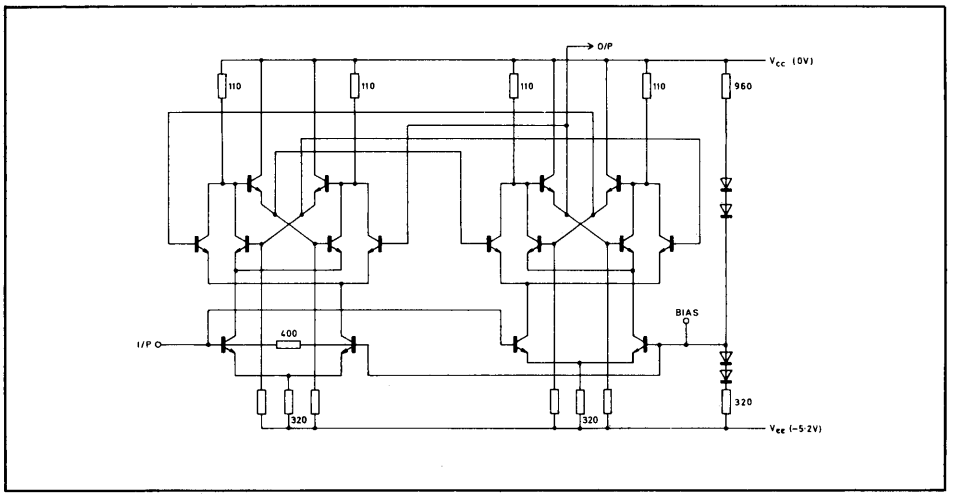


Fig. 3 Circuit diagram of 1st element (–2) showing input biasing arrangement

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the emitter follower outputs are inadvertantly shorted to ground.

The signal source is normally capacitively coupled to the input: 1000 pF is usually sufficient. If the input signal is likely to be interrupted a 15 k ohm resistor should be connected between the input pin and the negative rail to prevent circuit oscillation under no-signal conditions. The addition of the pulldown resistor causes a slight loss of sensitivity of the device, but this does not normally cause problems in practice.

The input waveform may be sinusoidal, but below 40 MHz the operation of the circuit becomes dependent on the slew rate of the waveform rather than the amplitude. A square wave input with a slew rate of 100 V/μs will allow correct operation down to DC. At high frequencies, increasing drive level above minimum typically increases the max. operating frequency by up to 25%

The output swing of the device can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5k ohms will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8630 device to drive directly into ECL II devices with no loss in noise immunity.

The value of capacitance needed for the decoupling capacitors is not critical. Values down to 15 pF have been found satisfactory in practice.

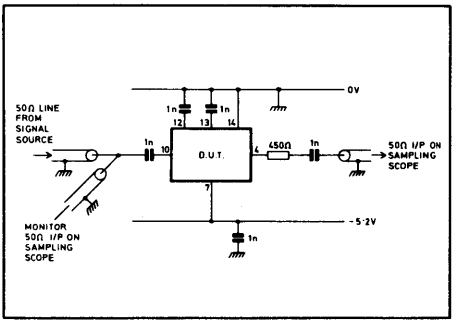


Fig. 4 Test circuit

Test Circuit Notes

The values of the coupling and decoupling capacitors are uncritical but they should be of a type and value suitable for the frequencies involved.

All connections should be physically short when not in a 50Ω environment to minimise reflections due to mismatching.

The +ve pin should be connected to a low impedance earth plane to minimise feed-through of the input signal to the output.

Typical Operating Characteristics

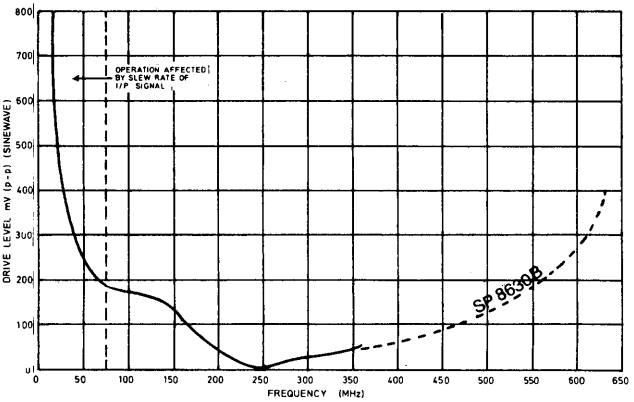


Fig. 5 Minimum drive level v. input frequency at +25 C

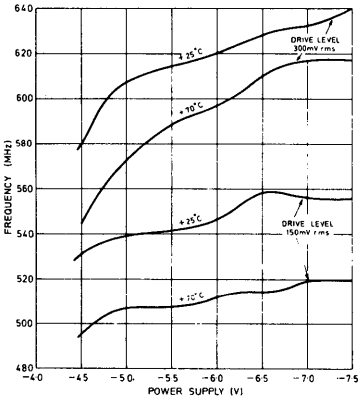


Fig. 6 Max. operating frequency v. power supply voltage for a typical SP8630B

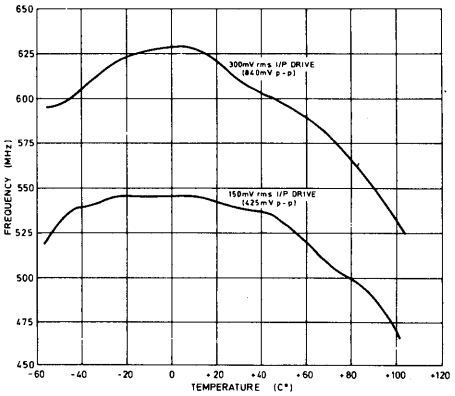


Fig. 7 Max. operating frequency v. ambient temperature for a typical SP8630B (Vcc = −5.2V)

APPLICATION NOTES

Direct coupling to the SP8630

It can be seen from the circuit diagram that the input arrangement of the SP8630 series is not compatible with the normal ECL logic levels. The input reference level is approximately −3.2 volts but it is not well defined and has a temperature coefficient of approximately −1.6 mV/°C. If DC coupling is required, the input would have to be larger than would be the case with capacitive coupling.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	8V.
Input voltage V_{IN}	Not greater than the supply voltage in use
Output current I_{OUT}	15 mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP8634B
÷ 10 700 MHz

The SP8634B, is a divide-by-ten circuit th binary coded decimal outputs for opera- ɔn from DC up to specified input frequencies 700 MHz, over a guaranteed temperature ŋge of 0°C to +70°C.

These devices, optimised for counter applications in tems using both ECL and TTL, are intended to be ɛrated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset ʃorces the 0000 state regardless of the state of the other inputs.

ɛATURES
- Direct gating capability at up to 700 MHz
- TTL- compatible BCD outputs
- TTL- and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

ᵖPLICATIONS
- Counters
- Timers
- Synthesisers

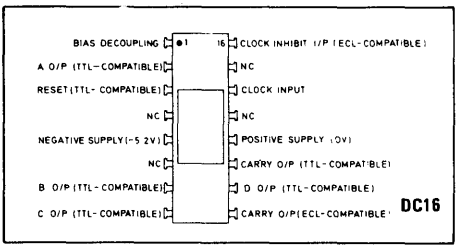

Fig. 1 Pin connections (top)

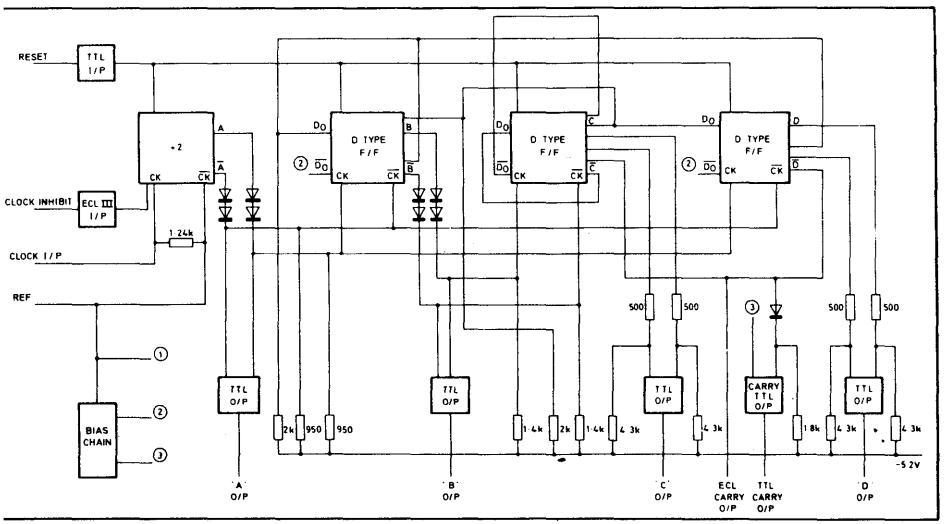

Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated)

T_{amb}		0°C to +70°C
Power Supplies	V_{CC}	0V
	V_{EE}	−5.2V ± 0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Input (pin 14)					
Max. input frequency SP8634B	700			MHz	Input voltage 400-800mV p-p
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
Logic levels					
High (inhibit)	−0.960			V	T_{amb} = +25°C
Low			−1.650	V	(see Note 1)
Edge speed for correct operation at maximum clock I/P frequency			2.5	ns	10%–90%
Reset input (pin 3)					
Logic levels					
High (reset)	See Note 2				
Low			+0.4	V	
Reset ON time	100			ns	
TTL outputs ABCD (pins 2,7,8,10)					See Note 3 and Fig. 4
Output Voltage					
High	+2.4			V	10k Ω resistor and TTL gate from O/P
Low			+0.4	V	to +5V rail
TTL carry output (pin 11)					
Output Voltage					
High state	+2.4			V	5kΩ resistor and 3 TTL gates from o/p
Low			+0.4	V	to 5V rail
ECL carry output (pin 9)					
Output Voltage					
High	−0.975			V	T_{amb} = +25°C External current
Low			−1.375	V	= 0mA (See Note 4)
Power supply drain current		75	90	mA	V_{EE} = 5.2V

NOTES

1. The clock inhibit input levels are compatible with ECL III and ECL 10000 levels throughout the temperature range 0°C to +70°C.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8kΩ resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series device.
3. These outputs are current sources which can be readily made TTL-compatible voltages by connecting them to +5V via 10kΩ resistors.
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

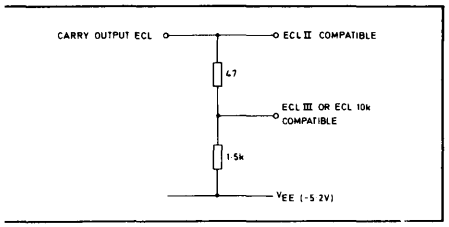

Fig. 3 ECL III/ECL 10000 interfacing

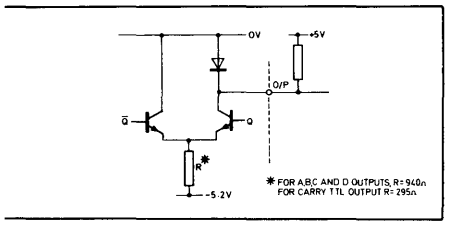

Fig. 4 TTL carry and ABCD output structure

)PERATING NOTES

The devices are intended to be used with TTL and ECL ı a counting system – the ECL and the decade counter eing connected between voltage rails of OV and –5.2V nd the TTL between voltage rails of OV and +5.0V. rovided that this is done ECL and TTL compatability is chieved (see Figs. 4 and 5).

The clock is normally capacitively coupled to the signal ɔurce: a 1000pF UHF capacitor is normally adequate. If ɔw frequency operation is required the 1000pF capacitor ıould be connected in parallel with a higher value apacitor. The bias decoupling (pin 1) should be connected ɔ earth via a capacitor – preferably a chip type – but in ny case a low inductance type suitable for UHF pplications. The devices normally have an input amplitude perating range far greater than the specified 400 to 00 mV pk/pk. However, if the decoupling capacitor is not f a UHF type, or it is connected to an earth point that has significant impedance between the capacitor and the V_{CC} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 68kΩ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL-compatible outputs (fanout = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

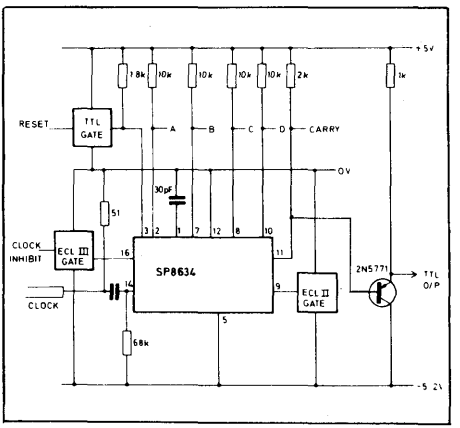

Fig. 5 Typical application configuration

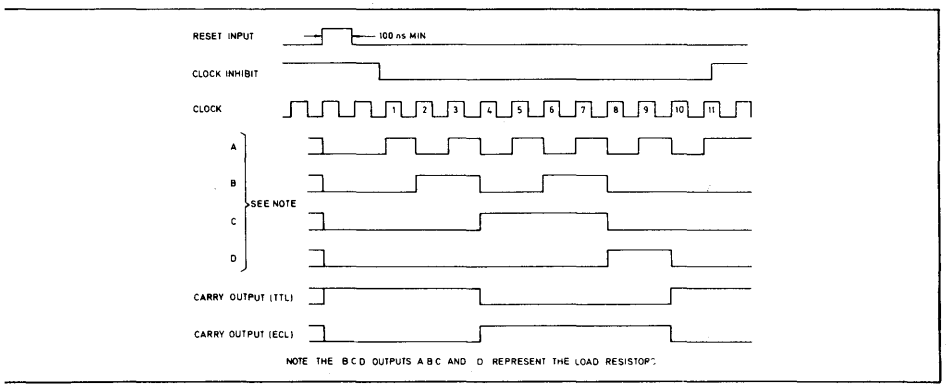

Fig. 6 Decade counter timing diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage ($V_{CC} - V_{EE}$	8V
Clock inhibit voltage	Not greater than the supply voltage in use
Clock input voltage	2V pk/pk
Bias voltage (V_{OUT}) on BCD outputs, $V_{OUT} - V_{EE}$ (10kΩ resistor in series with output)	11V
Bias voltage (V_{OUT}) on TTL carry output, $V_{OUT} - V_{EE}$ (1.2kΩ resistor in series with output)	11V
Output current from ECL carry output (I_{OUT}) (Note: the device will be destroyed if the ECL output is shorted to the negative rail)	10mA
Operating junction temperature	+150°C
Storage temperature range	−55°C to +150°C

QUICK REFERENCE DATA

■ Power Supplies	V_{CC}	0V
	V_{EE}	5.2V ± 0.25V
■ Range of clock input amplitude		400-800mV p-p
■ Operational temperature range		0°C to +70°C
■ Frequency range with sinusoidal I/P		40-700 MHz
■ Frequency range with square wave I/P		DC to 700 MHz

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SP 8000 SERIES

HIGH SPEED DIVIDERS

SP 8643A & B 350 MHz

SP 8647 A & B 250 MHz TTL OUTPUTS

UHF PROGRAMMABLE DIVIDERS ÷10/11

In frequency synthesis it is desirable to start rogrammable division at as high a frequency as possible, ecause this raises the comparison frequency and so nproves the overall synthesiser performance.

The SP8640 series are UHF integrated circuits that an be logically programmed to divide by either 10 or 11, ith input frequencies up to 350 MHz. The design of very ast fully programmable dividers is therefore greatly mplified by the use of these devices and makes them articularly useful in frequency synthesisers operating in he UHF band.

Inputs and outputs are ECL compatible throughout the temperature range: the clock inputs and programming inputs are ECL III compatible while the two complementary outputs are ECL II compatible to reduce power consumption in the output stage. ECL 10K output compatability can be achieved very simply however (see Operating Notes). The SP8643/7 feature an additional TTL compatible output.

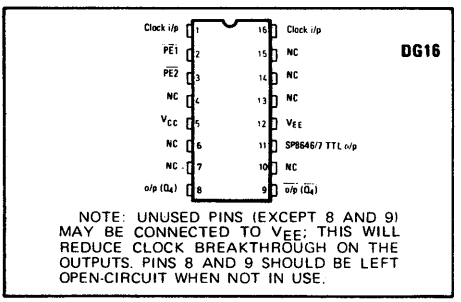
The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either $\overline{PE}$ input is in the high state and by 11 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).

EATURES

- Military and Industrial Variants.
- 350 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs
- Optional TTL Output

UICK REFERENCE DATA

- Full Temperature Range Operation:
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
- Supply Voltage
  $|V_{CC} - V_{EE}|$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.



NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE.

Fig. 1 Pin connections (top)

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\|V_{CC} - V_{EE}\|$	8V
Input voltage $V_{in\ (d.c.)}$	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

Clock Pulse	Q_1	Q_2	Q_3	Q_4	TTL O/P
1	L	H	H	H	H
2	L	L	H	H	H
3	L	L	L	H	H
4	H	L	L	H	H
5	H	H	L	H	H
6	L	H	H	L	L
7	L	L	H	L	L
8	L	L	L	L	L
9	H	L	L	L	L
10	H	H	L	L	L
11	H	H	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

The maximum possible loop delay for control obtained if the L→H transition from Q_4 or the H→ transition from $\overline{Q_4}$ is used to clock the stage controlling th ÷10/11. The loop delay is 10 clock periods minus th internal delays of the ÷10/11 circuit.

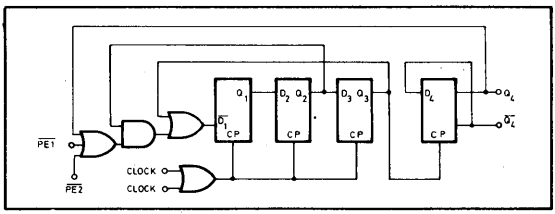


Fig. 2 Logic diagram (positive logic)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: −55 C to −125 C (A grade)
0 C to −70 C (B grade)
Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics (all SP8640 series devices)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3.
					I_{out} (external) = 0mA
					(There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES
1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

ynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	SP8643	350			MHz	
	SP8647	250			MHz	
Min. frequency with sinewave clock input	All			50	MHz	
Min. slew rate of square wave input for correct operation down to DC	All			100	V/μs	
Output (ECL)	All	500			mVpp	
Propagation delay (clock input to device output)	All		3		ns	ECL Output
Set-up time	All		1.5		ns	See note 5
Release time	All		1.5		ns	See note 6

OTES

. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.

. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse (see Fig. 3).

. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse (see Fig. 4).

. SP8647 TTL output current = 8mA at V_{OL} = +0.5V, measured at +25°C, temperature coefficient = +0.5mV/°C

. SP8647 Q_4 to TTL output delay = 3ns, typical

. The TTL O/P is a free collector and requires a 2k Ω (typ) pull-up resistor. The current taken by this resistor must be included in the 8mA current in Note 7 above.

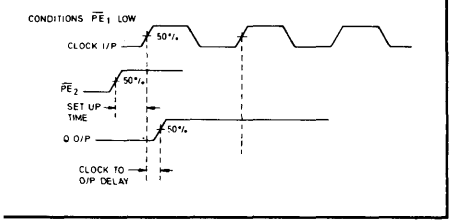


Fig. 3 Set-up timing diagram

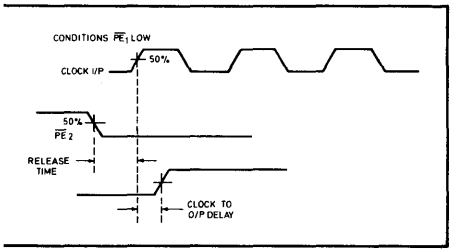


Fig. 4 Release timing diagram

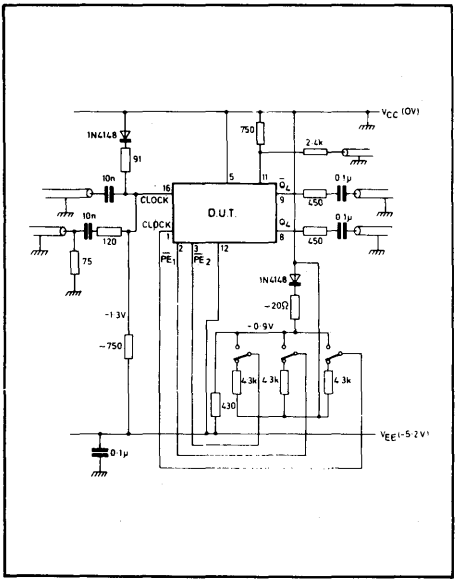


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8640 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

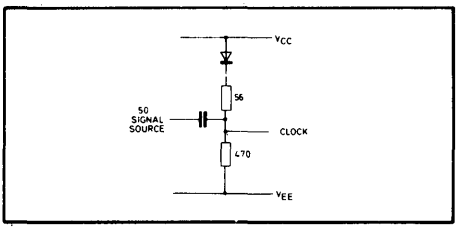


Fig. 6 Recommended input bias configuration for capacitive coupling to a contir uous 50Ω signal source.

The ÷10/11 can be controlled by a TTL fully programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface has been provided on chip in the SP8646/7. A discrete interface may be constructed as shown in Fig. 7. Both output interfaces will operate satisfactorily over the full military temperature range (−55°C to +125°C). The propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10 ns. At an input frequency of 350 MHz this would only leave about 16 ns for the fully-programmable counter to control the ÷10/11. The loop delay can be increased by extending the ÷10/11 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

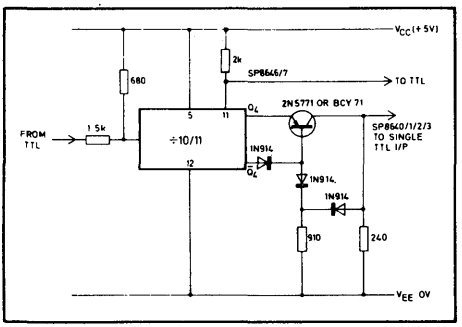


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8640 devices and TTL operating from the same supply rails)

The SP8643 device ECL o/ps are compatible wit ECL II levels when there is no external loa.. They can b made compatible with ECL III and ECL 10K with a simpl potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatibl with ECL III and ECL 10K. The interface circuit of Fig. can be used to increase noise immunity when interfacin from ECL III and ECL 10K outputs at low current levels t ECL III and ECL 10K inputs.

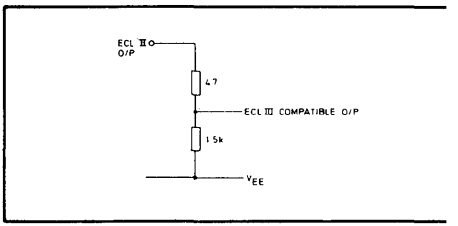


Fig. 8 ECL II to ECL III interface

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP8650A&B
600MHz÷16

The SP8650 series of UHF16 counters are fixed ratio synchronous emitter coupled logic counters with, in the case of the SP8650, a maximum operating frequency in excess of 600MHz. All three devices operate up to their maximum specified operating frequencies over temperature ranges of −55°C to +125°C ('A' grade), 0°C to +20°C ('B' grade). The input is normally capacitively coupled to the signal source but the circuits can be DC driven if required. The inputs can be either single driven relative to the on-chip reference voltage or differentially driven.

There are two complementary emitter follower outputs.

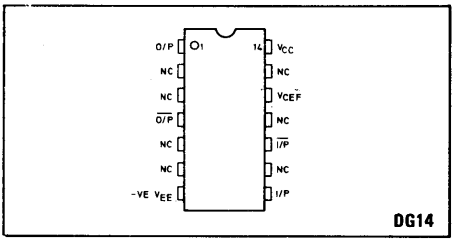

Fig. 1 Pin connections

FEATURES

- Low Power - Typically 250mW
- ECL II & ECL III Output Compatability
- Easy Operation From UHF Signal Source

APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

QUICK REFERENCE DATA

- Power Supplies $V_{CC} = 0V$
  $V_{EE} = -5.2V \pm 0.25V$
- Temperature Range 'A' grade −55°C to +125°C
  'B' grade 0°C to +70°C
- Input Amplitude Range 400mV to 800mVp-p
- Output Voltage Swing 800mV typ. p-p

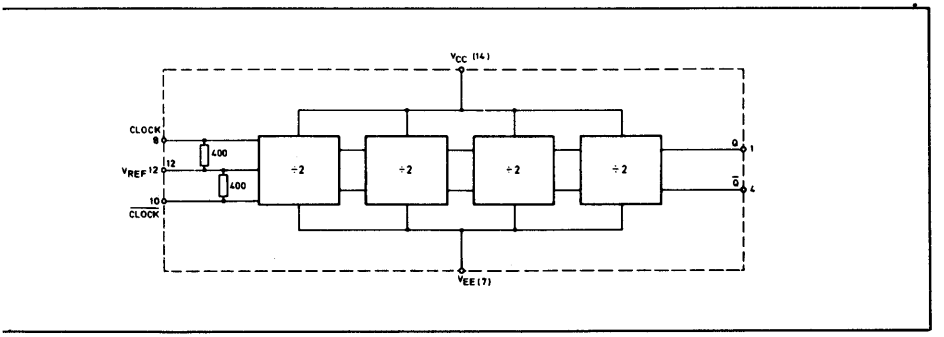

Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
T_{amb} = −55°C to +125°C ('A' grade)
0°C to +70°C ('B' grade)
Supply Voltage
V_{CC} = 0V
V_{EE} = −5.2V ± 0.25V
Output load = 500Ω in parallel with approx. 3pF

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Toggle frequency	SP8650	600			HMz	Test circuit as in fig. 2 V_{IN} = 400 to 800mV p-p
Min. toggle frequency for correct operation with a sinewave input				40	MHz	VIN = 400 to 800mV p-p
Min. slew rate for square wave input to guarantee correct operation to OHz				100	V/μs	
Input reference voltage			2.6		V	
Output voltage swing (dynamic)		500	800		mV	p-p
Output voltage (static)						
high state		−8.95		.615	V	
Low state		−1.83		−1.435	V	
Power supply drain current			45	60	mA	

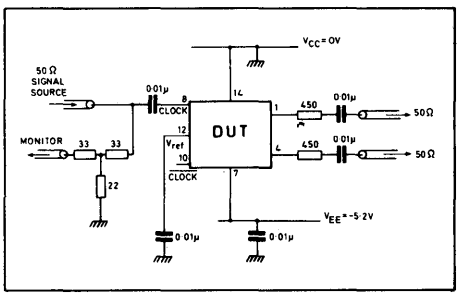

Fig. 3 Toggle frequency test circuit

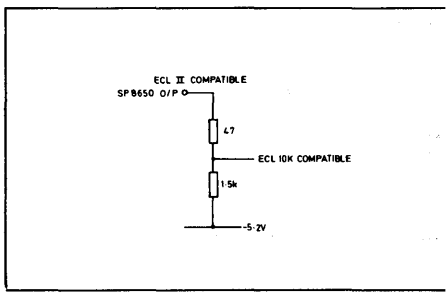

Fig. 4 SP8650 to ECL 10K interface

Toggle Frequency Test Circuit

1. All leads are kept short to minimise stray capacitance and induction.
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

ABSOLUTE MAXIMUM RATINGS

Power supply voltage /V_{CC} − V_{EE}/		8 volts
Input voltage	V_{INac}	2.5V p-p
Output source curr	I_{out}	10mA
Storage temperature range		−55°C to +125°C
Operating junction temperature		150°C max.

PERATING NOTE

Normal UHF layout techniques should be ed if the SP8650 divider is to operate satis- ctorily. If the positive supply is used as the rth connection, noise immunity is improved d the risk of damage due to inadvertently orting the output emitter followers to the gative rail is reduced.

The circuit is normally capacitively coupled to the ınal source. In the absence of an input signal the cuit will self-oscillate. This can be prevented by nnecting a 10KΩ resistor between one of the inputs d the negative rail.

The device will also miscount if the input transitions e slow — a slew rate of 100V/μs or greater is necessary r low frequency operation.

The outputs interface directly to ECL II or to ECL 10K th a potential divider (see Fig. 4).

A typical application of the SP8650 device ould be in the divider chain of a synthesiser perating in the military frequency range 225 lHz to 512 MHz. A binary division rate is ptimum where power is at a premium and so ıe SP8650 would normally be used in low ower applications.

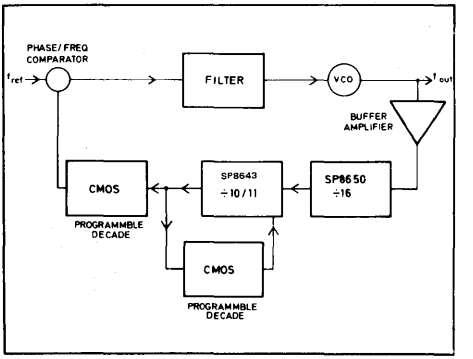

Fig. 5 A low power synthesiser loop

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8655A & B (÷32)
SP8657A & B (÷20)
SP8659A & B (÷16)

The SP8655A, B & M, SP8657A, B & M and SP8659A, B & M are fixed ratio (divide by 32, 20 and 16) low power counters for operation at frequencies in excess of 200MHz over the temperature ranges −55°C to +125°C ('A' grade), 0°C to+ 70°C ('B' grade).

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

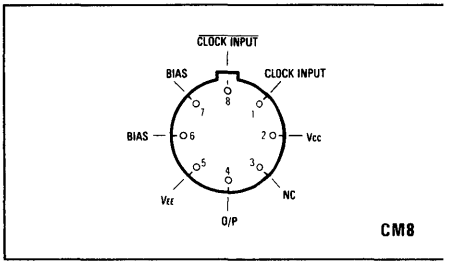

Fig. 1 Pin connections (viewed from beneath)

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, V_{CC}—V_{EE}	8V
Input voltage V_{in}	Not greater than supply voltage in use
Output sink current, I_O	10mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

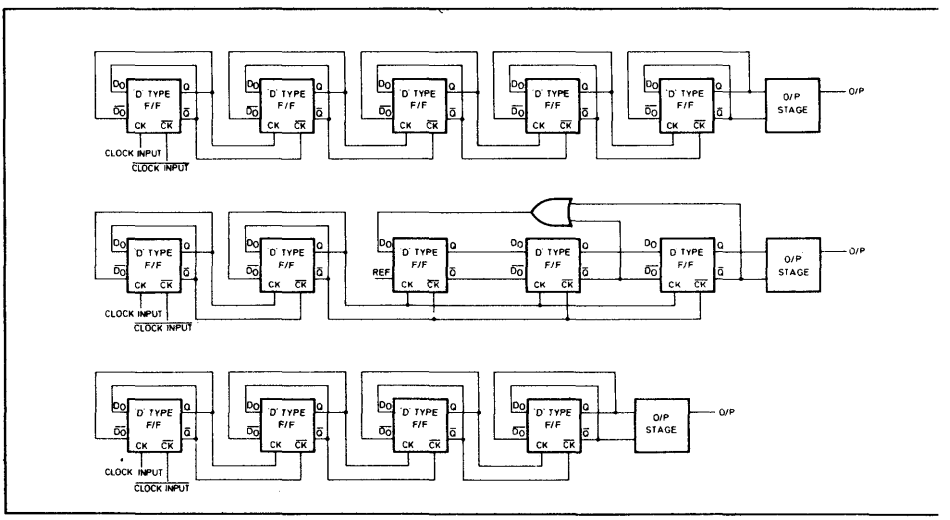

Fig. 2 Logic diagram

LECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating ambient temperature T_{amb}: —55°C to +125°C ('A' grade)
0°C to +70°C ('B' grade)
Operating supply voltages V_{CC}: +5.2V±0.25V; V_{EE}: OV
Input voltage single drive: 400mV to 800mV p-p
double drive: 250mV to 800mV p-p
Output load 3.3k Ω to −10V, in parallel with 7pF.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency	200			MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μs	
Power supply drain current		10	13	mA	V_{CC}=+5.2V
Output level (high)	9.0			V	
Output level (low)			400	mV	

PERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling f the input and bias points on the test circuit; these alues are not critical and will depend on the operating equency.

The devices will normally self-oscillate in the sence of an input signal. This can be easily tpre- ented by connecting a 39k Ω pulldown resistor from ther input (double drive) to V_{EE}; if the device is ngle driven then it is recommended that the pulldown sistor be connected to the decoupled unused input. ne slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3k Ω (or less) to a +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

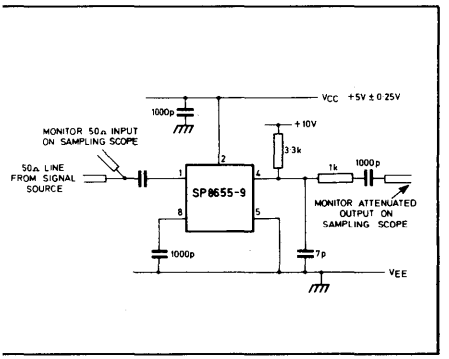

Fig. 3 Test circuit

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8656 ÷ (24)
SP8658 ÷ (20)

The SP8656 and SP8658 are fixed ratio (divide by 24 and 20) low power counters for operation at frequencies in excess of 200MHz over the temperature ranges -30°C to -70°C.

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

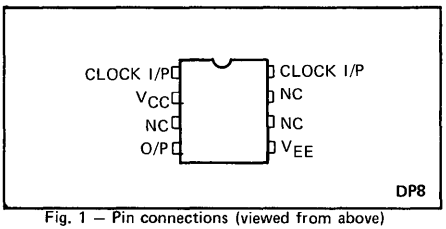

Fig. 1 – Pin connections (viewed from above)

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

ABSOLUTE MAXIMUM RATINGS

Power supply voltage: $[V_{CC} - V_{EE}]$	8V
Input voltage V_{IN}	Not greater than sup voltage in use.
Output sink current I_O	10mA
Operating junction temperature	+150°C
Storage temperature	-55°C to +125°C

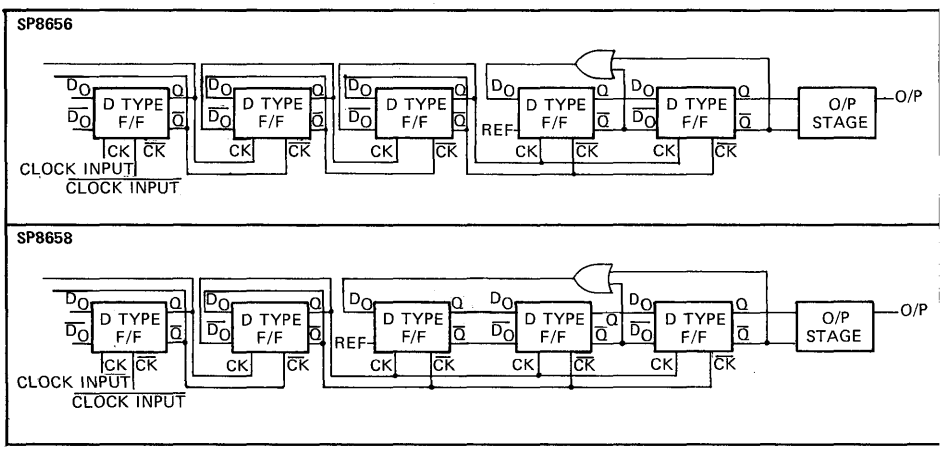

Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating ambient temperature T_{amb} -30°C to + 70°C

Operating supply voltage V_{cc} : 4.75v to 5.25v

Input voltage single drive: 400mV to 800mV pk-pk

double drive: 250mV to 800mV pk-pk

Output load 3.3kΩ to -10V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency	200			MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μsec	
Power supply drain current		20	30	mA	Vcc = +5.5V
Output level (high)	9.0			V	
Output level (low)			400	mV	

OPERATING NOTES

Fig. 3 gives capacitive values for AC and DC coupling of the input capacitor and bias points on the test circuit – these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39kΩ resistor from either input (double drive) to V_{EE}; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz. correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3kΩ to a +10V will allow the output to drive a CMOS counter at a frequency of up to 5MHz.

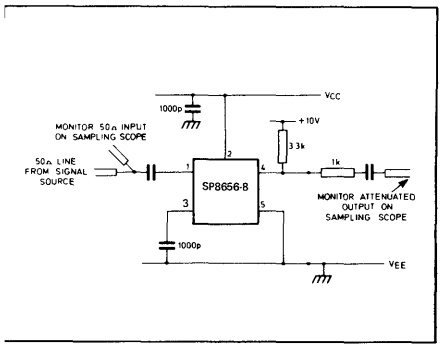

Fig. 3 Test circuit

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SP8000 SERIES

HIGH SPEED DIVIDERS

SP8660 A&B

200 MHz ÷ 10 (LOW POWER)

The SP8660 is a fixed ratio (divide by 10) low power counter for operation at frequencies in excess of 100MHz over the temperature ranges −55°C to +125°C ('A' grade) 0°C to +70°C ('B' grade).

The input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used, the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should also be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

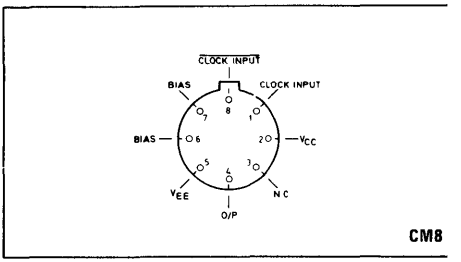

Fig. 1 Pin connections (viewed from beneath)

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible
- Military and Commercial Temperature Ranges

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $\|V_{CC} - V_{EE}\|$	8V
Input voltage V_{in}	Not greater than supply voltage in use
Output sink current, I_o	10mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling c the input and bias points on the test circuit; these values ar not critical and will depend on the operating frequency.

The device will normally self-oscillate in the absence c an input signal. This can be easily prevented by connectin a 39kΩ pulldown resistor from either input (double drive to V_{EE}; if the device is single driven then it recommended that the pulldown resistor be connected t the decoupled unused input. The slight loss of inpu sensitivity resulting from this technique does not seriousl affect the operation of the device.

The input waveform will normally be sinusoidal bu below 40MHz correct operation depends on the slew rate c the input signal. A slew rate of 100V/μs will enable th device to operate down to DC.

The output stage will drive three TTL gates without th addition of a pull-up resistor. Using a pull-up resistor c 3.3kΩ (or less) to +10V will allow the output to drive CMOS binary counter at a frequency of up to 5MHz.

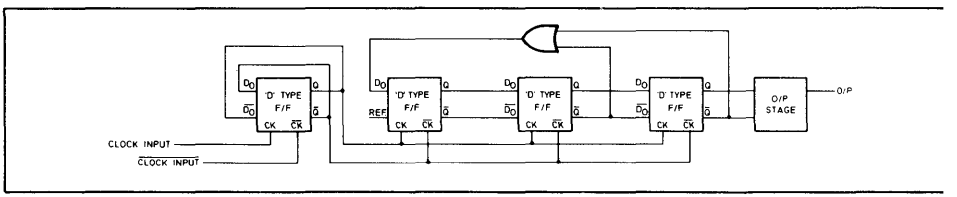

Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Operating ambient temperature T_A

'A' grade: −55°C to +125°C; 'B' grade: 0°C to 70°C;

Operating supply voltages

V_{CC} : +5.0V± 0.25V; V_{EE} : 0V

Input voltage

Single drive: 400mV to 800mV p-p; double drive: 250mV to 800mV p-p

Output load 3.3kΩ to +10V, in parallel with 7pF

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Maximum input frequency	200	250		MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μs	
Power supply drain current		10	13	mA	V_{CC} = +5.0V
Output level (high)	9.0			V	
Output level (low)			400	mV	

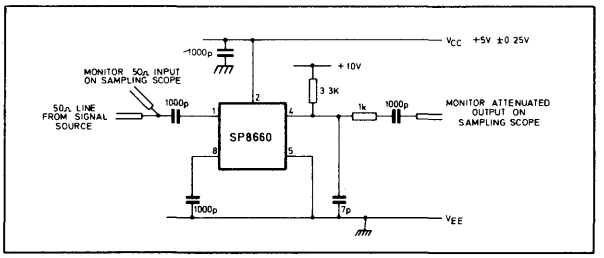

Fig. 3 Test circuit

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SP8000 SERIES
HIGH SPEED DIVIDERS

UHF DECADE COUNTERS

SP8665B 1.0GHz ÷ 10

SP8667B 1.2GHz ÷ 10

The SP8665/7 high speed decade counters operating at an input frequency of up to 1GHz over the temperature range 0°C to +70°C.

The device has a typical power dissipation of 550mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input to V_{EE} (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common V_{CC} to the SP8665/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8665/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

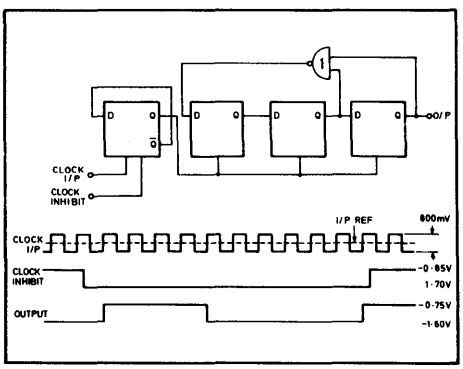

Fig. 2 Logic diagram

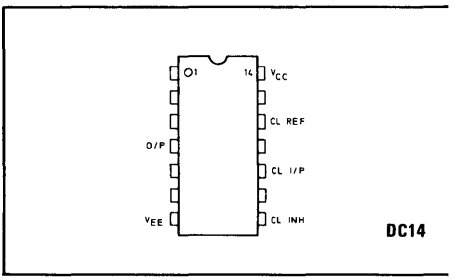

Fig. 1 Pin connections

FEATURES

- Guaranteed operation over large temperature range 0°C to 70°C
- Wide input dynamic range
- Self biasing clock input
- Clock inhibit input for direct gating capability

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage inhibit input	V_{EE} to V_{CC}
Input voltage CP input	2.5V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to 150°C

LECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

Supply voltage	6.8V ± 0.3V
Clock input	AC coupled, self-biasing
Clock inhibit input	ECL III compatible
Output	ECL II compatible
T_{amb}	0°C to +70°C
Supply voltage	V_{CC} = 0V V_{EE} = −6.8V
Clock input voltage	400mV to 1.2V (peak to peak)

Characteristics		Value			Units	Conditions
		Min.	Typ.	Max.		
Max. i/p frequency	SP8665	1.0			GHz	400mV to 1.2V p-p
	SP8667	1.2			GHz	600mV to 1.2V p-p
Min. i/p frequency				200	MHz	Sine wave input 400mV p-p
Min. i/p frequency				100	MHz	Sine wave input 600mV p-p
Min. slew rate for square wave input				200	V/μsec	
Clock i/p impedance			400		Ω	At low frequency
Inhibit input reference level			−1.3		V	At 25°C compatible with ECL III throughout the temperature range.
Inhibit input pulldown resistor (internal)			6		kΩ	
Output pulldown resistor (internal)			3		kΩ	
Power supply drain current			80	105	mA	At 25°C

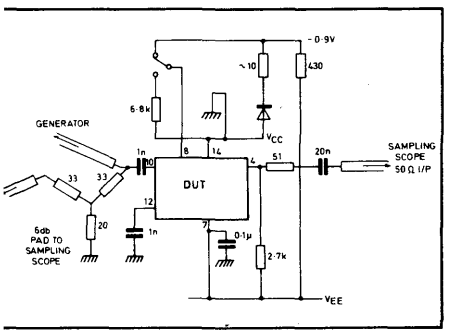

Fig. 3 Test circuit

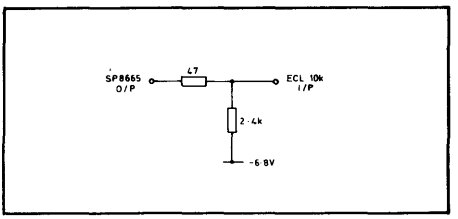

Fig. 4 SP8665 to ECL 10K

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Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8670 A&B
600MHz ÷8

The SP8670, SP8671 and SP8672 are fixed ratio –8 asynchronous ECL counters with a maximum operating frequency of 600, 500 and 400 MHz respectively. The operating temperature is specified by the final coding letter: –55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade). The input is normally capacitively coupled to the signal source but the circuit can be DC driven if required. The inputs can be either single driven, relative to the on-chip reference voltage, or driven differentially. There are two complementary emitter-follower outputs.

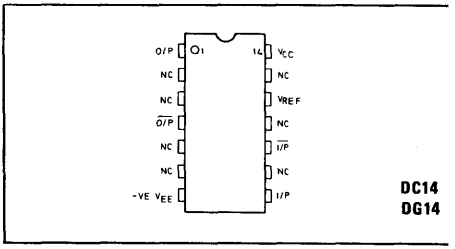

Fig. 1 Pin connections

FEATURES

- Low Power – Typically 250mW
- ECL II & ECL III Output Compatibility
- Easy Operation From UHF Signal Source

APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

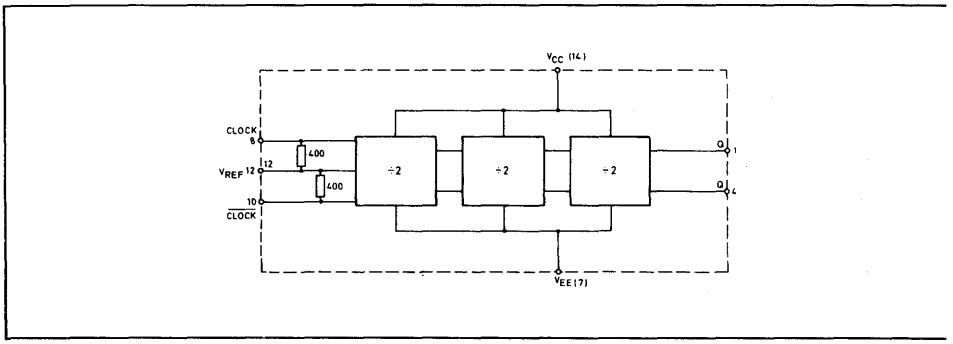

Fig. 2 Functional diagram

QUICK REFERENCE DATA

Power Supplies	V_{CC} = 0V V_{EE} = –5.2V ± 0.25V
Input Amplitude range	400mV to 800mV p-p
Output Voltage Swing	800mV typ. p-p
Temp. Ranges:	–55°C to +125°C ('A' Grade) 0°C to +70°C ('B' Grade)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

T_{amb} = 'A' grade: −55°C to +125°C;
Supply Voltage 'B' grade: 0°C to 70°C;
V_{CC} = 0V
V_{EE} = −5.2V ± 0.25V
Output load = 500Ω line in parallel with approx. 3pF

Characteristic		Value			Units	Condition
		Min.	Typ.	Max.		
Max. Toggle frequency	SP8670	600			MHz	
Min. Toggle frequency for correct operation with a sinewave input				40	MHz	V_{IN} = 400 to 800mV p-p
Min. slew rate for square wave input to guarantee correct operation to 0Hz				100	V/μs	
Input reference voltage			2.6		V	
Output voltage swing (dynamic)		500	800		mV	p-p
Output voltage (static)						
High state		−8.95		.615	V	
Low state		−1.83		−1.435	V	
Power supply drain current			45	60	mA	

Toggle Frequency Test Circuit

. All leads are kept short to minimise stray capacitance and inductance
'. Resistors and capacitors are non-inductive UHF types.
i. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

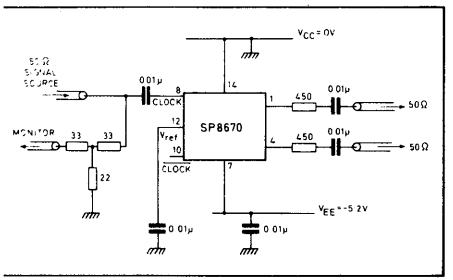

Fig. 3 Toggle frequency test circuit

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a 10KΩ resistor between one of the inputs and the negative rail.

V_{ref} must be decoupled to RF earth by a capacitor in the range 30pF to 1000pF. It is important that this decoupling is adequate, otherwise input sensitivity will be reduced.

The device will also miscount if the input transitions are slow — a slew rate of 100V/μs or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SP8670 would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division ratio is optimum where power is at a premium and so the SP8670 would normally be used in low power applications.

OPERATING NOTE

Normal UHF layout techniques should be used to ensure satisfactory operation. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

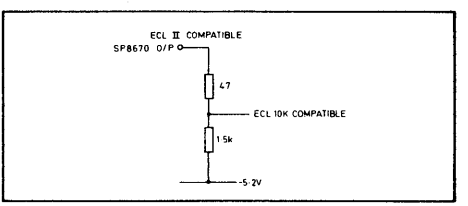

Fig. 4 SP8670 to ECL 10K interface

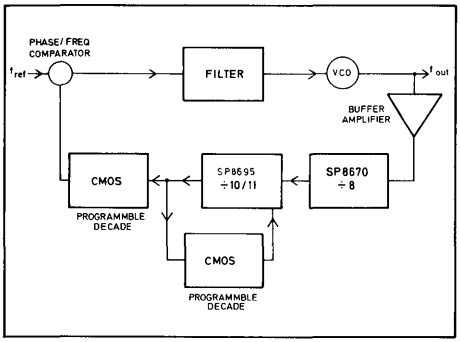

Fig. 5 A low power synthesiser loop

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8 volts
Input voltage V_{INac}	2.5V p-p
Output source current I_{out}	10mA
Storage temperature range	-55°C to $+125^{\circ}$C
Operating junction temperature	150°C max.

Plessey
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SP 8000 SERIES

HIGH SPEED DIVIDERS

SP8675B&M 1.0GHz ÷8
SP8677B&M 1.2GHz ÷8

The SP8675/7 are high speed counters for operation at input frequencies up to 1.2GHz.

The devices have a typical power dissipation of 270mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input V_{EE} (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common V_{CC} to the SP8675/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8675/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

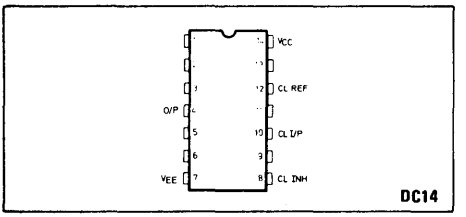


Fig. 1 Pin connections

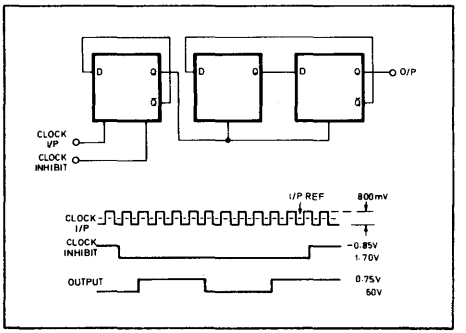


Fig. 2 Logic diagram and timing

FEATURES

- Guaranteed Operation over Large Temperature Range: 'B' Grade 0°C to +70°C
  'M' Grade —40°C to +85°C
- Wide Input Dynamic Range
- Self Biasing Clock Input
- Clock Inhibit Input for Direct Gating
- Capability

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC}—V_{EE} 0 to 10V
Input voltage inhibit input V_{EE} to V_{CC}
Input voltage CP input 2.5V p-p
Output current 20mA
Operating junction temperature +150°C
Storage temperature —55°C to +150°C

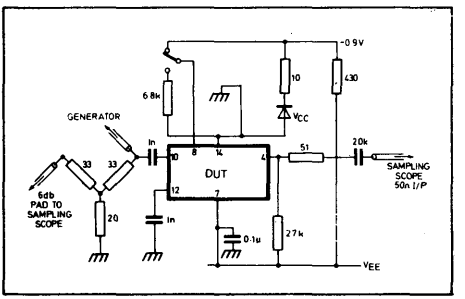


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

Supply voltage	6.8V ±0.3V
Clock input	AC coupled, self-biasing
Clock inhibit input	ECL III compatible
Output	ECL II compatible
T_{amb} 'B' grade	0°C to +70°C (see note 1)
'M' grade	−40°C to +85°C (see note 1)
Supply voltage	V_{CC} = OV V_{EE} = −6.8V
Clock input voltage	400mV to 1.2V (peak to peak)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency SP8675	1.0			GHz	400mV to 1.2V p-p
SP8677	1.2			GHz	600mV to 1.0V p-p
Min i/p frequency			200	MHz	Sine wave input 400mV p-p
			150	MHz	Sine wave input 600mV p-p
Min slew rate for square wave input			200	V/µsec	
Clock i/p impedance		400		Ω	At low frequency
Inhibit input reference level		−1.3		V	At 25°C compatible with ECL III throughout the temperature range
Inhibit input pulldown resistor (internal)		6		kΩ	
Output pulldown resistor (internal)		3		kΩ	
Power supply drain current		70	95	mA	at 25°C

NOTES

1. The SP8677M is tested at T_{case} = −40°C to +85°C. The SP8677M requires a suitable heatsink to be connected during operation.

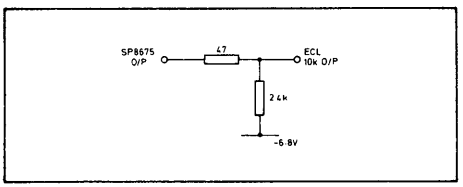


Fig. 4 SP8675 to ECL10K interface

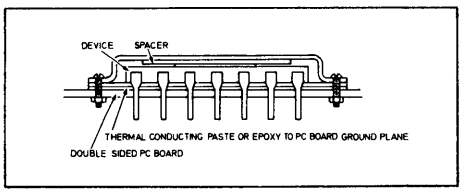


Fig. 5 Heat sink for 'M' grade devices

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

SP8000 SERIES

UHF PROGRAMMABLE DIVIDERS

SP8680 A& B

600 MHz ÷ 10/11

The SP8680 A & B are high speed programmable – 10/11 counters which operate at input frequencies up to 600 MHz over the temperature ranges -55°C to +125°C (A grade), -30°C to +70°C (B grade). The devices operate on a single +5V or T5.2V power supply and may be easily interfaced to E.C.L., or (by connecting the internal V_{REE}) capacitively coupled to the signal source. A clock enable, which is E.C.L. compatible, is provided. The division ratio is controlled by two mode inputs which are also ECL compatible. The counter will divide by 10 when either input is in the high state and by 11 when both inputs are low. The counter may be set to the eleventh state by applying a high level to the MS input. The set command is asynchronous and overrides the clock input. All inputs have internal -50KΩ pull down resistors, so that unused inputs may be left open circuit.

Two complementary ECL outputs are provided. They are both capable of driving 50Ω lines. A T.T.L. push pull output is also provided which may be powered up separately from the counter using the V_{EE} on pin 13.

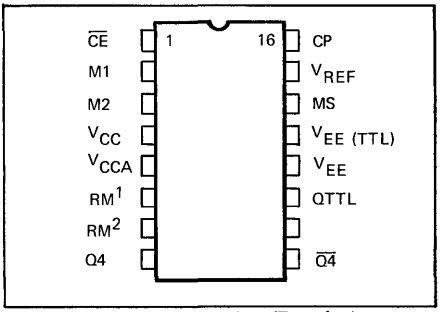


Fig. 1 – Pin Connections (Top View)

FEATURES

- D.C. to 600 MHz operation
- ECL and TTL compatible
- D.C. or A.C. clock input
- Clock enable
- Asynchronous master set

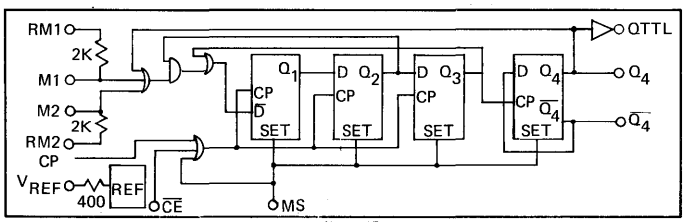


Fig. 2 – Logic Diagram

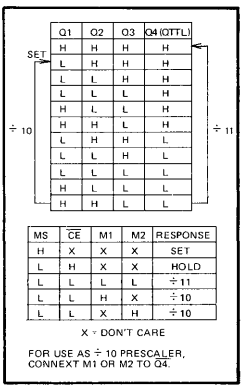


Fig. 3 – Count Sequence & Control Input Truth Table

QUICK REFERENCE DATA

- Supply voltage ($V_{CC} - V_{EE}$) = 5.0V +0.5V -0.25V
- Power consumption 400mW typ. (no load) T.T.L. output 20mW typ.
- Maximum input frequency 600 MHz SP8680B 550 MHz SP8680A
- Input amplitude (a.c. coupled) 350mV to 700mV.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

Power Supply Voltage	$[V_{CC} (V_{CCA}) - V_{EE}]$ -0.5 to +7V
Input Voltage	V_{EE} TO V_{CC}
ECL Output Source Current	50mA
TTL Output Sink Current	30mA
Voltage Applied to TTL Output High	V_{EE} to V_{CC}
Operating Ambient Temperature	-55°C to +125°C
Storage Temperature	-55°C to +150°C

STATIC CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min	Typ.	Max		
Guaranteed Input High Voltage V_{INH}	4.1		4.4	V	V_{CC} = +5.2V Tamb = 25°C
Guaranteed Input Low Voltage V_{INL}	3.35		3.7	V	(See Note 2)
Input High Current I_{INH}					V_{CC} = +5.2V T_{amb}
CP and MS inputs			400	μA	
M1 and M2 inputs			250	μA	V_{INH} = 4.4V
Input Low Current I_{INL}	0.5			μA	V_{INL} = 3.35V
E.C.L. Output Low Voltage V_{OL}	3.38	3.49	3.58	V	V_{CC} = +5.2V Tamb = 25°C
E.C.L. Output High Voltage V_{OH}	4.22	4.30	4.38	V	Load 100Ω to +3.2V (See Note 2)
T.T.L. Output High Voltage V_{OH}	2.7	3.3		V	$V_{CC} = V_{CCA}$ = 4.75V I_{OH} = -1mA Tamb = 25°C
T.T.L. Output Low Voltage V_{OL}		0.3	0.5	V	$V_{CC} = V_{CCA}$ = 4.75V I_{OL} = 20mA Tamb = 25°C
T.T.L. Output Short Circuit Current	-80	-40	-20	mA	$V_{CC} = V_{CCA}$ = 5.5V V_{OUT} = 0V Pin 14 = V_{INH}
M1, M2 Input Low Current (using int. 2KΩ pull up)	-4.0	-2.5		V	$V_{CC} = V_{CCA}$ = 5.5V V_{IN} = 0.4V Pins 6, 7 = V_{CC}
Power Supply Current		75	105	mA	No Load Pins 6, 7, 13 open circuit
T.T.L. Output Stage Supply Current		4		mA	Mean, Output High and Low

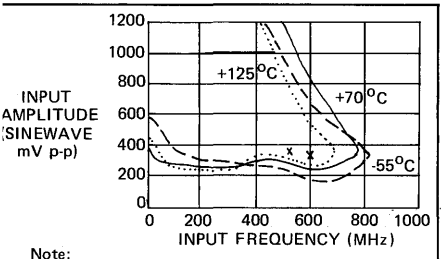
DYNAMIC CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min	Typ.	Max		
Max. Count Frequency					V_{CC} = +5.2V a.c. coupled input 350mV peak to peak
SP8680B	600			MHz	-30°C to +70°C
SP8680A	550			MHz	-55°C to +125°C
Min. Frequency with sinewave clock input			10	MHz	V_{CC} = +5.2V a.c. coupled input 600mV peak to peak Tamb = 25°C
Min. slew rate of square wave clock input			20	V/ usec	V_{CC} = +5.2V
Propagation Delay CP to Q4		2.2	3.0	nsec	Tamb = 25°C
Propagation Delay MS to Q4		4.5	6.0	nsec	Ouptut Load
Min Set Up Time M to CP		2.0	4.0	nsec	100Ω to +3.2V
ECL Output Rise & Fall Times		1.3		nsec	
Propagation Delay CP to QTTL		8	14	nsec	V_{CC} = +5.0V Tamb = 25°C
TTL Output Rise Time		3		nsec	
TTL Output Fall Time		3		nsec	

Notes:

1. The SP8680 may be used in a positive earth system with V_{CC} = 0V and V_{EE} = -4.75V to -5.5V.
2. The input threshold has a temperature coefficient of 0.8mV/°C. This may be used to calculate V_{INH} and V_{INL} values at the temperature extremes.
3. The E.C.L. outputs are capable of driving a 50Ω load to +3.2V over a limited temperature range of 0°C to 70°C. The output high level will be reduced by typically 50mV.

The output high level has a temperature coefficient of 1.2mV/°C, whilst the output low level has a coefficient of 0.2mV/°C.



Note:
The above graphs are with the TTL output connected. Sensitivity in the 300 to 500 MHz frequency range is improved by 100mV peak to peak when pin 13 is disconnected.

Fig.4 Clock Input Frequency versus Amplitude (a.c. coupled)

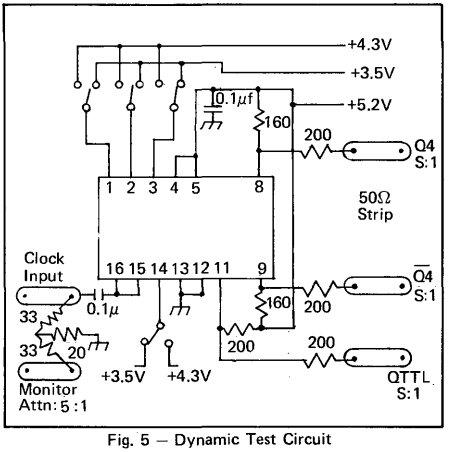
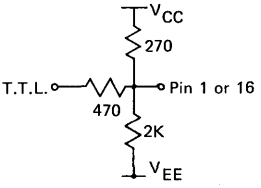


Fig. 5 — Dynamic Test Circuit

OPERATING NOTES

The SP8680 is designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g., short tracks, low inductance capacitors, etc.

All clock and control inputs are compatible with ECL 10K throughout the temperature range. The clock input may be capacitively coupled by connecting pin 16 to pin 15. All inputs may be interfaced with T.T.L. logic as shown in Figure 6.

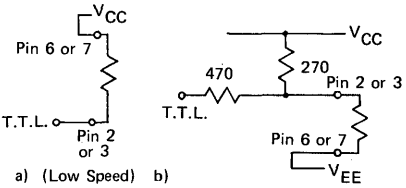


T.T.L. INTERFACE CP & $\overline{CE}$

Two E.C.L. compatible outputs are available (true and inverse) both capable of driving a 100Ω load (to +3.2V) over the full temperature range. These outputs have no internal pull down, so an external resistor to V_{EE} is required when interfacing to other E.C.L. logic. A T.T.L. output is also provided which is powered up by connecting pin 13 to V_{EE}.

The SP8680 may be controlled by a following variable divider to produce effective variable division at up to 600 MHz. Some points to be noted when this technique is employed are as follows:

1) The 0 – 1 edge of the Q_4 or TTL outputs must be used to clock the following divider. This gives a maximum control loop delay time (equal to ten clock periods minus internal delays).
2) At 600 MHz the required control loop delay time is only 13 nsec. (using ECL outputs) and, hence, only an E.C.L. variable divider can be used in the control loop. A suitable device is the 10136.
3) To overcome the above problem, the modulus may be extended from 10/11 to 20/21, 40/41 to 100/101. This will considerably increase the control loop delay time so that a TTL variable divider may be used in the control loop.



T.T.L. INTERFACE M1 & M2

4) The minimum division number of a 'two modulus' n/n + 1 when employed as a fully variable divider is n(n-1). Therefore, for a 10/11, this will give 90. If the modulus has been extended to 100/101, the minimum divide number will be 9,900 which may well be too large.
5) If the above two-modulus approach does not give a satisfactory systems' solution, then a four-modulus system may be required. An example of this would be a 100/101/110/111 followed by two control dividers. The two control dividers decide on the number of +1 and +10 counts required. The minimum division number of such a system is 900.

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8685 A&B
UHF PROGRAMMABLE DIVIDER 500MHz ÷ 10/11

The SP8685 A&B are high speed programmable–10/11 counters operating at an input frequency of up to 500 MHz over the temperature ranges -55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade).

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either input is in the high state, and by 11 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-ten prescaler the inverse output (o/p) should be connected to a PE input.

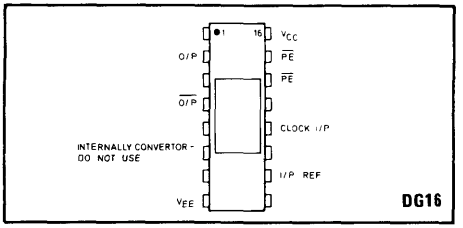


Fig. 1 Pin connections

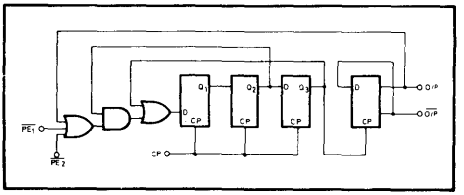


Fig. 2 Logic diagram SP8685

Clock Pulse	Q_1	Q_2	Q_3	Q_4
1	L	H	H	H
2	L	L	H	H
3	L	L	L	H
4	H	L	L	H
5	H	H	L	H
6	L	H	H	L
7	L	L	H	L
8	L	L	L	L
9	H	L	L	L
10	H	H	L	L
11	L	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	PE_2	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

FEATURES

- Full temperature range operation:
  'A' grade -55°C to +125°C
  'B' grade 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	–55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible

Outputs – ECL II compatible

Test conditions (unless otherwise stated)

Tamb 'A' grade -55°C to +125°C
'B' grade 0°C to +70°C

Supply voltages: V_{CC} = +5.2V ±0.25V

V_{EE} = 0V

Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	500			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slow rate for square wave input			100	V/μs	
Propogation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown Resistors,		4.3		KΩ	
Clock i/p impedance (i/p to i/p ref low frequency)		400		Ω	

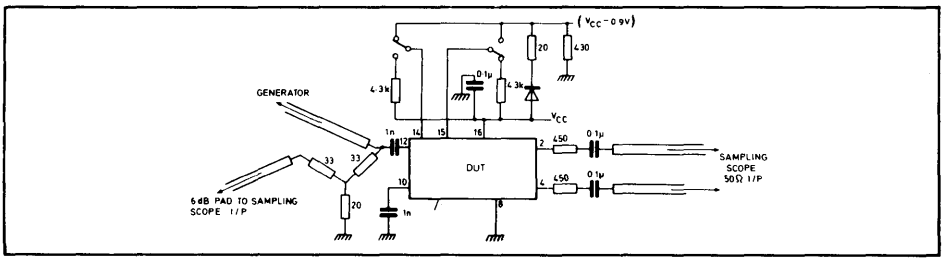


Fig. 3 Test circuit

APPLICATION NOTES

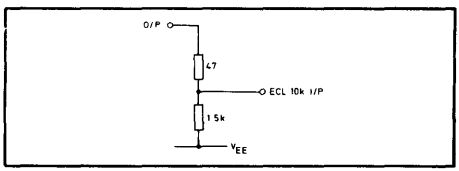


Fig. 4 SP8685 output – ECL 10K i/p and ECLII (or ECL 10K o/ps unloaded) – ECL 10K i/p

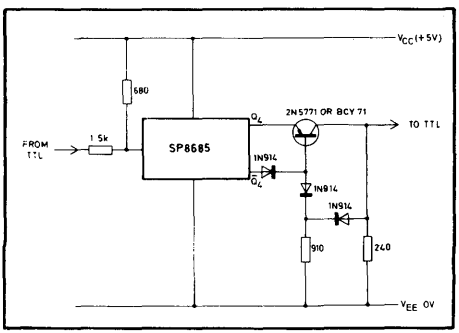


Fig. 5 TTL o/p – SP8685 $\overline{PE}$ i/p; SL8685 o/p – TTL i/p. (Total delay from SP8685 clock i/p to Schottky gate o/p = 15ns, typ.)

At an input frequency of 500 MHz the control loop delay time (SP8685 o/p to PE i/p) is approximately 16 ns. This will be a severe problem if TTL is used in the control loop.

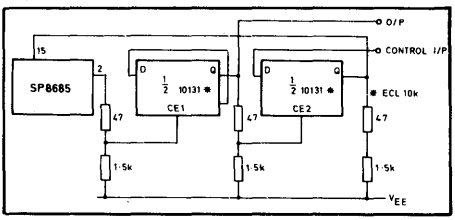


Fig. 6 Divide-by-20/22. Control loop delay time approximately 40ns.

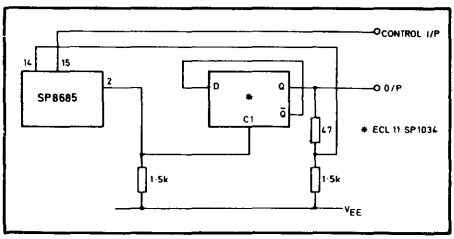


Fig. 7 Divide-by-20/21. Control loop delay time approximately 30ns using SP1034.

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1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES

HIGH SPEED DIVIDERS

SP8690 A & B 200 MHz ÷ 10/11

AC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8690 A&B are divider circuits that can be logically programmed to divide by either 10 or 11.

The device is available over three temperature ranges: 'A' grade is —55 °C to +125 °C and the 'B' grade is 0 °C to +70 °C.

The clock inputs can be either single or differentially driven and must be AC-coupled to the signal source. If single driven then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present; to prevent this, a 68kΩ resistor should be connected from pin 1 or 16 to 0V. This will reduce the sensitivity of the device by approximately 100mV p-p.

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.

The device may be used as a fixed ÷10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{Q4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

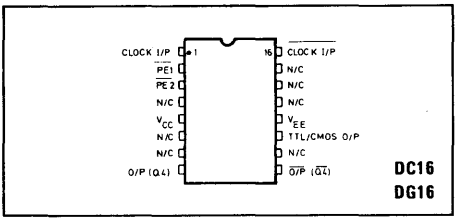
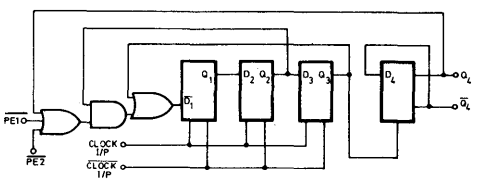


Fig.1 Pin connections

FEATURES

- Full Temperature Range Operation
  'A' Grade —55 °C to +125 °C
  'B' Grade 0°C to +70°C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 70mW Typical
- ECL Compatibility on All Inputs
- Capacitively Coupled Clock Input for Synthesiser and Counter Applications
- True and Inverse Outputs Available with ECL Compatibility
- Output Available for Driving TTL or CMOS



Division ratio				
I/P	11	10	10	10
$\overline{PE1}$	L	H	L	H
$\overline{PE2}$	L	L	H	H

Count sequence				
Q_1	Q_2	Q_3	Q_4	
L	H	H	H	
L	L	H	H	
L	L	L	H	
H	L	L	H	
H	H	L	H	
L	H	H	L	
L	L	H	L	
L	L	L	L	
H	L	L	L	
H	H	L	L	
H	H	H	H	Extra state

Fig.2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltage V_{CC} = +5V ±0.25V
V_{EE} = 0V
Clock I/P voltage 400mV to 800mV peak to peak
Pin 16 (decoupled to 0V)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. toggle frequency	200			MHz	
Min. freq. with sine wave clock input		15		MHz	
Min. slew rate of square wave I/P for correct operation		40		V/µs	
$\overline{PE}$ input levels					
V_{INH}	+4.1		+4.5	V	V_{CC}=+5V
V_{INL}	0.0		+3.5	V	T_{amb}=+25°C (note 1)
					T_{amb}=+25°C (note 2)
Q4 & $\overline{Q4}$ output voltage levels					
V_{OH}	4.15			V	I_{out} (external) = 0mA
V_{OL}			+3.5	V	(There is internal circuitry equivalent to a 3.8kΩ pulldown resistor on each output)
TTL/CMOS output voltage levels					
V_{OL}			+0.4	V	Sink current 3.2mA on
V_{OH}	see note 3				TTL output
Input pulldown resistors between input pins 2 & 3 and −ve rail		10		kΩ	
Power supply drain current		14	19	mA	V_{CC}=+5V; T_{amb}=25°C
Impedance of clock I/P		1.6		kΩ	in=0Hz
Clock to TTL output delay (O/P −ve going)		22		ns	8mA sink current
Clock to TTL output delay (O/P −ve going)		8		ns	TTL output
Clock to ECL output delay		6		ns	
Set up time		2		ns	See note 4
Release time		4		ns	See note 5

NOTES
1. The $\overline{PE}$ reference voltage level is compatible with ECL II and ECL 10k over the specified temperature range.
2. The Q_4 and $\overline{Q_4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
3. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed +12V.
4. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
5. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

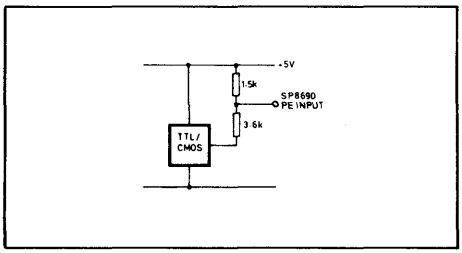


Fig.3 TTL/CMOS interface

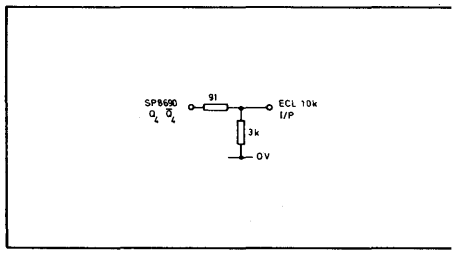


Fig.4 ECL 10K output interface

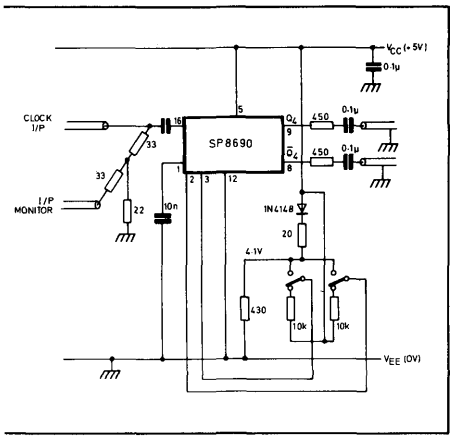


Fig.5 Test circuit for dynamic measurements

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC}-V_{EE}\rvert$	V8
Input voltage V_{IN} d.c.	Not greater than the supply voltage in use
Output current I_{out} (Q_4 & $\overline{Q_4}$)	10mA
Maximum junction temperature	150°C
Storage temperature range	−55°C to +150°C

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP8691 A & B
200 MHz ÷ 8/9

The SP8691 A & B are divider circuits that can be logically progressed to divide by either 8 or 9.

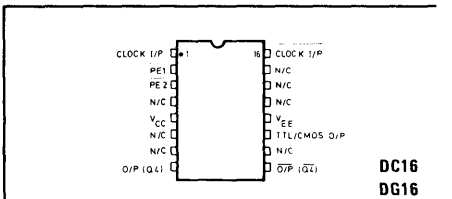
The device is available over two temperature ranges, 'A' variant is -55°C to +125°C and the 'B' variant is 0°C to +70°C.

The clock inputs can be either single or differentially driven and must be a.c. coupled to the signal source. If single driven then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present. To prevent this a 68k resistor should be connected from pin 1 or 16 to OV. This will reduce the sensitivity of the device by approximately 100mV p-p.

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III, 10k compatible throughout the temperature range. The device will divide by eight when either input is high and by nine when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10k as shown in Fig. 4.

The device may be used as a fixed ÷8 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 or the 1 → 0 transition of $\overline{Q4}$ is used to clock the next stage then this will give the maximum loop delay for control i.e., 8 clock periods minus the internal delays.



DC16
DG16

Fig. 1 Pin Connections

FEATURES

Full temperature range operation

'A' variant -55°C to +125°C
'B' variant 0°C to +70°C

Toggle frequency in excess of 200MHz
Power dissipation 70mW typical
ECL compatibility on all inputs
Capacitively coupled clock input for synthesiser and counter applications
True and inverse outputs available with ECL compatibility
Output available for driving TTL or CMOS

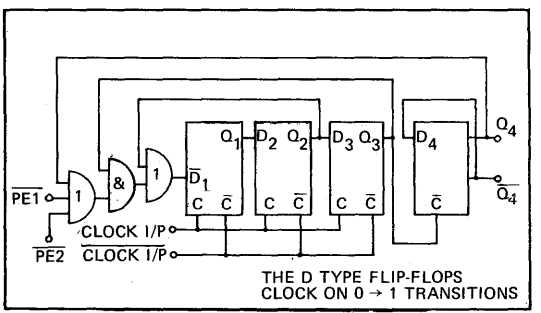


Fig. 2 LOGIC DIAGRAM (+VE LOGIC)

COUNT SEQUENCE				DIVISION RATIO
Q_1	Q_2	Q_3	Q_4	
				9 8 8 8
H	L	L	H	
H	H	L	H	$\overline{PE1}$ L H L H
L	H	H	H	
L	L	H	H	$\overline{PE2}$ L L H H
H	L	L	L	
H	H	L	L	
L	H	H	L	
L	L	H	L	
L	L	L	H	←Extra state

ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC} - V_{EE}$ 8V

Input voltage V_{IN} d.c. Not greater than the supply voltage in use

Output current $I_{out}(Q_4$ & $\overline{Q_4})$ 10mA

Maximum junction temperature 150°C

Storage temperature range -55°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

T_{amb} 'A' variant -55°C to +125°C
'B' variant 0°C to +70°C

Supply voltage V_{CC} = +5V ± 0.25V
V_{EE} = O_V

Clock I/P voltage 400mV to 800mV peak to peak ($\overline{\text{Clock I/P}}$ decoupled to O_V)

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Max. toggle frequency	200			MHz	
Min. freq. with sine wave clock input		15		MHz	
Min. slew rate of square wave i/p for correct operation		40		V/μs	
PE input levels					
V_{IMH}	+4.1		+4.5	volts	V_{CC} = +5V
V_{INL}	0.0		+3.5	volts	T_{amb} = +25°C (note 1)
Q4 & $\overline{Q4}$ output voltage levels					T_{amb} = +25°C (note 2)
V_{OH}	4.15			volts	I_{out} (external) = OmA
V_{OL}			+3.5	volts	(There is internal circuitry equivalent to a 3.8k ohms pulldown resistor on each output.)
TTL/CMOS output voltage levels					
V_{OL}	*see*		+0.4	volts	Sink current 3.2mA on
V_{OH}	note 3				TTL output.
Input pulldown resistors between input pins 2 & 3 and -ve rail		10		k ohms	
Power supply drain current		14		mA	V_{CC} = +5V T_{amb} = +25°C
Impedance of clock i/p		1.6		k ohms	F_{IN} = OHz

NOTE 1

The $\overline{PE}$ reference voltage level is compatible with ECL II and 10k over the specified temperature range.

NOTE 2

The Q_4 and $\overline{Q_4}$ output levels are compatible with ECL II and 10k over the specified temperature range.

NOTE 3

The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed +12V.

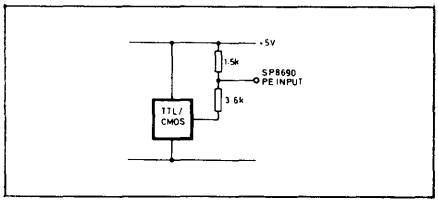


Fig.3 TTL/CMOS interface

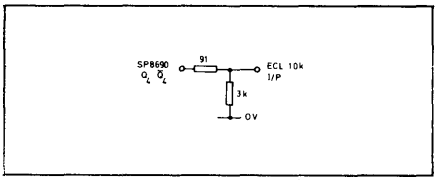


Fig.4 ECL 10K output interface

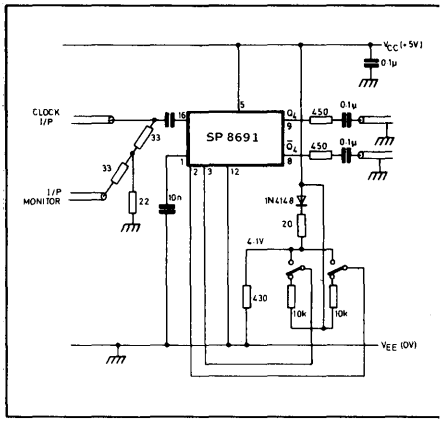


Fig.5 Test circuit for dynamic measurements

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SP8000 SERIES

HIGH SPEED DIVIDERS

SP8695 A & B 200 MHz ÷ 10/11

DC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8695 A&B are divider circuits that can be logically programmed to divide by either 10 or 11.
The device is available over two temperature ranges, 'A' grade is —55 C to +125 C, the 'B' grade is 0 C to +70 C.
The clock inputs are ECL II, III & 10K compatible throughout the temperature range (see note 1).
The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.
The device may be used as a fixed ÷ 10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.
If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

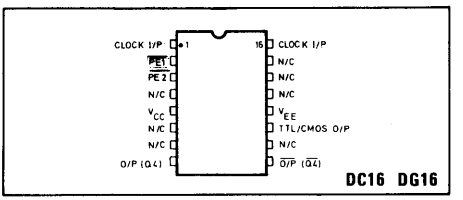
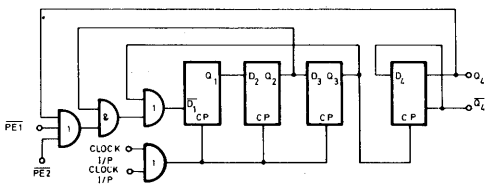


Fig.1 Pin connections

FEATURES

- Full Temperature Range Operation
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 80mW Typ.
- ECL Compatibility on All Inputs
- Excellent Low Frequency Operation
- True and Inverse Outputs Available with ECL Compatibility.
- Output Available for Driving TTL or CMOS



Division ratio				
I/P	11	10	10	10
$\overline{PE1}$	L	H	L	H
$\overline{PE2}$	L	L	H	H

Count sequence				
Q_1	Q_2	Q_3	Q_4	
L	H	H	H	
L	L	H	H	
L	L	L	H	
H	L	L	H	
H	H	L	H	
L	H	H	L	
L	L	H	L	
L	L	L	L	
H	L	L	L	
H	H	L	L	
H	H	H	H	Extra state

Fig.2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltage V_{CC} = +5V ±0.25V
V_{EE} = 0V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. toggle frequency	200			MHz	
Min. freq. with sine wave clock input		1		MHz	
Min. slew rate of square wave I/P for correct operation		3		V/µs	
Clock I/P voltage levels					
V_{INH}	+4.0		4.2*	V	V_{ref} = +3.8V
V_{INL}	−3.4*		+3.6	V	at T_{amb} = 25°C (note 1)
$\overline{PE}$ input levels					
V_{INH}	+4.1		+4.5	V	T_{amb} = +25°C (note 2)
V_{INL}	0.0		+3.5	V	
Q4 & $\overline{Q4}$ output voltage levels					T_{amb} = +25°C (note 3)
V_{OH}	+4.15			V	I_{out} (external) = 0mA
V_{OL}			+3.5	V	(There is internal circuitry equivalent to 1 3.8kΩ pulldown resistor on each output)
TTL/CMOS output voltage levels					
V_{OL}			+0.4	V	Sink current 3.2mA on TTL output
V_{OH}	see note 4				
Input pulldown resistors between input pins 1, 2, 3 & 16 and −ve rail		10		kΩ	
Power supply drain current		16	21	mA	V_{CC} = +5V; T_{amb} = +25°C.
Clock to TTL output delay (O/P −ve going)		22		ns	8mA sink current
Clock to TTL output delay (O/P −ve going)		8		ns	TTL output
Clock to ECL output delay		6		ns	
Set up time		2		ns	See note 5
Release time		4		ns	See note 6

NOTES
1. This reference level of −3.8V will enable the clock inputs to be driven from ECL II, III & 10K when their outputs are sinking 3mA. The input reference voltage is compatible with ECL II, III and 10k over the specified temperature range.
2. The $\overline{PE}$ reference voltage level is compatible with ECL II and 10k over the specified temperature range.
3. The Q_4 and $\overline{Q4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
4. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed −12V.
5. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
6. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

*High frequency limits only.

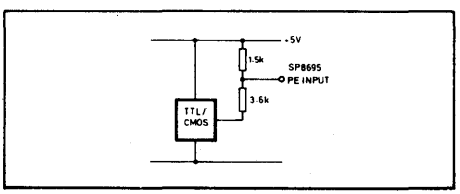


Fig.3 TTL/CMOS interface

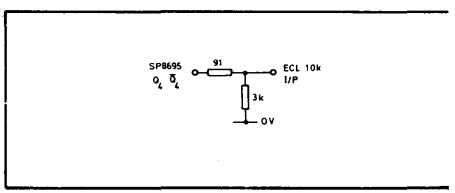


Fig.4 ECL 10K output interface

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}—V_{EE}	V8
Input voltage V_{IN} d.c.	Not greater than the supply voltage in use
Output current I_{out} (Q_4 & Q_4)	10mA
Maximum junction temperature	150 C
Storage temperature range	—55 C to + 150 C

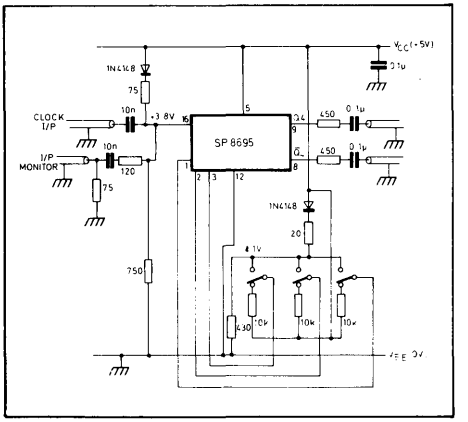


Fig.5 Test circuit for dynamic measurements

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8720 A & B
UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 3/4

The SP8720 A&B are high speed programmable ÷3/4 counters operating at an input frequency of up to 300MHz over the temperature ranges −55°C to +125°C, 0°C to +70°C.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 3 when either input is in the high state, and by 4 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-three prescaler the inverse output ($\overline{Q2}$) should be connected to a $\overline{PE}$ input.

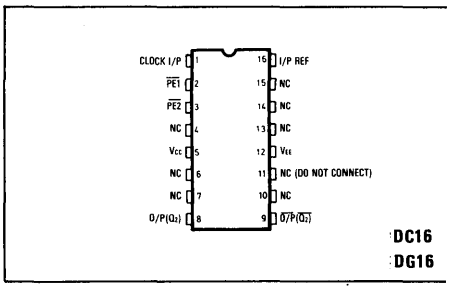

Fig. 1 Pin connections (top view)

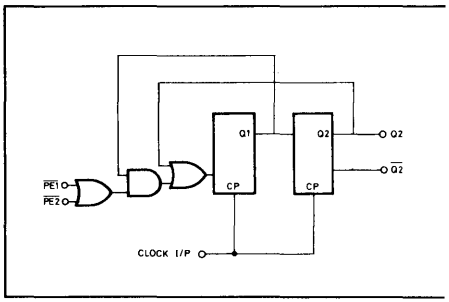

Fig. 2 Logic diagram SP8720

FEATURES

- Full temperature range operation :
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to + 70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K - Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | V_{CC} - V_{EE} |	0V to +8V
Input voltage, $\overline{PE}$ inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to + 150°C

Clock Pulse	Q_1	Q_2	
1	L	H	
2	L	L	
3	H	L	
4	H	H	← Extra State

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio.
L	L	4
H	L	3
L	H	3
H	H	3

Table 2 Truth table for control inputs

P8720

LECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs - ECL 10K compatible
Outputs - ECL II compatible

Test conditions (unless otherwise stated)
Tamb 'A' Grade: −55°C to +125°C
'B' Grade: 0°C to + 70°C
Supply voltages: V_{CC} = + 5.2V ±0.25V
V_{EE}=0V
Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency	300			MHz	Vcc= + 5.2V
Min.i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
PE input reference level		+ 3.9		V	V_{cc} = + 5.2V, 25°C
Power supply drain current		40	55	mA	V_{cc} = + 5.2V, 25°C
PE input pull down resistors		4.3		kΩ	
Clock i/p impedance (i/p to i/p ref. low frequency)		400		Ω	

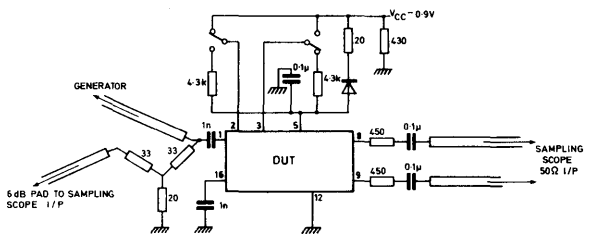

Fig. 3 Test circuit

APPLICATION NOTES

When operating the SP8720 in a synthesiser loop at 00MHz, the delay time through the programmable di-ider controlling the SP8720 is approximately 5.5ns, nd will require ECL.

The simple passive interface from the output of the P8720 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, nd the output of the SP8720 into TTL, is shown in ig.5.

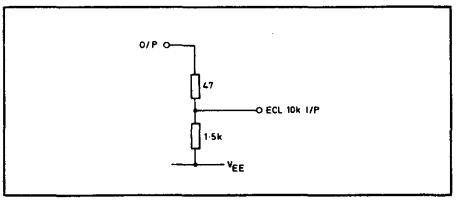

Fig. 4

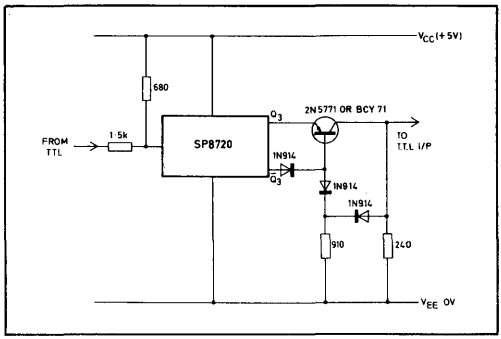

Fig. 5

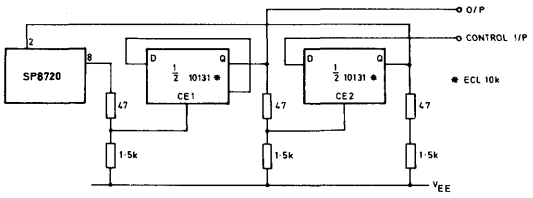

Fig. 6 Divide by 6/8 Control loop delay time approximately 20ns at 300MHz I/P frequency

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SP8000 SERIES

HIGH-SPEED DIVIDERS

SP 8725 A & B

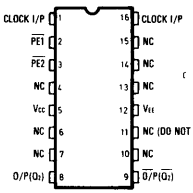
UHF PROGRAMMABLE DIVIDER 300MHz ÷ 3/4

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8725 series are UHF integrated circuits that can be logically programmed to divide by either 3 or 4 with input frequencies up to 300MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL10K-compatible while the two complementary outputs are ECLII-compatible to reduce power consumption in the output stage. ECL 10K output compatibility can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 3 when either $\overline{PE}$ input is in the high state and by 4 when both inputs are in the low state. Both the PE inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).



DC16 DG16

NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE. PIN 11 IS INTERNALLY CONNECTED AND MUST ALWAYS BE LEFT OPEN-CIRCUIT.

Fig. 1 Pin connections (top)

FEATURES

- Military and Industrial Variants
- 300 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps and O/Ps
- Low Propagation Delay
- True and Inverse Outputs

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade – 55°C to + 125°C
  'B' Grade 0°C to + 70°C
- Supply Voltage | Vcc - V_{EE} | 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

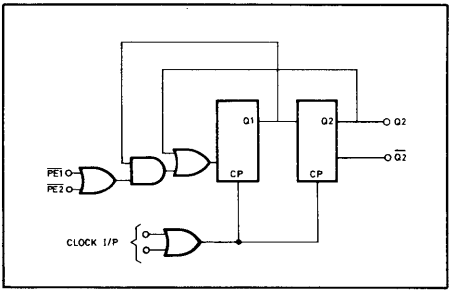


Fig. 2 Logic diagram (positive logic)

ABSOLUTE MAXIMUM RATINGS

Supply voltage |Vcc — V_{EE}|	8V
Input voltage V_{in} (d.c.)	Not greater than the supply voltage in use.
Output current $\|_{out}$	20mA.
Max. junction temperature	+150°C
Storage temperature range	—55°C to +175°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: 'A' Grade −55°C to +125°C
'B' Grade 0°C to +70°C
Supply coltage (see note 1): V_{CC} = 0V
V_{EE} = −5.2V

Static Characteristics

Charactistic	Value			Units	Conditions
	Min	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see note
Input pulldown resistance, between pins 1, 2, 3 and 16 and V_{EE} (pin 12)		4.3		k Ω	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2k Ω pulldown resistor on each output)
Power supply drain current		45	60	mA	

NOTES
1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} =0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock input voltage levels					
V_{INH}	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	−1.70		−1.50	V	see note 4
Max. toggle frequency	300			MHz	
Min. frequency with sinewave clock input			10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz			20	V/μs	
Propagation delay (clock input to device output)		3		ns	
Set-up time		1.5		ns	See note 5
Release time		1.5		ns	See note 6

NOTES
4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL II and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitude of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L → H transition of a control input and the next L → H clock pulse transition to ensure that the ÷3 mode is forced by that clock pulse (see Fig.3).
6. Release time is defined as the minimum time that can elapse between a H → L transition of a control input and the next L → H clock pulse transition to ensure that the ÷4 mode is forced by that clock pulse (see Fig. 4.)

OPERATING NOTES

The SP8725 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

The ÷3/4 requires ECL control logic at the maximum input frequency, but can be controlled by a TTL fully programmable counter at a reduced input clock frequency. When used the outputs and inputs must be interfaced to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_2 and $\overline{Q_2}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to + 125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 1200MHz this would only leave about 15ns for the fully programmable counter to control the ÷3/4. The loop delay can be increased by extending the ÷3/4 function to, say, ÷12/13 or ÷24/25.

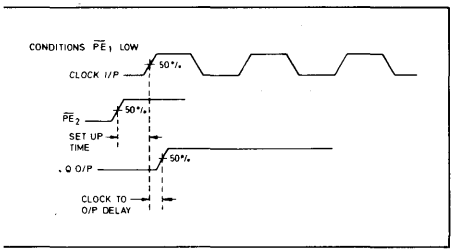


Fig. 3 Set-up timing diagram

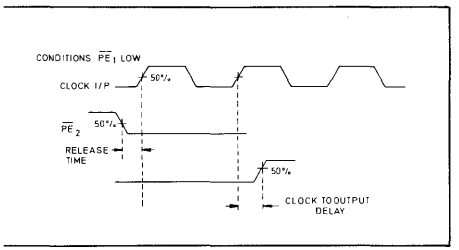


Fig. 4 Release timing diagram

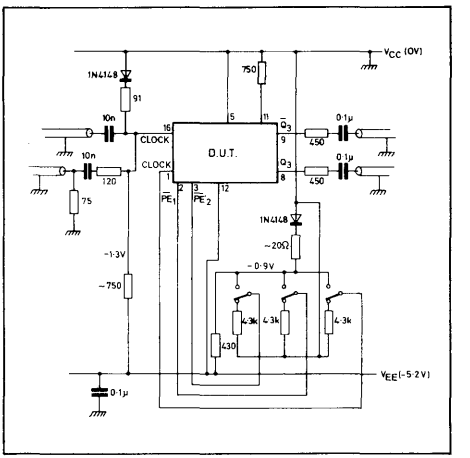


Fig. 5 Test circuit for dynamic measurements

Clock Pulse	Q_1	Q_2	
1	L	H	
2	L	L	
3	H	L	
4	H	H	← Extra State

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio.
L	L	4
H	L	3
L	H	3
H	H	3

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L→H transition from Q_2 or the H→L transition from $\overline{Q_2}$ is used to clock the stage controlling the ÷3/4 circuit. The loop delay is 3 clock periods minus the internal delays of the ÷ 3/4 circuit.

The SP8725 device O/Ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can also be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

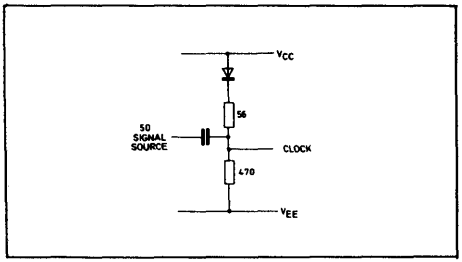


Fig 6. Recommended input bias configuration for capacitive coupling to a continuous 50 Ω signal source

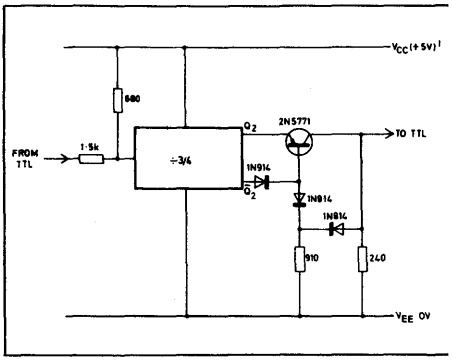


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8725 device and TTL operating from the same supply rails)

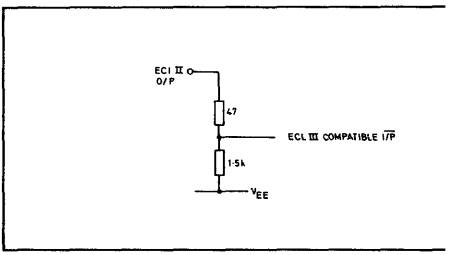


Fig. 8 ECL II to ECL III interface.

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SP 8000 SERIES

HIGH SPEED DIVIDERS

SP8735B

÷8 AT 600MHz WITH BINARY OUTPUTS

The SP8735B is a divide-by-eight circuits with binary outputs for operation from DC up to specified input frequencies of 600 MHz and 500 MHz respectively over a guaranteed temperature range of 0°C to +70°C.

This device, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The binary outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacively coupled to the signal source, is gated by an ECL I/ECL 10K compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other outputs.

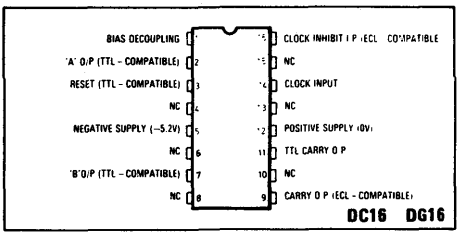

Fig.1 Pin connections (viewed from top)

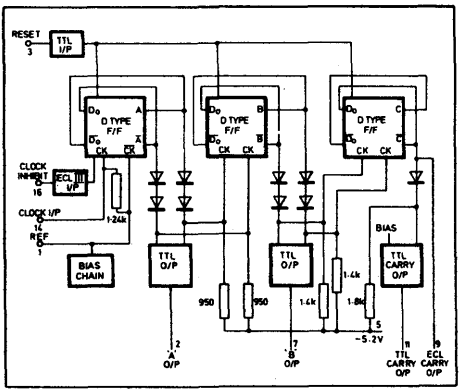

Fig.2 SP8735 logic diagram

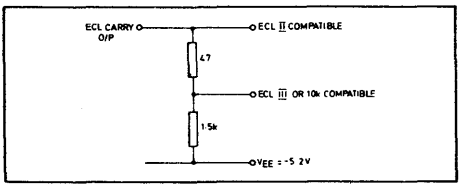

Fig.3 ECL II to ECL 10K interface

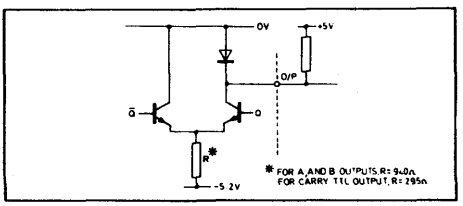

Fig. 4 TTL output circuit diagram

FEATURES

- Direct Gating Capability at up to 600 MHz
- TTL Compatible Binary Outputs
- TTL and ECL Compatible Carry Outputs
- Power Consumption Less Than 450mW
- Wide Dynamic Input Range

APPLICATIONS

- Counters
- Timers
- Synthesisers

QUICK REFERENCE DATA

- Power Supplies: V_{cc} 0V
  V_{ee} −5.2V ± 0.25V
- Range of Clock Input Amplitude: 400 – 800 mV p-p
- Operating Temperature Range:
  0°C to 70°C
- Frequency Range with Sinusoidal I/P: 40 – 600MHz
- Frequency Range with Square Wave I/P: DC to 600MHz

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated):

T_{amb} 0°C to +70°C
Power Supplies V_{CC} OV
V_{EE} −5.2V ±0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock input (pin 14)					
Max. input frequency SP8735B	600			MHz	Input voltage 400–800mV p-p
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
High level (inhibit)	−0.960			V	T_{amb} = +25°C (see note 1)
Low level			−1.650	V	
Edge speed for correct operation at max. clock I/P frequency			2.5	ns	10% to 90%
Reset input (pin 3)					
High level (reset)	See note 2				See note 2
Low level			+0.4	V	
Reset ON time	100			ns	
TTL outputs A & B (pins 2 & 7)					
Output high level	+2.4			V	10k Ω resistor and 3 TTL gate
Output low level			+0.4	V	from O/P to 5V rail (see note 3)
TTL carry output (pin 11)					
Output high level	+2.4			V	5k Ω resistor and 3 TTL gates from O/P to +5V rail
Output low level			+0.4	V	
ECL carry output (pin 9)					
Output high level	−0.975			V	T_{amb} = +25°C
Output low level			−1.375	V	External current = 0mA (See note 4)
Power supply drain current		70	90	mA	V_{EE} − 5.2V

NOTES

1. The clock inhibit input levels are compatible with the ECL III and ECL 10K levels throughout the temperature ranges specified.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series devices.
3. These outputs are current sources which can be readily made TTL compatible voltages by connecting them to +5V via 10k Ω resistors (see Fig. 4).
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

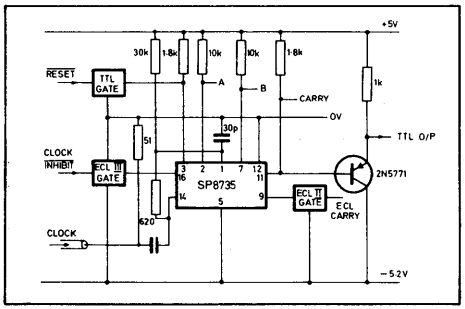

Fig.5 Typical operating diagram

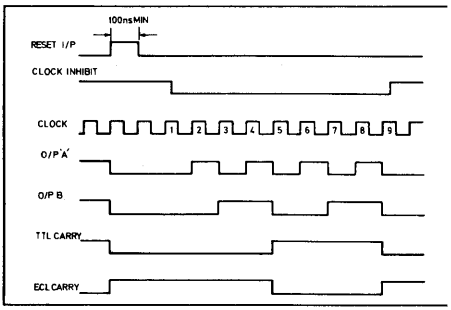

Fig.6 Output waveforms

OPERATING NOTES

The device is intended to be used with TTL and ECL in a counting system — the ECL and the decade counter being connected between voltage rails of 0V and −5.2V and the TTL between voltage rails of 0V and +5V. Provided that this is done ECL and TTL compatibility is achieved. (See Figs. 4 and 5)

The clock is normally capacitively coupled to the signal source: a 1000 pF UHF capacitor should be adequate. For low frequency operation, the 1000 pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor — preferably a chip type, but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV p – p. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{cc} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 30Ω resistor between the clock input and the positive supply and a 620Ω resistor between clock and pin 1. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason the input slew rates should be greater than 100V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit will clock the device, provided that the other input is in the low state.

The binary outputs give TTL-compatible outputs (fan out = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the counter and so the state on the TTL outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

A typical application is shown in Fig. 7.

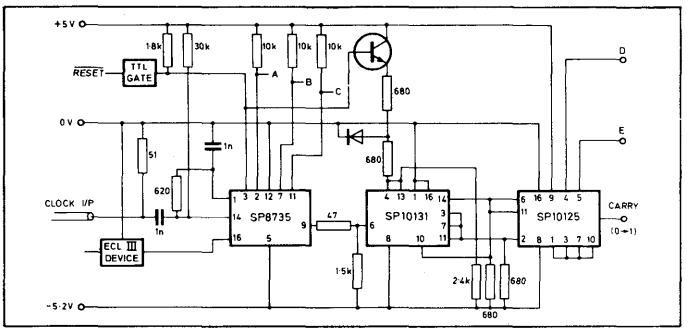

Fig.7 600MHz ÷ 32 with reset and inhibit

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8740.A & B
AC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 5/6

The SP8740 A & B are high speed programmable ÷5/6 counters operating at an input frequency of up to 300 MHz over the temperature ranges −55°C to +125°C, 0°C to +70°C.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 5 when either input is in the high state, and by 6 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

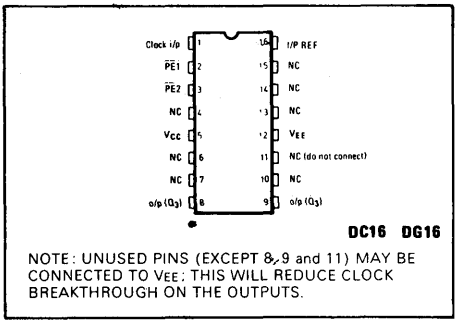
When using the device as a divide-by-five prescaler the inverse output (o/p) should be connected to a PE input.

Clock Pulse	Q_1	Q_2	Q_3	
1	L	H	H	
2	L	L	H	
3	L	L	L	
4	H	L	L	
5	H	H	L	
6	H	H	H	← Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Table 2 Truth table for control inputs



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO VEE; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

Fig. 1 Pin connections

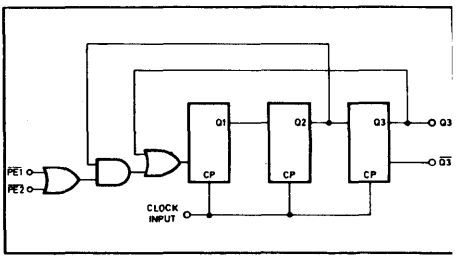


Fig. 2 Logic diagram SP8740

FEATURES

- Full Temperature Range Operation
  - 'A' Grade —55°C to +125°C
  - 'B' Grade 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

Test conditions (unless otherwise stated)

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V
Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	300			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown Resistors		4.3		KΩ	
Clock i/p impedance (i/p to i/p ref low frequency)		400		Ω	

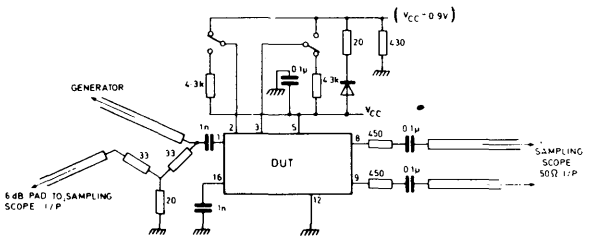


Fig. 3 Test circuit

APPLICATION NOTES

When operating the SP8740 in a synthesiser loop at 300MHz, the delay time through the programmable divider controlling the SP8740 is approximately 13ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

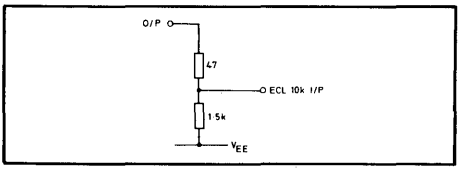


Fig. 4

The simple passive interface from the output of the SP8740 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins and the output of the SP8740 into TTL, is shown in Fig. 5

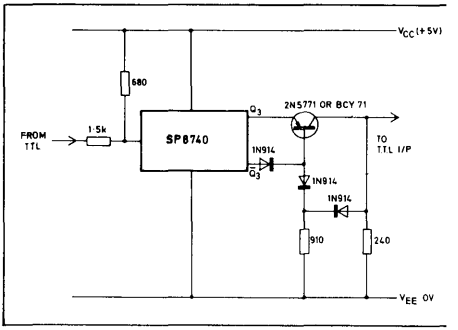


Fig. 5

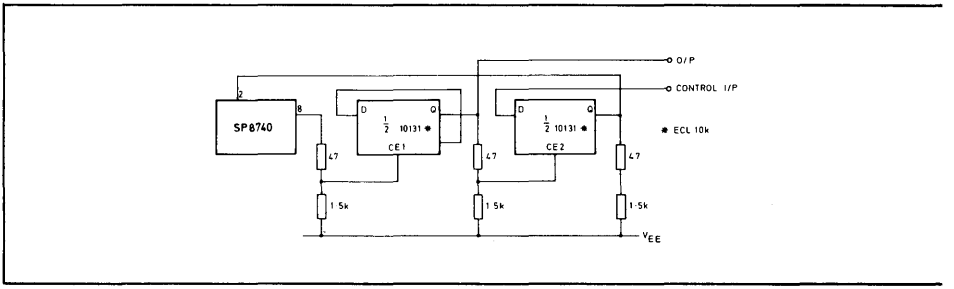


Fig. 6 Divide by 10/12. Control loop delay time approximately 33 ns

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8741 A & B
AC COUPLED UHF PROGRAMMABLE DIVIDERS 300 MHz ÷ 6/7

The SP8741 A,' B & M are high speed programmable ÷6/7 counters operating at an input frequency of up to 300 MHz over the temperature ranges −55°C to +125°C, 0°C to 70°C.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 6 when either input is in the high state, and by 7 'when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-six prescaler the inverse output (o/p) should be connected to a PE input.

Clock Pulse	Q_1	Q_2	Q_3	
1	L	H	H	
2	L	L	H	
3	H	L	H	
4	L	H	L	
5	L	L	L	
6	H	L	L	
7	H	H	H	← Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Table 2 Truth table for control inputs

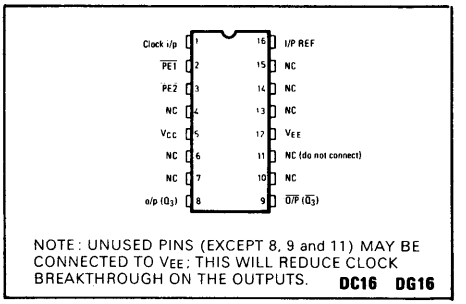

Fig. 1 Pin connections

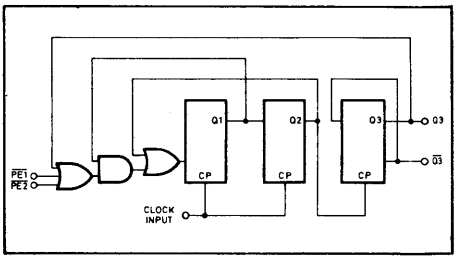

Fig. 2 Logic diagram

FEATURES

- Full Temperature Range Operation
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

Test conditions (unless otherwise stated)

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V
Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	300			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propagation delay					
(clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown					
Resistors		4.3		KΩ	
Clock i/p impedance					
(i/p to i/p ref low frequency)		400		Ω	

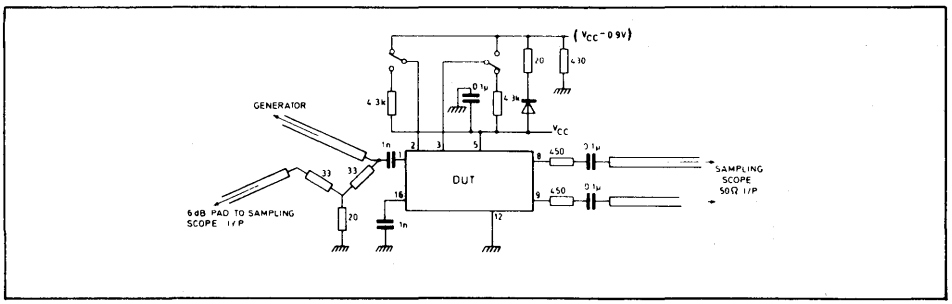

Fig. 3 Test circuit

APPLICATION NOTES

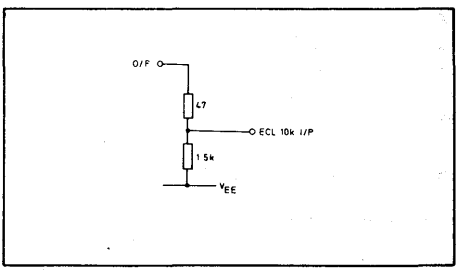

Fig. 4

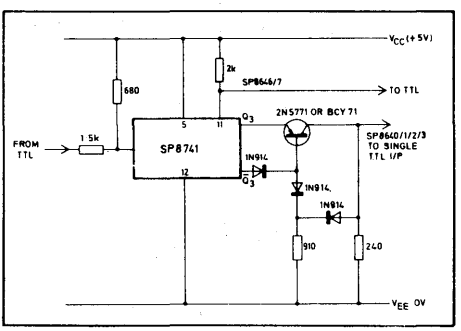

Fig. 5

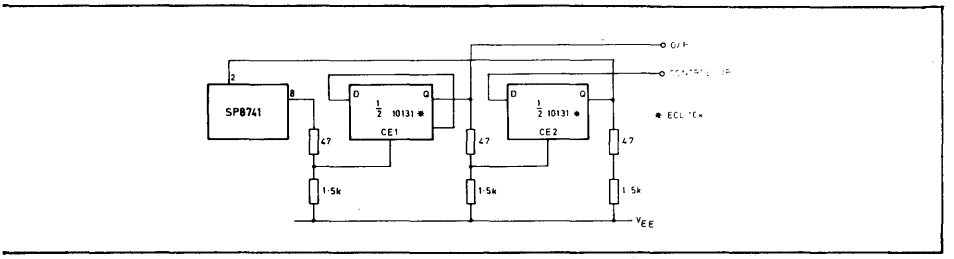

Fig. 6 Divide-by-12/14. Control loop delay time approximately 40ns.

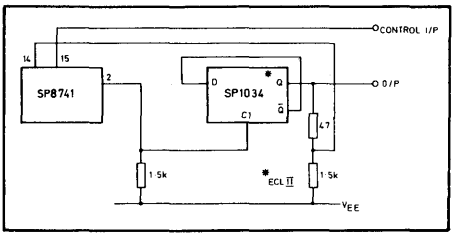

Fig. 7 Divide-by-12/13. Control loop delay time approximately 30ns using SP1034.

When operating the SP8741 in a synthesiser loop at 300MHz the delay time through the programmable divider controlling the SP8741 is approximately 16ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8741 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8741 into TTL, is shown in Fig. 5.

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1641 Kaiser Avenue,
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SP 8000 SERIES

HIGH SPEED DIVIDERS

SP 8743 B & M

AC COUPLED UHF PROGRAMMABLE DIVIDER 500 MHz ÷8/9

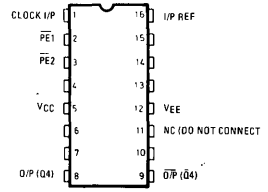
The SP8743M and B are high speed, programmable ÷ 8/9 counters operating at an input frequency of up to 500MHz over the temperature ranges −40°C to +85°C and 0°C to 70°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 8 when either input is in the high state and by 9 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-eight prescaler the inverse output (o/p) should be connected to a $\overline{PE}$ input.



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

DG 16
DC 16

Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $\lvert V_{CC} - V_{EE} \rvert$	0V to +8V
Input voltage PE inputs	0V to V_{CC}
Input voltage CP input	2V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

FEATURES

- Operating Temperature Range:
  0°C to 70°C ('B' grade)
  −40°C to +85°C ('M' grade)
- Self Biasing Clock Input
- Wide Input Dynamic Input
- Control Inputs ECL 10K Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

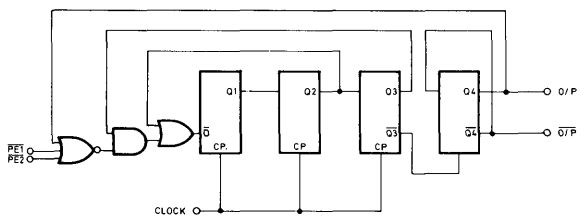


Fig. 2 SP8743 logic diagram

Count Sequence			
Q_1	Q_2	Q_3	Q_4
L	H	H	H
L	L	H	H
H	L	L	L
H	H	L	L
L	H	H	L
L	L	H	L
L	L	L	H ← Extra state
H	L	L	H
H	H	L	H

Division Ratio				
	9	8	8	8
$\overline{PE1}$	L	L	H	H
$\overline{PE2}$	L	H	L	H

LECTRICAL CHARACTERISTICS

$\overline{E}$ inputs – ECL 10K compatible
utputs – ECL II compatible

Test Conditions (unless otherwise stated):
TAMB 0 °C to +70 °C ('B' grade) –40 °C to + 85 °C ('M' grade)
Supply Voltage V_{CC} = +5.2V ± 0.25V V_{EE} = 0V
Clock Input Voltage 400mV to 800mV p-p

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency	500			MHz	V_{CC} = +5.2V
Min. i/p frequency			40		Sinewave Input
Min. Slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{CC} = +5.2V, 25°C
Power Supply drain current		45	60	mA	V_{CC} = +5.2V, 25°C
$\overline{PE}$ input pulldown resistors		4.3		kΩ	
Clock i/p impedance (i/p to i/p ref. low freq.)		400		Ω	

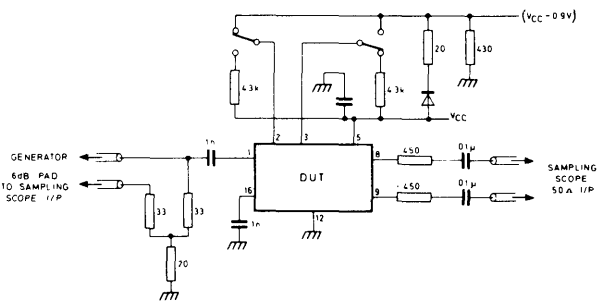


Fig. 3 Test circuit

APPLICATIONS INFORMATION

Interfaces

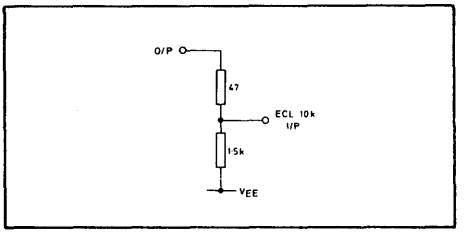


Fig. 4

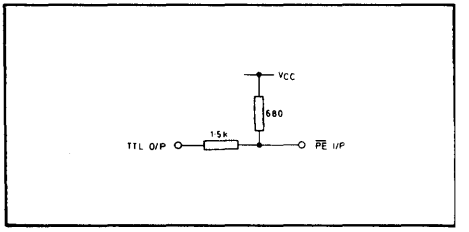


Fig. 5

When operating the SP8743 in a synthesiser loop at 500MHz, the delay time through the programmable divider controlling the SP8743 is approximately 12ns As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8743 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8743 into TTL, is shown in Fig. 5.

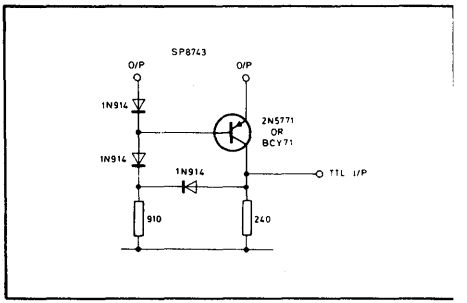


Fig. 6 SP8743 O/P to TTL I/P. Total delay from SP8743 clock I/P to Schottky gate O/P = 15ns typical.

Sub-Systems

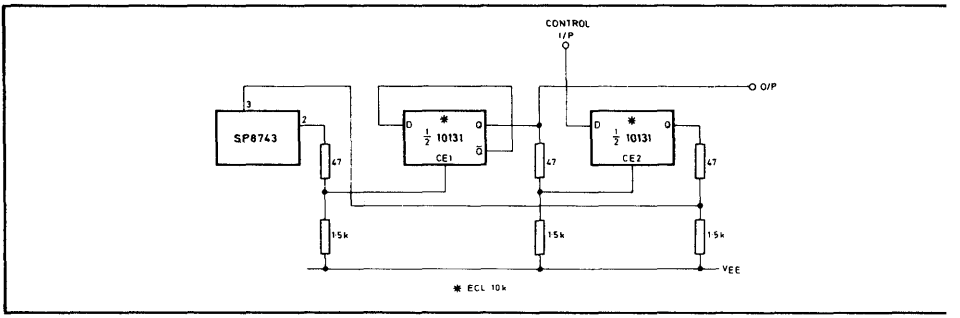


Fig.7 A ÷32/33 application. Control loop delay time approx. 56ns.

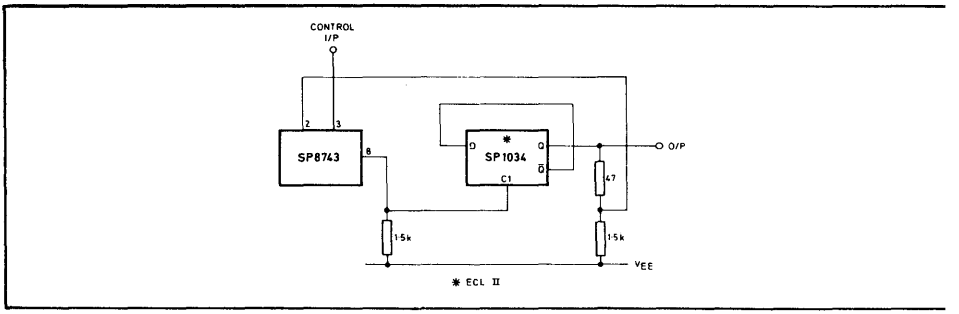


Fig.8 A÷16/17 application. Control loop delay time approx. 24ns using SP1034

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SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8745 A & B
DC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 5/6

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8745 series are UHF integrated circuits that can be logically programmed to divide by either 5 or 6 with input frequencies up to 300 MHz. MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL III-compatible while the two complementary outputs are ECL II-compatible to reduce power consumption in the output stage. ECL III output compatibility can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 5 when either $\overline{PE}$ input is in the high state and by 6 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3kΩ pulldown resistors to V_{EE} (negative rail)

FEATURES

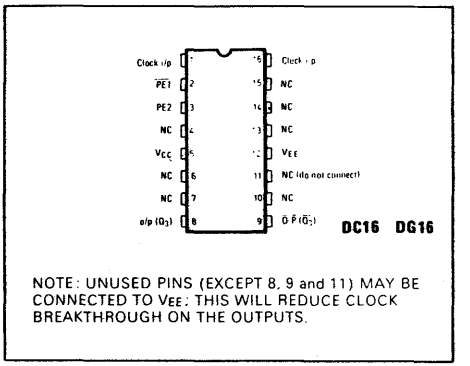
- Military and Industrial Variants.
- 300 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
- Supply Voltage
  $|V_{CC} - V_{EE}|$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\|V_{CC} - V_{EE}\|$	8V
Input voltage $V_{in\ (d.c.)}$	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

Fig. 1 Pin connections (top)

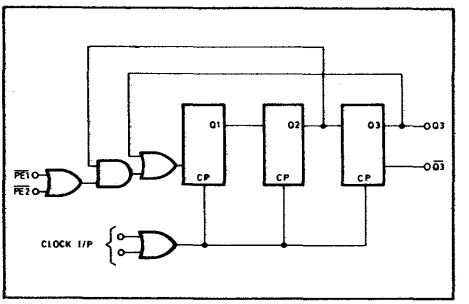


Fig. 2 Logic diagram (positive logic)

Clock Pulse	Q_1	Q_2	Q_3	
1	L	H	H	
2	L	L	H	
3	L	L	L	
4	H	L	L	
5	H	H	L	
6	H	H	H	← Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L → H transition from Q_3 or the H → L transition from $\overline{Q_3}$ is used to clock the stage controlling the ÷5/6. The loop delay is 5 clock periods minus the internal delays of the ÷5/6 circuit.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: (A grade) −55°C to +125°C
(B grade) 0°C to +70°C
Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal EC supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

)ynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	All	300			MHz	
Min. frequency with sinewave clock input	All			10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz	All			20	V/μs	
Propagation delay (clock input to device output)	All		3		ns	
Set-up time	All		1.5		ns	See note 5
Release time	All		1.5		ns	See note 6

OTES

The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.

Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷5) mode is forced by that clock pulse (see Fig. 3).

Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷6 mode is forced by that clock pulse (see Fig. 4).

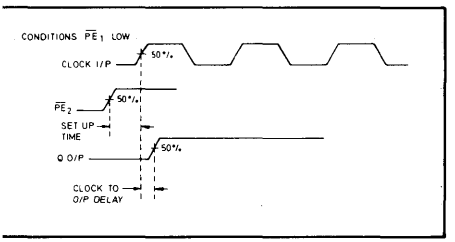


Fig. 3 Set-up timing diagram

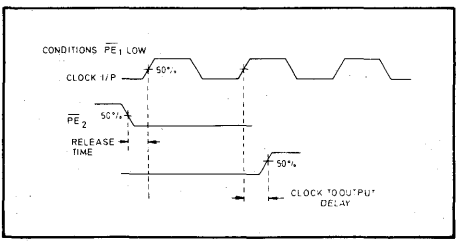


Fig. 4 Release timing diagram

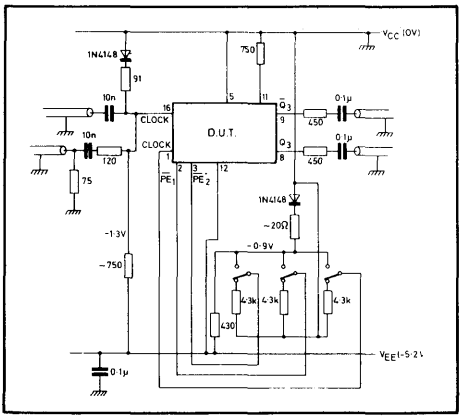


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8745 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig.6, or alternatively an internally biased SP8742.

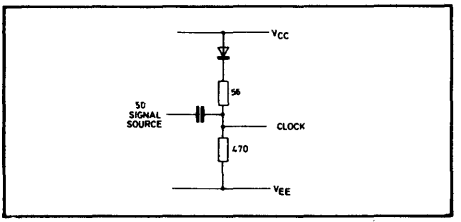


Fig. 6 Recommended input bias configuration for capacitive coupling to a continuous 50Ω signal source.

The ÷5/6 can be controlled by a TTL fully-programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_3 and $\overline{Q_3}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 300 MHz this would only leave about 6.5ns for the fully-programmable counter to control the ÷5/6. The loop delay can be increased by extending the ÷5/6 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

The SP8745 device O/Ps are compatible with ECL II level: when there is no external load. They can be mad compatible with ECL III and ECL 10K with a simpl potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatibl with ECL III and ECL 10K. The interface circuit of Fig. can also be used to increase noise immunity whe interfacing from ECL III and ECL 10K outputs at lo current levels to ECL III and ECL 10K inputs.

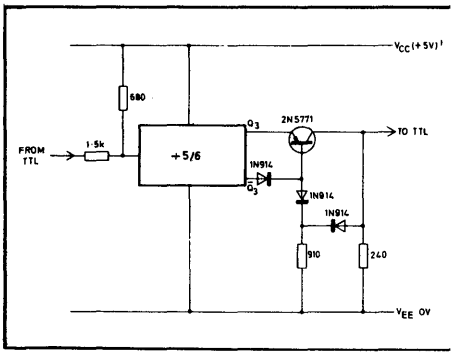


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8745 device and TTL operating from the same supply rails)

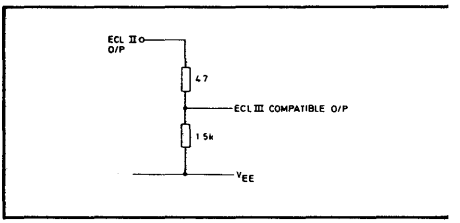


Fig. 8 ECL II to ECL III interface

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Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

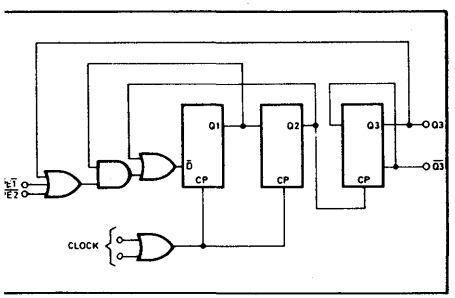
SP 8746 A&B
DC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 6/7

In frequency synthesis it is desirable to start rogrammable division at as high a frequency as possible, ecause this raises the comparison frequency and so nproves the overall synthesiser performance.

The SP8746 series are UHF integrated circuits that an be logically programmed to divide by either 6 or 7, . ith input frequencies up to 300 MHz. The design of very ist fully programmable dividers is therefore greatly mplified by the use of these devices and makes them articularly useful in frequency synthesisers operating in ie UHF band.

All inputs and outputs are ECL-compatible throughout ie temperature range: the clock inputs and programming iputs are ECL III -compatible while the two omplementary outputs are ECL II-compatible to reduce ower consumption in the output stage. ECL III output ompatibility can be achieved very simply, however (see perating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The ounter will divide by 6 when either $\overline{PE}$ input is in the igh state and by 7 when both inputs are in the low state. oth the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}: THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

DC16 DG16

Fig. 1 Pin connections (top)

Fig. 2 Logic diagram (positive logic)

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage $V_{in\ (d.c.)}$	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

FEATURES

- Military and Industrial Variants.
- 300 MHz Toggle Frequency.
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
- Supply Voltage
  $\lvert V_{CC} - V_{EE} \rvert$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

Clock Pulse	Q_2	Q_3	Q_4
1	L	H	H
2	L	L	H
3	H	L	H
4	L	H	L
5	L	L	L
6	H	L	L
7	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L → H transition from Q_3 or the H → L transition from $\overline{Q_3}$ is used to clock the stage controlling the ÷6/7. The loop delay is 6 clock periods minus the internal delays of the ÷6/7 circuit.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal EC supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

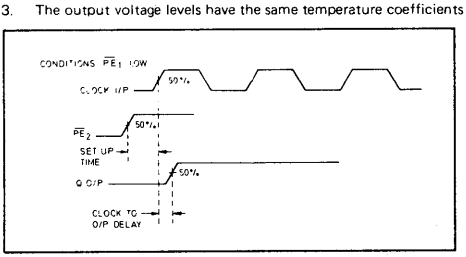


Fig. 3 Set-up timing diagram

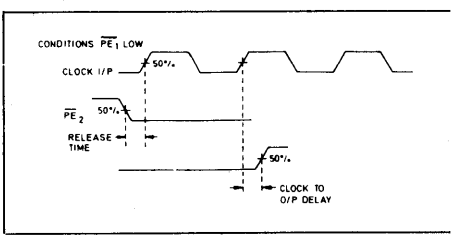


Fig. 4 Release timing diagram

ynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	All	300			MHz	
					MHz	
					MHz	
					MHz	
Min. frequency with sinewave clock input				10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz				20	V/μs	
Propagation delay (clock input to device output)			3		ns	
Set-up time			1.5		ns	See note 5
Release time			1.5		ns	See note 6

TES

The devices are dynamically tested using the circuit shown in Fig.5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.

Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷6 mode is forced by that clock pulse (see Fig. 3).

Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷7 mode is forced by that clock pulse (see Fig. 4).

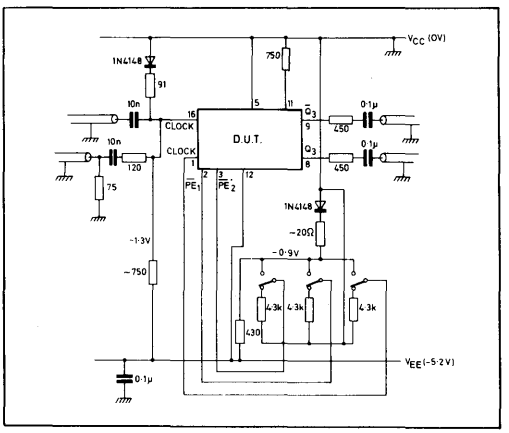


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8746 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control imputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6. Alternatively an SP8741 can be substituted.

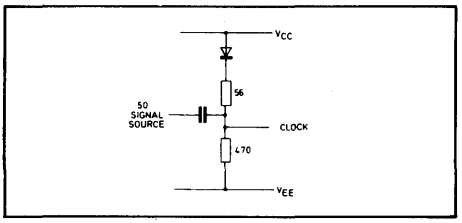


Fig. 6 Recommended input bias configuration for capacitive coupling to a continuous 50Ω signal source.

The ÷6/7 can be controlled by a TTL fully-programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_3 and $\overline{Q_3}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 300 MHz this would only leave about 10 ns for the fully programmable counter to control the ÷6/7. The loop delay can be increased by extending the ÷6/7 function to, say, ÷24/25 or 48/49 (see Application Notes)

The SP8746 device O/Ps are compatible with ECL II leve when there is no external load. They can be ma compatible with ECL III and ECL 10K with a simp potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatit with ECL III and ECL 10K. The interface circuit of Fig. can also be used to increase noise immunity wh interfacing from ECL III and ECL 10K outputs at lc current levels to ECL III and ECL 10K inputs.

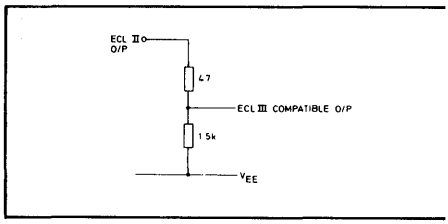


Fig. 8 ECL II to ECL III interface

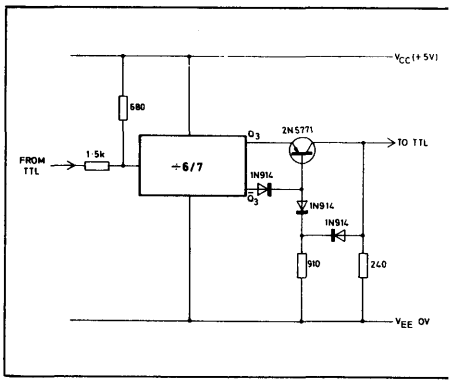


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8746 device and TTL operating from the same supply rails)

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP 8000 SERIES

HIGH SPEED DIVIDERS

SP 8750 B,M 1.0 GHz SP 8752 B 1.2 GHz

UHF ÷ 64 PRESCALERS

The SP8750 range of devices are ECL vide-by-sixtyfours which will operate at frequencies up to 2GHz.

The device has a typical power dissipation of 470mW at ıe nominal supply voltage of +6.8V.

EATURES

- Input Ports for VHF and UHF
- Self-Biasing Clock Inputs
- Variable Input Hysteries Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input
- Push Pull TTL. O/P

ıBSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Band change input	+7.2 tc −0.5V or −10mA
Output current	+30 mA to −30 mA
Operating junction temperature	+150°C
Storage Temperature	−55°C to +150°C

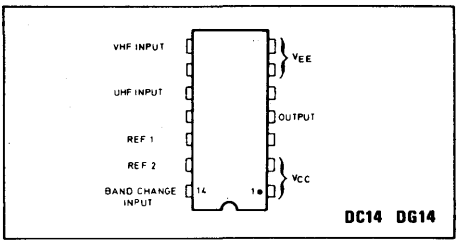


Fig. 1 Pin connections

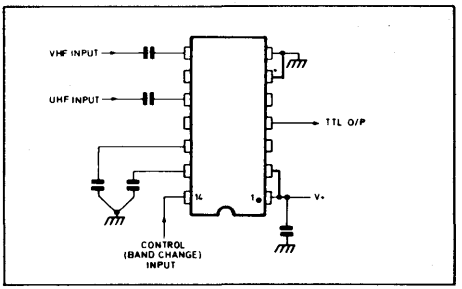


Fig. 2 Typical application

ıPERATING NOTES

Two input ports are available on this device. Switching etween these inputs is accomplished by operation of the and change input. A logic '1' activates the UHF input, ɔgic '0' the VHF input. When an input is not in use the ıput signal must be removed to prevent cross-modulation ccuring on the other input at high frequencies. Both in- uts are terminated by a nominal 400 and should be AC oupled to their respective signal sources. Input power to ıe device is terminated to ground by the two decoupling apacitors on the reference pins. Input coupling and eference decoupling capacitors should be of a type suitable or use at a frequency of 1.2Hz.

When the device is switched to the VHF input, an input ysteresis of 50mV is set by the internal band change ircuit. This improves the low frequency sinewave opera- ion of the device. The hysteresis level may be measured s $V_{REF1} - V_{REF2}$.

If the UHF input only is used and the device is required to operate with a sinewave input below 100 MHv, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The devices may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/µs.

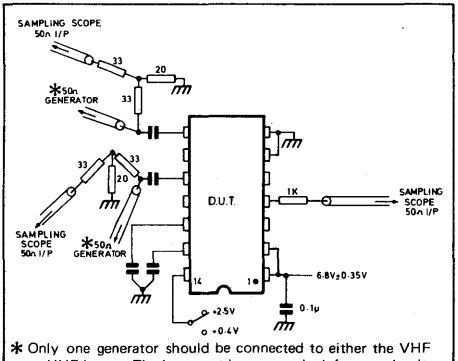
The divider is clocked on low to high transitions of either clock input.

ELECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 68 mA typ., 90 mA max.
Temperature range: 'B' grade 0°C to +70°C, 'M' grade −40°C to +85°C
Clock inputs: AC coupled, self-biasing via 400Ω
Band change input: TTL type including negative input voltage clamp, 0.8 mA max. sink current

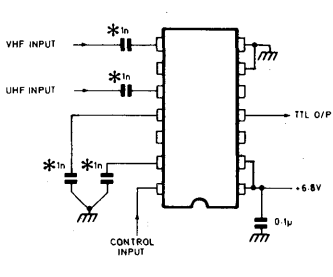
Test conditions (unless otherwise stated):
Supply voltage: V_{EE} = 0V, V_{CC} = +6.45V to +7.15V
Clock input voltage: 400mV to 1.0Vp-p
T_{amb} = 0°C to +70°C ('B' grade), −40°C to +85°C ('M' grade)

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
UHF clock input						
Max. input frequency	SP8752	1.2			GHz	600mV p-p input
	SP8751	1.1			GHz	600mV p-p input
	SP8750	1.0			GHz	400mV p-p input
Min. input frequency	All			100	MHz	600mV p-p sinewave input
Min. slew rate for square wave input	All			200	v/μs	
VHF clock input						
Max. input frequency	All		1.0		GHz	
Min. input frequency			30	50	MHz	600mV p-p sinewave input
Band change input						
High level	All	2.5			V	
Low level				0.4	V	
Low level input current	All			0.8	mA	at 0.4V
Max. clamp current	All	−3			mA	at approx. −0.7V
Output						
High level	All	2.5	3.5	4.5	V	
Low level				0.4	V	5mA current sink
Supply current	All		68	90	mA	V_{CC} = 6.8V



* Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

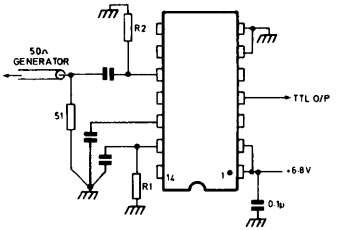
Fig. 3 AC test circuit



*Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

For single input operation leave pins 8 and 14 open circuit.

Fig. 4 Application circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.
For 50 mV hysteresis R1 = 36kΩ R2 = ∞
For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

Fig. 5 Wideband operation

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

SP8755A & B

1200 MHz ÷ 64 PRESCALER

FEATURES

- DC to 1200MHz
- -55°C to +125°C temperature range
- TTL compatible output

QUICK REFERENCE DATA

- Supply voltage 5V ±0.25V
- Power consumption 270mW typ. (no load)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	2.5V p-p
Output current	+30 mA to -30 mA
Operating junction temperature	+150°C
Storage Temperature	-55°C to +150°C

OPERATING NOTES

The input is terminated by a nominal 400Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the decoupling capacitor on the reference pin. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1GHz.

If the device is required to operate with a sinewave input below 100MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when the clock input changes from a low to a high level.

The device may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/μs.

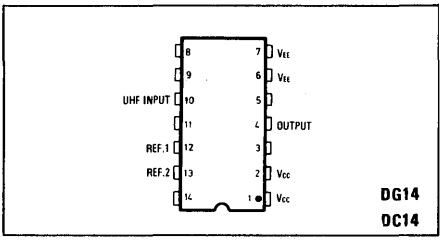


Fig. 1 Pin connections

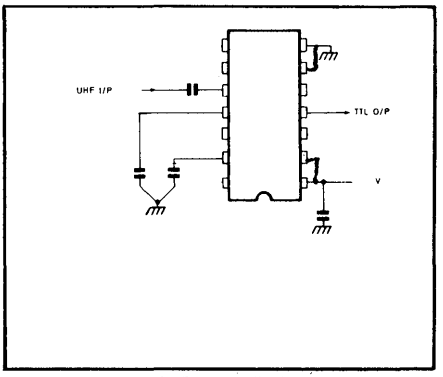


Fig. 2 Typical application

LECTRICAL CHARACTERISTICS

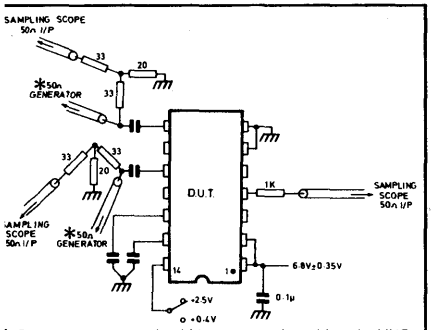
ıst conditions (unless otherwise stated):

Supply voltage V_{CC} : 4.75V to 5.25V

Input signal amplitude : 400mV to 1.0V (f < 1GHz)
600mV to 1.2V (1GHz≤ f < 1.2GHz)

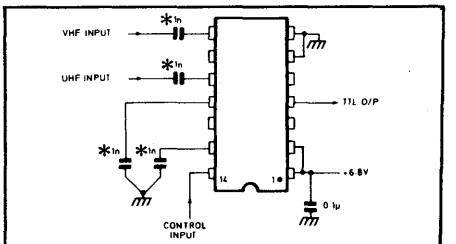
Ambient temperature : -30°C to +70°C (SP8755B)
-55°C to +125°C (SP8755A)

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		54	75	mA	
Max. input frequency	1200			MHz	600mV pk-pk sine wave input
Min. input frequency			100	MHz	
Min. slew rate (with square wave input)			200	V/μS	
Output voltage level (high)	2.5		4.5	V	V_{CC} = 5.0V
Output voltage level (low)			0.4	V	5mA current into pin 4



* Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

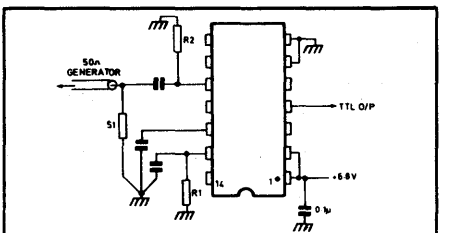
Fig. 3 AC Test Circuit



*Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

For single input operation leave pins 8 and 14 open circuit.

Fig. 4 Application Circuit



Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

For 50 mV hysteresis R1 = 36kΩ R2 = ∞

For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

Fig. 5 Wideband Operation

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8770B 1.0GHz SP8772B 1.2GHz
UHF ÷ 256 PRESCALERS

The SP8770/1/2 are ECL divide by 256 prescalers which will operate at frequencies up to 1.2 GHz.
The device has a typical power dissipation of 500mW at the nominal supply voltage of +6.8V.

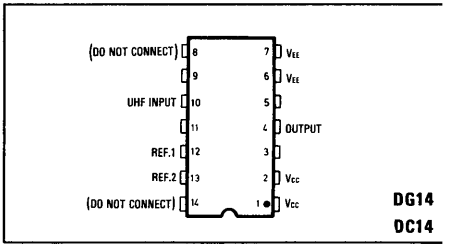


Fig. 1 Pin Connections

FEATURES

- Self-Biasing Clock Input
- Variable Input Hysteries Capability for Wide Band Operation
- Push Pull TTL O/P

OPERATING NOTES

The input is terminated by a nominal 400Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

If the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 4.

Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 256 output is designed to interface with TTL which has a common V_{EE} (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/ Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The devices may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/μs.

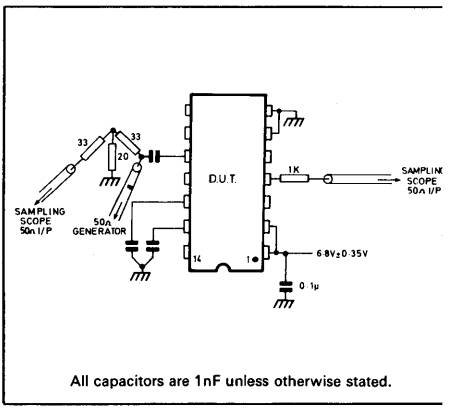


Fig. 2 AC test circuit

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC}-V_{EE}\rvert$	0V to +10V
Input voltage, clock input	2.5V p-p
Output current	+30mA to −30mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

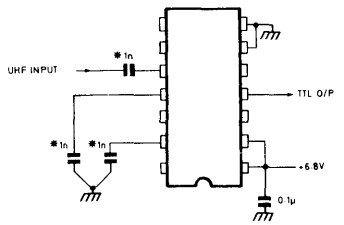
.ECTRICAL CHARACTERISTICS

Supply voltage: 6.8V ± 0.35V
Supply current: 72mA typ., 95mA max.
Temperature range: 0°C to +70°C
Clock input: AC coupled, self biasing via 400 Ω

Test conditions (unless otherwise stated):

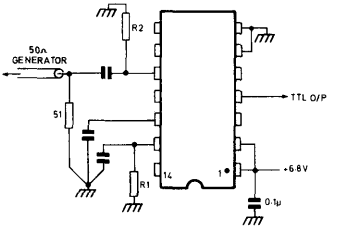
Supply voltage: V_{EE} = 0V,
V_{CC} = +6.45V to + 7.15V
Clock input voltage: 400mV to 1.2V p-p
T_{amb} = 25°C

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Max. input frequency	SP8770	1.0			GHz	400mV p-j. input
	SP8772	1.2			GHz	600mV p-j. input
Min input frequency				200	MHz	400mV p-j. sinewave input
				100	MHz	600mV p-j. sinewave input
				75	MHz	800mV p-j. sinewave input
Min. slew rate for square wave input				200	V/μs	
Output						
High level		2.5	3.5	4.5	V	
Low level				0.4	V	5mA current sink
Supply current			68	90	mA	V_{CC}=6.8V



* Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1 GHz.

Fig. 3 Application circuit

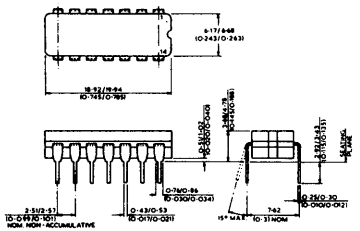


Capacitors are 1 nF unless otherwise stated. Values should be increased if operation below 10 MHz is desired.
For 50mV hysteresis R1=36kΩR2=∞
For 100mV hysteresis R1=18kΩR2=18kΩ

Fig. 4 Wideband operation

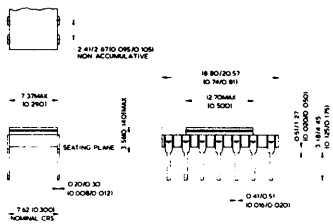
PACKAGE DETAILS

Dimensions are shown thus: mm (in)



14 LEAD CERAMIC D.I.L.

DG14



14 LEAD DILMON

DC14

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP 8000 SERIES

HIGH SPEED DIVIDERS

SP8760 B & M

GENERAL PURPOSE SYNTHESISER CIRCUIT

The SP8760 is a multi-function device for use in ıase-lock-loop systems. It contains a crystal oscillator aintaining circuit, followed by a divide-by-four stage; digital phase/frequency comparator; and a two-odulus divider programmable to divide by 15 or 16.

It may be used with a prescaler to phase-lock single equency transmitters or receivers in the HF, VHF or HF bands.

The addition of an MOS/CMOS programmable plus ed divider will generate a complete frequency synthe-ser. The maximum frequency requirement of the control vice is only 1 MHz, enabling complex functions to be rformed using LSI technologies. With suitable pre-alers, the controlled frequency source may extend to the 1GHz region.

The SP8760 is available in two temperature grades: C to +70°C ('B' grade) and −40°C to +85°C ('M' ade).

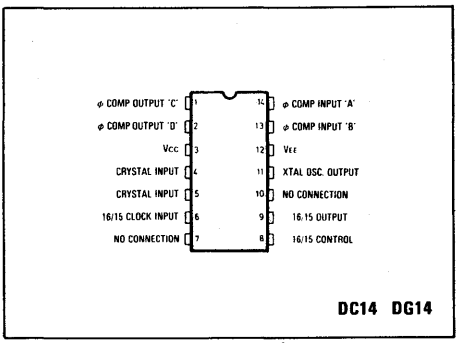


Fig. 1 Pin connections

FEATURES

- TTL/MOS Compatible Inputs and Outputs
- Low Power Consumption (<250mW Typ)
- Minimum External Components
- Voltage Pump Outputs on Phase/ Frequency Comparator
- Zero Phase Difference Pulses <30nSec
- Crystal Oscillator Stability + 5 ppm at 4MHz, 0°C to + 70°C
- Crystal Oscillator Interfaces with SL680 for Very High Stability Applications

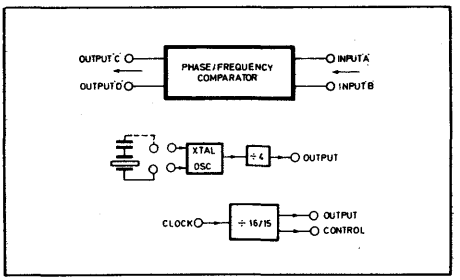


Fig. 2 SP8760 block diagram

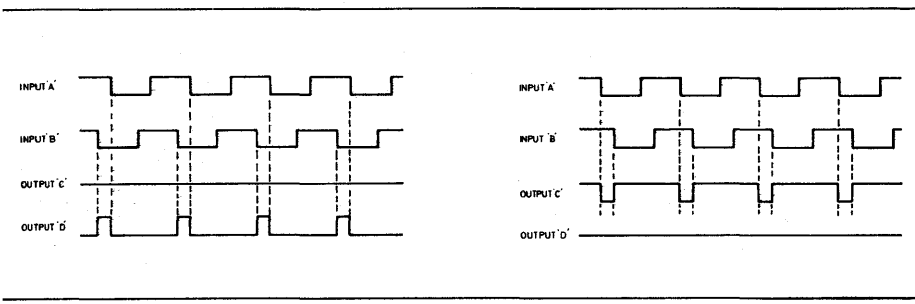


Fig. 3 Phase/frequency comparator waveforms

ELECTRICAL CHARACTERISTICS

Supply voltage 5V ± 0.5V
Supply current 45mA typ

Test conditions (unless otherwise stated):
V_{CC} = 4.5V to 5.5V
V_{EE} = 0V
T_{AMB} 0°C to +70°C ('B' grade)
−40°C to +85°C ('M' grade)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Power Supply Current		45	65	mA	
Crystal Osc. ÷4					
Crystal series capacitor		28		pF	at 4MHz
Crystal series capacitor		20		pF	at 10 MHz
Temperature Stability			0.2	ppm/°C	at 4MHz, excluding crystal temperature coefficient.
Supply voltage stability		−1		ppm/V	at 4 MHz
External oscillator drive required		±1		mA	See Fig. 8.
Divide-by-four output, external current sink capability	5			mA	at 0.5V
Phase/Frequency Comparator					
Input current		250	350	uA	at Vin = 2.4V
Output 'C' current sink capability	6			mA	at 0.5V
Output 'D' current source capability	6				at (V_{CC} - 1.15V)
Zero phase pulse width			30	ns	
Input to Output delay		40		ns	
Divide by 16/15					
Control input current		250	350	µA	at Vin = 2.4V
Clock input current		−1.0	−1.6	mA	at Vin = 0.4V
Output external current sink capability	5			mA	at 0.5V
Maximum clock frequency	16	28		MHz	Divide by 16
	12	18		MHz	Divide by 15
Clock to output delay		35		ns	Output 1 - 0

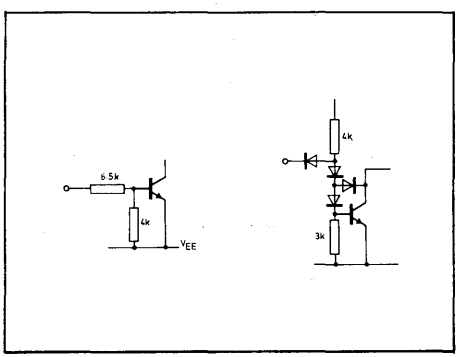


Fig. 4 Phase comp./divider control inputs

ABSOLUTE MAXIMUM RATINGS

Power supply V_{CC} − V_{EE} 0V to +10V
Output current 20mA
Operating junction temperature +150°C
Storage temperature −55°C to +150°C

PERATING NOTES

The crystal oscillator is an emitter coupled circuit :th an internal roll off capacitor to prevent oscillation overtone frequencies. The crystal is connected in ries with a capacitor between pins 4 and 5. It may be ed with series resonant crystals at frequencies up to)MHz. The stability of the crystal oscillator is better an ±5 p.p.m. at 4MHz over the temp range 0°C to)°C (excluding the temperature coefficient of the ystal). If a higher stability is required the SL680 crystal :illator maintaining circuit should be used. This may : interfaced to the SP8760 as shown in Fig. 8. The vide by four has a free collector output with an internal 5 KΩ resistor to Vcc.

The phase frequency comparator is an infinite pull- range circuit which gives zero phase shift lock. The rcuit triggers on the 1 - 0 edge of each input and ves an output which is proportional to the phase fference between the two edges (see Fig. 3). When e input 'A' edge precedes the input 'B' edge output ' will pulse to a low level while output 'D' will remain a permanent low level. When the input 'B' edge pre- :des the input 'A' edge, output 'D' will pulse to a high vel while output 'C' will remain at a permanent high vel. The two outputs may be used to drive a charge ump and filler as shown in Figs. 5 and 6. The output of e filter may be used to drive directly the varactor line of a voltage controlled oscillator. For optimum 'noise' performance the output pulses from the phase detector must tend to zero when 'in lock'. The leakage on the filter output must therefore be kept to a minimum. If the varactor line draws a significant current it should be buffered using an emitter follower arrangement as shown in Fig. 7.

The phase/frequency comparator inputs are of the current source type as shown in Fig. 4. These may be driven by standard TTL or CMOS. Output 'C' is a free collector with an internal 10KΩ resistor to Vcc. Output 'D' is an emitter follower with an internal 10KΩ resistor to VEE.

The two-modulus prescaler may be controlled to divide by 16 or 15 using the control input. With the control input high the circuit will divide by 16. When a counter is used to control the two-modulus it should be clocked on the 1 - 0 edge of the 16/15 output. If the two-modulus is used only as a fixed divide-by-16 the control input - should be tied to Vcc. The prescaler clock input is a current sink input with a standard TTL fan in of one. It may be driven by standard or low power Schottky TTL. The control input is identical to the phase/frequency comparator inputs as shown in Fig. 4. The two modulus output is a free collector with an internal 1.5KΩ resistor to Vcc.

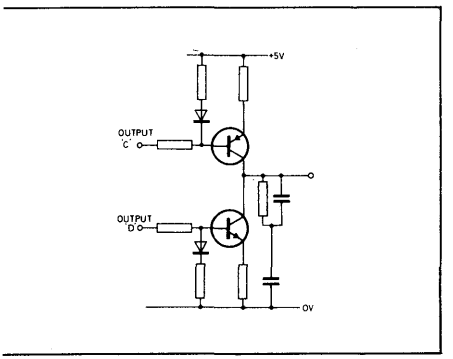


Fig. 5 Low voltage charge pump and filter
Divider clock input

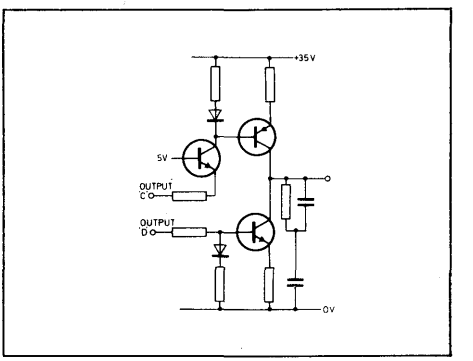


Fig. 6 High voltage charge pump and filter

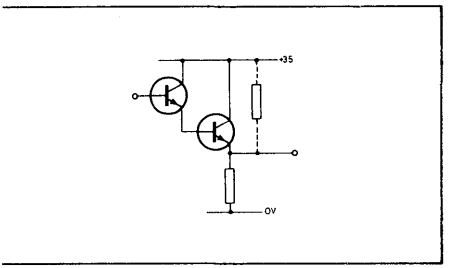


Fig. 7 Emitter follower buffer

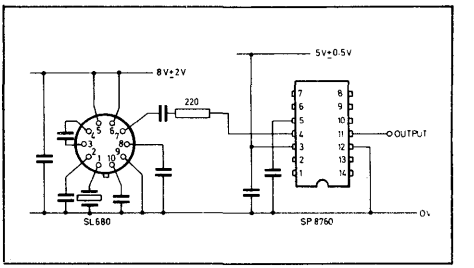


Fig. 8 SL680 to SP8760 interface

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8785B&M 1.0GHz ÷ 20/22
SP8786B&M 1.3GHz ÷ 20/22
UHF PROGRAMMABLE DIVIDERS

The SP8785 B & M and SP8786 B & M are high speed programmable ÷20/22 counters which operate at input frequencies up to 1.0GHz and 1.3GHz respectively over the temperature ranges 0°C to +70°C (B grade) and −40°C to +85°C (M grade).

The clock input is biased internally and is coupled to the signal source by a capacitor. The input RF path is completed by two input reference decoupling capacitors which are connected to earth.

The division ratio is controlled by two PE inputs. The counter will divide by 20 when either input is in the high state and by 22 when both inputs are in the low state. These inputs are ECL III/10K compatible and have internal 4.3KΩ pulldown, unused inputs may therefore be left open. When using the device as a ÷20 prescaler the inverse output should be connected to a PE input.

In keeping with the device performance the complementary outputs are ECL 10K compatible.

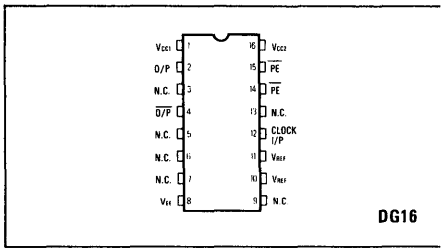


Fig. 1 Pin connections (viewed from above)

FEATURES

- DC to 1.3GHz operation
- 0°C to +70°C operation (B Grade)
- −40 to +85°C operation (M grade)
- Complementary outputs and control inputs are ECL 10K/ECL III compatible.
- AC coupled clock input with wide dynamic range.

QUICK REFERENCE DATA

- Supply voltage $V_{CC} - V_{EE} = 5.2V \pm .25v$
- Power Consumption 440 mW typ (no load)
- ECL compatible
- Maximum input frequency 1GHz (SP8785), 1.3GHz (SP8786)
- Control loop delay time 12 ns typ with 1.3GHz input.

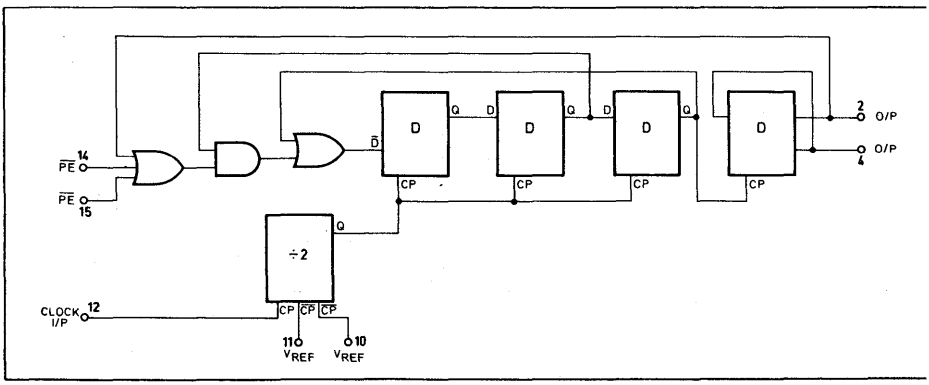


Fig. 2 Logic diagram

CLOCK PULSE	Q_1	Q_2	Q_3	Q_4
2	L	H	H	H
4	L	L	H	H
6	L	L	L	H
8	H	L	L	H
10	H	H	L	H
12	L	H	H	L
14	L	L	H	L
16	L	L	L	L
18	H	L	L	L
20	H	H	L	L
22	H	H	H	H

— PE	— PE	DIV RATIO
L	L	22
H	L	20
L	H	20
H	H	20

The maximum possible loop delay for control is obtained if the L → H transition from Q_4 or the H → L transition from Q_4 is used to clock the stage controlling the ÷20/22. The loop delay is 20 clock periods minus the internal delays of the ÷20/22 circuit.

Table 1 Count sequence and control input truth table

LECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 0°C to +70°C (B Grade)
−40°C to +85°C (M Grade)
Supply voltage V_{CC}=OV
V_{EE}= −5.2V*

tatic characteristics

Characteristic		Value Min.	Typ.	Max.	Units	Conditions
PE input voltage	V_{INH}	−.96		V_{CC}	V	T_{amb}=25°C
	V_{INL}	V_{EE}		−1.62	V	see note 2
PE input pulldown resistor			4.3		KΩ	
Output Voltage levels						
	V_{OH}	−.93		−.78	V	T_{amb}=25°C
	V_{OL}	−1.85		−1.62	V	430Ω from o/p to V_{EE} see note 2
Power supply current			85	115	mA	No load

The SP8785/6 may be operated with a +5.2V supply provided sufficient care is taken with supply decoupling and interfacing of input and utputs.

ynamic characteristics

Characteristic	Value Min.	Typ.	Max.	Units	Conditions
Max. toggle frequency					
SP8786	1300			MHz	See Note 3
SP8785	1000			MHz	
Min. frequency sinewave drive			150	MHz	
Min. slew rate of square wave for correct operation to D.C.			200	V/µS	
Propagation delay clock input to output		2.5		µS	
Set up time		.5		nS	See note 4
Release time		.5		nS	See note 5

OTES:

Correct operation is specified for $V_{CC} - V_{EE}$ = 5.2V ± .25V
The input threshold and output voltage levels have the same temperature coefficients as ECL 111/10K.
The devices are dynamically tested using the circuit shown in Fig. 4 with input amplitudes of 400 and 1000 mVpp over the full tempera-e range.
Set up is defined as the minimum time that can elapse between a L → H transition of control input and the last L → H clock pulse nsition to ensure the ÷20 mode is selected.
Release time is defined as the minimum time that can elapse between a H → L transition of the control input and the last L → H clock lse transition to ensure the ÷22 mode is selected.

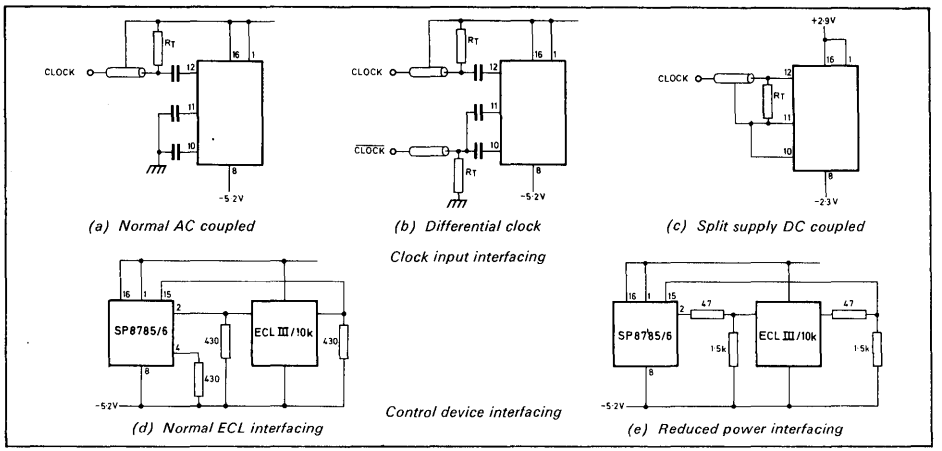


Fig. 3 Interface circuit configurations

OPERATING NOTES

It is recommended that high frequency construction techniques are used with these devices with the positive rail connected to a ground plane. All components used in the circuit layout should be suitable for the frequencies involved.

The clock input to the device is normally capacitively coupled to the signal source as shown in Fig. 3a. The input is self biased by an internal 400Ω resistor to a bias voltage, and in order to complete the input path the two input reference pins must be decoupled to the earth plane with minimum of series inductance. Alternative connections which allow the use of complementary drive or DC coupling for added sensitivity are also shown in Fig. 3.

In the absence of an input signal, circuit will self oscillate with an output frequency of approximately 50MHz. This can be prevented by connecting a 10KΩ resistor between pin 11 and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8785/6 will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The input impedance of the SP8785/6 is a function of frequency and minimises at about the same frequency as the maximum input sensivity, so although it can load the signal source significantly there is generally enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The modulus control inputs have been designed to interface directly to ECL III/ECL10k since on ECL counter such as the 10136 is required to directly control the device at the maximum input clock frequency. If the input frequency is reduced or the modulus extended as shown in the application notes, the device may be controlled by a TTL. or CMOS. counter provided the loop delay requirements are met and suitable interfacing is applied. Unused PE inputs should be left open circuit.

The SP8785/6 have outputs which are compatable with the ECL 10k logic family. The device will drive 100Ω lines and can be used with line impedances down to 50Ω with a small loss in noise immunity.

An equal load on the unused output will reduce waveform distortion.

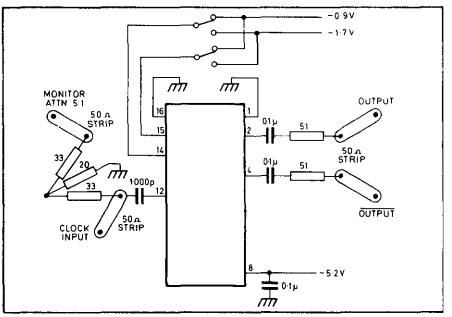


Fig. 4 Dynamic test circuit (all capacitors 1000pF unless stated)

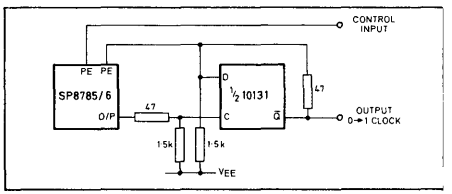


Fig. 5 ÷ 40/42 control loop delay time 24ns typ.

APPLICATION NOTES

The SP8785/6 when used in a system operating at 1.3GHz may be controlled by a variable divider to give effective variable division at half the input frequency. The variable divider must produce a control signal within the period of the output of the SP8785/6 minus the delays within this device. The control loop delay time is typically 12 nsec.

Two methods may be used to achieve a satisfactory delay time within the control divider–

1. An extra divider may be inserted to increase the division ratio of the two modulus from 20/22 to 40/42, 80/82 or 100/102, hence reducing the control divider frequency and increasing the control loop delay time.
2. An ECL variable counter may be used to produce the control command. A device which is suitable is the 10136, in the ECL10k range.

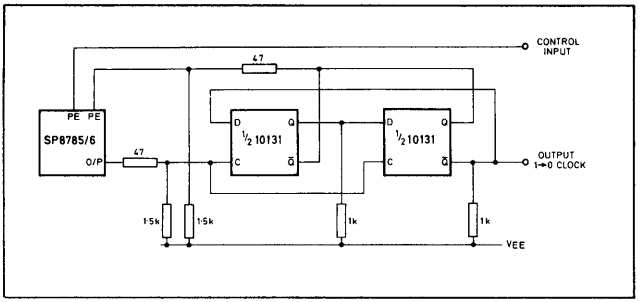


Fig. 6 ÷ 80/81 control loop delay time 55ns typ.

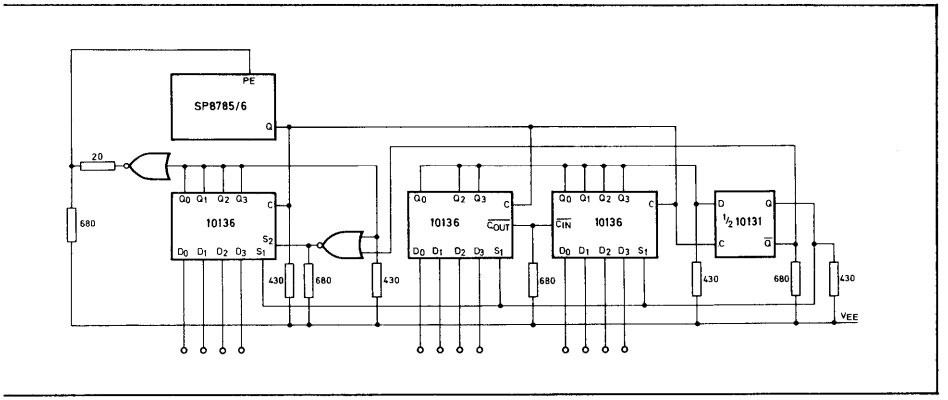


Fig. 7 1.3 GHz variable divider (200—2000 in steps of 2)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	V_{EE} to V_{CC}
Input voltage	2V peak to peak
Output current	40mA
Operating function temperature	+150°C
Storage temperature	−55°C to +150°C

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES

HIGH SPEED DIVIDERS

SP8790 A & B

÷4 EXTENDER FOR 2-MODULUS COUNTERS

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide-by-10 or 11 with the SP8790 becomes a divide-by-40 or 41, a divide by 5 or 6 becomes a divide by 20 or 21.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8790 into the region where CMOS or low power TTL can control the divider. The power-saving advantages are obvious.

The device interfaces easily to the SP8690 range of divide by 10 or 11s. The control inputs are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8790 is available in three temperature grades: 0°C to +70°C (SP8790B) −55°C to+125°C (SP8790A)

The SP8790 requires supplies of OV and +5V ±0.25V.

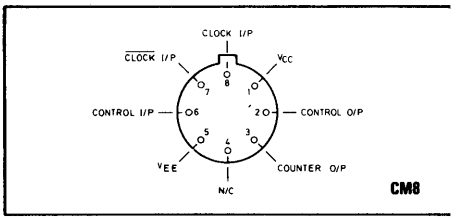


Fig. 1 Pin connections

FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- I/P and O/P Interface Direct to CMOS/TTL

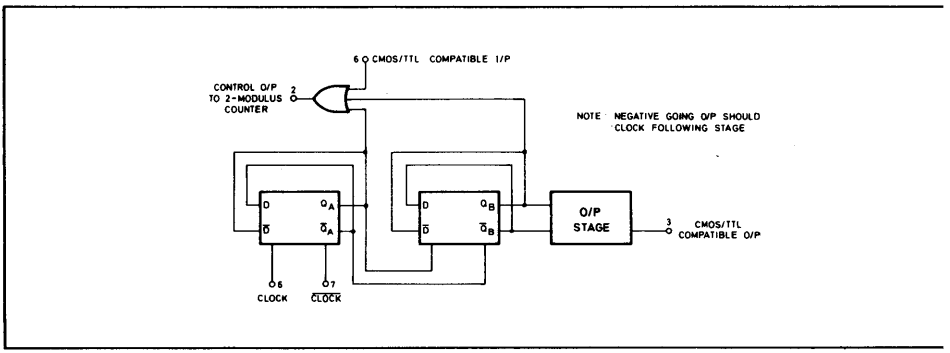


Fig. 2 Logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | VCC—VEE|	8V
DC input voltage	Not greater than supply
AC input voltage	2.5Vp-p
Output bias voltage	12V
Control input bias voltage	12V
Operating junction temperature	+150°C
Storage temp. range	−55°C to 150°C

LECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: −55°C to +125°C (A grade)
0°C to +70°C (B grade)
V_{CC} = −5V ± 5%
V_{EE} = 0V
Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Dynamic					
Toggle frequency	See note 1			MHz	
Min toggle frequency with sine-wave input			20	MHz	See note 2
Min toggle frequency with square wave input	0			Hz	Slew rate 50V/μs
Clock to O/P delay (O/P − ve going)		14		ns	
Clock to O/P delay (O/P + ve going)		28		ns	
Control I/P to control O/P delay (O/P−ve going)		20		ns	10kΩ pulldown on control O/P (See note 5)
Clock I/P to control O/P delay (O/P+ve going)		10		ns	10kΩ pulldown on control O/P (See note 5)
Control I/P to control O/P delay (O/P−ve going)		12		ns	4.3kΩ pulldown on control O/P (See note 6)
Control I/P to control O/P delay (O/P+ve going)		9		ns	4.3kΩ pulldown on control O/P (See note 6)
Clock to control O/P delay (O/P −ve going)		26		ns	10kΩ pulldown on control O/P (See note 5)
Clock to control O/P delay (O/P −ve going)		12		ns	10kΩ pulldown on control O/P (See note 5)
Clock to control O/P delay (O/P−ve going)		17		ns	4.3kΩ pulldown on control O/P (See note 6)
Clock to control O/P delay (O/P−ve going)		12		ns	4.3kΩ pulldown on control O/P (See note 6)
Static					
Control I/P voltage level					
High state	3.5		10	V	See note 3
Low state	0		1.5	V	
Output voltage level					
V_{OL}			0.4	V	Sink current = 6.0mA
V_{OH} (See note 4)					
Input impedance		1.6		kΩ	f_{in} = 0Hz
Input vias voltage (CLOCK and $\overline{CLOCK}$)		2.4		V	Inputs open circuit
Power supply drain current		8.0	11	mA	

NOTES

1. The maximum frequency of operation is in excess of 60MHz when the SP8790 is used as a prescaler. The limitation on this maximum frequency is the saturating O/P stage. When the SP8790 is used as a controller its internal delays do not permit operation at frequencies in excess of 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. V_{OH} will be the supply voltage that the output pull-up resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695 with which the SP8790 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of the SP8640 series SP8745 and SP8746 with which the SP8790 can be used.

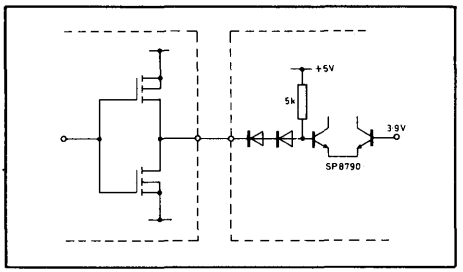


Fig. 3 CMOS and TTL compatible control input

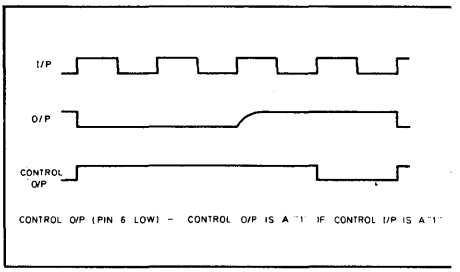


Fig. 4 SP8790 waveforms

OPERATING NOTES

The SP8790 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷40/41 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present. This may be prevented by using one of the arrangements shown in Fig. 6.

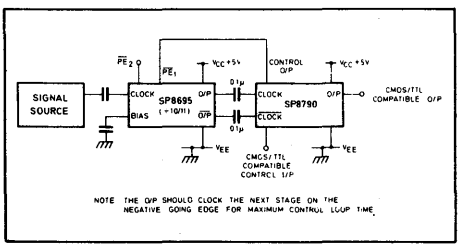


Fig. 5 SP8790 with SP8695 connected to give a ÷40/4

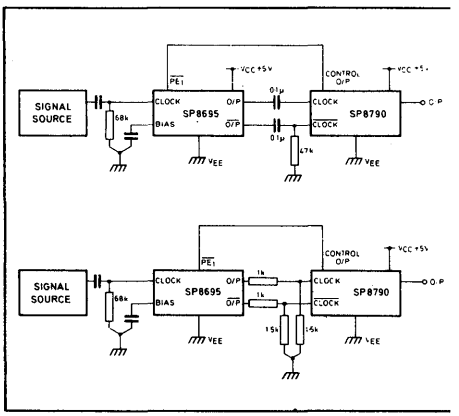


Fig. 6 Methods of preventing self-oscillation

TRUTH TABLE	
Control Input	**Div. Ratio With ÷10/11**
0	41
1	40

Max input frequency to combination=200MHz (min.).
Power consumption of combination=120mWtyp.
Time available to control the ÷40/41=(40 clock periods minus delays through the dividers) — 340ns (f_{in}=100MHz).

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8792 ÷ 80/81
200 MHz LOW POWER TWO MODULUS PRESCALER
SP8793 ÷ 40/41
200 MHz LOW POWER TWO MODULUS PRESCALER

GENERAL DESCRIPTION

The SP8792/3 A&B are divider circuits that can be logically programmed to divide by either 40/41 or 80/81.

The devices are available over two temperature ranges, "A" variant is -55°C to +125°C and the "B" variant is 0°C to +70°C.

The clock inputs can be either single or differentially driven and must be a.c. coupled to the signal source. If single driven, then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present. To prevent this a 68K resistor should be connected from pins 5 or 6 to 0V. This will reduce the sensitivity of the device by approximately 100MV peak to peak.

The division ratio is controlled by the control input which is CMOS compatible throughout the temperature range. The device will divide by 40 or 80 when the input is high and by 41 or 81 when the input is low. The input may be interfaced directly with CMOS. There is a free collector saturating output stage for interfacing with either TTL or CMOS. When using TTL, V_{CC2} must be connected to 5V. For use with CMOS, V_{CC2} should not be connected and the external pullup resistor (10K) to the CMOS supply is required.

The devices may be used as a fixed ÷ 40 or 80 by connecting O/P to control input.

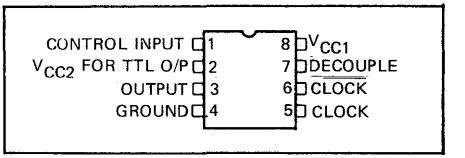


Fig. 1 — Pin connections

FEATURES

- Full temperature range operation
  - "A" variant -55°C to +125°C
  - "B" variant 0°C to +70°C
- Toggle frequency > 250 MHz typical
- Power dissipation 70mW typical
- Capacitively coupled clock input for synthesiser and counter applications
- ECL compatibility on the programming inputs
- True and inverse outputs availalbe with CMOS compatibility

QUICK REFERENCE DATA

- Supply voltage 6.8V to 9.5V
- Supply current 5mA typ., 7mA max.

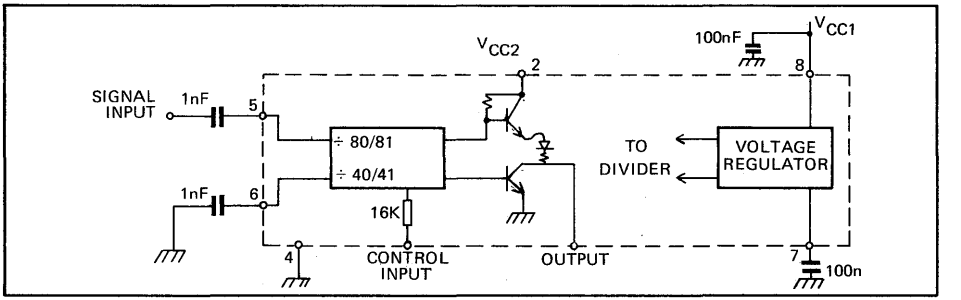


Fig. 2 — Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} : 6.8V to 9.5V
Input signal amplitude: 200mV to 800mV pk-pk
Ambient temperature: -30°C to +70°C

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Supply current		5	7	mA	Pin 2 open circuit
Max. input frequency	200			MHz	
Min. input frequency			20	MHz	400mV pk-pk sine wave input
Min. slew rate with square wave input)			50	V/μS	
Output voltage level (low)			0.5	V	2mA current, Pin 2 open or linked to pin 8.
Output voltage level (high)	4.8			V	V_{CC} = 6.8V, Pins 2, 8 linked
Control input level (low)			2.0	V	÷ 41 or ÷ 81
Control input level (high)	4.0			V	÷ 40 or ÷ 80
Propagation Delay, clock input to output		40		nS	Output 1 to 0 transition
Set up time		4		nS	See note 1.
Release time		4		nS	See note 2.

NOTES:

1. The minimum time between a L → H signal input transition to ensure the ÷ 40 or ÷ 80 mode is selected.
2. The minimum time between a H → L transition of control input and the last L → H signal input transition to ensure the ÷ 41 or ÷ 81 mode is selected.

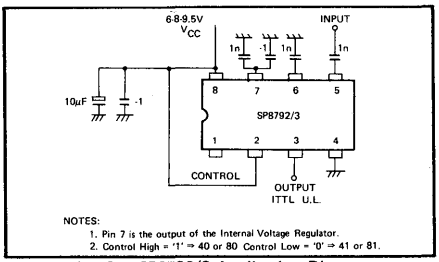


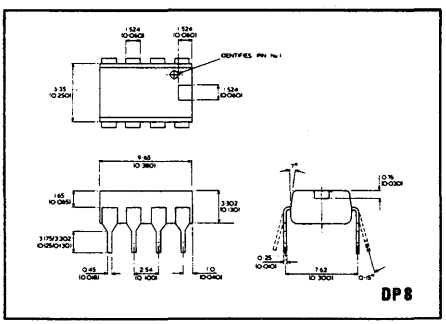
Fig. 3 – SP8792/3 Application Diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage (pins 2, 3 and 8): 12V
Storage temperature : -55°C to +125°C
Operating temperature : -30°C to +70°C

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



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1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES

HIGH SPEED DIVIDERS

SP 8794 A & B

÷ 8 CONTROL CIRCUIT FOR 2 - MODULUS DIVIDERS

The SP8794 is a divide by eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide by 10 or 11 with the SP8794 becomes a divide by 80 or 81, a divide by 5 or 6 becomes a divide by 40 or 41.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8794 into the region where CMOS or low power TTL can control the divider.

The device interfaces easily to the SP8000 range of 2-modulus dividers. The control I/Ps are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8794 is available over three temperature ranges: 0°C to +70°C (SP8794B), −40°C to +85°C (SP8794M) and −55°C to +125°C (SP8794A).

The SP8794 requires supplies of 0V and +5V ± 0.25V

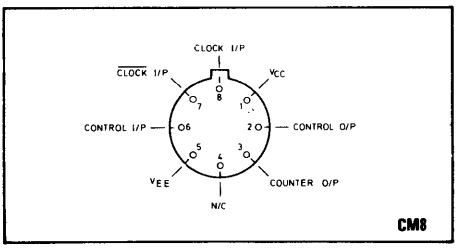

Fig. 1 Pin connections.

FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- Direct I/P & O/P Interfacing to CMOS & TTL
- Operates with 500MHz ÷ 10/11

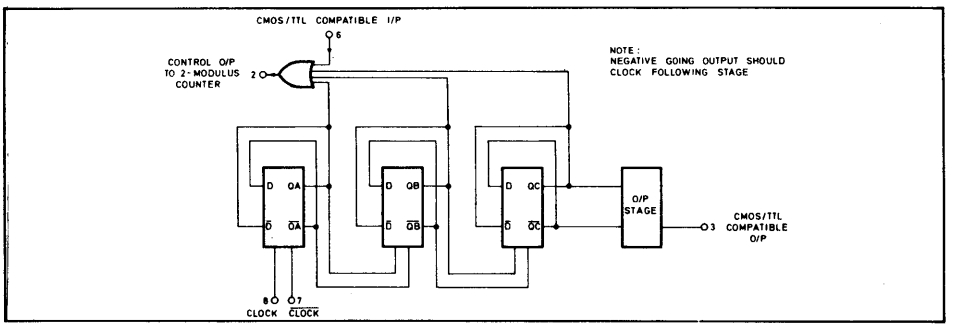

Fig. 2 Logic diagram.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
DC input voltage	Not greater than supply
AC input voltage	2.5Vp-p
Output bias voltage	12V
Control input bias voltage	12V
Operating junction temperature	+150°C
Storage temp. range	−55°C to 150°C

APPLICATION

- Frequency Synthesisers

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
V_{CC} = +5V ±5%
V_{EE} = 0V
Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Dynamic					
Toggle frequency	120			MHz	SP8794 as a prescaler (see note 1)
	40			MHz	SP8794 controlling a 2-modulus divider (see note 1)
Min. toggle frequency with sinewave input			20	MHz	See note 2
Min. toggle frequency with square wave input	0			Hz	Slew rate > 50V/μs
Clock to O/P delay (O/P −ve going)		18		ns	
Clock to O/P delay (O/P +ve going)		32		ns	
Control I/P to control O/P delay (O/P −ve going)		20		ns	10kΩ pulldown on O/P, see note 5
Control I/P to control O/P delay (O/P +ve going)		10		ns	10kΩ pulldown on O/P, see note 5
Control I/P to control O/P delay (O/P −ve going)		12		ns	4.3kΩ pulldown on O/P, see note 6
Control I/P to control O/P delay (O/P +ve going)		9		ns	4.3kΩ pulldown on O/P, see note 6
Clock to control O/P delay (O/P −ve going)		30		ns	10kΩ pulldown on O/P, see note 5
Clock to control O/P delay (O/P +ve going)		16		ns	10kΩ pulldown on O/P, see note 5
Clock to control O/P delay (O/P −ve going)		21		ns	4.3kΩ pulldown on O/P, see note 6
Clock to control O/P delay (O/P +ve going)		16		ns	4.3kΩ pulldown on O/P, see note 6
Static					
Control I/P voltage level					
High state	3.5		10	V	See note 3
Low state	0		1.5	V	
Output voltage level					
V_{OL}			0.4	V	Sink current = 6.0mA
V_{OH} (see note 4)			12	V	See note 4
Input impedance		1.6		kΩ	f_{in} = 0Hz
I/P bias voltage (CLOCK & $\overline{CLOCK}$)					
Power supply drain current					

NOTES
1. The maximum frequency of operation is in excess of 120MHz when the SP8794 is used as a prescaler. The limitation on its maximum operating frequency is the saturating output stage. When the SP8794 is used as a controller for a 2-modulus device its internal delays do not permit operation at frequencies above 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. V_{OH} will be the supply voltage that the output pull-out resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695, with which the SP8794 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of all the SP8640 series ÷ 10/11 devices, the SP8740 & SP8745 ÷ 6/6, the SP8741 & SP8746 ÷ 6/7 and the SP8743 ÷ 8/9, with which the SP8794 can be used.

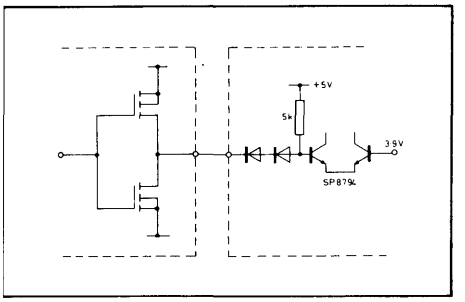

Fig. 3 CMOS and TTL compatible control I/P.

TRUTH TABLE	
Control I/P	**Div. Ratio with ÷ 10/11**
0	81
1	80

Max input frequency to combination = 200MHz (min.).
Power consumption of combination = 120mWtyp.
Time available to control the ÷ 80/81
= 80 clock periods minus delays through dividers
≅ 740ns (f_{in} = 100MHz)

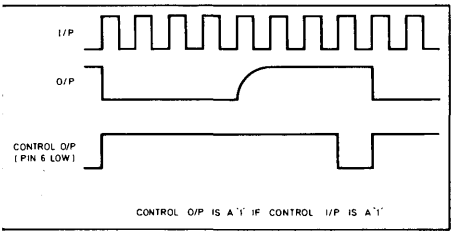

Fig. 4 SP8794 waveforms

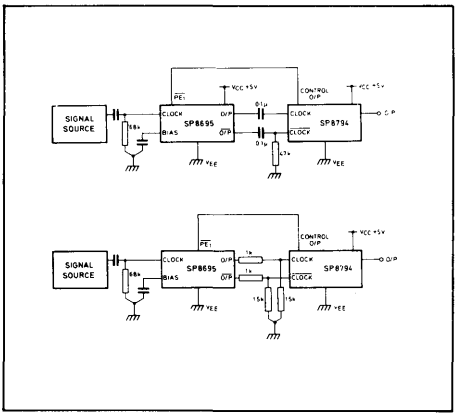

Fig. 6 Methods of preventing self-oscillation.

APPLICATION NOTES

The SP8794 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷ 80/81 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present, This may be prevented by using one of the arrangements shown in Fig. 6.

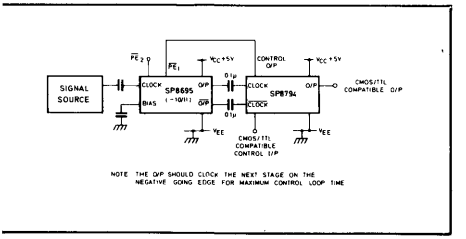

Fig. 5 SP8794 with SP8695 connected to give a low power ÷ 80/81

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

SP8000 SERIES
HIGH SPEED DIVIDER

SP8901
1GHz ÷ 512

The SP8901 is a four modulus ÷512 operating at frequencies up to 1GHz. The device has a typical power dissipation of 500mW, and operates over the temperature range -30°C to 70°C. The SP8901 has been designed to interface with the NJ8911 and NJ8916 to produce a 16 bit binary programmed frequency synthesiser but can also be interfaced with standard programmable divider to produce a wide range of general purpose synthesisers.

FEATURES
- Self Biasing Clock Inputs
- Current Limited TTL/MOS Compatible Inputs
- TTL/MOS Compatible Control Inputs
- 5V Supply
- Variable Input Hysterisis Capability For Wide Band Operation

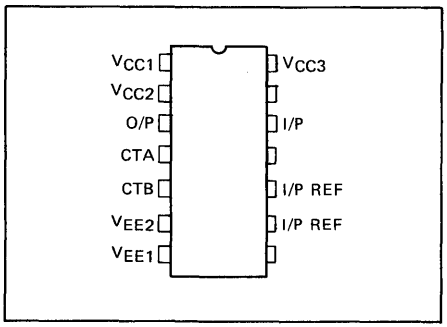

Fig. 1 – Pin Configuration

APPLICATIONS
- Mobile Radio
- Scanning Radio Receivers
- Microprocessor Controlled Frequency Synthesis

ABSOLUTE MAXIMUM RATINGS

Power Supply voltage ($V_{CC} - V_{EE}$)	8V
Input voltage, Clock inputs	2.5V peak to peak
Control inputs	-0.5V to 8V
Operating Junction temperature	+150°C
Storage temperature	-55°C to 150°C

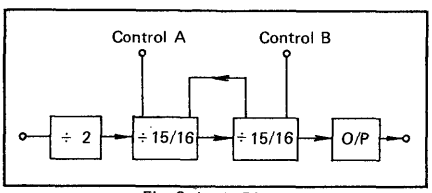

Fig. 2–Logic Diagram

Control A	Control B	Ratio
1	1	512
0	1	510
1	0	480
0	0	478

Fig. 3 – Table of Divide Ratios

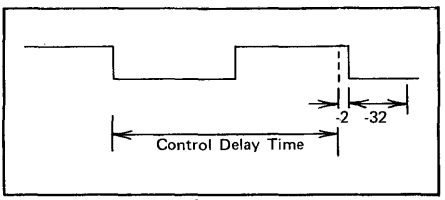

Fig. 4

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Supply Voltage: V_{CC} +5.0V±0.25V V_{EE}: OV

T_{amb}: -30°C to +70°C

Clock Input: 400mV to 1.0V peak to peak

DYNAMIC CHARACTERISTICS

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Max. Input frequency	900			MHz	V_{CC3} = 5V See Fig. 5.
Max. Input frequency	1.0			GHz	V_{HS} = +12v R_3 = 120Ω See Fig. 5.
Min. Input frequency with sine wave input			100	MHz	600mV p-p
Min. slew rate of square wave input			200	V/μS	
Clock to output delay		40	60	nsec	
Control setup and release time:					
Control A Input		2		nsec	
Control B Input		5		nsec	

OPERATING NOTES –

The circuit is configured as two ÷15/16 counters which are clocked via a front end ÷2 counter as shown in figure 2. The circuit will divide by 512 when the control inputs are left open circuit or both inputs are at logic '1'. The control A and B pins control the minus 2 and 32 counters respectively, when a logic '0' signal is applied. Figure 3 shows the division ratio table. The minus 2 counts of the control A occur before the negative going output edge, whereas the minus 32 counts occur after the negative going edge as shown in figure 4. The maximum possible control delay is obtained by clocking the control device on the negative going edge of the SP8901, and is equal to 480 clock input periods (minus the internal delays in the SP8901).

The clock input should be correctly terminated and all input coupling and decoupling capacitors should be of a type suitable for operation at 1GHz. At low frequencies the divider is limited by the slew rate of the input signal and for correct operation this must be greater than 200V/μs. The low frequency sinewave operation of the device can be improved by adding hysterisis to the reference inputs. This can be carried out externally as shown in figure 5 and can be measured as Vref1 – Vref2. Care must be taken when applying hysterisis as large values of hysterisis will degrade the input sensitivity at maximum frequency. A maximum value of 50mV (R1 = 32KΩ) should not be exceeded.

The output is TTL or MOS compatable and is current limited at 3 mA sink in the low state and 5ma source in the high state. The modulus control inputs have a 5kΩ pull up resistor and can be interfaced to open collector or open drain circuits. There are separate supply lines for the output (V_{CC2}, V_{EE2}) to reduce both input to output and output to input coupling.

A separate supply pin (V_{CC3}) is available for the front end ÷2, and determines the maximum frequency of the device. With V_{CC3} connected to the 5v supply the circuit will operate up to 900MHz. The high frequency limit may be increased to 1GHz by connecting V_{CC3} via a resistor to a supply greater than 10v as shown in Fig. 6. The resistor value is given by: $R_3 = [(V_{HS}\ (MIN) - 7)/25.] K\Omega$.

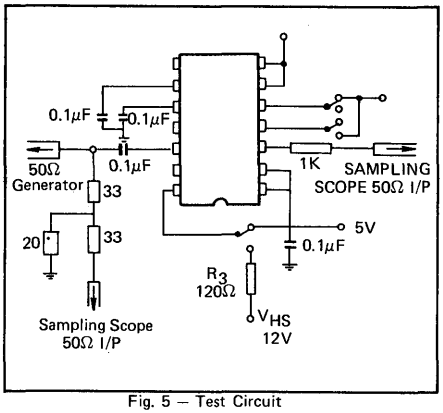

Fig. 5 – Test Circuit

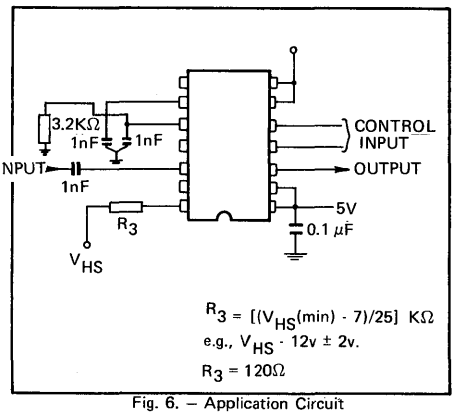

Fig. 6. – Application Circuit

STATIC CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Logic '1' Output Voltage	3.5			V	
	2.5			V	1ma source
Output short circuit current			10	mA	
Logic '0' output voltage			0.5	V	2mA sink
Supply Current		100	135	mA	
Control inputs:					
Min. Input high level			2.3	V	
Max. input low level	1.3V			V	
Low level input current		0.8	1.2	mA	Vin = 0.5V

NOTE 1:

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table "Electrical Characteristics" provides conditions for actual device operation.

NOTE 2:

Unless otherwise stated, tests are carried out at T_{amb} = +25°C.

NOTE 3:

All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

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1641 Kaiser Avenue,
Irvine, CA. 92714

SP8000 SERIES
HIGH SPEED DIVDERS

SP8906
500 MHz ÷ 256

The SP8906 is a four modulus ÷256 operating at frequencies up to 500MHz. The device has a typical power dissipation of 400mW, and operates over the temperature range -30°C to 70°C. The SP8906 has been designed to interface with the NJ8911 and NJ8916 to produce a 16 bit binary programmed frequency synthesiser, but can also be interfaced with standard programmable dividers to produce a wide range of general purpose synthesisers.

FEATURES

- Self Biasing Clock Inputs
- Current Limited TTL/MOS Compatible Inputs
- TTL/MOS Compatible Control Inputs
- 5V Supply

APPLICATIONS

- Mobile Radio
- Scanning Radio Receivers
- Microprocessor Controlled Frequency Synthesis

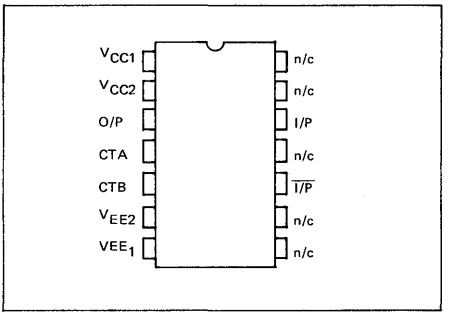


Fig. 1 Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Power Supply voltage ($V_{CC} - V_{EE}$)	8V
Input voltage, Clock inputs	2.5V peak to peak
Control inputs	-0.5V to 8V
Operating Junction temperature	+150°C
Storage temperature	-55°C to 150°C

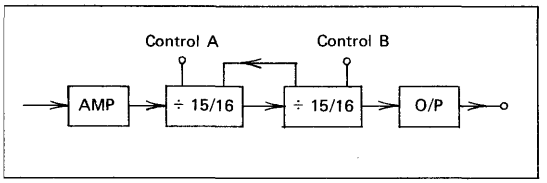


Fig. 2 Logic Diagram

Control A	Control B	Ratio
1	1	256
0	1	255
1	0	240
0	0	239

Fig. 3. Table of Divide Ratios

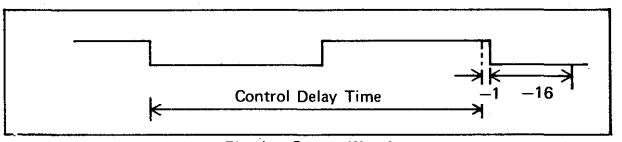


Fig. 4. Output Waveform

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise

Supply Voltage: V_{CC} + 5.0V ±0.25V V_{EE}: OV
T_{amb}: -30°C to +70°C
Clock Input: 400mV to 1.0V peak to peak

STATIC CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Logic '1' Output Voltage	3.5 2.5			V V	 1 mA source
Output short circuit current			10	mA	
Logic '0' output voltage			0.5	V	2mA sink
Supply Current		75	100	mA	
Control inputs: Min. Input high level			2.3	V	
Max. Input low level	1.3v			V	
Low level input current		0.8	1.2	mA	Vin=0.5V

NOTE 1:

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table "Electrical Characteristics" provides conditions for actual device operation.

NOTE 2:

Unless otherwise stated, tests are carried out at T_{amb} = +25°C.

NOTE 3:

All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

DYNAMIC CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Max. input frequency	500			MHz	V_{CC} =5V See Fig. 5
Min. Input frequency with sine wave input		10	20	MHz	600mV p-p
Min. slew rate of square wave input			50	$V/\mu S$	
Clock to output delay		40	60	nsec	
Control setup and release time:					
Control A Input		2		nsec	
Control B Input		5		nsec	

)PERATING NOTES

The circuit is configured as two ÷15/16 counters /hich are clocked via a front end amplifier as shown in igure 2. The circuit will divide by 256 when the control ıputs are left open circuit or both inputs are at logic '1'. he control A and B pins control the minus 1 and 16 ounters respectively, when a logic '0' signal is applied igure 3 shows the division ratio table. The minus 1 ounts of the control A occur before the negative going utput edge, whereas the minus 16 counts occur after the ɜgative going edge as shown in figure 4. The maximum ɔssible control delay is obtained by clocking the control ɜvice on the negative going edge of the SP8906, and is ɟual to 240 clock input periods (minus the internal ɜlays in the SP8906).
n the negative going edge of the SP8906, and is equal to 40 clock input periods (minus the internal delays in the P8906).

The clock input should be correctly terminated and all input coupling and decoupling capacitors should be of a type suitable for operation at 500MHz. At low frequencies the divider is limited by the slew rate of the input signal and for correct operation this must be greater than 50 $V/_{\mu s}$. If the input to the device is likely to be interrupted the device will tend to self oscillate at an output frequency of 2MHz. This can be prevented by the addition of R_1 = 120KΩ but will cause a loss of input sensitivity. (See Figure 6.)

The output is TTL or MOS compatable and is current limited at 3mo sink in the low state and 5ma source in the high state. The modulus control inputs have a 5kΩ pull up resistor and can interface to open collector, open drain circuits or standard TTL outputs. There are separate supply lines for the output (V_{CC2}, V_{EE2}) to reduce both input to output and output to input coupling.

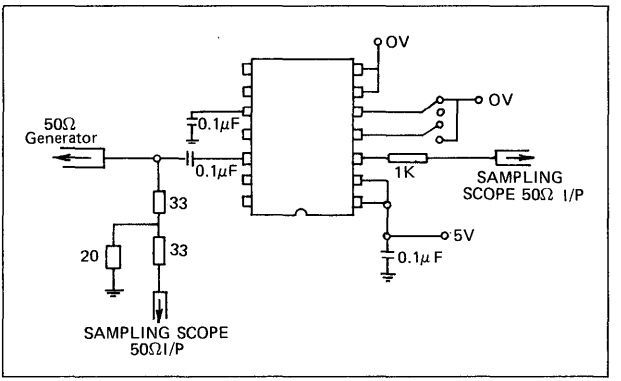


Fig. 5 – Test Circuit

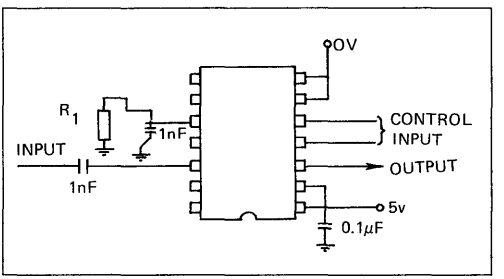


Fig. 6. Application Circuit

PROVISIONAL DATA

40 – CHANNEL CITIZENS' BAND SYNTHESISER IC SETS

SP8922 SP8921 SP8923

BINARY BCD

Recognising the different requirements of citizens' band transceiver manufacturers, Plessey Semiconductors have developed a range of integrated circuits for 40-channel CB. This datasheet describes three of these: SP8921, SP8922 and SP8923.

The devices are designed for use in pairs. SP8922 and SP8921 incorporate all the functions for a synthesised local oscillator with binary-coded channel entry; the SP8923/21 pair offering similar facilities but with BCD channel entry.

FEATURES

- Low External Component Count
- Binary (SP8922) or BCD (SP8923) Channel Setting
- Internal Pulldowns on Channel I/Ps
- Integral 10.24MHz Crystal Oscillator with Buffered O/P
- 10.695MHz IF Offset for Double Conversion
- 455 kHz IF offset for Single Conversion
- No Mixing or Prescaling Required between VCO and Synthesiser I/P
- Digital Phase/Frequency Comparator has Source and Sink O/Ps
- Lock Detect O/P
- 5V Supply Rail
- Low Power: 225mW Typ. (SP8921)
  225mW Typ. (SP8922)
  325mW Typ. (SP8923)

The synthesisers are partitioned into two parts as shown in Figs. 2 and 3. The SP8922 and SP8923 contain a preamplifier followed by a fixed divide by four prescaler. The amplifier input will accept a signal at a frequency up to 30MHz. The input is a high impedance and requires an AC coupled source which is achieved by a series capacitor. The prescaler is followed by seven bits of programmable division. In the SP8922, these seven bits are programmed from the six binary inputs, as shown in Table 1, plus the 5kHz program input.

The SP8923 is programmed by seven BCD channel inputs (see Table 2), the 40 input codes being converted by a decoding matrix to the appropriate citizens' band frequencies.

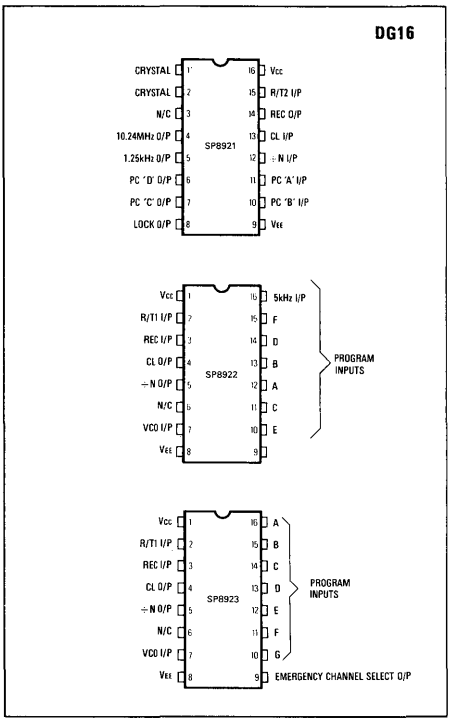


Fig. 1 Pin connections (top view)

A receive/transmit (R/T) input is provided on both SP8922 and SP8923 to give an offset of 91 counts (corresponding to −455kHz) when the receive mode is selected.

Clock and preset outputs to the SP8921 are provided by SP8922 and SP8923, which in turn accept a recognition signal from the SP8921.

Pin 9 on the SP8923 is an Emergency Channel Select output, which gives a low output whenever channel 9,

or a non-permitted channel, is selected. When this output is low, the synthesiser programs to channel 9.

The device common to both sets, SP8921, contains the six most significant bits of the programmable counter, a 10.24MHz crystal oscillator maintaining circuit, a 2^{13} fixed divider, and a digital phase/frequency comparator. The six bits of the programmable counter have a fixed preset code which, combined with the variable code of the SP8922 or SP8923, give the total count required to select the 40 citizens' band frequencies. The R/T input to the SP8921 gives an offset in the programmable count of minus 2048 (corresponding to −10.24 MHz) when in the receive mode.

The crystal oscillator has a direct emitter follower output which may be used as an input to the second mixer in a double conversion transceiver as shown in Fig. 4. The oscillator is connected internally to the fixed divider, which gives an output reference frequency of 1.25kHz with a 10.24MHz crystal. The phase/frequency comparator has two outputs which may be used to drive a variety of charge pump filter circuits as shown in Figs. 7 through10.There is also a 'lock detect' output which requires an external filter as shown in Figs. 2 and 3.

The frequencies available from the SP8922/1 and SP8923/1 when connected in a synthesiser loop are shown in Tables 1 and 2 respectively.

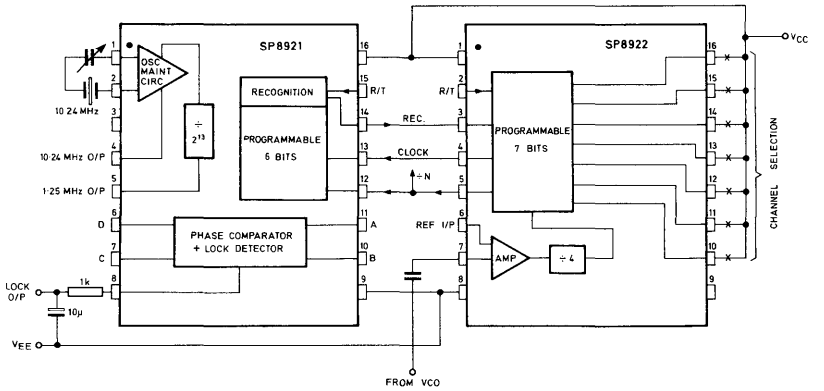


Fig. 2 SP8921/SP8922 interconnections (10.695MHz receive offset)

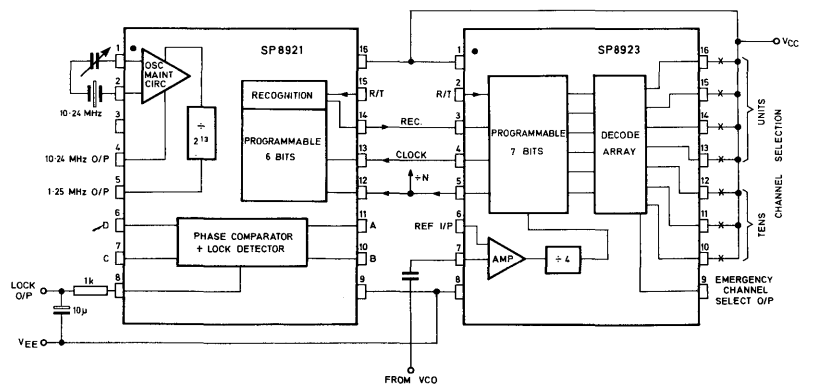


Fig. 3 SP8921/SP8923 interconnections (10.695MHz receive offset)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
V_{EE} = 0V, V_{CC} = +4.75V to +5.5V
T_A = −30°C to +70°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Inputs (see Note 1)					
Low	0		0.5	V	
High	2.4		Vcc	V	
VCO	0.4		1.0	Vp-p	AC-coupled
Max. clock frequency	30	50		MHz	
Outputs (except 10.24MHz O/P and phase comparator C and D O/Ps)					
Low			0.5	V	6mA sink
High	Vcc−0.5			V	No load, see Note 2
10.24MHz O/P	600	800		mVp-p	
Phase comp. C O/P					
Leakage O/P high			50	µA	
O/P low			0.5	V	5mA sink
Phase comp. D O/P					
Leakage O/P low			50	µA	
O/P high	Vcc−1.2			V	5mA source
Power supply					
Vcc	+4.75		+5.5	V	
Icc SP8921		45	60	mA	
SP8922		45	60	mA	
SP8923		65	90	mA	

NOTES
1. Programming inputs may be left open circuit as input low, or connected Vcc as input high. All inputs (except VCO I/P) have internal 10k Ω pull down resistors to V_{EE}. SP8922, SP8923 pin 6 is the VCO I/P reference; this pin may be left open circuit, or decoupled to V_{EE} to improve I/P sensitivity.
2. Outputs have an internal 5k Ω pull up resistor to Vcc. Lock output (SP8921 pin 8) has an internal 10k Ω pull up resistor to Vcc.

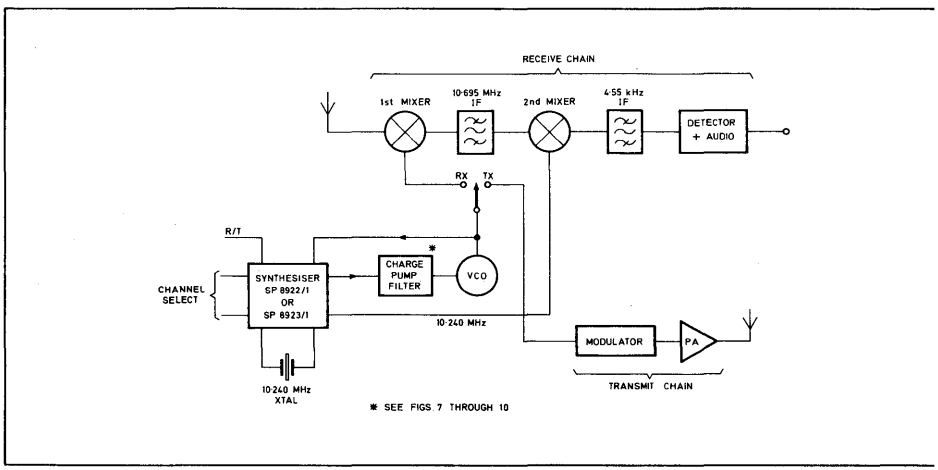


Fig. 4 Double conversion transceiver

Channel No.	Input Code F E D C B A	Output frequency with R/T = 0 (MHz)
1	0 0 0 1 1 1	26.965
2	0 0 1 0 0 0	26.975
3	0 0 1 0 0 1	26.985
4	0 0 1 0 1 1	27.005
5	0 0 1 1 0 0	27.015
6	0 0 1 1 0 1	27.025
7	0 0 1 1 1 0	27.035
8	0 1 0 0 0 0	27.055
9	0 1 0 0 0 1	27.065
10	0 1 0 0 1 0	27.075
11	0 1 0 0 1 1	27.085
12	0 1 0 1 0 1	27.105
13	0 1 0 1 1 0	27.115
14	0 1 0 1 1 1	27.125
15	0 1 1 0 0 0	27.135
16	0 1 1 0 1 0	27.155
17	0 1 1 0 1 1	27.165
18	0 1 1 1 0 0	27.175
19	0 1 1 1 0 1	27.185
20	0 1 1 1 1 1	27.205
21	1 0 0 0 0 0	27.215
22	1 0 0 0 0 1	27.225
23	1 0 0 1 0 0	27.255
24	1 0 0 0 1 0	27.235
25	1 0 0 0 1 1	27.245
26	1 0 0 1 0 1	27.265
27	1 0 0 1 1 0	27.275
28	1 0 0 1 1 1	27.285
29	1 0 1 0 0 0	27.295
30	1 0 1 0 0 1	27.305
31	1 0 1 0 1 0	27.315
32	1 0 1 0 1 1	27.325
33	1 0 1 1 0 0	27.335
34	1 0 1 1 0 1	27.345
35	1 0 1 1 1 0	27.355
36	1 0 1 1 1 1	27.365
37	1 1 0 0 0 0	27.375
38	1 1 0 0 0 1	27.385
39	1 1 0 0 1 0	27.395
40	1 1 0 0 1 1	27.405

ıble 1 SP8922/1 O/P frequencies with 10.240 crystal (0 = ıntact open, 1 = contact closed to Vcc)

Channel No.	Input Code G F E D C B A	Output Frequency with R/T = 0 (MHz)
1	0 0 0 0 0 0 1	26.965
2	0 0 0 0 0 1 0	26.975
3	0 0 0 0 0 1 1	26.985
4	0 0 0 0 1 0 0	27.005
5	0 0 0 0 1 0 1	27.015
6	0 0 0 0 1 1 0	27.025
7	0 0 0 0 1 1 1	27.035
8	0 0 0 1 0 0 0	27.055
9	0 0 0 1 0 0 1	27.065
10	0 0 1 0 0 0 0	27.075
11	0 0 1 0 0 0 1	27.085
12	0 0 1 0 0 1 0	27.105
13	0 0 1 0 0 1 1	27.115
14	0 0 1 0 1 0 0	27.125
15	0 0 1 0 1 0 1	27.135
16	0 0 1 0 1 1 0	27.155
17	0 0 1 0 1 1 1	27.165
18	0 0 1 1 0 0 0	27.175
19	0 0 1 1 0 0 1	27.185
20	0 1 0 0 0 0 0	27.205
21	0 1 0 0 0 0 1	27.215
22	0 1 0 0 0 1 0	27.225
23	0 1 0 0 0 1 1	27.255
24	0 1 0 0 1 0 0	27.235
25	0 1 0 0 1 0 1	27.245
26	0 1 0 0 1 1 0	27.265
27	0 1 0 0 1 1 1	27.275
28	0 1 0 1 0 0 0	27.285
29	0 1 0 1 0 0 1	27.295
30	0 1 1 0 0 0 0	27.305
31	0 1 1 0 0 0 1	27.315
32	0 1 1 0 0 1 0	27.325
33	0 1 1 0 0 1 1	27.335
34	0 1 1 0 1 0 0	27.345
35	0 1 1 0 1 0 1	27.355
36	0 1 1 0 1 1 0	27.365
37	0 1 1 0 1 1 1	27.375
38	0 1 1 1 0 0 0	27.385
39	0 1 1 1 0 0 1	27.395
40	1 0 0 0 0 0 0	27.405

Table 2 SP8923/1 O/P frequencies with 10.240 crystal (0 = contact open, 1 = contact closed to Vcc)

R/T 1	R/T 2	Offset
0	0	0
1	0	–455kHz
0	1	–10.240MHz
1	1	–10.695MHz

Table 3 Receive/Transmit truth table

SP8921 CRYSTAL OSCILLATOR PERFORMANCE

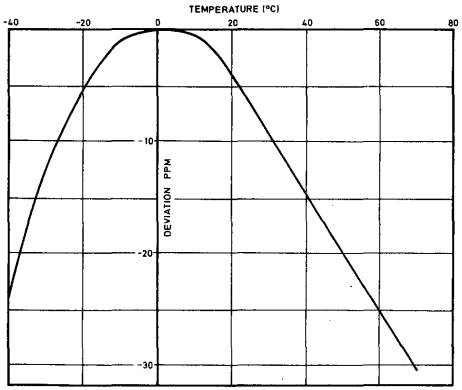


Fig. 5 Frequency/temperature characteristics of CB 10.24 MHz crystal oscillator

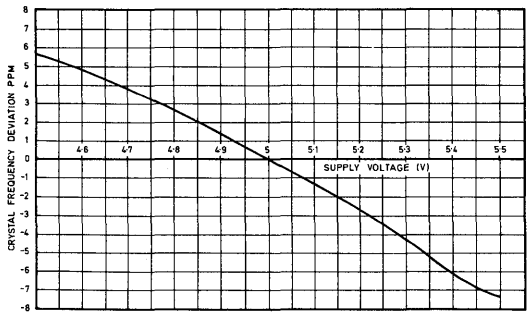


Fig. 6 Crystal frequency v. supply voltage

CHARGE PUMP FILTER ARRANGEMENTS (FIGS.7 THROUGH 10)

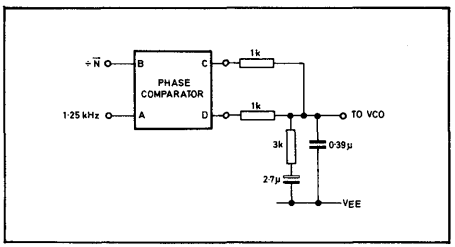


Fig. 7 Filter A. Simple voltage pump, output range 2.5V

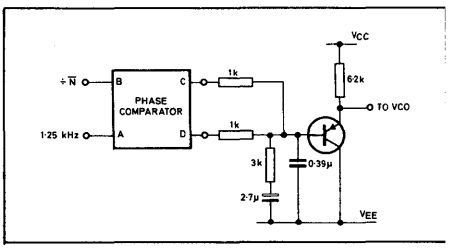


Fig. 8 Filter B. Simple voltage pump with buffered output

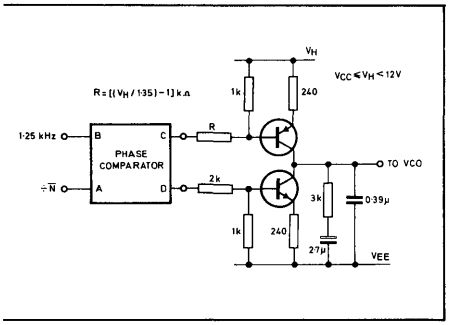


Fig. 9 Filter C. Current pump, output voltage range $V_H - 1.5V$ for V_H less than 12V

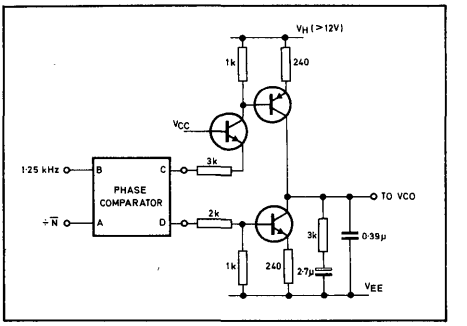


Fig. 10 Filter D. Current pump output voltage range $V_H - 1.5V$ for V_H greater than 12V

NPUT/OUTPUT CIRCUITS (FIGS. 11 THROUGH 16)

The following diagrams show input and output circuit configurations used on the SP8921, 2 and 3.

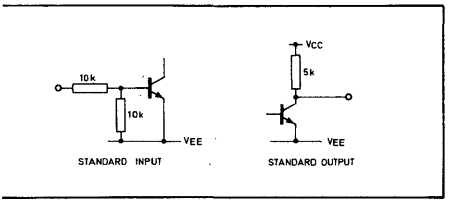


Fig. 11 Standard input and output

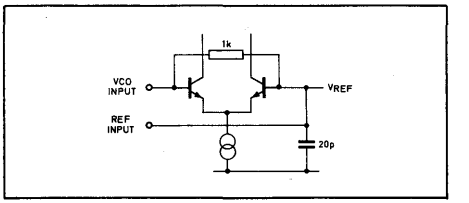


Fig. 12 VCO input

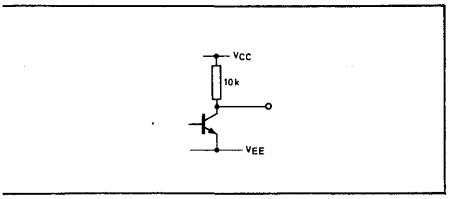


Fig. 13 Lock detect output

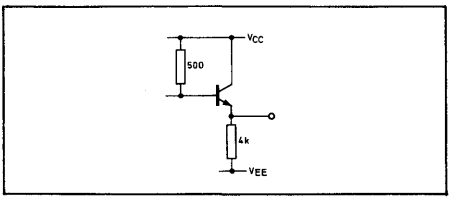


Fig. 14 10.24 MHz output

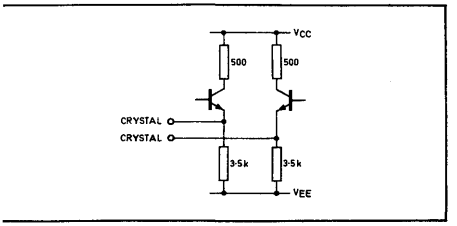


Fig. 15 Crystal oscillator inputs

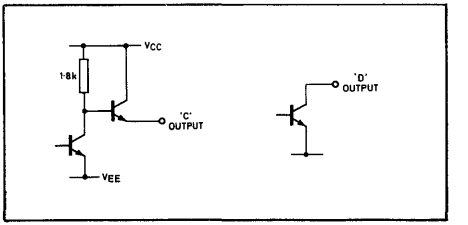


Fig. 16 Phase/frequency comparator outputs

FURTHER APPLICATIONS

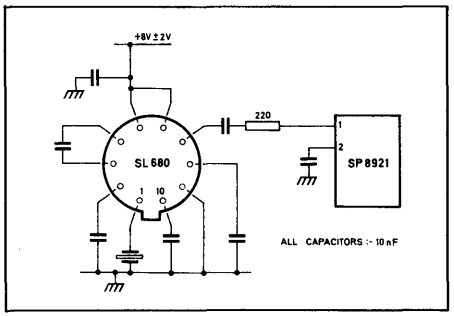


Fig. 17 High stability crystal reference oscillator using SL680

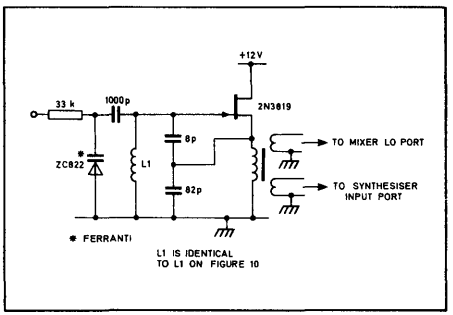


Fig. 18 Voltage controlled oscillator for 27MHz CB synthesiser

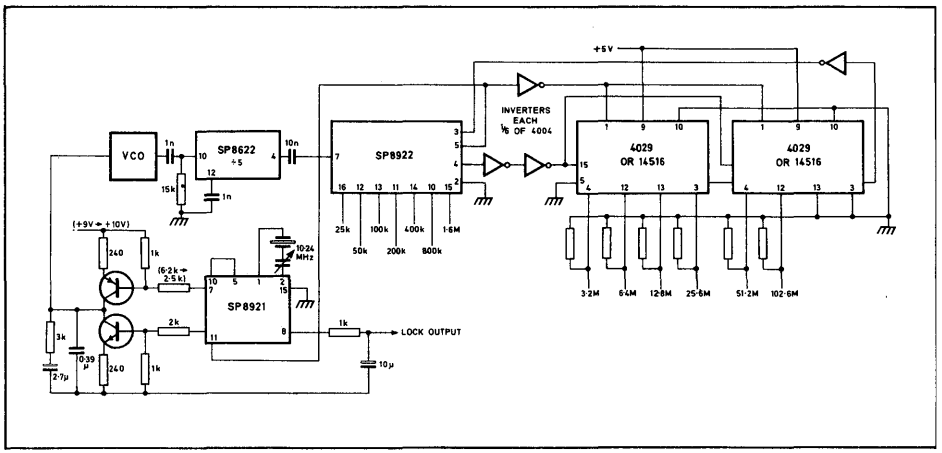


Fig. 19 200 MHz general purpose binary programmed synthesiser with 25KHz resolution using SP8921/22

PLESSEY
Semiconductors

SP9000 SERIES
DATA CONVERSION PRODUCTS

SP 9685
ULTRA FAST COMPARATOR

The SP 9685 is an ultra-fast comparator, and the SP 9687 is an ultra-fast dual comparator, both manufactured with a high performance bipolar process which makes possible very short propagation delays 2.2 nS typ ./ 2.7 nS typ. respectively. The circuits have differential inputs and complementary outputs fully compatible with ECL logic levels. The output currents capability are adequate for driving 50 ohm terminated transmission lines. The high resolution available makes the devices ideally suited to analogue-to-digital signal processing applications.

With the SP 9685 a latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used the latch enable may be connected to ground.

With the SP 9687 a latch function is provided to allow the comparator to operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If $\overline{LE}$ is high, and $\overline{LE}$ is low, the comparator function is in operation. When $\overline{LE}$ is driven low and $\overline{LE}$ high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, $\overline{LE}$ Must be connected to ground.

Both devices are compatible with the AM 685/AM 687 respectively but operate from conventional +5V and −5.2V rails.

FEATURES

- Propagation Delay 2.2 ns typ/2.7 ns typ respectively.
- Latch Set-up Time 1 ns max./0.5 ns typ
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM 685/687 but faster

QUICK REFERENCE DATA

- Supply voltages +5V, −5.2V
- Operating tempurature range −30°C to +85°C

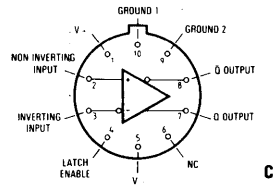
ABSOLUTE MAXIMUM RATINGS

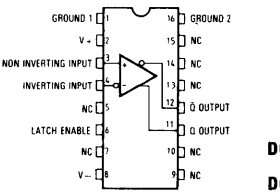
Positive supply voltage	6V
Negative supply voltage	−6V
Output current	30mA
Input voltage	± 5V
Differential input voltage	± 5V
Power dissipation	500mW
Storage	−55° to 150°C
Lead temperature (soldering 60 sec)	300°

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
V_{CC} = +5.0V ±.25V
V_{EE} = −5.2V ±.25V
R_L = 50 Ω

SP 9687
ULTRA FAST DUAL COMPARATOR





On metal package, pin 5 is connected to case. On DIP pin 8 is connected to case

Fig. 1 Pin connections

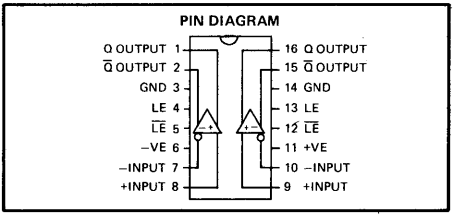
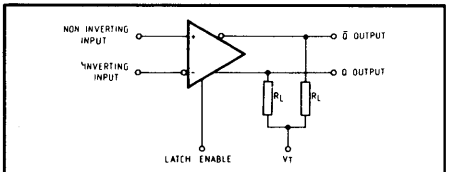


Fig. 1A



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V or 200–2000Ω connected to −5.2V

Fig. 2 Functional diagram

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Input offset voltage	Both	−5		+5	mV	Rs 100 ohms
Input bias current	Both		10	20	uA	
Input offset current	Both			5	uA	
Supply Currents Icc	SP 9685		19	23	mA	
IEE			23	34	mA	
	SP 9687		30		mA	
			54		mA	
Total Power Dissipation	SP 9685		210	300	mW	
	SP 9687		430		mW	Nominal Conditions
Min. Latch Set-up Time	SP 9685		0.5	1	ns	
	SP 9687		0.5		ns	
Input to Q Output Delay	SP 9685		2.2	3	ns	
	SP 9687		2.7	4	ns	
Input to $\overline{Q}$ Output Delay	SP 9685		2.2	3	ns	
	SP 9687		2.7	4	ns	100 mV pulse
Latch to Q delay	SP 9685		2.5	3	ns	10 mV Overdrive
	SP 9687		2.7	4	ns	
Latch to $\overline{Q}$ delay	SP 9685		2.5	3	ns	
	SP 9687		2.7	4	ns	
Min. latch pulse width	Both		2	3	ns	
Min. hold time	Both			1	ns	
Common Mode Range	Both	−2.5		+2.5	V	
Input Capacitance	Both		3		pF	
Input Resistance	Both	60			K ohms	
Output Logic Levels						
Output High	Both	−.96		−.81	V	At Nominal Supply
Output Low	Both	−1.85		−1.65	V	Voltages.
Common Mode Rejection Ratio	Both	80			dB	See Fig. 4
Supply Voltage Rejection Ratio	Both	60			dB	

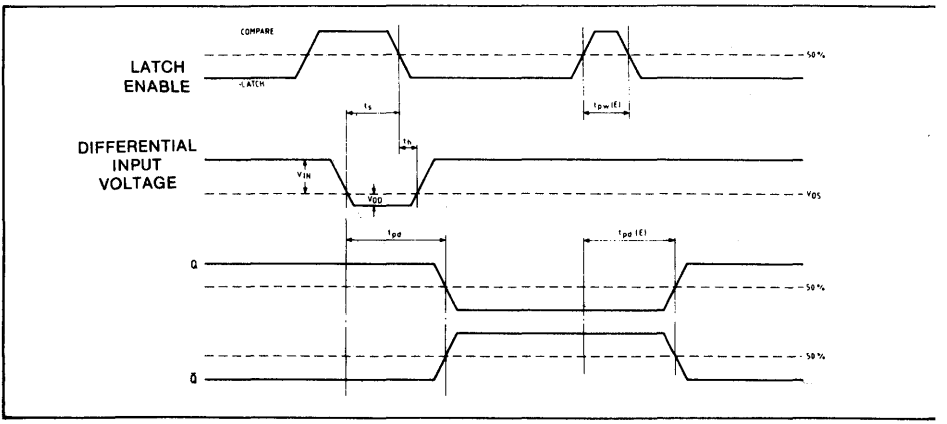


Fig. 3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse, switches the comparator over after a time tpd. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse with $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Definition of terms

Vos Input offset voltage – The potential difference required between the input terminals to obtain zero output potential difference.

Ios Input offset current – The difference betweer

the currents into the inputs when there is zero potential difference between the outputs.

I_B Input bias currents - The average of the two input currents. I_B is a chip design trade-off parameter; externally, it is desirable to have I_B as low as possible, while internally, circuit performance requirements demand higher I_B.

R_{IN} Input resistance - The resistance looking into either input with the other grounded.

C_{IN} Input capacitance - The capacitance looking into either input pin with the other grounded.

Switching terms (refer to Fig. 3)

t_{pd+} Input to output high delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to output low delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ Latch enable to output high delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ Latch enable to output low delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transistion to the 50% point of an output HIGH to LOW transition.

t_s Minimum set-up time – The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h The minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ Minimum latch enable pulse width – The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

V_{CM} Input voltage range – The range of input voltages for which the offset and propagation delay specifications are valid.

CMRR Common mode rejection ratio – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Latched and unlatched gain

The gain of a high speed, high gain comparator is difficult to measure, because of input noise and the possibility of oscillations when in the linear region. For a full ECL output level swing, the unlatched input shift required is approximately 1mV. In the latched mode, the feedback action in effect enhances the gain and the limitation in the noise/oscillation level; under these conditions the usable resolution is 100μV, although this is only achieved by careful circuit design and layout.

Interconnection techniques

High speed components in general need special precautions in circuit board design to achieve optimum system performance. The SP 9685/SP9687, with around 50 dB gain at 200MHz, should be provided with a ground plane having a low inductance ground return. All lead lengths should be as short as possible, and RF decoupling capacitors should be mounted close to the supply pins. In most applications, it will be found to be necessary to solder the device directly into the circuit board. The output lines should be designed as microstrip transmission lines backed by the ground plane with a characteristic impedance between 50Ω and 150Ω. Terminations to −2V, or Thevenin equivalents, should be used.

Measurement of propagation and latch delays

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

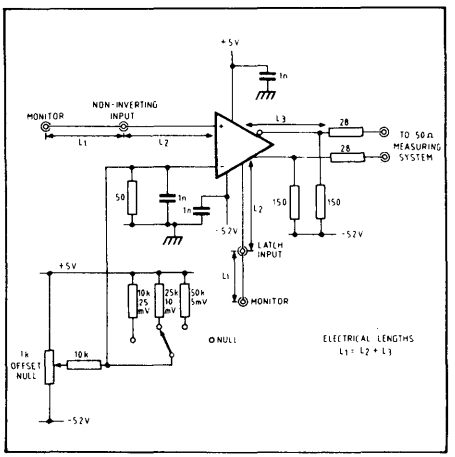


Fig. 4 SP9685/9687 test circuit

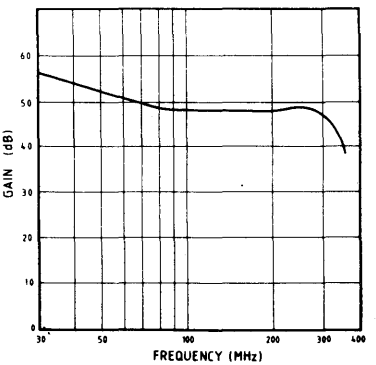


Fig. 5 Open loop gain as a function of frequency

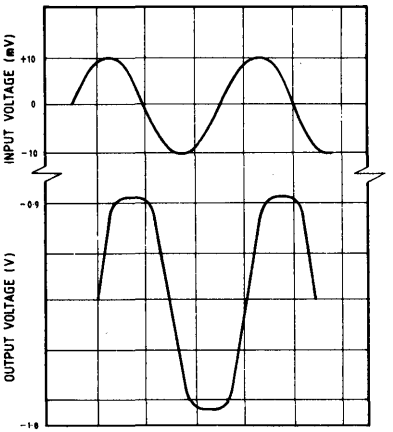


Fig. 6 Response to a 100MHz sine wave

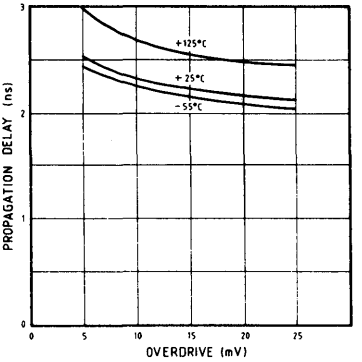


Fig. 7 Propagation delay, latch to output as a function of overdrive

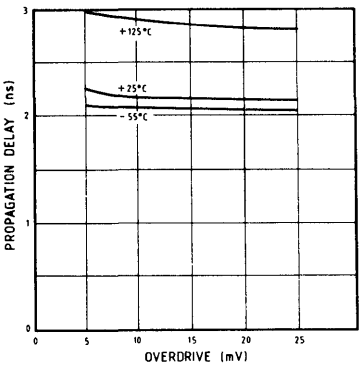


Fig. 8 Propagation delay, input to output as a function overdrive

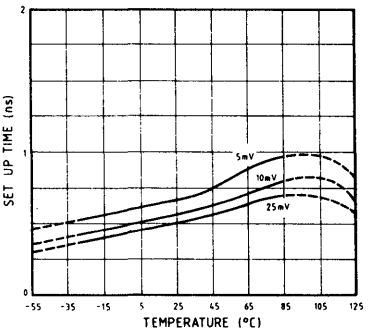


Fig. 9 Set-up time as a function of temperature

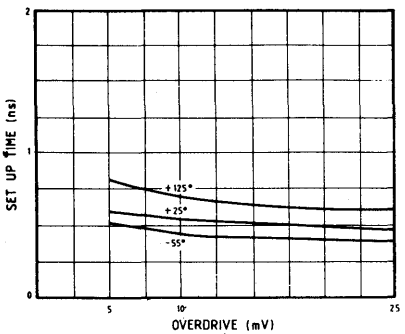


Fig. 10 Set-up time as a function of input overdrive

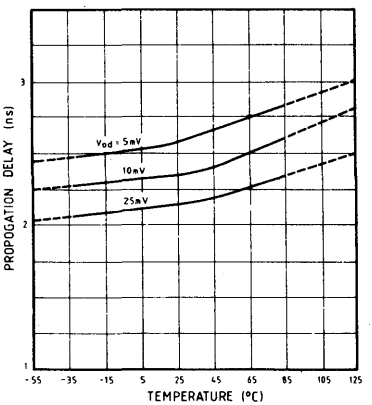


Fig. 11 Propagation delay, input to output as a function of temperature

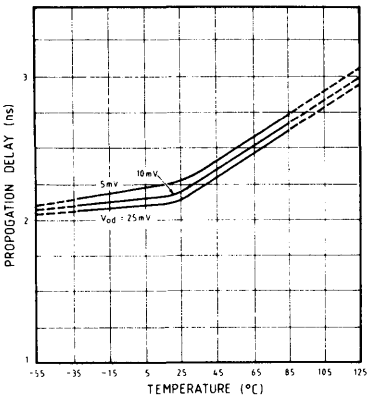


Fig. 12 Propagation delay, latch to output as a function of temperature

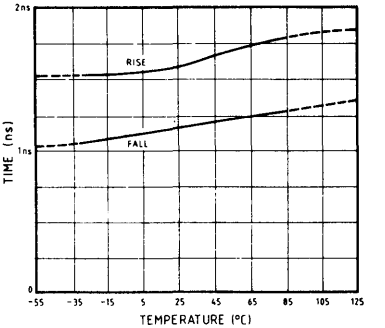


Fig. 13 Output rise and fall times as a function of temperature

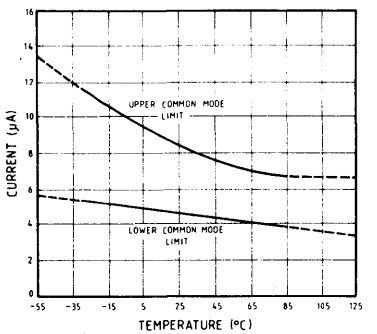


Fig. 14 Input bias currents as a function of temperature

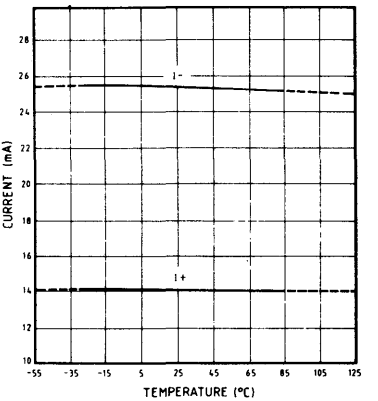


Fig. 15 Supply current as a function of temperature

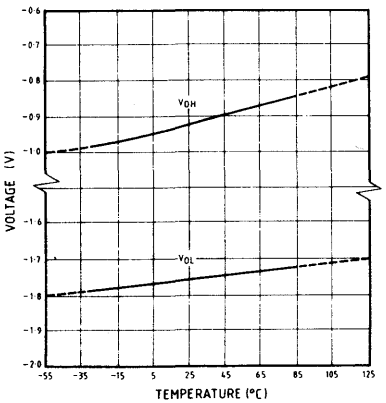


Fig. 16 Output levels as a function of temperature

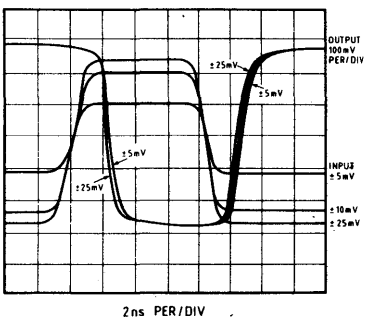


Fig. 17 Response to various input signal levels

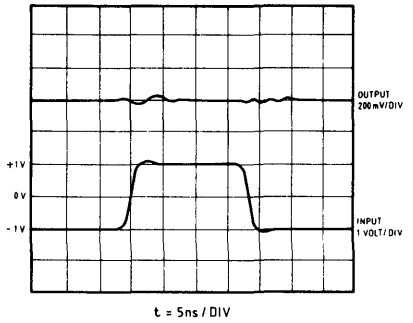


Fig. 18 Common mode pulse response

SP9750

HIGH SPEED COMPARATOR

The SP9750 is a high speed comparator with a latch circuit and other facilities intended for use in the construction of fast A–D converter systems. The speed capability of the device is compatible with conversion rates of up to 100 Mega-samples per second. Input and output logic levels are ECL compatible.

FEATURES

- Latch Set-up Time 2ns Max.
- Max. Input Offset Voltage 5mV
- Propagation Delay 3ns (Typ.)
- ECL Compatible
- Comparator Output Gating
- Wired OR Decoding for 4 Bits
- Current Output Settling to 0.2% in 8ns

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	−5.5V
Reference supply voltage	−8.5V
Reference current output	15 mA
Input voltage	±4V
Differential input voltage	±6V
Power dissipation	500 mW
Operating temperature range	−30°C to +85°C
Storage temperature range	−65°C to +150°C
Lead temperature (soldering 30 sec)	300°C

Logic input voltages to gate and latch V_{EE} to 0

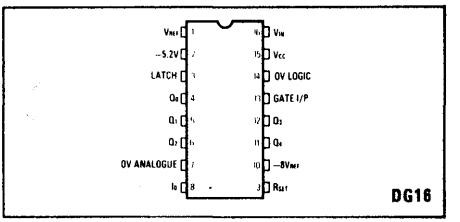


Fig. 1 Pin connections

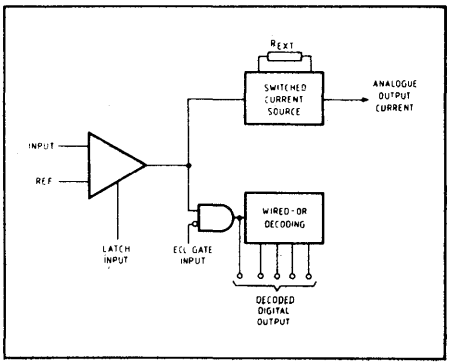


Fig. 2 Block diagram of SP9750

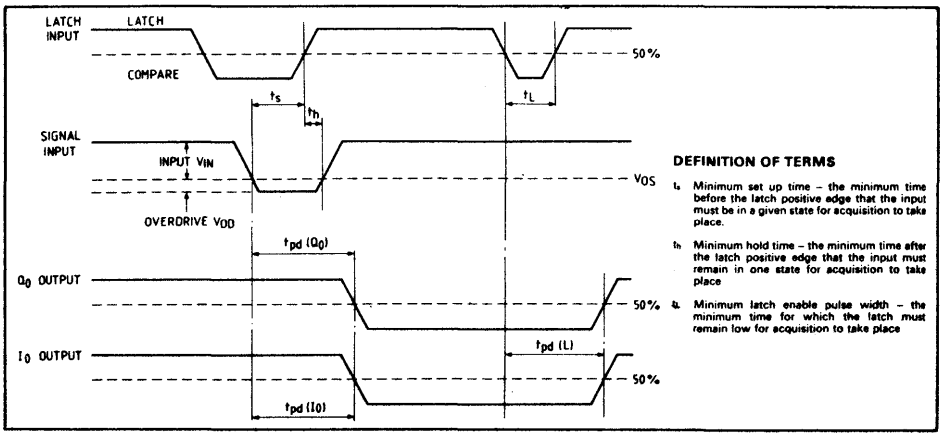


Fig. 3 Timing diagram SP9750

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = +25°C
V_{CC} = +5V ±0.25V
V_{EE} = −5.2V ±0.25V
V_{REF} = −8V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−5		+5	mV	
Input bias current			25	µA	
Input offset current			5	µA	
Supply currents V_{CC}		16	20	mA	
V_{EE}		35	42	mA	
V_{REF}		14	18	mA	
Total power dissipation		390	470	mW	
Analogue O/P current 'on'		5		mA	See operating note 1
Analogue O/P current 'off'			5	µA	+5V on pin 8
Precision current stability		20		ppm/°C	Also depends on R_{EXT}
Min. latch set-up time (t_s)			2	ns	See operating note 2
Input to Q_o O/P delay (tpd (Q_o))		3	4.5	ns	V_{IN} = 100 mV, 25 mV over drive, 50Ω load
Input to I_o delay (tpd (I_o))		3	4.5	ns	on I_o to 0 volts (Note 3)
Delay gate input to Q_{1-4} high		1.5	2.5	ns	See operating note 4
Delay gate input to Q_{1-4} low		1.5	2.5	ns	
Latch to I_o (tpd (LI_o))					
between 50% points		3	4.5	ns	
to 1% settling		4	8	ns	See operating note 5
to 0.2% settling		8	12	ns	
Min. hold time t_h		1		ns	
Min. latch pulse width (t_L)		2		ns	
Common mode range	−2.5V		+2.5V	V	
Diff. mode range			5	V	
Node capacitance I_o		3.5		pf	
Node capacitance analogue input			3	pf	
Input resistance	60			KΩ	
Output logic levels					
Logic '1'	−.98		−0.78	V	V_{CC} = +5V, V_{EE} = −5.2V
Logic '0'	−1.85		−1.6	V	R_L = 220Ω to −2V

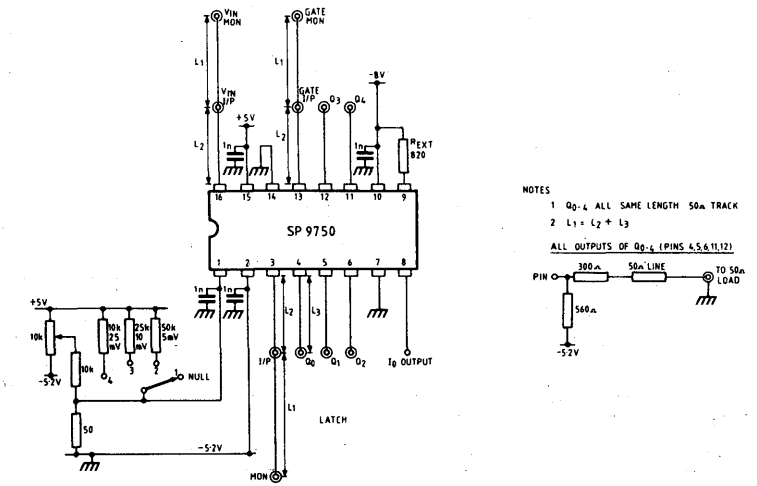


Fig. 4 Test circuit

GENERAL DESCRIPTION

The SP9750 is a fast comparator combined with a latch facility which allows the device to be operated in the sample and hold mode.

When the latch is 'low' the comparator is in the 'follow' mode, and when the latch is driven 'high' the output is locked in the existing state. The latch circuitry will therefore always produce a decision on the input state.

The comparator has a relatively low gain in the follow mode, which assists in achieving an extremely fast response. However, due to the positive feedback action of the latch function, the gain approaches infinity during the latch cycle, thereby ensuring high resolution.

In addition to the basic comparator, the following functions are provided on the chip to optimise the performance of high speed parallel-series-parallel A to D converter systems.

1. An ECL compatible gating function for simplified multi-comparator output logic.

2. Four emitter follower outputs from the gate to provide wired OR decoding for four bits.

3. A precision current source, set by an external resistor.

4. A high speed switch for the precision current to provide a fast and convenient reconstruction of the analogue input. Summing the currents in a multi-level comparator chain provides the D to A conversion directly for the construction of converters of the parallel-series-parallel type.

The philosophy adopted in the SP9750 makes possible the construction of ultra-fast, high accuracy *parallel-series-parallel converters* by integrating a significant portion of the system function on the same chip as the comparator. The result is not only to reduce considerably the total hardware count but to reduce the propagation delays where they are most critical, and eliminate redundant operations.

OPERATING NOTES

1. The analogue output current (Io) is set by means of an external setting resistor (R_{EXT}) and is equal to the reference voltage on Pin 9 (−8V nominal), divided by R_{EXT}. The accuracy of this reference voltage must be consistent with the conversion accuracy required. The output (Pin 8) compliance is −0.8V to +5.0 volts for correct operation.

2. This parameter is defined with +100 mV input and −10 mV overdrive, corrected to take account of the comparator offset, i.e. the switching threshold effectively is at OV on the input waveform. The relationship between setup time and overdrive is shown in Fig. 7c. The test circuit diagram, Fig. 4 indicates a method of performing this test.

3. Due to the relatively low gain of the comparator in the unlatched state, propagation measurements are defined with a 25 mV overdrive. The relationship between overdrive and delay is shown in Figs. 7a and b.

4. The gate input accepts an ECL drive. The outputs Q_1 to Q_4 are active when the gate input is at an ECL 'low' level, (−1.75V) and are switched by the internal circuitry. A 'high' gate input (− 0.9 V) switches the outputs to 'low', allowing the bussing of multiple devices onto the Q_1 – Q_4 rails.

5. Output settling times are measured at 10 mV overdrive conditions; larger overdrives produce shorter delays.

6. The test arrangement shown in Fig. 4 provides for a simple dynamic test of the SP9750 functions. When the switch is in position 1, the input offset voltage is nulled with the potentiometer, a condition detected by observing the output to be at the mid-point of its range (I_o or Q_o). The latch must be 'low' for this measurement. The offset voltage can be measured with a high impedance instrument. Positions 2, 3 and 4 provide increasing amounts of bias to the reference input corresponding to overdrives of 5mV, 10 mV, and 25 mV. For convenience of operation, the input analogue signal is referred to ground, and the reference input is set above ground, so that an input waveform which is positive going and referred to ground is all that is necessary. It should have an amplitude of (100 mV + overdrive voltage) and should have less than 5% overshoot. The risetime should be about 2 nS. Simple circuit modifications and a negative going signal would provide for inputs of opposite polarity. For accurate timing, the path length L_1 should be equal to $L_2 + L_3$ properly terminated.

Static (DC) measurements can also be performed on the same test arrangement.

APPLICATIONS

Although the SP9750 was aimed at a particular system configuration it is sufficiently flexible to find application in a variety of conversion methods. In an all-parallel A–D converter, the SP9750 is capable of achieving sampling rates of up to 100 Megasamples per second. This technique is usable up to 5-bit accuracy. For higher bit accuracies, techniques such as the parallel-series method are required. Fig. 5 shows the schematic *diagram of an A–D converter system capable of giving* 8-bit accuracy at sampling rates of up to 30 Mega-samples per second. The SP9750 is used in two 4-bit stages operating in the parallel-series-parallel mode. The analogue current output settling time from the first stage (an effective DAC facility) is dominated by the settling time of the one comparator which has the smallest overdrive. All other comparators have longer to settle, since the preceding sample and hold must be allowed to settle. For an 8-bit system, each comparator in the first 4-bit conversion has a weighting of 1/15 of full scale input. Therefore the settling band of interest for $\pm \frac{1}{2}$ L.S.B. is 2.9%. Typically the SP9750 settles to less than this, 1%, in four nanoseconds, illustrating the possibility of converter construction at higher speeds, or higher accuracies.

In order to achieve the optimum performance of this device, care must be taken to ensure that good layout practice is used, consistent with high frequency practice. A ground plane construction should be used and all leads should be designed to be microstrip transmission lines. The device should be soldered directly into the circuit board and the supplies decoupled with RF capacitors as close to each device as possible. In addition, to achieve the shortest possible settling time for the analogue current output, it is essential to keep the stray capacitance on Pin 9 (R_{SET}) to a minimum.

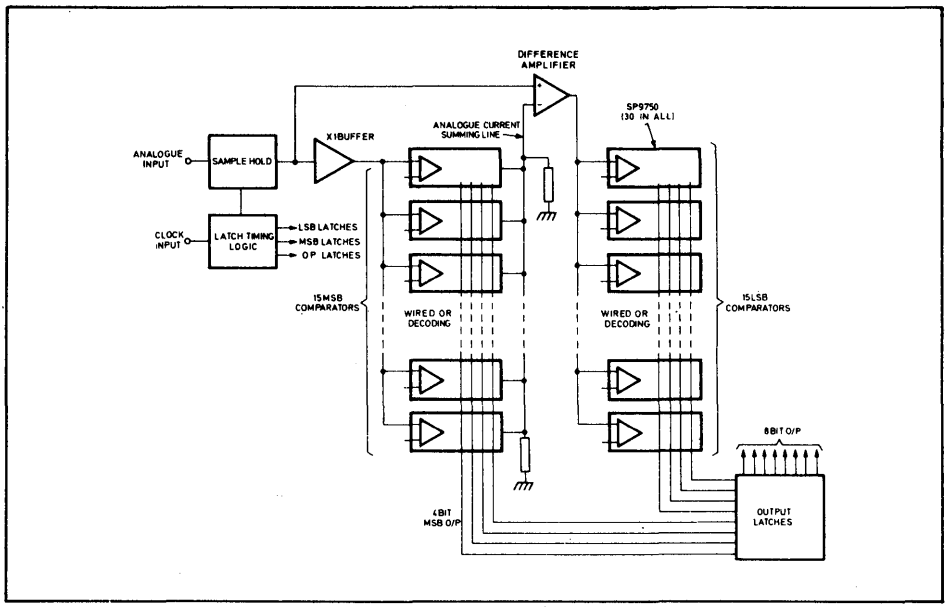


Fig. 5 Block diagram of a 4 x 4 bit parallel-series A/D converter

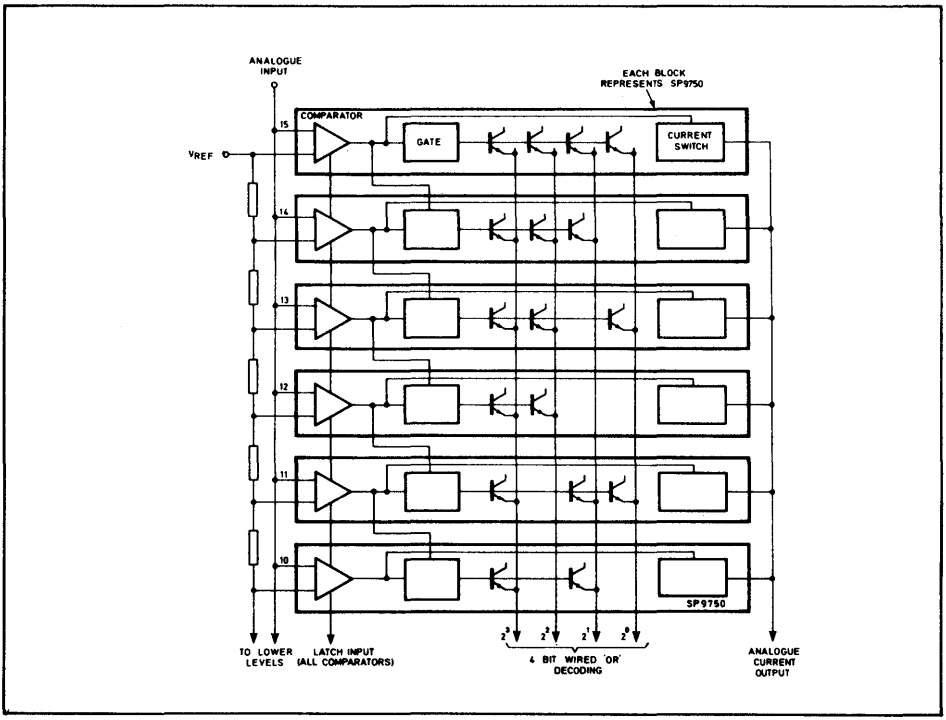


Fig. 6 Block diagram of 4-bit LSB stage showing top six levels

Fig. 7 Performance curves. Unless otherwise specified, standard conditions for all curves are $T_{AMB} = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.2V$, $V_{REF} = -8.0V$, I_O load $= 50\Omega$

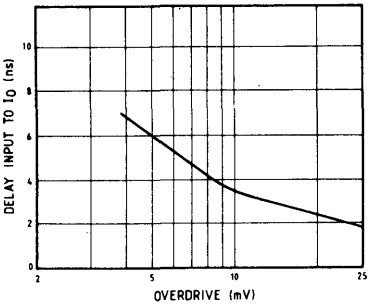


Fig. 7a input to 1_O output delay v. overdrive

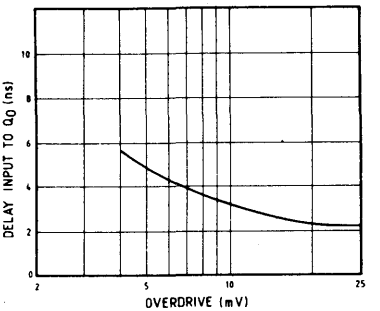


Fig. 7b Input to Q_O output delay v. overdrive

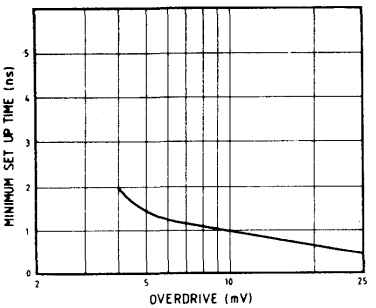


Fig. 7c T_S v. overdrive set-up time

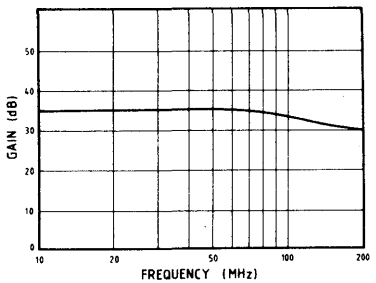


Fig. 7d Small signal gain v. frequency (to Q_O output). Latch input low.

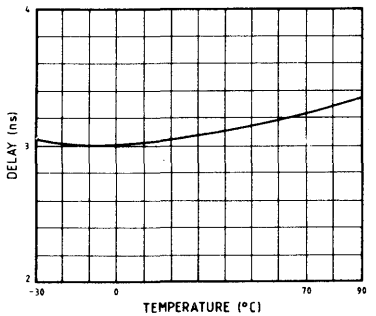


Fig. 7e Input to 1_O output delay as a function ot temperature

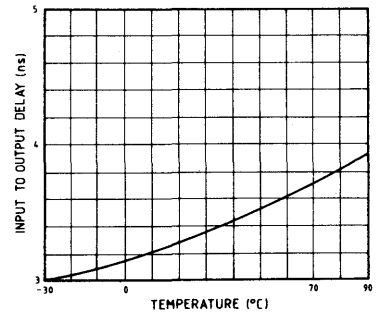


Fig. 7f Input to Q_O output delay as a function of temperature

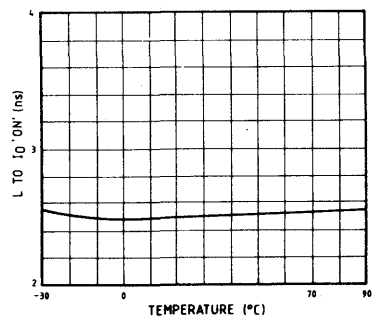


Fig. 7g Latch to I_O 'on' delay as a function of temperature

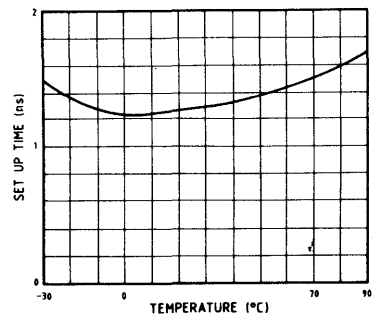


Fig. 7h Minimum set-up time as a function of temperature

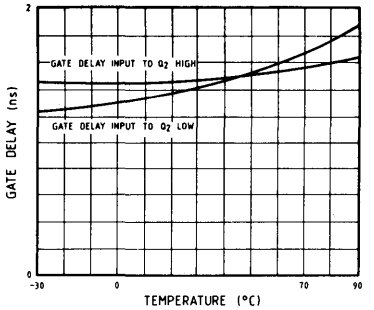


Fig. 7i Gate input to Q_1 – Q_4 delay variation with temperature

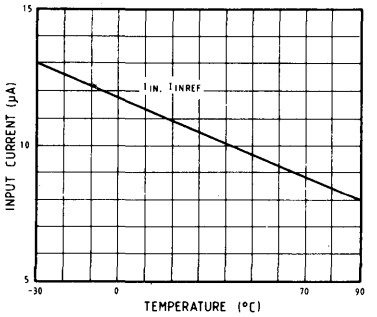


Fig. 7k Input current variation with temperature

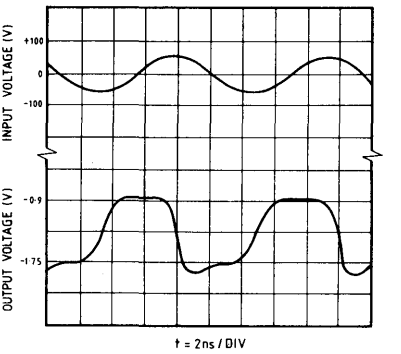


Fig. 7j Response to 100MHz sine wave

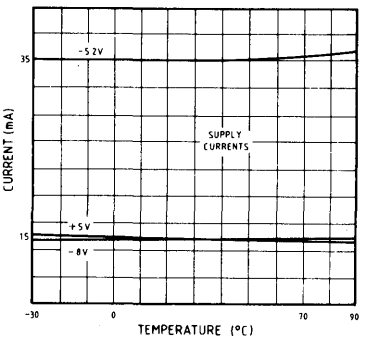


Fig. 7l Supply current variation with temperature

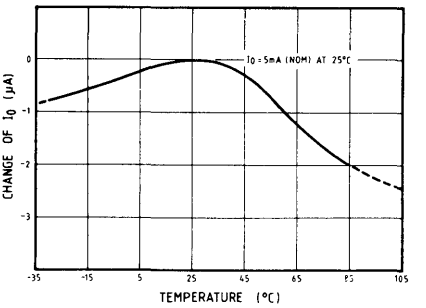


Fig. 7M Analogue output current variation with temperature

PLESSEY
SEMICONDUCTORS

NOVOL
NON-VOLATILE LOGIC

PROVISIONAL DATA

MN9102

NON-VOLATILE QUAD LATCH

The Plessey MN9102 is a non-volatile 4-bit data latch which uses MNOS transistors as memory elements to retain stored data in the absence of applied power. The data that is applied to the four inputs is written into the memory when the SAVE control is taken to a logic '0' level and the data subsequently appears on the four outputs. The stored data is also automatically restored to the outputs whenever power is re-applied to the device.

An OUTPUT ENABLE is also available, which when taken to logic '0' level presents a high impedance state on each data output line, permitting multiplexed operation.

The high voltage usually associated with MNOS memory devices is generated internally, requiring only a single external capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.

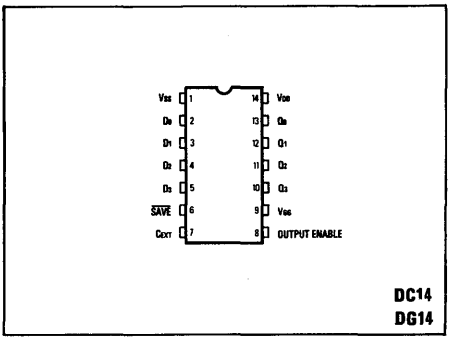


Fig. 1. Pin connections (top).

FEATURES

- Data Retention for One Year in the Absence of Applied Power
- Simple to Use
- Standard Power Supplies Only (+5V, —12V)
- CMOS/TTL Compatible
- 14-lead DIL Package
- Typically Ten Million SAVE Operations

APPLICATIONS

- Metering Systems
- Elapsed Time Indicators
- Security Code Storage
- Last Channel Memory for Digital Tuning

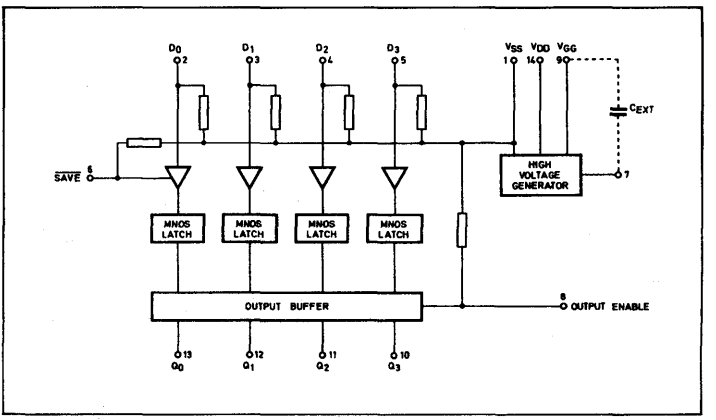


Fig. 2 Block diagram of MN9102

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):
V_{SS} = + 5V ± 5%
V_{DD} = 0V
V_{GG} = —12V ± 5%
Output loading = 1 TTL load
Ambient operating temperature range including data retention in the absence of applied power: 0°C to + 70°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Logic '0' input voltage	V_{IL}			0.8	V	Nominal 20kohms internal pullup
Logic '1' input voltage	V_{IH}	V_{SS}–1			V	resistor to V_{SS} on all inputs
Logic '0' output voltage	V_{OL}			0.6	V	Output current = —1.6mA
Logic '1' output voltage	V_{OH}	V_{SS}—1			V	Output current = 100 µA
Output leakage current		—10		+10	µA	$V_{SS} \geqslant V_{OUT} \geqslant V_{DD}$ with OUTPUT ENABLE = V_{DD}
Output voltage on C_{EXT}			—38		V	Load on $C_{EXT} \geqslant$ 10Mohms
External reservoir capacitor	C_{EXT}	0.1		0.47	µF	See note 1
Data set-up time	t_s	1			µs	
Data hold time	t_h	1			µs	
Data settling time	t_d			7	µs	C_{LOAD} = 47pf
Output enable delay	t_o			2.5	µs	C_{LOAD} = 47pf
SAVE time	t_{SAVE}	10			ms	See note 2
SAVE duty cycle				50	%	See note 3
SAVE cycles		10^6	10^7			See note 5
SAVE rise and fall times	t_e			5	µs	
Data retention time		1			year	
Power dissipation			50	100	mW	See note 4

ABSOLUTE MAXIMUM RATINGS

(all voltages with respect to V_{SS})

Voltage on C_{EXT} —46 to + 0.3V
Voltage on V_{GG} —20 to + 0.3V
Voltage on any other pin —7 to + 0.3V
Storage temperature —55°C to + 125°C
Ambient operating temperature —40°C to + 80°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

OPERATING NOTES

1. When two or more devices are used, the C_{EXT} outputs may be tied together with a single external capacitor. The size of this capacitor should be increased in proportion to the number of devices.
2. Data can be entered into the latch with SAVE times much less than ten milliseconds, however the retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur, particularly when power is applied to the device.
3. Duty cycles in excess of 50% may be required in certain applications. An external supply (—37V ±5%) must then be used to maintain sufficient voltage on the C_{EXT} output.
4. The majority of the power dissipation arises from the current flow between V_{SS} and V_{GG}. The current level on V_{DD} is the sum of the logic '0' level current plus leakage currents.
5. Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of 10^5 may cause a reduction in the data retention time.

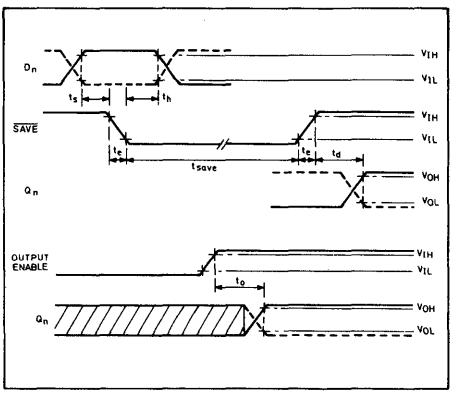


Fig. 3 Timing diagram

ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

PLESSEY
SEMICONDUCTORS

NOVOL
NON-VOLATILE LOGIC

PROVISIONAL DATA

MN9105

QUAD DECADE UP/DOWN COUNTER

The Plessey MN9105 is a 4-decade BCD counter which counts up or down on negative transitions of the CLOCK input. In parallel with the counter is a 16-bit non-volatile MNOS memory into which the contents of the counter can be written by holding CLOCK low and then taking $\overline{SAVE}$ to a low level. When data has been written into the memory, it can be retained even in the absence of applied power, and then subsequently be recalled from the memory to preset the counter.

Also associated with each counter decade is a 4-bit latch, the outputs of which follow the count sequence when $\overline{LOAD}$ is low. When $\overline{LOAD}$ goes high, the latches retain the data present at the time of the transition. The outputs from each latch are multiplexed onto a 4-bit data highway under the control of a 2-bit address (MX1, MX2). All four outputs may be put into a high input impedance state by holding $\overline{OUTPUT\ ENABLE}$ high, so allowing multiplexed operation between devices.

The final decade has a CARRY output to enable devices to be cascaded in series. An input CLOCK pulse ripples through to the CARRY output when the counter is in the 'up' mode and the '9999' state or when in the 'down' mode and the '0000' state.

The high voltage usually associated with MNOS devices is generated internally, requiring only a single capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.

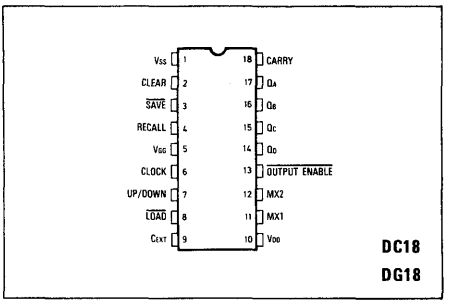


Fig. 1 Pin connections (top)

FEATURES

- Data Retention Guaranteed for One Year in the Absence of Applied Power Over Temperature Range 0°C to +70°C
- DC to 250 kHz Count Frequency
- Up/Down Count Facilities
- Standard Power Supplies (+5V, −12V)
- TTL/CMOS Compatibility
- 18-pin DIL Package

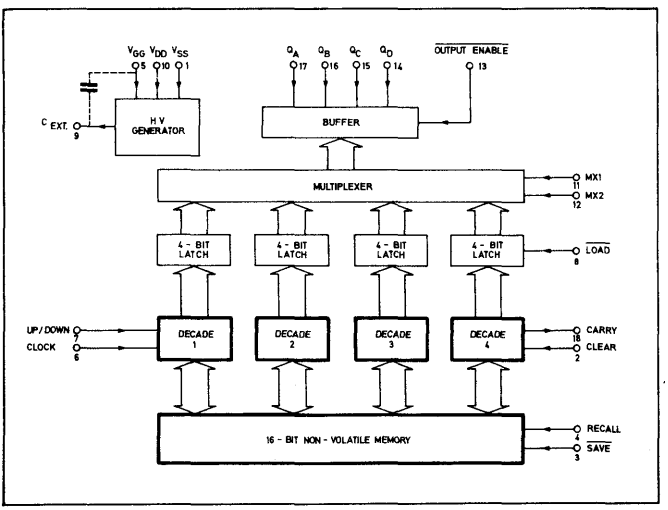


Fig. 2 MN9105 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{SS} = + 5V ± 5%
V_{DD} = 0V
V_{GG} = —12V ± 5%
Output loading = 1 TTL load
Ambient operating temperature range including data retention in the absence of applied power: 0°C to + 70°C

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Logic '0' input voltage	V_{IL}			0.8	V	
Logic '1' input voltage	V_{IH}	V_{SS}–1			V	
Logic '0' output voltage	V_{OL}			0.6	V	Output current= –1.6mA
Logic '1' output voltage	V_{OH}	V_{SS}–1			V	Output current= 100μA
High impedance leakage current		–10		+10	μA	$V_{SS} > V_{OUT} > V_{DD}$ with OUTPUT ENABLE = Vss
External capacitor	C_{EXT}	0.1		0.47	μF	
Output voltage on C_{EXT}			–37		V	
External leakage on C_{EXT}				2.5	μA	} See Note 3
SAVE duty cycle				10	%	
SAVE cycles		10^6	10^7			See Note 2
Data retention time		1			year	
Total integrated RECALL time between SAVE cycles		10^6			secs	
Power dissipation			250	400	mW	See Note 1

OPERATING NOTES

1. The majority of the power dissipation arises from current flow between V_{SS} and V_{GG}. The current level on V_{DD} is the sum of the logic '0' level currents plus leakage current only.
2. Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of 10^6 may cause a reduction in the data retention time.
3. An external capacitor is required to act as a charge reservoir for the high voltage which is generated on-chip from a high impedance source. Excessive external leakage on this capacitor or exceeding the quoted duty cycle can cause appreciable loading of the high voltage resulting in reduced data retention times. If operation outside these limits is required then an external high voltage (—37 volts ±5%) may be used to maintain the voltage level.
4. The CARRY pulse is equivalent to a CLOCK pulse which ripples through the counter when in the correct count sequence. For CLOCK pulse widths greater than or equal to 5 μs, the CARRY output may be connected directly to the input of a following device. For smaller widths, then pulse stretching must be used on the CARRY output to maintain the pulse width.
5. Data can be entered into the memory with SAVE times much less than 10 milliseconds; however the data retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur particularly when power is applied to the device.

MX2	MX1	OE	Q_D, Q_C, Q_B, Q_A	SAVE	Clock	Clear	Recall	Up/Down	Mode
*	*	1	High output impedance	1	↓	0	0	0	Count up
0	0	0	Decade 1	1	↓	0	0	1	Count down
0	1	0	Decade 2	1	*	↓	0	*	Set counter to 0000
1	0	0	Decade 3	1	*	0	↓	*	Preset counter from memory
1	1	0	Decade 4	0	0	0	0	*	Write into memory

* Logic '0' or '1' level
↓ Logic '1' to '0' transition

Table 1 Function table

ABSOLUTE MAXIMUM RATINGS

(all voltage with respect to V_{SS})

Voltage on C_{EXT} —46 to + 0.3V
Voltage on V_{GG} —20 to + 0.3V
Voltage on any other pin —7 to + 0.3V
Storage temperature —55°C to + 125°C
Ambient operating temperature —40°C to + 80°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

SWITCHING CHARACTERISTICS

Loading = 1TTL LOAD

$C_L = 10pF$

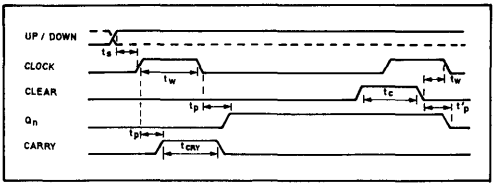


Fig. 3 Counter timing

Parameter	Symbol	Value	Units	Notes
Maximum CLOCK frequency		250	kHz	
Minimum CLOCK width	t_W	2	µs	
Minimum CLEAR width	t_C	1	µs	
Minimum up/down select	t_S	1	µs	
Maximum CLOCK to Qn delay Maximum CLOCK to CARRY delay	t_P	3	µs	
Maximum CLEAR to Qn delay	t_P'	2	µs	
Minimum CARRY width	t_{CRY}	2	µs	tw = 5µs (Note 4)
Maximum CLOCK rise/fall time Maximum CLEAR rise/fall time	t_e	10	µs	

Table 2 Counter switching characteristics

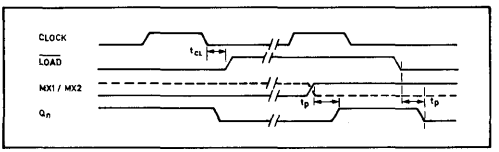


Fig. 4 Output control timing

Parameter	Symbol	Value	Units	Notes
Minimum CLOCK to $\overline{LOAD}$ delay	t_{CL}	2	µs	
Maximum Load to Qn delay Maximum MX1/MX2 to Qn delay	t_P	3	µs	

Table 3 Output control switching characteristics

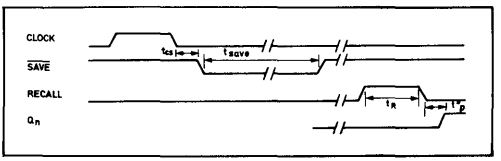


Fig. 5 Memory timing

Parameter	Symbol	Value	Units	Notes
Minimum SAVE time	t_{SAVE}	10	ms	Note 5
Minimum CLOCK to SAVE delay	t_{CS}	2	µs	
Minimum RECALL width	t_R	2	µs	
Maximum $\overline{RECALL}$ to Qn delay	t_P	3	µs	
Maximum $\overline{SAVE}$ rise/fall time Maximum RECALL rise/fall time	t_e	10	µs	

Table 4 Memory switching characteristics

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue, Irvine, CA 92714

NOVOL
NON-VOLATILE LOGIC

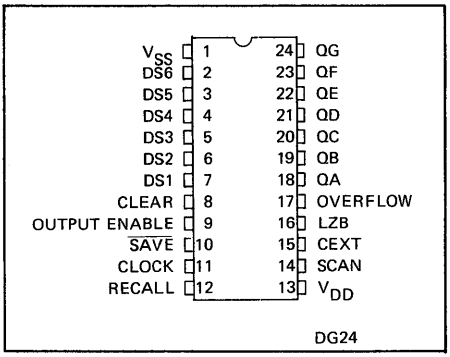
MN9106

SIX-DECADE UP-COUNTER

The MN9106 is a six-decade up-counter with a 24-bit parallel MNOS memory which can provide non-volatile data storage of the current count position. An additional latch and memory bit is also available to indicate a count overflow condition. In addition to the conventional counter controls there are RECALL and SAVE inputs available to control the two-way transfer of data between the counter and memory.

Output data is available in the form of multiplexed seven segment outputs with multiplexing under the control of an on-chip oscillator which can also be overdriven by an external source. The device operates from a single 12 volts supply and the high voltage required for the MNOS memory is generated on-chip requiring only a single external capacitor on CEXT.

The chip design for this device includes additional facilities discussed in the appendix such that variants of the device could be easily available using simple changes to the metallisation interconnection pattern.



MAIN FEATURES

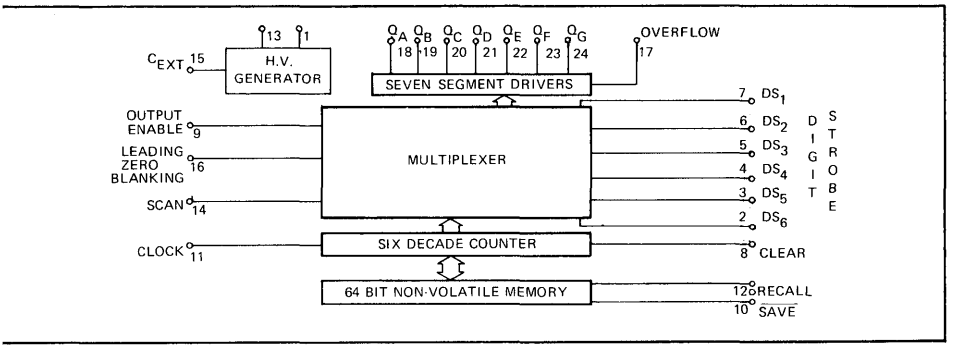
- DC to 100KHz count frequency
- Non-volatile data retention for 1 year over the temperature range $0^{o}C$ to $70^{o}C$.
- Operation from single 12 volt supply with CMOS compatible inputs.
- Operation from split supplies (+5, -7volts) allowing inputs to interface with TTL.
- Data "SAVE" time of 10 milliseconds.
- Leading zero and full blanking facilities.
- Multiplexed seven-segment outputs.
- Self scanning multiplexing.
- Counter overflow indicator.

ABSOLUTE MAXIMUM RATINGS

(All voltages w.r.t. V_{SS})

Externally applied voltage on C_{EXT}	+0.3 to -46 volts
Voltage on any other pin	+0.3 to -15 volts
Current drain on any digit strobe	10mA
Current drain on any other output	25mA
Ambient operating temperature	$-40^{o}C$ to $80^{o}C$
Storage temperature	$-55^{o}C$ to $125^{o}C$

The above limits are absolute limiting values above which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.



OPERATING CONDITIONS

Ambient operating temperature (including non-volatile date retention in the absence of applied power).	0°C to 70°C
	V_{SS} = 0 volts
	V_{DD} = -12±1 volts

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Logic '0' input level			V_{ss}-4	Volts	
Logic '1' input level	V_{ss}-1			Volts	
Input leakage current*	-10		+10	μA	$V_{DD} \leqslant V_{IN}$ $^{S}V_{SS}$
Logic '0' output leakage current	-10		+10	μA	$V_{DD} \leqslant V_{out} \Sigma V_{SS}$
Logic '1' output current					
Segment Drivers	10			mA)	
Overflow	10			mA)	$V_{out} = V_{ss}$ -3volts
Digit Strobes	3			mA)	
Count frequency	D.C.		100	KHz	
Clear width	5			μS	
Recall width	5			μS	
Clock width	5			μS	
Save width	10			mS	
Output delay			10	μS	
Internal Scan frequency		1		KHz	
External Scan frequency			25	KHz	
High Voltage output		-42		Volts)	
Save duty cycle			10	%)	

*Not applicable to SCAN input when overdriving from an external source.

CIRCUIT DESCRIPTION

The counter is a synchronous six decade B.C.D. counter, the outputs of which are multiplexed onto a 4-bit data highway and subsequently decoded into a seven segment format which drives open drain output transistors. An additional output transistor is driven directly from the overflow latch. Blanking facilities are available such that by holding OB at a logical '1', all eight outputs are turned off. When LZB is at a logical '1', leading zeros are blanked by turning off the seven segment outputs provided that the overflow latch is not at a logical 1. All outputs are also blanked when the device is in RECALL or CLEAR mode.

Count Sequence	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	
0 0 0 0 (0)	1	1	1	1	1	1	0	0
0 0 0 1 (1)	0	1	1	0	0	0	0	1
0 0 1 0 (2)	1	1	0	1	1	0	1	2
0 0 1 1 (3)	1	1	1	1	0	0	1	3
0 1 0 0 (4)	0	1	1	0	0	1	1	4
0 1 0 1 (5)	1	0	1	1	0	1	1	5
0 1 1 0 (6)	1	0	1	1	1	1	1	6
0 1 1 1 (7)	1	1	1	0	0	0	0	7
1 0 0 0 (8)	1	1	1	1	1	1	1	8
1 0 0 1 (9)	1	1	1	1	0	1	1	9
INVALID*	0	1	1	1	1	1	0	U

*Incorrect use of the device or operation outside of normal conditions can result in invalid B.C.D. characters appearing in the counter.

TABLE 1.

OE	LZB	OVERFLOW LATCH	$Q_A - Q_G$
1	X	X	Outputs off
0	0	0	As table 1
0	0	1	As table 1
0	1	0	As table 1 but with leading zero blanking
0	1	1	As table 1

TABLE 2

The multiplexing sequence is generated from an on-chip oscillator whose frequency is set by an external capacitor between the SCAN input and V_{SS}. This oscillator may also be forced from an external scan signal which must be capable of sinking and sourcing current on the SCAN input. The multiplex control scans through the counter a decade at a time in the sequence most significant decade to least significant. The decoded data from a particular decade is present for an entire oscillator period and the corresponding digit strobe output is turned on. The digit strobe outputs are independent of the LZB input, but all digit strobes are turned off during RECALL and CLEAR modes and also when OB = 0. The scan sequence is also reset at this time. The scan position increments on negative transitions of the scan input.

COUNT MODE – (Minimum CLOCK width = 5μsec)

The device is in count mode when RECALL and CLEAR are at a logical '0' input level and $\overline{SAVE}$ is at a logical '1'. The counter then increments on negative transitions of the CLOCK input. When the counter is in the '999999' state, the next negative CLOCK edge will set the overflow latch to a high state and counting commences again at "000000".

RECALL MODE – (Minimum RECALL width = 5μsec)

During recall mode the contents of the memory are preset into the counter and the overflow latch, the multiplex scanning sequence is reset and all outputs are turned off. The scanning sequence then recommences at the end of the recall period. The device is put into recall mode by taking the RECALL input to a logical '1' while CLEAR = 0, and $\overline{SAVE}$ = 1. The CLOCK input is disabled when in RECALL mode.

CLEAR MODE – (Minimum CLEAR width = 5μsec)

A logical '1' level on the CLEAR input with $\overline{SAVE}$ = 1 disables the CLOCK and RECALL inputs and puts the device into CLEAR mode. The counter and overflow latch are then reset to the all zeros state and the outputs are again turned off and the scanning sequence reset.

SAVE MODE – (SAVE width = 10 milliseconds)

During save mode, the data content of the counter and the overflow latch is written into the non-volatile memory. This is achieved by pulling the $\overline{SAVE}$ input to a logical '0' level, however if CLEAR, CLOCK or RECALL are at a logical '1' level, then the SAVE mode is inhibited until all of these three inputs have returned to a logical '0' level. These inputs are then subsequently disabled for the save period. This means that no external synchronisation is required between the save command and the other control inputs and ensures that valid data is present in the counter before saving and that this data is fixed throughout the entire save period.

Mode	Recall	Clear	Clock	Save
Clear	X	1	X	1
Recall	1	0	X	1
Count	0	0	↓	1
Save *	0	0	0	0

X = Don't Care ↓ = Logical '1' to '0' transition.

* Once this condition is satisfied any changes on CLOCK, CLEAR or RECALL are disabled until $\overline{SAVE}$ returns to a logical '1'.

NOTE:

Automatic recall at power-on is not included as the circuitry could only be guaranteed with carefully defined rise and fall times on the power rail, and would cause difficulties in other applications where rise and fall times are not controlled. No guarantee is therefore given as to the state of the counter at power-on and it is therefore the users responsibility to generate a RECALL or CLEAR pulse at power-on.

APPENDIX

The chip design for this device includes additional features that may be subsequently used for variants of the MN9106. These additional features do not impose any system or economic restrictions on the basic device, and variants of the device will be available by producing a modified aluminum interconnection layer only. The features included are:

1) Provision for CARRY output for cascading devices – The OVERFLOW output will be replaced by a CARRY output. This output will be such that an input CLOCK pulse appears on this output when the counter is in the "999999" state. The output characteristics of the CARRY will be the same as for the OVERFLOW output but the blanking function will be removed.

2) Provision for making one or more of the decard counters a divide by six element. By use of aluminum variants it is possible to have a range of counters specifically for timing applications (e.g., Elapsed time indicators, programmable timers). Possible counting configurations are then:

	Hours	Minutes	Seconds	$Seconds_{/100}$	Input Freq.
Variant A		59	59	99	100 Hz
Variant B		9999	59		1 Hz
Variant C	99	59	59		1 Hz
Variant B	9999	59			1/60 Hz

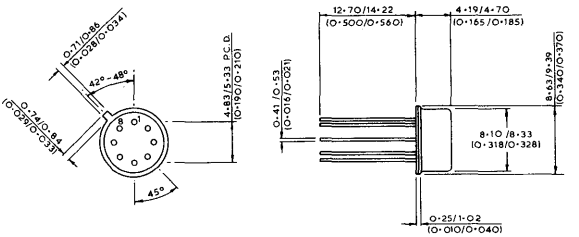
packages

package outlines

Dimensioned outline diagrams of the packages currently available for standard products are given on this and the following pages. Whilst every effort is made to ensure that the packages offered conform to these diagrams, certain changes may occur from time to time dependent on the supplies of piece parts. However, Plessey Semiconductors will attempt to ensure that such changes, should they occur, shall be minimal.

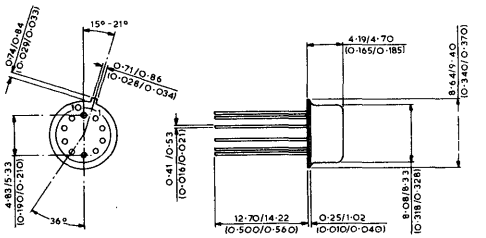
The code used to identify package outlines is that shown on the appropriate datasheet and on the following diagrams. The Pro-Electron code (see Ordering Information) is used – with the addition of numerals indicating the number of leads.

Note: Dimensions are shown thus: mm (inches)



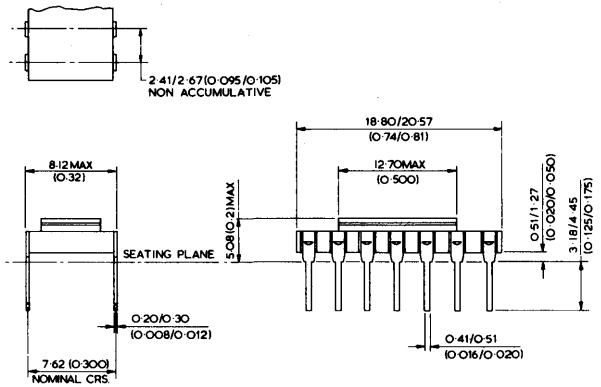
8 LEAD TO–5

CM8



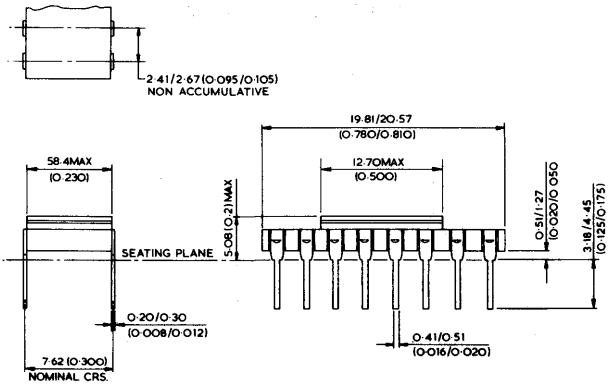
10 LEAD TO–5

CM10



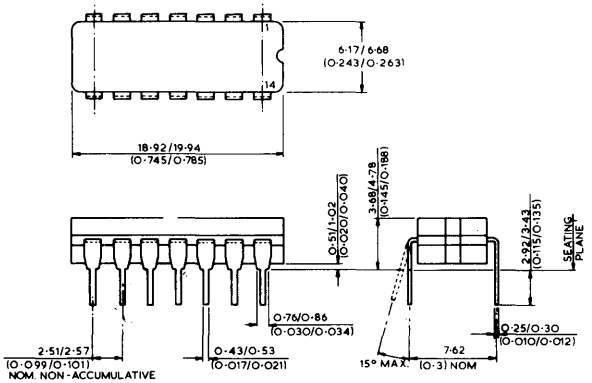
14 LEAD DILMON

DC14



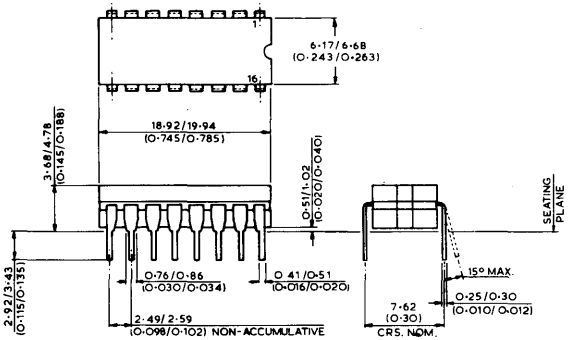
16 LEAD DILMON

DC16



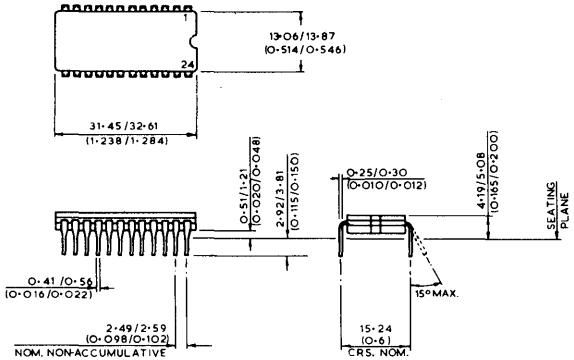
14 LEAD CERAMIC DIL

DG14



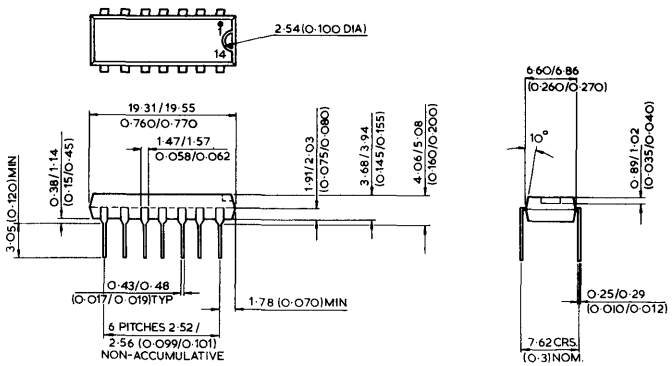
16 LEAD CERAMIC DIL

DG16



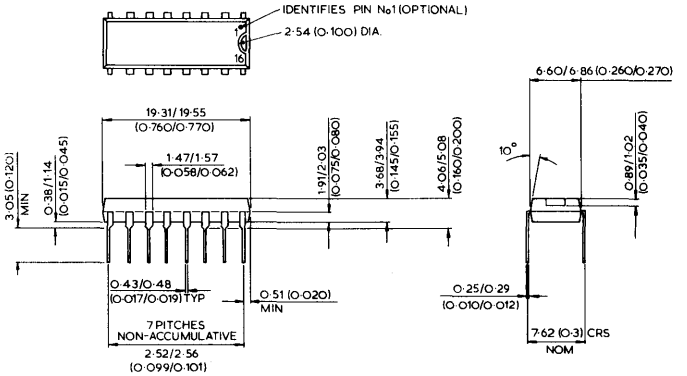
24 LEAD CERAMIC DIL

DG24



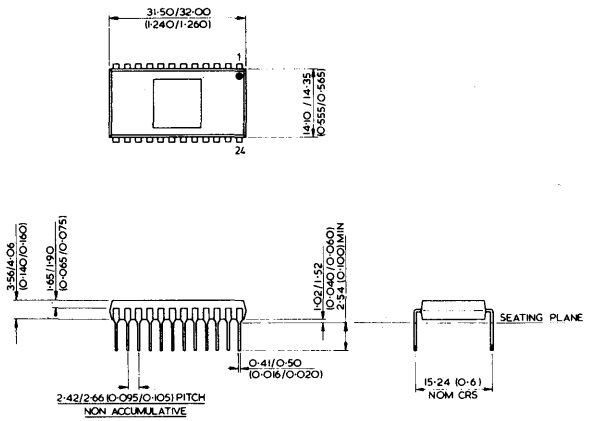
14 LEAD PLASTIC DIL

DP14



16 LEAD PLASTIC DIL

DP16



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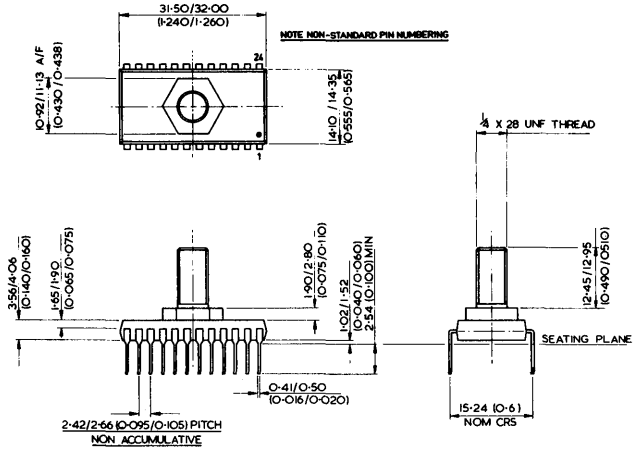
DP24



24 LEAD PLASTIC DIL WITH HEAT SINK STUD

DP24

ordering information

ordering information

U.K. ORDERS

Orders for quantities up to 99 received by Plessey Semiconductors at Swindon will be referred automatically to our U.K. distributors; quantities of 1000 and over must be ordered from Plessey Semiconductors direct, at the following address:

Plessey Semiconductors
Cheney Manor
Swindon
Wilts. SN2 2QW
Tel: (0793) 36251
Telex: 449637

OVERSEAS ORDERS

Products contained in this Databook can be ordered from your listed Plessey Office. Agent or Distributor.

PLESSEY SEMICONDUCTORS IC TYPE NUMBERING

Plessey Semiconductors integrated circuits are allocated type numbers which must be used when ordering. The Pro-Electron code is used to identify package outlines.

CM – Multilead TO-5
DC – Dilmon
DG – Ceramic Dual In-Line
DP – Plastic Dual In-Line
EP – Power Stud

This package code is for reference purposes only and need only be used when ordering where a device is offered in more than one package style. The package code does not appear on the device itself.

Plessey Semiconductors U.S.A.

PLESSEY SALES REPRESENTATIVES:

ALABAMA:	Huntsville	(205) 883-9260	REMCO
ARIZONA:	Scottsdale	(602) 948-4404	Faser Technical Sales
	Phoenix	(602) 997-1042	Eltron
CALIFORNIA:	Goleta	(805) 964-8751	The Thorson Company of So. California
	Marina Del Rey	(213) 822-1187	RELCOM
	San Diego	(714) 455-0055	Littlefield and Smith Assocs.
	Sunnyvale	(408) 245-9890	Bryan Procter
FLORIDA:	Kenneth City	(813) 546-6390	Kirkwood Assocs.
GEORGIA:	Duluth	(404) 476-1730	REMCO
ILLINOIS:	Elk Grove Village	(312) 439-9090	R-TEK
MARYLAND:	Beltsville	(301) 937-8321	Applied Engineering Consultants
MASSACHUSETTS:	Wayland	(617) 655-6080	Wayland Engineering Sales
MICHIGAN:	Brighton	(313) 227-1786	S.A.I. Marketing Corp.
MINNESOTA:	Bloomington	(612) 884-8291	Electronic Sales Agency Inc.
MISSOURI:	Independence	(816) 254-3600	Engineering Services Company
	St. Louis	(314) 997-1515	Engineering Services Company
NEW YORK:	Plainview	(516) 681-3155	Robert Smith Assocs.
	Spring Valley	(914) 354-6067	Robert Smith Assocs.
	Skaneateles	(315) 685-5731	Robtron Inc.
NORTH CAROLINA:	Raleigh	(919) 787-1461	REMCO
OHIO:	Shaker Hieghts	(216) 751-3633	S.A.I. Marketing Corp.
	Centerville	(513) 435-3181	S.A.I. Marketing Corp.
	Zanesville	(614) 454-8942	S.A.I. Marketing Corp.
ONTARIO:	Bolton	(416) 626-3805	MacKay Associates
OREGON:	Portland	(503) 227-0599	Bryan Procter
PENNSYLVANIA:	Pittsburgh	(412) 782-5120	S.A.I. Marketing Corp.
	Huntingdon Valley	(215) 947-5641	Dick Knowles Assocs.
TEXAS:	Arlington	(817) 640-9101	W. Pat Fralia Company Inc.
	Houston	(713) 772-1572	W. Pat Fralia Company Inc.
	Austin	(512) 451-3325	W. Pat Fralia Company Inc.
VIRGINIA:	Lorton	(703) 550-9799	Applied Engineering Consultants
WASHINGTON:	Seattle	(206) 345-0376	Bryan Procter

PLESSEY DISTRIBUTORS:

(Dial direct for orders under 100 pieces and faster delivery)

MARYLAND:	Beltsville	(301) 937-8321	Applied Engineering Consultants
NEW YORK:	Plainview	(516) 822-5357	Plainview Electronics Supply Corp.
TEXAS:	Arlington	(817) 649-8981	Patco Supply

PLESSEY REGIONAL OFFICES:

PAUL COOPER
National Sales Manager
1641 Kaiser Avenue
Irvine, CA 92714
(714) 540-9979
TWX 910-595-1930

BRYAN PROCTER
Western Sales/Applications
710 Lakeway
Suite 265
Sunnyvale, CA 94086
(408) 245-9890

JONATHAN HILL
Midwest Sales Manager
4825 N. Scott
Suite 308
Schiller Park, IL 60176
(312) 678-3280/3281
TWX 910-227-3746

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Eastern Sales Manager
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Hauppauge, New York 11787
(516) 273-3060
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A.J. Willis
S.E. Sales/Applications
Mailing Address:
89 Marcus Blvd.
Hauppauge, N.Y. 11787
Orlando Answering Service
(305) 859-4643

Plessey Semiconductors world-wide

;ales offices

RANCE Plessey France S.A., 16/20 Rue Petrarque, 75016 Paris. Tel: 727 43 49 Tx: 62789

'ALY Plessey S.p.A., Corso Sempione 73, 20149 Milan. Tel: 349 1741 Tx: 37347

CANDINAVIA Svenska Plessey A.B., Alstromergatan 39, 4tr, S-112 47 Stockholm 49, (P.O. Box 49023 S-100 28 Stockholm 49) Sweden. Tel: 08 23 55 40 Tx: 10558

WITZERLAND Plessey Verkaufs A.G., Glattalstrasse 18, CH-8052 Zurich. Tel: 50 36 55/50 36 82 Tx: 54824

NITED KINGDOM Plessey Semiconductors, Cheney Manor, Swindon, Wilts. SN2 2QW Tel: 0793 36251 Tx: 449637

SA Plessey Semiconductor Products, 1641 Kaiser Avenue, Irvine, Calif. 92714, Tel: (714)540-9979 Twx: 910 595 1930

essey Microsystems, Semiconductor Products Divn., 4825 N. Scott Street, Suite 308 74A, Schiller Park, Ill. 60176 Tel: (312) 671 4554 Twx: 910-227-0794

EST GERMANY Plessey GmbH., 8 Munchen 40, Motorstrasse 56, Tel: (89) 351 6021/6024 Tx: 5215322

Plessey GmbH, Moselstrasse 18, Postfach 522, 4040 Neuss. Tel: (02101) 44091 Tx: 517844

;gents

USTRALIA Plessey Ducon Pty. Ltd., P.O. Box 2, Christina Road, Villawood, N.S.W. 2163. Tel:72 0133 Tx: 20384

USTRIA Plessey GmbH., Rotenturmstrasse 25, Postfach 967, A-1011 Vienna. Tel: 63 45 75 Tx: 75 963

ELGIUM & LUXEMBOURG Plessey S.A., Chausee de St. Job 638, Brussels 1180, Belgium. Tel: 74 5971. Tx: 22100

RAZIL Plessey Brazil, Caixa Postal 7821, Sao Paulo. Tel: (011) 269 0211. Tx: 112338

ANADA Plessey Canada Ltd., 300 Supertest Road, Downsview, Toronto, Ontario. Tel: 661 3711. Tx: 065-24488

ASTERN EUROPE Commercial Manager, Mid and Eastern Europe, Plessey Co. Ltd., Ilford, Essex, IG1 4AQ England. Tel: 01-478-3040. Tx: 23166

IRE Plessey Ireland Ltd., Mount Brown, Old Kilmainham, Dublin 8. Tel: 75 84 51/2. Tx: 4831

ONG KONG Plessey Co. Ltd., Room 1002, Connaught Building, 54-46 Connaught Road C, (P.O. Box 617) Tel: 5-452145. Tx: 74754

APAN Cornes & Co Ltd., Maruzen Building, 2 Chome Nihonbashi-Dori. C.P.O. Box 158, Chuo-ku, Tokyo 103. Tel: 272-5771. Tx: 24874

Cornes & Co Ltd., Marden House, C.P.O. Box 239, Osaka. Tel: 532-1012/1019. Tx: 525-4496

ETHERLANDS Plessey Fabrieken N.V., Van de Mortelstraat 6, P.O. Box 46, Noordwijk. Tel: 01719 19207. Tx: 32008

EW ZEALAND Plessey (N.Z.) Ltd., Ratanui Street, Private Bag, Henderson, Auckland 8. Tel: Henderson 64 189. Tx: 2851

ORTUGAL Plessey Automatica Electrica, Portugesa S.A.R.L., Av. Infant D. Henrique 333, Apartado 1060, Lisbon 6. Tel: 313173/9 Tx: 12190

OUTH AFRICA Plessey South Africa Ltd., Forum Building, Struben Street, (P.O. Box 2416) Pretoria 0001, Transvaal. Tel: 34511 Tx: 30277

'AIN The Plessey Company Ltd, Calle Martires de Alcala, 4-3 Dcha., Madrid 8. Tel: 248 12 18 and 248 38 82 Tx: 42701

distributors

FRANCE Scientech, 11 Avenue Ferdinand Buisson, 75016 Paris. Tel: 609 91 36 Tx: 26042

ITALY Melchioni, Via P. Colletta 39, 20135 Milan. Tel: 5794

SCANDINAVIA Scansupply A/S., Nannasgade 20, Dk-2200 Copenhagen, Denmark. Tel: 93 5090 Tx: 19037

Oy Ferrado A.B. Nylandsgatan 2C, 00120 Helsinki 12, Finland. Tel: 65 60 05 Tx: 121394

Skandinavisk Elektronikk A/S., Ostre Aker Vei 99, Veitvedt, Oslo 5, Norway. Tel: (02) 15 00 90 Tx: 11963

SWITZERLAND Lacoray S.A., 8049 Zurich, Ackersteinstrasse 161, Tel: 56 56 70 Tx: 57653

UNITED KINGDOM (For all circuits except T.V.)

Farnell Electric Components Ltd., Canal Road, Leeds LS12 2TU Tel: 0532 636311 Tx: 55147

Gothic Electronic Components, Beacon House, Hampton Street, Birmingham B19 3LP. Tel: 021 236 8541 Tx: 338731

Semiconductor Specialists (UK) Ltd., Premier House, Fairfield Road, Yiewsley, West Drayton, Middlesex. Tel: 08954 46415 Tx: 21958

SDS Components Ltd., Hilsea Industrial Estate, Portsmouth, Hampshire PO3 5JW. Tel: 0705 65311 Tx:86114

For T.V. circuits only:-

Best Electronics (Slough) Ltd., Unit 4, Farnburn Avenue, Slough, Bucks SL1 4XU Tel: (0753) 31700 Tx: 847571

C.P.C. Ltd., 194-200 North Road, Preston PR1 1YP. Tel: (0772) 55034 Tx: 677122

USA Semiconductor Specialists, P.O. Box 66125, O'Hare Internatl Airport, Chicago, Ill. Tel: 312 279 1000 Twx: 910-254-01

WEST GERMANY

PLZ1 Dr. Guenther Dohrenberg, 1000 Berlin 30, Bayreuther Strasse 3. Tel: (030) 21 38 043-45

PLZ2 Nordelektronik GmbH-KG, 2085 Quickborn, Harksheiderweg 238-240. Tel: (04 106) 4031 Tx: 02 14299

PLZ6 Mansfield GmbH & Co. KG, 6000 Frankfurt, Zobelstrasse 11. Tel: (0611) 4470 20

PLZ7 Astronic GmbH & Co. KG, 7000 Stuttgart-Vaihingen, Gruendgenstrasse 7. Tel: (0711) 734918

PLZ8 Nuemuller & Co. GmbH, 8 Munchen 2, Karlstrasse 55. Tel: 089 5991 231 Tx: 0522106