ENSC 252

Fundamentals of Digital Logic and Design

Calendar Description

Design of digital systems. In particular, students will learn basic digital design concepts including the implementation of synthesizable combinational and sequential logic using HDL and computer based design tools to implement their designs on a FPGA.

Prerequisites: CMPT 128

Workload: ENSC 252 is a 4 credit course

Course Staff

Instructor:

Name: Ameer Abdelhadi
Office: ASB 10827
Email: aabdelha@sfu.ca
Office hours: Fridays @ 3:00 pm – 4:00 pm

Teaching Assistants:

Mubina Sarwar msarwar@sfu.ca
Nasreen Mohsin nmohsin@sfu.ca
Yousra Wakil ywakil@sfu.ca

Scheduled Activities

Lectures:

Monday:	D.100	@ 2:30 pm – 4:20 pm	EDB 7618
Wednesday:	D.100	@ 2:30 pm – 4:20 pm	EDB 7618

Scheduled Laboratory Times:

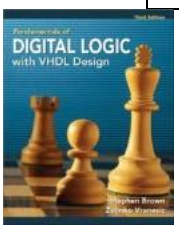
Tuesday:	LA01	@ 11:00 am – 1:20 pm	ASB 10810 / ASB 10808
Tuesday:	LA02	@ 2:30 pm – 4:50 pm	ASB 10810 / ASB 10808
Thursday:	LA03	@ 11:00 am – 1:20 pm	ASB 10810 / ASB 10808
Thursday:	LA04	@ 2:30 pm – 4:50 pm	ASB 10810 / ASB 10808

The Digital Hardware Laboratory has two doors numbered ASB 10810 and ASB 10808. The card reader is associated with ASB 10808. Please enter through this door.

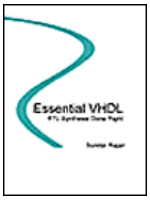
Office Hours:

Friday	@ 3:00 pm – 4:00 pm	ASB 10827

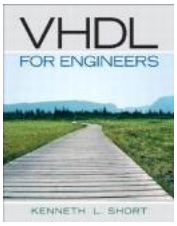
Course Textbooks:



Required: ***Fundamentals of Digital Logic with HVDL Design***,
By Stephen Brown & Zvonko Vranesic,
McGraw Hill, 2009, 3rd Edition,
ISBN: 978-0-07-352953-0 also 978-0-07-722143-0
Call #: TK7888.4.B76 2009



Optional: ***Essential VHDL, RTL synthesis done right***,
By Sundar Rajan,
Barnes & Noble, 1998, 1st Edition
ISBN: 0-9669590-0-0



Optional: ***VHDL for Engineeers***,
By Kenneth L. Short,
Pearson Prentice Hall, 2009, 1st Edition
ISBN: 978-0-13-142478-4
Call #: TK7885.7.S525 2009

Website: SFU Canvas

Software Requirements:

Students will require the use of software circuit design tools. The primary tools will be the integrated FPGA development environment (IDE), ***Quartus Prme***. and the industry standard VHDL simulator, ***ModelSim-Altera***. Fully-functional professional versions are installed in ASB 10808/10.

- Students should download and install the free ***Quartus Prime Lite Edition***, available from the Altera website. (***www.altera.com***)
- Students should download the accompanying DE2-115 CD-ROM (NXP USB) Version 1.0.6 for the DE2-115 Development kit available from (***www.terasic.com***)
- A vector drawing program, ***Visio***, by microsoft, is also available on most computers administered by the school of engineering science. ***Visio*** is extremely easy to use and will be immensely useful in preparing documents for this and future Ensc courses.
- Students may be able to acquire a license for ***Visio*** through the Schools MSDNAA using your DreamSpark Account. Please ask the school of engineering sciences IT services for further information. ensc-help@sfu.ca

Homework:

There will be 11 weekly problem sets and 5 (Pre-Lab) assignments. The problem sets contain questions from the textbook. The assignments contains one or two laborious and challenging tasks. These tasks involve the analysis, and design of complex digital circuits. The circuits will require verification by simulation and should in some cases will be implemented and tested on an FPGA.

Homework assignment are to be submitted to the Canvas LMS as .pdf documents.
Once marked, the files containing annotations and scores are returned to each student using the Canvas LMS.

Labwork:

There are 9 worksheets to be complete within the 2.5 hours scheduled weekly lab periods **and** also during any open-lab hours. The weekly lab worksheets require significant effort and most usually will not be completed within the scheduled lab period. The completed tasks will be checked at the end of the scheduled lab period and all task completed during after the lab period will be checked **at the beginning** of the subsequent lab period.

Some worksheets require preparation before entering the laboratory. Students will work in groups containing three members. The worksheets develop one's ability to design, verify, implement and test digital circuits using industry standard EDA tools and an FPGA. Students are expected to conduct

Midterm Examination:

The Midterm Exam is a formal examination of duration 2 hours, that is held in the lecture hall during the lecture-allocated time. The Midterm Exam will be held on **Monday October 30th 2017** from **2:30 pm – 4:20 pm**. (tentative)

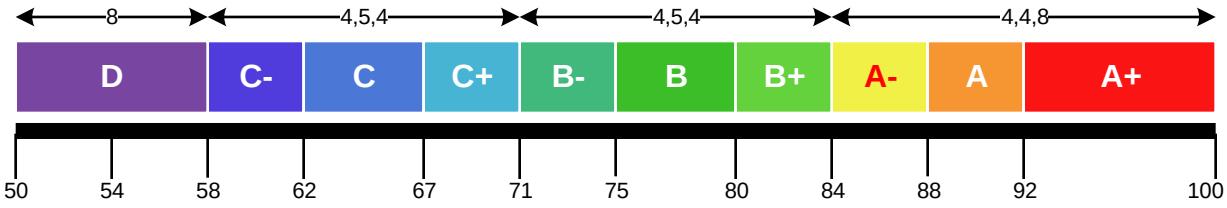
Final Exam:

The Final Exam is a regularly scheduled exam of duration 3 hours. The Exam will be held on **Wednesday December 13th 2017** from **12:00 pm – 3:00 pm**. Further information will be available by **December 1st 2017**.

Note:

The date of the midterm exam is tentative. The course information file will be updated to reflect the actual dates once a decision has been made.

92% – **A+** – 100%	80% – **B+** – 84%	67% – **C+** – 71%
88% – **A** – 92%	75% – **B** – 80%	62% – **C** – 67%
84% – **A–** – 88%	71% – **B–** – 75%	58% – **C–** – 62%
50% – **D** – 58%	00% – **F** – 50%	



Grading:

Students' final grade will be assessed from Homework, Labwork and Exam scores. The exact weighting will be set at the end of the semester however students may find the following tentative proposal useful when assessing one's priorities.

Standard Problems Sets	≈ 10%
In-Lab Worksheets	≈ 15%
Pre-Lab Assignments	≈ 5%
Midterm Exam	≈ 25%
Final Exam	≈ 45%

Academic Integrity:

SFU policy: "*Code of Academic Integrity and Good Conduct*"
http://www.sfu.ca/policies/gazette/student/s10-01.html

Students must be aware that the University and the School of Engineering Science have a zero tolerance for cheating. Students in caught cheating may be subjected to any combination of the following penalties.

- failure in a particular assignment,
- failure in the course,
- a written record on file with the Director of Engineering Science,
- a written record on file with the SFU Registrar's office,
- an FD (Failed for Dishonesty) an annotation on their transcripts,
- suspension/expulsion from the university.

Students should note that the potential benefits of cheating are far outweighed by the potential penalties.