SONY

Semiconductor IC

Data Book 1989

Memory

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Semiconductor Integrated Circuit Data Book 1989

Semiconductor Integrated Circuit Data Book
1989

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PREFACE

This is the 1989 version of the Sony semiconductor IC databook. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

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CXK581020SP CXK581020J	131072 word × 8 bit 45/55ns SRAM (A)	MIX CMOS	137

(P) : Preliminary
(A) : Advance Information

2) ASM (Application Specific Memory)

Type	Function	Process	Page
CXK7701J	8192 word × 16 bit 4096 word × 16 bit × 2 way High-speed latched cache-SRAM (P)	MIX CMOS	141

2. Cross Reference Guide (1)

Density	Organization	Product name		Access time ns	Package	Other Major Suppliers						
						Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu
16K	2K×8	CXK5816PN	-10L -12L -15L	100 120 150	24 pin 600mil DIP	HM6116AP						
		CXK5816M	-10L -12L -15L	100 120 150	24 pin 450mil SOP	HM6116AFP						
64K	64K×1	CXK5164P	-25 -30 -35	25 30 35	22 pin 300mil DIP	HM6787P	TC5562P	M5M5187AP	CY7C187	IDT7187	MT5C6401	MB81C71A
		CXK5164J	-25 -30 -35	25 30 35	24 pin 300mil SOJ		TC5562J	M5M5187AJ			MT5C6401DJ	MB81C71A
	16K×4	CXK5464AP	-25 -30 -35	25 30 35	22 pin 300mil DIP	HM6788P	TC55416P	M5M5188AP	CY7C164	IDT7188	MT5C6404	MB81C74
		CXK5464AJ	-25 -30 -35	25 30 35	24 pin 300mil SOJ			M5M5188AJ			MT5C6404DJ	
		CXK5465P	-25 -30 -35	25 30 35	24 pin 300mil DIP	HM6789P	TC55417P	M5M5189AP	CY7C166	IDT6198		MB81C75
		CXK5465J	-25 -30 -35	25 30 35	24 pin 300mil SOJ		TC55417J 5M5189AJ	CY7C166				
	8K×8	CXK5863AP	-20 -25	20 25	28 pin 300mil DIP		TC5588P		CX7C185	IDT7164	MT5C6408	
		CXK5863AJ	-20 -25	20 25	28 pin 300mil SOJ		TC5588J		CX7C185		MT5C6408DJ	
		CXK5863P	-25 -30 -35	25 30 35	28 pin 300mil DIP		TC5588P		CY7C185	IDT7164	MT5C6408	MB81C78A
		CXK5863M	-25 -30 -35	25 30 35	28 pin 450mil SOP							
		CXK5863J	-25 -30 -35	25 30 35	28 pin 300mil SOJ		TC5588J		CY7C185		MT5C6408DJ	
		CXK5864BP	-70L -10L -12L	70 100 120	28 pin 600mil DIP	HM6264AP	TC5563AP	M5M5165P				MB8464A
		CXK5864BSP	-70L -10L -12L	70 100 120	28 pin 300mil DIP	HM6264ASP						
		CXK5864BM	-70L -10L -12L	70 100 120	28 pin 450mil SOP	HM6264AFP	TC5563AF	M5M5165FP				MB8464A

Cross Reference Guide (2)

Density	Organization	Product name	Access time ns	Package	Other Major Suppliers						
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu
72K	8K×9	CXK5971P -25 -30 -35	25 30 35	28 pin 300mil DIP		TC5589P					MB81C79A
		CXK5971J -25 -30 -35	25 30 35	28 pin 300mil SOJ		TC5589J					
256K	256K×1	CXK51256P -35 -45 -55	35 45 55	24 pin 300mil DIP	HM6207		M5M5257P	CY7C197	IDT71257	MT5C2561	
	64K×4	CXK54256P -35 -45 -55	35 45 55	24 pin 300mil DIP	HM6208		M5M5258P	CY7C194	IDT71258	MT5C2564	MB81C86
	32K×8	CXK58255AP -25 -30	25 30	28 pin 300mil DIP							MB8287
		CXK58255AJ -25 -30	25 30	28 pin 300mil SOJ							
		CXK58258P -35 -45 -55	35 45 55	28 pin 600mil DIP				CY7C198	IDT71256	MT5C2568W	
		CXK58258SP -35 -45 -55	35 45 55	28 pin 300mil DIP				CY7C199		MT5C2568	
		CXK58257P -70L -85L -10L -12L	70 85 100 120	28 pin 600mil DIP	HM62256P	TC55257 AP	M5M255P				MB84256
		CXK58257SP -70L -85L -10L -12L	70 85 100 120	28 pin 300mil DIP							
		CXK58257M -70L -85L -10L -12L	70 85 100 120	28 pin 450mil DIP	HM62256FP	TC55257 AF	M5M255FP				MB84256
1M	128K×8	CXK581020SP -45 -55	45 55	32 pin 400mil DIP							
		CXK581020J -45 -55	45 55	32 pin 400mil SOJ							
		CXK581001P -70L -85L	70 85	32 pin 600mil DIP	HM628128P	TC551001P	M5M51008P				
		CXK581001M -70L -85L	70 85	32 pin 525mil SOP	HM628128FP		M5M51008FP				
		CXK581000P -10L -12L -15L	100 120 150	32 pin 600mil DIP	HM628128P	TC551001P	M5M51008P				
		CXK581000M -10L -12L -15L	100 120 150	32 pin 525mil SOP	HM628128FP		M5M51008FP				
128K	4K×16×2way 8K×16	CXK7701J -30 -35 -45 -55	30 35 45 55	52 pin PLCC	CY7C184 (Cypress) V63C 328 (Vitelic)					MT56C2416EJ	

3. SRAM Product Over View

Density	Organization	Product name		Speed (ns)	Package	Process	Page
16K	2K×8	CXK5816PN	-10 L	100	24pin	MIX CMOS	
			-12 L	120	600mil DIP		
			-15 L	150			
		CXK5816M	-10 L	100	24pin	MIX CMOS	
			-12 L	120	450mil SOP		
			-15 L	150			
64K	64K×1	CXK5164P	-25	25	22pin	MIX CMOS	
			-30	30	300mil DIP		
			-35	35			
		CXK5164J	-25	25	24pin	MIX CMOS	
			-30	30	300mil SOJ		
			-35	35			
	16K×4	CXK5464AP	-25	25	22pin	MIX CMOS	
			-30	30	300mil DIP		
			-35	35			
		CXK5464AJ	-25	25	24pin	MIX CMOS	
			-30	30	300mil SOJ		
			-35	35			
		CXK5465P	-25	25	24pin	MIX CMOS	
			-30	30	300mil DIP		
			-35	35			
		CXK5465J	-25	25	24pin	MIX CMOS	
			-30	30	300mil SOJ		
			-35	35			
	8K×8	CXK5863AP	-20	20	28pin	FULL CMOS	
			-25	25	300mil DIP		
		CXK5863AJ	-20	20	28pin	FULL CMOS	
			-25	25	300mil SOJ		
		CXK5863P	-25	25	28pin	FULL CMOS	
			-30	30	300mil DIP		
			-35	35			
		CXK5863M	-25	25	28pin	FULL CMOS	
			-30	30	450mil SOP		
			-35	35			
		CXK5863J	-25	25	28pin	FULL CMOS	
			-30	30	300mil SOJ		
			-35	35			
		CXK5864BP	-70 L	70	28pin	MIX CMOS	
			-10 L	100	600mil DIP		
			-12 L	120			
		CXK5864BSP	-70 L	70	28pin	MIX CMOS	
			-10 L	100	300mil DIP		
			-12 L	120			
		CXK5864BM	-70 L	70	28pin	MIX CMOS	
			-10 L	100	450mil SOP		
			-12 L	120			

Density	Organization	Product name		Speed (ns)	Package	Process	Page
72K	8K×9	CXK5971P	-25	25	28pin	FULL CMOS	
			-30	30	300mil DIP		
			-35	35			
		CXK5971J	-25	25	28pin	FULL CMOS	
			-30	30	300mil SOJ		
			-35	35			
256K	256K×1	CXK51256P	-35	35	24pin	MIX CMOS	
			-45	45	300mil DIP		
			-55	55			
	64K×4	CXK54256P	-35	35	24pin	MIX CMOS	
			-45	45	300mil DIP		
			-55	55			
	32K×8	CXK58255AP	-25	25	28pin	FULL CMOS	
			-30	30	300mil DIP		
		CXK58255AJ	-25	25	28pin	FULL CMOS	
			-30	30	300mil SOJ		
		CXK58258P	-35	35	28pin	MIX CMOS	
			-45	45	600mil DIP		
			-55	55			
		CXK58258SP	-35	35	28pin	MIX CMOS	
			-45	45	300mil DIP		
			-55	55			
		CXK58257P	-70L	70	28pin	MIX CMOS	
			-85L	85	600mil DIP		
			-10L	100			
			-12L	120			
		CXK58257SP	-70L	70	28pin	MIX CMOS	
			-85L	85	300mil DIP		
			-10L	100			
			-12L	120			
		CXK58257M	-70L	70	28pin	MIX CMOS	
			-85L	85	450mil SOP		
			-10L	100			
			-12L	120			
1M	128K×8	CXK581020SP	-45	45	32pin	MIX CMOS	
			-55	55	400mil DIP		
		CXK581020J	-45	45	32pin	MIX CMOS	
			-55	55	400mil SOJ		
		CXK581001P	-70L	70	32pin	MIX CMOS	
			-85L	85	600mil DIP		
		CXK581001M	-70L	70	32pin	MIX CMOS	
			-85L	85	525mil SOP		
		CXK581000P	-10L	100	32pin	MIX CMOS	
			-12L	120	600mil DIP		
			-15L	150			
		CXK581000M	-10L	100	32pin	MIX CMOS	
			-12L	120	525mil SOP		
			-15L	150			
128K	4K×16×2WAY 8K×16	*CXK7701J	-30	30	52pin PLCC	MIX CMOS	
			-35	35			
			-45	45			
			-55	55			

*Application Specific Memory (ASM)

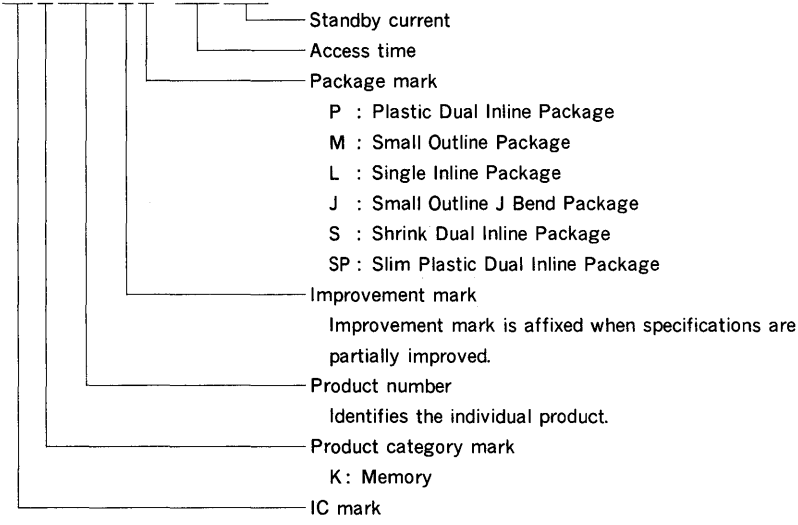
4. IC Nomenclature

Nomenclature of SRAM product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

SRAM Nomenclature

[Example] CX K 5464 A P—□□ □□



5. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

Maximum rating must never be reached for any TWO items at the SAME time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit; the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with the amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta = 25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

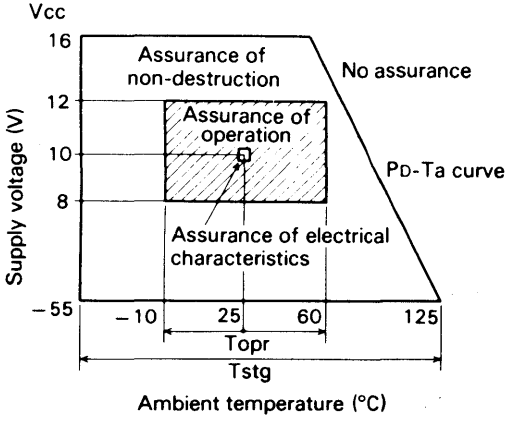
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; that is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

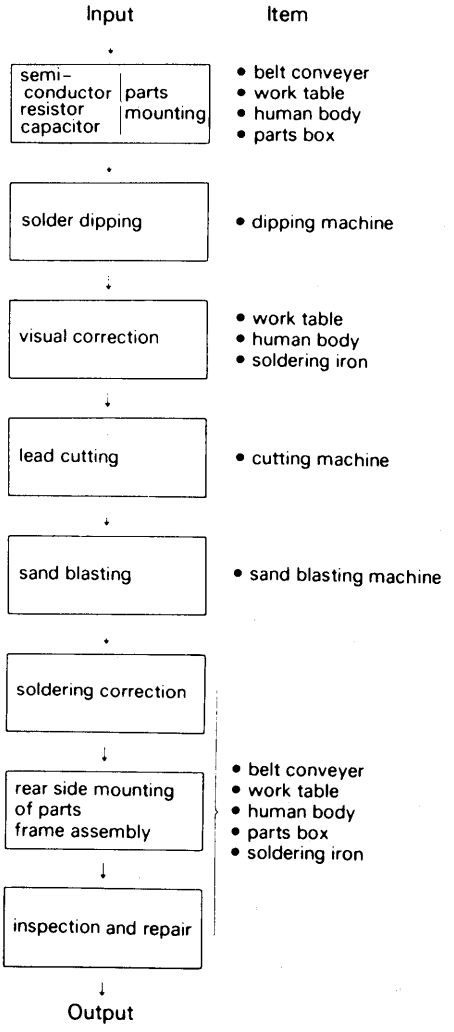
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

① Equalize potentials of terminals when transporting or storing.

② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③ Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room to about 50%.

Operator

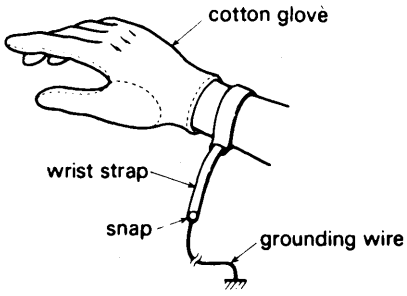
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling any semiconductor device.

example of grounding band

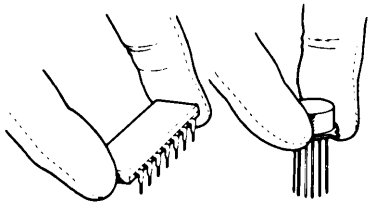


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

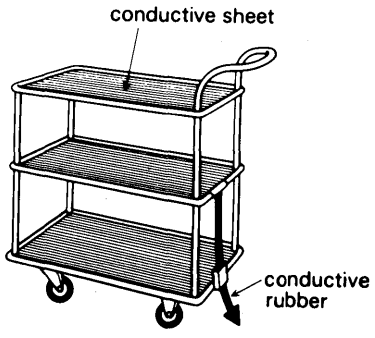
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

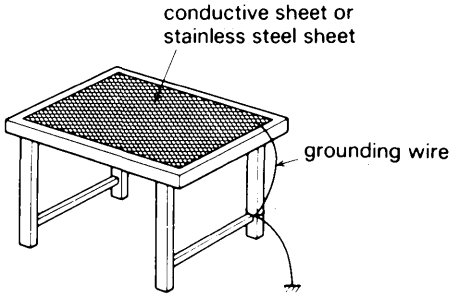
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

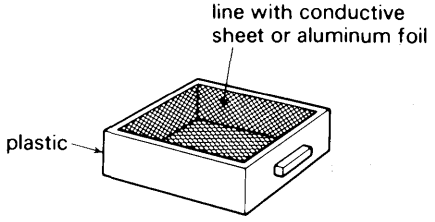
grounding of work table



(3) Semiconductor device case

Use a metal case, or an antistatic plastic case (lined with conductive sheet or aluminum foil).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or on a wood or on a metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

(6) Other points of caution

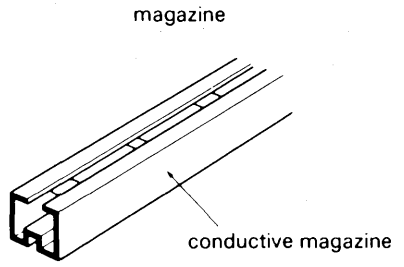
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

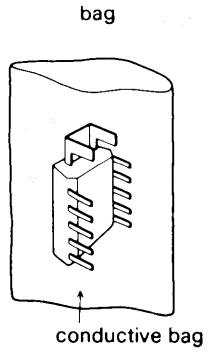
Use metal, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

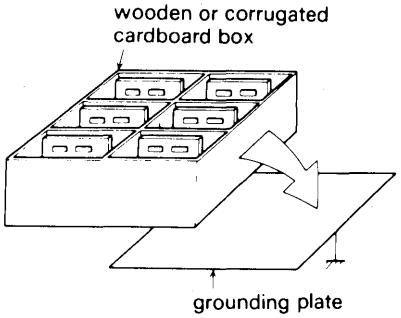
Use a conductive bag to store ICs. If the use of a vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



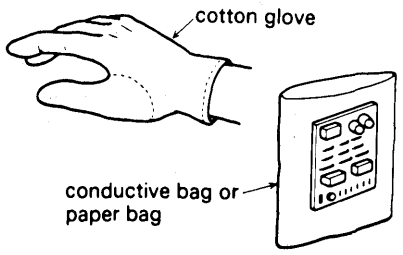
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10 MΩ (DC 500V). after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

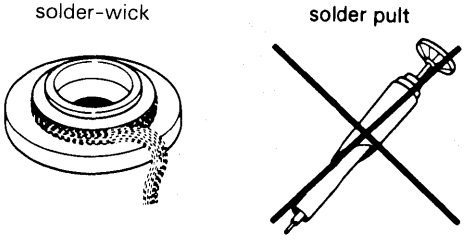
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

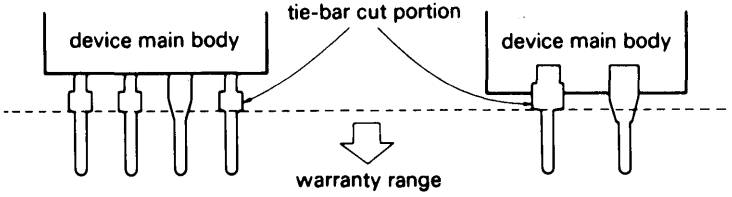
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which has been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{-0}$ seconds in a solder bath of 350°C ±10°C, for a distance of up to 1 to 1.5 mm from the main body.

  For the solder flow system temperature should be 260 °C ±5 °C. To solder by soldering iron temperature should be 350 °C ±10 °C.
- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260 °C ±5 °C. The distance between the device main body and solder bath is 1.6 mm.

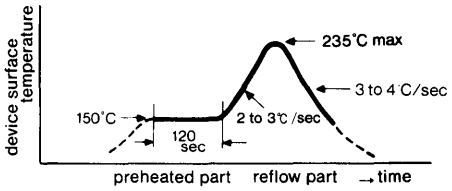
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



6. Quality Assurance and Reliability

Sony's Policy of Quality Assurance

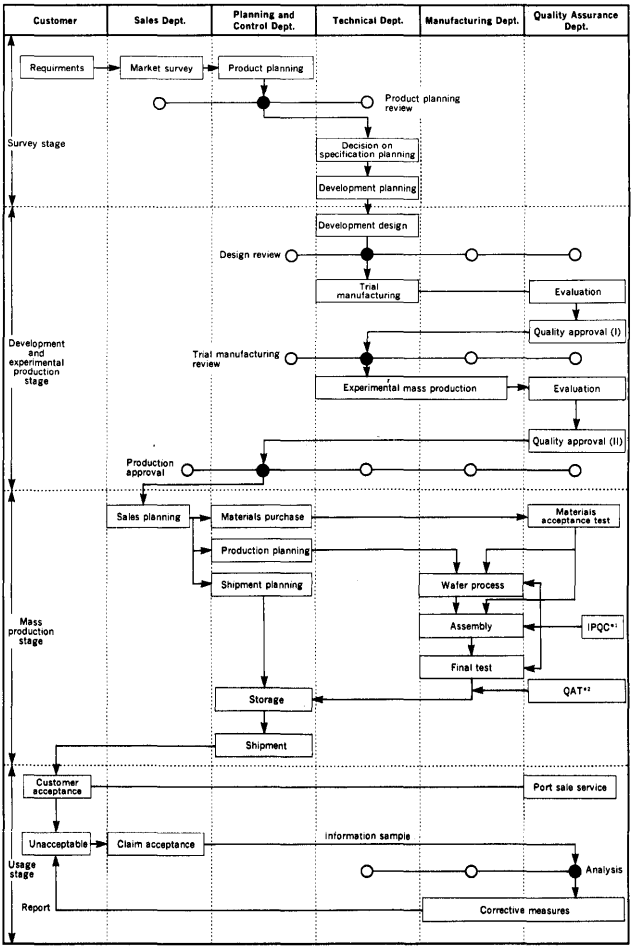
The Sony semiconductor embodies two fundamental ideas: "highest quality" and "lowest cost". These are the two key points for realizing such ideas.

One is the "quality" of men fabricating the semiconductor devices. The reliability of these people is reflected in the Sony products. Accordingly, Sony is making a continuous effort to raise the "quality" of people capable of manufacturing and fabricating Sony semiconductor devices.

The other point is a source management system combined with the concept of thorough quality design. With this system, higher quality products can be steadily manufactured through automation of device design, process design, and the fabrication process.

Sony is making constant efforts to supply the most economical and most useful products of very high quality to users.

Quality assurance system of semiconductor products



Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature storage	up to 1000 h	10%
	low temperature storage	up to 1000 h	10%
	high temperature and high humidity storage	up to 1000 h	10%
	high temperature with bias	up to 1000 h	10%
	high temperature and high humidity with bias	up to 500 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	10 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and Inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

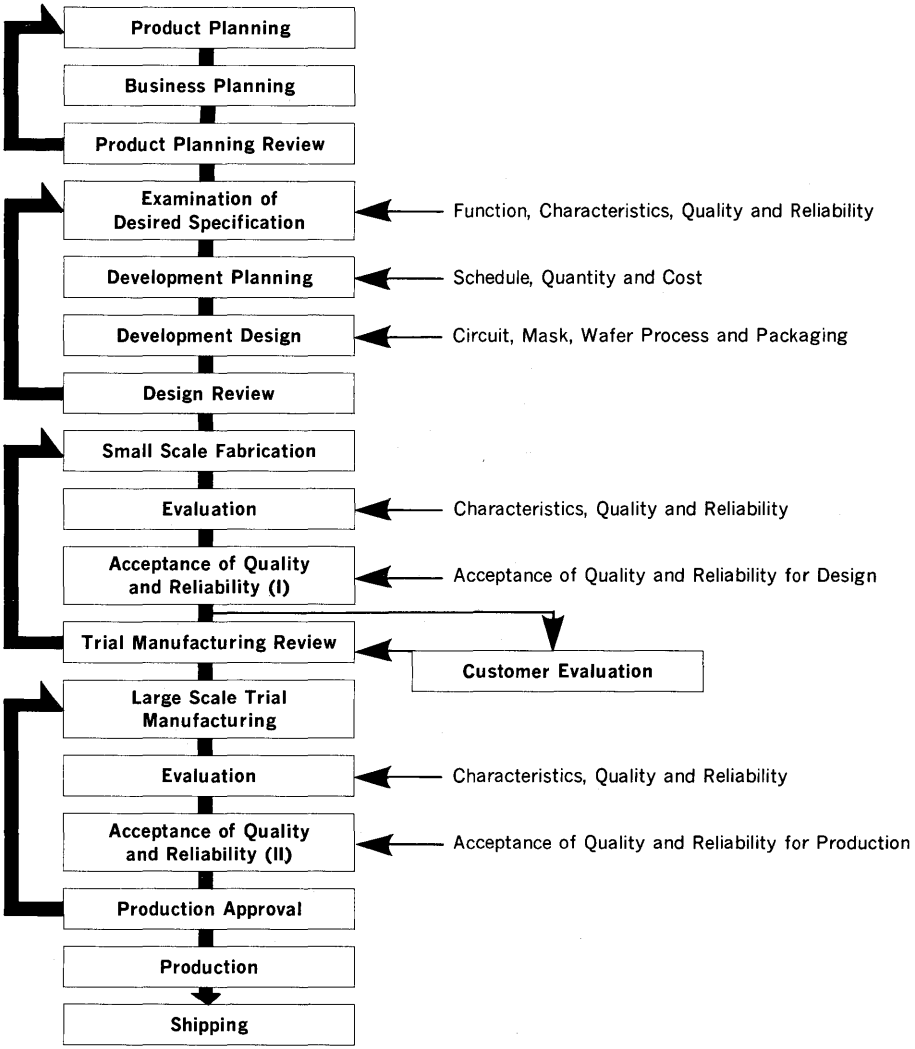
Reliability Test Standards for Acceptance of Products

Item	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical (1h on/3h off)	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		5c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

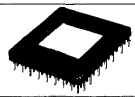
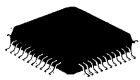
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

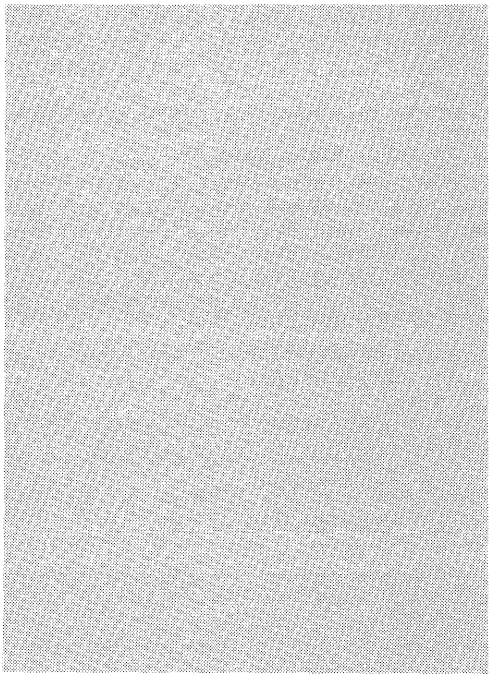
Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



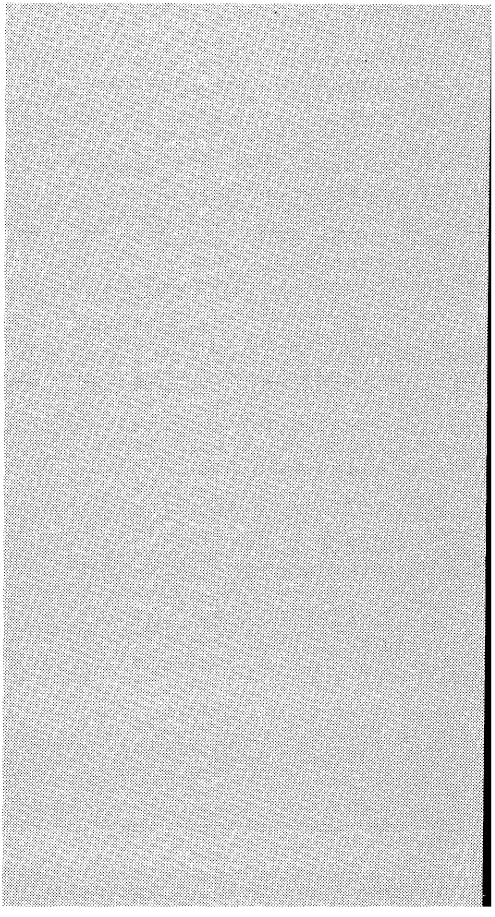
7. Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		L C C	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic



Static RAM



1) Static RAM

Type	Function	Process	Page
CXK5816PN CXK5816M	2048 word × 8 bit 100/120/150ns SRAM	MIX CMOS	27
CXK5864BP CXK5864BSP CXK5864BM	8192 word × 8 bit 70/100/120ns SRAM	MIX CMOS	35
CXK5863P CXK5863M CXK5863J	8192 word × 8 bit 25/30/35ns SRAM	FULL CMOS	44
CXK5863AP CXK5863AJ	8192 word × 8 bit 20/25/ns SRAM	FULL CMOS	'54
CXK5464AP CXK5464AJ	16384 word × 4 bit 25/30/35ns SRAM	MIX CMOS	55
CXK5465P CXK5465J	16384 word × 4 bit 25/30/35ns SRAM, with $\overline{OE}$	MIX CMOS	62
CXK5164P CXK5164J	65536 word × 1 bit 25/30/35ns SRAM	MIX CMOS	69
CXK5971P CXK5971J	8192 word × 9 bit 25/30/35ns SRAM	FULL CMOS	76
CXK58257P CXK58257SP CXK58257M	32768 word × 8 bit 70/85/100/120 SRAM	MIX CMOS	86
CXK58258P CXK58258SP	32768 word × 8 bit 35/45/55ns SRAM	MIX CMOS	94
CXK58255AP CXK58255AJ	32768 word × 8 bit 25/30ns SRAM (P)	FULL CMOS	102
CXK54256P	65536 word × 4 bit 35/45/55ns SRAM	MIX CMOS	108
CXK51256P	262144 word × 1 bit 35/45/55ns SRAM	MIX CMOS	115
CXK581000P CXK581000M	131072 word × 8 bit 100/120/150ns SRAM (P)	MIX CMOS	123
CXK581001P CXK581001M	131072 word × 8 bit 70/85ns SRAM (P)	MIX CMOS	130
CXK581020SP CXK581020J	131072 word × 8 bit 45/55ns SRAM (A)	MIX CMOS	137

(P) : Preliminary
(A) : Advance Information

SONY CXK5816PN/M

10/10L/12/
12L/15/15L

2048-word × 8 bit High Speed CMOS Static RAM

Description

CXK5816PN/M is a 16,384 bits high speed CMOS static RAM organized as 2,048 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power spplications in which battery back up for nonvolatility is required.

Features

- High speed operation (Access time)
  - CXK5816PN/M -10, 10L 100ns (Max.)
  - CXK5816PN/M -12, 12L 120ns (Max.)
  - CXK5816PN/M -15, 15L 150ns (Max.)
- Low power consumption (Standby) (Operation)
  - CXK5816PN/M -10, 12, 15 100μW(Typ.) 125mW(Typ.)
  - CXK5816PN/M -10L, 12L, 15L 5μW(Typ.) 125mW(Typ.)
- Single +5V supply: 5V±10%.
- Fully static memory ..... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)

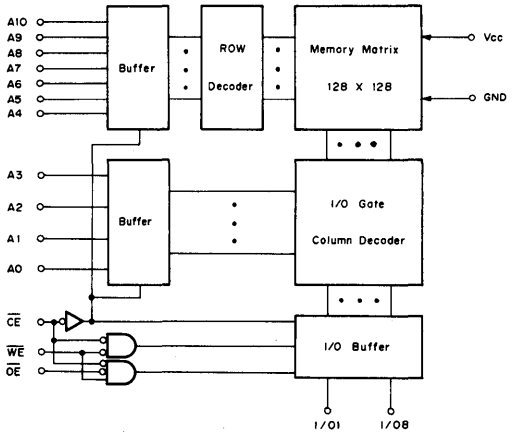
Function

2048-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

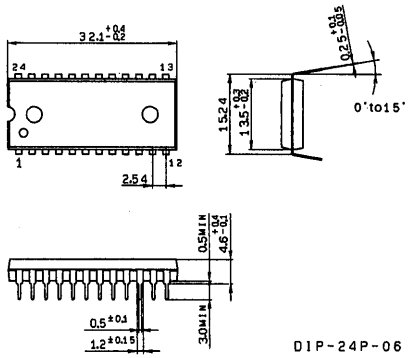
Block Diagram



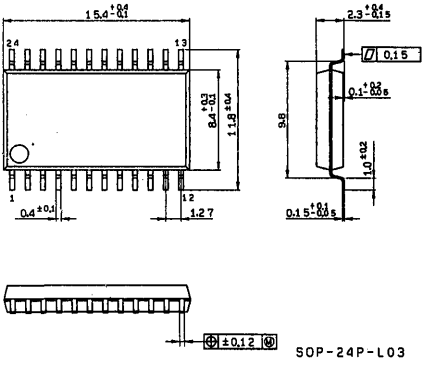
Package Outline

Unit: mm

CXK5816PN 24 Pin DIP (Plastic)



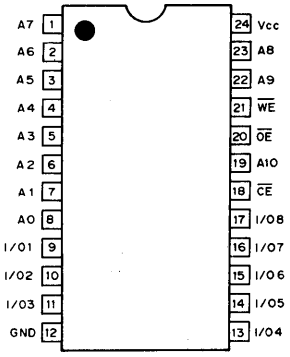
CXK5816M 24 Pin SOP (Plastic)



Note) All Typical values are measured under the conditions Vcc=5.0V and Ta=25°C.

50846C-ST

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A10	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings

Ta=25℃, GND=0V

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5* to +7.0	V
Input voltage	V_{IN}		−0.5* to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		−0.5* to Vcc+0.5	V
Allowable power dissipation	P_D	CXK5816PN/SP	1.0	W
		CXK5816M	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260•10	°C • sec

* V_{CC}, V_{IN} $V_{I/O}$ Minimum value=−3.0V, Pulse width is under 50 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	D out	I_{CC1}, I_{CC2}
L	X	L	Write	D in	I_{CC1}, I_{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to +70°C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3	—	0.8	V

DC and Operating Characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5816PN/M/SP −10/12/15			CXK5816PN/M/SP −10L/12L/15L			Unit
			Min.	Typ.**	Max.	Min.	Typ.**	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−2	—	2	−2	—	2	μA
Output leakage current	I_{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	−2	—	2	−2	—	2	μA
Operating power supply current	I_{CC1}	$\overline{CE}=V_{IL}$, I_{OUT} = 0mA	—	25	60	—	25	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100% I_{OUT} = 0mA	—	28 *(31)	60 *(75)	—	28 *(31)	60 *(75)	mA
Standby current	I_{SB1}	$\overline{CE}\geqq V_{CC}-0.2V$	—	0.02	1.0	—	0.001	0.05	mA
	I_{SB2}	$\overline{CE}=V_{IH}$	—	0.3	2	—	0.2	1	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 4.0mA	—	—	0.4	—	—	0.4	V

* **Note)** Shows CXK5816PN/M/SP-10, 10L value.

** V_{CC}=5V, Ta=25°C

Capacitance

Ta=25°C, f=1 MHz

Item	Test condition	Symbol	Min.	Max.	Unit
Input capacitance	V_{IN}=0V	C_{IN}	—	7	pF
Input/output capacitance	$V_{I/O}$=0V	$C_{I/O}$	—	10	pF

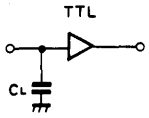
Note) This parameter is sampled and is not 100% tested.

AC Operating Characteristics

- **AC test condition**

V_{CC} = 5V ± 10%, Ta = 0 to +70°C

Item	Condition
Input pulse high level	V_{IH} = 2.4V
Input pulse low level	V_{IL} = 0.6V
Input rise time	t_R = 5ns
Input fall time	t_F = 5ns
Input and output timing reference level	1.5V
Output load	C_L* = 100pF, 1TTL



* C_L includes scope and jig capacitance.

• **Read cycle**

Item	Symbol	CXK5816PN/M -10/10L		CXK5816PN/M -12/12L		CXK5816PN/M -15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time	t_{CO}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	55	—	60	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	15	—	15	—	15	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	10	—	10	—	10	—	ns
Chip disable to output in high Z ($\overline{CE}$)	*t_{HZ}	0	30	0	40	0	50	ns
Output disable to output in high Z ($\overline{OE}$)	*t_{OHZ}	0	30	0	40	0	50	ns

*** Note)** t_{HZ} and t_{OHZ} are specified by the time length until the output circuit is turned off and not specified by the output voltage level.

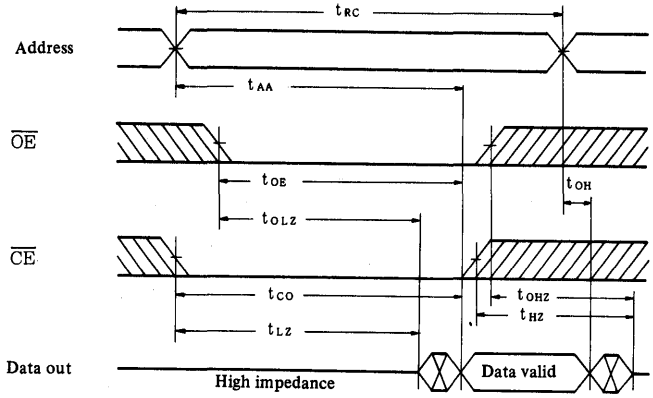
• **Write cycle**

Item	Symbol	CXK5816PN/M -10/10L		CXK5816PN/M -12/12L		CXK5816PN/M -15/15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	80	—	100	—	120	—	ns
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	60	—	75	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	5	—	5	—	5	—	ns
Output active from end of write	t_{OW}	15	—	15	—	15	—	ns
Write to output in high Z	t_{WHZ}*	0	30	0	40	0	50	ns

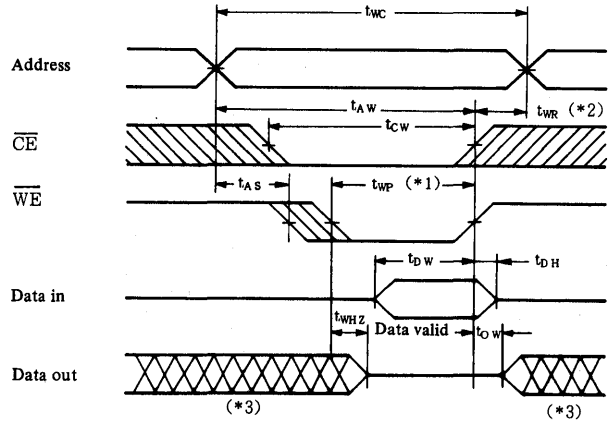
*** Note)** t_{WHZ} is specified by the time length until the output circuit is turned off and not specified by the output voltage level.
level.

Timing Waveform

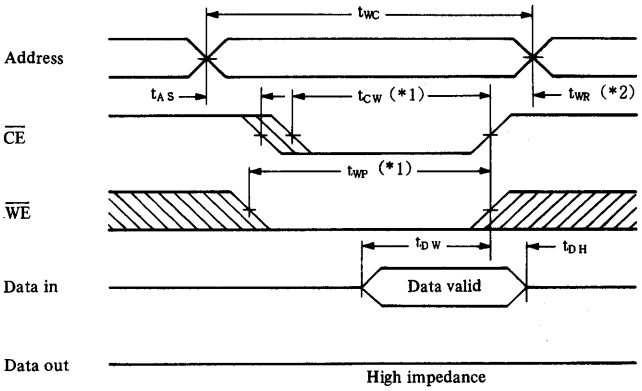
(1) **Read Cycle [$\overline{WE}$=V_{IH}]**



(2) **Write Cycle (1): $\overline{WE}$ Control [$\overline{OE}$=V_{IH}]**



Write Cycle (2): $\overline{CE}$ Control [$\overline{OE}$=V_{IL}]



Note)

*1 A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
*2 t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
*3 During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

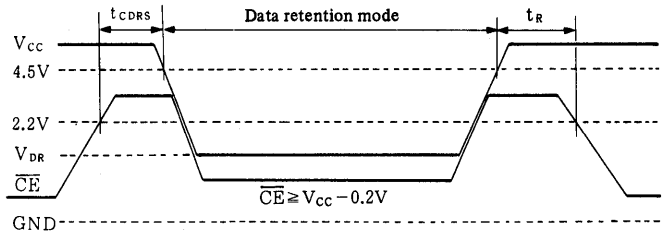
Data Retention Characteristics

Ta = 0 to +70°C

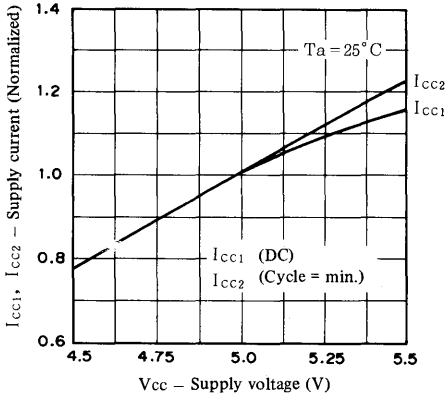
Item	Symbol	Test condition	CXK5816PN/M -10/12/15			CXK5816PN/M -10L/12L/15L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$	2.0	5.0	5.5	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE} \geqq 2.8V$	—	12	600	—	0.6	30	μA
	I_{CCDR2}	V_{CC}=2.0 to 5.5V, $\overline{CE} \geqq V_{CC}-0.2V$	—	20	1000	—	1.0	50	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		t_{RC}*	—	—	t_{RC}*	—	—	ns

* t_{RC} : Read cycle time

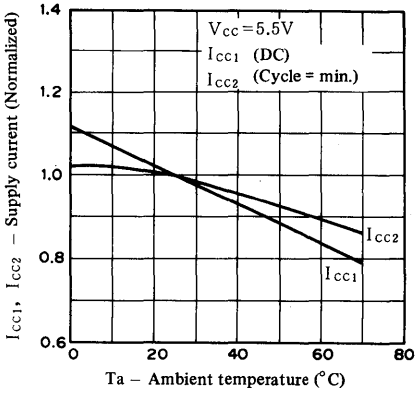
Data Retention Waveform



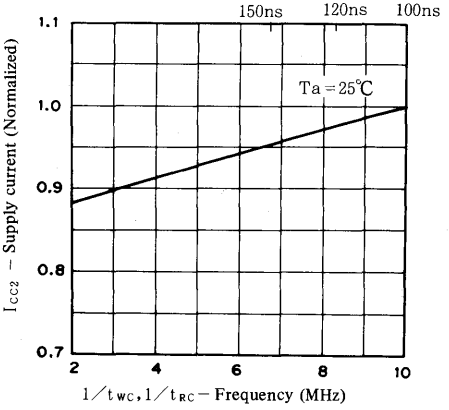
Supply current vs. Supply voltage



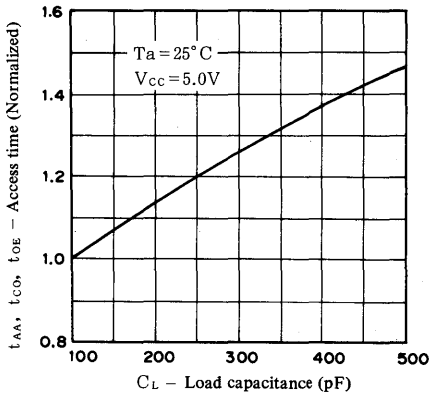
Supply current vs. Ambient temperature



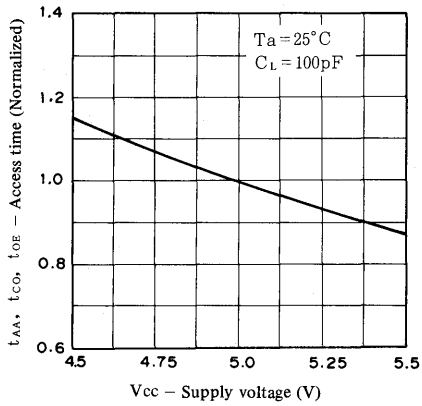
Supply current vs. Frequency



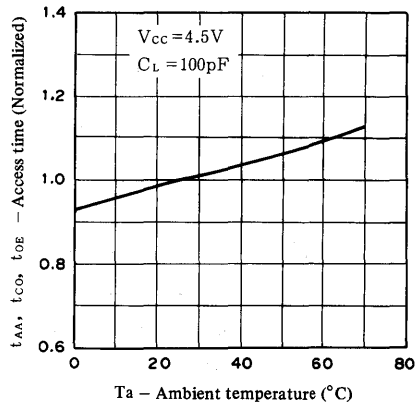
Access time vs. Load capacitance



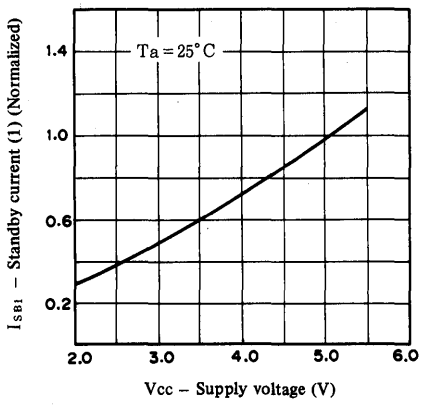
Access time vs. Supply voltage



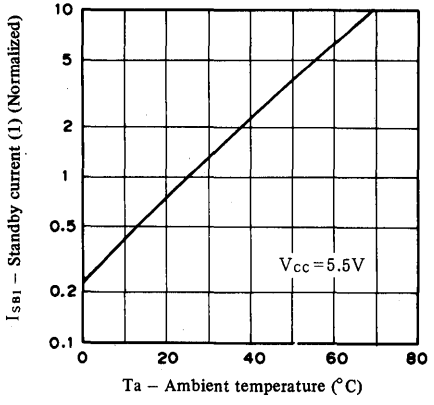
Access time vs. Ambient temperature



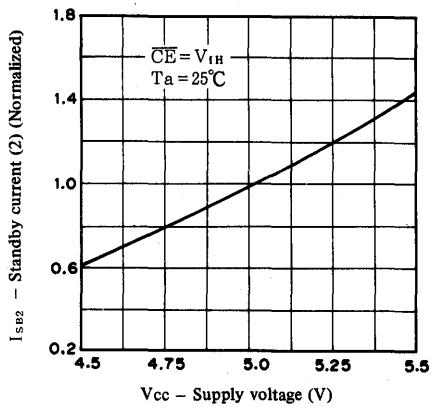
Standby current (1) vs. Supply voltage



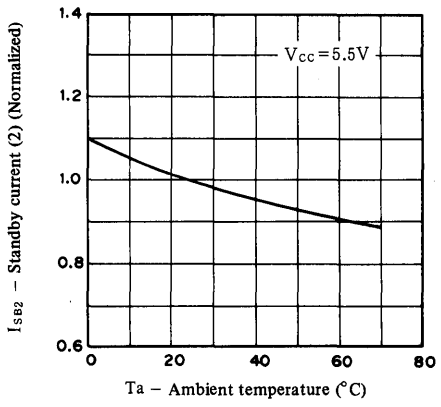
Standby current (1) vs. Ambient temperature



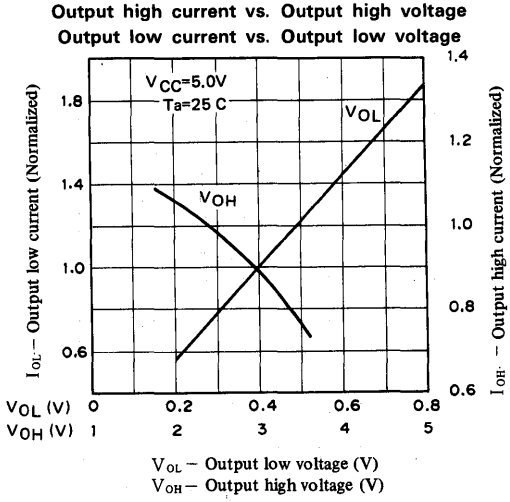
Standby current (2) vs. Supply voltage



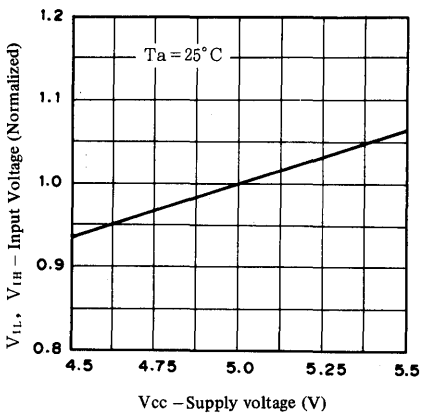
Standby current (2) vs. Ambient temperature



Output high current vs. Output high voltage
Output low current vs. Output low voltage



Input voltage vs. Supply voltage



8,192 words × 8 bit High Speed CMOS Static RAM

Description

CXK5864BP/BSP/BM is a 65,536 bits high speed CMOS static RAM organized as 8,192 words by 8 bits and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
  CXK5864BP/BSP/BM-70L, 70LL 70ns(Max.)
  CXK5864BP/BSP/BM-10L, 10LL 100ns(Max.)
  CXK5864BP/BSP/BM-12L, 12LL 120ns(Max.)
- Low power operation:
  CXK5864BP/BSP/BM-70LL, 10LL, 12LL;
  Standby/Operation: 5 μW (Typ.)/40 mW (Typ.)
  CXK5864BP/BSP/BM-70L, 10L, 12L;
  Standby/Operation: 10 μW (Typ.)/40 mW (Typ.)
- Single power supply 5V: +5V ±10%
- Fully static memory . . . No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28pin 600-mil DIP, 300-mil DIP and 450-mil SOP

Function

- 8192-word × 8 bit static RAM

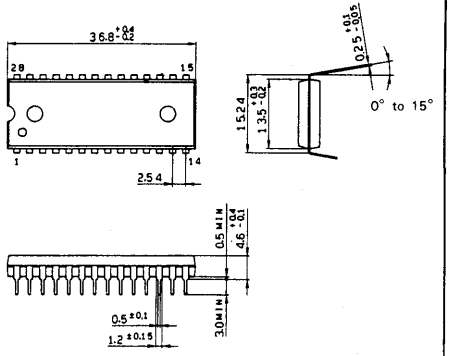
Structure

Silicon gate CMOS IC

Package Outline

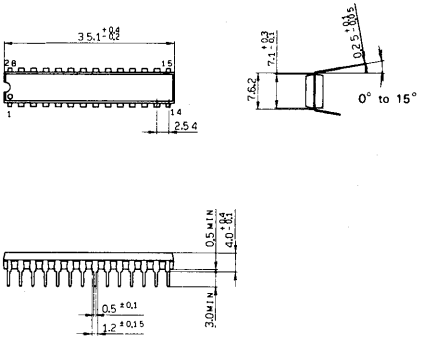
Unit: mm

CXK5864BP 28pin DIP (Plastic) [600-mil]



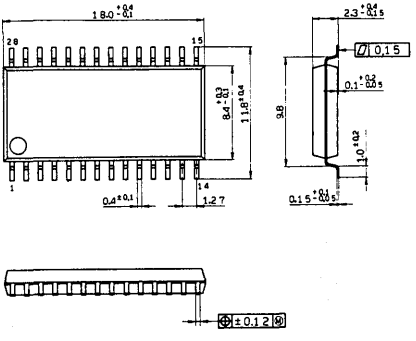
DIP-28P-04

CXK5864BSP 28pin DIP (Plastic) [300-mil]



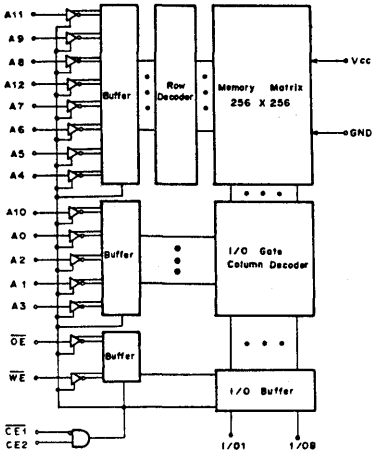
DIP-28P-06

CXK5864BM 28pin SOP (Plastic) [450-mil]

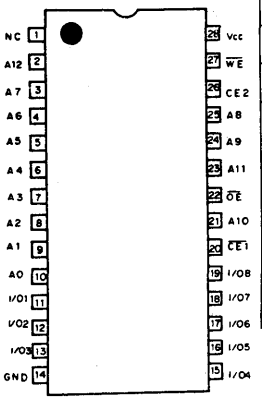


SOP-28P-L05

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	Vcc		−0.5 to +7.0	V
Input voltage	VIN		−0.5* to Vcc+0.5	V
Input and output voltage	VI/O		−0.5* to Vcc+0.5	V
Allowable power dissipation	PD	CXK5864BP/BSP	1.0	W
		CXK5864BM	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260·10	°C·sec

***Note)** VIN, VI/O=−3.0V Min. for pulse width less than 50 ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	X	Not selected	High Z	ISB1, ISB2
X	L	X	X	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	ICC1, ICC2
L	H	L	H	Read	Data output	ICC1, ICC2
H	L	X	L	Write	Data input	ICC1, ICC2

Note) X: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	VIH	2.2	–	Vcc+0.3	V
Input low voltage	VIL	−0.3*	–	0.8	V

***Note)** VIL=−3.0V Min. for pulse width less than 50 ns.

Electrical Characteristics

DC characteristics

(V_{CC}=5V±10%, GND=0V, Ta=0 to+70°C)

Item	Symbol	Test condition		CXK5864BP/BSP/BM −70L/10L/12L −70LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}		−500	–	500	nA
Output leakage current	I_{LO}	$V_{I/O}$=GND to V_{CC} CE1=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}		−500	–	500	nA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		–	8	15	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA		–	30	50	mA
Standby current	I_{SB1}	CE2≦0.2V or $\overline{CE1}$≧V_{CC}−0.2V CE2≧V_{CC}−0.2V	−L	–	2	60	μA
			−LL	–	1	30	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		–	0.1	2	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.4	–	–	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		–	–	0.4	V

***Note)** V_{CC}=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	–	7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	7	pF

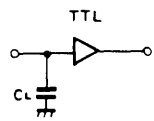
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• **AC test conditions** (V_{CC}=5V±10%, Ta=0 to +70°C)

Item		Condition
Input pulse high level		V_{IH}=2.2V
Input pulse low level		V_{IL}=0.8V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load	10L/10LL/12L/12LL	C_L*=100pF, 1TTL
	70L/70LL	C_L*=30pF, 1TTL

• **Test circuit**



* C_L includes scope and jig capacitances.

• **Read cycle**

Item	Symbol	CXK5864 BP/BSP/BM −70L/70LL		CXK5864 BP/BSP/BM −10L/10LL		CXK5864 BP/BSP/BM −12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	–	100	–	120	–	ns
Address access time	t_{AA}	–	70	–	100	–	120	ns
Chip enable access time ($\overline{CE1}$, CE2)	t_{CO1}, t_{CO2}	–	70	–	100	–	120	ns
Output enable to output valid	t_{OE}	–	35	–	50	–	60	ns
Output hold from address change	t_{OH}	10	–	10	–	10	–	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	–	10	–	10	–	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	–	5	–	5	–	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}* t_{HZ2}*	0	30	0	35	0	45	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	35	0	45	ns

***Note)** t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

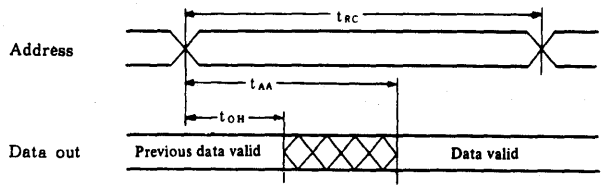
• **Write cycle**

Item	Symbol	CXK5864 BP/BSP/BM −70L/70LL		CXK5864 BP/BSP/BM −10L/10LL		CXK5864 BP/BSP/BM −12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	–	100	–	120	–	ns
Address valid to end of write	t_{AW}	60	–	80	–	85	–	ns
Chip enable to end of write	t_{CW}	60	–	80	–	85	–	ns
Data to write time overlap	t_{DW}	30	–	35	–	50	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	40	–	60	–	70	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	–	0	–	0	–	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	–	0	–	0	–	ns
Output active from end of write	t_{OW}	5	–	5	–	5	–	ns
Write to output in high Z	t_{WHZ}*	0	30	0	35	0	45	ns

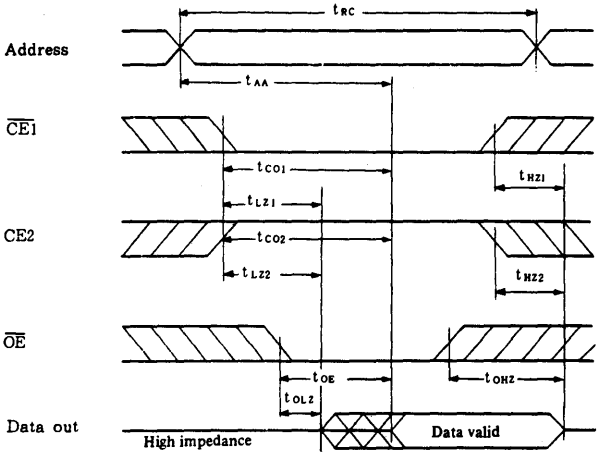
***Note)** t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

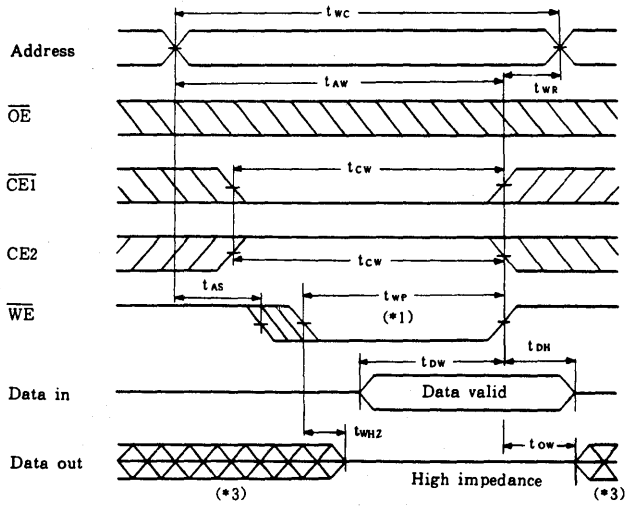
- Read cycle (1): $\overline{CE1}$=OE=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



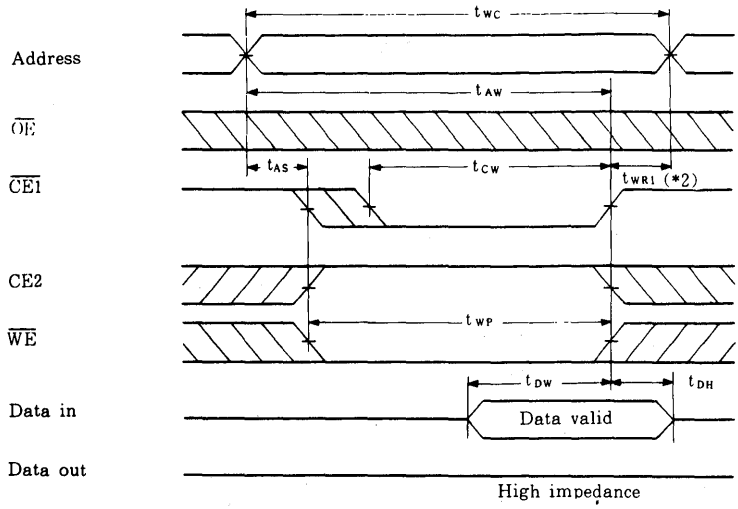
- Read cycle (2): $\overline{WE}$=V_{IH}



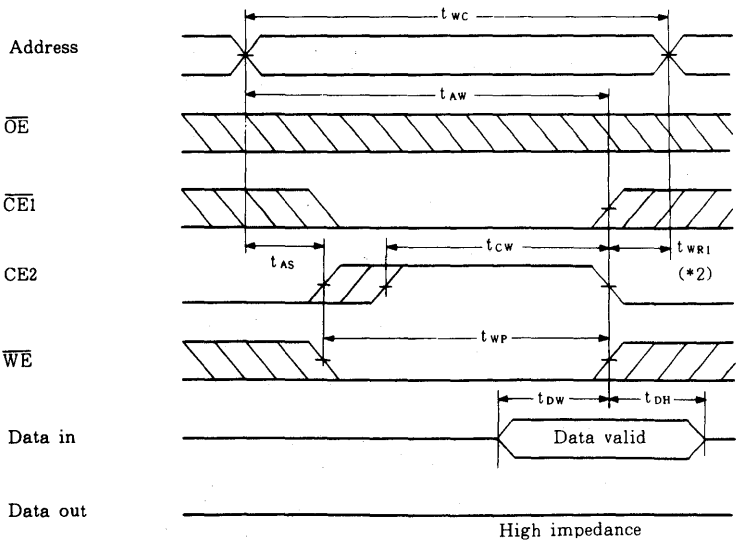
- Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): CE2 control



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at Low and CE2 is at high simultaneously.

*2. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write circle.

*3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

Data Retention Characteristics

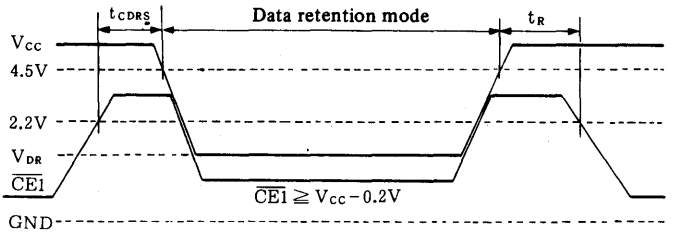
(Ta=0 to 70°C)

Item	Symbol	Test condition		CXK5864 BP/BSP/BM −70L/10L/12L			CXK5864 BP/BSP/BM −70LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	*1 Vcc=3.0V	Ta=0°C to 70°C	—	1	35	—	0.5	15	μA
			Ta=0°C to 40°C	—	—	—	—	—	3	
	I_{CCDR2}	Vcc=2.0 to 5.5V, *1		—	2	60	—	1	30	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

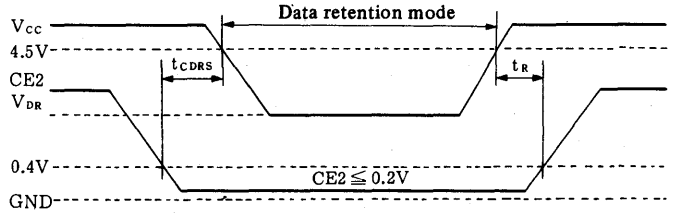
Note) *1. $\overline{CE1} \geqq V_{CC}-0.2V$, $CE2 \geqq V_{CC}-0.2V$ [$\overline{CE1}$ Control] or $CE2 \leqq 0.2V$ [CE2 Control]
*2. t_{RC}: Read cycle time

• Data retention waveform

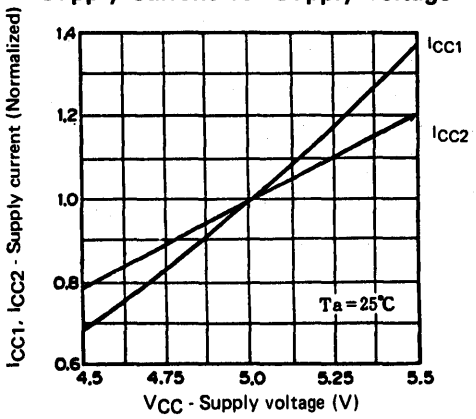
2. $\overline{CE1}$ control



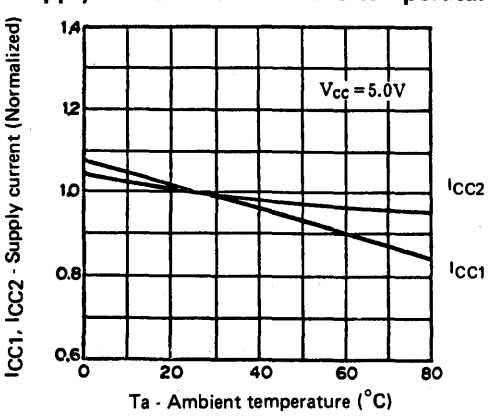
2. CE2 control



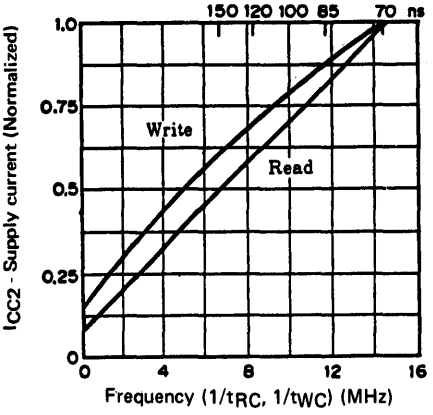
Supply current vs. Supply voltage



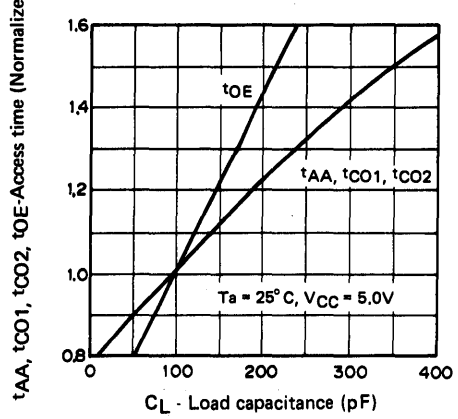
Supply current vs. Ambient temperature



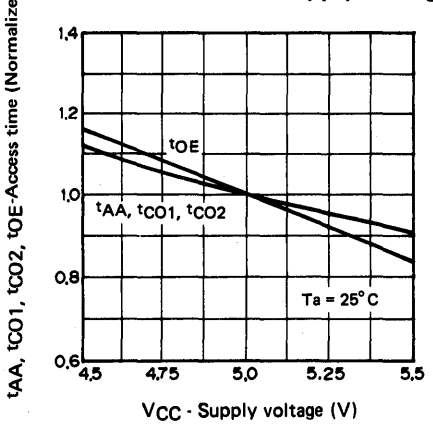
Supply current vs. Frequency



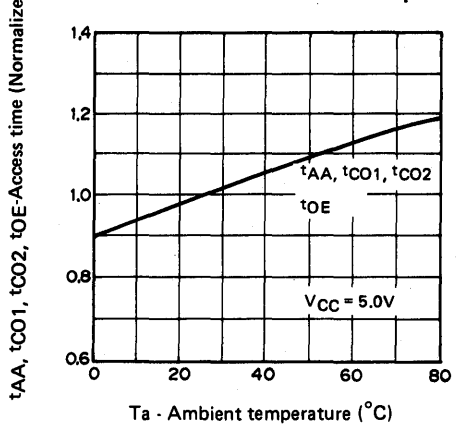
Access time vs. Load capacitance



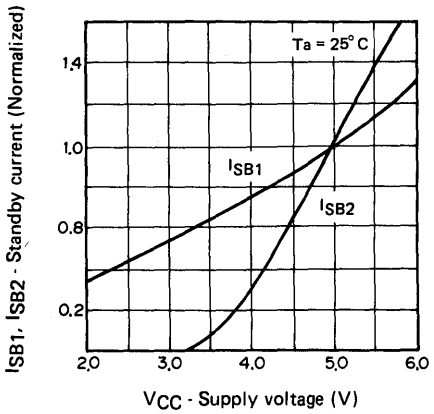
Access time vs. Supply voltage



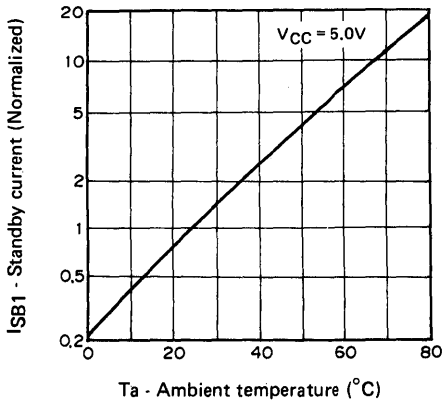
Access time vs. Ambient temperature



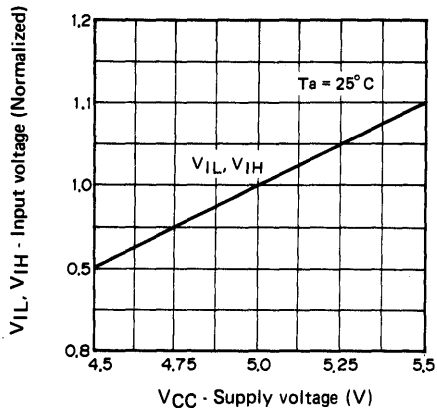
Standby current vs. Supply voltage



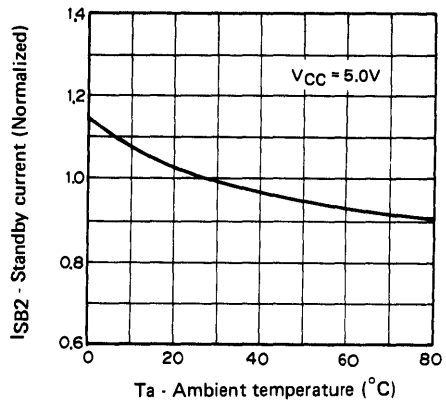
Standby current vs. Ambient temperature



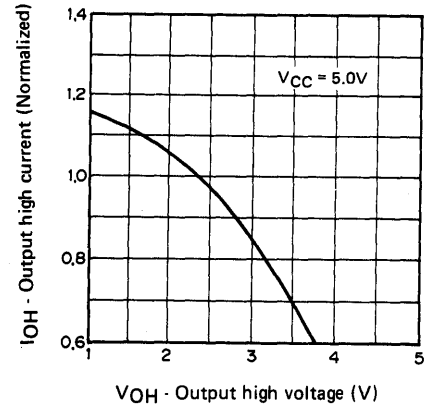
Input voltage vs. Supply voltage



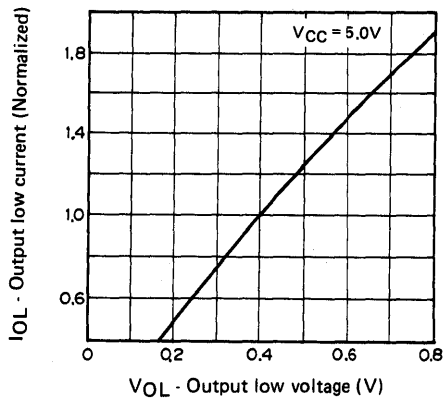
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



8192 word × 8-bit High Speed CMOS Static RAM

Description

CXK5863P/M/J are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8-bits and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is requred.

Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μW (Typ.)
- Low power operation 150 mW (Typ.)
- Single +5V supply: 5V ±10%
- Fully static memory . . . No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.

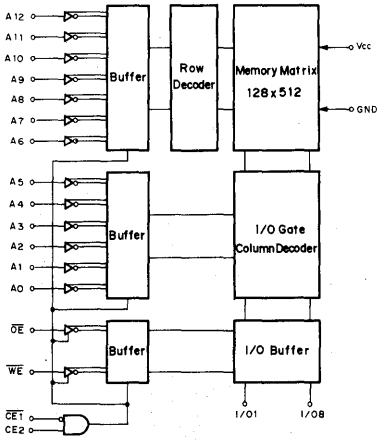
Structure

Silicon gate CMOS IC

Function

8192 word × 8-bits static RAM

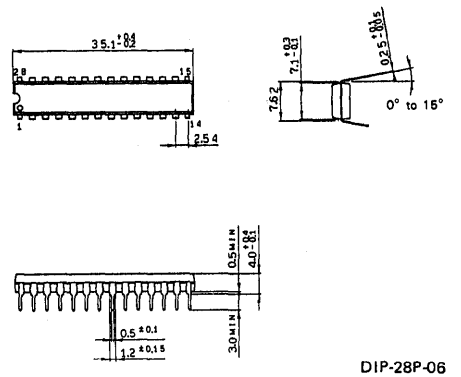
Block Diagram



Package Outline

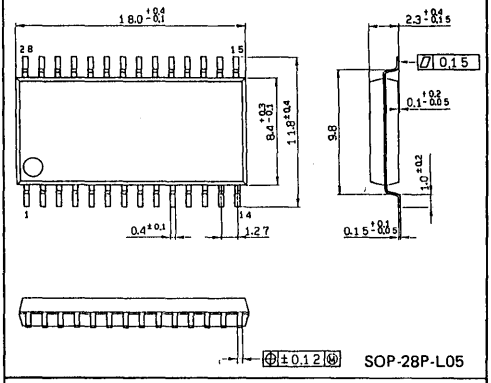
Unit: mm

CXK5863P 28 pin DIP (Plastic)

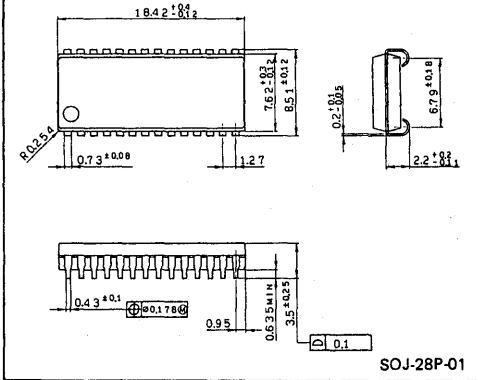


DIP-28P-06

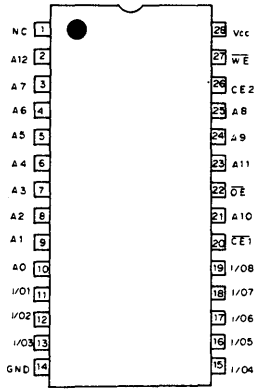
CXK5863M 28 pin SOP (Plastic)



CXK5863J 28 pin SOJ (Plastic)



Pin Configuration (Top View)



Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

Ta=25°C, GND=0V

Item	Symbol		Rating	Unit
Supply voltage	Vcc		−0.5* to +7.0	V
Input voltage	VIN		−0.5* to Vcc+0.5	V
Input and output voltage	VI/O		−0.5* to Vcc+0.5	V
Allowable power dissipation	PD	CXK5863P/J	1.0	W
		CXK5863M	0.7	W
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260·10	°C·sec

***Note)** Vcc, VIN, VI/O=−3.5V Min. for pulse width less than 20 ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	X	Not selected	High Z	ISB1, ISB2
X	L	X	X	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	ICC1, ICC2
L	H	L	H	Read	D out	ICC1, ICC2
L	H	X	L	Write	D in	ICC1, ICC2

X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*	–	0.8	V

***Note)** V_{IL}=−3.0V Min. for pulse width less than 20 ns.

Electrical Characteristics
DC and operating characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5863P/M/J −25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−1	–	1	μA
Output leakage current	I_{LO}	$V_{I/O}$=GND to V_{CC}, $\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	−1	–	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	–	30	60	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0mA	–	60	90	mA
Standby current	I_{SB1}	$\overline{CE1}$≧V_{CC}−0.2V or CE2≦0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	–	1	100	μA
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}, V_{IN}=V_{IL} or V_{IH}	–	10	25	mA
Output high voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	–	–	0.4	V

* V_{CC}=5V, Ta=25°C

I/O capacitance

Ta=25°C, f =1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	–	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	10	pF

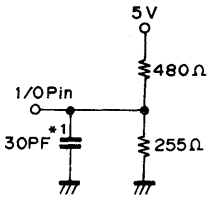
Note) This parameter is sampled and is not 100% tested.

AC characteristics

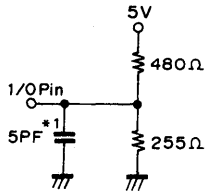
- AC test conditions
  V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_r=5ns
Input fall time	t_f=5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



*1. including scope and jig capacitance

*2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	CXK5863P/M/J -25		CXK5863P/M/J -30		CXK5863P/M/J -35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	–	30	–	35	–	ns
Address access time	t_{AA}	–	25	–	30	–	35	ns
Chip enable access time ($\overline{CE}1$)	t_{CO1}	–	25	–	30	–	35	ns
Chip enable access time (CE2)	t_{CO2}	–	25	–	30	–	35	ns
Output enable to output valid	t_{OE}	–	15	–	15	–	20	ns
Output hold from address change	t_{OH}	5	–	5	–	5	–	ns
Chip enable to output in low Z ($\overline{CE}1$, CE2)	t_{LZ1}* t_{LZ2}*	5	–	5	–	5	–	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	–	0	–	0	–	ns
Chip disable to output in high Z ($\overline{CE}1$, CE2)	t_{HZ1}* t_{HZ2}*	0	15	0	15	0	20	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	13	0	13	0	15	ns
Chip enable to power up time ($\overline{CE}1$, CE2)	t_{PU}	0	–	0	–	0	–	ns
Chip disable to power down time ($\overline{CE}1$, CE2)	t_{PD}	–	20	–	20	–	20	ns

2) Write cycle

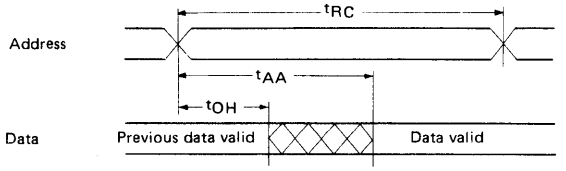
Item	Symbol	CXK5863P/M/J -25		CXK5863P/M/J -30		CXK5863P/M/J -35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	–	30	–	35	–	ns
Address valid to end of write	t_{AW}	20	–	20	–	30	–	ns
Chip enable to end of write	t_{CW}	20	–	20	–	30	–	ns
Data to write time overlap	t_{DW}	12	–	12	–	15	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	20	–	20	–	25	–	ns
Address set up time	t_{AS}	0	–	0	–	0	–	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	–	0	–	0	–	ns
Write recovery time ($\overline{CE}1$, CE2)	t_{WR1}	0	–	0	–	0	–	ns
Output active from end of write	t_{OW}*	5	–	5	–	5	–	ns
Write to output in high Z	t_{WHZ}*	0	13	0	13	0	15	ns

***Note)** Transition is measured ±500 mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

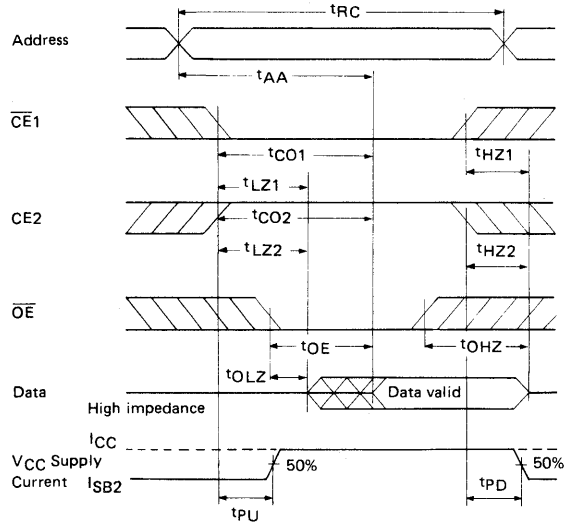
Timing Waveform

1) Read cycle

- Read cycle No. 1: [$\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}]

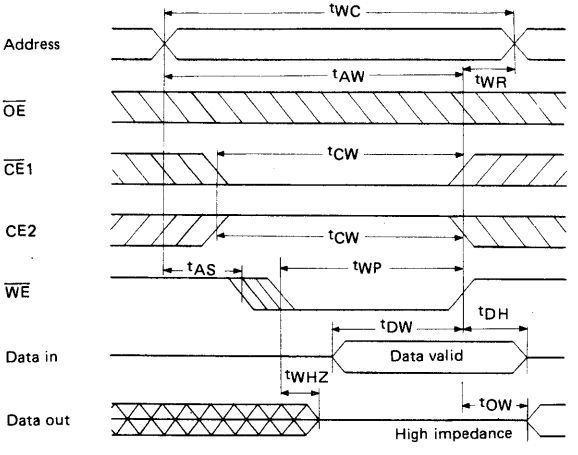


- Read cycle No. 2: [$\overline{WE}$=V_{IH}]

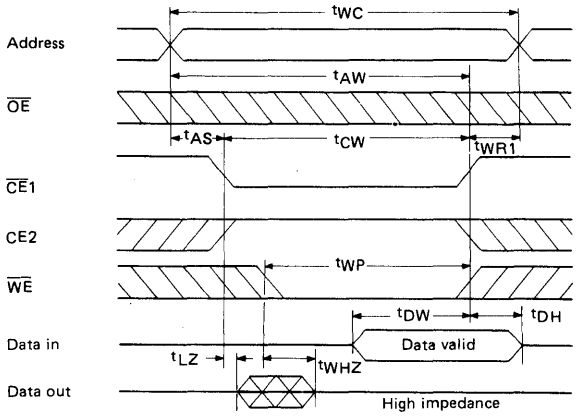


2) Write cycle

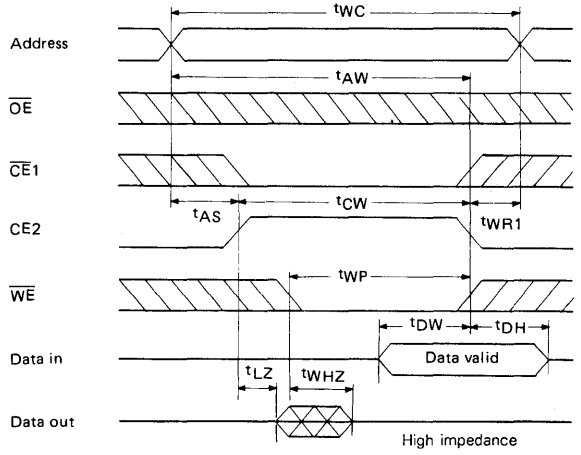
- Write cycle No. 1: [$\overline{WE}$ control]



- Write cycle No. 2: [$\overline{CE}$1 control]



- Write cycle No. 3: [CE2 control]



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

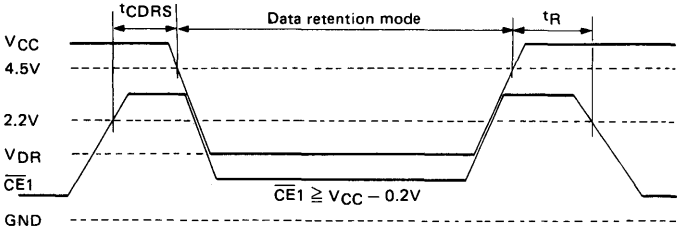
Ta=0 to +70°C

Item	Symbol	Test condition	CXK5863P/M/J −25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V *1	–	0.5	50	μA
	I_{CCDR2}	V_{CC}=2.0 to 5.5V *1	–	1.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	–	–	ns
Recovery time	t_R		t_{RC}*2	–	–	ns

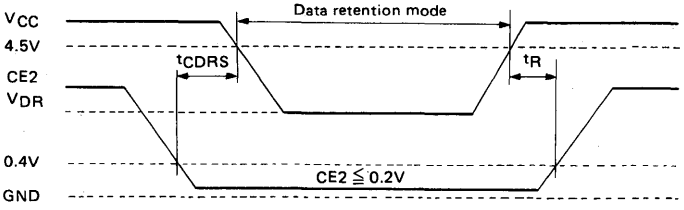
*1. $\overline{CE1} \geqq V_{CC}-0.2V$ or $CE2 \leqq 0.2V$,
$V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$

*2. t_{RC}: Read cycle time

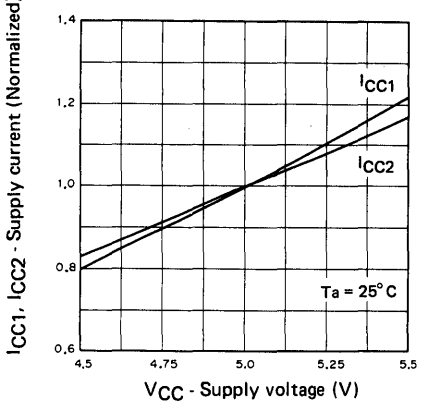
Data Retention Waveform (1): [$\overline{CE1}$ control]



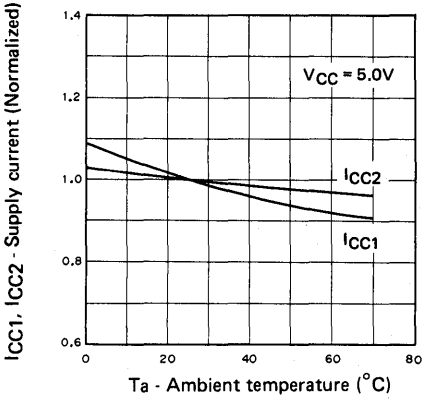
Data Retention Waveform (2): [CE2 control]



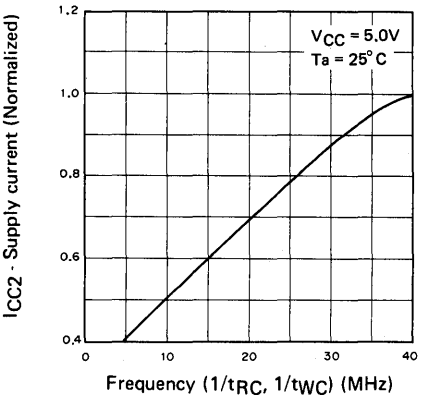
Supply current vs. Supply voltage



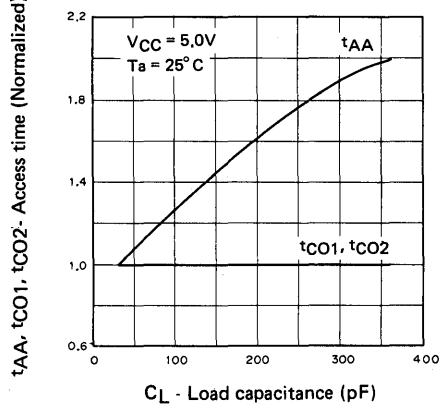
Supply current vs. Ambient temperature



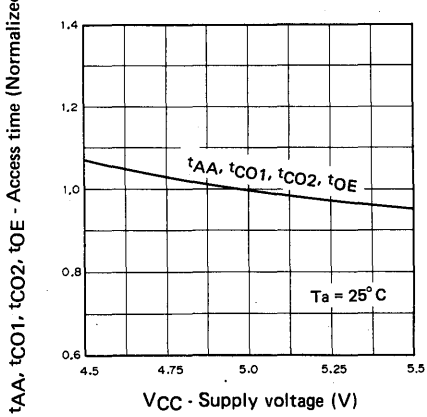
Supply current vs. Frequency



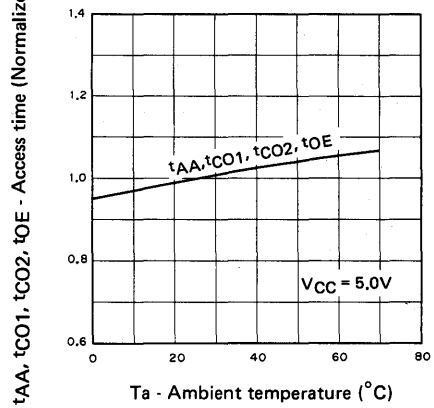
Access time vs. Load capacitance



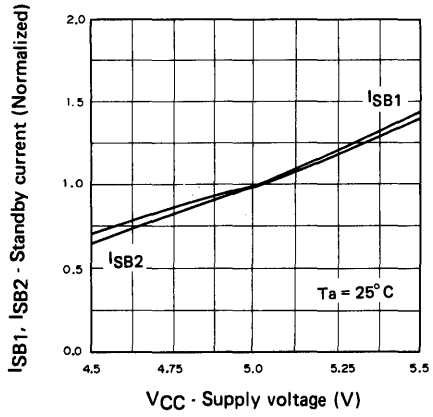
Access time vs. Supply voltage



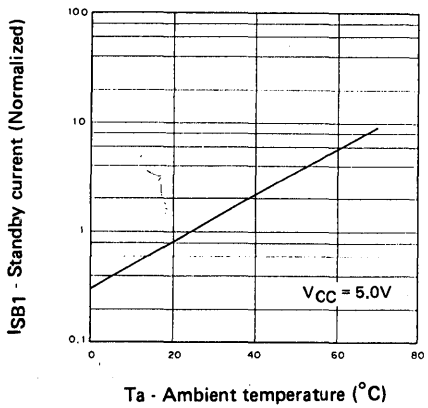
Access time vs. Ambient temperature



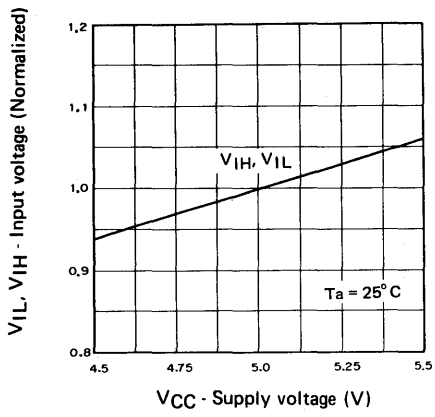
Standby current vs. Supply voltage



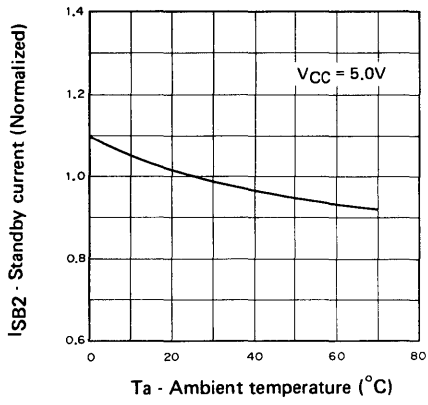
Standby current vs. Ambient temperature



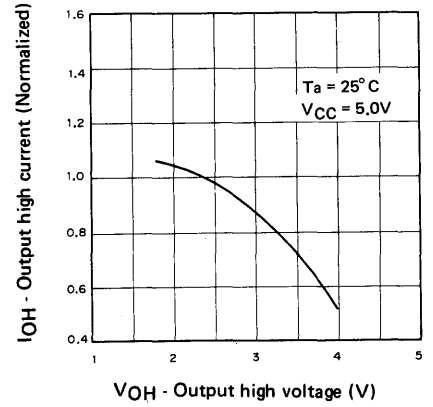
Input voltage vs. Supply voltage



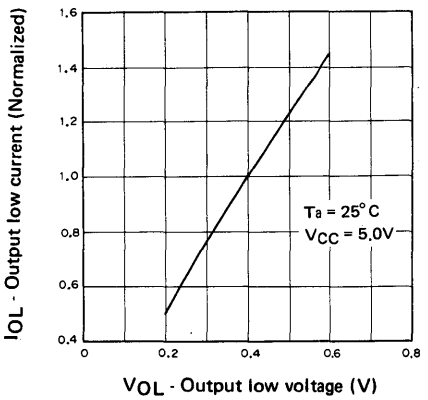
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



8192 word × 8 bit High-Speed CMOS Static RAM

Preliminary

Description

CXK5863AP/AJ are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8-bits and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is requred.

Features

- Fast access time 20ns/25ns (Max.)
- Low power operation 200 mW (Typ.)
- Single +5V supply: 5V ±10%
- Fully static memory . . . No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.

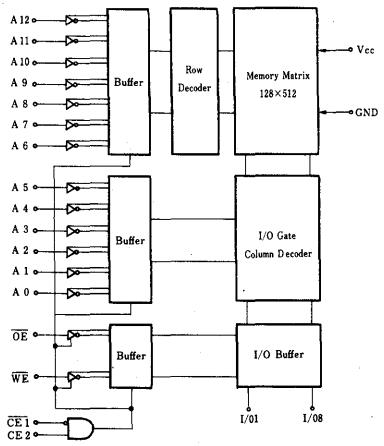
Structure

Silicon gate CMOS IC

Function

8192 word × 8-bits static RAM

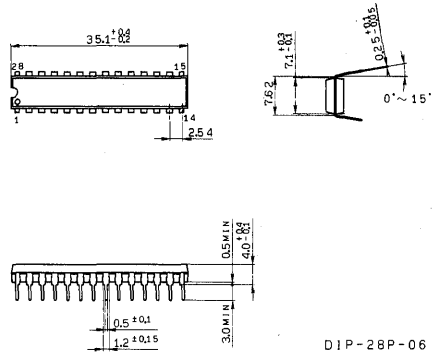
Block Diagram



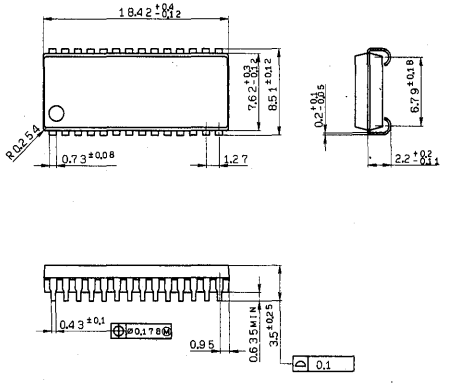
Package Outline

Unit: mm

CXK5863AP 28 pin DIP (Plastic)



CXK5863AJ 28 pin SOJ (Plastic)



16,384 word × 4-bit High Speed CMOS Static RAM

Description

CXK5464AP/AJ are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

Features

- Fast access time:
  - CXK5464AP/AJ-25 25 ns (Max.)
  - CXK5464AP/AJ-30 30 ns (Max.)
  - CXK5464AP/AJ-35 35 ns (Max.)
- Low power operation: 125 mW (Typ.)
- Single +5V supply: +5V ±10%
- Fully static memory. . No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three-state output
- Directly TTL compatible: All inputs and outputs.
- High density: 300 mil 22 pin plastic DIP.
  300 mil 24 pin plastic SOJ.

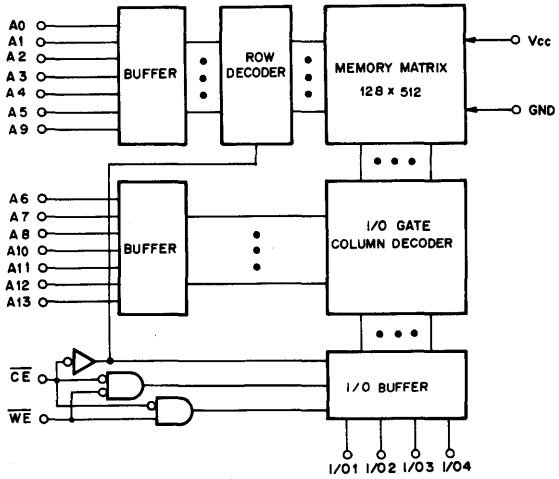
Function

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

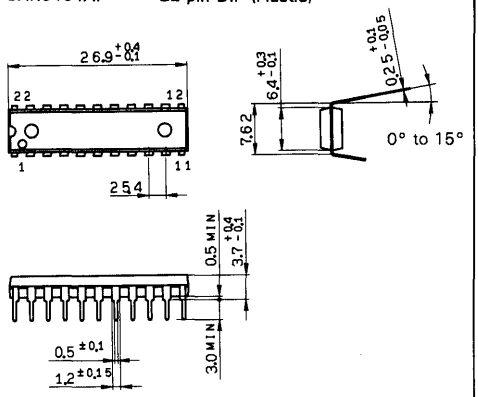
Block Diagram



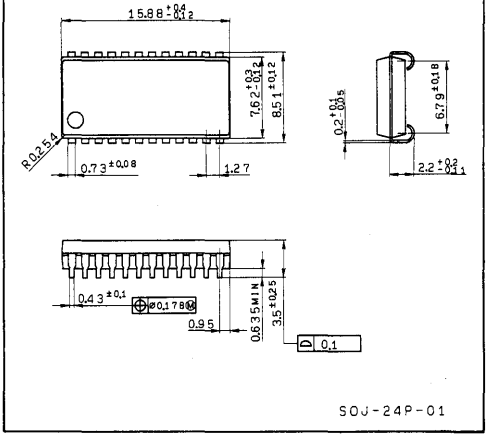
Package Outline

Unit: mm

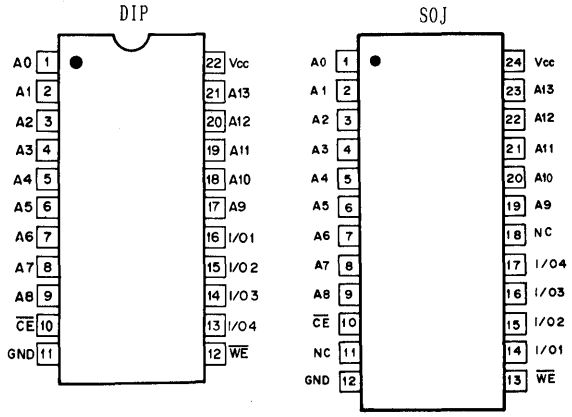
CXK5464AP 22 pin DIP (Plastic)



CXK5464AJ 24 pin SOJ (Plastic)



Pin Configuration (Top View)



Symbol	Description
A0 to A13	Address input
I/O 1 to I/O 4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

Ta = 25°C, GND = 0V

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5* to +7.0	V
Input voltage	VIN	−0.5* to Vcc+0.5	V
Input and output voltage	VI/O	−0.5* to Vcc+0.5	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	260 • .10	°C • sec
Allowable power dissipation	PD	1.0	W

***Note)** Vcc, VIN, VI/O Min.=−3.5V for pulse width less than 20 ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O 1 to I/O 4	Vcc Current
H	X	Not selected	High Z	ISB1, ISB2
L	H	Read	DOUT	ICC1, ICC2
L	L	Write	DIN	ICC1, ICC2

X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	VIH	2.2	—	Vcc+0.3	V
Input low voltage	VIL	−0.3*2	—	0.8	V

Note) *1. Vcc = 5V, Ta = 25°C

*2. VIL Min. = −3.0V for pulse width less than 20 ns.

Electrical Characteristics

DC and operating characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5464AP/AJ -25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0 mA V_{IN}=V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0 mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$=V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0 mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0 mA	—	—	0.4	V

*Note) V_{CC}=5.0V. Ta=25°C

I/O capacitance

Ta=25°C, f=1 MHz

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

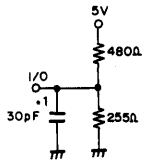
AC characteristics

- **AC test condition**

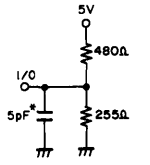
V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_r=5 ns
Input fall time	t_f=5 ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



*1. Including scope and jig.
*2. For t_{LZ}, t_{HZ}, t_{ON}, t_{WHZ}.

Fig. 1

• **Read cycle**

Item	Symbol	CXK5464AP/AJ-25		CXK5464AP/AJ-30		CX5464AP/AJ-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	25	ns

***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

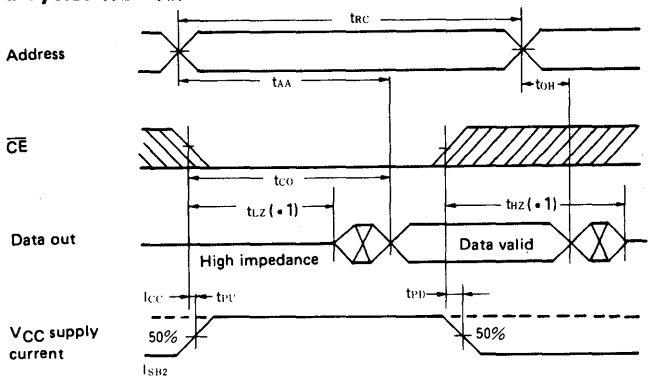
• **Write cycle**

Item	Symbol	CXK5464AP/AJ-25		CXK5464AP/AJ-30		CXK5464AP/AJ-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

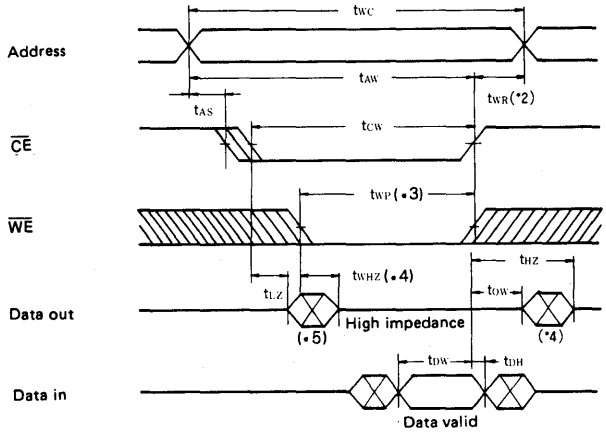
***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

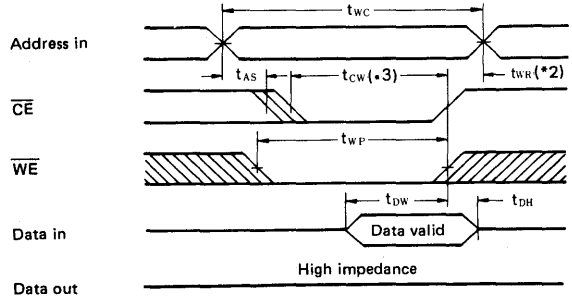
- **Read cycle:** $\overline{WE}$ = V_{IH}



- **Write cycle (1):** $\overline{WE}$ Control



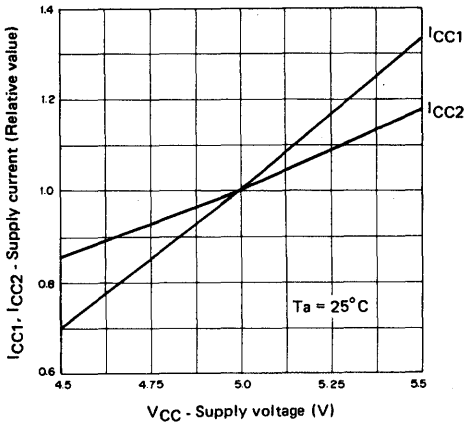
- **Write cycle (2):** $\overline{CE}$ Control



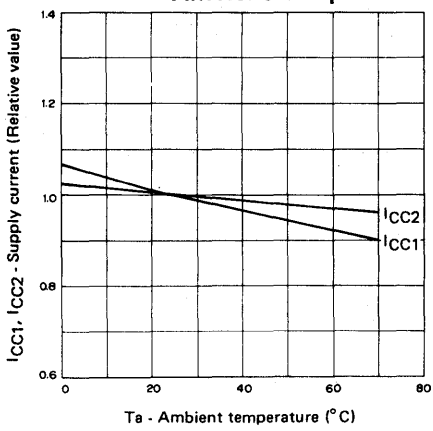
***Note)**

1. At any conditions, t_{HZ} is less than t_{LZ}.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

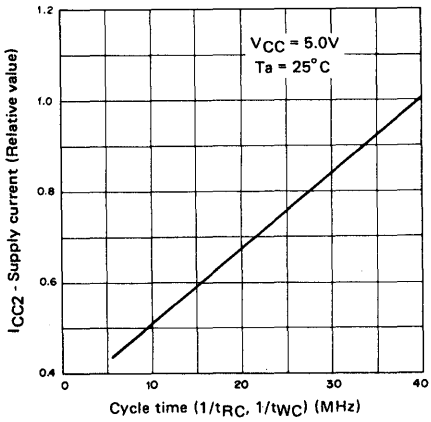
Supply current vs. Supply voltage



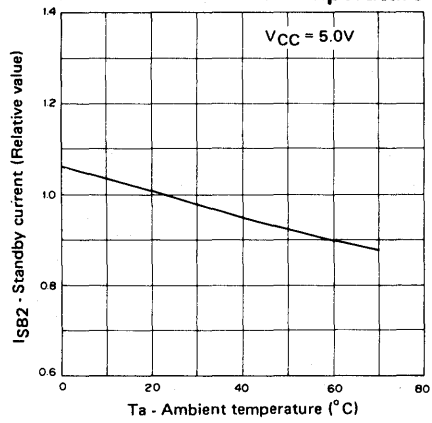
Supply current vs. Ambient temperature



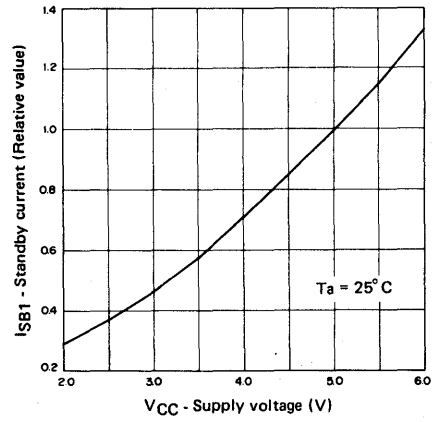
Supply current vs. Cycle time



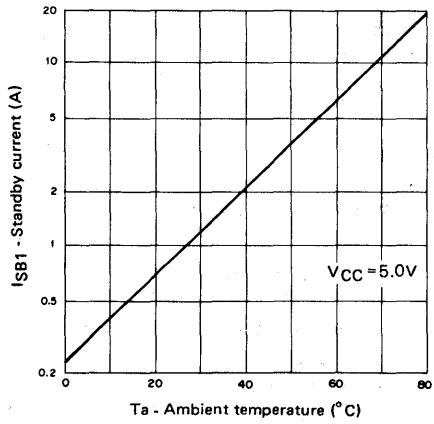
Standby current vs. Ambient temperature



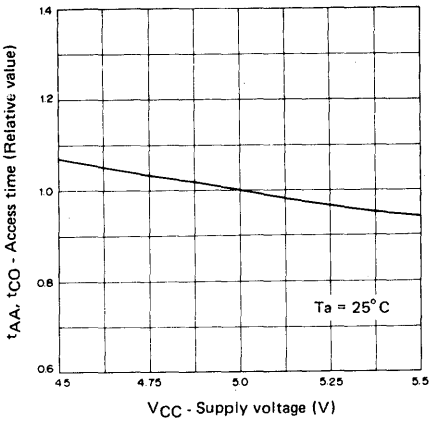
Standby current vs. Supply voltage



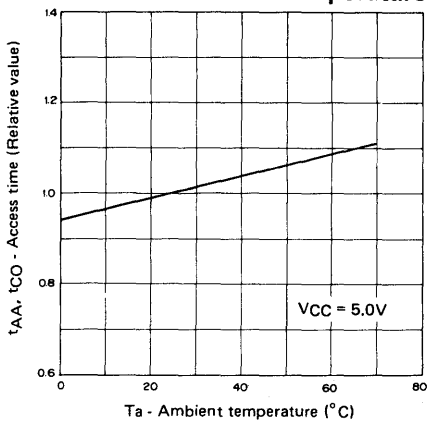
Standby current vs. Ambient temperature



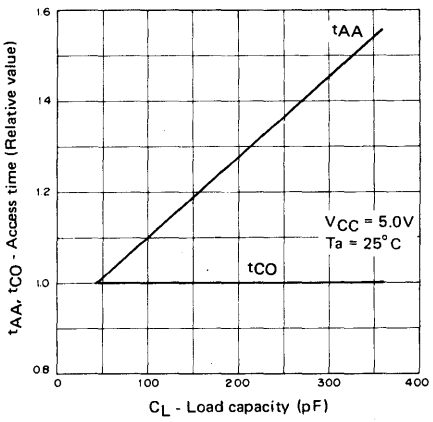
Access time vs. Supply voltage



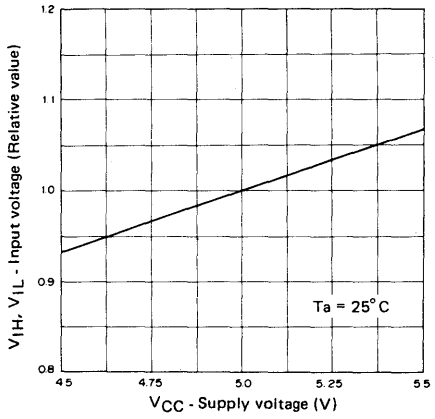
Access time vs. Ambient temperature



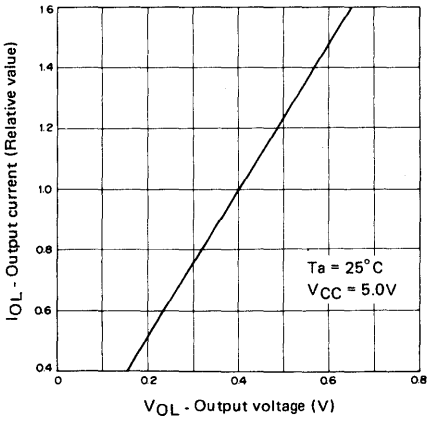
Access time vs. Load capacity



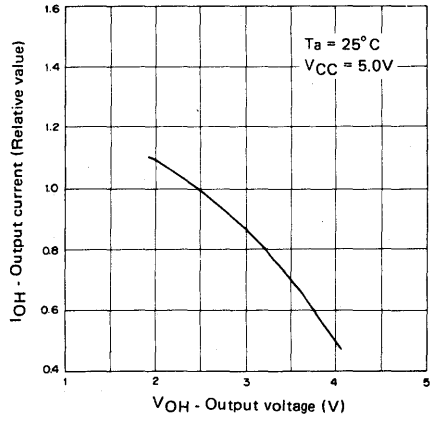
Input voltage vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



16,384 word × 4-bit High Speed CMOS Static RAM

Description

CXK5465P/J are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

These devices feature Output Enable ($\overline{OE}$) to enhance their flexibility in high-speed memory applications.

Features

- Fast access time:
  - CXK5465P/J-25 25ns (Max.)
  - CXK5465P/J-30 30ns (Max.)
  - CXK5465P/J-35 35ns (Max.)
- Low power operation: 125 mW (Typ.)
- Single +5V supply: +5V ±10%
- Fully static memory . . No clock or timing strobe required.
- Output Enable ($\overline{OE}$) control available.
- Equal access and cycle time.
- Common data input and output: three-state output.
- Directly TTL compatible: All inputs and outputs.
- High density: 300 mil 24 pin plastic DIP
  300 mil 24 pin plastic SOJ

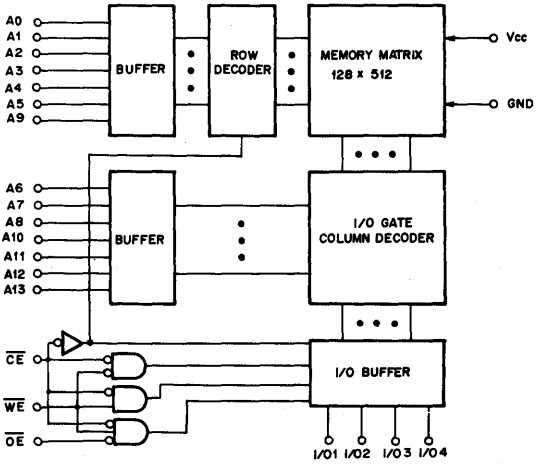
Function

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

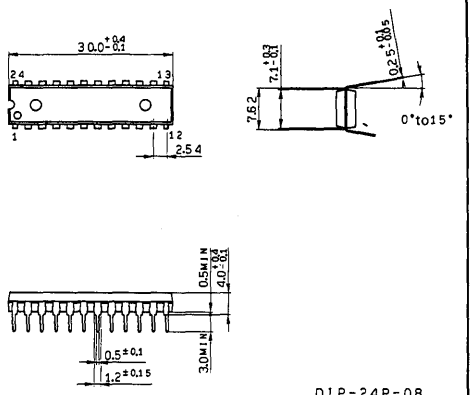
Block Diagram



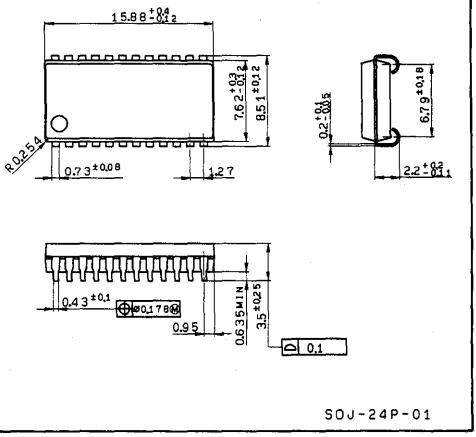
Package Outline

Unit: mm

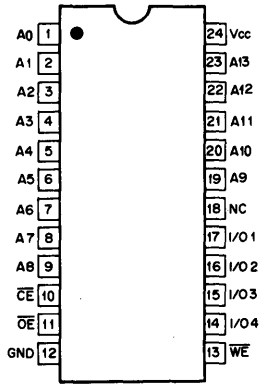
CXK5465P 24 pin DIP (Plastic)



CXK5465J 24pin SOJ (Plastic)



Pin Configuration (Top View)



Symbol	Description
A0 to A13	Address input
I/O 1 to I/O 4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC}+0.5	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	260 • .10	°C • sec
Allowable power dissipaiton	P_D	1.0	W

***Note)** V_{CC}, V_{IN}, $V_{I/O}$ Min. = −3.5V for pulse width less than 20 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O 1 to I/O 4	Vcc Current
H	X	X	Not Selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	D_{OUT}	I_{CC1}, I_{CC2}
L	X	L	Write	D_{IN}	I_{CC1}, I_{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to +70°C, GND = 0V

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

Note) *1. V_{CC} = 5V, Ta = 25°C

*2. V_{IL} Min. = −3.0V for pulse width less than 20 ns.

DC Electrical Characteristics

DC and operating characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5465P/J -25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0 mA V_{IN}=V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0 mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$=V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0 mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0 mA	—	—	0.4	V

***Note)** V_{CC}=5.0V, Ta=25°C

I/O capacitance

Ta=25°C, f=1 MHz

Item	Test Condition	Symbol	Min.	Max.	Unit
Input capacitance	V_{IN}=0V	C_{IN}	—	7	pF
Input/Output capacitance	$V_{I/O}$=0V	$C_{I/O}$	—	7	pF

Note) This parameter is sampled and is not 100% tested.

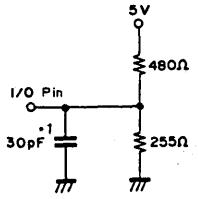
AC characteristics

- **AC test conditions**

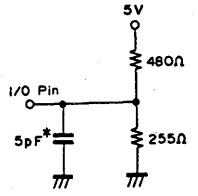
V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_R=5 ns
Input fall time	t_F=5 ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2) *2



*1. Including scope and jig
*2. For t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	CXK5465P/J-25		CXK5465P/J-30		CXK5465P/J-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output enable to output valid	t_{OE}	—	12	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	10	0	10	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	25	ns

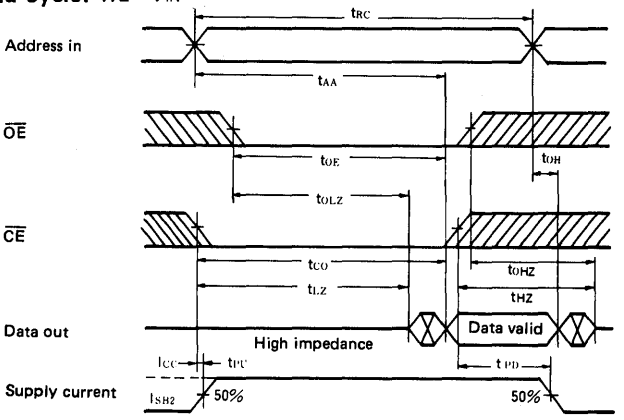
• Write cycle

Item	Symbol	CXK5465P/J-25		CXK5465P/J-30		CXK5465P/J-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

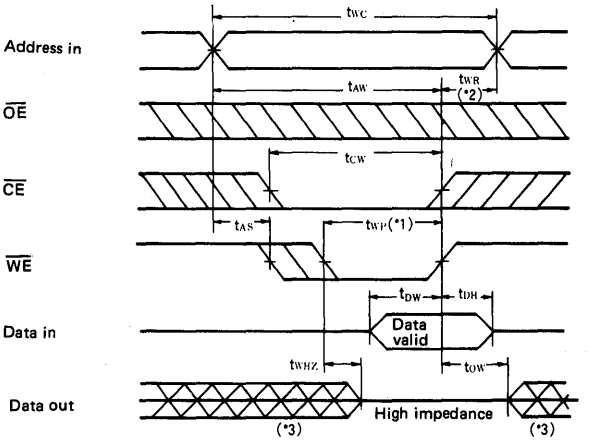
***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

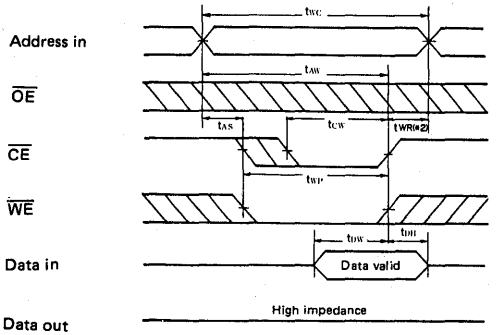
- **Read cycle:** $\overline{WE}$ = VIH



- **Write cycle (1):** $\overline{WE}$ Control



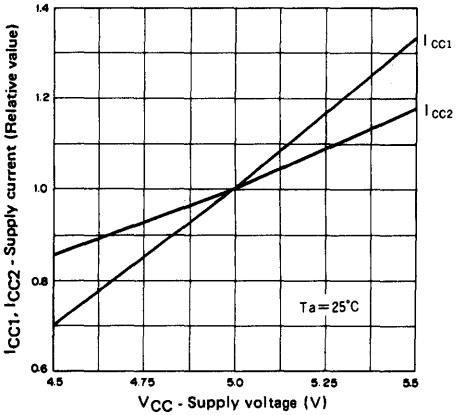
- **Write cycle (2):** $\overline{CE}$ Control



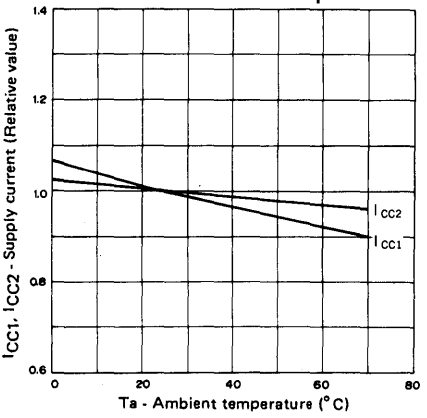
*** Note)**

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. tWR is measured from the rising of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.
3. While I/O pins are in output state, a data input voltage of a phase opposite to the output must not be applied.

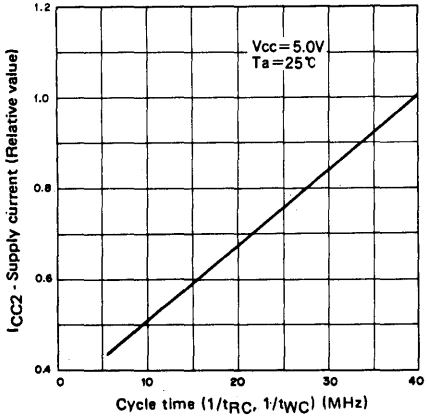
Supply current vs. Supply voltage



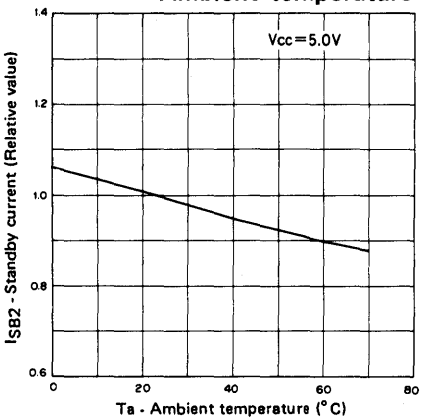
Supply current vs. Ambient temperature



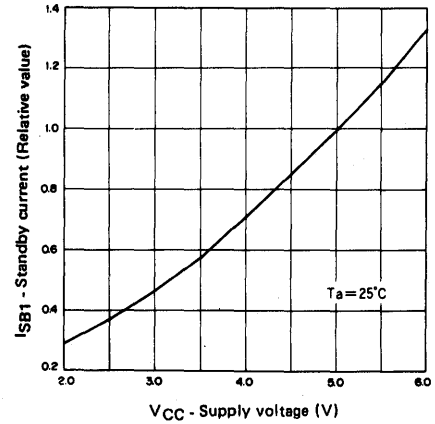
Supply current vs. Cycle time



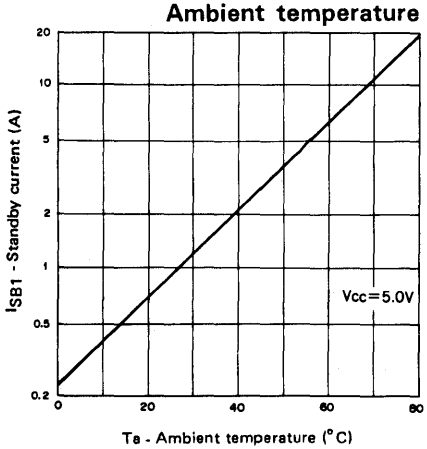
Standby current vs. Ambient temperature



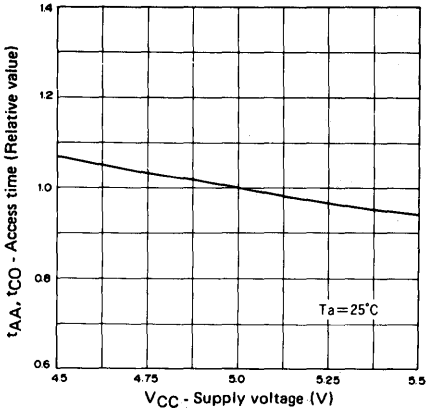
Standby current vs. Supply voltage



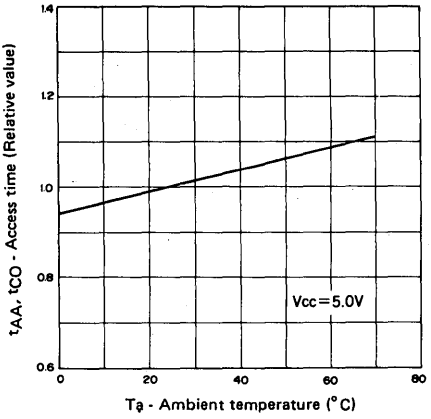
Standby current vs. Ambient temperature



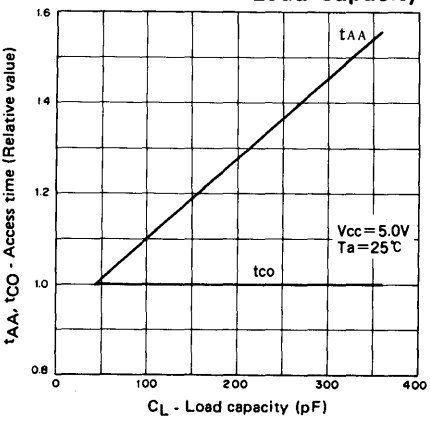
Access time vs. Supply voltage



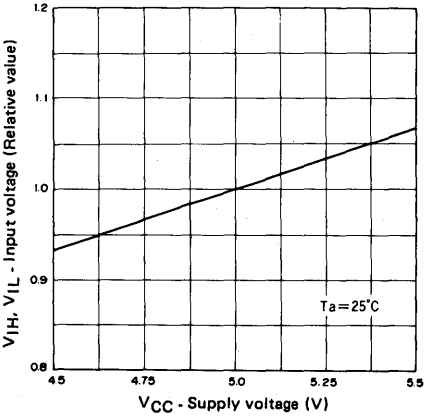
Access time vs. Ambient temperature



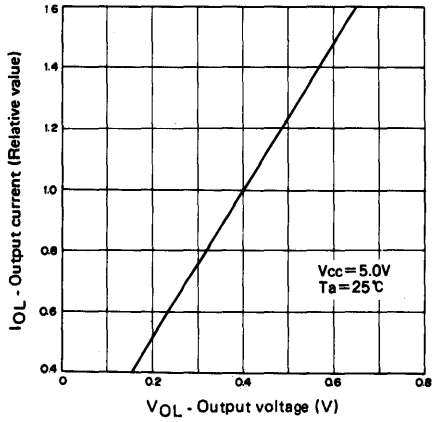
Access time vs. Load capacity



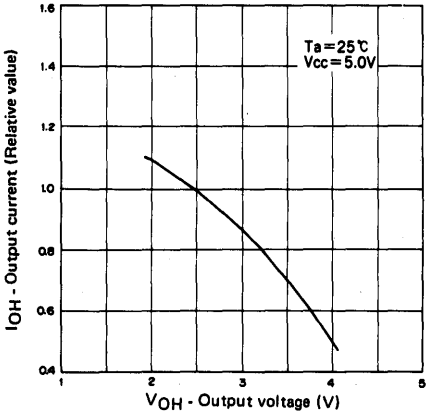
Input voltage vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



65,536 word × 1-bit High Speed CMOS Static RAM

Description

CXK5164P/J are 65,536 bits high speed CMOS static RAMs organized as 65,536 words by 1 bit and operates from a single 5V supply.

These devices have separate Data Input and Data Output pins.

Features

- Fast access time:
  - CXK5164P/J-25 25ns (Max.)
  - CXK5164P/J-30 30ns (Max.)
  - CXK5164P/J-35 35ns (Max.)
- Low power operation: 125 mW (Typ.)
- Single +5V supply: +5V ±10%
- Fully static memory . . No clock or timing strobe required.
- Equal access and cycle time
- Separate I/O pins
- Three-state output
- Directly TTL compatible: All inputs and outputs.
- High density: 300 mil 22 pin plastic DIP
  300 mil 24 pin plastic SOJ

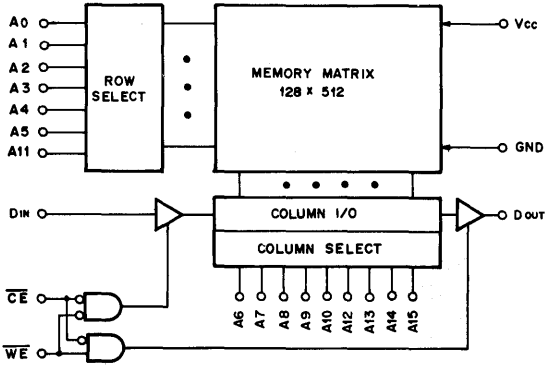
Function

65,536 word × 1-bit static RAM

Structure

Silicon gate CMOS IC

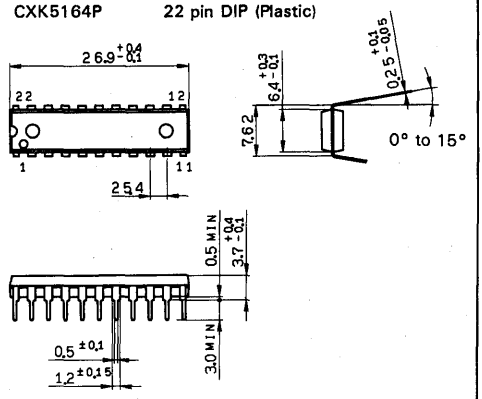
Block Diagram



Package Outline

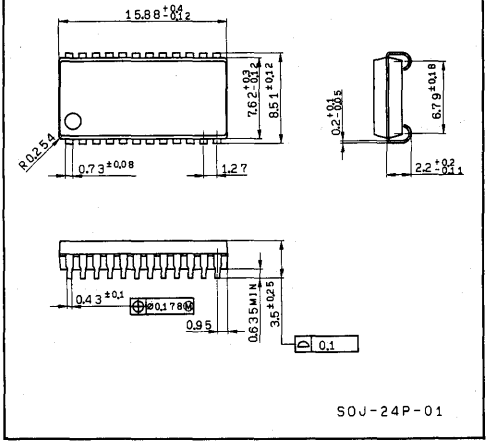
Unit: mm

CXK5164P 22 pin DIP (Plastic)



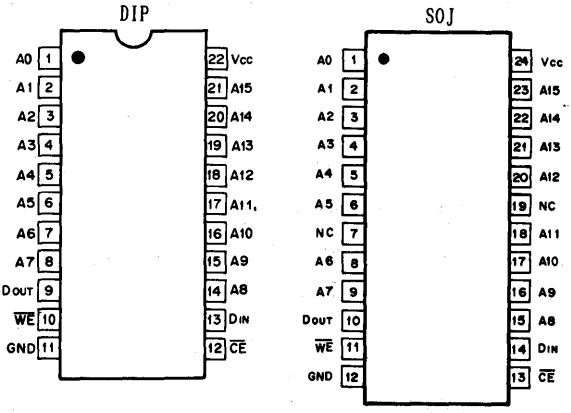
DIP-22P-02

CXK5164J 24 pin SOJ (Plastic)



SOJ-24P-01

Pin Configuration (Top View)



Symbol	Description
A0 to A15	Address input
Din	Data input
Dout	Data output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5* to +7.0	V
Input voltage	VIN	−0.5* to Vcc+0.5	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	260·10	°C·sec
Voltage applied to output	VOUT	−0.5* to Vcc+0.5	V
Allowable power dissipation	PD	1.0	W

***Note)** Vcc, VIN, VOUT min = −3.5V for pulse width less than 20 ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	Dout	Vcc Current
H	X	Not Selected	High Z	ISB1, ISB2
L	H	Read	DOUT	ICC1, ICC2
L	L	Write	High Z	ICC1, ICC2

X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	VIH	2.2	—	Vcc+0.3	V
Input low voltage	VIL	−0.3*2	—	0.8	V

Note) *1. Vcc = 25°C
*2. VIL min. = −3.0V for pulse width less than 20 ns.

Electrical Characteristics

DC and operating characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5164P/J -25/30/35			Unit
			Min.	Typ.	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0 mA V_{IN}=V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0 mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$=V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0 mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0 mA	—	—	0.4	V

***Note)** V_{CC}=5.0V, Ta=25°C

I/O capacitance

Ta=25°C, f=1 MHz

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Output capacitance	C_{OUT}	V_{OUT}=0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

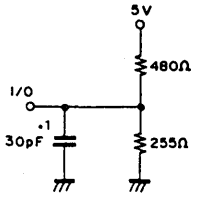
AC characteristics

- **AC test condition**

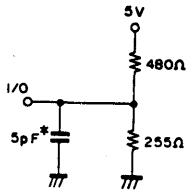
V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_r=5 ns
Input fall time	t_f=5 ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2) *2



*1. Including scope and jig
*2. For tLZ, tHZ, tOW, tWHZ

Fig. 1

• Read Cycle

Item	Symbol	CXK5164P/J-25		CXK5164P/J-30		CXK5164P/J-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	25	ns

***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

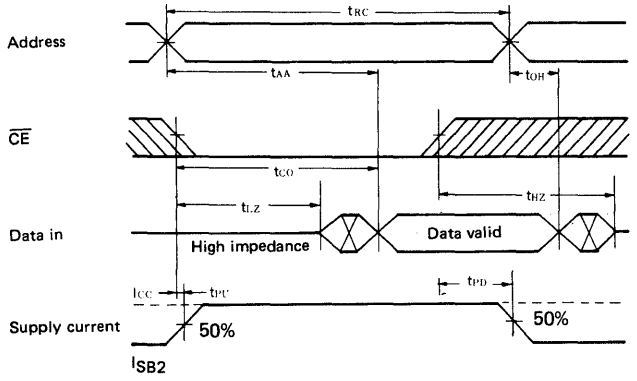
• Write Cycle

Item	Symbol	CXK5164P/J-25		CXK5164P/J-30		CXK5164P/J-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

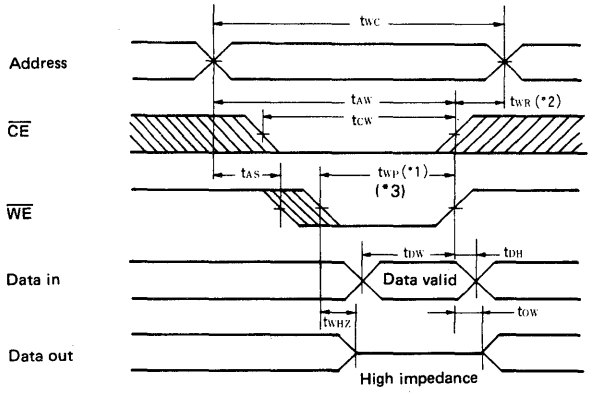
***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

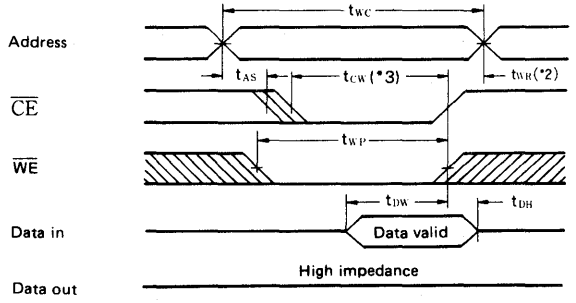
- **Read cycle:** $\overline{WE} = V_{IH}$



- **Write cycle (1):** $\overline{WE}$ Control



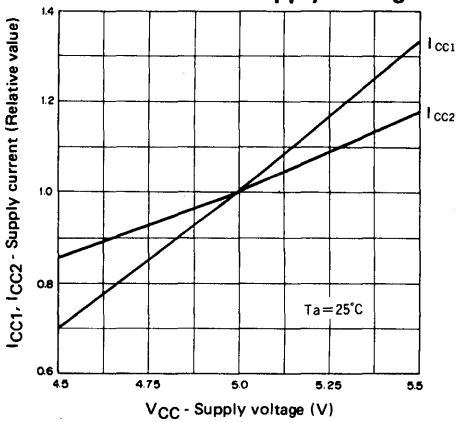
- **Write cycle (2):** $\overline{CE}$ Control



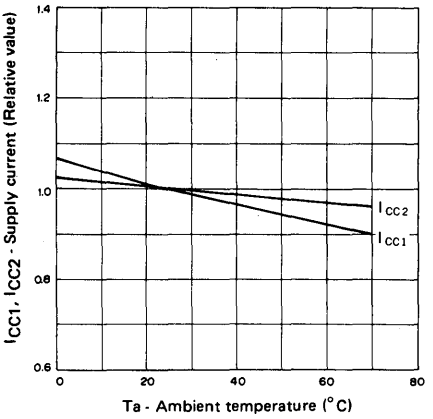
*** Note)**

1. At any conditions, tHZ is less than tLZ.
2. tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.

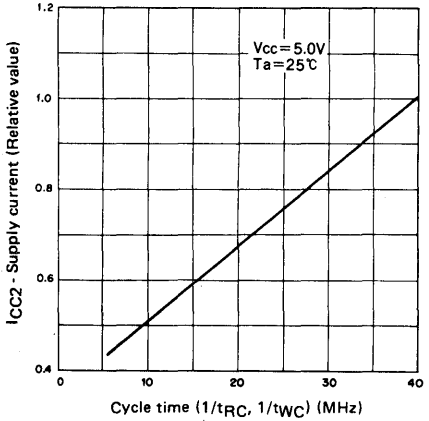
Supply current vs. Supply voltage



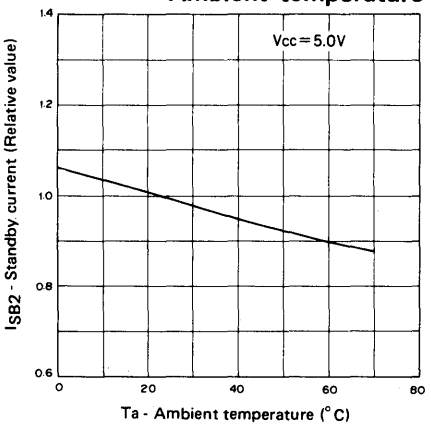
Supply current vs. Ambient temperature



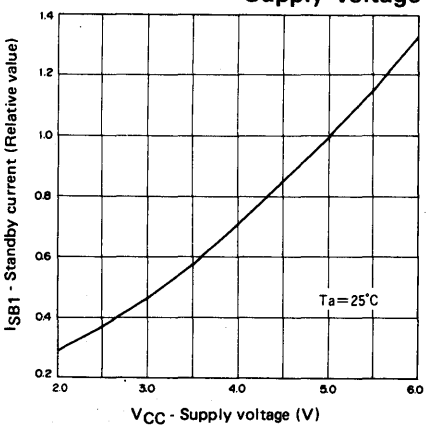
Supply current vs. Cycle time



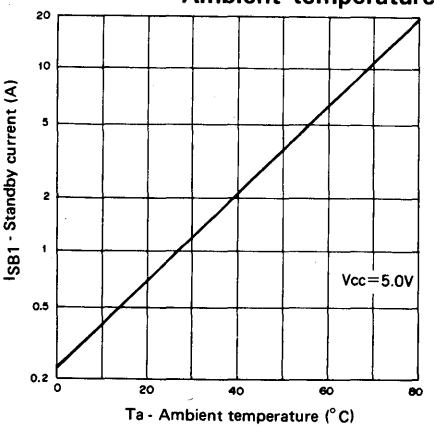
Standby current vs. Ambient temperature



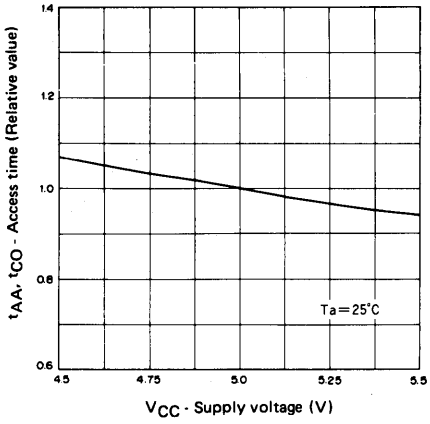
Standby current vs. Supply voltage



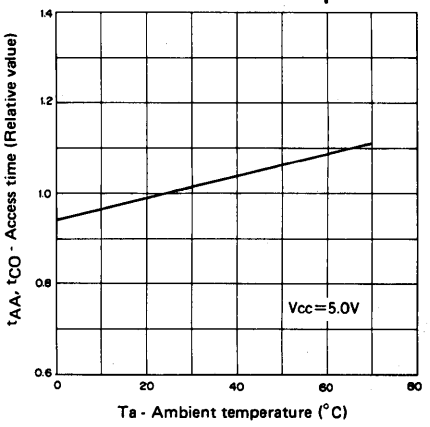
Standby current vs. Ambient temperature



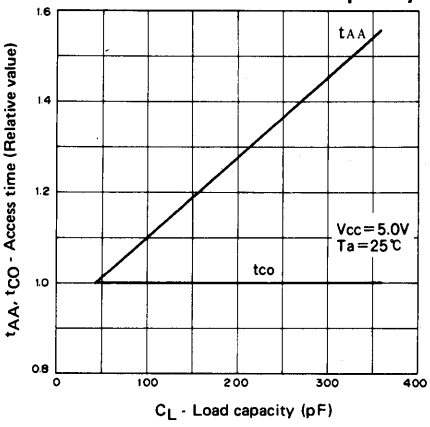
Access time vs. Supply voltage



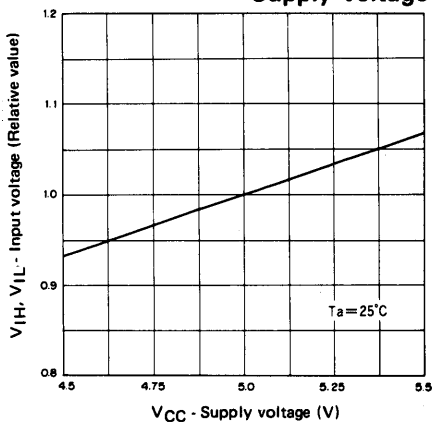
Access time vs. Ambient temperature



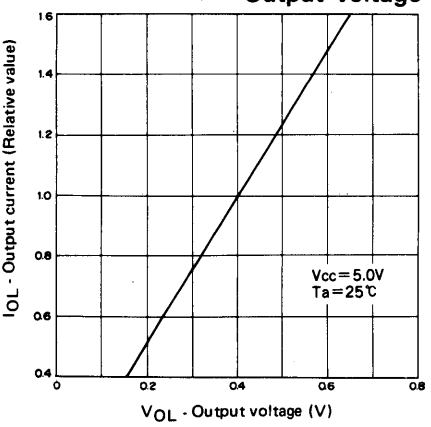
Access time vs. Load capacity



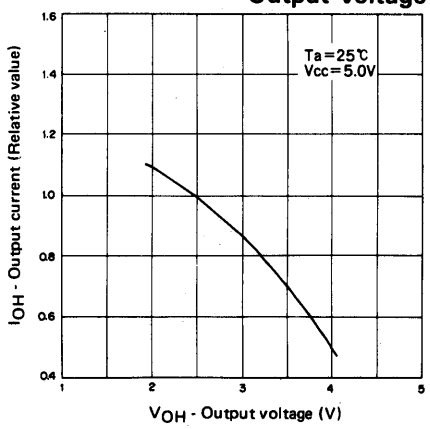
Input voltage vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



8192 word × 9-bit High Speed CMOS Static RAM

Description

CXK5971P and CXK5971J are 73,728 bits high speed CMOS static RAMs organized as 8,192 words by 9 bits and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μW (Typ.)
- Low power operation 150 mW (Typ.)
- Single +5V supply: 5V ±10%
- Fully static memory . . . No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.

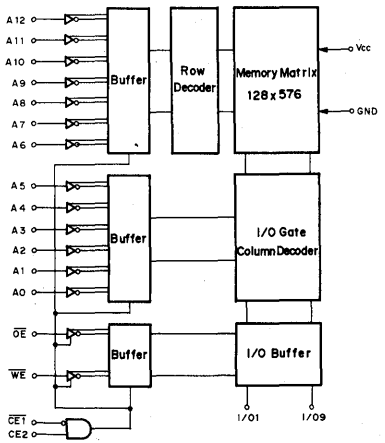
Structure

Silicon gate CMOS IC

Function

8192-word × 9-bit static RAM

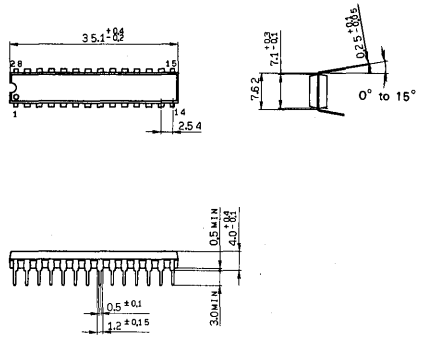
Block Diagram



Package Outline

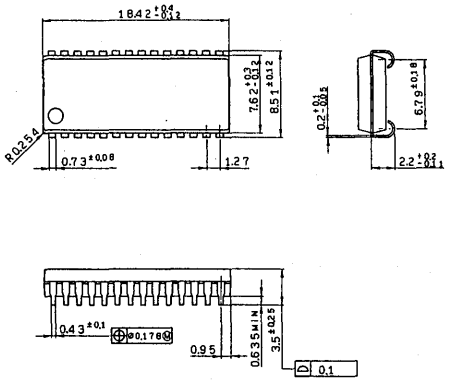
Unit: mm

CXK5971P 28 pin DIP (Plastic)



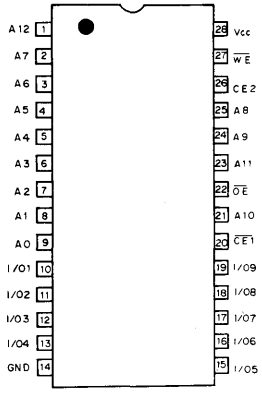
DIP-28P-06

CXK5971J 28 pin SOJ (Plastic)



SOJ-28P-01

Pin Configuration (Top View)



Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

Ta=25°C, GND=0V

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to Vcc+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	260·10	°C·sec

***Note)** V_{CC}, V_{IN}, $V_{I/O}$=−3.5V Min. for pulse width less than 20 ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	Vcc Current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	D out	I_{CC1}, I_{CC2}
L	H	X	L	Write	D in	I_{CC1}, I_{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*	–	0.8	V

***Note)** V_{IL}=−3.0V Min. for pulse width less than 20 ns.

Electrical Characteristics

DC and operating characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK5971P/J −25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	−1	–	1	μA
Output leakage current	I_{LO}	$V_{I/O}$=GND to V_{CC}, $\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	−1	–	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	–	30	60	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0mA	–	60	90	mA
Standby current	I_{SB1}	$\overline{CE1}$≧V_{CC}−0.2V or CE2≦0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	–	1	100	μA
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}, V_{IN}=V_{IL} or V_{IH}	–	10	25	mA
Output high voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	–	–	0.4	V

* V_{CC}=5V, Ta=25°C

I/O capacitance

Ta=25°C, f=1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	–	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	10	pF

Note) This parameter is sampled and is not 100% tested.

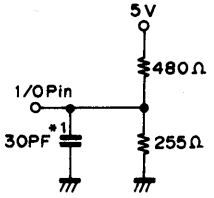
AC characteristics

- AC test conditions

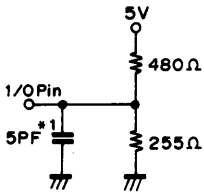
Vcc = 5V ± 10%, Ta = 0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_r=5ns
Input fall time	t_f=5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



*1. including scope and jig capacitance

*2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	CXK5971P/J -25		CXK5971P/J -30		CXK5971P/J -35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	–	30	–	35	–	ns
Address access time	t_{AA}	–	25	–	30	–	35	ns
Chip enable access time ($\overline{CE}1$)	t_{CO1}	–	25	–	30	–	35	ns
Chip enable access time (CE2)	t_{CO2}	–	25	–	30	–	35	ns
Output enable to output valid	t_{OE}	–	15	–	15	–	20	ns
Output hold from address change	t_{OH}	5	–	5	–	5	–	ns
Chip enable to output in low Z ($\overline{CE}1$, CE2)	t_{LZ1}* t_{LZ2}*	5	–	5	–	5	–	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	–	0	–	0	–	ns
Chip disable to output in high Z ($\overline{CE}1$, CE2)	t_{HZ1}* t_{HZ2}*	0	15	0	15	0	20	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	13	0	13	0	15	ns
Chip enable to power up time	t_{PU}	0	–	0	–	0	–	ns
Chip disable to power down time	t_{PD}	–	20	–	20	–	20	ns

2) Write cycle

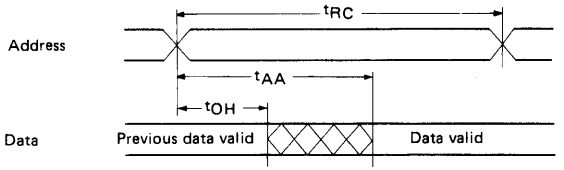
Item	Symbol	CXK5971P/J -25		CXK5971P/J -30		CXK5971P/J -35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	–	30	–	35	–	ns
Address valid to end of write	t_{AW}	20	–	20	–	30	–	ns
Chip enable to end of write	t_{CW}	20	–	20	–	30	–	ns
Data to write time overlap	t_{DW}	12	–	12	–	15	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	20	–	20	–	25	–	ns
Address set up time	t_{AS}	0	–	0	–	0	–	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	–	0	–	0	–	ns
Write recovery time ($\overline{CE}1$, CE2)	t_{WR1}	0	–	0	–	0	–	ns
Output active from end of write	t_{OW}*	5	–	5	–	5	–	ns
Write to output in high Z	t_{WHZ}*	0	13	0	13	0	15	ns

* Transition is measured ±500 mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and not 100% tested.

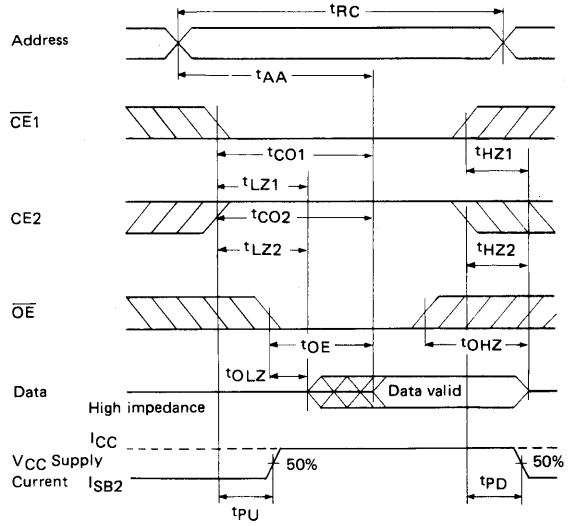
Timing Waveform

1) Read cycle

- Read cycle No. 1: [$\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}]

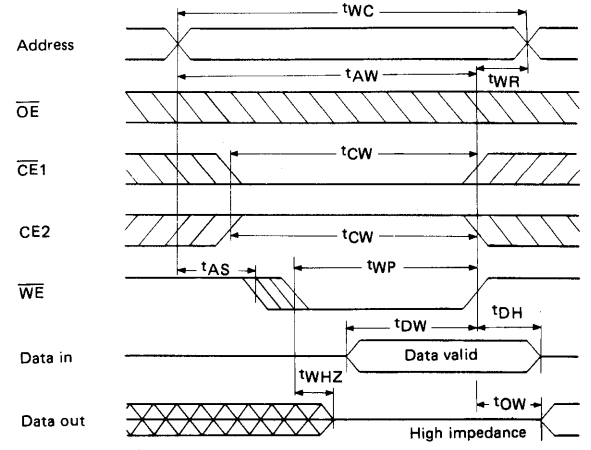


- Read cycle No. 2: [$\overline{WE}$=V_{IH}]

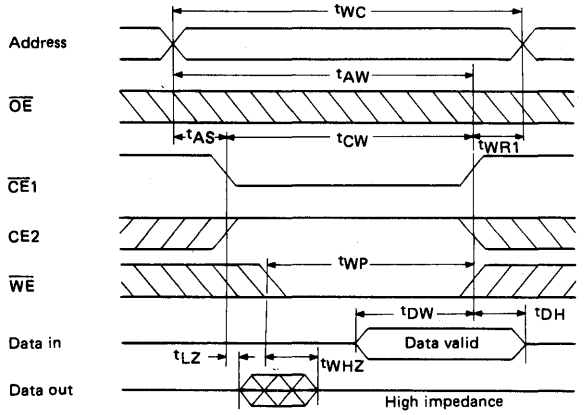


2) Write cycle

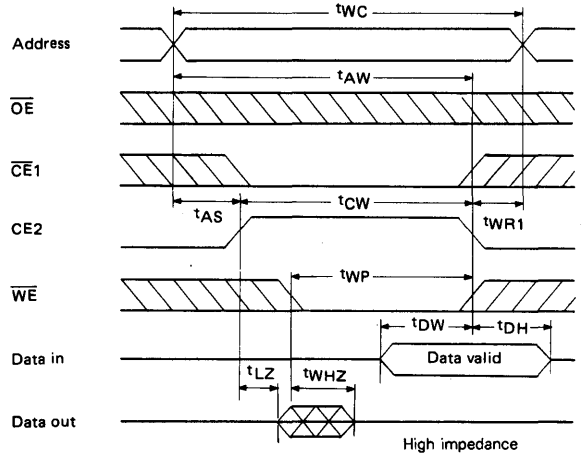
- Write cycle No. 1: [$\overline{WE}$ control]



• Write cycle No. 2: [$\overline{CE1}$ control]



• Write cycle No. 3: [CE2 control]



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

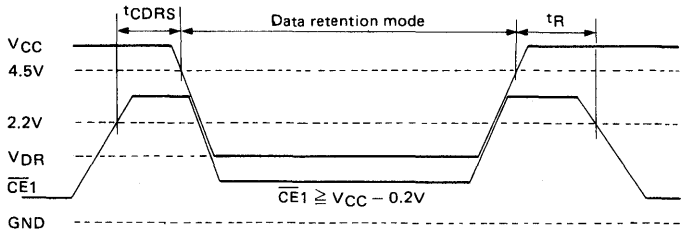
Ta=0 to +70°C

Item	Symbol	Test condition	CXK5971P/J -25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V *1	–	0.5	50	μA
	I_{CCDR2}	V_{CC}=2.0 to 5.5V *1	–	1.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	–	–	ns
Recovery time	t_R		t_{RC}*2	–	–	ns

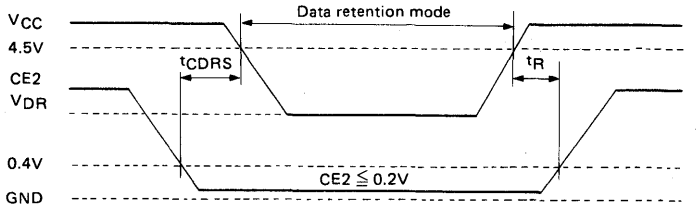
*1. $\overline{CE1} \geqq V_{CC}-0.2V$ or $CE2 \leqq 0.2V$,
$V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$

*2. t_{RC}: Read cycle time

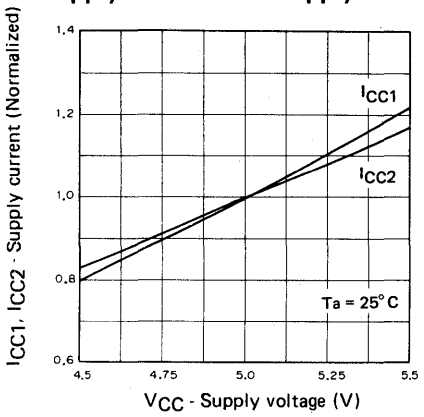
Data Retention Waveform (1): [$\overline{CE1}$ control]



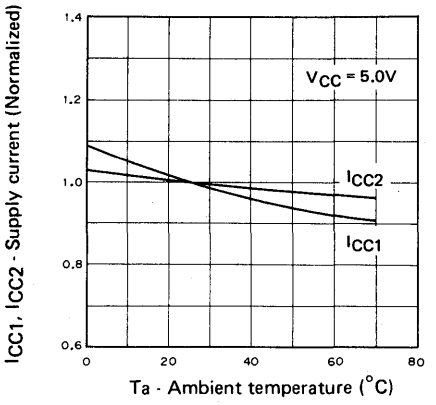
Data Retention Waveform (2): [CE2 control]



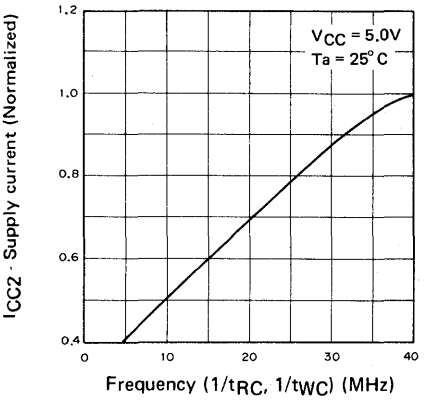
Supply current vs. Supply voltage



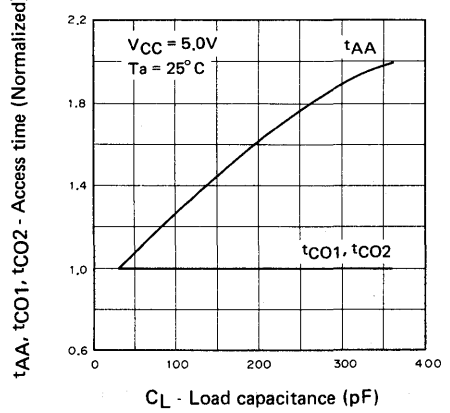
Supply current vs. Ambient temperature



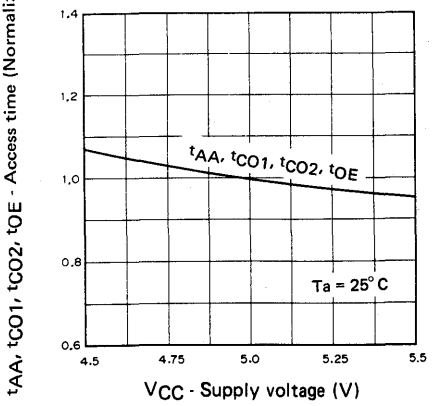
Supply current vs. Frequency



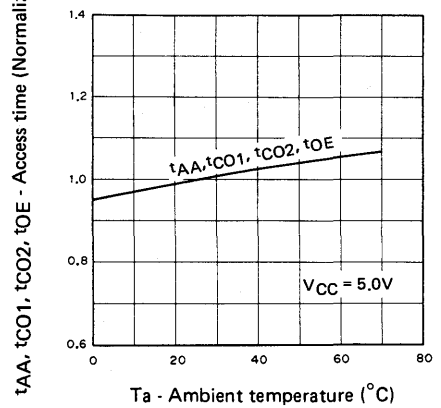
Access time vs. Load capacitance



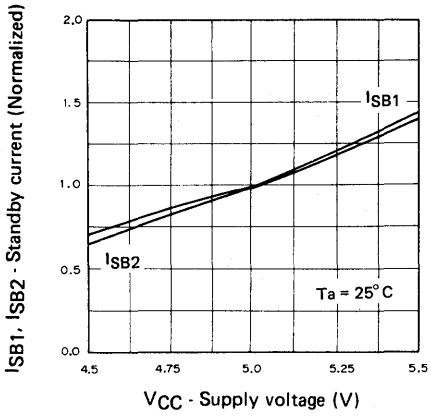
Access time vs. Supply voltage



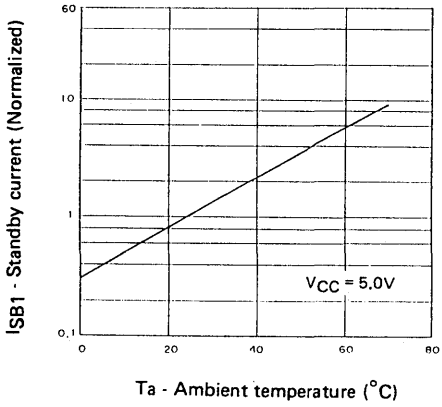
Access time vs. Ambient temperature



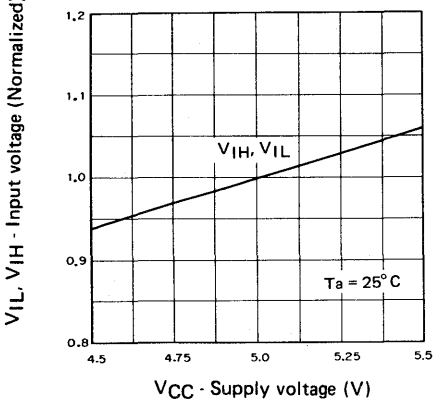
Standby current vs. Supply voltage



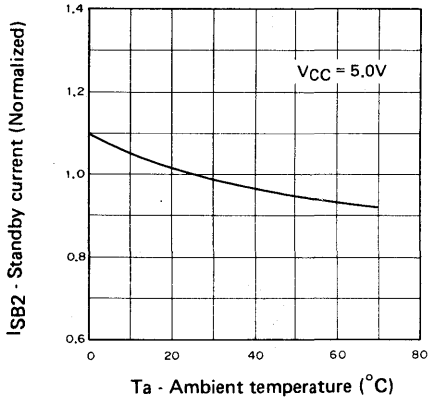
Standby current vs. Ambient temperature



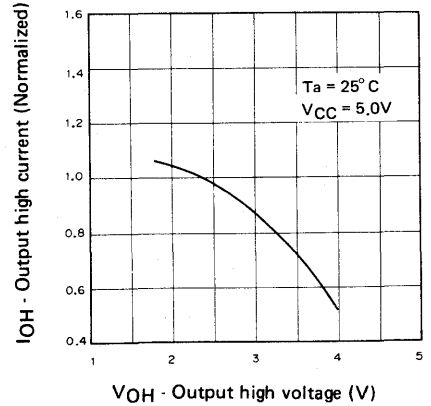
Input voltage vs. Supply voltage



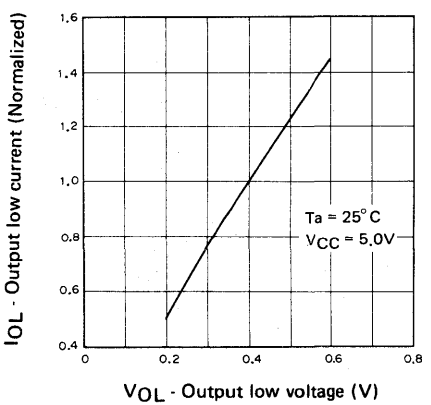
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



32768-word × 8 bit High Speed CMOS Static RAM

Description

CXK58257P/SP/M is a 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time:

	(Access time)
CXK58257P/SP/M-70L, 70LL	70ns (Max.)
CXK58257P/SP/M-85L, 85LL	85ns (Max.)
CXK58257P/SP/M-10L, 10LL	100ns (Max.)
CXK58257P/SP/M-12L, 12LL	120ns (Max.)

- Low power operation:
  CXK58257P/SP/M-70LL, 85LL, 10LL, 12LL;
  Standby/Operation: 5 μW (Typ.)/40 mW (Typ.)
  CXK58257P/SP/M-70L, 85L, 10L, 12L;
  Standby/Operation: 10 μW (Typ.)/40 mW (Typ.)
- Single +5V supply: +5V ±10%
- Fully static memory . . . No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28pin 600-mil DIP, 300-mil DIP and 450-mil SOP

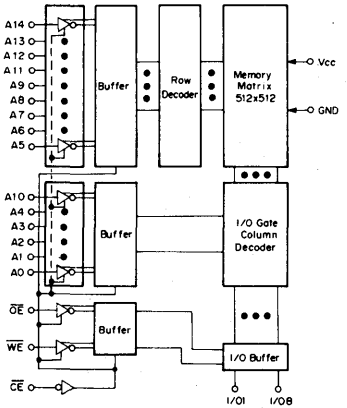
Function

32768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

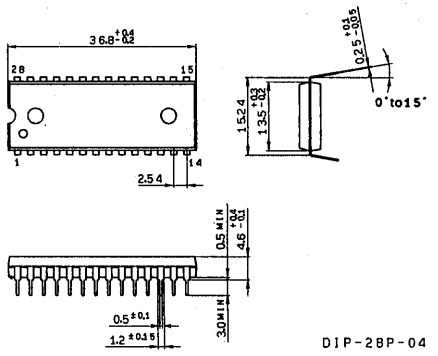
Block Diagram



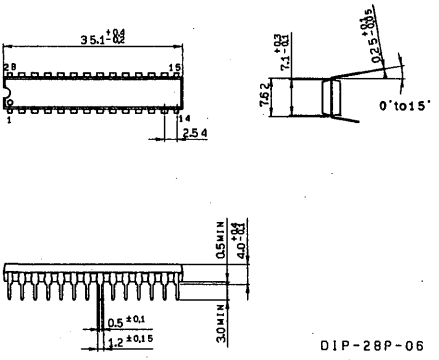
Package Outline

Unit: mm

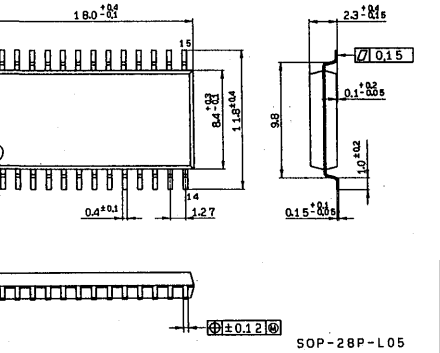
CXK58257P 28 Pin DIP (Plastic)



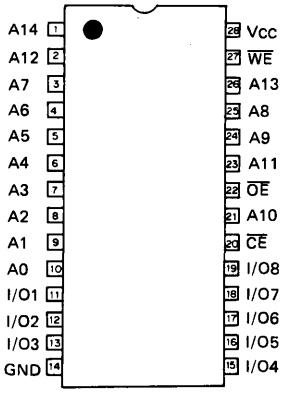
CXK58257SP 28 Pin DIP (Plastic)



CXK58257M 28 Pin SOP (Plastic)



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	Vcc		−0.5 to +7.0	V
Input voltage	VIN		−0.5* to Vcc+0.5	V
Input and output voltage	VI/O		−0.5* to Vcc+0.5	V
Allowable power dissipation	PD	CXK58257P/SP	1.0	W
		CXK58257M	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260·10	°C·sec

***Note)** VIN, VI/O=−3.0V Min. for pulse width less than 50 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not Selected	High Z	ISB1, ISB2
L	H	H	Output Disable	High Z	ICC1, ICC2
L	L	H	Read	Data out	ICC1, ICC2
L	X	L	Write	Data in	ICC1, ICC2

Note) X: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	VIH	2.2	−	Vcc+0.3	V
Input low voltage	VIL	−0.3*	−	0.8	V

***Note)** VIL=−3.0V Min. for pulse width less than 50 ns.

Electrical Characteristics

DC and operating characteristics

(Vcc=5V±10%, GND=0V, Ta=0 to+70°C)

Item	Symbol	Test condition		CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		−0.5	−	0.5	−0.5	−	0.5	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to Vcc		−0.5	−	0.5	−0.5	−	0.5	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		−	8	15	−	8	15	mA
		$\overline{CE}$≦0.2V V_{IN}≦0.2V or≧Vcc−0.2V		−	3	7	−	3	7	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	70L/70LL	−	45	70	−	45	70	mA
			85L/85LL	−	40	70	−	40	70	mA
			10L/10LL	−	35	70	−	35	70	mA
			12L/12LL	−	30	70	−	30	70	mA
Standby current	I_{SB1}	$\overline{CE}$≧Vcc−0.2V		−	0.002	0.1	−	0.001	0.05	mA
	I_{SB2}	$\overline{CE}$=V_{IH}		−	0.2	2	−	0.2	2	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.4	−	−	2.4	−	−	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		−	−	0.4	−	−	0.4	V

***Note)** Vcc=5V, Ta=25°C

Capacitance

(Ta=25°C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	−	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0V	−	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (Vcc=5V±10%, Ta=0 to +70°C)

Item		Condition
Input pulse high level		V_{IH}=2.2V
Input pulse low level		V_{IL}=0.8V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load	85L/85LL/10L/10LL 12L/12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL

* C_L includes scope and jig capacitances.

• **Read cycle**

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	–	85	–	100	–	120	–	ns
Address access time	t_{AA}	–	70	–	85	–	100	–	120	ns
Chip enable access time	t_{CO}	–	70	–	85	–	100	–	120	ns
Output enable to output valid	t_{OE}	–	35	–	45	–	50	–	60	ns
Output hold from address change	t_{OH}	5	–	5	–	10	–	10	–	ns
Chip enable to output in low Z($\overline{CE}$)	t_{LZ}	10	–	10	–	10	–	10	–	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	35	0	40	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	35	0	40	ns

***Note)** t_{HZ} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

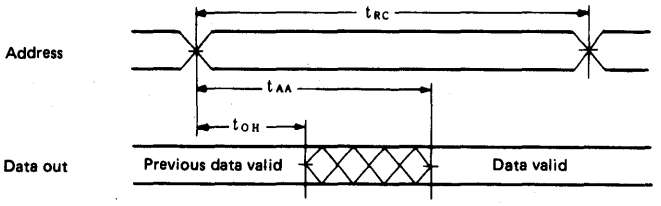
• **Write cycle**

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	–	85	–	100	–	120	–	ns
Address valid to end of write	t_{AW}	65	–	75	–	80	–	100	–	ns
Chip enable to end of write	t_{CW}	65	–	75	–	80	–	100	–	ns
Data to write time overlap	t_{DW}	30	–	40	–	40	–	50	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	55	–	60	–	70	–	80	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	–	0	–	0	–	0	–	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	–	0	–	0	–	0	–	ns
Output active from end of write	t_{OW}	5	–	5	–	10	–	10	–	ns
Write to output in high Z	t_{WHZ}*	0	30	0	30	0	30	0	30	ns

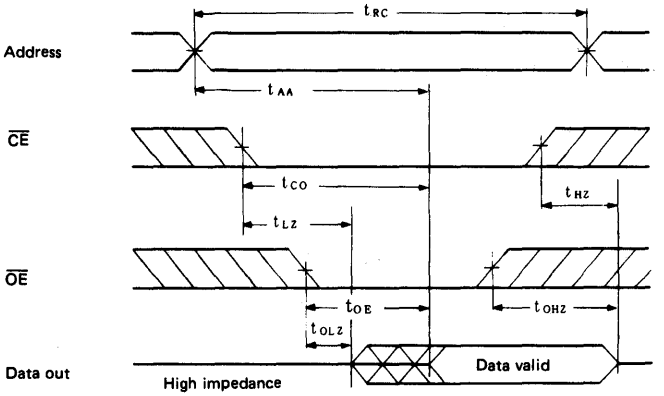
***Note)** t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

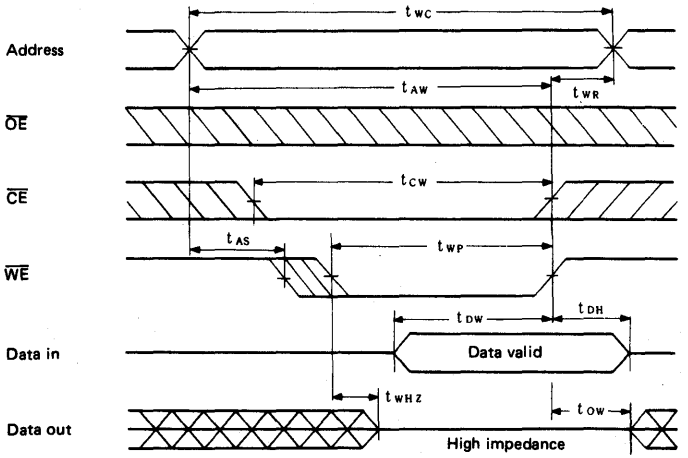
- Read cycle (1): $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



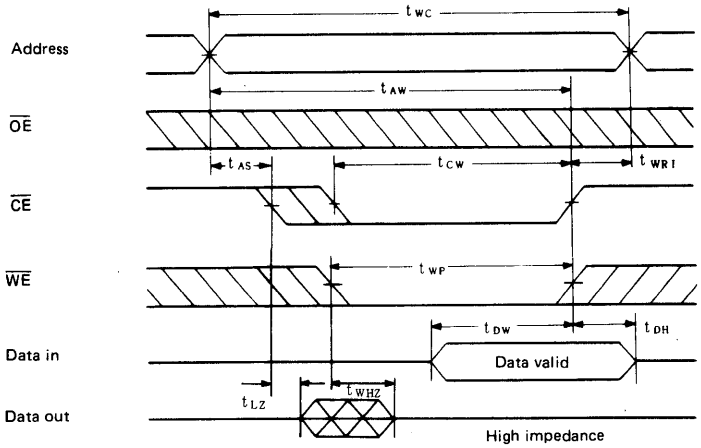
- Read cycle (2): $\overline{WE}=V_{IH}$



- Write cycle (1): $\overline{WE}$ control



- Write cycle (2): $\overline{CE}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

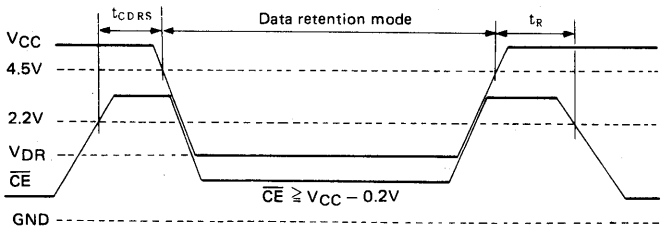
Data Retention Characteristics

(Ta=0 to 70°C)

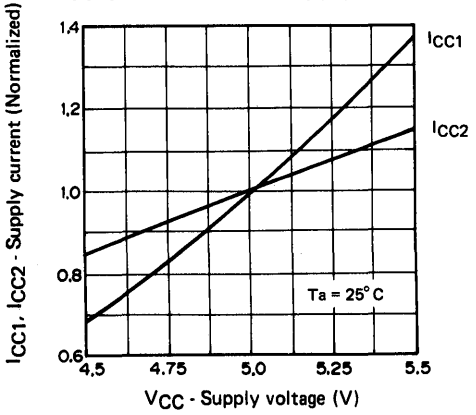
Item	Symbol	Test condition		CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$		2.0	–	5.5	2.0	–	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE} \geqq 2.8V$	Ta=0°C to 70°C	–	1	50	–	0.4	10	μA
			Ta=0 C to 50°C	–	–	–	–	0.4	5	
			25°C	–	–	–	–	0.4	1	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V, $\overline{CE} \geqq V_{CC}-0.2V$		–	0.002	0.1	–	0.001	0.05	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	–	–	0	–	–	ns
Recovery time	t_R			t_{RC}*	–	–	t_{RC}*	–	–	ns

* t_{RC}: Read cycle time

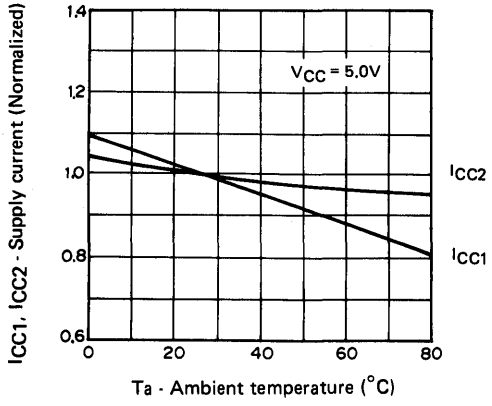
- **Data retention waveform**



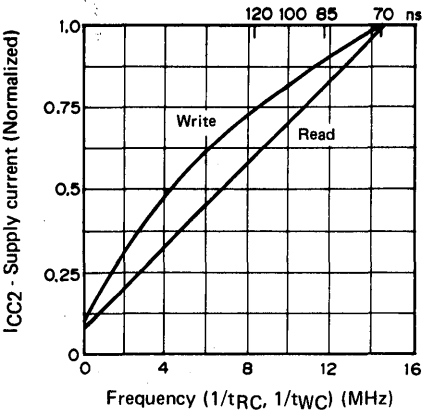
Supply current vs. Supply voltage



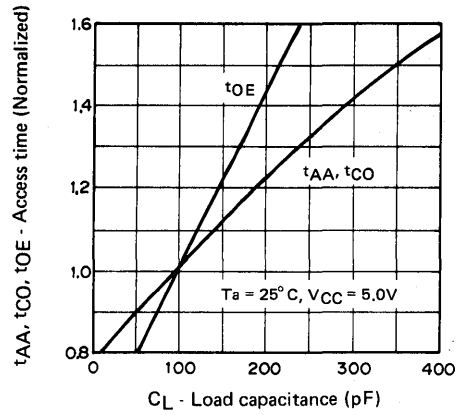
Supply current vs. Ambient temperature



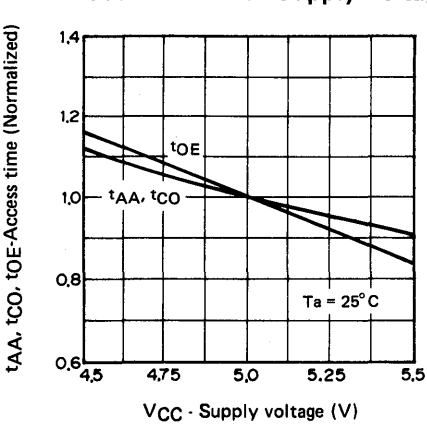
Supply current vs. Frequency



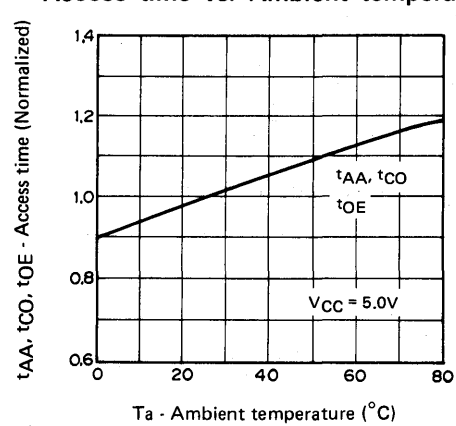
Access time vs. Load capacitance



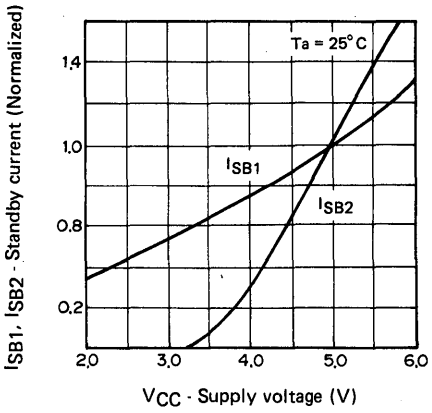
Access time vs. Supply voltage



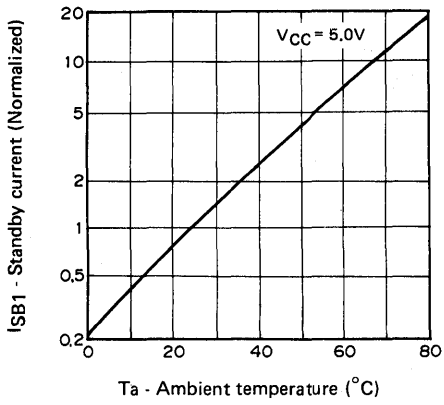
Access time vs. Ambient temperature



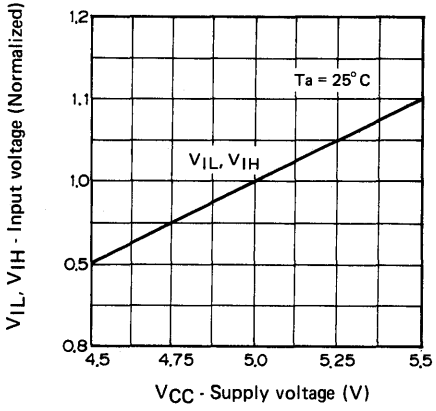
Standby current vs. Supply voltage



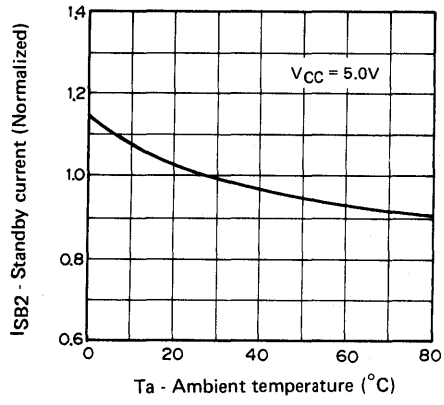
Standby current vs. Ambient temperature



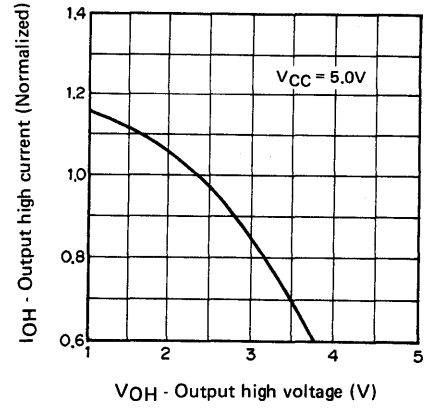
Input voltage vs. Supply voltage



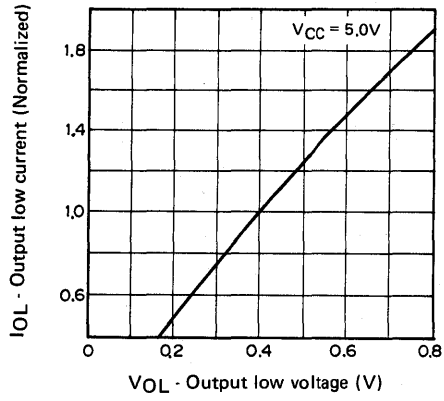
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



32768-word×8-bit High Speed CMOS Static RAM

Description

CXK58258P/SP are 262,144-bit high speed CMOS static RAMs suitable for use in high speed and low power applications.

Organized as 32,768 words by 8 bits, it operates from a single 5V supply.

Features

- Fast access time : (Access time)
  CXK58258P/SP-35 35ns (Max.)
  CXK58258P/SP-45 45ns (Max.)
  CXK58258P/SP-55 55ns (Max.)
- Low power operation : (Standby) (Operation)
  CXK58258P/SP-35, 45, 55
  50 μW(Typ.) 250mW(Typ.)
- Single +5V supply : +5V±10%
- Fully static memory ••• No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 28 pin 600-mil DIP and 300-mil DIP.

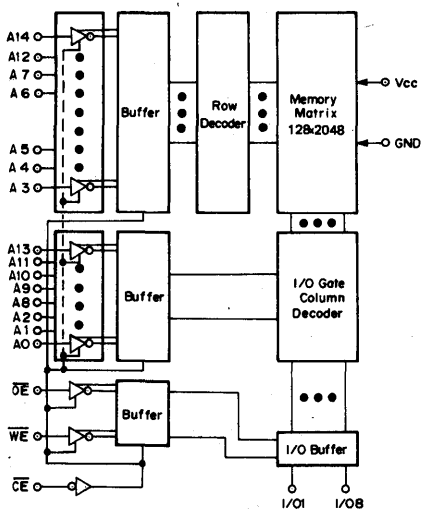
Function

- 32768-word×8-bit static RAM

Structure

Silicon gate CMOS IC

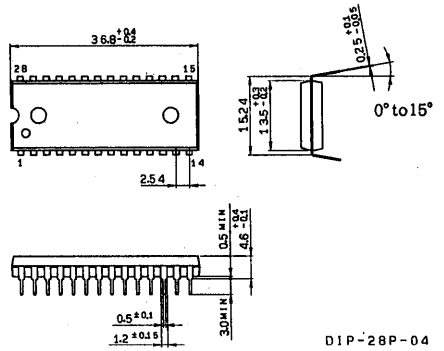
Block Diagram



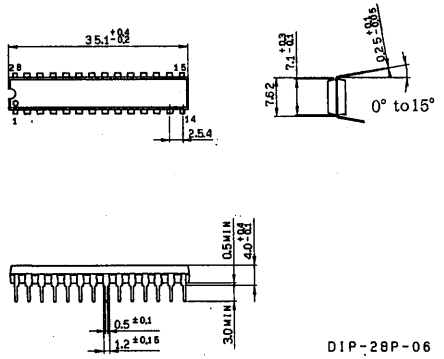
Package Outline

Unit : mm

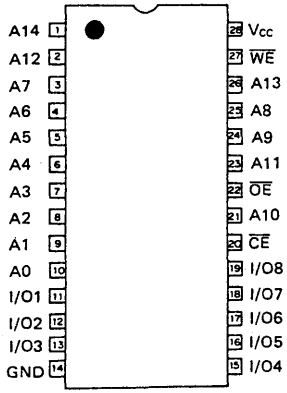
CXK58258P 28 pin DIP (Plastic) (600-mil)



CXK58258SP 28 pin DIP (Plastic) (300-mil)



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC}+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • Time	Tsolder	260 • 10	°C • sec

∗**Note**) V_{CC}, V_{IN}, $V_{I/O}$=−3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	X	L	Write	Data in	I_{CC1}, I_{CC2}

Note) X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	−	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*	−	0.8	V

∗**Note**) V_{IL}=−3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(Vcc=5V±10%, GND=0V, Ta=0 to +70℃)

Item	Symbol	Test condition	CXK58258P/SP-35/45/55			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN}=GND to V_{CC}	−2	−	2	μA
Output leak current	I_{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{I/O}$=GND to V_{CC}	−2	−	2	μA
Operating supply current	I_{CC1}	$\overline{CE}=V_{IL}$, $V_{IN}=V_{IH}$ or V_{IL}, I_{OUT}=0mA	−	50	80	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	−	90	140	mA
Standby current	I_{SB1}	$\overline{CE}\geqq V_{CC}-0.2V$	−	0.01	2	mA
	I_{SB2}	$\overline{CE}=V_{IH}$	−	−	10	
Output high voltage	V_{OH}	I_{OH}=−4.0mA	2.4	−	−	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	−	−	0.4	V

*Note) Vcc=5V, Ta=25℃

I/O capacitance

(Ta=25℃, f=1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	−	5	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	−	7	pF

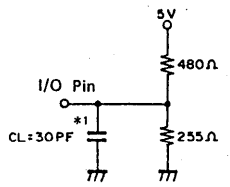
Note) This parameter is sampled and not 100% tested.

AC characteristics

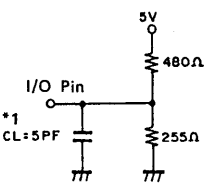
• **AC test conditions** Vcc=5V±10%, Ta=0 to +70℃

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



*1. C_L includes scope and jig capacitances.

*2. For t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

• **Read cycle**

Item	Symbol	CXK58258P/SP-35		CXK58258P/SP-45		CXK58258P/SP-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	–	45	–	55	–	ns
Address access time	t_{AA}	–	35	–	45	–	55	ns
Chip enable access time	t_{CO}	–	35	–	45	–	55	ns
Output enable to output valid	t_{OE}	–	20	–	25	–	30	ns
Output hold from address change	t_{OH}	5	–	5	–	5	–	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	–	5	–	5	–	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	–	0	–	0	–	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	–	15	–	20	–	25	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	–	15	–	20	–	25	ns
Power up time	t_{PU}	0	–	0	–	0	–	ns
Power down time	t_{PD}	–	35	–	45	–	55	ns

∗**Note**) Transition is measured ±500mV from steady voltage with specified loading in Fig.1-(2). This parameter is sampled and is not 100% tested.

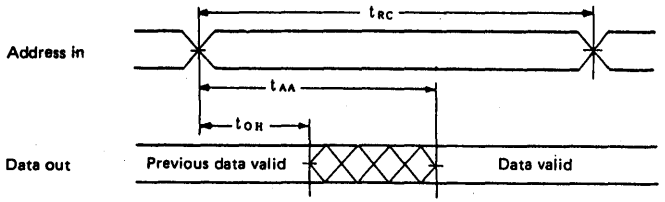
• **Write cycle**

Item	Symbol	CXK58258P/SP-35		CXK58258P/SP-45		CXK58258P/SP-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	–	45	–	55	–	ns
Address valid to end of write	t_{AW}	30	–	40	–	45	–	ns
Chip enable to end of write	t_{CW}	35	–	40	–	45	–	ns
Data to write time overlap	t_{DW}	18	–	20	–	20	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	30	–	35	–	35	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	ns
Output active from end of write	t_{OW}*	5	–	5	–	5	–	ns
Write to output in high Z	t_{WHZ}*	–	12	–	15	–	15	ns

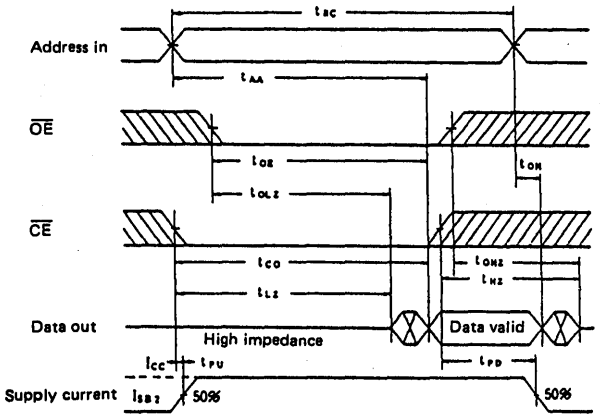
∗**Note**) Transition is measured ±500mV from steady voltage with specified loading in Fig.1-(2). This parameter is sampled and is not 100% tested.

Timing Waveform

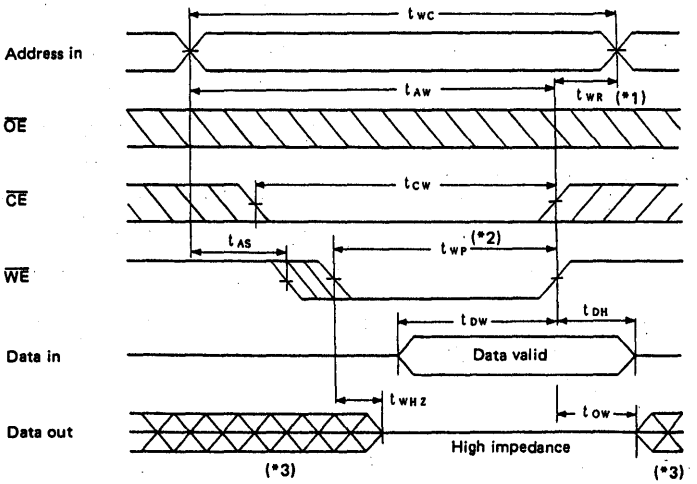
• Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



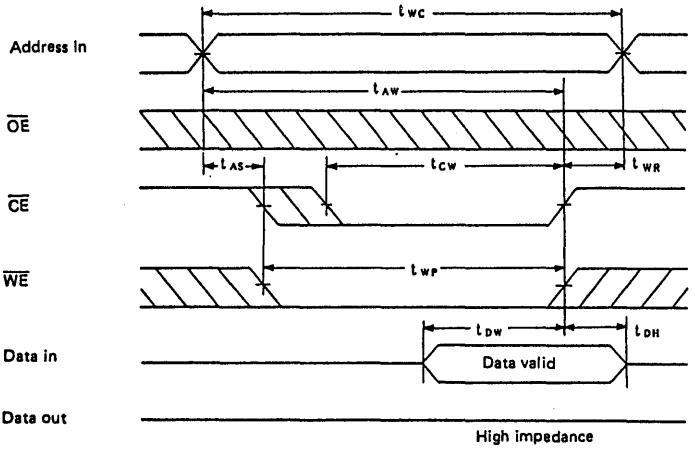
• Read cycle (2) : $\overline{WE}=V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



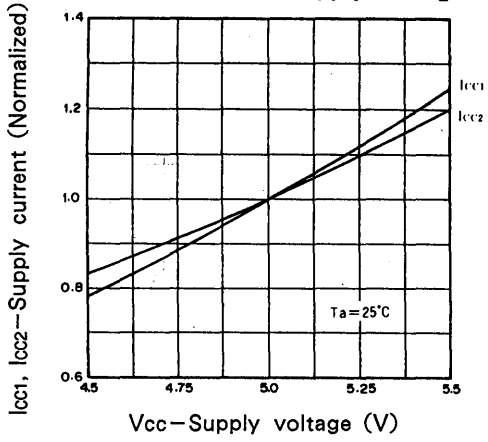
Note)

*1. t_{WR} is measured from the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.

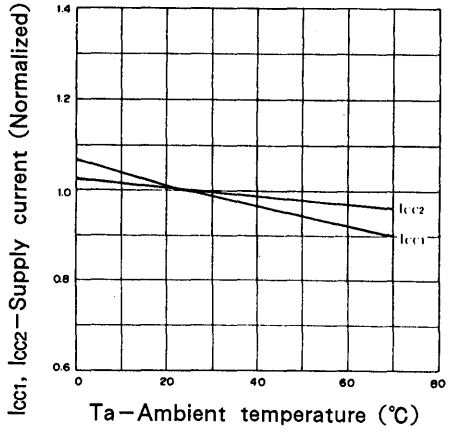
*2. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.

*3. While I/O pins are in output state, do not apply data input signals of opposite phase to the output.

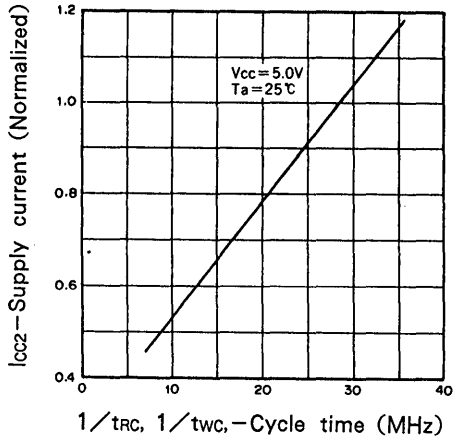
Supply current vs. Supply voltage



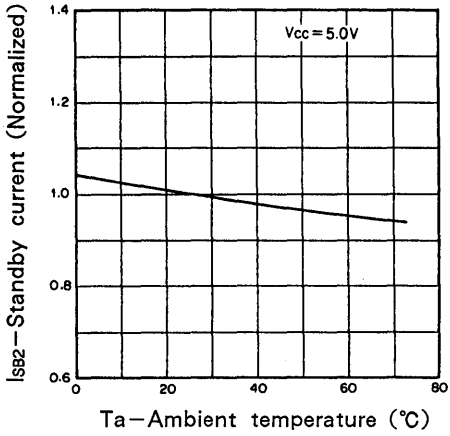
Supply current vs. Ambient temperature



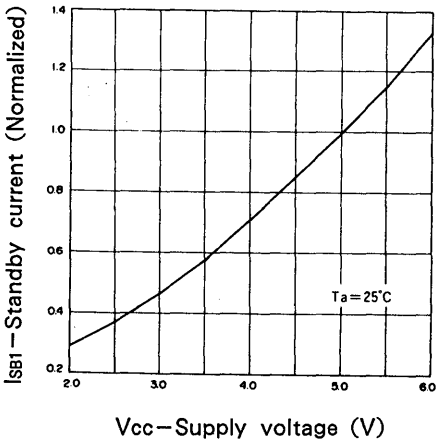
Supply current vs. Cycle time



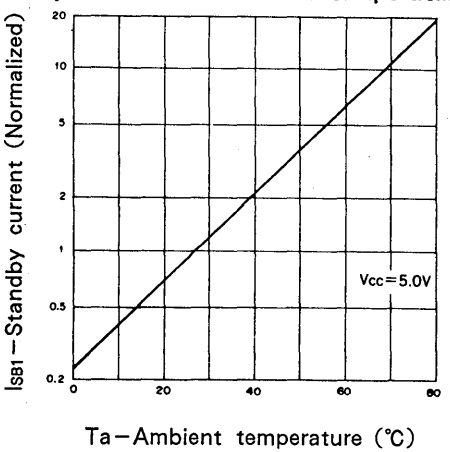
Standby current vs. Ambient temperature



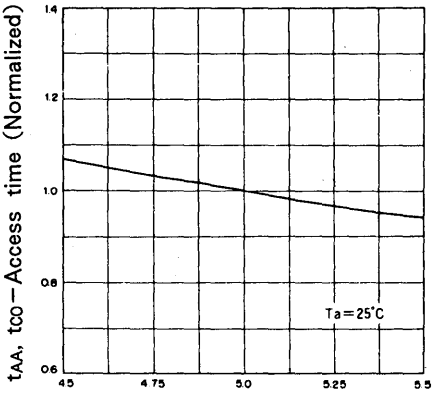
Standby current vs. Supply voltage



Standby current vs. Ambient temperature

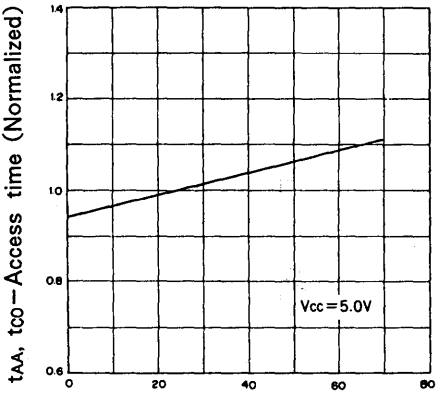


Access time vs. Supply voltage



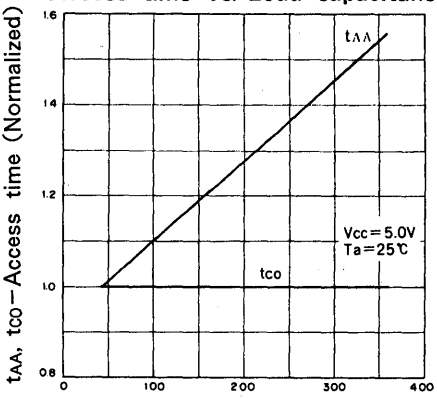
Vcc—Supply voltage (V)

Access time vs. Ambient temperature



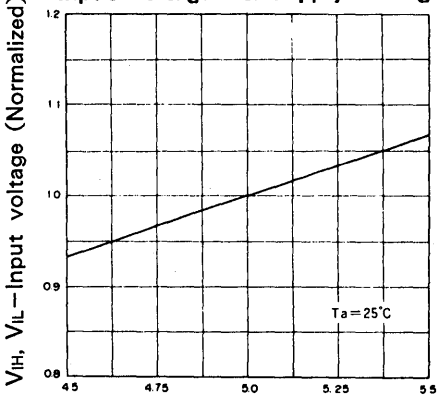
Ta—Ambient temperature (°C)

Access time vs. Load capacitance



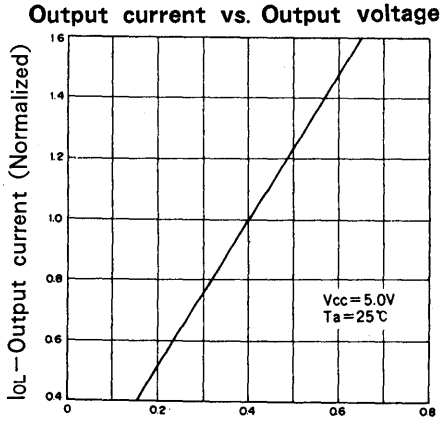
CL—Load capacitance (pF)

Input voltage vs. Supply voltage



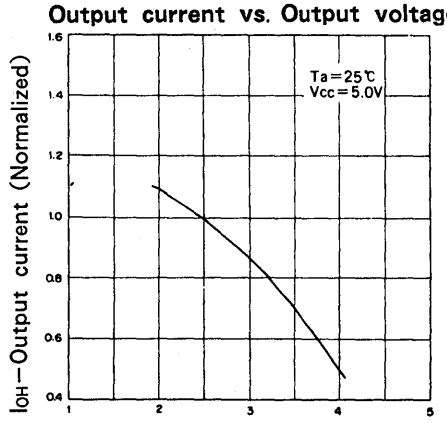
Vcc—Supply voltage (V)

Output current vs. Output voltage



VOL—Output voltage (V)

Output current vs. Output voltage



VOH—Output voltage (V)

32768-word × 8 bit High Speed CMOS Static RAM **Preliminary**

Description

CXK58255AP and CXK58255AJ are 262,144 bits high speed CMOS static RAMs organized as 32, 768 words by 8bits and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time (Access time)
  CXK58255AP/AJ-25 25ns (Max.)
  CXK58255AP/AJ-30 30ns (Max.)
- Low power standby 10μW (Typ.)
- Low power operation 200mW (Typ.)
- Single +5V supply
- Fully static memory.... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: 3-state output.
- Low voltage data retention: 2.0V (Min.)
- Directly TTL compatible: All input and outputs.
- Full CMOS
- Operating temperature Topr 0 to 70°C

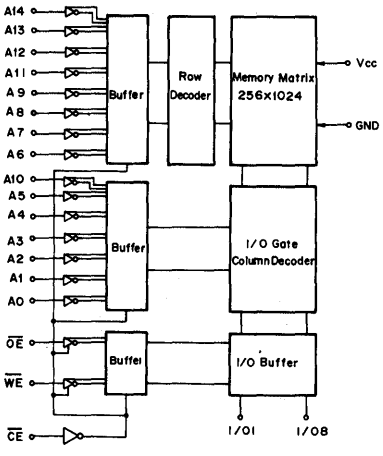
Function

32,768 word×8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

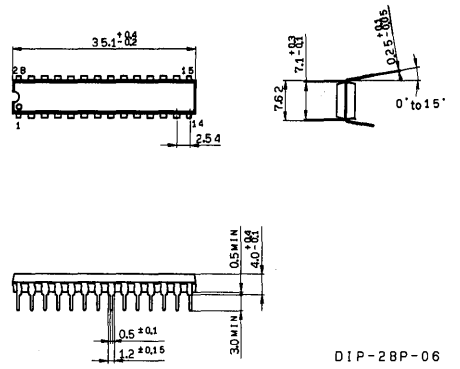


Note) All typ. values are measured under the conditions Vcc=5.0V and Ta=25°C

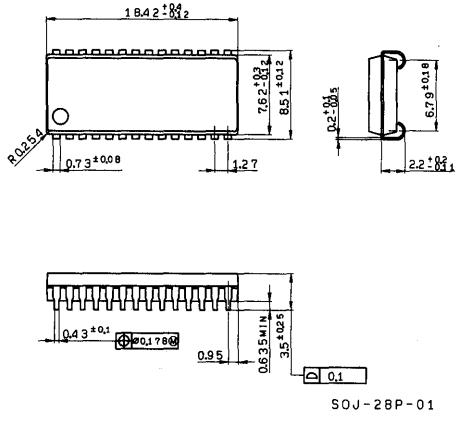
Package Outline

Unit: mm

CXK58255AP 28pin DIP(Plastic)

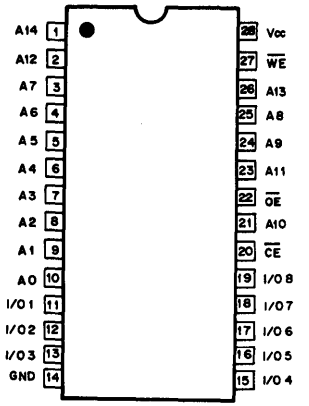


CXK58255AJ 28pin SOJ(Plastic)



P80960-HP

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply+5V
GND	Ground

Absolute Maximum Ratings

Ta=25°C, GND=0V

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 to V_{CC}+0.5	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Soldering temperature	T_{solder}	260 • 10	°C • sec
Allowable power dissipation	P_D	1.0	W

***Note)** V_{CC}, V_{IN}, $V_{I/O}$ (Min.)=−3.5V at pulse width less than 20 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	D out	I_{CC1}, I_{CC2}
L	X	L	Write	D in	I_{CC1}, I_{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	H_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

***Note)** V_{IL} (Min.) =−3.0V at pulse width less than 20ns.

Electrical Characteristics
DC characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK58255AP/AJ 25/30			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN}=GND to V_{CC}	−1	—	1	μA
Output leak current	I_{LO}	$V_{I/O}$=GND to V_{CC}, $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL} V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	—	40	80	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0mA	—	70	120	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	2	100	μA
	I_{SB2}	$\overline{CE}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V

*) V_{CC}=5V, Ta=25°C

I/O capacitance

Ta=25°C, f=1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics
- **AC test conditions**

V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse "High" level	V_{IH}=3.0V
Input pulse "Low" level	V_{IL}=0V
Input rise time	t_r=5ns
Input fall time	t_f=5ns
Input and output reference level	1.5V
Output load	Fig. 1

*1. C_L includes scope and jig capacitances.
*2. For t_{LZ} t_{HZ}, t_{OHZ}, t_{OW}, t_{WHZ}.

Load condition (1) Load condition (2)*2

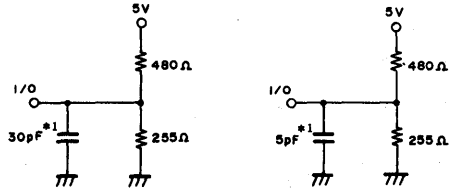


Fig. 1

*1. C_L includes scope and jig capacitances.
*2. For t_{LZ} t_{HZ}, t_{OHZ}, t_{OW}, t_{WHZ}.

• **Read cycle**

Item	Symbol	CXK58255AP/AJ −25		CXK58255AP/AJ −30		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	ns
Address access time	t_{AA}	—	25	—	30	ns
Chip enable access time	t_{CO}	—	25	—	30	ns
Output enable access time	t_{OE}	—	12	—	15	ns
Output data hold time	t_{OH}	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	—	15	—	15	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	13	—	13	ns
Chip enable to power up time	t_{PU}	0	—	0	—	ns
Chip disable to powe down time	t_{PD}	—	20	—	20	ns

***Note)** Transition is measured by ±500 mV from the normal state with the load circuit Fig. 1.
This paramerter is sampled and is not 100% tested.

• **Write cycle**

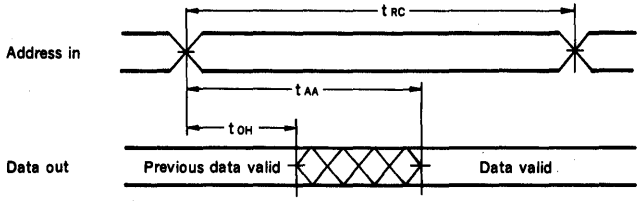
Item	Symbol	CXK58255AP/AJ −25		CXK58255AP/AJ −30		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	ns
Chip enable to end of write	t_{CW}	20	—	20	—	ns
Data setup time	t_{DW}	12	—	12	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	20	—	ns
Address set up time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}*	0	—	0	—	ns
Write to output in high Z	t_{WHZ}*	—	13	—	13	ns

***Note)** Transition is measured by ±500 mV from the normal state with the load circuit Fig. 1.
This paramerter is sampled and is not 100% tested.

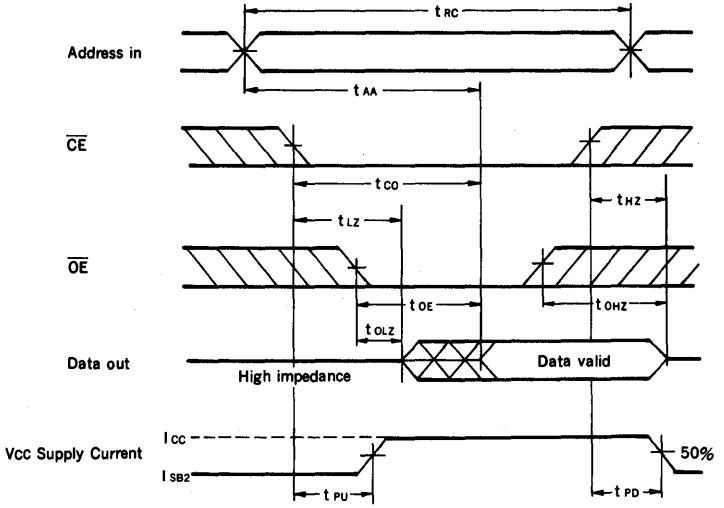
Timing Waveform

1. Read cycle

- Read cycle No. 1 [$\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}]

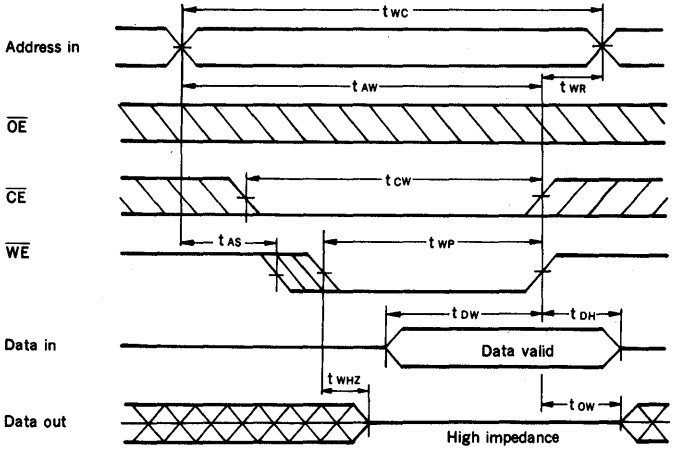


- Read cycle No. 2 [$\overline{WE}$=V_{IH}]

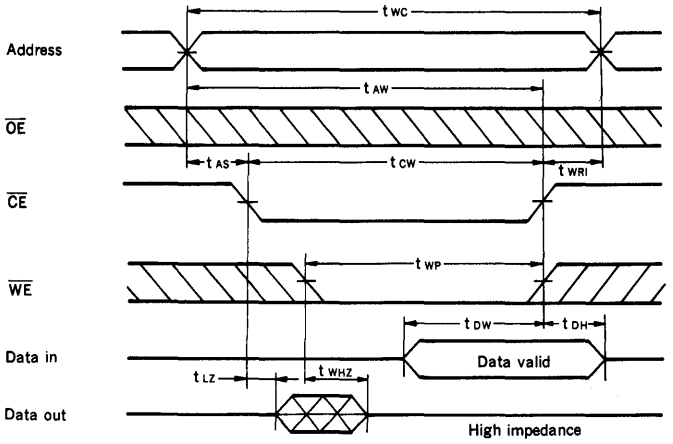


2. Write cycle

- Write cycle No. 1 [$\overline{WE}$ control]



• Write cycle No. 2 [$\overline{CE}$ control]



Note)

1. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

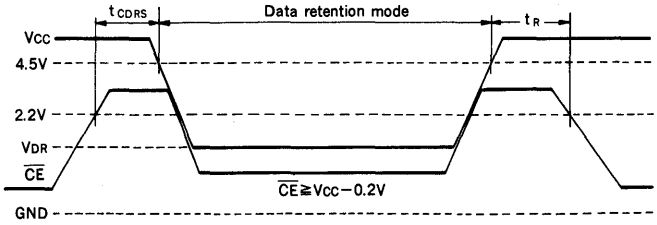
Data Retention Characteristics

Ta=0 to +70°C

Item	Symbol	Test condition	CXK58255AP/AJ 25/30			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V *1	—	1.0	50	μA
	I_{CCDR2}	V_{CC}=2.0 to 5.5V *1	—	2.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

*1. $\overline{CE} \geqq V_{CC}-0.2V$
*2. t_{RC}: Read Cycle Time

Data Retention Waveform



65,536-word × 4 bit High Speed CMOS Static RAM

Description

CXK54256P is a 262, 144 bits high speed CMOS static RAM organized as 65,536 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

- Fast access time (Access time)
  CXK54256P-35 35 ns (Max.)
  CXK54256P-45 45 ns (Max.)
  CXK54256P-55 55 ns (Max.)
- Low power consumption (operation): 100 mW (Typ.)
- Single +5V supply: 5V ± 10%
- Fully static memory . . . . No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- High density: 300 mil 24 pin plastic package

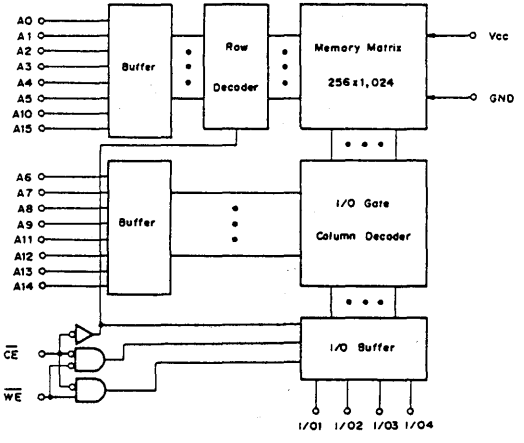
Function

65,536-word × 4 bit static RAM

Structure

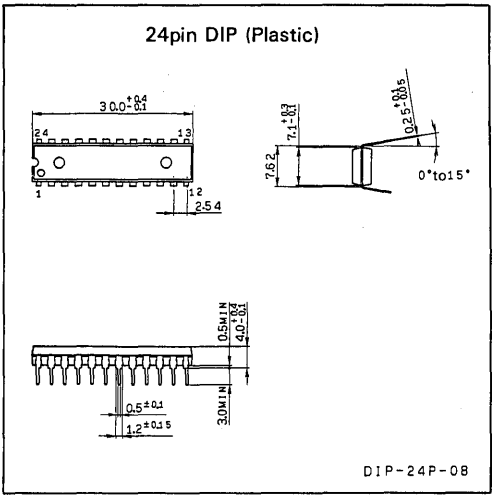
Silicon gate CMOS IC

Block Diagram

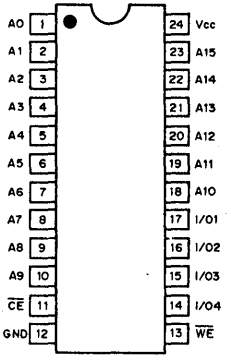


Package Outline

Unit: mm



Pin Configuration (Top View)



Symbol	Description
A0 to A15	Address input
I/O 1 to I/O 4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

Ta = 25°C, GND = 0V

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC}+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	260 • .10	°C • sec

* **Note)** V_{CC}, V_{IN}, $V_{I/O}$ Min. = −3.5V for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O 1 to I/O 4	V_{CC} current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	D_{OUT}	I_{CC1}, I_{CC2}
L	L	Write	D_{IN}	I_{CC1}, I_{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

Note) *1. V_{CC} = 5V, Ta = 25°C

*2. V_{IL} Min. = −3.0V for pulse width less than 20 ns.

DC and Operating Characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK54256P -35/45/55			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC} V_{CC}=5.5V	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} $V_{I/O}$=GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0 mA V_{IN}=V_{IH}/V_{IL}	—	20	45	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0 mA	—	55	85	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	—	2	mA
	I_{SB2}	$\overline{CE}$=V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0 mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0 mA	—	—	0.4	V

*V_{CC}=5V, Ta=25°C

I/O Capacitance

Ta=25°C, f=1 MHz

Item	Test Condition	Symbol	Min.	Max.	Unit
Input capacitance	V_{IN}=0V	C_{IN}	—	7	pF
Input/Output capacitance	$V_{I/O}$=0V	$C_{I/O}$	—	7	pF

Note) This parameter is sampled and is not 100% tested.

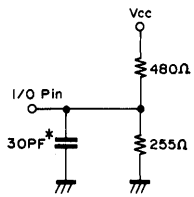
AC Operating Characteristics

- **AC test condition**

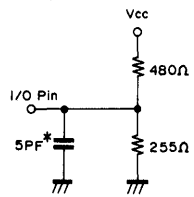
V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_R=5 ns
Input fall time	t_F=5 ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)**



* Including scope and jig

** For t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

Read Cycle

Item	Symbol	CXK54256P -35		CXK54256P -45		CXK54256P -55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	—	45	—	55	—	ns
Address access time	t_{AA}	—	35	—	45	—	55	ns
Chip enable access time($\overline{CE}$)	t_{CO}	—	35	—	45	—	55	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	15	0	15	0	20	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	30	—	30	—	30	ns

***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

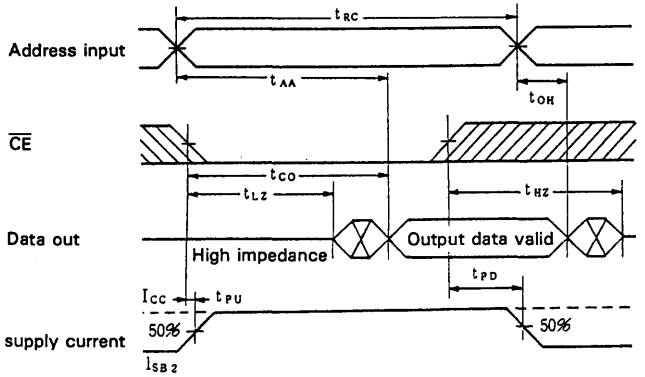
Write Cycle

Item	Symbol	CXK54256P -35		CXK54256P -45		CXK54256P -55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t_{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t_{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t_{DW}	15	—	20	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	30	—	35	—	45	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	15	0	15	0	20	ns

***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

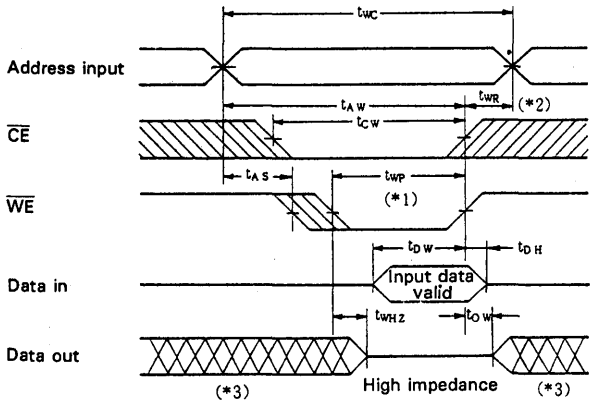
Timing Waveform

1) Read cycle [$\overline{WE}$ = V_{IH}]

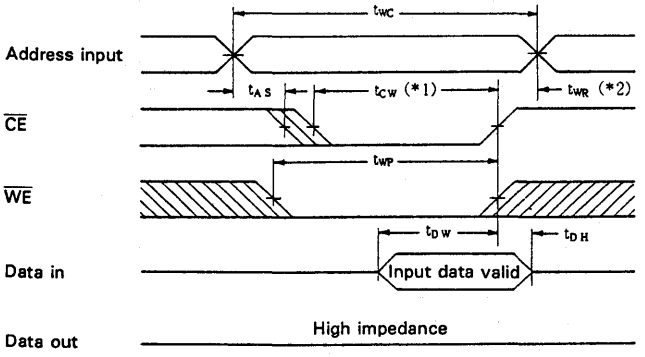


2) Write cycle

- Write Cycle 1.



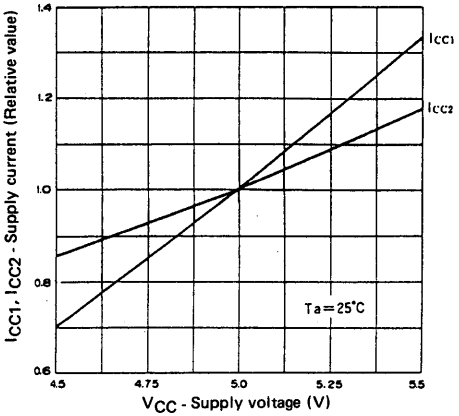
- Write Cycle 2: [$\overline{CE}$ = V_{IL}]



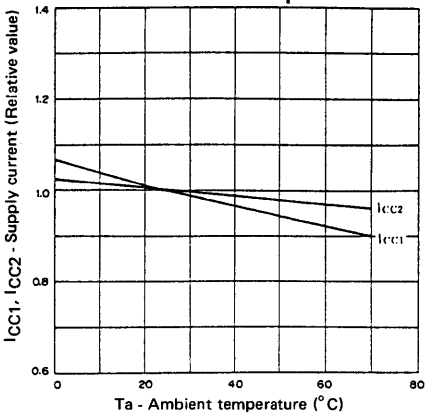
*** Note)**

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

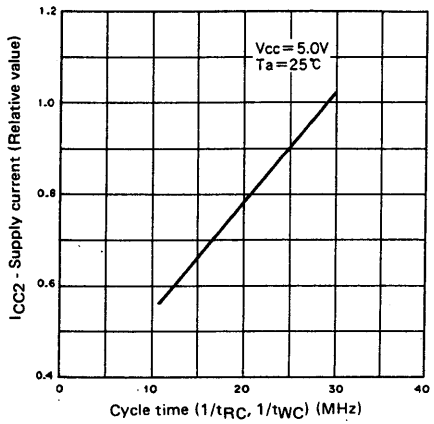
Supply current vs. Supply voltage



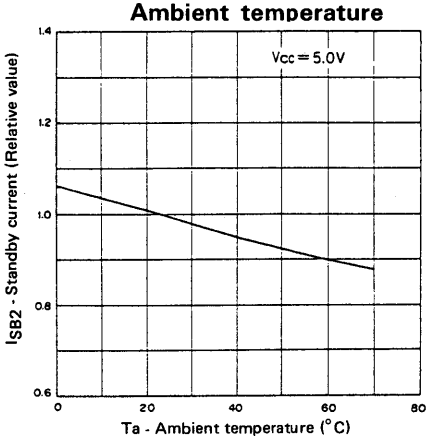
Supply current vs. Ambient temperature



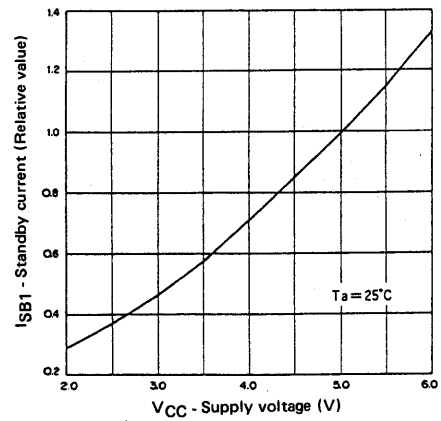
Supply current vs. Cycle time



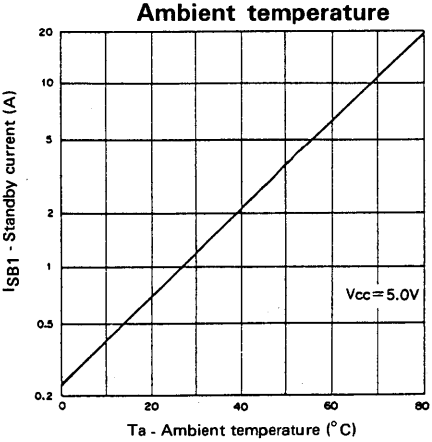
Standby current vs. Ambient temperature



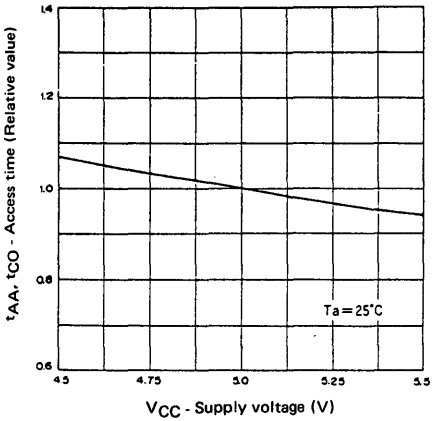
Standby current vs. Supply voltage



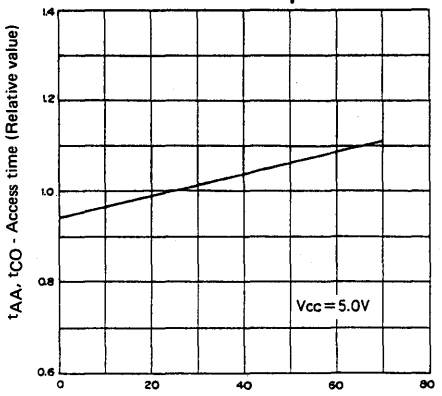
Standby current vs. Ambient temperature



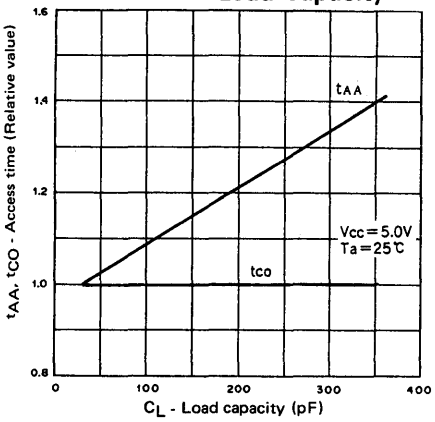
Access time vs. Supply voltage



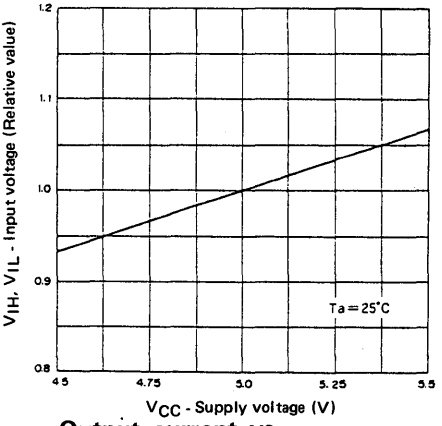
Access time vs. Ambient temperature



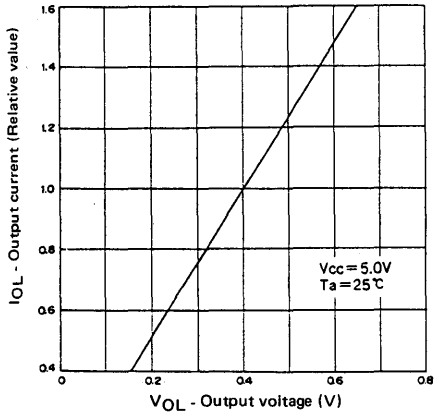
Access time vs. Load capacity



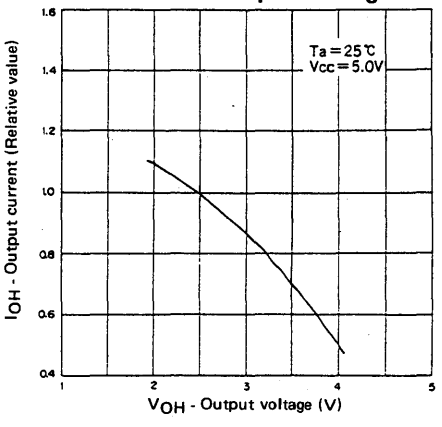
Input voltage vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



262,144-word × 1bit High Speed CMOS Static RAM

Description

CXK51256P is a 262,144 bits high speed CMOS static RAM organized as 262,144 words by 1 bit and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

- Fast access time (Access time)
  CXK51256P-35 35ns (Max.)
  CXK51256P-45 45ns (Max.)
  CXK51256P-55 55ns (Max.)
- Low power consumption (operation): 100 mW (Typ.)
- Single +5V supply: 5V ±10%
- Fully static memory . . . . No clock or timing strobe required.
- Equal access and cycle time.
- Separate data input and output.
- Three-state output
- Directly TTL compatible: All inputs and output.
- High density: 300 mil 24 pin plastic package

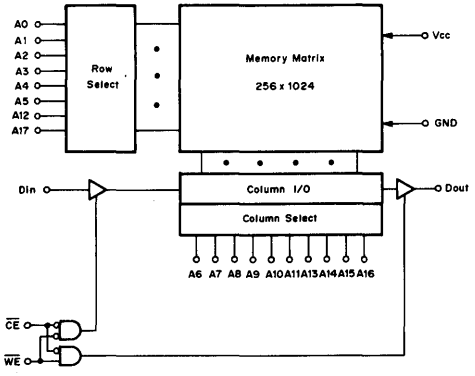
Function

262,144-word × 1 bit static RAM

Structure

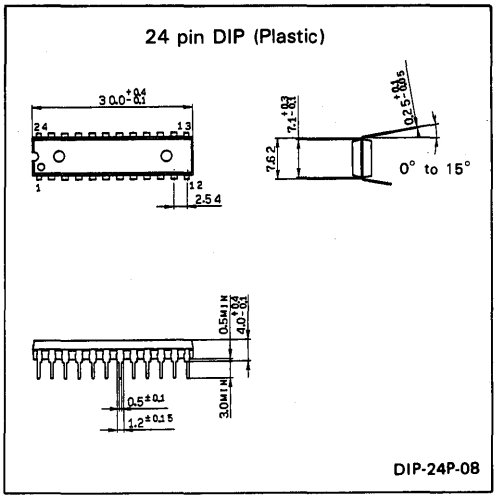
Silicon gate CMOS IC

Block Diagram

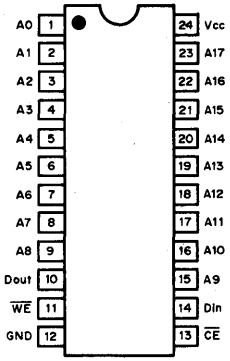


Package Outline

Unit: mm



Pin Configuration (Top View)



Symbol	Description
A0 to A17	Address input
Din	Data input
Dout	Data output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC}+0.5	V
Voltage applied to output	V_{OUT}	−0.5* to V_{CC}+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	260 • .10	°C • sec

***Note)** V_{CC}, V_{IN}, V_{OUT} min = −3.5V for pulse width less than 20 ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	Dout	Vcc Current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	D_{OUT}	I_{CC1}, I_{CC2}
L	L	Write	High Z	I_{CC1}, I_{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

Ta=0 to +70°C, GND=0V

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

Note) *1. V_{CC} = 5V, Ta = 25°C

*2. V_{IL} min = −3.0V for pulse width less than 20 ns.

DC and Operating Characteristics

V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C

Item	Symbol	Test condition	CXK51256P -35/45/55			Unit
			Min.	Typ.	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC} V_{CC}=5.5V	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} V_{OUT}=GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{OUT}=0 mA V_{IN}=V_{IH}/V_{IL}	—	20	45	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0 mA	—	55	85	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	—	2	mA
	I_{SB2}	$\overline{CE}$=V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0 mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0 mA	—	—	0.4	V

I/O Capacitance

Ta=25°C, f=1 MHz

Item	Test Condition	Symbol	Min.	Max.	Unit
Input capacitance	V_{IN}=0V	C_{IN}	—	7	pF
Output capacitance	V_{OUT}	C_{OUT}	—	7	pF

Note) This parameter is sampled and is not 100% tested.

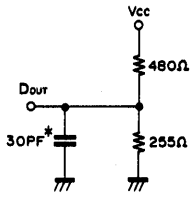
AC Operating Characteristics

- **AC test condition**

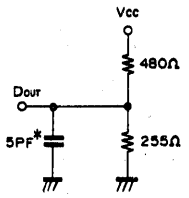
V_{CC}=5V±10%, Ta=0 to +70°C

Item	Condition
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_R=5 ns
Input fall time	t_F=5 ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)**



* Including scope and jig

** For t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

Read cycle

Item	Symbol	CXK51256P -35		CXK51256P -45		CXK51256P -55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	—	45	—	55	—	ns
Address access time	t_{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	35	—	45	—	55	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	20	0	20	0	25	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	30	—	30	—	30	ns

***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

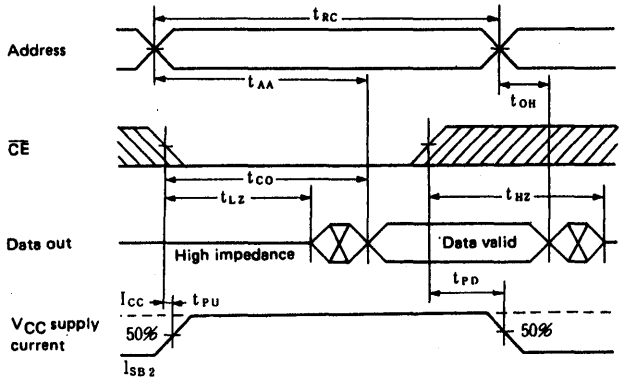
Write cycle

Item	Symbol	CXK51256P -35		CXK51256P -45		CXK51256P -55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t_{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t_{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t_{DW}	20	—	25	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	25	—	25	—	35	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	20	0	20	0	25	ns

***Note)** Transition is measured ±200 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

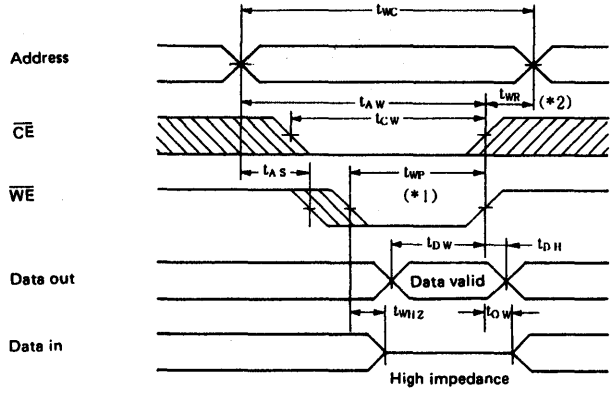
Timing Waveform

1) Read cycle [$\overline{WE}$=VIH]

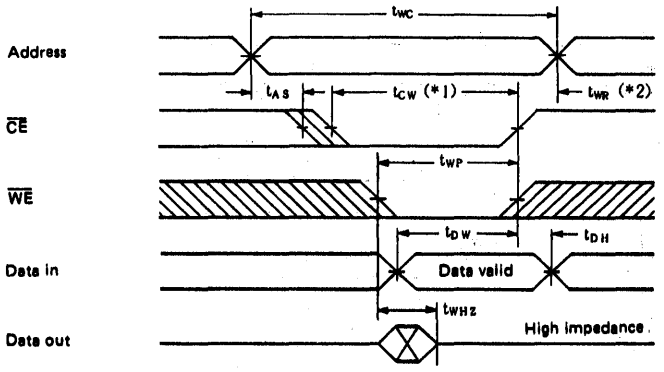


2) Write cycle

- **Write cycle 1 : $\overline{WE}$ Control**



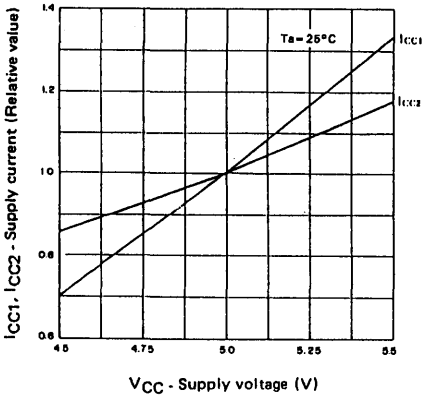
- Write Cycle 2: [$\overline{CE}$ = V_{IL}]



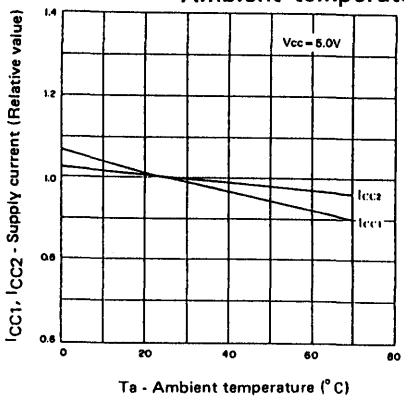
*** Note)**

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

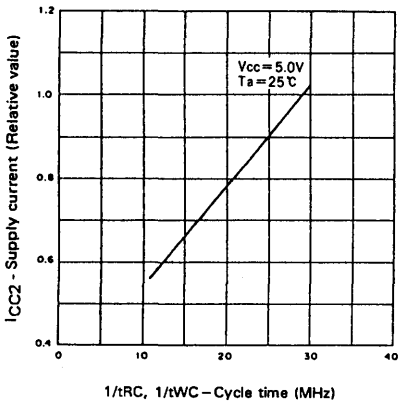
Supply current vs. Supply voltage



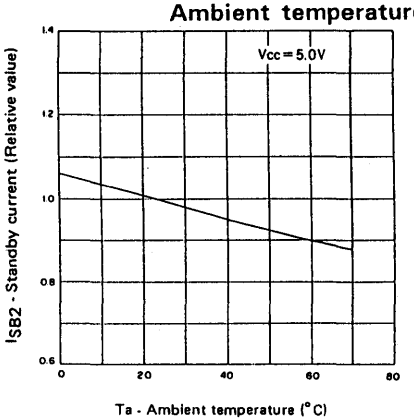
Supply current vs. Ambient temperature



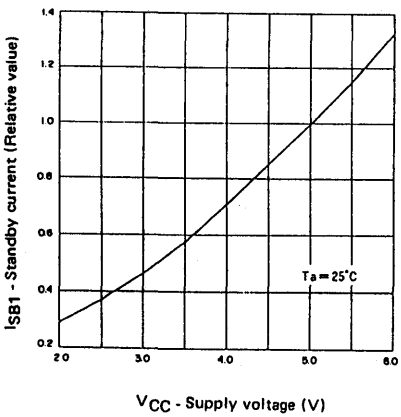
Supply current vs. Cycle time



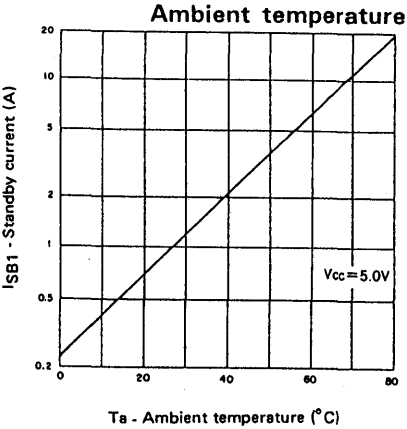
Standby current vs. Ambient temperature



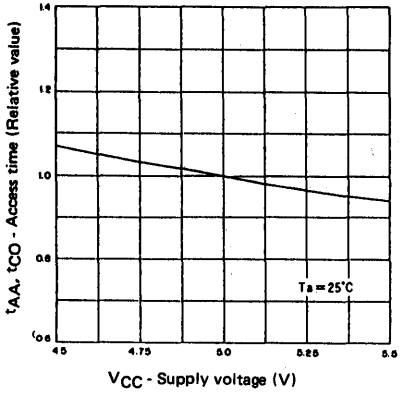
Standby current vs. Supply voltage



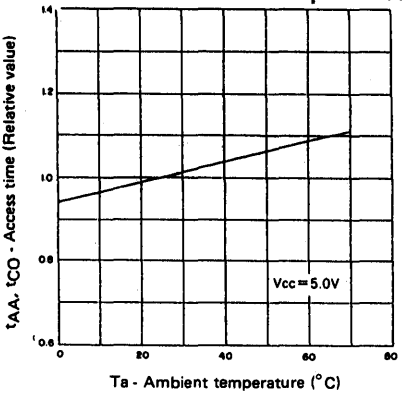
Standby current vs. Ambient temperature



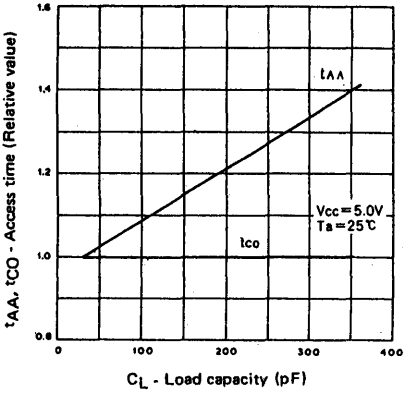
Access time vs. Supply voltage



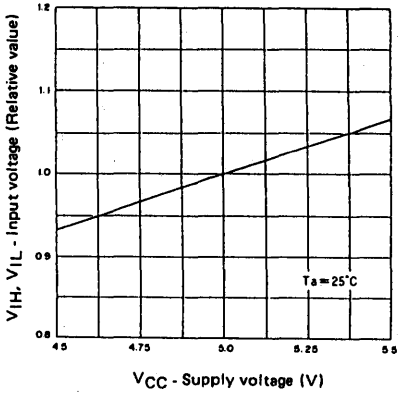
Access time vs. Ambient temperature



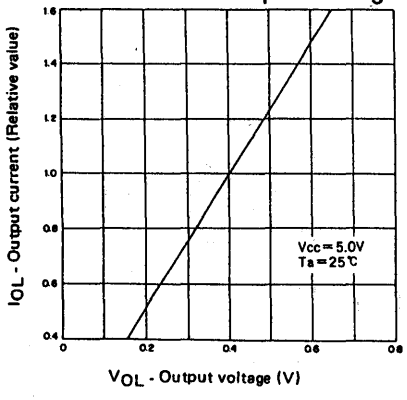
Access time vs. Load capacity



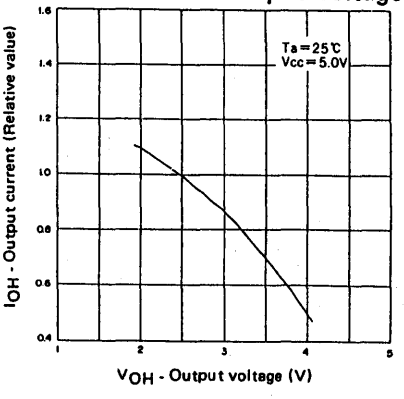
Input voltage vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



SONY CXK581000P/M 10L/12L/15L

131072-word × 8 bit High Speed CMOS Static RAM **Preliminary**

Description

CXK581000P/M is a 1,048,576 bits high speed CMOS static RAM organized as 131,072 words by 8 bits and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time : (Access time)
  CXK581000P/M-10L 100ns (Max.)
  CXK581000P/M-12L 120ns (Max.)
  CXK581000P/M-15L 150ns (Max.)
- Low power operation :
  CXK581000P/M-10L, 12L, 15L ; Standby/DC operation : 10 μ W (Typ.) /35mW (Typ.)
- Single + 5V supply : + 5V ± 10 %
- Fully static memory ··· No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581000P 600-mil 32pin DIP package
  CXK581000M 525-mil 32pin SOP package

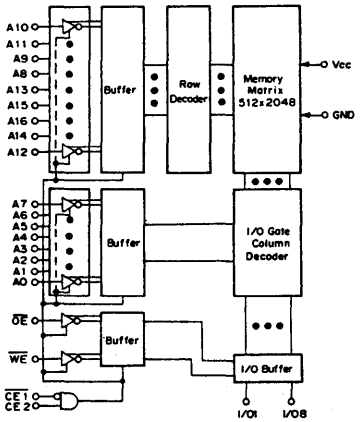
Function

- 131,072 word × 8 bit static RAM

Structure

Silicon gate CMOS IC

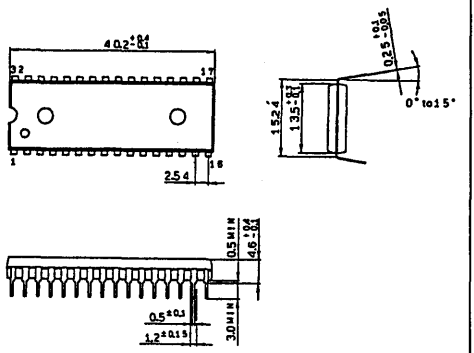
Block Diagram



Package Outline

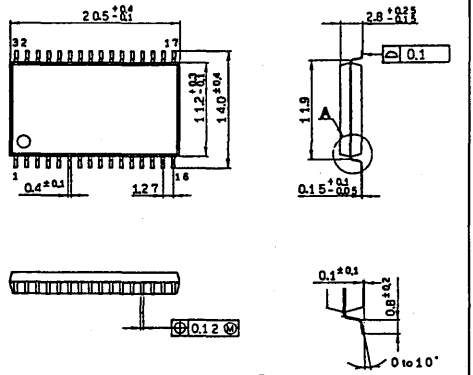
Unit : mm

CXK581000P 32 pin DIP (Plastic) (600-mil)



DIP-32P-01

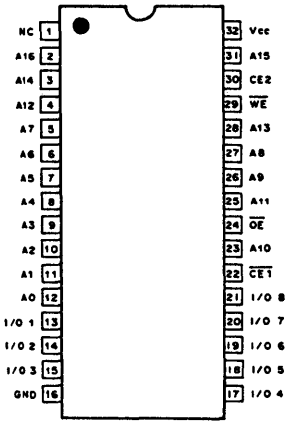
CXK581000M 32 pin SOP (Plastic) (525-mil)



Detailed diagram of A

SOP-32P-L02

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to + 7.0	V
Input voltage	V_{IN}		− 0.5 * to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK581000P	1.0	W
		CXK581000M	0.7	
Operating temperature	Topr		0 to + 70	°C
Storage temperature	Tstg		− 55 to + 150	°C
Soldering temperature	Tsolder		260 • 10	°C • sec

* **Note)** V_{IN}, $V_{I/O}$ = − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

Note) × : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

* **Note)** V_{IL} = − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

DC characteristics

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70℃)

Item	Symbol	Test condition		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA		—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty = 100% I_{OUT} = 0mA	Write cycle	—	35	60	mA
			Read cycle	—	25	40	
	I_{CC3}	Cycle time 1 μS Duty = 100% I_{OUT} = 0mA $\overline{CE1} \leqq 0.2V$, CE2 ≧ V_{CC} − 0.2V $V_{IL} \leqq 0.2V$, $V_{IH} \geqq V_{CC} - 0.2V$	Write cycle	—	10	20	mA
			Read cycle	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1} \geqq V_{CC} - 0.2V$ CE2 ≧ V_{CC} − 0.2V		—	2	100	μA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V

* **Note**) V_{CC} = 5V, Ta = 25℃

I/O capacitance

(Ta = 25℃, f = 1MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

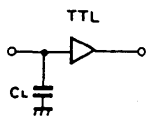
AC characteristics

• **AC test conditions** (V_{CC} = 5V ± 10%, Ta = 0 to +70℃)

Item	Condition
Input pulse high level	V_{IH} = 2.2V
Input pulse low level	V_{IL} = 0.8V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load	C_L * = 100pF, 1TTL

* **Note**) C_L includes scope and jig capacitances.

• **Test circuit**



• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	CXK581000 P/M-10L		CXK581000 P/M-12L		CXK581000 P/M-15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2}*	—	35	—	40	—	50	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	35	—	40	—	50	ns

* **Note)** t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

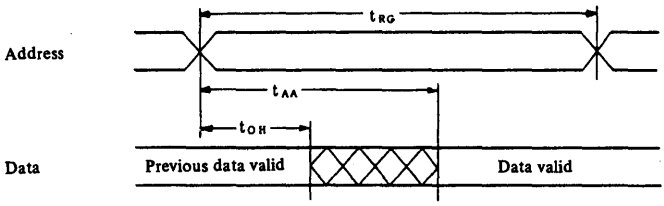
• **Write cycle**

Item	Symbol	CXK581000 P/M-10L		CXK581000 P/M-12L		CXK581000 P/M-15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ} *	—	30	—	30	—	30	ns

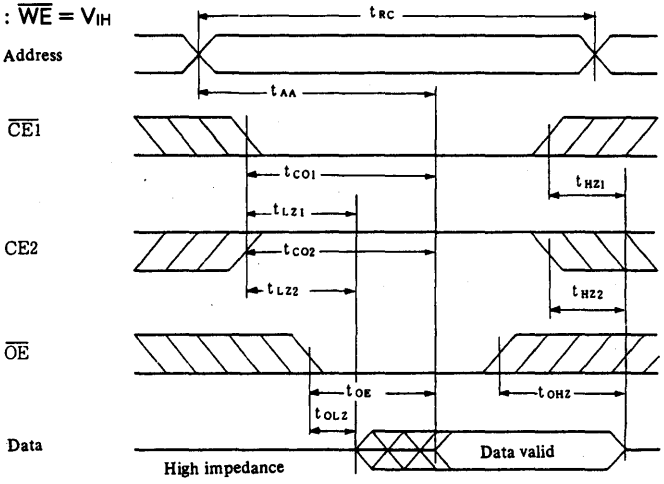
* **Note)** t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

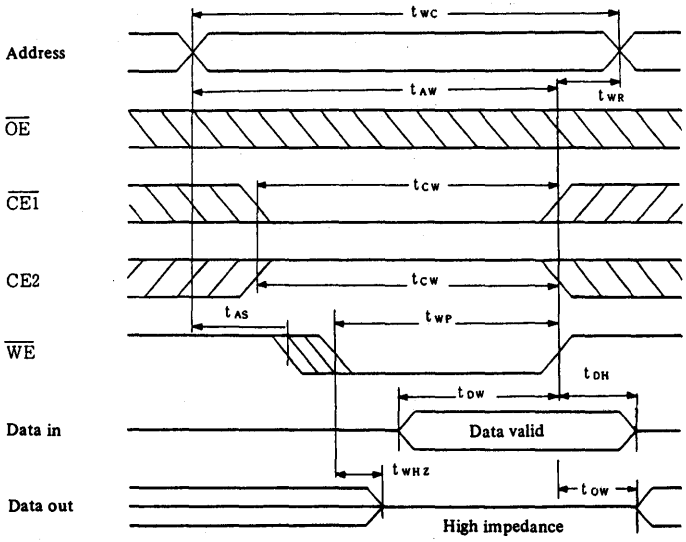
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, CE2 = V_{IH}, $\overline{WE} = V_{IH}$



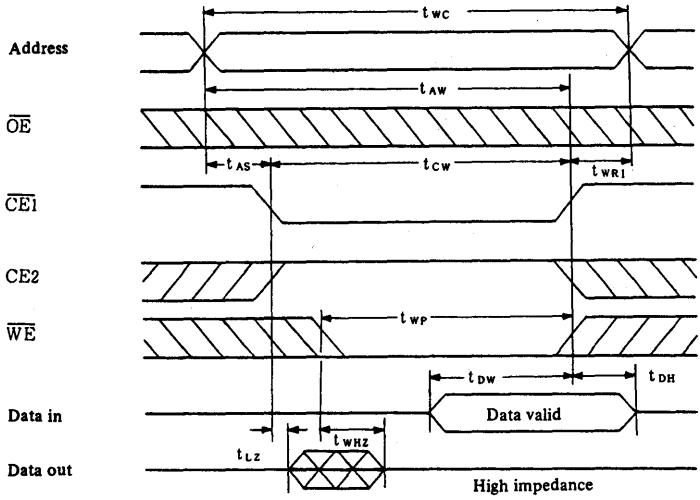
- Read cycle (2) : $\overline{WE} = V_{IH}$



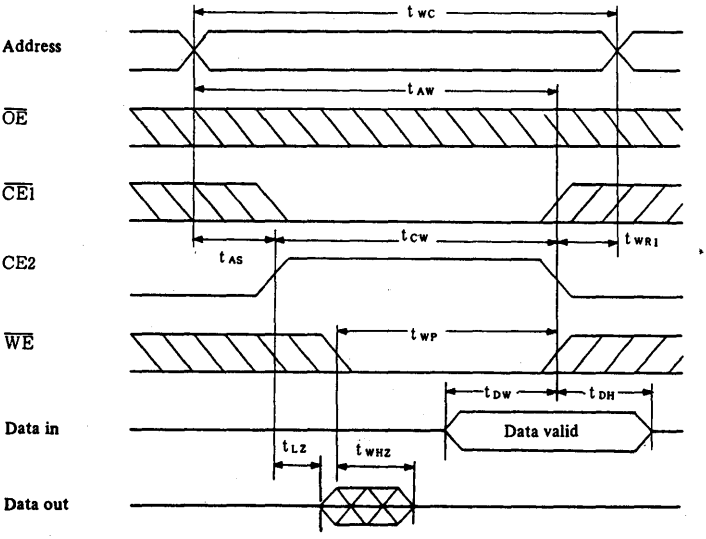
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta = 0 to 70°C)

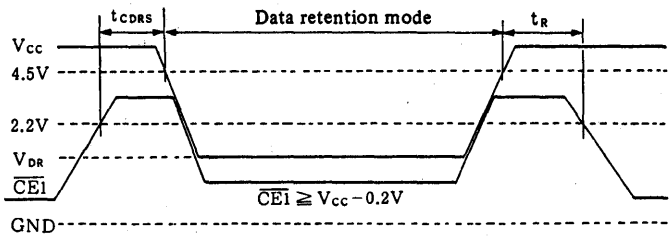
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$ *1	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ *1	—	1	50	μA
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ *1	—	0.002	0.1	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

Note)

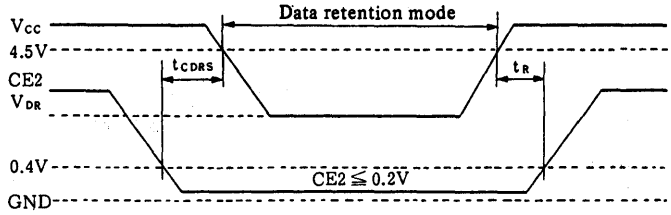
* 1. $\overline{CE1} \geqq V_{CC} - 0.2V$, $CE2 \geqq V_{CC} - 0.2V$ (CE control) or $CE2 \leqq 0.2V$ (CE2 control)
* 2. t_{RC} : Read cycle time

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



• Low supply voltage data retention waveform (2) (CE2 control)



131072-word × 8 bit High Speed CMOS Static RAM Preliminary

Description

CXK581001P/M is a 1,048,576 bits high speed CMOS static RAM organized as 131,072 words by 8 bits and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time : (Access time)
  CXK581001P/M-70L 70ns (Max.)
  CXK581001P/M-85L 85ns (Max.)
- Low power operation :
  CXK581001P/M-70L, 85L ; Standby/DC operation : 10 μW (Typ.) /35mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory ··· No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581001P 600-mil 32pin DIP package
  CXK581001M 525-mil 32pin SOP package

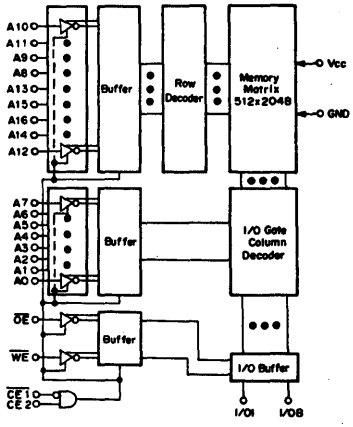
Function

- 131,072 word × 8 bit static RAM

Structure

Silicon gate CMOS IC

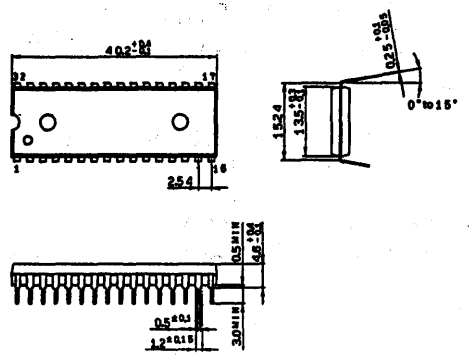
Block Diagram



Package Outline

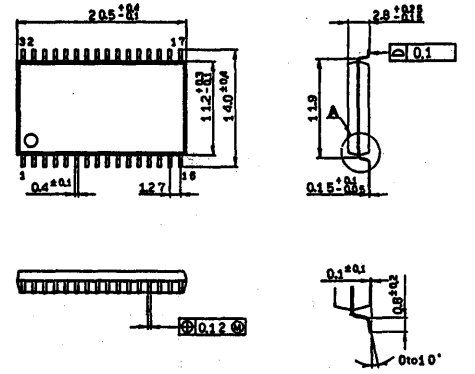
Unit : mm

CXK581001P 32 pin DIP (Plastic) (600-mil)



DIP-32P-01

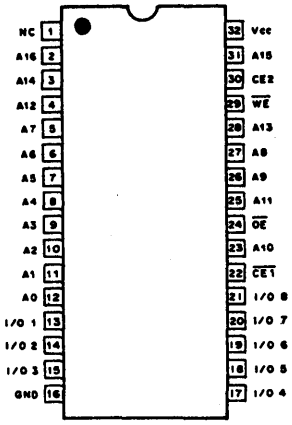
CXK581001M 32 pin SOP (Plastic) (525-mil)



Detailed diagram of A

SOP-32P-L02

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to + 7.0	V
Input voltage	V_{IN}		− 0.5 * to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK581001P	1.0	W
		CXK581001M	0.7	
Operating temperature	Topr		0 to + 70	°C
Storage temperature	Tstg		− 55 to + 150	°C
Soldering temperature	Tsolder		260 • 10	°C • sec

* **Note)** V_{IN}, $V_{I/O}$ = − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

Note) × : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

* **Note)** V_{IL} = − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

DC characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test condition		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA		—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty = 100% I_{OUT} = 0mA	Write cycle	—	45	70	mA
			Read cycle	—	30	45	
	I_{CC3}	Cycle time 1 μS Duty = 100% I_{OUT} = 0mA $\overline{CE1} \leqq 0.2V$, CE2 ≧ Vcc − 0.2V $V_{IL} \leqq 0.2V$, $V_{IH} \geqq$ Vcc − 0.2V	Write cycle	—	10	20	mA
			Read cycle	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc − 0.2V CE2 ≧ Vcc − 0.2V		—	2	100	μA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V

* **Note)** Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

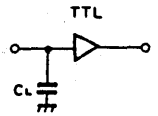
AC characteristics

• **AC test conditions** (Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Condition
Input pulse high level	V_{IH} = 2.2V
Input pulse low level	V_{IL} = 0.8V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load	C_L * = 100pF, 1TTL

* **Note)** C_L includes scope and jig capacitances.

• **Test circuit**



• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	CXK581001 P/M-70L		CXK581001 P/M-85L		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	ns
Address access time	t_{AA}	—	70	—	85	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	70	—	85	ns
Chip enable access time (CE2)	t_{CO2}	—	70	—	85	ns
Output enable to output valid	t_{OE}	—	35	—	45	ns
Output hold from address change	t_{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2} *	—	30	—	30	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	30	—	30	ns

* **Note)** t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

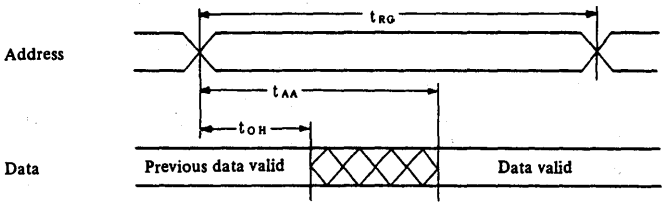
• **Write cycle**

Item	Symbol	CXK581001 P/M-70L		CXK581001 P/M-85L		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	ns
Address valid to end of write	t_{AW}	60	—	75	—	ns
Chip enable to end of write	t_{CW}	60	—	75	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	55	—	65	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	ns
Write to output in high Z	t_{WHZ} *	—	25	—	30	ns

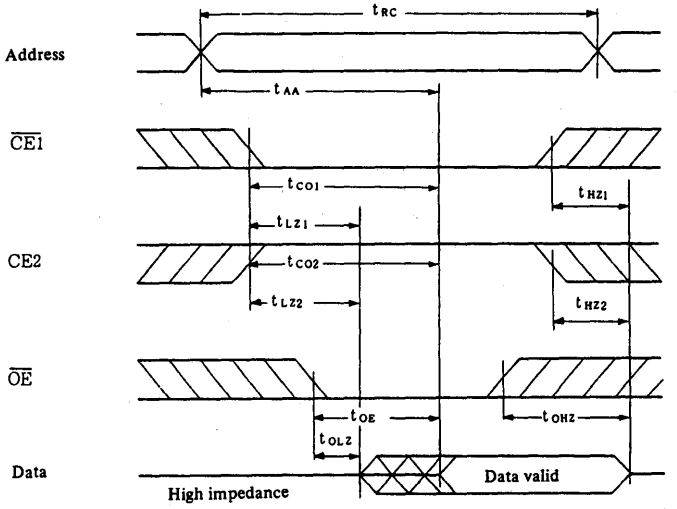
* **Note)** t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

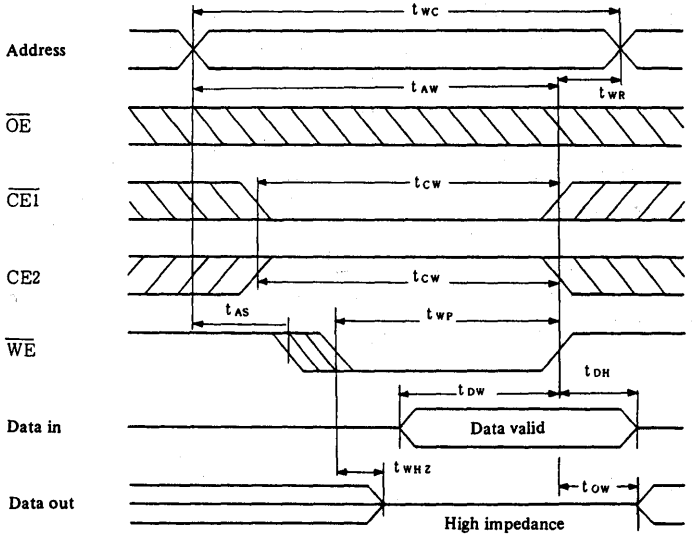
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



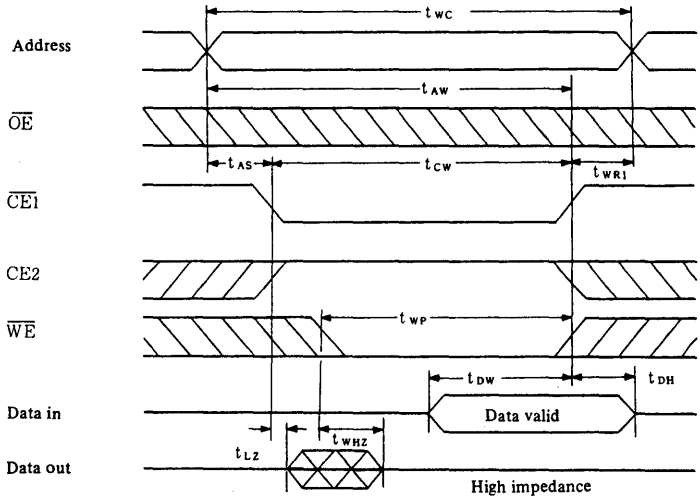
- Read cycle (2) : $\overline{WE} = V_{IH}$



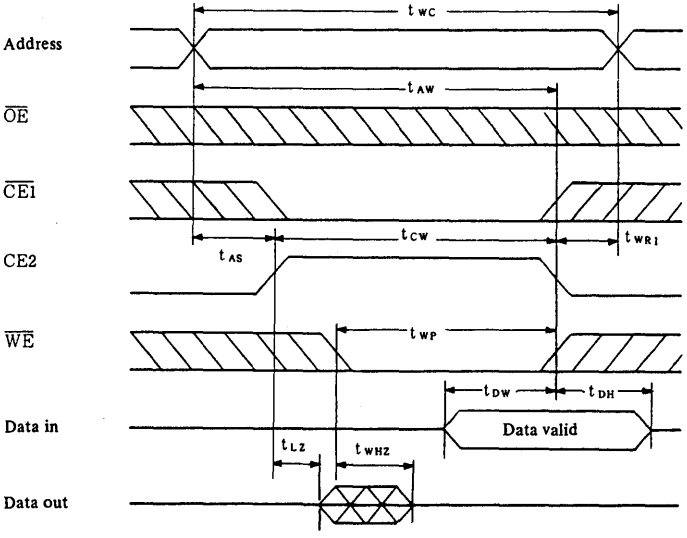
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta = 0 to 70°C)

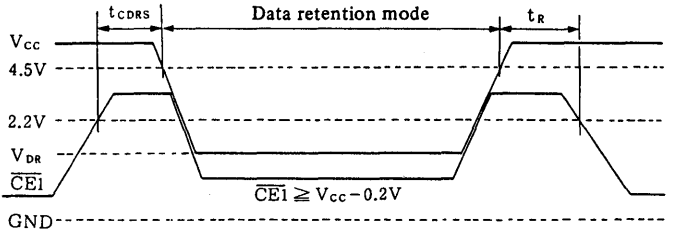
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$ *1	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ *1	—	1	50	μA
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ *1	—	0.002	0.1	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

Note)

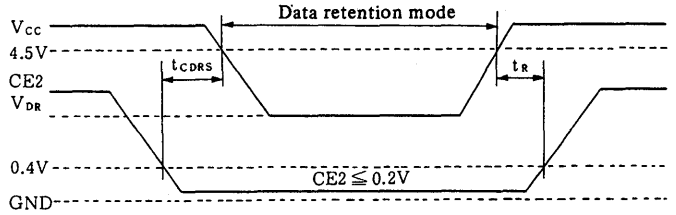
* 1. $\overline{CE1} \geqq V_{CC} - 0.2V$, $CE2 \geqq V_{CC} - 0.2V$ [CE control] or $CE2 \leqq 0.2V$ [CE2 control]
* 2. t_{RC} : Read cycle time

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



• Low supply voltage data retention waveform (2) (CE2 control)



SONY® CXK581020SP/J 45/55

131072 word x 8-bit High Speed CMOS Static RAM

Advance Information

Descriptions

CXK581020SP/J are fast CMOS static RAMs with a construction of 131072 word x 8 bit for general purpose.

These non-sync type ICs operate on single power supply of 5 V and feature low power consumption and fast operation. Battery back-up operation is also possible.

Features

- Fast operation (Access time)
  CXK581020SP/J-45 45 ns (Max.)
  CXK581020SP/J-55 55 ns (Max.)
- Low power consumption
  CXK581020SP/J-45, 55 In stand-by:
  50μW (as of specifications)
- Single power supply 5 V: 5 V±10 %
- Complete static memory
- Access time and cycle time are the same.
- Common input/output (3 state output)
- TTL compatible inputs/outputs.
- Data storage voltage: 2.0 V (Min.)
- Applicable to various packages.
  CXK581020SP 400 mill width 32 pin DIP package
  CXK581020J 400 mill width 32 pin SOJ package

Function

131027 word x 8-bit static RAM

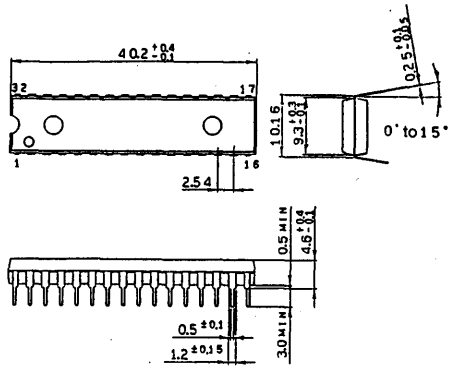
Structure

Silicon gate CMOS IC

Package Outline

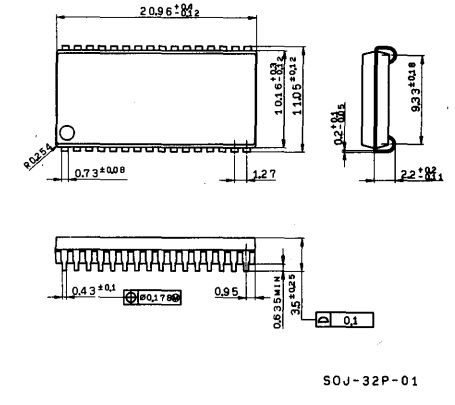
Unit: mm

CXK581020SP 32 pin DIP (Plastic 400 mil)



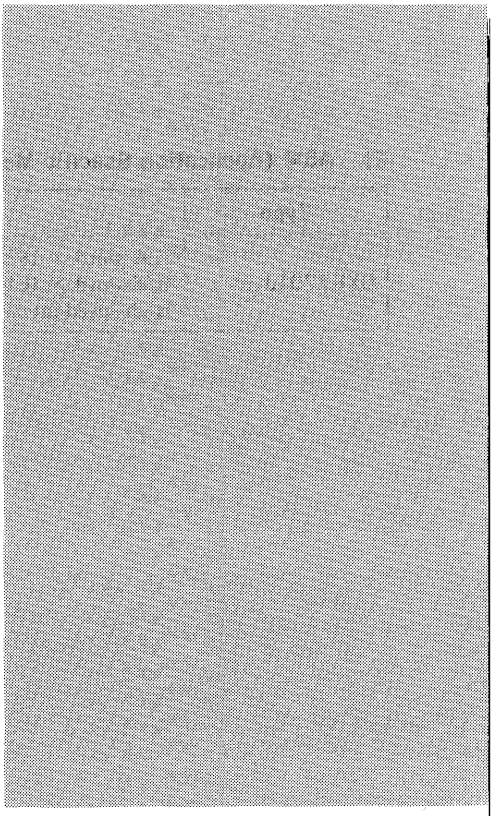
DIP-32P-02

CXK581020J 32 pin SOJ (Plastic 400 mil)

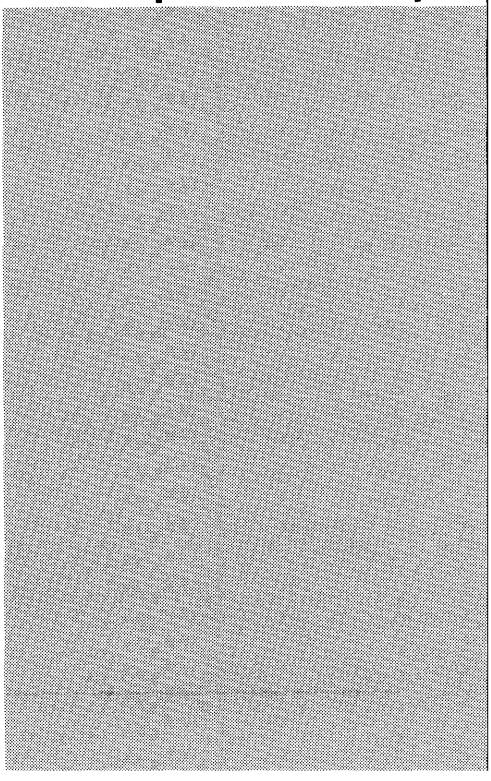


SOJ-32P-01

81062A-HO



ASM
(Application Specific Memory)



2) ASM (Application Specific Memory)

Type	Function	Process	Page
CXK7701J	8192 word × 16 bit 4096 word × 16 bit × 2 way High-speed latched cache-SRAM (P)	MIX CMOS	141

SONY

CXK7701J 30/35/45/55

8192 word × 16 bit
4096 word × 16 bit × 2 way

High-Speed Latched Cache-SRAM

Preliminary

Description

CXK7701J is a 131,072-bit high speed latched Cache-SRAM suitable for use in high speed cache configurations and low power applications.

Organized as 8192 word × 16 bit or 4096 word × 16 bit × 2 WAY selected by mode control pin, it operates from a single 5V supply.

Features

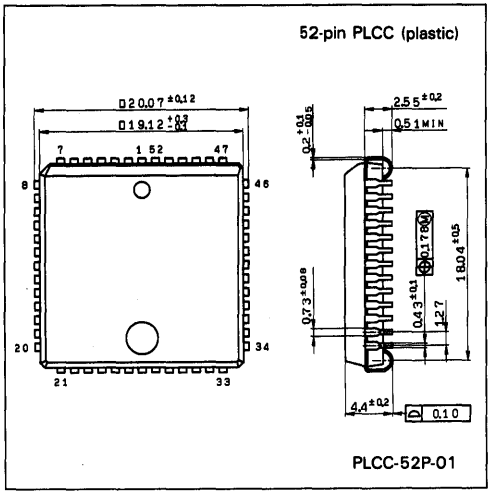
- Best fit for Cache configurations
  Intel 82385 Cache Controller (for 80386-33 MHz, 25 MHz, 20 MHz, 16 MHz)
- Fast access time: (Access time)
  CXK7701J-30 30 ns (MAX)
  CXK7701J-35 35 ns (MAX)
  CXK7701J-45 45 ns (MAX)
  CXK7701J-55 55 ns (MAX)
- Fast output Enable
  CXK7701J-30 10 ns (MAX)
  CXK7701J-35 13 ns (MAX)
  CXK7701J-45 16 ns (MAX)
  CXK7701J-55 18 ns (MAX)
- Available in 52 pin PLCC
- Internal 12 bit address latch (A0-A11)
- Directly TTL compatible: All inputs and outputs

Structure

Silicon gate CMOS IC

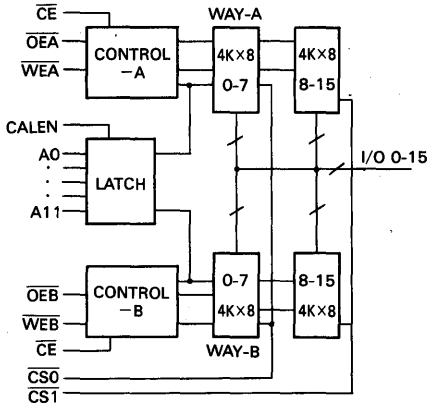
Package Outline

Unit: mm

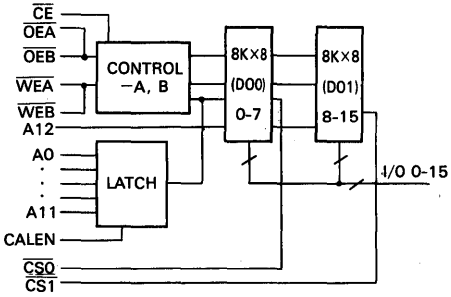


Block Diagram

• 2 WAY SET ASSOCIATIVE (MODE="High")

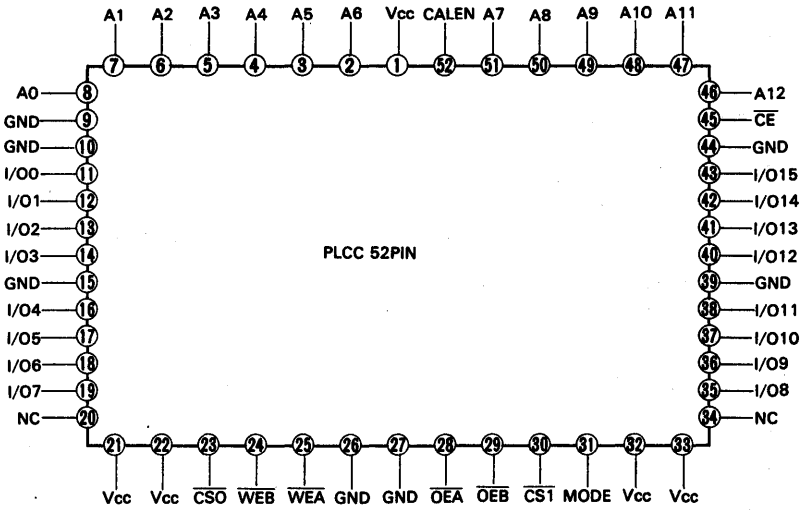


• DIRECT MAP (MODE="Low")



PE88Z04-HO

Pin Configuration



Pin Description

Symbol	Description
A0 to A12	Address Input
I/O 0 to I/O 15	Data Input Output
$\overline{CE}$	Global Chip Enable Input
$\overline{CSO}$, $\overline{CS1}$	Chip Enable Input for I/O 0-7, I/O 8-15
$\overline{OEA}$, $\overline{OEB}$	Output Enable Input for Bank-A, Bank-B
$\overline{WEA}$, $\overline{WEB}$	Write Enable Input for Bank-A, Bank-B
CALEN	Address Latch Enable Input
MODE	Mode Control
Vcc	Power Supply
GND	Ground
NC	No Connection

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	−0.5 to +7.0	V
Input Voltage	Vin	−0.5 to Vcc +0.5	V
Input & Output Voltage	Vi/o	−0.5 to Vcc +0.5	V
Power Dissipation	Pd	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C
Soldering Temperature	Tsolder	260•10	°C•Sec

DC and Operating Characteristics

Unless otherwise noted Vcc=5V±5%, GND=OV, Ta=0 to +70°C

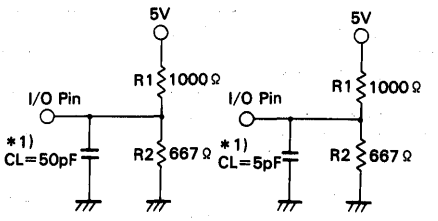
Item	Test condition	Symbol	Min	Max	Unit
Power Supply Voltage		Vcc	4.75	5.25	V
Input High Voltage		VIH	2.2	Vcc+0.3	V
Input Low Voltage		VIL	−0.3	0.8	V
Input Leakage Current	Vin=GND to Vcc	ILI	−2	2	μA
Output Leakage Current	Vi/o=GND to Vcc $\overline{CS0}$, $\overline{CS1}$=VIL or $\overline{OEA}$, $\overline{OEB}$ & $\overline{WEA}$, $\overline{WEB}$=VIL	ILO	−2	2	μA
Operating Supply Current	Vin=VIL or VIH Iout=0 mA	ICC1		80	mA
Average Operating Current	100% Duty Cycle Vin=GND to VCC Iout=0 mA	ICC2		140	mA
	50% Duty Cycle Vin=GND to VCC Iout=0 mA	ICC3		110	mA
Output Low Voltage	IOL=4.0 mA	VOL		0.4	V
Output High Voltage	IOH=−1.0 mA	VOH	2.4		V

A. C. Test Condition (Applies to Read & Write Cycle Timing)

Vcc = 5V ± 5%, Ta = 0 to +70°C

Item		Condition	Unit
Input Pulse High Level		VIH = 3.0	V
Input Pulse Low Level		VIL = 0.0	V
Input Rise Time		tR = 3	ns
Input Fall Time		tF = 3	ns
Input and Output Reference Level		1.5V	V
Output Load (See Test Circuit Fig-1)	R1	1000	Ω
	R2	667	Ω
	CL	50	pF

Fig-1



*1. Including scope and jig Capacitance
*2. For tLZ, tHZ, tOHZ, tOLZ, tWLZ, tWHZ

Truth Tables

Two-Way Mode (Mode = High)

$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	Operation	
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled	
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled	
X	X	X	H	H	X	X	Outputs High-Z	
X	X	X	L	L	X	X	Outputs High-Z	
L	L	H	L	H	H	H	Read I/O 0-7	Way A
L	L	H	H	L	H	H	Read I/O 0-7	Way B
L	H	L	L	H	H	H	Read I/O 8-15	Way A
L	H	L	H	L	H	H	Read I/O 8-15	Way B
L	L	L	L	H	H	H	Read I/O 0-15	Way A
L	L	L	H	L	H	H	Read I/O 0-15	Way B
L	L	H	X	X	L	H	Write I/O 0-7	Way A
L	L	H	X	X	H	L	Write I/O 0-7	Way B
L	H	L	X	X	L	H	Write I/O 8-15	Way A
L	H	L	X	X	H	L	Write I/O 8-15	Way B
L	L	L	X	X	L	H	Write I/O 0-15	Way A
L	L	L	X	X	H	L	Write I/O 0-15	Way B
L	L	H	X	X	L	L	Write I/O 0-7	Way A&B
L	H	L	X	X	L	L	Write I/O 8-15	Way A&B
L	L	L	X	X	L	L	Write I/O 0-15	Way A&B

Truth Tables (cont)

Direct Mode (Mode = Low)

$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O 0-7
L	H	L	L	L	H	H	Read I/O 8-15
L	L	L	L	L	H	H	Read I/O 0-15
L	L	H	X	X	L	L	Write I/O 0-7
L	H	L	X	X	L	L	Write I/O 8-15
L	L	L	X	X	L	L	Write I/O 0-15

I/O Capacitance

Unless otherwise stated f = 1 MHz, Ta = 25°C

Item	Test condition	Symbol	Min	Max	Unit
Input Capacitance	VIN = 0 V	CIN	—	7	pF
I/O Capacitance	VI/O = 0 V	CI/O	—	8	pF

Write Cycle Timing

(Vcc = 5V ± 5%)

Item	Symbol	30		35		45		55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	30	—	35	—	45	—	55	—	ns
Address Valid to End of Write	tAW	25	—	30	—	40	—	50	—	ns
A12 Valid to End of Write	ta12W	20	—	25	—	30	—	40	—	ns
Chip Select to End of Write	tCW	20	—	25	—	30	—	40	—	ns
Data Valid to End of Write	tDW	15	—	15	—	20	—	20	—	ns
Data Hold from End of Write	tDH	0	—	0	—	0	—	0	—	ns
Write Enable Active to High-Z	tWHZ	—	15	—	15	—	20	—	20	ns
WRITE Enable Inactive to Low-Z	tWLZ	3	—	3	—	3	—	3	—	ns
Write Pulse Width	tWP	20	—	25	—	30	—	40	—	ns
$\overline{CE}$ Pulse Width During Chip Enable Controlled Write	tCP	20	—	25	—	30	—	40	—	ns
Address Setup Time	tAS	0	—	0	—	0	—	0	—	ns
Write Recovery Time	tWR	0	—	0	—	2	—	2	—	ns
Address Latch Enable Pulse Width	tCALEN	8	—	10	—	15	—	15	—	ns
Address Setup to Latch Low	tASL	4	—	6	—	10	—	10	—	ns
Address Hold to Latch Low	tAHL	5	—	5	—	5	—	5	—	ns

Read Cycle Timing

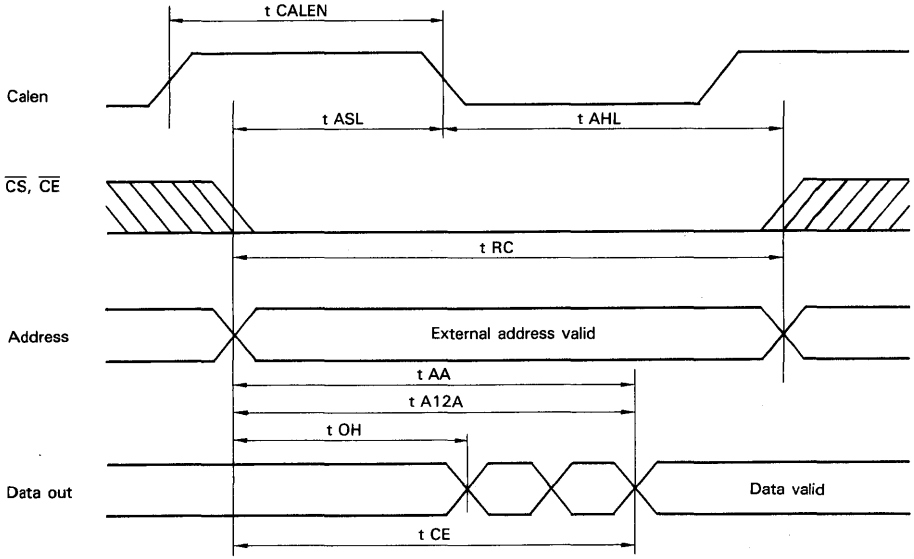
(Vcc = 5V ± 5%)

Item	Symbol	30		35		45		55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	30	—	35	—	45	—	55	—	ns
Address Access	tAA	—	30	—	35	—	45	—	55	ns
A12 Address Access	tA12A	—	17	—	25	—	30	—	30	ns
Chip Select Access Time	tCS tCE	—	20	—	25	—	35	—	45	ns
Output Enable to Output Valid	tOE	—	10	—	13	—	16	—	18	ns
Output Hold from Address Change	tOH	3	—	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	tLZ	3	—	3	—	3	—	3	—	ns
Output Enable to Output Low -Z	tOLZ	2	—	2	—	2	—	2	—	ns
Chip Deselect to Output High-Z	tHZ	—	15	—	25	—	30	—	30	ns
Output Disable to Output High-Z	tOHZ	—	10	—	14	—	14	—	14	ns
Address Latch Enable Pulse Width	tCALEN	8	—	10	—	15	—	15	—	ns
Address Setup to Latch Low	tASL	4	—	6	—	10	—	10	—	ns
Address Hold to Latch Low	tAHL	5	—	5	—	5	—	5	—	ns

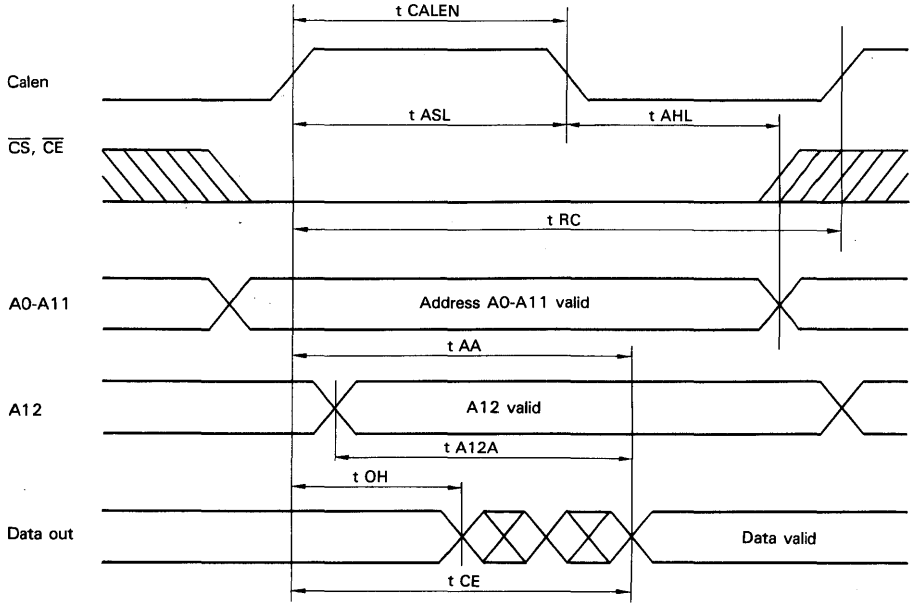
Timing Waveform

1) Read Cycle

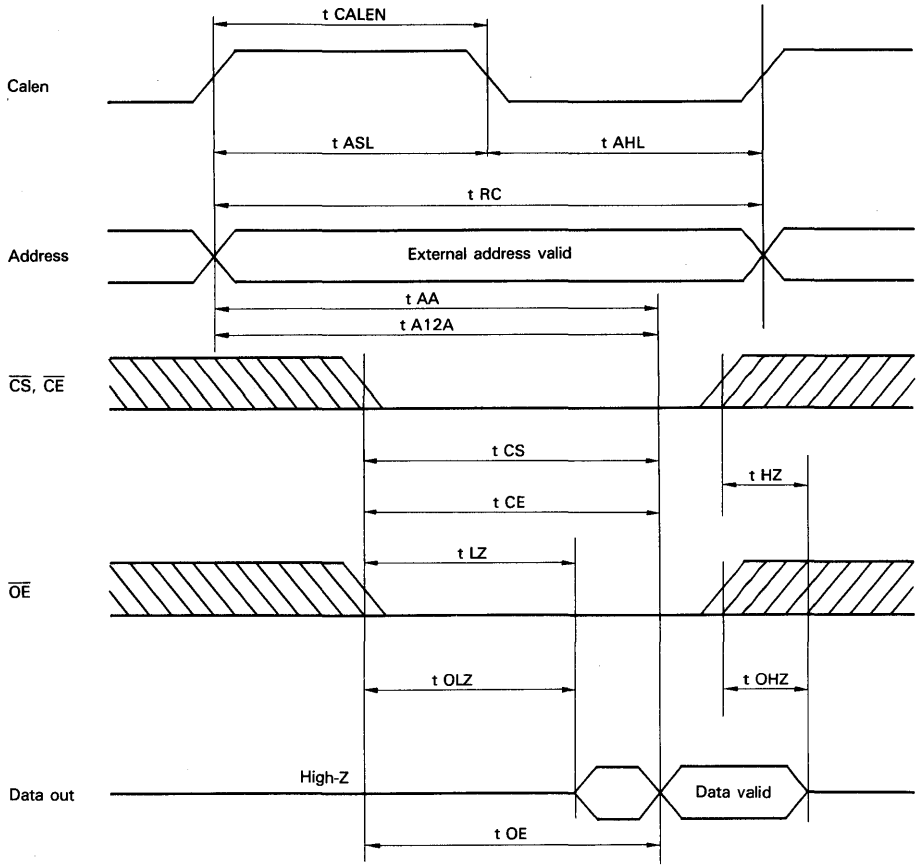
Read Cycle 1
($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, $\overline{CS}$ = V_{IL})



Read Cycle 2
($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, $\overline{CS}$ = V_{IL})

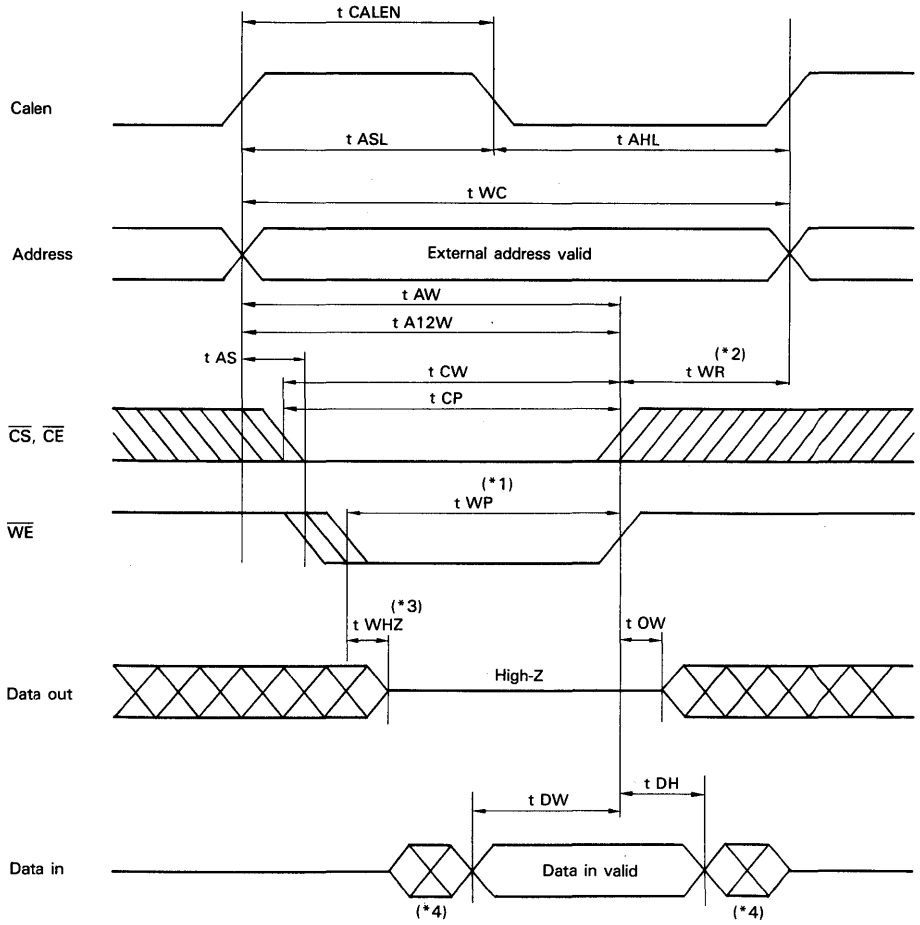


Read Cycle 3
($\overline{WE}$ = V_{IH})

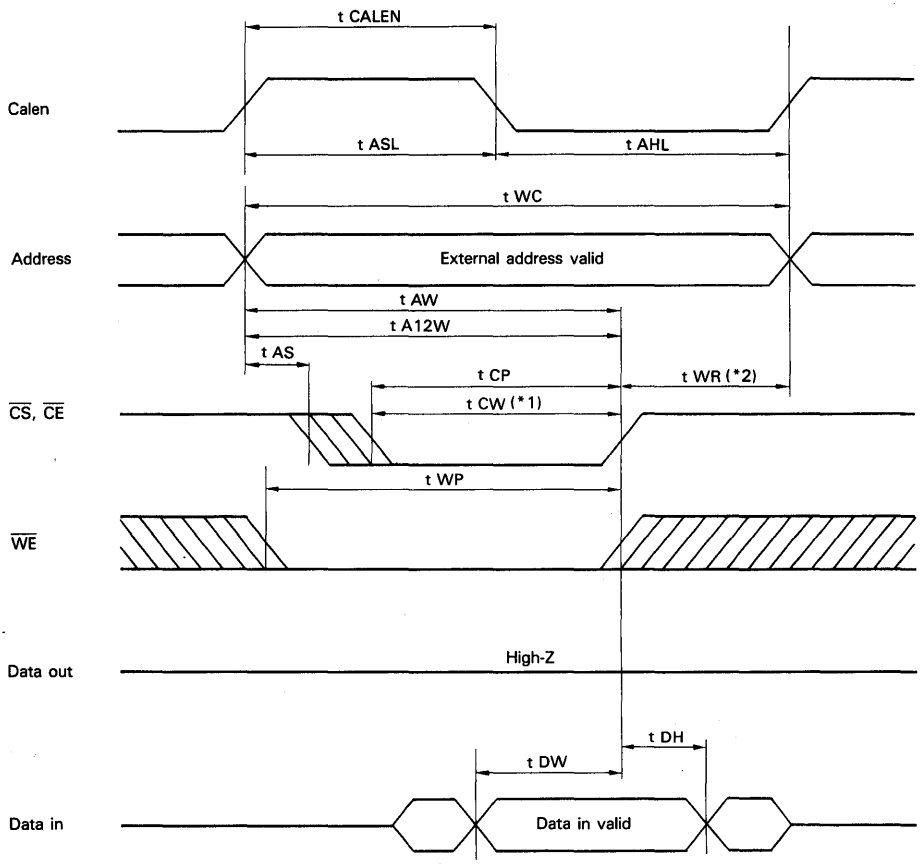


2) Write Cycle

Write Cycle 1
($\overline{WE}$ controlled)



Write Cycle 2
($\overline{CE}$ controlled write)



***Note)**

1. A write occurs during the low overlap of $\overline{CS}$, $\overline{CE}$ and $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. If $\overline{CE}$ and $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Control Pin Description

CALEN (Cache Address Latch Enable)

This signal controls the internal address latch that resides between the address inputs and the memory array. When CALEN is high the latch is transparent. The falling edge of CALEN latches the current address inputs.

MODE

This signal controls whether the memory device is to be used in a direct mapped (8k × 16) configuration or a two-way set associative (2-4k × 16) configuration. When the mode signal is high, the device is placed in two-way mode. When the mode pin is low, the device is placed in direct mode.

$\overline{CS0}$, $\overline{CS1}$ (Cache Chip Selects)

These active low signals tie to the cache ram chip selects and individually enable the two bytes of the memory. $\overline{CS0}$ enables bits D0-D7 and, $\overline{CS1}$ enables bits D8-D15.

$\overline{CE}$ (Cache Chip Enable)

This active low signal, when active, enable writes to the data ram or reads from the data ram. It is a global signal, and controls both cache bank A and cache bank B. It's function is the same in both the set associative mode and the direct mapped mode.

This input also functions as a chip enable controlled write.

$\overline{OEA}$, $\overline{OEB}$ (Cache Output Enables)

In two-way mode, these active low signals enable cache bank A or B to drive the data bus. Either $\overline{OEA}$ or $\overline{OEB}$ is active during a read hit, depending on which bank is selected. Activation of $\overline{OEA}$ simultaneous with $\overline{OEB}$ will cause both banks ot become deselected.

In direct mode, these inputs will be externally wired together and A12 will determine which 4K × 16 memory bank is enabled.

$\overline{WEA}$, $\overline{WEB}$ (Cache Write Enables)

In two-way mode, these active low signals enable cache bank A or B to receive data from the data bus. Either $\overline{WEA}$ or $\overline{WEB}$ is enabled in a read miss update or write hit.

In direct mode, these inputs will be externally wired together and A12 will datermine which 4K × 16 memory bank will be enabled for writing.

A0-A11 (Addresses)

The address input provide the address into the SRAM array. These signals are latched in the trailing edge of CALEN.

A12 (Address)

In two-way mode, the upper address input A12 will be a "don't care" and will be externally wired to ground.

In direct mode, A12 will determine which 4K × 16 memory bank is enabled by $\overline{WEA}$ and $\overline{WEB}$, and $\overline{OEB}$. Unlike the other address lines, A12 is not latched.

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