Design guide for power supply with IDP2303, IDP2308 and IDP2303A

Design guide for TV power supply with digital multi-mode PFC + LLC combo IC IDP230x

About this document

Scope and purpose

This design guide is to help customers design a TV power supply using an Infineon digital controller. It provides guidelines on power stage design, control parameters and protection settings as well as PCB layout and dpVision GUI usage.

Intended audience

This document is intended for design engineers that want to design a high performance TV power supply using Infineon's digital multi-mode PFC + LLC combo IC.

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Abstract

1 Abstract

Infineon's digital platform controller IC (IDP230x) combines the PFC and LLC controls for a high efficiency power supply. This design guide provides detailed calculation examples for major power stage component values as well as the settings for parameters associated with general functions and protection features. Useful tips on PCB layout are included to help the customers optimize their PCB design. Lastly, the installation and usage of a General User Interface - dpVision - is described to assist the customer in setting parameters for the digital IC.

The design example used in this guide is a 120 W power supply for a UHD TV. The customer can easily apply their own target specifications and obtain the design parameters by themselves.

2 Introduction

2.1 IC Introduction

The IDP230x is a multi-mode PFC and LLC controller combined with a floating high side driver and a startup cell. A digital engine provides advanced algorithms for multi-mode operation to support the highest efficiency over the whole load range. A comprehensive and configurable protection feature set is implemented. Only a minimum of external components are required. The integrated HV startup cell and advanced burst mode enable the achievement of low stand-by power. In addition, a one-time-programming (OTP) unit is integrated to provide a wide set of configurable parameters that help to ease the design in phase of the project. [1][2].

2.2 Product highlights

- Integrated 600 V startup cell
- Integrated floating driver based on coreless transformer technology
- Digital multi-mode operation for higher efficiency
- Supports low standby power by means of a direct X-cap discharge function and advanced burst mode control
- Eliminates the auxiliary power supply by means of anintegrated startup cell and burst mode
- UART interface for communication and in-circuit configuration
- Flexible design-in by means of one time programming capability for a wide range of parameters

2.3 Application

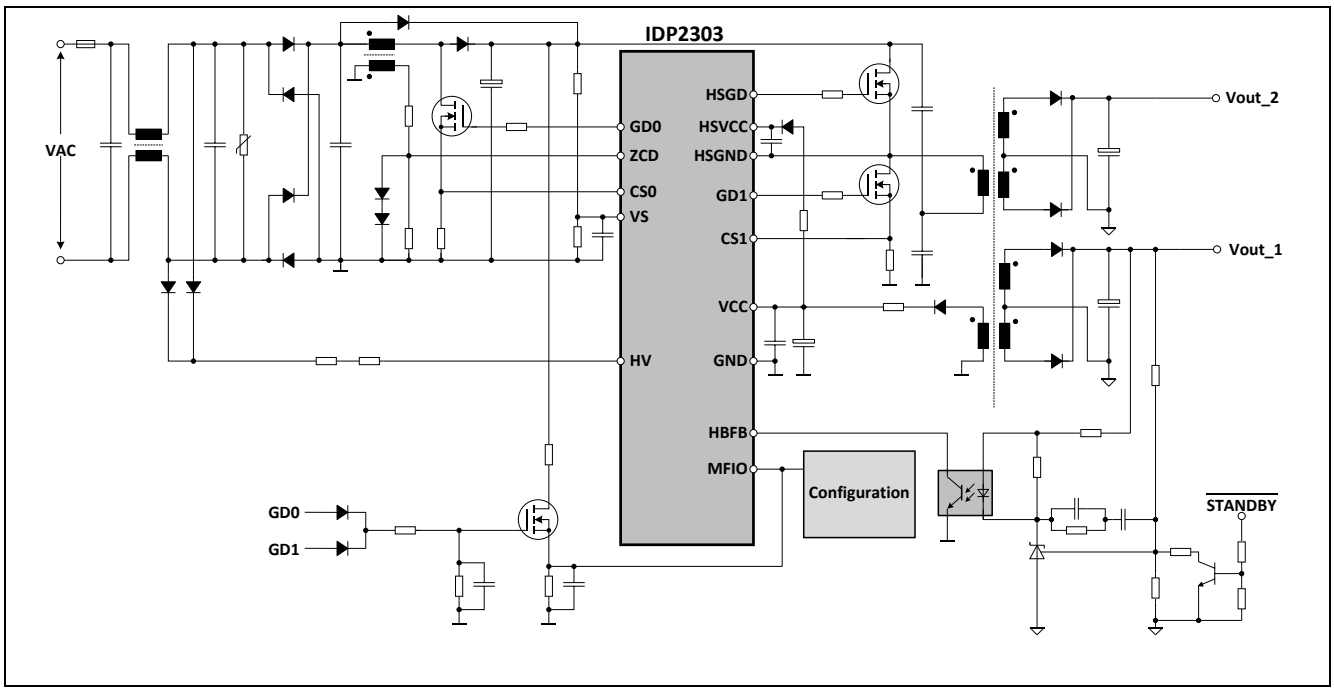

Figure 1 Typical application circuit for a power supply with IDP2303 & IDP2308

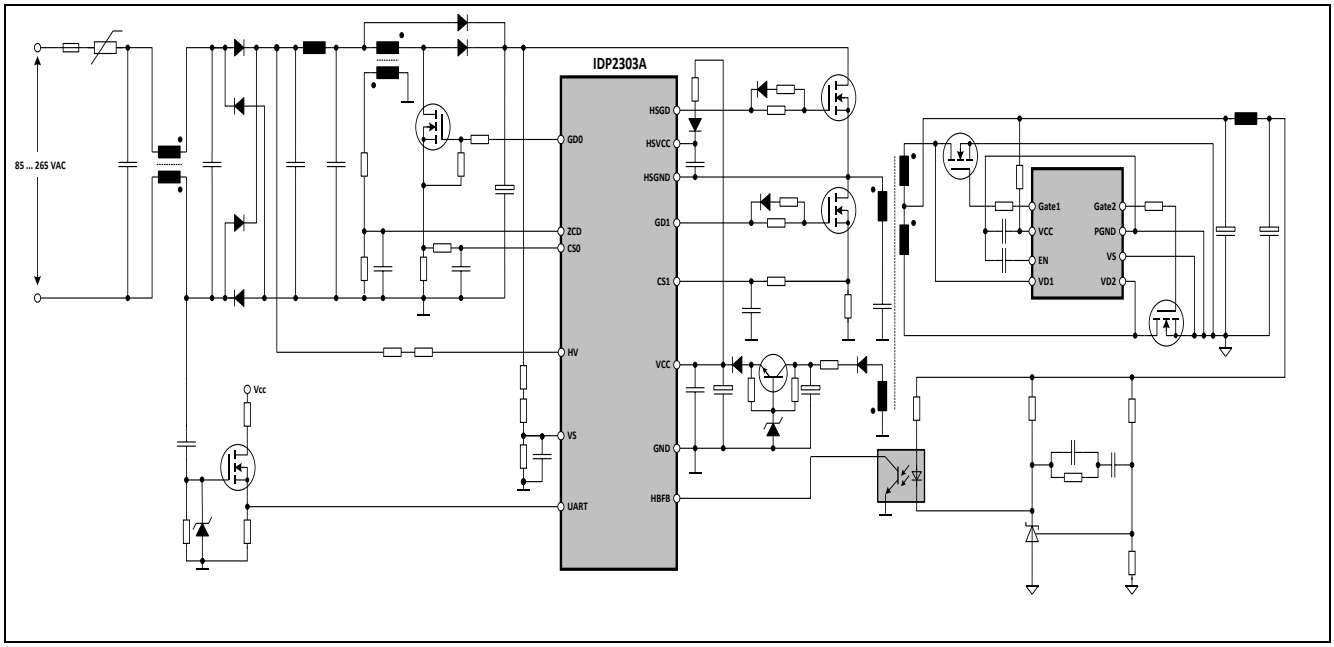

Figure 2 Typical application circuit for a power supply with IDP2303A

3 PFC design

3.1 Target specifications

Table 1 shows the major specifications for the target PFC design.

Table 1 System specification

Parameter	Symbol	Value	Unit
Input voltage minimum	V_{in_min}	90	V_{AC}
Input voltage maximum	V_{in_max}	265	V_{AC}
Nominal bus voltage	V_{bus}	390	V
PFC output power	P_{o_PFC}	130	W
Estimated efficiency of system (PFC+LLC) at 90 V_{AC}	η_{sys}	> 87%	
Estimated efficiency of PFC at 90 V_{AC}	η_{PFC}	~93%	
Estimated efficiency of PFC at 265 V_{AC}	η_{PFC_265}	~96%	
Minimum switching frequency	f_{sw_min}	25	kHz
Power factor		> 0.9	

3.2 Power stage

A simplified application circuit for PFC stage is given in Figure 3.

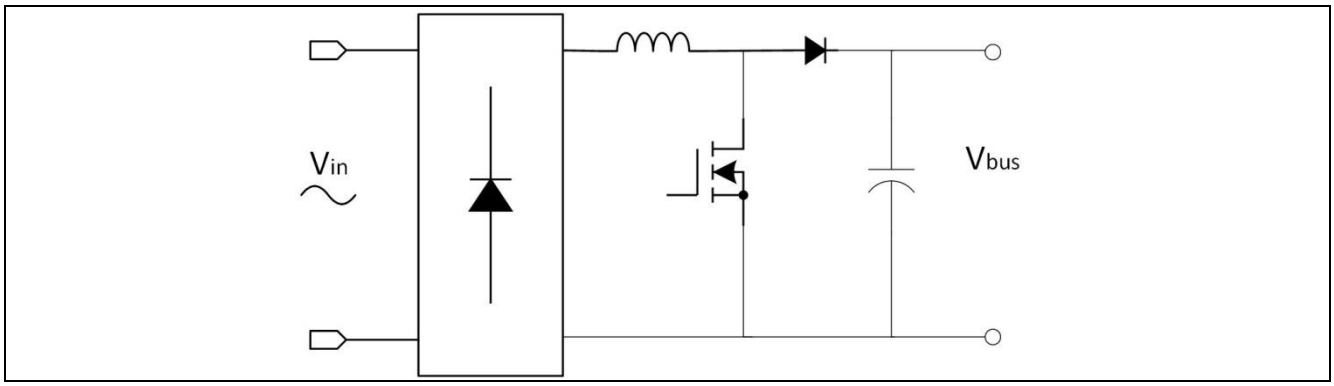

Figure 3 Simplified circuit for PFC converter

3.2.1 Bridge rectifier

The total bridge power loss is calculated using the average input current flowing through two of the bridge rectifying diodes.

$$P_{rect\_loss} = I_f * 2V_f = \frac{2\sqrt{2}}{\pi}\frac{P_o}{V_{in\_min} * \eta_{PFC_{90}}} * 2V_f = \frac{4\sqrt{2}}{\pi}\frac{130}{90 * 0.93} * 2 * 0.35 = 1.96\,W$$

Knowing the value of the power loss, one can choose an appropriate bridge rectifier based on its thermal characteristics.

3.2.2 Selection of power MOSFET

In order to select an optimum MOSFET, one must understand the MOSFET requirements in a DCM boost converter [3]. The following are some major MOSFET selection considerations:

- Low Figure of Merit - R_{on}*Q_g and R_{on}*Q_{oss}
- Fast Turn-on/off switching to reduce the device switching losses
- Low output capacitance C_{oss} for low switching energy, to increase light load efficiency.
- Switching and conduction losses must be balanced for minimum total loss - this is typically optimized at the low line condition, where worst case losses and temperature rises occur.
- V_{DS} rating to handle spikes/overshoots
- Low thermal resistance R_{thJC}. Package selection must consider the resulting total thermal resistance from junction to ambient.
- Body diode speed and reverse recovery charge are not important, since the body diode never conducts in a boost converter.

Infineon high voltage MOSFETs have several families based on different technologies, each of which target a specific application, topology or operation. Several CoolMOS™ series devices can be used for boost applications depending upon the customer's requirement for the voltage rating and thermal characteristics.

With the CE in 500 V, E6 and P6 family in 600 V, Infineon offers various series with extremely low conduction and switching losses that can make switching applications more efficient, more compact, lighter and cooler.

Two IPD50R280CE in parallel are preselected for the design and their parameters will be used for the loss calculation. The thermal characteristic can be estimated and the device shall be replaced if it cannot meet the thermal requirement at the end of the calculation process.

The conduction loss dissipated by each MOSFET is calculated as:

$$P_{con} = \left(\frac{I_{Q_{rms}}}{2}\right)^2 R_{DS_{on}} = \left(\frac{1.5}{2}\right)^2 * 0.5 = 0.28\ W$$

In which,

$$I_{Q\_rms} = I_{peak\_Vin\_min}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}V_{in\_min}}{9\pi V_{bus}}} = \frac{2\sqrt{2}P_{o\_PFC}}{\eta_{PFC\_90} * V_{in\_min}}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}V_{in\_min}}{9\pi V_{bus}}} = \frac{2\sqrt{2} * 130}{0.93 * 90}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} * 90}{9\pi * 390}}$$
$$= 4.39 * 0.347 = 1.5\ A$$

$R_{DS_{on}} = 0.5\ \Omega$ is the on-state resistance of the MOSFET at a junction temperature of 100°C.

For CrCM or DCM operation, the turn-on loss due to the voltage-current crossover is negligible because when MOSFET turns on, the MOSFET current rises from zero. Therefore, only the loss due to the discharge of the drain-source capacitance of the MOSFET shall be considered.

The calculation of the MOSFET discharge loss at turn-on ($P_{discharge}$) and turn-off loss ($P_{turnoff}$) is complicated due to the changing values of voltage, current, frequency etc. over the whole AC cycle. So based on a rule-of-thumb, the total switching loss for each MOSFET is roughly estimated as half of the conduction loss.

$$P_{sw} = \frac{1}{2}P_{con} = 0.5 * 0.28 = 0.14\ W$$

Then the total power loss of each MOSFET can be estimated as:

$$P_{MOS\_loss} = P_{con} + P_{sw} = 0.42\ W$$

3.2.3 MOSFET gate driving

3.2.3.1 Unique gate drive concept

The IDP230x gate drive offers unique features including configurable charge current and output voltage, which offer many advantages (Figure 4):

- turn-on slope optimization for EMI by configurable current with dpVision
- no need to solder and re-solder resistors
- turn-off current limited by external R_{gate}
- due to fast 1 A/0.5 A discharge, a local discharge PNP transistor is not required in some relatively low power applications
- V_{gate_high} up to VCC possible (rail-to-rail operation)

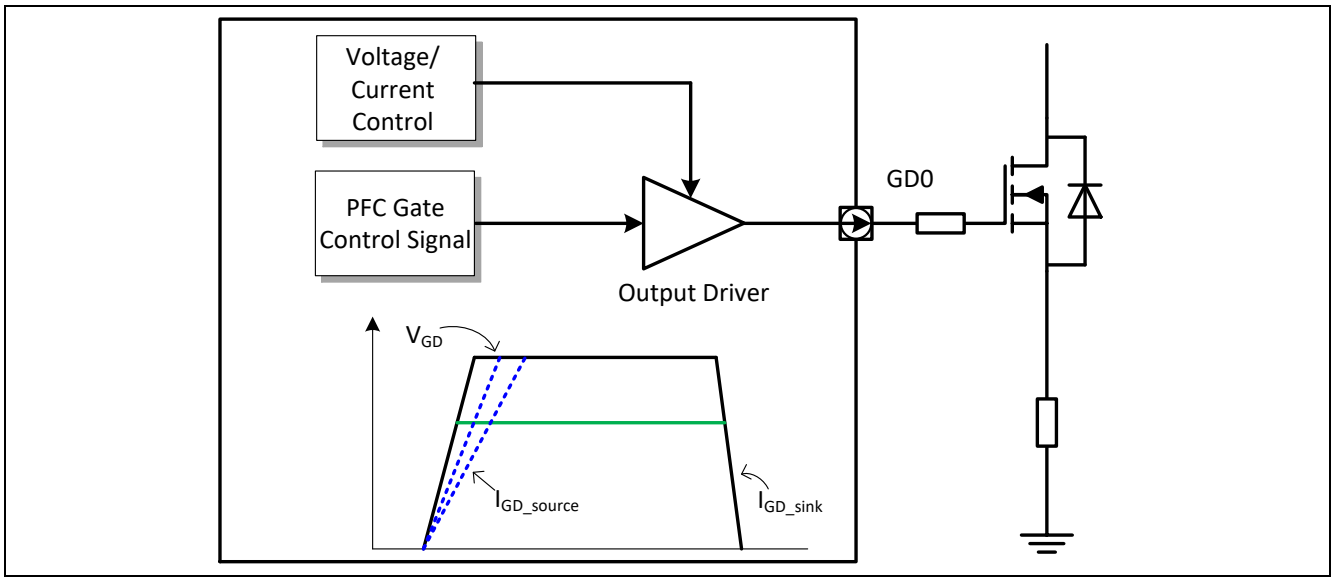

Figure 4 Gate drive concept

3.2.3.2 Gate drive stability

Due to the unique gate drive with configurable charge current and regulated gate high voltage, R_{gate} should not be too large. Table 2 shows the recommend range for stable gate drive operation. A 10Ω R_{gate} resistor is suitable for most applications. Soft turn-on for trouble-free EMI is guaranteed by the configurable constant current gate charging.

Table 2 Recommended R_{gate} values for different C_{gate}, R_{gs} and gate source current

C_{gate} (nF)	1.0~2.0			
Gate source current (mA)	**100**		**310**	
R_{gs} (Ω)	**10 k**	**100 k**	**10 k**	**100 k**
Recommended R_{gate} (Ω)	5~20	15~25	4~14	2~18

3.2.3.3 Other design tips for the gate driving circuit

For some high power SMPS applications, two MOSFETs are often connected in parallel for the PFC converter. In this case, it is recommended to enhance the PFC driving capability by adding an additional circuit close to the PFC MOSFET, as shown in the example in Figure 5.

During turn-off, transistors Q3 and Q4 are turned on, discharging the PFC MOSFET gate capacitor. As a result, the turn-off of the MOSFETs is accelerated, which reduces the MOSFETs turn-off losses. Meanwhile, the turn-on is defined by the constant gate charge current, which can be kept relatively slow for better EMI performance.

Apart from the gate drive resistance itself, 10 kΩ resistors (R5 and R6) are also commonly connected between MOSFET gate and source to help damping some overshoot and oscillations and discharge gate capacitor when there is no gate signal.

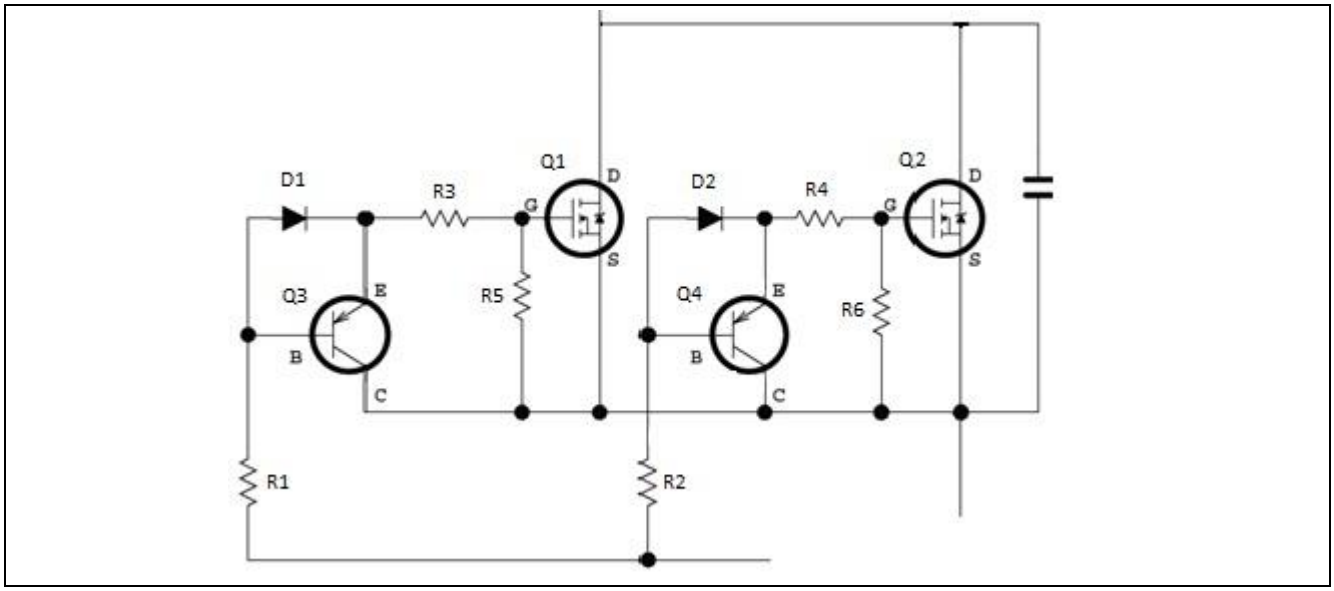

Figure 5 PFC gate driving circuit

3.2.4 Boost diode

To select an appropriate boost diode, its thermal characteristic needs to be considered.

The average diode current can be calculated by:

$$I_{D\_avg} = I_{o\_PFC} = \frac{P_{o\_PFC}}{V_{bus}} = \frac{130}{390} = 0.33\ A$$

The total diode conduction loss can be calculated by:

$$P_{D\_loss} = I_{D\_avg} * V_f = 0.33 * 0.5 = 0.17\ W$$

3.2.5 Boost inductor

One of the key design considerations for a boost inductor is to ensure the minimum switching frequency is always higher than 25 kHz to avoid any audible noise. The worst cases are usually at extremes of operation such as minimum and maximum voltage and during start up and load transients - e.g. twice full power.

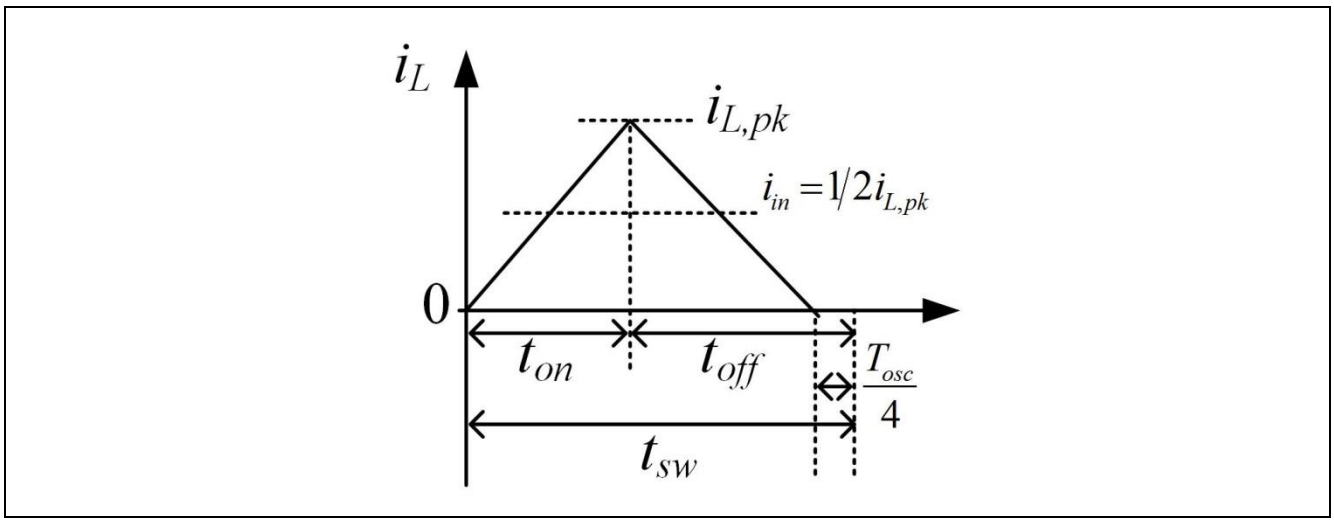

Figure 6 Current and timing in QR1 operation

With the IDP230x, the minimum switching frequency of 25 kHz is guaranteed by the “maximum switching period time-out” approach, which turns the MOSFET on when 40 us of switching period is reached.

Based on the PFC control concept of the IDP230x, the frequency may reach the 25 kHz limit in two extreme conditions:

- Heavy load when QR=1 (MOSFET turn-on at the first switching valley according to the frequency law, which will be discussed in a later section of this document.)
- Light load when QRN>10 according to the frequency law, or when the ZCD signal is too weak to be detected within 40 us.

The second condition will not affect the design of inductor.

Figure 6 illustrates the inductor current and timing during QR1 operation. In which

$$T_{osc} = 2\pi\sqrt{L_{PFC}C_{oss}}$$

Where L_{PFC} is the PFC inductance and C_{oss} is the time related output capacitance of the PFC MOSFET.

T_{osc} is usually around 1 us, and is negelected in the analysis below to simplify the calculation.

The switching frequency at the AC peak, double full load with QR1 operation can be calculated as:

$$f = \frac{{v_{in\_pk}}^2 * \left(v_{bus} - v_{in\_pk}\right) * \eta}{v_{bus} * L_{PFC} * 8P_{o\_PFC}}$$

For 265 V_{ac},

$$f_{265V\_pk} = \frac{(265 * \sqrt{2})^2 * \left(390 - 265 * \sqrt{2}\right) * \eta_{PFC\_265}}{390 * L_{PFC} * 8P_{o\_PFC}} = \frac{658}{L_{PFC} * P_{o\_PFC}}$$

For 90 V_{ac},

$$f_{90V\_pk} = \frac{(90 * \sqrt{2})^2 * \left(390 - 90 * \sqrt{2}\right) * \eta_{PFC\_90}}{390 * L_{PFC} * 8P_{o\_PFC}} = \frac{1268}{L_{PFC} * P_{o\_PFC}}$$

Comparing the switching frequency at 265 Vac and 90 Vac peak, it is obvious that the frequency at 265 Vac is lower. Therefore,

$$f_{265V\_pk} > 25\ kHz$$

Then the PFC inductance to meet the requirement can be calculated as:

$$L_{PFC} < \frac{{v_{265\_pk}}^2 * \left(v_{bus} - v_{265\_pk}\right) * \eta_{PFC\_265}}{v_{bus} * f * 8P_{o\_PFC}} = \frac{(265 * \sqrt{2})^2 * \left(390 - 265 * \sqrt{2}\right) * 0.96}{390 * 25 * 10^3 * 8 * 130} = 202\ uH$$

Thereby, a PFC inductance of 200 µH is selected.

Another design consideration for the boost inductor is to ensure that the ferrite core will not go into saturation. Then the number of turns in the winding is calculated as:

$$N_{PFC} > \frac{i_{pk\_90Vac} * L_{PFC}}{B_{max}A_{min}} = \frac{4.33 * 200 * 10^{-6}}{0.3 * 99 * 10^{-6}} = 29$$

in which

$$i_{pk\_90Vac} = \frac{2\sqrt{2}P_{o\_PFC}}{\eta * v_{90}} = \frac{2\sqrt{2} * 120}{0.87 * 90} = 4.39A$$

B_{max} is up to 0.3T, A_{min} is $99mm^2$ if an EQ30 core with PC40 ferrite material is selected.

After the threshold of Over Current Protection (OCP) is defined and its tolerance taken into consideration, verification is needed that the inductor is able to carry the maximum current defined by OCP, and not become saturated. Otherwise, a large current will result from the saturation, and potentially damage devices if it is present for some time.

3.3 Control parameters and protections

3.3.1 Output voltage sense and protections

The VS pin is used for feedback regulation of the PFC Bus voltage. A simple resistor divider is used to step down the bus voltage as shown in Figure 7.

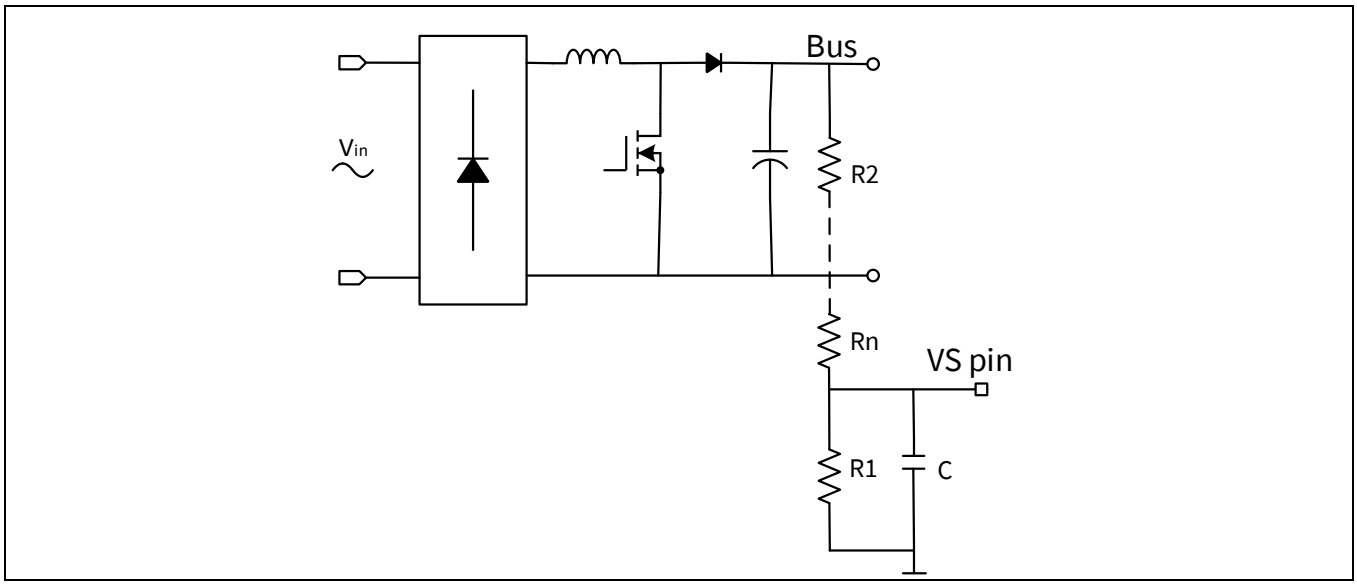

Figure 7 PFC bus voltage sensing

It is recommended to use sense resistors with a tolerance of 1% for accurate sensing. Due to the voltage stress across the upper arm resistor, it is recommended to split this value into a few resistors in series.

In order to achieve a better standby performance, the resistance of sensing resistors is suggested to select a high value. The power loss brought by these sensing resistors under standby operation can be calculated as:

$$P_{Rs\_loss} = \frac{{V_{bus}}^2}{R_1 + R_2 + \cdots + R_n}$$

To meet the low standby power consumption requirement, P_{Rs_loss} should be optimized. For example, the expected maximum power loss across these resistors, which occurs at 264Vac, is designed to be less than 15mW under standby operation,

$$P_{Rs\_loss} = \frac{(\sqrt{2}*264)^2}{R_1+R_2+\cdots+R_n} < 15mW.$$

So (R1+…+Rn) is calculated to be higher than 9.3 MΩ.

A capacitor of approximately 1nF should be added at the VS pin to ground to filter high frequency switching noise.

$$V_s = \frac{R_1}{R_1 + R_2 + \cdots + R_n} V_{bus}$$

For Over Voltage Protection (OVP), if the average sensed PFC bus voltage exceeds the OVP threshold, the PFC will stop switching while the LLC continues to run. Once the average sensed PFC bus voltage reduces and reaches the reference bus voltage, the PFC converter resumes normal operation.

The PFC Under Voltage Protection (UVP) is a protection for the LLC converter against LLC input under voltage, to avoid LLC transformer saturation or capacitive mode operation. If the average sensed PFC bus voltage falls below a configurable UVP threshold for a blanking time, then PFC under voltage is detected. As a result, PFC and LLC will stop switching immediately.

3.3.2 Redundant OVP (ROVP)

Customers may request an additional protection, Redundant Overvoltage Protection (ROVP) in case there is a component failure in the main OVP voltage divider, for a higher level of reliability.

At the same time, the requirements for standby power consumption of a power supply unit (PSU) in TV applications becomes more and more stringent.

To implement ROVP, a voltage divider consisting of resistors is usually connected between the bus and ground to detect the bus voltage (usually 350 V in standby mode, and 390 V in normal mode). These resistors will consume some power (p=v^2/R, usually 30~100 mW), which adds to the total power consumption of the PSU, and becomes a critical concern in standby mode.

Figure 9 shows a typical ROVP circuit, which is almost lossless during standby mode.

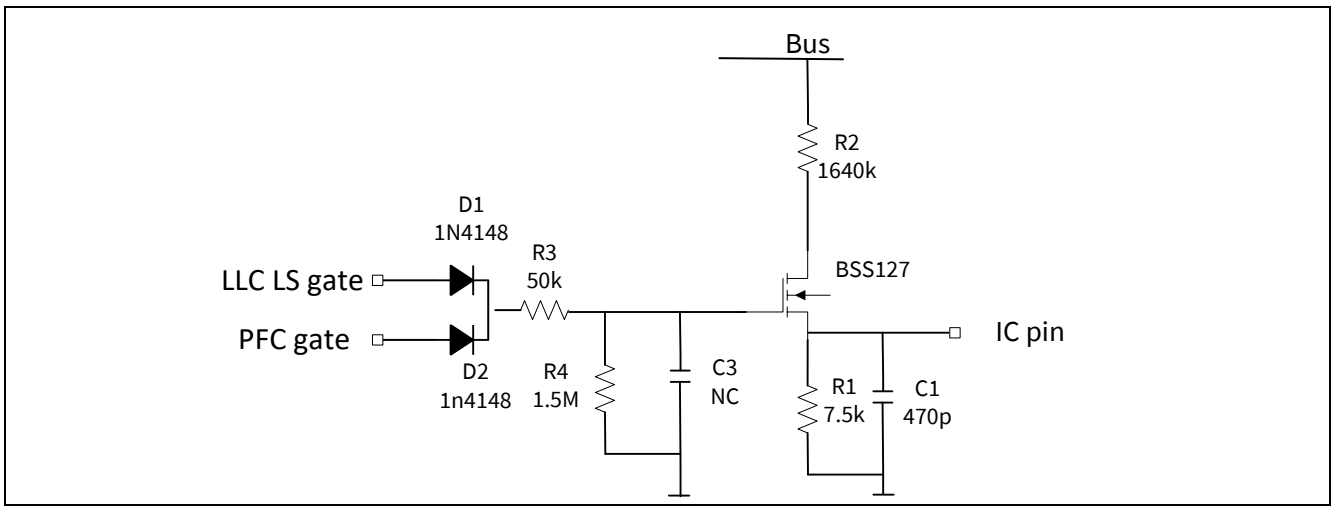

Figure 8 Typical circuit of ROVP

In Figure 8, R1&R2 are the resistor voltage divider to detect the bus voltage. The voltage divider is effective only when the BSS127 MOSFET is turned on.

The BSS127 gate drive consists of:

- two small signal diodes D1 & D2 to introduce LLC and PFC gate signals as control inputs
- R3 as a current limiter at turn on
- R4 & C3 (the input capacitance of BSS127 or an additional capacitor) network, as an RC integrator that converts “pulse” signal into a “step” signal.

In standby mode, during burst-on, when there is either PFC or LLC switching, the BSS127 MOSFET will be turned on and the voltage divider is connected to the MCOM (Multi-function and Communication) pin to detect bus voltage. During burst-off, when there is neither PFC nor LLC gate switching, the BSS127 MOSFET is open and the voltage divider is out-of-circuit. Thus, the conduction loss in the voltage divider can be avoided during burst-off, thereby saving power during standby.

During normal operation when the load is usually much larger, the IC is always active and the PFC and/or LLC switch continuously so the voltage divider is always in-circuit. However, the conduction loss is only a very small portion of the total loss.

With the IDP2303&IDP2308, the MFIO pin is used for PFC output ROVP.

As the MCOM pin is a multifunction pin, that is not dedicated for high impedance bus voltage sensing, it **must not** be connect to the bus voltage divider at start up. Current leakage into the pin during system start-up could affect the IC start-up behaviour. The proposed solution above with the BSS127 ensures a proper start-up and an almost lossless 2nd OVP function, which is almost lossless during standby mode.

Below in Figure 9 are the typical waveforms of PFC (green) and LLC (blue) gate signals, the gate signal of BSS127 (red) and voltage at the MCOM pin (yellow).

Figure 9 Typical waveforms during standby(left:20 ms/div; right: 20 ms/div)

After the IC wakes from sleep mode, the firmware starts to check the voltage at the MCOM pin after it reaches a peak and is stable. If the ROVP threshold is reached, after a defined blanking time, the IC ceases PFC switching.

If the ROVP function is not needed, customers can connect a resistor between the MCOM and GND pins to pull the ROVP pin voltage below the threshold to disable ROVP.

3.3.3 PFC ZCD divider design

To ensure apporiate operation of PFC ZCD detection, the value of R_zcd_h and R_zcd_l, as well as the PFC inductor turn ratio, should be optimized. For PFCZCD pin, there are an internal negative clamping (V_{INPCLN}), as shown in Ttable 4, with current capabitly of 2.5mA and a positive clampling (V_{D_zcd}) by two external diodes. Thus PFCZCD pin voltage can be calculated during PFC MOSFET on and inductor demagnetizing period.

PFC MOSFET on: $V_{zcd} = \begin{cases} -\frac{VIN}{n}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l}, & -\frac{VIN}{n}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l} > V_{INPCLN} \\ V_{INPCLN}, & -\frac{VIN}{n}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l} \le V_{INPCLN} \end{cases}$

PFC inductor demagnetizing period: $V_{zcd} = \begin{cases} \frac{VBUS-VIN}{n}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l}, & \frac{VBUS-VIN}{n}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l} < V_{D\_zcd} \\ V_{D\_zcd}, & \frac{VBUS-VIN}{n}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l} \ge V_{D\_zcd} \end{cases}$

In order to get a better noise Immunization performance, PFCZCD voltage is recommended to be higher than the clamping voltage. Thus the clamping current can be calculated as:

Negative clamping current: $I_{zcd} = -\frac{\left(\frac{VIN}{n}-V_{INPCLN}\right)}{R\_zcd\_h}$

Positive clamping current: $I_{zcd} = \frac{\left(\frac{V_{bus}-VIN}{n}-V_{D\_zcd}\right)}{R\_zcd\_h}$

For example, with a turn ratio of 8, diode forward voltage drop of 0.7V each, and minimum negative claming voltage 0.14V, the minimum resistor ratio can be calculated:

$$V_{zcd} = \frac{390-\sqrt{2}*264}{8}\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l} > 1.4,$$

where we can get $\frac{R\_zcd\_l}{R\_zcd\_h+R\_zcd\_l} > 0.67$. Based on the maximum negative clamping current, we could have

$$I_{zcd} = -\frac{\left(\frac{VIN}{n}-0.14\right)}{R\_zcd\_h} > -2.5mA.$$

Thus,

$$R_{zcd\_h} > 18.6k\Omega$$

Based on the calculation, the R_zcd_h can select a resistor of higher than 18.6k, while R_zcd_l can be higher than 2 times of R_zcd_h.

Table 3 PFCZCD Parameters

Parameters	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Zero-crossing threshold	V_{ZCTHR}	15	40	70	mV	
Comparator propagation delay	t_{ZCPD}	30	50	70	ns	$dV_{ZCD}/dt = 4V/\mu s$
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	

3.3.4 Current sense and Over Current Protection (OCP)

The PFCCS pin is used to sense the drain-source current of the switching MOSFET. The voltage measured is only valid after a certain blanking time following the turn-on of the switch. A low pass RC filter should be added the pin to filter high frequency switching noise.

An appropriate sensing resistor value should ensure that:

- The triggering of OCP protects the PFC inductor from saturation and other components from over current stress.
- The triggering of OCP does not occur during normal operation.

3.3.4.1 Over Current Protection(OCP) tolerance & selection of current sense resistor

From the datasheet (Table 4), the parameters of the IC that will affect OCP protection tolerance are:

- OCP1 threshold tolerance
- OCP1 comparator propagation delay

Table 4 Electrical characteristics of the CSx pin

Parameters	Symbol	Values			Unit	Note/Test condition
		Min.	Typ.	Max.		
OCP, OCP1 threshold tolerance	ΔV_{OCP1}	—	—	±6.2	%	
Delay from V_{CSx} crossing $V_{CSxOCP1}$ to CSx_OCP1 rising edge, 1.2 V range	t_{CSOCP1}	20	320	620	ns	[1] input signal slope dV_{CS}/dt = 10 mV/µs [2]
		90	170	250	ns	[1] input signal slope dV_{CS}/dt = 150 mV/µs [2]
		90	140	210	ns	[1] input signal slope dV_{CS}/dt = 300 mV/µs [2]

[1] Not tested in production test.

[2] This slope represents a use case of a switch-mode power supply with minimum input voltage.

In reality, external circuit specifications also come into play. For example, from Figure 10, it can be seen that the external parameters affecting OCP protection are:

- The gain error caused by the external RC filter
- The external delay caused by the RC filter
- External propagation delays caused by the gate discharge and MOSFET drain-source capacitor discharge

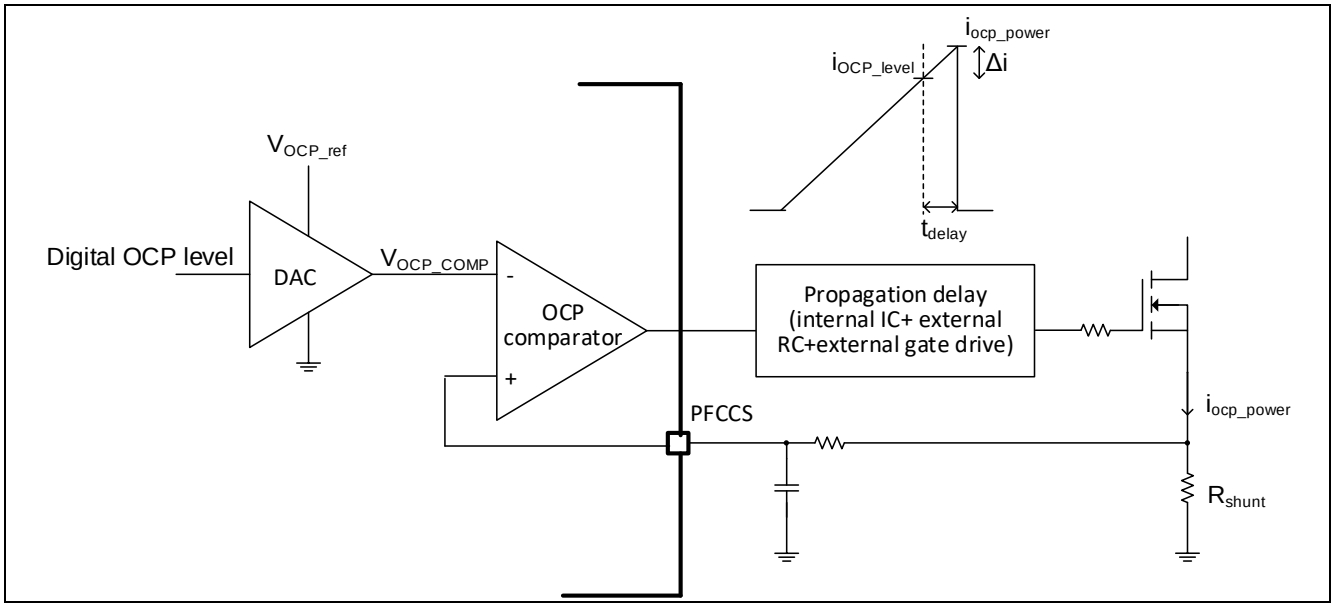

Figure 10 OCP protection implementation structure

A spradsheet-based calculation example for selecting the current sense resistor and the OCP tolerance is shown in Figure 11.

Calculation of OCP tolerance:						
	tolerance	unit	min	typ	max	note
Calculation of OCP						
OCP1 threshold	6.20%	mV	563	600	637	
R_{filter}	1%	Ω	504.9	510	515.1	
C_{filter}	20%	pF	800.0	1000	1200.0	selected by customer
f_{sw}		kHz	60.0	90	120.0	Frequency law range
RC filter gain g_{filter}			0.906	0.961	0.989	$g_{filter}=\frac{1}{\sqrt{1+(2\pi fRC)^2}}$
OCP1 level after RC filter gain			510	577	630	
OCP1 level tolerance with RC filter			-11.51%	577	9.27%	
Calculation of OCP delay time:						
delay caused by RC filter τ		ns	403.9	510	618.1	τ=RC
internal propagation delay t_{int}		ns	90	170	250	Internal Propagation delay
external propagation delay t_{ext}	20%	ns	200.0	250	300.0	external Propagation delay from IC gate low threshold to MOSFET off, including gate discharge, MOSFET drain source cap discharge (measured by customer)
Calculation of ΔI due						
lowest V_in (results in max. current)		Vrms	90.0	90	90.0	
L of inductor	7%	µH	158.1	170	181.9	
dI/dt max. rising at V_in peak		A/µs	0.700	0.749	0.805	$\frac{di}{dt}$=V/L
Δ I due to propagation delay		A	0.486	0.696	0.940	$\Delta i=\frac{V}{L}(t_{int}+t_{ext}+\tau)$
Calculation of shunt resistor value						
Pout_90Vac		W	130			minimum deliverable output power
Efficiency			0.93			
Pin		W	140			
Vinac_min		V	90			
Ipk_power		A	4.393			$I_{pk\_power}=2\sqrt{2}\frac{P_{in}}{V_{in}}$
due to propagation delay I_{OCP_level}		A	3.907			$I_{OCP\_level}=I_{pk\_power}-\Delta I$
R_shunt		mΩ	131			
R_shunt	5%	mΩ	111.6	124	131	selected actual shunt resistance value
Calculation of current and power tolence						
Ipk_power		A	4.393	5.34	6.584	
Ipk_power with tolerance			-18%	5.34	23%	
Pout_90Vac			130	158	195	
Pout with tolerance			-18%	158	23%	

Figure 11 Accurate calculation of OCP tolerance

It can be seen from the calculation that the actual tolerance of current and power can be very high. Methods to reduce tolerances include:

- Reduce the tolerance of the shunt resistor
- Reduce the tolerance of the PFC choke
- Reduce the value of R and C for the RC filter to reduce the delay

The above calculation is accurate, but is relatively complicated, and requires input data from actual measurements on a real power board (e.g. external propagation delay). A faster and simpler way to obtain a value for the current sense resistor is for customers to use the spreadsheet calculation to finalize the value after the power board is built.

$$R_{PFC\_CS} < \frac{V_{OCP\_PFC} * (1 - g_{error}) * g_{filter}}{I_{pk} * (1 - \Delta_{delay})} = \frac{0.6 * 0.94 * 0.9}{4.39 * (1 - 0.1)} = 0.13\ \Omega$$

Where g_{error} is the OCP threshold gain error, g_{filter} is the gain of RC filter and Δ_{delay} is the estimated error due to the internal and external propagation delay.

3.3.4.2 Verification of PFC inductance with OCP tolerance

The maximum peak current allowed by the OCP (considering the tolerance) can be obtained from the spreadsheet calculation results and then applied to the equation below to verify the B_{max} of the PFC inductance:

$$B_{max} = \frac{i_{pk} * L_{PFC}}{N_{PFC} A_{min}} = \frac{6.7 * 200}{39 * 99} = 0.34\ T$$

This value is less than the saturation magnetic flux density (B) of 0.35 T (PC40 magnetic material). Therefore, the PFC choke will not saturate under worst case conditions.

3.3.5 Frequency law for multi-mode PFC

3.3.5.1 Multimode PFC

For a PFC circuit operating in Critical Conduction Mode (CrCM), the MOSFET is turned on with a constant on-time throughout the complete AC half cycle and the off-time varies during the AC half cycle depending on the instantaneous input voltage applied. A new switching cycle starts just after the inductor current reaches zero. CrCM is also equivalent to quasi-resonant switching at the first inductor current valley or QR1 operation.

CrCM is ideal for full load operation, where the constant on-time is large. However, the constant on-time reduces at light load, resulting in very high switching frequency - particularly near the zero crossings of the input voltage. The high switching frequency will increase the switching losses, resulting in poor efficiency at light load.

The multimode PFC control can lower the switching frequency by adding an additional delay (t_w) into each switching cycle through selecting further inductor current valleys (matching also with valleys of V_{DS} of MOSFET) to achieve QR2, QR3 and up to QR10 operation. Figure 12 illustrates the QR2 valley switching in multimode PFC control as an example.

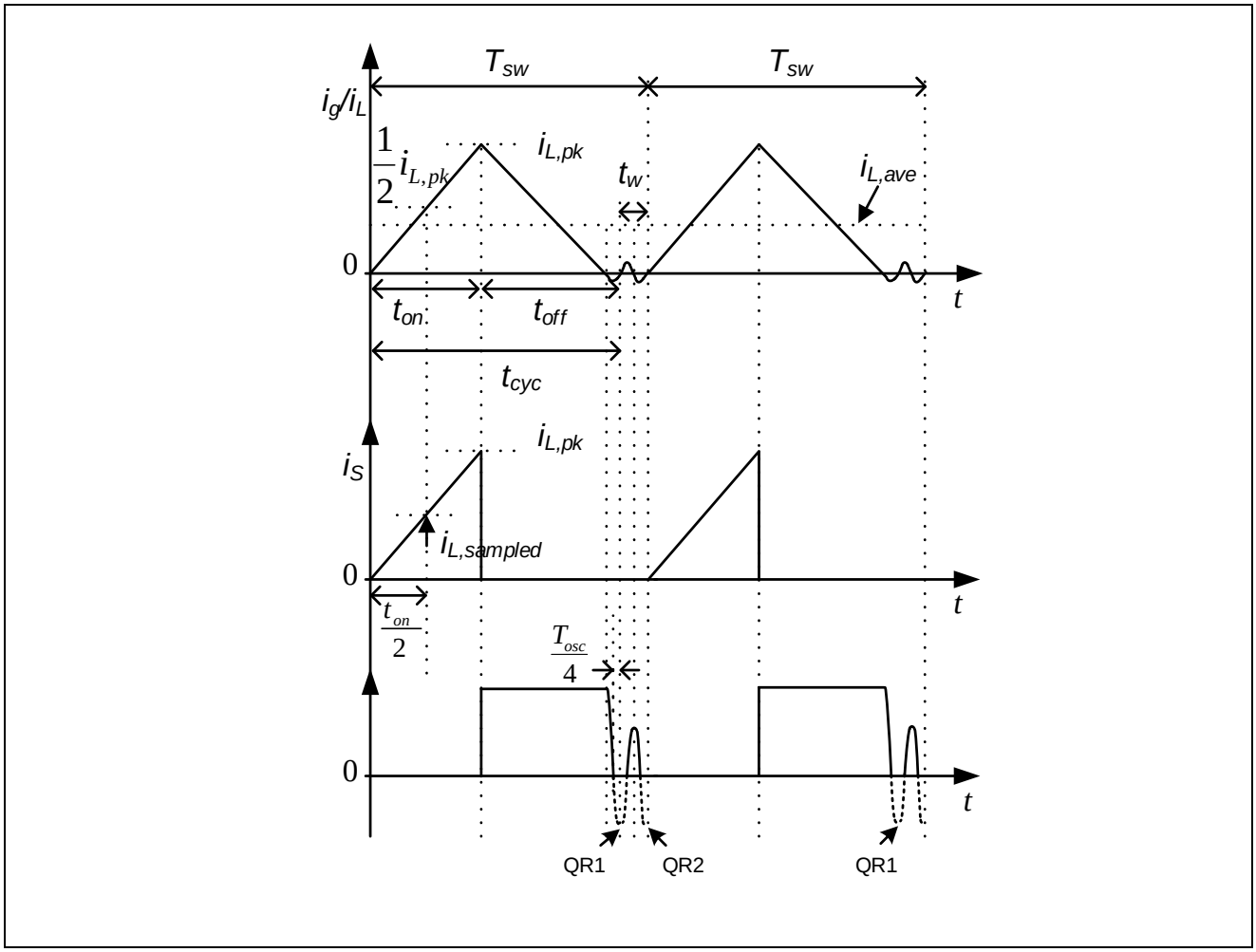

Figure 12 Current and timing in QR2 operation

3.3.5.2 Frequency law

A frequency law consisting of a maximum switching frequency f_{swmax} and the minimum switching frequency f_{swmin} is defined for the valley selection (QRN). In this way, the switching frequency is limited to the defined range and efficiency at light load can be improved. An illustration of the frequency law is shown in Figure 13.

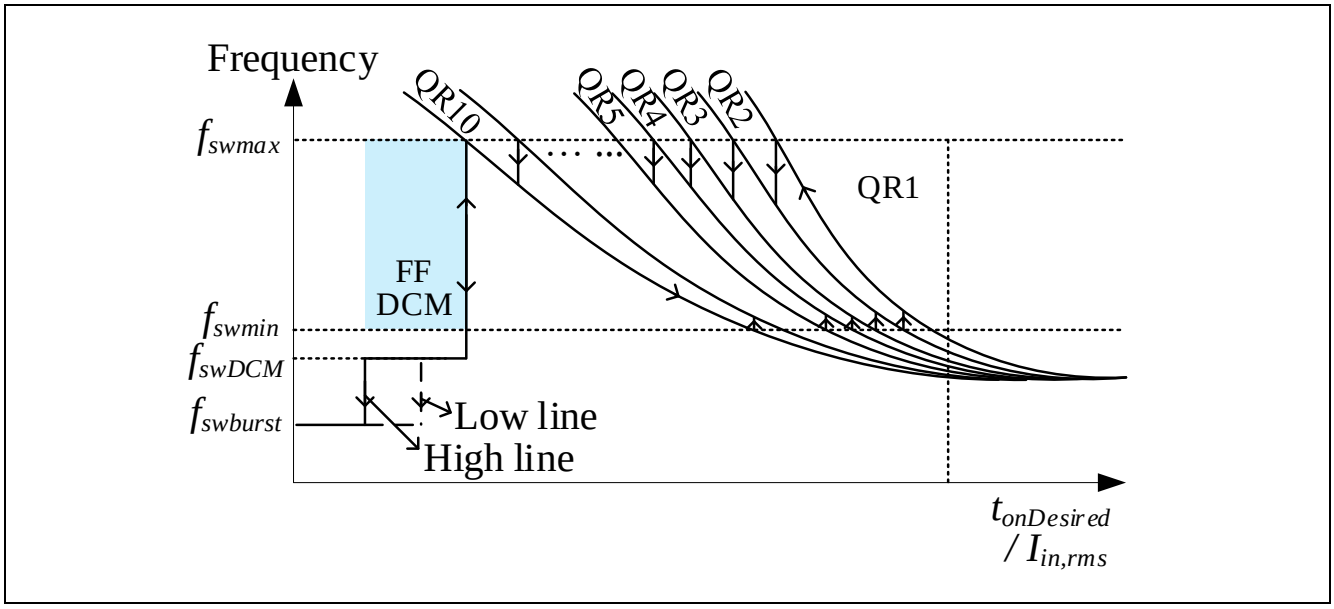

Figure 13 Frequency law for selecting operating modes

The real-time operation of QRN is executed by the IDP230x hardware peripheral QR-timer. A new switching cycle of QRN operation starts with the N-th valley detection of the sensed inductor voltage or with the end of the maximum switching period, whichever occurs first. As illustrated in Figure 12, occurrence of the N-th valley is determined by the N-th falling edge of the ZCD comparator plus a propagation delay that is equivalent to $T_{osc}/4$ to reach the valley switching point. T_{osc} is the resonance period of the oscillation due to the PFC inductor and the parasitic capacitance across the MOSFET after the end of boost inductor demagnetization time.

The changing of QRN in multimode control is dependent on the frequency law. When the switching frequency reaches the min frequency, the frequency law defines that the frequency is too low and the switching frequency must increase by reducing the QRN. When the switching frequency reaches the maximum frequency, the frequency law defines that the frequency is too high and switching frequency must reduce by increasing the QRN. The changing of QRN within each AC half cycle is dependent on both the load and AC line, and is inherent in multimode PFC control.

3.3.5.3 Setting of f_{min} and f_{max}

The setting of minimum and maximum frequencies of the frequency law needs to meet the application requirement that in the condition where V_{IN} = 90 V_{AC}, full load, the PFC should operate with QR1 mode operation over the whole AC cycle.

From the equation defining the switching frequency with QR1 operation

$$f = \frac{v_{in} * (v_{bus} - v_{in})}{v_{bus} * L_{PFC} * i_{in}}$$

It can be concluded that over the AC cycle, the switching frequency is at a minimum at AC peak and at a maximum at zero crossing. The same applies to QR2 operation.

Therefore, selection rule for f_{min} is : A value above the maximum switching frequency at the peak of the AC input voltage with QR2 operation and minimum PFC inductance should be selected to force QR1 operation.

Selection rule for f_{max} is: A value above the maximum switching frequency near the zero crossing of the AC input voltage with QR1 operation and minimum PFC inductance should be selected to keep QR1 operation.

3.3.6 AC brown-in & out

The PFC brown-in & out protections prevent the system from starting up or operating at very low input voltage outside the designed operating range. For a system without input brown-in & out protection, the boost converter may draw a higher current from the mains at a given output power which may lead to overheating of the MOSFET and boost diode. PFC brown-in & out protections are implemented by firmware and utilize the HV pin for AC input voltage sampling.

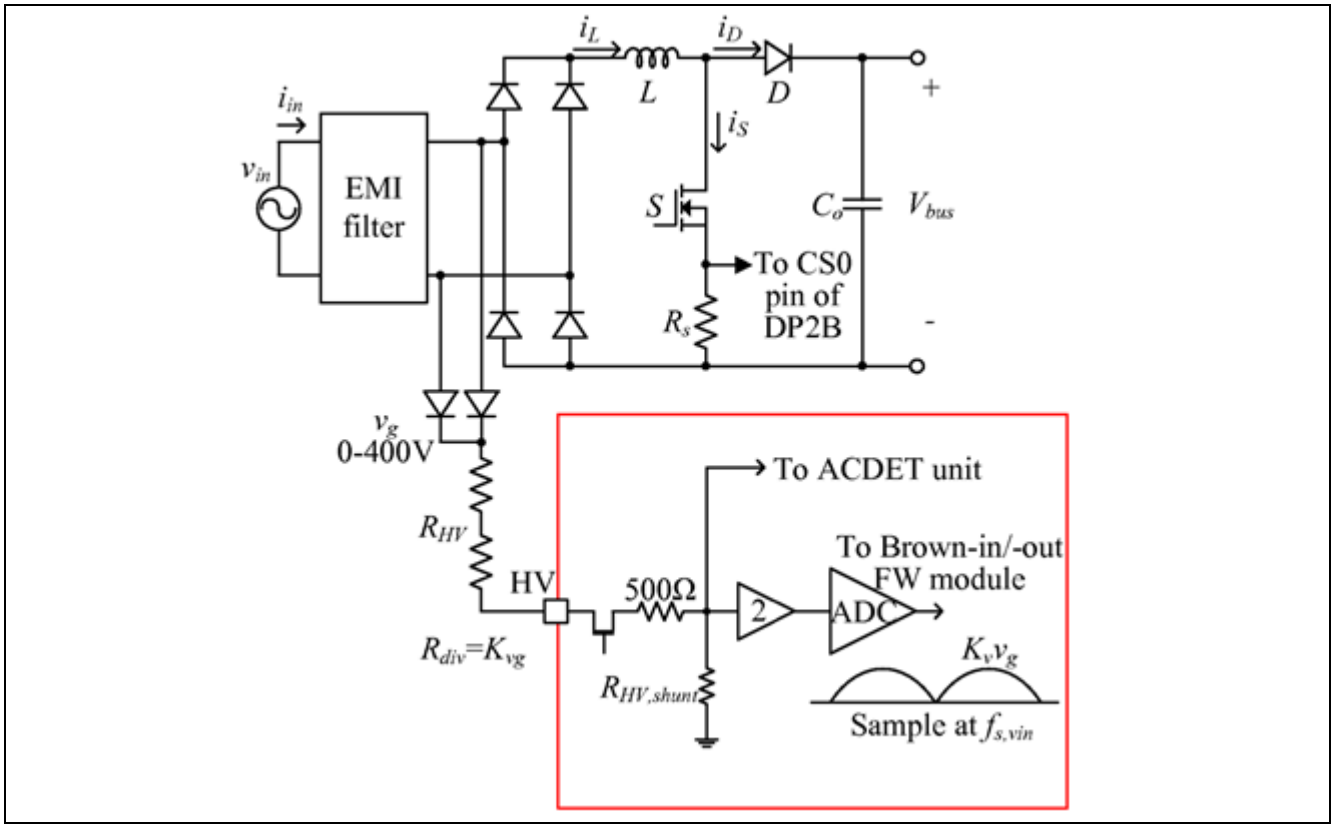

Figure 14 Sampling of the rectified AC input voltage

The rectified AC input voltage V_g is measured using the HV pin of the IDP230x across an internal shunt resistor as shown in Figure 14. The internal shunt resistor R_{HV}, shunt (set to 125 Ω), internal 500 Ω series resistor and the external R_{HV} resistors (to save design effort, a value of 51k Ω, with 1% tolerance is advised) form a resistor divider with the ratio K_{vg}. There is an internal op-amp with a fixed gain of 2. Thus, the magnitude of the sensed input voltage at the ADC buffer is given by:

$$v_{g\_ADC} = 2K_{vg}v_g = 2\frac{R_{HV\_shunt}}{R_{HV} + 500 + R_{HV\_shunt}}v_g = 2\frac{125}{51 \times 10^3 + 500 + 125}v_g = 4.84 \times 10^{-3}v_g$$

For ease of implementation, the RMS input voltage v_{g_rms} is estimated from the peak value $v_{g\_ADC\_pk}$ of the sampled input voltage.

If v_{g_rms} exceeds the desired brown-in input voltage threshold, brown-in is detected and the system enters startup.

If v_{g_rms} falls below the desired brown-out input voltage threshold then, after a blanking time, brown-out is detected. The PFC will stop switching immediately.

The brown-in and out thresholds are set as 70 V_{AC} and 60 V_{AC} and they are configurable via dpVision.

4 LLC design

4.1 Target specifications

The LLC target specifications are summarized in Table 5.

Table 5 Design parameters for the LLC design

Parameter	Symbol	Value	Unit
Bus bulk capacitor	C_{bulk}	68 x 2	µF
Output voltage	V_{o_24}	24	V
Output current	I_{o_24}	3.5	A
Output voltage	V_{o_12}	12	V
Output current	I_{o_12}	3	A
Output power	P_{o_LLC}	120	W
LLC efficiency	η_{LLC}	93%	
Resonant frequency	f_r	100	kHz
Hold up time	t_{hold}	20	ms

4.2 Power stage

A simplified application circuit for the LLC stage is given in Figure 15 :

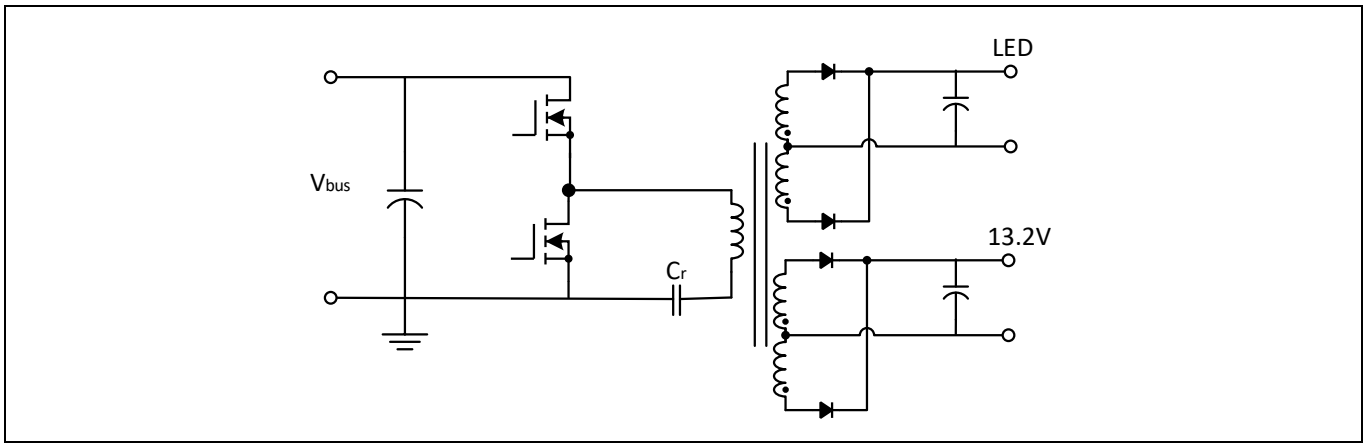

Figure 15 Simplified circuit for LLC converter

4.2.1 System parameter calculation

Based on the required 20 ms hold-up time for the system, the minimum operation voltage for the LLC stage can be calculated as:

$$V_{bus\_min} = \sqrt{{V_{bus}}^2 - \frac{2P_{o\_LLC}T_{hold}}{\eta C_{bulk}}} = \sqrt{390^2 - \frac{2 * 120 * 20 * 10^{-3}}{0.93 * 68 * 2 * 10^{-6}}} = 337\ V$$

4.2.2 Main transformer and resonant network

4.2.2.1 Transformer turns ratio

In this design, an integrated transformer is considered, where the leakage inductance is used as a series inductor, while the magnetizing inductor is used a shunt inductor. The all-primary-referred model of the transformer is shown in Figure 16, where n_e is the equivalent turns ratio. All the elements related to leakage flux are located on the primary side.

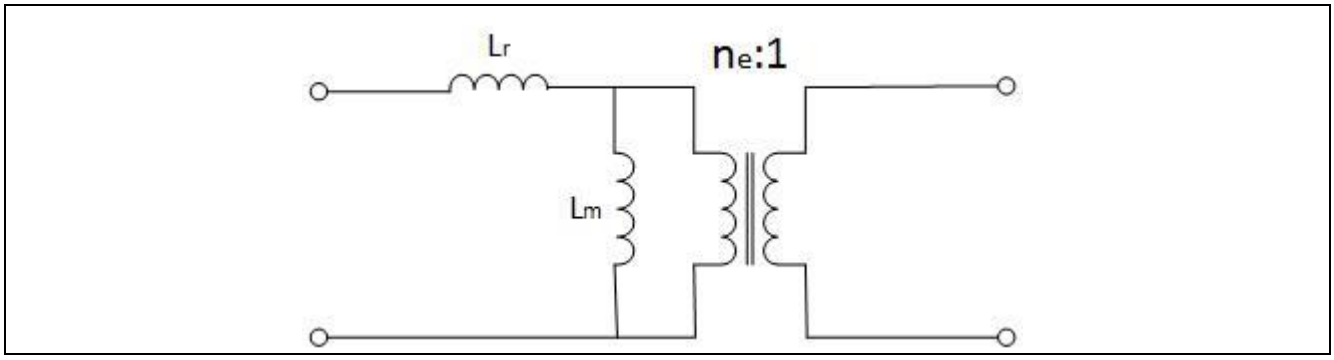

Figure 16 Transformer primary referred model

When a separate resonant inductor is used, the equivalent turns ratio n_e is equal to the physical turns ratio. With an integrated resonant inductor, the equivalent turns ratio n_e is less than the physical turns ratio, due to the leakage inductance in the transformer secondary.

The equivalent turns ratio can be estimated as:

$$n_e = \frac{n}{M_v}$$

where

$$M_v = \sqrt{\frac{m}{m-1}}$$

m is the ratio between the primary inductance L_p $(= L_m + L_r)$ and resonant inductance L_r:

$$m = L_p / L_r$$

In this design example, $m = 4.35$ is pre-selected as a starting point, based on the transformer bobbin available and the rule of thumb. Verification and optimization is required for a given implementation, switching frequency and design power level. Guidance on selection will be provided in a later section.

The required equivalent turns ratio can be calculated as:

$$n_e = \frac{V_{bus\_nom}}{2(V_o + V_f)} = \frac{390}{2(24 + 0.5)} = 8$$

Assuming the forward voltage drop of secondary-side rectifier diode $V_f = 0.5\ V$.

Correspondingly the physical turns ratio of the transformer n will be -

$$n = n_e M_v = n_e \sqrt{\frac{m}{m-1}} = 8 * 1.14 = 9.1$$

Consider that, in an actual design, n is adjusted to be 8.5. Then the corresponding n_e is 7.5. The corresponding gain at nominal input voltage is

$$M_{nom} = \frac{2(V_o + V_f)n_e}{V_{bus\_nom}} = 0.94$$

The maximum voltage gain M_{max} required is during conditions of full load operation at minimum input voltage V_{bus_min}, which can be calculated as:

$$M_{max} = \frac{V_{bus\_nom}}{V_{bus\_min}} M_{nom} = \frac{390}{338} 0.94 = 1.08$$

4.2.2.2 Equivalent circuit and resonant network

All analysis and calculation in this section is based upon the equivalent circuit in Figure 17 that can be derived with the First Harmonic Approximation (FHA) modelling methodology.

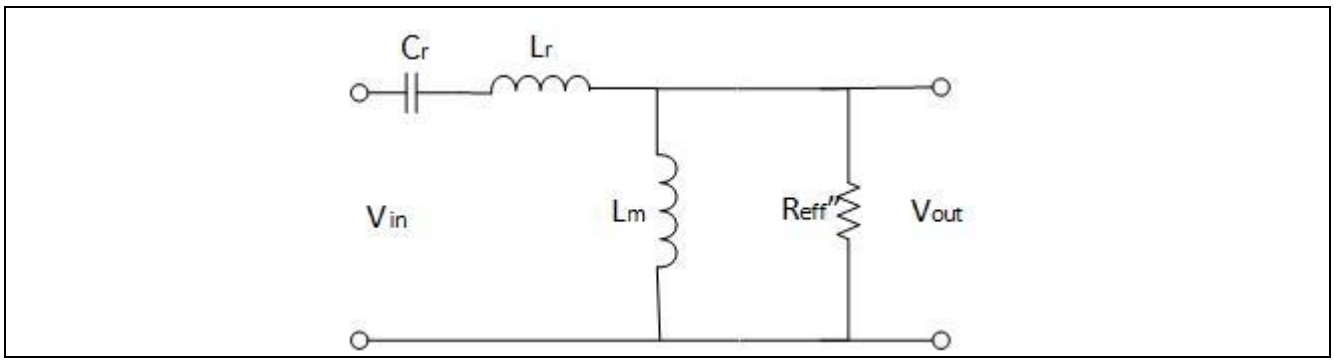

Figure 17 Equivalent circuit

If the total output load is referred to 24 V, the effective load resistance can be given as:

$$R_{eff} = \frac{8}{\pi^2} {n_e}^2 \frac{V_o}{I_o} = \frac{8}{\pi^2} 7.55^2 \frac{24}{5} = 216\ \Omega$$

Defining the normalised frequency f_r is $F = \frac{f}{f_r}$, the load factor of the LLC converter is $Q_e = \frac{\sqrt{L_r/C_r}}{R_{eff}}$, the voltage gain of the converter can be obtained based on the equivalent circuit Figure 18:

$$M_j(F,Q) = \frac{F^2(m-1)}{(F^2 m - 1) + jF(F^2-1)(m-1)Q_e}$$

Its magnitude is:

$$G(F,Q) = \sqrt{Re(M_j(F,Q_e))^2 + Im(M_j(F,Q_e))^2}$$

The graph of voltage gain G vs F for different values of Q can be plotted as in Figure 18, based on the equation above:

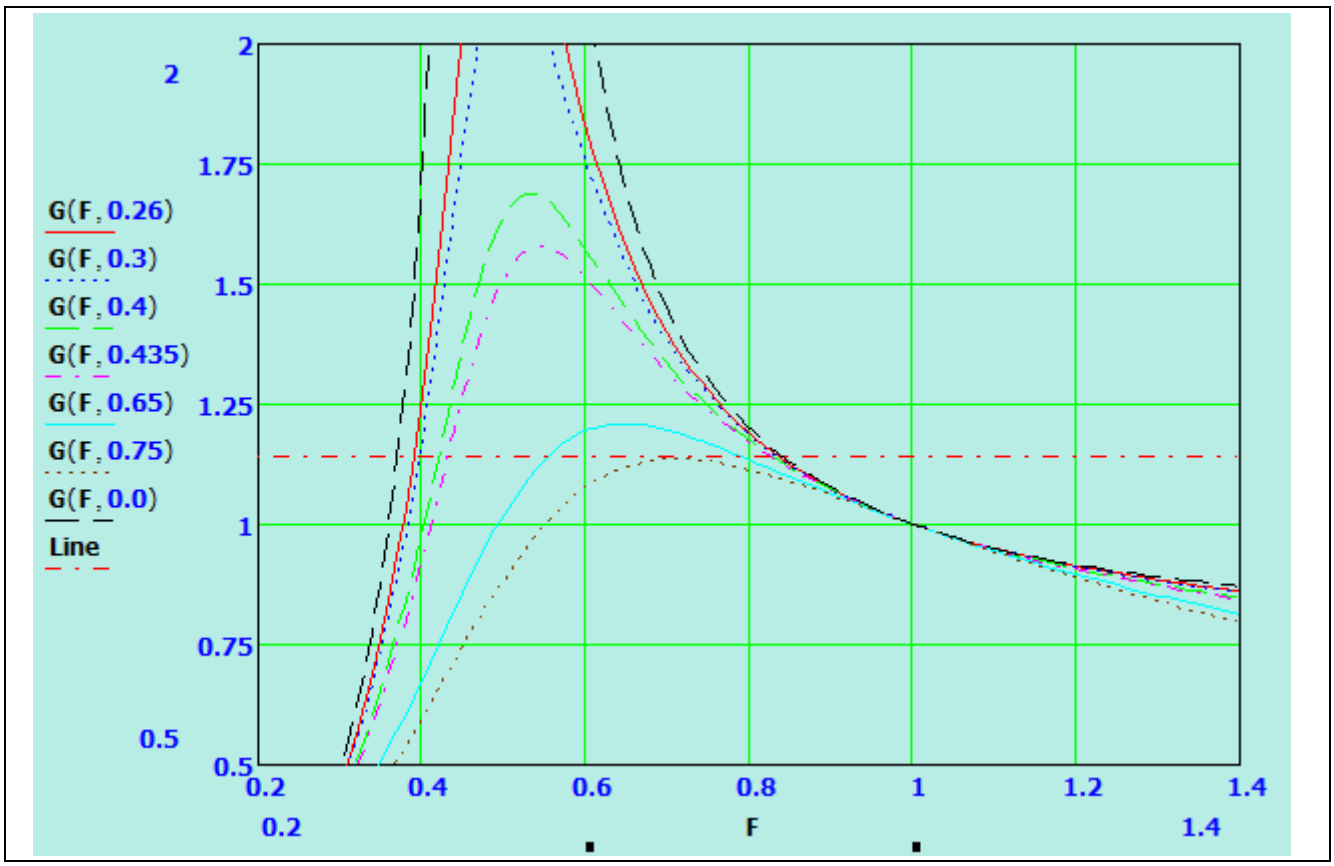

Figure 18 Voltage gain G Vs normalized frequency F

The curve where $Qe = 0.75$ can achieve the required peak gain, G_{pk}, which is M_{max} , $G_{pk} = M_{max} * 1.05 = 1.14$

Having found the proper Qe, we can calculate C_r, L_r and L_p as follows:

$$C_r = \frac{1}{2\pi * Qe * f_{r*}R_{eff}} = \frac{1}{2\pi * 0.75 * 100 * 10^3 * 218} = 9.8\ nF$$

If a 10 nF capacitor is selected as C_r, then, in the actual design, Qe must be re-calculated as

$$Qe = \frac{1}{2\pi * C_r * f_{r*}R_{eff}} = 0.74$$

$$L_r = \frac{1}{(2\pi f_r)^2 C_r} = \frac{1}{(2\pi * 100 * 10^3)^2 * 10 * 10^{-9}} = 253\ uH$$

$$L_p = mL_r = 1.1\ mH$$

The value of L_p can be achieved by adjusting the gap length.

From the gain curve with $Qe = 0.74$ in Figure 18, the normalized frequency $F_{min} = 0.87$ can be located to achieve the required maximum gain $G_{pk} = 1.08$, for the condition of minimum input voltage at full load. Accordingly, the actual minimum frequency f_{min} is:

$$f_{min} = F * f_r = 0.87 * 100 = 87\ kHz$$

Similarly, the normalized frequency $F_{nom} = 1.1$ can be located to achieve gain, $G = M_{nom} = 0.94$ for nominal input voltage at full load. Accordingly, the actual nominal frequency f_{nom} is:

$$f_{nom} = F * f_r = 1.1 * 100 = 110\ kHz$$

4.2.2.3 Calculation of transformer turn ratio

In the above section, the actual minimum frequency f_{min} has been calculated as 87 kHz.

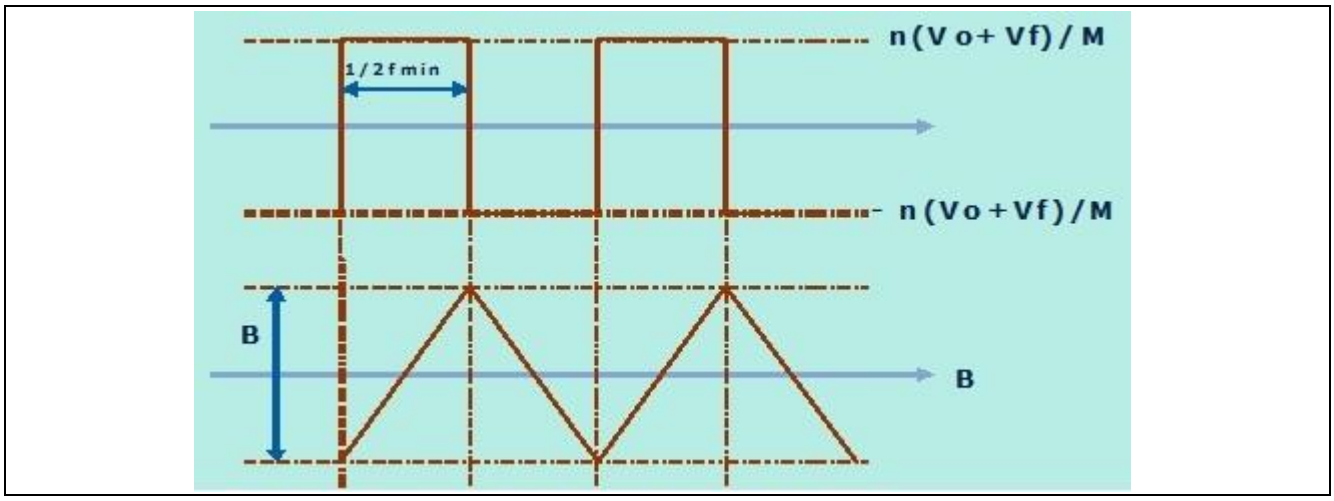

Figure 19 Flux density swing

According to the flux density swing illustrated in Figure 19, the voltage across the primary winding can be calculated as $V_p = n_e(V_o + V_f)$. The half switching cycle period is around $t = \frac{1}{2f}$. According to Faraday's law:

$$\frac{n_e(V_o + V_f)}{2f} = N_p A_e \Delta B$$

The number of turns on the primary side can be found by:

$$N_P = \frac{n_e(V_o + V_f)}{2f * A_e \Delta B}$$

Where $A_e = 88\ mm^2$ with an EFD38 core. $\Delta B = 0.62T$ is selected to avoid magnetic saturation.
Then N_{pmin} can be calculated at minimum bus voltage V_{bus_min} by:

$$N_{pmin} = \frac{n_e(V_o + V_f)}{2f_{min} * A_e \Delta B} = \frac{7.5 * (24 + 0.5)}{2 * 87 * 10^{-3} * 88 * 10^{-6} * 0.62} = 20$$

The selection of the number of turns on the primary side must also take other factors into consideration. For example, to minimize the circulating current in the primary side due to the magnetizing current, a relatively larger magnetizing inductance is preferred. Furthermore, the number of turns on the secondary side for 24 V and 12 V should be integers. The selection is also limited by the structure of the EFD38 transformer available. Lastly, the number of turns on the primary side is selected as $N_p = 51$. The secondary side turns for 24 V and 12 V can then be calculated accordingly by:

$$N_{s\_24V} = \frac{N_p}{n} = 6$$

$$N_{s\_12V} = \frac{N_{s\_24V}}{2} = 3$$

4.2.2.4 Selection of resonant factor m

Numerous factors come into play while considering the value of the resonant factor m.

$$m = \frac{L_p}{L_r} = \frac{L_m + L_r}{L_r}$$

In order to achieve the highest efficiency possible, the magnetizing inductance L_m should be set to be large. Therefore, the magnetizing current I_{mag} is small for the specified value of bus voltage and switch-on time, thus allowing for low core and conduction loss in transformer.

$$I_{mag} = \frac{1}{4}\frac{V_{bus} t_{on}}{L_m}$$

On the other hand, the magnetizing current must be large enough to charge and discharge the output capacitance C_{sw} of the primary side MOSFET during the deadtime t_{dt}, to achieve ZVS and thus ensure safe switching and reduce switching losses.

$$I_{mag} \cong \frac{V_{bus} C_{sw}}{t_{dt}}$$

Furthermore, sufficient magnetizing current is required to ensure that the MOSFET body diode can complete reverse recovery during turn-on at light load [4].

The value of the resonant factor m also has an effect on the shape of gain curves and the attainable maximum gain. Larger values of m result in flatter gain curves which leads to a wider operation frequency range.

In the real world, the selection of m is also limited by the structure of the selected transformer, which determines the value of the leakage inductance L_r.Therefore, determining the value of m can be an iterative process involving many factors.

4.2.2.5 Selection of resonant capacitor

The current through the resonant capacitor is the sum of the magnetizing current and the load current referred to the primary. Its RMS value can be calculated as:

$$I_{C_r\_rms} = \frac{1}{\eta}\sqrt{\left(\frac{\pi I_o}{2n_e\sqrt{2}}\right)^2 + \left[\frac{n_e(V_o+V_F)}{4\sqrt{2}f_{nom}M_{nom}(L_p-L_r)}\right]^2}$$

$$= \frac{1}{0.93}\sqrt{\left(\frac{\pi * 5}{2 * 7.5\sqrt{2}}\right)^2 + \left[\frac{7.5 * (24+0.5)}{4\sqrt{2} * 110 * 10^3 * 0.94 * 847 * 10^{-6}}\right]^2} = \frac{1}{0.93}\sqrt{0.74^2 + 0.37^2}$$

$$= 0.89\ A$$

The voltage across the resonant capacitor reaches a peak at the over current trigger point (OCP), which is estimated to have a 65% margin over the peak current in the primary side during normal operation. The accurate maximum OCP trigger point, including consideration of the tolerance is calculated in section 4.3.2.

$$I_{ocp} = \sqrt{2} I_{C_r\_rms}(1 + 65\%) = 2.1\ A$$

$$V_{C_r} \cong \frac{V_{bus}}{2} + \frac{I_{ocp}}{2\pi f_{min} C_r} = \frac{390}{2} + \frac{2.1}{2\pi * 100 * 10^3 * 10 * 10^{-9}} = 529\ V$$

A 630 V rated low-ESR film capacitor is selected as the resonant capacitor.

4.2.3 Power MOSFET selection

It is important to select the correct MOSFET; not only for the efficiency but also for the reliability of an LLC resonant converter [4]. In addition to the basic criteria such as package, drain-source voltage rating, drain current rating and on-state resistance, two considerations are required for power MOSFET selection and driving signal design in an LLC resonant converter:

- maintenance of Zero Voltage Switching (ZVS) operation of the power MOSFET;
- avoidance of system reliability issues due to incomplete body diode reverse recovery in the power MOSFET

Infineon high voltage MOSFETs have several families based on different technologies, which each target a specific application, topology or operation. Several CoolMOS™ series can be used for boost applications depends on customer's requirement for the voltage rating, thermal characteristic etc.

With the CE in 500 V, E6 and P6 family in 600 V, Infineon offers series with extremely low conduction and switching losses and can make switching applications more efficient, more compact, lighter and cooler.

The IPD50R1K4CE is pre-selected for the design and the conduction loss is calculated as below.

The maximum drain current through the MOSFET is the same as that through the resonant capacitor.

$$I_{Q2\_RMS} = I_{C_{r\_rms}} = 0.89\ A$$

$$P_{con} = {I_{Q2\_rms}}^2 R_{DS_{on}} = 0.89^2 * 2.5 = 1.98\ W$$

$R_{DS_{on}} = 2.5\ \Omega$ is the on-state resistance of MOSFET at junction temperature of 100°C.

4.2.4 MOSFET gate driving

Similar to the PFC gate driver, the LLC low side gate driver offers unique features such as configurable charge current and output voltage.

The recommended R_{gate} values for different application cases with all possible values of C_{gate}, R_{gs} and gate-source current are summarized below in Table 6. As a rule-of-thumb, a 10 Ω gate resistor generally fits for most application cases.

Table 6 Recommended R_{gate} values for different C_{gate}, R_{gs} and gate source current

C_{gate} (nF)	0.4~2.0					
gate source current (mA)	30		73		120	
R_{gs} (Ω)	10 k	100 k	10 k	100 k	10 k	100 k
Recommended R_{gate} (Ω)	5~30	5~35	5~25	5~25	5~15	5~15

The LLC high side gate driver is an integrated floating driver based on coreless transformer technology. To generate a balanced gate driving signal (rise/fall time) with a low side to avoid shoot-through and other possible problems, a larger gate resistor is usually required (approximately 120 Ω). The customer can fine-tune the value by monitoring the gate and other signals at the high and low side to ensure safe operation.

4.2.5 Output rectifier

The voltage stress on the 12 V and 24 V output rectifier diodes are:

$$V_{D\_12} = 2 * (V_o + V_f) = 2 * (12 + 0.5) = 25\ V$$

$$V_{D\_24} = 2 * (V_o + V_f) = 2 * (24 + 0.5) = 49\ V$$

The RMS value of the current flowing through each diode is:

$$I_{D\_rms\_12} = \frac{\pi}{4} I_o = \frac{\pi}{4} * 3 = 2.36\ A$$
$$I_{D\_rms\_24} = \frac{\pi}{4} I_o = \frac{\pi}{4} * 3.5 = 2.75\ A$$

Considering the voltage overshoot due to the stray inductance, 60 V/20 A and 100 V/30 A Schottky diodes are selected as the rectifier diodes for the 12 V and 24 V channels, repectively.

4.3 Control parameters and protections

4.3.1 VCO frequency curve

During normal LLC operation, a voltage-controlled oscillator (VCO) generates the LLC converter switching frequency f_{HB} based on the average LLC feedback voltage V_{HBFB}.

With a DPdigital controller, a VCO curve based on switching period can be easily implemented digitally. The curve of the LLC switching period T_{HB} with respect to the feedback voltage V_{HBFB} is shown in the figure below.

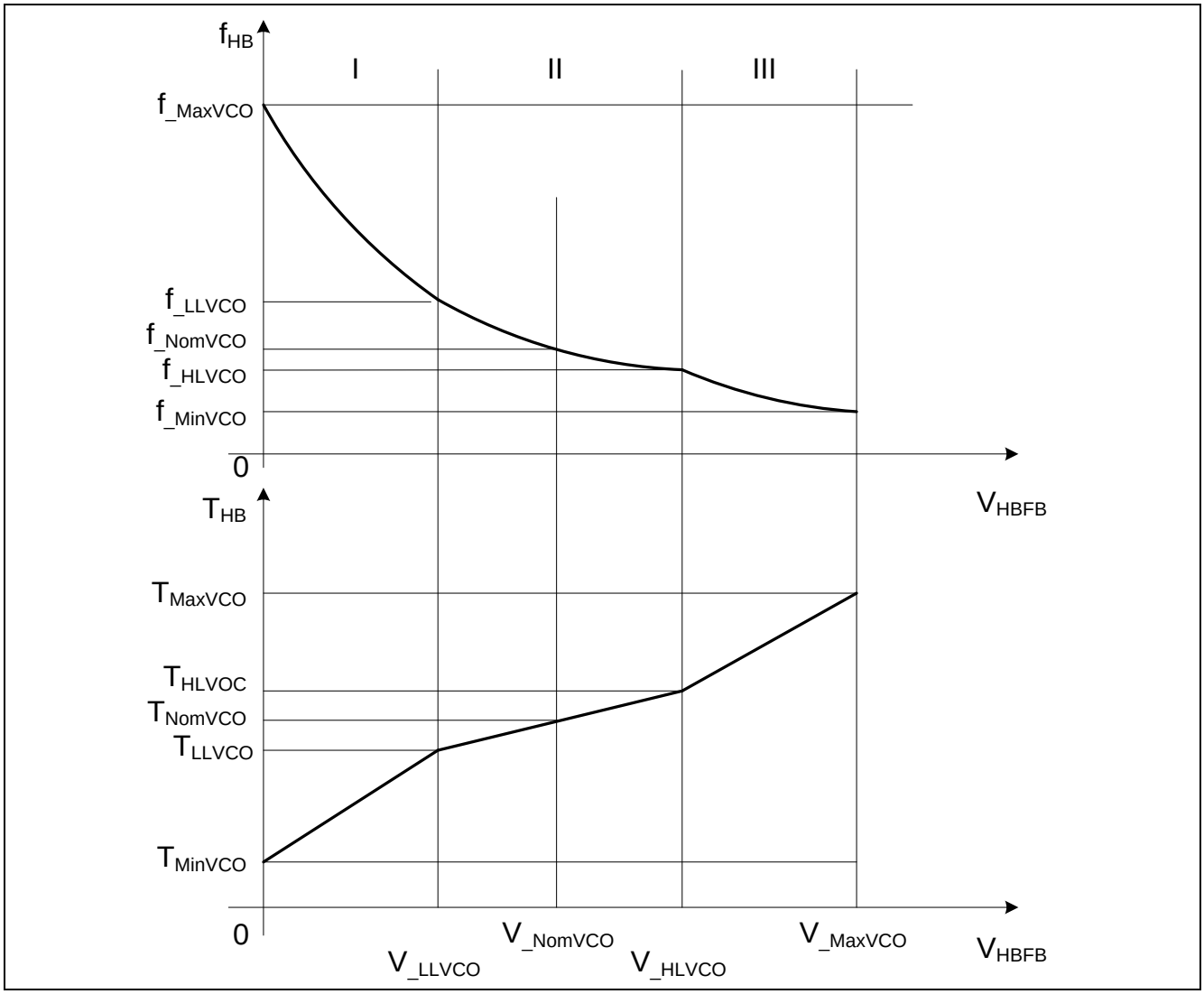

Figure 20 VCO curve

The VCO curve consists of three linear sections with different slew rates. As shown in the lower half of Figure 20, the line in area II (normal operation) has much lower slew rate than the line in areas I (light load) and III

(heavy load). Therefore, the VCO in the area II has a much better frequency resolution than in the area I and III. In this way, fine frequency resolution around the nominal operating point V_{NomHB} is realized, while a wide operating frequency range can be covered with fast response to the load change in both heavy and light load is realized.

To define a proper VCO, 4 key points have to be determined.

- $V_{\_MinVCO}$: $f_{\_MaxVCO}$ (feedback origin)
- $V_{\_LLVCO}$: $f_{\_LLVCO}$ (light load)
- $V_{\_HLVCO}$: $f_{\_HLVCO}$ (heavy load)
- $V_{\_MaxVCO}$: $f_{\_MaxVCO}$ (feedback maximum)

Once these points are defined, the switching period is calculated by a linear interpolation of the switching period to the feedback voltage, and the switching frequency curve over the whole feedback range is generated, which is naturally a non-linear function of the feedback voltage, as shown in Figure 20.

4.3.1.1 $V_{\_MinVCO}$ and $V_{\_MaxVCO}$

The minimum and maximum voltages are determined by the hardware configuration. For example, the IDP230x IO pullup voltage range is 0~3.3 V, and the ADC range is 0~2.4 V, thus the full VCO range should be within 0~2.4 V.

4.3.1.2 $f_{\_MinVCO}$ and $f_{\_MaxVCO}$

The frequency, $f_{\_MinVCO}$ is determined by the operating condition where full load is applied at minimum bus voltage during the hold-up time. Under this condition, the maximum gain is achieved at the minimum switching frequency, f_{min}. It can be derived that:

$$f_{\_MinVCO} = f_{min} = 87\ kHz$$

The maximum operation frequency $f_{\_MaxVCO}$ can possibly be seen when the maximum input voltage (threshold value of OVP1, say 420 V) is applied, and the converter is run at a no load condition ($Q = 0$), if burst mode is disabled. The gain in this condition can be given as:

$$M_{min} = \frac{V_{bus\_nom}}{V_{bus\_max}} M_{nom} = \frac{390}{420} * 0.94 = 0.87$$

From the gain equation, we get:

$$G(F,Q) = \frac{F^2(m-1)}{(F^2 m - 1)} = M_{\min}, (Q = 0)$$

The corresponding normalized frequency $F_{\max}$ can be found by:

$$F = \sqrt{\frac{M_{min}}{1 - m + mM_{min}}} = 1.41$$

Therefore, $f_{max} = F_{max} * 100 = 141$. This frequency corresponds to the actual minimum feedback voltage of 0.4 V. Given 15% deviation to accommodate the tolerance of the resonant tank and other tolerances in the circuit that will affect the voltage gain, the maximum frequency is set as:

$$f_{max} = 162\ kHz$$

With some interpolation, the frequency value at 0 V is calculated to be around 170 kHz.

4.3.1.3 $V_{\_LLVCO} : f_{\_LLVCO}$ (light load) : $V_{\_HLVCO} : f_{\_HLVCO}$ (heavy load)

These two points define the mid-frequency range of VCO, which covers the normal operation ranges from very light load to full load at nominal bus voltage.

To make the VCO slope lower and create better regulation performance, the covered voltage range should be large. For example, for 0 to 2.4 V full range, the value could be set as,

$$V_{\_LLVCO} = 0.45\ V$$
$$V_{\_HLVCO} = 2.0\ V$$

It can be seen from the voltage gain curve in Figure 18 that, when the system is working around nominal bus voltage (the resonant point), the frequency change is small while the load changes. Usually 15% deviation from the nominal point is assumed, considering the tolerances of the circuit parameters that will affect the voltage gain, i.e.

$$f_{\_LLVCO} = 1.1 f_{nom} = 121\ kHz$$
$$f_{\_HLVCO} = 0.8 f_{nom} = 88\ kHz$$

The above calculations are based on typical values of resonant components, a simplified transformer model and LLC equivalent circuit. In reality, it is difficult to build an accurate system model upon which an accurate gain/frequency curve and the consequent VCO frequency curve can be derived. Many factors come into play including:

- The tolerances of resonant tank component values will bring deviations of the switching frequency. For example, there may be 7% tolerance for the resonant inductance L_r and 3.5% for the resonant capacitance C_r.
- Additional equivalent voltage drops caused by the transformer winding and PCB traces will affect the actual voltage gain. Usually the transformer internal voltage drop is higher at heavy load than light load. As such higher equivalent conversion gain is needed at heavy load.
- The value of resonant factor m has an effect on the shape of gain curves; larger values of m result in flatter gain curves, which mean a wider operating frequency range.

Some of the factors above are difficult to quantify. So, the VCO curve can only be defined and optimized by a combination of theoretical analysis and actual measurements.

4.3.2 Current sense and OCP

The LSCS pin of IDP230x controller senses the primary side current by detecting the voltage across the sensing resistor in series with the low-side MOSFET. Typically, an RC low-pass filter is used to filter out the switching noise in the sensing signal. The RC time constant should be around 1/10 of the switching period.

There could be several overcurrent protections (OCP) for different operating conditions, such as normal operation, startup mode and burst mode. There are also OCPs with different threshold levels that trigger different subsequent actions, such as increasing switching frequency and entering into an auto-restart mode/latch mode.

The selection of current sense resistor is based upon the normal operation condition. An appropriate sensing resistor value should:

- Protect the LLC transformer from saturation and other components from over current stress.
- Avoid mis-triggering in normal operation.

The current sense and OCP tolerance calculation of the LLC is similar to the PFC as described in section 3.3.2.

Considering the parameters that affect OCP tolerance, a fast and simple way to obtain a value for the current sense resistor is:

$$R_{LLC\_CS} < \frac{V_{OCP\_LLC} * (1 - g_{error})}{I_{pk\_LLC} * g_{filter} * (1 + \Delta_{delay} + \Delta_{dynamic})} = \frac{0.4275 * 0.95}{1.13 * 0.9 * (1 + 0.2 + 0.65)} = 0.21\ \Omega$$

Where g_{error} is the OCP threshold gain error, g_{filter} is the gain of the RC filter, Δ_{delay} is the estimated error due to the external propagation delay and $\Delta_{dynamic}$ is the estimated error during dynamic operation (e.g. load jump).

4.3.3 Dead time

To identify the required dead time, two important limitations must be considered. One depends on the power MOSFET's minimum required dead time, which can easily be obtained from the datasheet, by considering MOSFET parameters such as body diode reverse recovery time, turn-on and turn-off delay times, rise, and fall times. Another is related to the minimum necessary dead time for achieving ZVS operation under even the worst-case conditions, i.e., when maximum input voltage is applied to the converter and the output voltage is adjusted to minimum value under light or no load conditions.

During the LLC converter's switching dead time, the magnetizing current charges or discharges the switching node to achieve ZVS. The relevant capacitance at the switch node is the sum of the transistor's time-related output capacitance and the value of the additional parasitic capacitance at this node. As the parasitic capacitance is difficult to estimate and usually much lower, the equivalent capacitance, denoted by C_{sw}, can be estimated as

$$C_{sw} \cong 2 * C_{o_{tr}} + C_{par} \cong 2 * C_{o_{tr}}$$

The dead time should be longer than the value calculated below to achieve ZVS across the load condition:

$$t_{dt} > \frac{V_{bus} C_{sw}}{I_{mag\_min}} = \frac{4 C_{sw} L_m}{t_{on\_min}} = \frac{4 * 72 * 10^{-12} * 847 * 10^{-6}}{\frac{1}{2 * 170 * 10^3}} = 83\ ns$$

In the above equation, the $C_{o_{tr}}$ of IPD50R1K4CE is 36 pF, the maximum frequency used for calculation is 170 kHz.

Considering the tolerance of capacitance and inductance, the dead time should be at least 100 ns.

4.3.4 LLC model and regulation loop

4.3.4.1 LLC small signal model

The normal PWM modeling technique is already mature with a state-space vector method. The pre-assumption of the state-space method is that the system resonant frequency is much lower than the switching frequency. But for resonant circuits such as LLC the pre-assumption is not valid. Hence, a new method is needed to obtain the bode plot (small signal characteristics) [5].

4.3.4.2 VCO modeling

Assume $\frac{\Delta t_{sw}}{\Delta V_{hbfb}} = \lambda$, which is the slope of the VCO, and $t_{sw} = \frac{1}{f_{sw}}$, the small signal relationship can be derived as,

$$\Delta f_{sw} = -\frac{f_{sw}}{t_{sw}} \times \Delta t_{sw} = -\frac{1}{{t_{sw}}^2} \times \Delta t_{sw}$$

$$\frac{\Delta f_{sw}}{\Delta V_{hbfb}} = -\frac{\lambda}{{t_{sw}}^2}$$

Note: Similar to the LLC transfer function, the VCO transfer function depends on the VCO steady-state switching period, t_{sw}. Usually, the VCO transfer function has a very high gain in order to cover the whole switching frequency range.

4.3.4.3 LLC regulation loop

The LLC regulation loop is based on external analog circuits and is controlled by the TL431 regulation network. The configuration is shown in Figure 21 below.

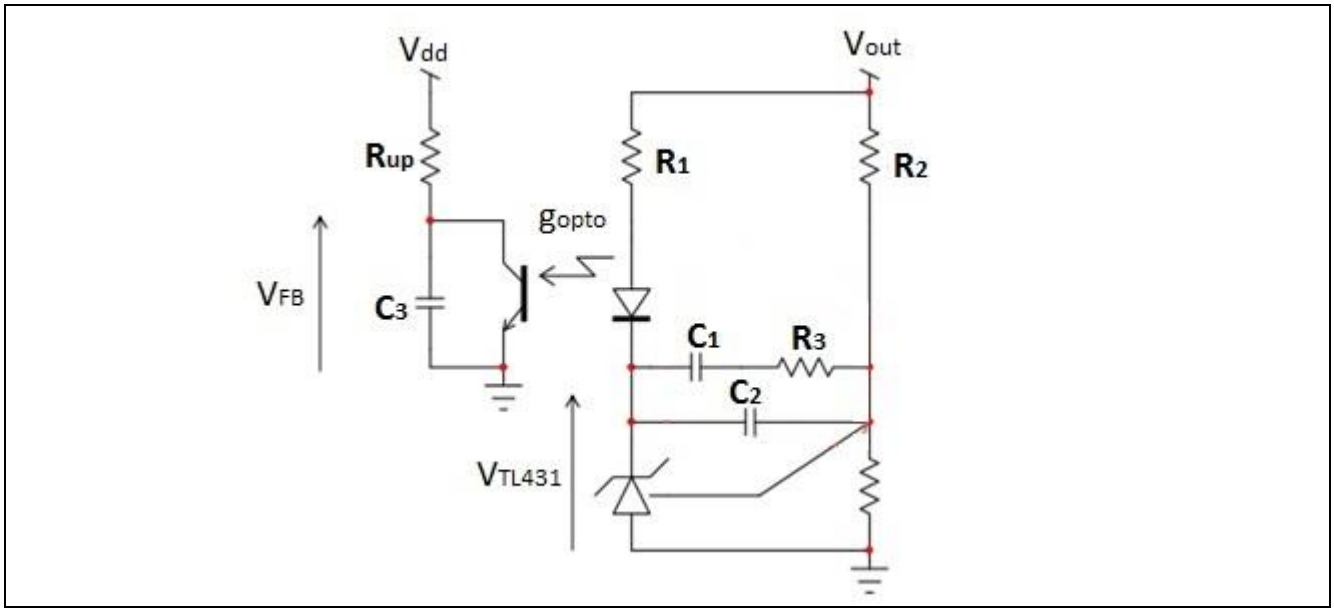

Figure 21 Analog control loop configuration

Assume the impedance of C_1, C_2 and R_3 network is Z_f. The small signal transfer function is

$$G(s) = -G_0 \frac{1 + \frac{\omega_{z1}}{s}}{1 + \frac{s}{\omega_{p1}}}$$

where

$$G_0 = \frac{R_{up}}{R_1} g_{opto}$$

$$\omega_{z1} = s\frac{Z_f}{R_2}$$

$$\omega_{p1} = \frac{1}{R_{up}C_3}$$

g_{opto} is the current transfer rate of the opto-coupler, and C_3 is the external capacitance plus the parasitic capacitance of the opto-coupler which is around 2 μF. The equivalent impedance Z_f is

$$Z_f(s) = \frac{\left(R_3 + \frac{1}{sC_1}\right) \cdot \frac{1}{sC_2}}{\left(R_3 + \frac{1}{sC_1}\right) + \frac{1}{sC_2}}$$

Substitute this into ω_{z1},

$$1+\frac{\omega_{z1}}{s}=1+\frac{Z_f(s)}{R_2}=\frac{1+s(C_1\,R_3+C_2R_2+C_1R_2)+s^2C_2C_1R_3R_2}{sR_2(C_1+C_2)\left(1+s\frac{R_2R_3C_1C_2}{R_2(C_1C_2)}\right)}$$
$$=\frac{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2}{\frac{s}{\omega_{po}}\left(1+\frac{s}{\omega_{p2}}\right)}$$

where,

$\omega_0=1/\sqrt{C_1C_2R_2R_2}, Q=\frac{1}{\omega_0(R_2(C_1+C_2)+C_1R_3)}, \omega_{po}=\frac{1}{R_2(C_1+C_2)}, \omega_{p2}=\frac{C_1+C_2}{R_3C_1C_2}$

The complete transfer function is

$$V_{FB}(s)=-G_0\frac{1+\frac{\omega_{z1}}{s}}{1+\frac{s}{\omega_{p1}}}=-G_0\frac{1+\frac{s}{\omega_0 Q}+\left(\frac{s}{\omega_0}\right)^2}{\frac{s}{\omega_{po}}\left(1+\frac{s}{\omega_{p2}}\right)}\frac{1}{1+\frac{s}{\omega_{p1}}}$$

There are 2 zeros, 2 poles and an origin pole; some of which are coupled to each other. The resistance and capacitance are also limited by the physical circuit constraints. So, it is not easy to design the network using the pole-zero placement method. Usually, ω_{po} is determined first by the gain requirement, then ω_{p1} and ω_{p2} are set. The Bode plot can then be deduced from above transfer function.

5 General features and system design considerations

5.1 VCC supply and high voltage startup cell

5.1.1 Start up

HV pin is connected to the AC input voltage via a resistor and two diodes. There are two main functions supported at HV pin: VCC startup and direct AC detection.

The integrated HV startup-cell is switched on during the VCC startup phase, when the IC is inactive. A current is flowing from pin HV to pin VCC via an internal diode, which charges the capacitor at pin VCC. Once the voltage at pin VCC exceeds the VCC_ON threshold, the active operating phase is entered.

As illustrated in Figure 22, the integrated HV startup-cell (depletion MOS, normally on device) is switched on during the VCC startup phase, when the IC is inactive. A current flows from the HV pin to the VCC pin via an internal diode, which charges the capacitor at the VCC pin. Once the voltage at the VCC pin exceeds the UVLO on-threshold VCC_ON (OVLO level), then the IC becomes active.

VCC will drop until the self-supply via the auxiliary winding of the LLC takes over the supply at the VCC pin during the active operating phase of the converter. The self-supply via the auxiliary winding must therefore be in place before VCC undershoots the VCC_OFF threshold.

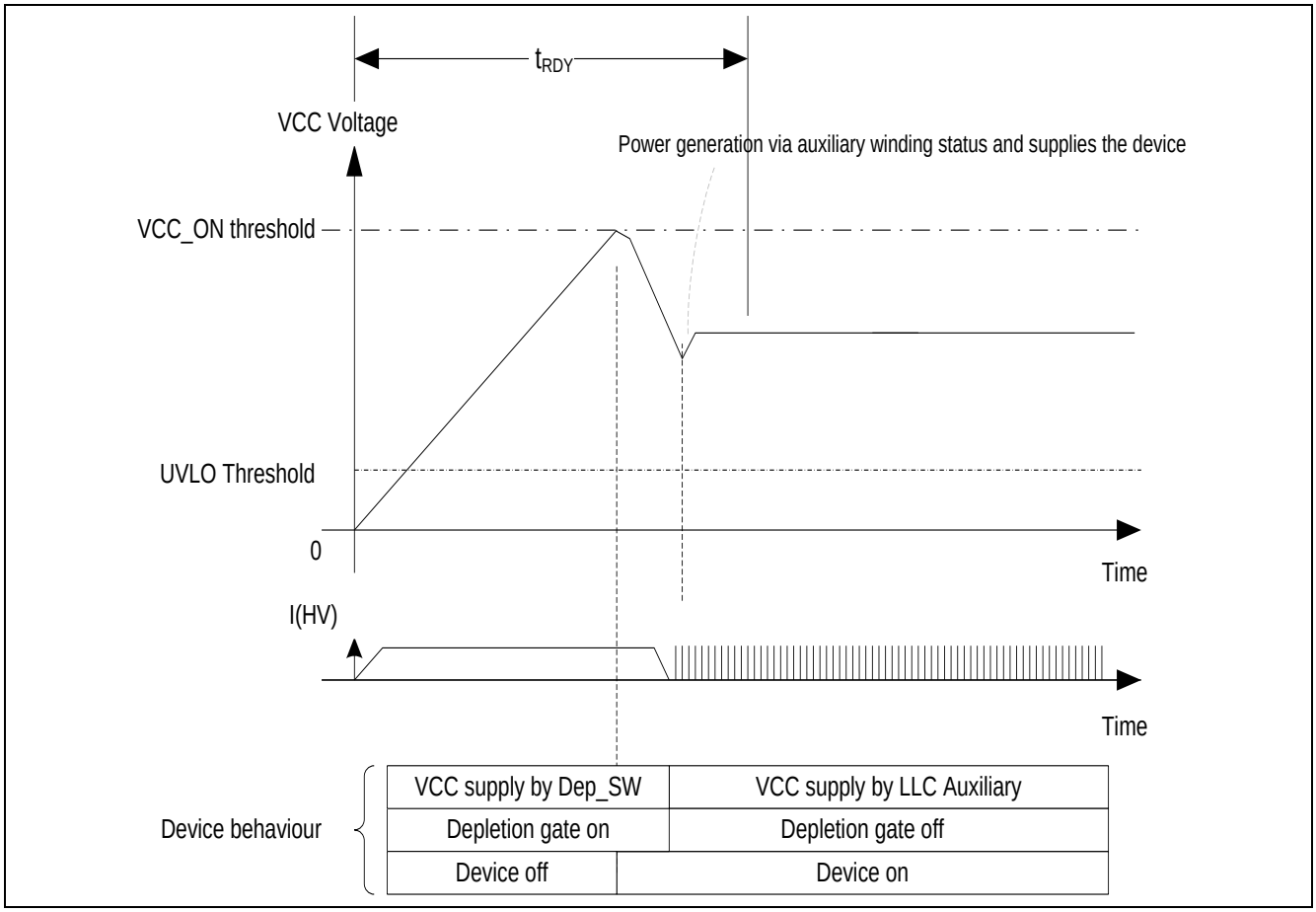

Figure 22 VCC voltage illustration of direct AC input powering up behavior

5.1.2 Selection of VCC capacitor

According to the start-up procedure described above, when setting the value of the VCC capacitor, the following conditions must be considered:

- The requirement for the start-up time of the IC ($t_{startup}$<1 second) is determined by the customer. With the same charging current, a larger capacitor value gives a longer start up time, and vice-versa.
- After the VCC voltage reaches VCC_ON, the energy stored in the VCC capacitor should be enough to supply the IC after it becomes active and before the LLC starts to supply the VCC voltage.

To meet the first criteria,

$$C_{VCC} < \frac{I_{HV} * t_{startup}}{V_{cc\_on}} = \frac{\frac{V_{90\_avg}}{R_{total}} * 1}{20.5} = \frac{\frac{90 * \frac{2\sqrt{2}}{\pi}}{51.7} * 1}{20.5} = \frac{1.57\ mA * 1s}{20.5V} = 76\ \mu F$$

$$R_{total} = R_{ext} + R_{int} = 51 + 0.7 = 51.7\ k\Omega$$

The value of VCC_ON can be found in the datasheet.

R_{int} is the effective resistance considering the IC internal current consumption.

To meet the second criteria,

$$C_{VCC} > \frac{I_{total*}t}{VCC\_ON - VCC\_OFF} = \frac{22.94\ mA * 20\ ms}{(20.5 - 7.5)V} = 35\ uF$$

$$I_{total} = I_{active} + I_{VDDP} - I_{HV} = 22.5 + 2 - 1.56 = 22.94\ mA$$

The value of I_{active}, I_{VDDP} and VCC_OFF can be found in the datasheet.

Combining the results above,

$$35\ \mu F < C_{VCC} < 76\ \mu F$$

5.1.3 VCC supply circuit linear regulator

It is recommended to regulate the voltage supplied to the VCC pin to not be higher than 15 V, so as to reduce the power consumed by the IC and avoid over temperature protection being triggered. A reference circuit using a linear regulator in the VCC supply circuit is shown below.

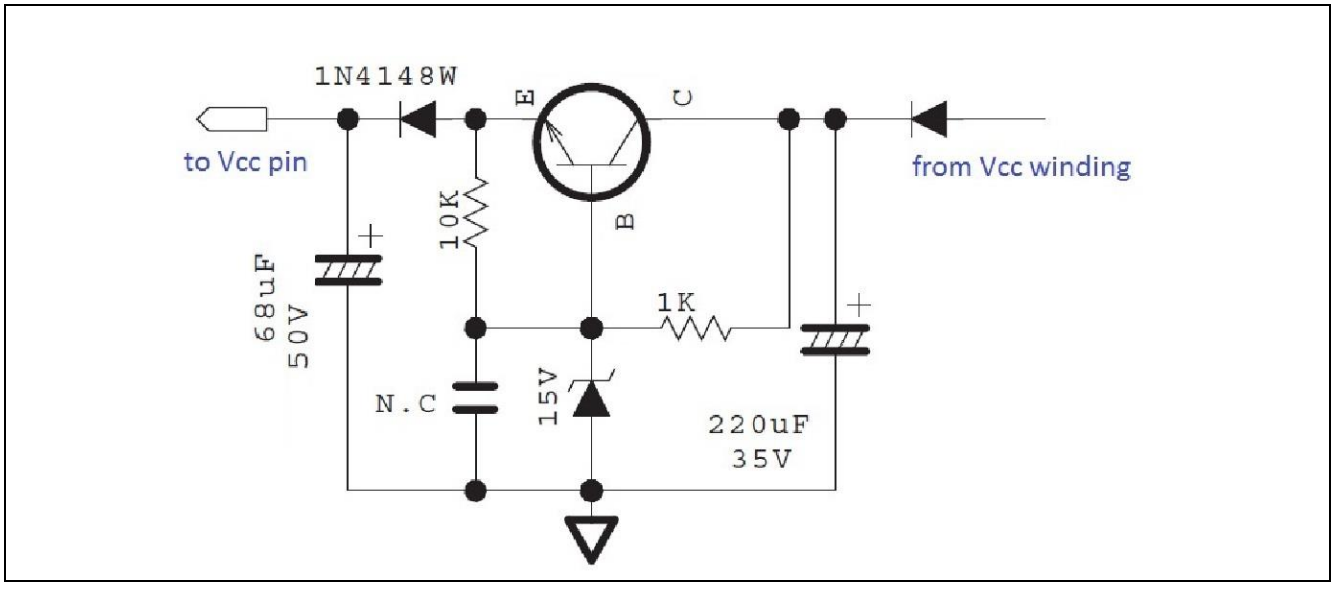

Figure 23 Linear regulator in the VCC supply circuit

5.2 LLC High-side VCC (HSVCC) cap

To optimize LLC switching behaviour during start-up and burst mode operation, HSVCC cap is targeted to reach its turn-on threshold within the first low-side gate pulse. Thus, its capacitance can be calculated as:

$$C_{HSVCC} < -\frac{t}{\ln\left(1-\frac{V_{HSVCC\_on}}{V_{cc}-V_D}\right) * R_{HSVCC}}$$

Considering LLC softstart frequency as 270kHz with 500ns dead time, and HSVCC on threshold V_{HSVCC_on} as 9.7V, V_{cc} as 15V, V_D as 0.7V and R_{HSVCC} as 10Ω, thus the HSVCC cap C_{HSVCC} can be calculated as :

$$C_{HSVCC} < 119nF$$

So in the design, a 100nF cap is recommended.

5.3 Touch current

There is an industrial standard for touch voltage/current that has to be met by the power supply. For example, IEC60065 specifies the limit for Class II equipment as 0.35 V/0.70 mA peak. In tropical climates the values given have to be halved so the limit becomes 0.175 V/0.35 mA peak.

Usually the challenge comes from standby (burst mode) operation: when the AC voltage is high (e.g. near the AC peak), the voltage across the Y-capacitor (between primary ground & secondary ground) is charged to a high value during burst-on. During burst-off, the voltage across the Y-capacitor is maintained and the energy remains as there is no discharge path. When the next burst-on or AC detection via the HV pin occurs, the AC voltage may be at a much lower value, then the Y-capacitor will be discharged through all possible discharge paths and thus causes spikes in the touch current. This spike current may exceed the 0.35 mA limit as defined by IEC60065.

During normal operation, the voltage across the Y-capacitor will follow the AC voltage through the cycle, and no touch current spike will occur.

The following are some design considerations in order to meet the touch current:

- Use a relatively small Y-capacitor between primary ground and secondary ground, so that the energy stored in is relatively small. The value is selected based on the tradeoff between the EMI/lightning surge requirement (where a bigger capacitor is preferred) and the touch current requirement.
- Add discharging resistor in parallel with the Y-capacitor. The value is selected based on the tradeoff between the standby power losses and the discharge speed, thus a 1~3 MΩ resistor value might be appropriate.
- Add a resistor (1~3 mΩ) and/or high-voltage capacitors (around 1 nF) in parallel with the bridge diodes to provide an alternative discharge path.
- Add a resistor (1~3 mΩ) from HV to the primary-side GND to provide an alternative discharge path.

5.4 Black box

The black box function is responsible for sending diagnostic data through the UART (MCOM) pin to a host MCU or for probing directly at the pin.

The UART (MCOM) pin will be configured as a digital output pin after protection is triggered, and will output the relevant diagnostic data digitally.

If the UART (MCOM) voltage is at a high level, it is counted as “1”; if at a low level, “0”. The duration of each bit is 36 us. This may vary with different firmware settings.

The start of the frame is 0xFF. After one bit of “0”, the following first byte can be read, which indicates the state of the gearbox (usually protection information).

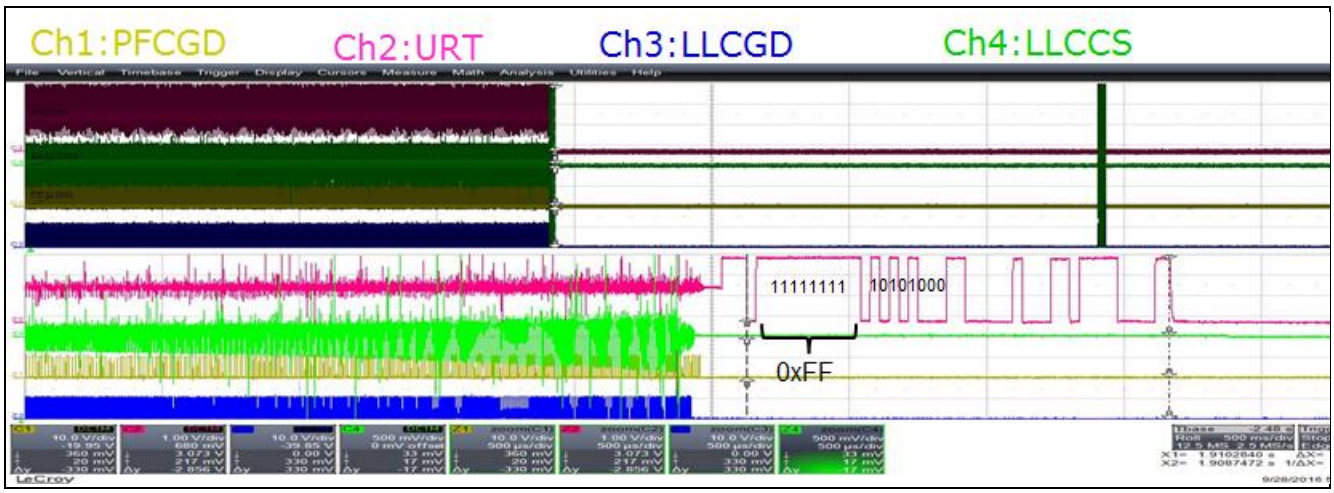

Figure 24 Example of black box function: OCP1

As an example, the digital information in Figure 25 can be read out in sequence as “10101000”. It should then be reversed to obtain the correct binary code “00010101”, and then be converted to Hexadecimal code “0x15”. With this hexadecimal code, we look up in the code in Figure 26 to obtain the information that OCP1 is triggered.

```
 GB_STATE_IDLE                                = 0x00,     /**< GB stays idle */
    GB_STATE_PFC_START                        = 0x01,     /**< GB starts the PFC. */
    GB_STATE_LLC_START                        = 0x02,     /**< GB starts the LLC. */
    GB_STATE_STEADY_OPERATION                 = 0x03,     /**< GB is in steady state operation, both PFC and LLC are
operating in their respective states. */
    GB_STATE_BURST_BREAK                      = 0x04,     /**< GB in standby burst off state. */
    GB_STATE_BURST_ACTIVE                     = 0x05,     /**< GB in standby burst on state. */
    GB_STATE_PROTECTION_AUTORECOVERY          = 0x06,     /**< GB keeps LLC running. This state is used to implement
common code while system is in a protection state with auto-recovery (neither auto-restart break time nor latch). */
    GB_STATE_PROTECTION_ACTIVE_AUTORESTART    = 0x07,     /**< GB is in active autorestart state. This state is used to
implement common code before entering the actual protection state. */
    GB_STATE_PROTECTION_PASSIVE_AUTORESTART   = 0x08,     /**< GB is in passive autorestart state. This state is used to
implement common code before entering the actual protection state. */
    GB_STATE_LLC_START_STANDALONE             = 0x09,     /**< GB starts LLC in standalone mode (without PFC). */
    GB_STATE_PFC_PROTECTION_BUS_OVP1          = 0x0a,     /**< GB in PFC bus overvoltage 1 state. */
    GB_STATE_PFC_PROTECTION_BUS_OVP2          = 0x0b,     /**< GB in PFC bus overvoltage 2 state. */
    GB_STATE_PFC_PROTECTION_CCMP              = 0x0c,     /**< GB in PFC continuous-conduction mode protection state. */
    GB_STATE_PFC_PROTECTION_OLP               = 0x0d,     /**< GB in PFC open loop state. */
    GB_STATE_PFC_PROTECTION_VSOPEN            = 0x0e,     /**< GB in PFC pin VSENSE open protection state. */
    GB_STATE_PFC_PROTECTION_SHORT_VS2ZCD      = 0x0f,     /**< GB in PFC pin short VS2ZCD protection state. */
    GB_STATE_PFC_PROTECTION_UVP               = 0x10,     /**< GB in PFC undervoltage state. */
    GB_STATE_LLC_PROTECTION_TCO_FAILURE       = 0x11,     /**< GB in LLC TCO-to-VCO handover failure state. */
    GB_STATE_LLC_PROTECTION_CMP               = 0x12,     /**< GB in LLC capacitive mode protection state. */
    GB_STATE_LLC_PROTECTION_OLP               = 0x13,     /**< GB in LLC open-loop/overload protection state. */
    GB_STATE_LLC_PROTECTION_OLP_STARTUP       = 0x14,     /**< GB in LLC open-loop/overload protection at startup state.
*/
    GB_STATE_LLC_PROTECTION_OCP1              = 0x15,     /**< GB in LLC over-current 1 protection state. */
    GB_STATE_LLC_PROTECTION_OCP2              = 0x16,     /**< GB in LLC over-current 2 protection state. */
    GB_STATE_PROTECTION_OVER_TEMPERATURE      = 0x17,     /**< GB in over temperature protection state. */
    GB_STATE_PROTECTION_VCC_OVER_VOLTAGE      = 0x18,     /**< GB in VCC over voltage protection state. */
    GB_STATE_PROTECTION_AC_BROWN_OUT          = 0x19,     /**< GB in brown out protection state. */
    GB_STATE_PROTECTION_XCAP_DISCHARGE_ACTIVE_MODE  = 0x1a,     /**< GB in AC unplugged protection state in active mode. */
    GB_STATE_PROTECTION_XCAP_DISCHARGE_STDBY_MODE   = 0x1b,     /**< GB in AC unplugged protection state in standby mode. */
    GB_STATE_RESUME_FROM_OVERTEMP_PROTECTION  = 0x1c,     /**< GB in resumes from overtemperature protection state. */
    GB_STATE_STOPPED                          = 0x1d,     /**< GB shuts down system. */
    GB_STATE_PFC_PROTECTION_VSOPEN_STOPPED    = 0x1e,     /**< GB shuts down system in idle state due to VSOPEN  */
```

Figure 25 Firmware code in gb.h

6 Tips on PCB layout

Infineon's digital platform controller IC integrates the PFC and LLC converter controllers in one package. Therefore, it is a good idea to physically separate the PFC and LLC circuits on the PCB to avoid mutual interference.

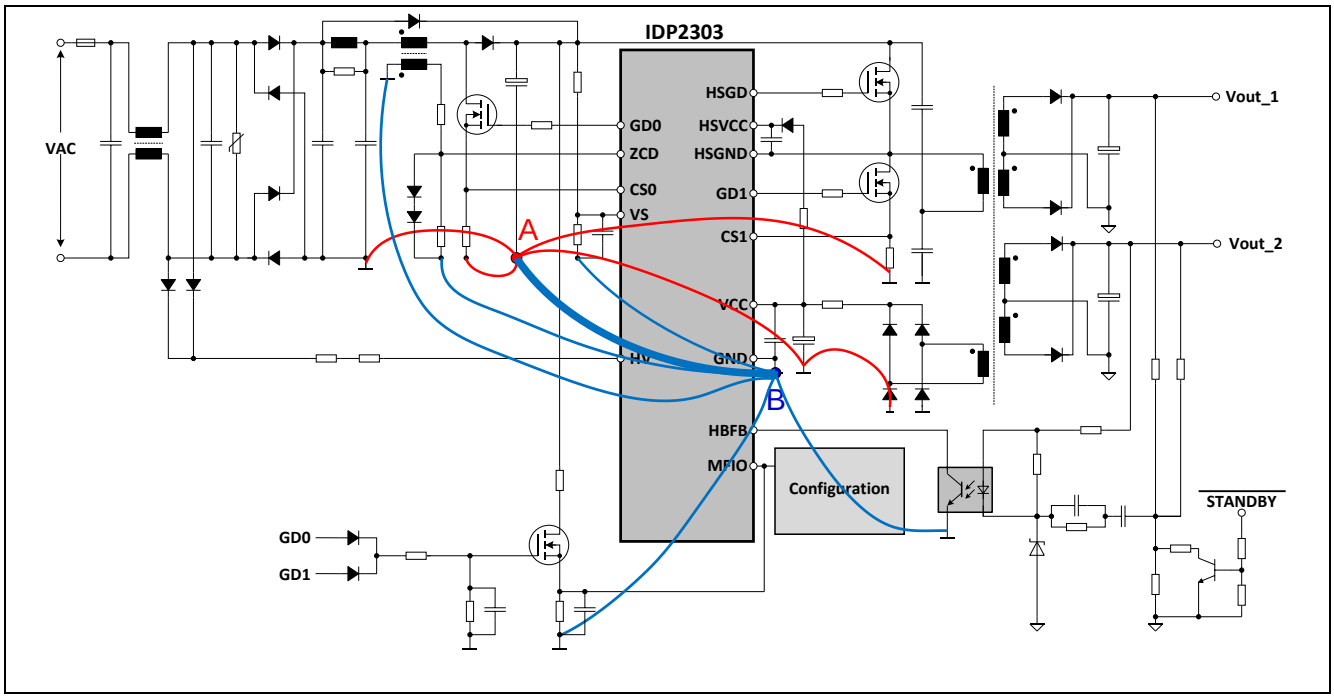

Figure 26 Star connection of grounding

6.1 Star connection of grounding

“Star connection” of grounding (illustrated in Figure 26) is a proven and effective way to minimize the risk of mutual interference among signals.

- The PFC bulk capacitor ground (red point A) is taken as the system ground reference at the primary side. The other power ground should have direct connections to this system ground reference point, shown as red lines.
- The IC Signal GND, VCC GND, current sense GND, MOSFET/diode heatsink and EMI return GND, shall all be “star” connected to the PFC bulk capacitor ground directly and the PCB traces should be as short as possible.
- The second ground reference is the ground of the IDP230x IC VCC capacitor (blue point B), which should be mounted very close to the IC ground. All ground connections of small signals around the controller IC are connected to the IC VCC ground point, shown as thin blue lines.
- The IC ground is connected to the PFC bulk Capacitor ground, shown as a thick blue line.
- The PCB ground traces for HBFB, PFCZCD and PFCVS signal are strongly recommended to be separately connected to the second ground reference, to avoid interference.
- In addition, in order to minimize the impedance of the ground PCB trace, it is strongly recommended that the ground connection PCB traces are as short and thick as possible.

6.2 Filtering capacitors

Filtering capacitors are often used to suppress the high frequency noise. These filtering capacitors, such as the capacitors for VCC (recommended value 100 nF), PFCVS pin (recommended value 1 nF), LSCS pin

(recommended value 1 nF) and HBFB pin (recommended value 4.7 nF) shall be mounted as close as possible to the controller IC, while their ground shall be connected to the IC ground directly. All these connection traces shall be as short as possible.

An optional 10~47 nF high frequency and high voltage bypass capacitor is recommended to be mounted in parallel with the PFC bulk capacitor, close to the PFC MOSFET and PFC diode, to suppress EMI.

An optional 10~100 nF high frequency and high voltage decoupling capacitor is recommended to be mounted between the LLC high side MOSFET drain and low side MOSFET source pin, to reduce the HF ripple and improve EMI behavior.

6.3 PFC ZCD signal detection circuit

A separate PCB trace is recommended to be used from the ground terminal of the PFC choke auxiliary winding to the IC GND as shown in Figure 27.

Another separate PCB trace is needed from the PFC choke auxiliary winding to the PFC ZCD sensing resistors R_zcd_h and R_zcd_l. Both resistors and clamping diodes shall be mounted close to the PFC ZCD pin and IC GND pin. This trace shall be kept far away from the LLC high side driver circuit, including the high side GND pin, to avoid high dv/dt coupling.

The two PCB traces from the PFC choke auxiliary winding shall be parallel and close to each other.

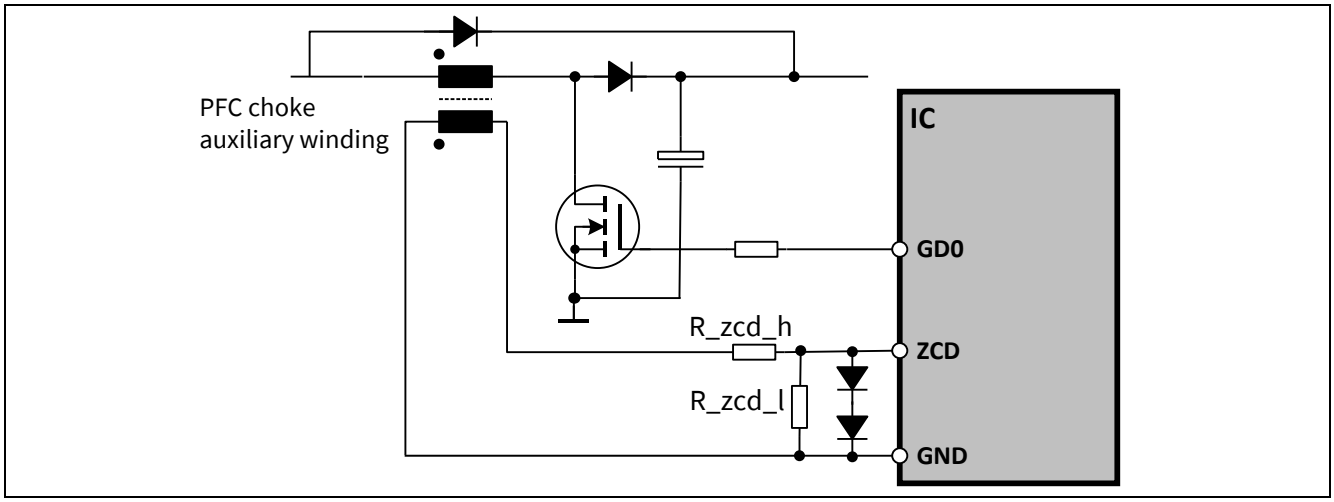

Figure 27 PFC ZCD signal detection circuit

6.4 HBFB voltage detection circuit

The two PCB traces from the opto-coupler to the HBFB pin and IC GND shall be parallel and close to each other.

The HBFB pin filtering capacitor shall be mounted close to HBFB and the GND pin. The loop area between the HBFB pin and opto-coupler shall be as small as possible. The PCB traces from the opto-coupler shall be kept far from other PCB tracks that carry switching current. Alternatively, a separate GND trace can be added to shield the HBFB pin signal. The two PCB traces from the opto-coupler shall be kept away from the LLC high side driver circuit, including the high side GND pin, to avoid high dv/dt coupling.

6.5 LLC high side bootstrap circuit

As the IDP230x HSVCC, HSGD and HSGND pins can see high voltage and high dv/dt, switching noise may be coupled to low voltage pins/traces through stray capacitance. Thus, the PCB traces and components connected to these pins need to be kept away from other low voltage pins/traces.

For example, the PFC ZCD and HBFB pin related PCB tracks shall be far away from these high voltage and high dv/dt pins.

6.6 Minimum current flowing loop area

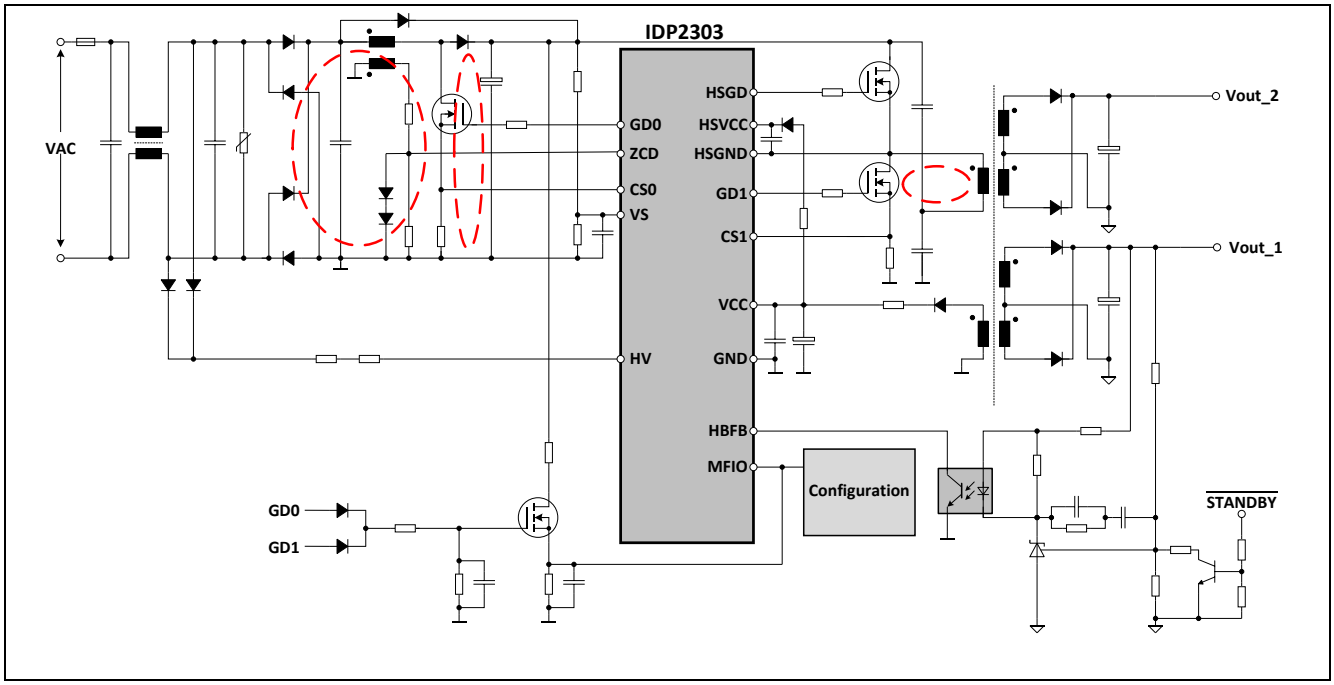

Figure 28 Main current loop

The main current loop areas (as shown in Figure 28) for PFC and LLC stages shall be minimized to be as small as possible, so that the radiated EMI noise can be effectively reduced.

6.7 Passing 4 kV lightning surge test

To pass the 4 kV lightning surge test, PCB spark gaps or spark gap devices across the input common mode choke are required to be added.

A PCB spark gap is a pair of saw-tooth like copper plates (circled red in Figure 29) facing each other that can discharge the accumulated charges during a surge test through the sharp saw-tooth points. The distance between the sharp tooth points should be 0.8 mm or less. The PCB spark gap can be replaced by two spark gap devices SP1 and SP2 (e.g. DSP-301N-S00B) as in Figure 29, such that it is placed in parallel to each winding of the input common mode choke.

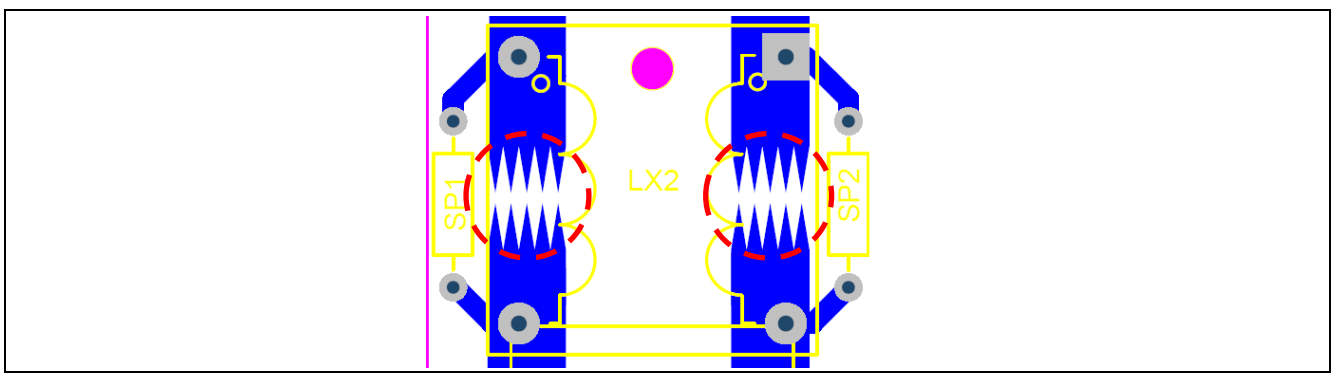

Figure 29 Spark gaps for lightning surge test

In addition, a ferrite bead (shown red in Figure 31) can be added between the bus track and the upper resistor in the bus voltage divider.

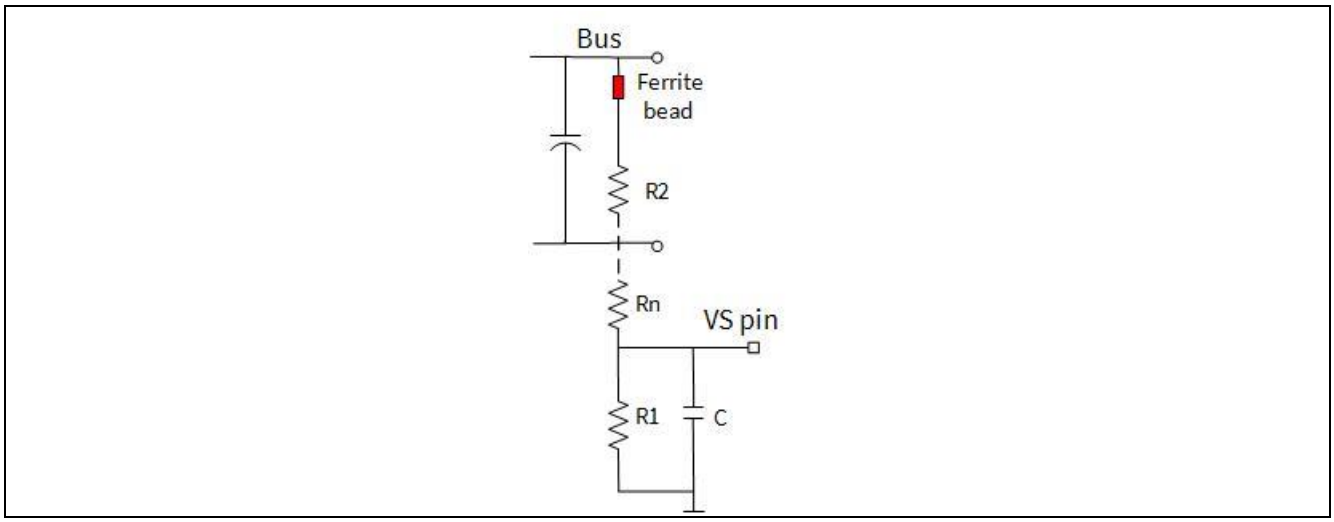

Figure 30 Ferrite bead for lightning surge test

6.8 Other considerations

To avoid possible mutual interference, the HBFB and PFC ZCD signal related PCB traces shall not be close or in parallel to the HV pin related PCB traces and LLC main current loop.

Any PCB track carrying a high current should be designed to be as short and wide as possible to reduce the parasitic inductance. For example, the PCB track along PFC MOSFET source, the shunt resistor and PFC bulk cap. GND shall be designed to be short and wide.

With a double layer PCB, assigning one layer as a GND plane will help to increase the power supply board's immunity to noise.

7 Usage of dpVision

7.1 Installation of dpVision

Customers are able to install the user interface - dpVision - on their own computer, following these installation instructions.

1) Install the latest dpVision_2.0.8.0 from the folder (double click dpVision_2.0.8.0.msi)
2) Unzip the IDP230x_addon_generator.zip file and install add ons folders, by double clicking on IDP230x_addon_generator.msi file.
3) Step 2 above will copy and paste, documents, images & parameters to C:\Users\<Login>\Infineon Technologies AG\.dp vision
4) Connect the **dpIFGen2** interface board using the USB cable provided to a laptop USB port and open the dpVision GUI by double clicking on “dpVision.exe” or using the icon below

Figure 31 .dpVision icon

5) Update the **dpIFGen2** interface board firmware (go to the "Tools" menu bar, click on dpIFGen2 FW update, read the current version and browse for the latest FW version “dpIfGen2_Rev2-4-0.hex “. Click 'Start')

Figure 32 Menu bar

6) Connect the IFX IDP230x sample to the **dpIFGen2** interface board using VCC, UART and GND pins,

Figure 33 dplFGen2 interface board (side view)

7) Open“idp230x_configuration_dpVision2.0.8.0_dpIfGen2FW240_appFwV0322_Rev_0.8_embedded_hisense.csv” using menu → File → Open browse to folder →\.....\.dpVision\Parameters

8) Press the “Power Device On/Off” button → “Device status” should turn green

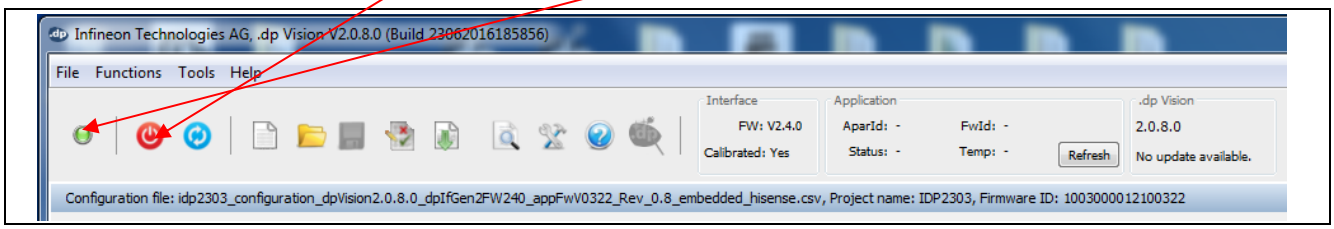

Figure 34 Power device On/Off button and device status

9) Press the “Test configuration set” button so that parameter values are loaded into the IDP230x sample and application firmware starts running.

10) Change the parameters using the “Value” field

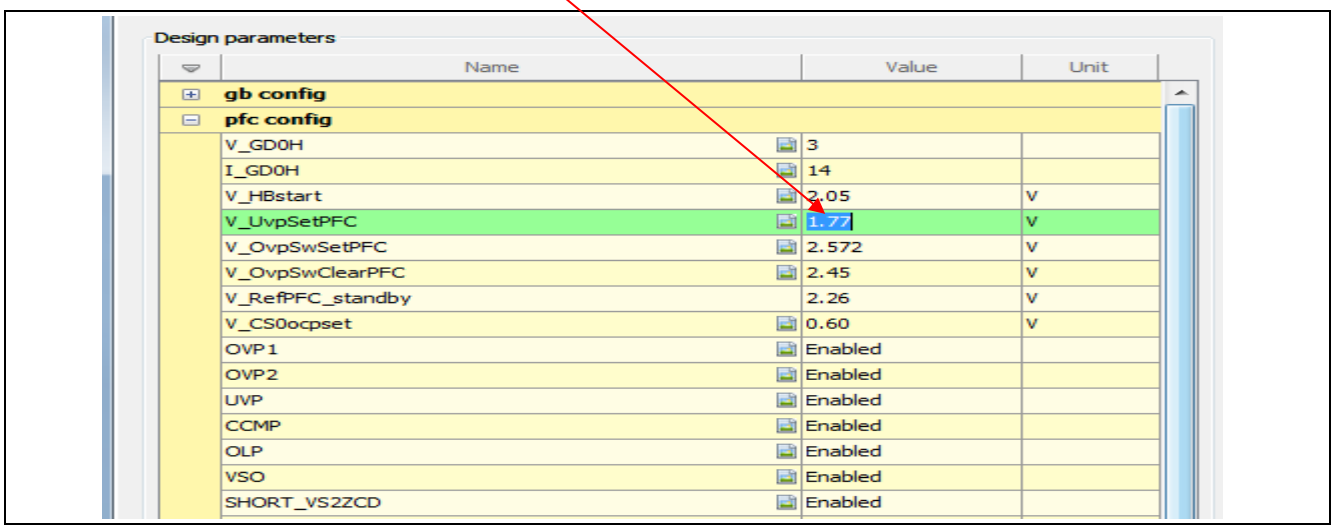

Figure 35 Value field

11) Changing the parameter will activate the “Save configuration set” button. Save the configuration and again press the “Power on /off” button and click on “Test configuration set” will load the new configuration set into the chip

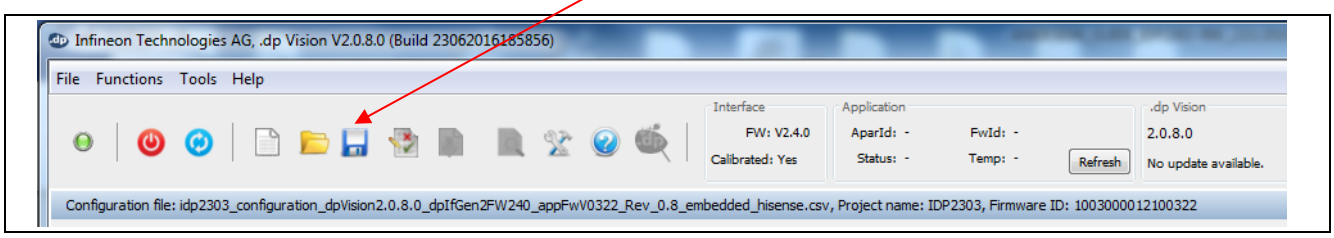

Figure 36 Save configuration set button

13) For the setting of parameters with dpVision, please press “Help” for the dpVision user manual.

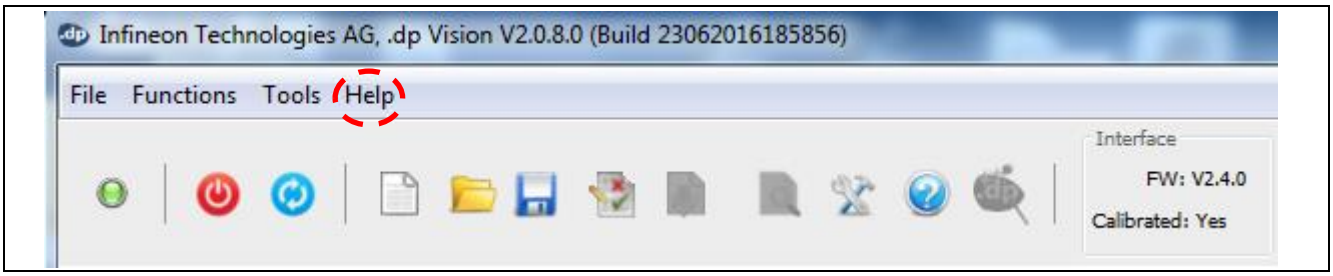

Figure 37 Help button

7.2 Parameter setting with dpVision

Table 8-10 list up all the configurable parameters by customers through dpVision. The setting of the major parameters has been explained in detail in this design guide. The description of each parameter together with explanatory image will be displayed with a click on each parameter name. In addition, a user manual can be obtained by pressing “Help” button.

Table 7 General parameters

Parameter symbol	Parameter description	Pin	Default	Range	Unit
$V_{\_HVBID}$	AC brownin	HV	70	1 ~ 255	V_{ac}
$V_{\_HVBOD}$	AC brownout	HV	60	1 ~ 255	V_{ac}
$t_{\_AR}$	Auto restart break time	-	2		s
$t_{\_VCCOVP}$	VCC OVP blanking time	-	9		ms

Table 8 PFC parameters

Parameter symbol	Parameter description	Pin	Default	Range	Unit
$V_{\_GD0H}$ [1]	PFC GD0 drive voltage	GD0	10.5	4.5 ~ 15	V
$I_{\_GD0H}$ [1]	PFC GD0 drive current	GD0	0.156	0.087 ~ 0.36	A
$V_{\_UvpSetPFC}$	PFC bus under voltage	VS	1.77	0.1 ~ 2.3	V
$V_{\_RefPFC\_burst}$	PFC control_burst	VS	2.2	0.1 ~ 2.3	V
$V_{\_HBstrt}$	LLC enter soft start	VS	2.05	0.1 ~ 2.3	V
$t_{\_UvpBlkPFC}$	PFC blanking time for bus under voltage	VS	3	0.128 ~ 8388	ms
$t_{\_ovc}$	PFC over voltage comparator filter time	VS	10000	0 ~ 31500	ns
$V_{\_OvpSwSetPFC}$	PFC bus over voltage	VS	2.572	2 ~ 2.8	V
$V_{\_OvpSwClearPFC}$	PFC bus over voltage clear	VS	2.45	2 ~ 2.8	V
$V_{\_CS0ocpSet}$ [1]	PFC over current	CS0	0.6	0.05 ~ 1.15	V
$f_{\_sw\_max\_pfc}$	PFC max switching frequency	-	120	1 ~ 300	kHz
$f_{\_sw\_min\_pfc}$	PFC min switching frequency	-	60	1 ~ 300	kHz
$svp_{\_startup}$	PFC PIT1 P-coe during startup	-	4	0 ~ 7	-
svp	PFC PIT1 P-coe	-	6	0 ~ 7	-
svi	PFC PIT1 I-coe	-	7	0 ~ 7	-
svt	PFC PIT1 T-coe	-	4	0 ~ 7	-
$t_{\_OnMinPFC}$	PFC min on time	-	0.1	0.016 ~ 63.98	µs

Parameter symbol	Parameter description	Pin	Default	Range	Unit
$t_{\_OnMaxPFC}$	PFC max on time	-	20	0.016 ~ 63.98	µs

[1] Refer to 5.4.6 for limits

Table 9 LLC Parameters

Parameter symbol	Parameter description	Pin	Default	Range	Unit
$V_{\_GD1H}$ [1]	LLC GD1 drive voltage	GD1	10.5	4.5 ~ 15	V
$I_{\_GD1H}$ [1]	LLC GD1 drive current	GD1	0.12	0.026 ~ 0.12	A
$V_{\_Ocp1\_norm}$ [1]	LLC OCP1 during steady state	CS1	0.4275	0.05 ~ 1.15	V
$V_{\_Ocp1\_start}$ [1]	LLC OCP1 during softstart	CS1	0.55	0.05 ~ 1.15	V
$V_{\_Ocp1\_burst}$ [1]	LLC OCP1 when leaving burst mode	CS1	0.75	0.05 ~ 1.15	V
$N_{\_Ocp1\_max}$	LLC max number of OCP1 events	CS1	8	1 ~ 255	-
$f_{\_Ocp1}$	LLC switching frequency during OCP1	CS1	200	100 ~ 600	kHz
$V_{\_burst\_enter}$	LLC HBFB voltage when entering a burst mode	HBFB	0.3	0.1 ~ 2.3	V
$V_{\_burst\_exit}$	LLC HBFB voltage when exiting burst mode	HBFB	2.05	0.1 ~ 2.3	V
$V_{\_OlpHB}$	LLC open-loop / overload protection	HBFB	2	0.1 ~ 2.3	V
$V_{\_HLVCO}$	LLC VCO heavy load voltage	HBFB	2	0.1 ~ 2.3	V
$V_{\_LLVCO}$	LLC VCO light load voltage	HBFB	0.45	0.1 ~ 2.3	V
$f_{\_MaxVCO}$	LLC VCO max frequency	-	250	1 ~ 300	kHz
$f_{\_LLVCO}$	LLC VCO light load frequency	-	140	1 ~ 300	kHz
$f_{\_NomVCO}$	LLC nominal operating frequency	-	100	1 ~ 300	kHz
$f_{\_HLVCO}$	LLC VCO heavy load frequency	-	85	1 ~ 300	kHz
$f_{\_MinVCO}$	LLC VCO minimal frequency	-	82	1 ~ 300	kHz
$f_{\_sw\_burst\_start}$	LLC starting frequency in burst mode	-	200	100 ~ 300	kHz
$f_{\_sw\_burst\_stop}$	LLC ending frequency in burst mode	-	200	100 ~ 300	kHz
$f_{\_sw\_burst}$	LLC switching frequency during burst mode	-	130	50 ~ 200	kHz
$f_{\_MaxTCO}$	LLC max. soft start frequency	-	270	100 ~ 300	kHz
$t_{\_Ocp1\_blk\_startup}$	LLC OCP1 blanking time from startup threshold to low threshold during startup	-	200	0.032 ~ 2097	ms
$t_{\_Ocp1\_release}$	LLC releasing OCP1 lapse time	CS1	100	0.032 ~ 2097	ms
$t_{\_Ocp1\_filter}$	LLC blanking filter time CS1 OCP1	CS1	0	0 ~ 984	ns
$t_{\_blk\_Ocp2}$	LLC blanking time for OCP2	CS1	0	0 ~ 984	ns
$t_{\_dead\_llc}$	LLC dead time	-	0.5	0.0157 ~ 0.984	µs
$t_{\_OlpHB}$	LLC blanking time before open-loop / overload protection	-	100	0.032 ~ 2097	ms
$t_{\_blk\_burst}$	Blanking time to enter burst mode	-	20	0.032 ~ 2097	ms

Parameter symbol	Parameter description	Pin	Default	Range	Unit
$Slope_{\_TCO\_init}$	LLC initial slope during soft start	-	0.85	0.0157 ~ 3.984	µs/0.5 ms
$Slope_{\_TCO\_min}$	LLC min slope during soft start	-	0.36	0.0157 ~ 3.984	µs/0.5 ms
$N_{\_burst\_sstart}$	LLC soft start steps	-	4	1 ~ 218	-
$N_{\_burst\_sstop}$	LLC soft stop steps	-	4	1 ~ 218	-
$T_{\_burst\_on\_max}$		-	160		us
$Slope_{\_burst\_leave}$	LLC slope of soft start when leaving burst mode	HBFB	0.32	0.0157 ~ 3.984	µs/0.5 ms
High_limit Burst_off_time	High limit of burst off time for adaptive minimum frequency during burst on	-	120	20 ~ 200	ms

[1] Refer to 5.4.6 for limits

8 References

[1] Infineon technologies: IDP2303 Digital Multi-Mode PFC + LLC combo controller, Datasheet Rev. V1.0, 2016-11-21

[2] Infineon technologies: IDP2303A Digital Multi-Mode PFC + LLC combo controller, Datasheet Rev. V1.0, 2016-11-21

[3] Infineon Technologies: CrCM Boost PFC Converter Design, Design Note, DN 2013-10 V1.0 January 2013.

[4] Infineon Technologies: Primary Side MOSFET Selection for LLC Topology, Application note, V1.0, June 2014.

[5] S.De Simone: 'Design-oriented steady state analysis of LLC resonant converters based on FHA', SPEEDAM 2006.

[6] Infineon technologies: IDP2308 Digital Multi-Mode PFC + LLC combo controller, Datasheet Rev. V2.0, 2017-7-20

Revision history

Major changes since the last revision

Page or reference	Description of change
12	PFCVS voltage devider design
15	PFC ZCD divider design
38	LLC High-side VCC (HSVCC) cap design
	Add IDP2308

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Edition 2019-04-09

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
DG_201702_PL21_007

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