Date: June 4, 2015

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-R8C-A056B/E	Rev.	2.00
Title	Corrections of the descriptions in the User's Manual		Information Category	Technical Notification		
Applicable Products	See below	Lot No. –	Reference Document			

This document describes corrections of the descriptions in the User's Manual: Hardware for the products listed in the tables in the Applicable Products. If the description to be corrected appears in the User's Manual on pages other than pages listed in this document, the same correction will also apply to the descriptions on those pages.

1-1. Applicable Products

Product	User's Manual	Target Page
R8C/LA3A Group	R01UH0024EJ0100 (Rev.1.00)	Page 320 of 581

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

1-2. Descriptions to Be Corrected

20.2 Registers

20.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Timer RH standby bit	0: Active 1: Standby (3)	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (4)	R/W
b4	MSTTRJ1	Timer RJ1 standby bit (6)	0: Active 1: Standby (5)	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRH bit is set to 1 (standby), any access to the timer RH associated registers (addresses 0110h to 011Fh) is disabled.
4. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.
5. When the MSTTRJ1 bit is set to 1 (standby), any access to the timer RJ1 associated registers (addresses 0088h to 008Eh) is disabled.
6. In the R8C/LA3A Group, set the MSTTRJ1 bit to 1 (standby).

Removed

2-1. Applicable Products

Product	User's Manual	Target Page
R8C/LA6A Group	R01UH0051EJ0103 (Rev.1.03)	Page 332 of 645

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

2-2. Descriptions to Be Corrected

20.2 Registers

20.2.1 Module Standby Control Register 1 (MSTCR1)

Address 0010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRJ2	MSTTRJ1	MSTTRJ0	MSTTRH	MSTTRB1	MSTTRB0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRB0	Timer RB0 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB1	Timer RB1 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRH	Timer RH standby bit	0: Active 1: Standby (3)	R/W
b3	MSTTRJ0	Timer RJ0 standby bit	0: Active 1: Standby (4)	R/W
b4	MSTTRJ1	Timer RJ1 standby bit	0: Active 1: Standby (5)	R/W
b5	MSTTRJ2	Timer RJ2 standby bit	0: Active 1: Standby (6)	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. When the MSTTRB0 bit is set to 1 (standby), any access to the timer RB0 associated registers (addresses 0108h to 010Eh) is disabled.
2. When the MSTTRB1 bit is set to 1 (standby), any access to the timer RB1 associated registers (addresses 0098h to 009Eh) is disabled.
3. When the MSTTRH bit is set to 1 (standby), any access to the timer RH associated registers (addresses 0110h to 011Fh) is disabled.
4. When the MSTTRJ0 bit is set to 1 (standby), any access to the timer RJ0 associated registers (addresses 0080h to 0086h) is disabled.
5. When the MSTTRJ1 bit is set to 1 (standby), any access to the timer RJ1 associated registers (addresses 0088h to 008Eh) is disabled.
6. When the MSTTRJ2 bit is set to 1 (standby), any access to the timer RJ2 associated registers (addresses 0090h to 0096h) is disabled.

The following note is added.

Timer RJ2 is not available for the R8C/LA6A Group. Do not access registers associated with timer RJ2 while the MSTTRJ2 bit is 0 (active).

3-1. Applicable products

Product	User's Manual	Target Page
R8C/36C Group	R01UH0095EJ0110 (Rev.1.10)	Page 130, 131 of 789
R8C/38C Group	R01UH0094EJ0110 (Rev.1.10)	Page 134, 135 of 794
R8C/34U, 34K Group	R01UH0245EJ0100 (Rev.1.00)	Page 118 of 706
R8C/3MU, 3MK Group	R01UH0244EJ0100 (Rev.1.00)	Page 113 of 683

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

3-2. Descriptions to Be Corrected (example shown in the R8C/36C Group)

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	CM02	Wait mode peripheral function clock stop bit	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	CM03	XCIN clock stop bit	0: XCIN clock oscillates 1: XCIN clock stops	R/W
b4	CM04	Port/XCIN-XCOUT switch bit (5, 6)	0: I/O ports P4_3 and P4_4 1: XCIN-XCOUT pin (7)	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 3)	0: XIN clock oscillates 1: XIN clock stops (2)	R/W
b6	CM06	CPU clock division select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	XIN, XCIN clock select bit (8)	0: XIN clock 1: XCIN clock	R/W

Notes:

1. The CM05 bit stops the XIN clock when the high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (1) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (2) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
3. Only when the CM05 bit is set to 1 (XIN clock stops) and the CM13 bit in the CM1 register is set to 0 (P4_6 and P4_7), P4_6 and P4_7 can be used as I/O ports.
   The P4_6 pin is shared with the XIN pin, and the P4_7 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the XIN clock.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
5. To use P4_3 and P4_4 as input ports, set the CM04 bit to 0 (I/O ports) and the CM03 bit to 1(XCIN clock stops).
   To use as external clock input, set the CM04 bit to 1 (XCIN-XCOUT pin), the CM03 bit to 1 (XCIN clock stops), and the CM12 bit in the CM1 register to 1 (on-chip feedback resistor disabled). When the PD4_3 bit in the PD4 register is further set to 0 (input mode), an external clock can be input. Set XCIN as the I/O port P4_3 at this time. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
   The P4_3 pin is shared with the XCIN pin, and the P4_4 pin is shared with the XCOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.

… (Other notes are omitted.)

Release the XCOUT pin at this time.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 7)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6)	0: I/O ports P4_6 and P4_7 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:

1. When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.
2. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. To use P4_6 and P4_7 as input ports, set the CM13 bit to 0 (I/O ports) and the CM05 bit in the CM0 register to 1 (XIN clock stops).
   To use as external clock input, set the CM13 bit to 1 (XIN-XOUT pin), the CM05 bit to 1 (XIN clock stops), and the CM11 bit to 1 (on-chip feedback resistor disabled). When the PD4_7 bit in the PD4 register is further set to 0 (input mode), an external clock can be input. Set XIN as the I/O port P4_6 at this time. When the pin is not used, treat it as an unassigned pin and use the appropriate handling.
   The P4_6 pin is shared with the XIN pin, and the P4_7 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the on-chip oscillation circuit.
6. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
7. Do not set the CM10 bit to 1 (stop mode) when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Release the XIN pin at this time.

4-1. Applicable Products

Product	User's Manual	Target Page
R8C/L35A, L35B Group, R8C/L36A, L36B Group, R8C/L38A, L38B Group, R8C/L3AA, L3AB Group	REJ09B0441-0100 (Rev.1.00)	Page 112 of 802

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

4-2. Descriptions to Be Corrected

8.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	CM13	Port/XIN-XOUT switch bit (4, 5)	0: I/O ports P12_0 and P12_1 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (3)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0, bits CM16 and CM17 are enabled.
2. When the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use P12_0 and P12_1 as input ports, set the CM13 bit to 0 (I/O ports), the CM05 bit in the CM0 register to 1 (XIN clock stops), and the CM07 bit to 1 (XCIN clock).
   To use as external clock input, set the CM13 bit to 0 (I/O ports), the CM05 bit to 1 (XIN clock oscillates), the CM07 bit to 0 (XIN clock). When the PD12_0 bit in the PD12 register is further set to 0 (input mode), an external clock can be input. XOUT can be used as the input port P12_1 at this time.
   The P12_0 pin is shared with the XIN pin, and the P12_1 pin is shared with the XOUT pin. These pins cannot be used as I/O ports when using the XIN clock.
5. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.

Stops

6-1. Applicable Products

Product	User's Manual	Target Page
R8C/33A Group	REJ09B0455-0020 (Rev.0.20)	Page 129 of 598
R8C/35A Group	REJ09B0407-0040 (Rev.0.40)	Page 148 of 736
R8C/36A Group	REJ09B0480-0020 (Rev.0.20)	Page 156 of 795
R8C/38A Group	REJ09B0485-0010 (Rev.0.10)	Page 161 of 800
R8C/3GA Group	REJ09B0472-0020 (Rev.0.20)	Page 123 of 580
R8C/3JA Group	REJ09B0508-0100 (Rev.1.00)	Page 137 of 723
R8C/33M Group	R01UH0132EJ0100 (Rev.1.00)	Page 128 of 605
R8C/34M Group	R01UH0131EJ0100 (Rev.1.00)	Page 143 of 740
R8C/35M Group	R01UH0130EJ0100 (Rev.1.00)	Page 150 of 744

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

6-2. Descriptions to Be Corrected (example shown in the R8C/33A Group)

Before correction:

10.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. The PRC2 bit is set to 0 after writing 1 to it and executing a write to any address. Since the other bits are not set to 0, set them to 0 by a program.

After correction:

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled (2)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (2)	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (2)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC activation between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

Notes 1 and 2 apply to the applicable products listed in the table above.

7-1. Applicable Products

Product	User's Manual	Target Page
R8C/L35A, L35B Group, R8C/L36A, L36B Group, R8C/L38A, L38B Group, R8C/L3AA, L3AB Group	REJ09B0441-0100 (Rev.1.00)	Page 90 of 802
R8C/L35C, L36C Group, R8C/L38C, L3AC Group	R01UH0151EJ0101 (Rev.1.01)	Page 107 of 836
R8C/L35M, L36M Group, R8C/L38 M, L3AM Group	R01UH0110EJ0100 (Rev.1.00)	Page 104 of 852

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

7-2. Descriptions to Be Corrected (example shown in the R8C/L38C Group)

Table 7.9 Port P3

Pin	Register	PD3	LSE3	INTSR	INTEN	INTEN1	ADMOD		TRBRCSR		TRCMR	TRCCR2		Function
	Bit	PD3_I	LSEI=24	INT0EL0	INTIEN	INTIEN	ADCAP1	ADCAP0	TRCTRGSEL1	TRCTRGSEL0	PWM2	TCEG1	TCEG0	
Port P3_0 SEG24 INT0	I = 0	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG24)
		0	0	0	1	—	—	—	—	—	—	—	—	INT0 input (1)
Port P3_1 SEG25 INT1	I = 1	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG25)
		0	0	0	1	—	—	—	—	—	—	—	—	INT1 input (1)
Port P3_2 SEG26 INT2	I = 2	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG26)
		0	0	0	1	—	—	—	—	—	—	—	—	INT2 input (1)
Port P3_3 SEG27 INT3	I = 3	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG27)
		0	0	0	1	—	—	—	—	—	—	—	—	INT3 input (1)
Port P3_4 SEG28 INT4	I = 4	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X	—	—	—	—	—	—	—	LCD drive control output (SEG28)
		0	0	0	—	1	—	—	—	—	—	—	—	INT4 input (1)
Port P3_5 SEG29 INT5	I = 5	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X	—	—	—	—	—	—	—	LCD drive control output (SEG29)
		0	0	0	—	1	—	—	—	—	—	—	—	INT5 input (1)
Port P3_6 SEG30 INT6	I = 6	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X	—	—	—	—	—	—	—	LCD drive control output (SEG30)
		0	0	0	—	1	—	—	—	—	—	—	—	INT6 input (1)
Port P3_7 SEG31 INT7 ADTRG TRCTRG	I = 7	0	0	X	—	X	X	X	X	X	X	X	X	Input port (1)
		1	0	X	—	X	X	X	X	X	X	X	X	Output port
		X	1	X	—	1	X	X	X	X	X	X	X	LCD drive control output (SEG31)
		0	0	0	—		X	X	X	X	X	X	X	INT7 input (1)
		0	0	0	—		1	1	X	X	X	X	X	ADTRG input (1)
		0	0	X	— —	X	X	X	0	1	0	0 1	1 X	PWM2 mode TRCTRG input (1)

X: 0 or 1; —: No change in outcome

Note:
1. Pulled up by setting the corresponding bit in the P3PUR register to 1.

X

8-1. Applicable Products

Product	User's Manual	Target Page
R8C/LA3A, LA5A Group	R01UH0024EJ0100 (Rev.1.00)	Page 84 of 581

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

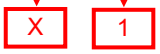
8-2. Descriptions to Be Corrected

Table 7.10 P0_5/SEG5/SSI

Register		PD0	LSE0	SSUIICSR		SSU Associated Register	Function
Bit		PD0_5	LSE05	SSISEL0	IICSEL		
Pin	P0_5	0	0	X	X	Refer to synchronous serial communication unit (**Table 23.4 Association between Communication Modes and I/O Pins**).	Input port (1)
		1	0	X	X		Output port
	SEG5	0	0	X	X		LCD drive control output
	SSI	0	0	1	0		$\overline{SCS}$ input (1)
		X	0	1	0		$\overline{SCS}$ output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU05 bit in the P0PUR register to 1.
2. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit to 0 (standard mode).



9-1. Applicable Products

Product	User's Manual	Target Page
R8C/32M Group	R01UH0133EJ0100 (Rev.1.00)	Page 448 of 592
R8C/33M Group	R01UH0132EJ0100 (Rev.1.00)	Page 459 of 605
R8C/34M Group	R01UH0131EJ0100 (Rev.1.00)	Page 586 of 740
R8C/35M Group	R01UH0130EJ0100 (Rev.1.00)	Page 592 of 744
R8C/36M Group	R01UH0259EJ0100 (Rev.1.00)	Page 650 of 806
R8C/38M Group	R01UH0258EJ0100 (Rev.1.00)	Page 655 of 812
R8C/3GM Group	R01UH0284EJ0100 (Rev.1.00)	Page 444 of 591
R8C/3JM Group	R01UH0285EJ0100 (Rev.1.00)	Page 581 of 734
R8C/33T Group	R01UH0156EJ0110 (Rev.1.10)	Page 392 of 531
R8C/3JT Group	R01UH0154EJ0100 (Rev.1.00)	Page 390 of 528
R8C/3NT Group	R01UH0087EJ0100 (Rev.1.00)	Page 456 of 601
R8C/L35C, L36C Group, R8C/L38C, L3AC Group	R01UH0151EJ0101 (Rev.1.01)	Page 660 of 836
R8C/L35M, L36M Group, R8C/L38 M, L3AM Group	R01UH0110EJ0100 (Rev.1.00)	Page 659 of 852
R8C/LA3A, LA5A Group	R01UH0024EJ0100 (Rev.1.00)	Page 439 of 581

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

9-2. Descriptions to Be Corrected

28.2.6 A/D Control Register 1 (ADCON1)

Address 00D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit (1)	0: Extended analog input pin not selected 1: On-chip reference voltage selected (2, 6, 7)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (3)	0: A/D operation stops (standby) (4) 1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (5, 7)	0: Disabled 1: Enabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (5)	0: Discharge before conversion 1: Precharge before conversion	R/W

Notes:
1. When on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).
   When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).
2. Do not set to 1 (A/D conversion using comparison reference voltage as input) in single sweep mode or repeat sweep mode.
3. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for 1 ϕAD cycle or more before starting A/D conversion.
4. Stop the A/D function before setting to standby. When the ADSBY bit is set to 1 (standby), any access to the A/D associated registers (addresses 00C0h to 00CFh, and 00D4h to 00D7h) is disabled.
5. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result with an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.
6. When on-chip reference voltage is used (ADEX0 = 1), set bits CH2 to CH0 in the ADINSEL register to 000b.
7. When on-chip reference voltage is used (ADEX0 = 1), set the ADDDAEN bit to 0 (A/D open-circuit detection assist function disabled).

When the ADSTBY bit is 0 (standby)

10-1. Applicable Products

Product	User's Manual	Target Page
R8C/35A Group	REJ09B0407-0040 (Rev.0.40)	Page 379 of 736
R8C/36A Group	REJ09B0480-0020 (Rev.0.20)	Page 390 of 795
R8C/38A Group	REJ09B0485-0010 (Rev.0.10)	Page 395 of 800
R8C/3JA Group	REJ09B0508-0100 (Rev.1.00)	Page 366 of 723

If the description to be corrected appears in the User's Manual on pages other than pages listed above, the same correction will also apply to the descriptions on those pages.

10-2. Descriptions to Be Corrected (example shown in the R8C/35A Group)

Before correction:

20.7.3 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

After correction:

20.7.3 Timer RD Trigger Control Register (TRDADCR) in Complementary PWM Mode

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	Set to 0.	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W