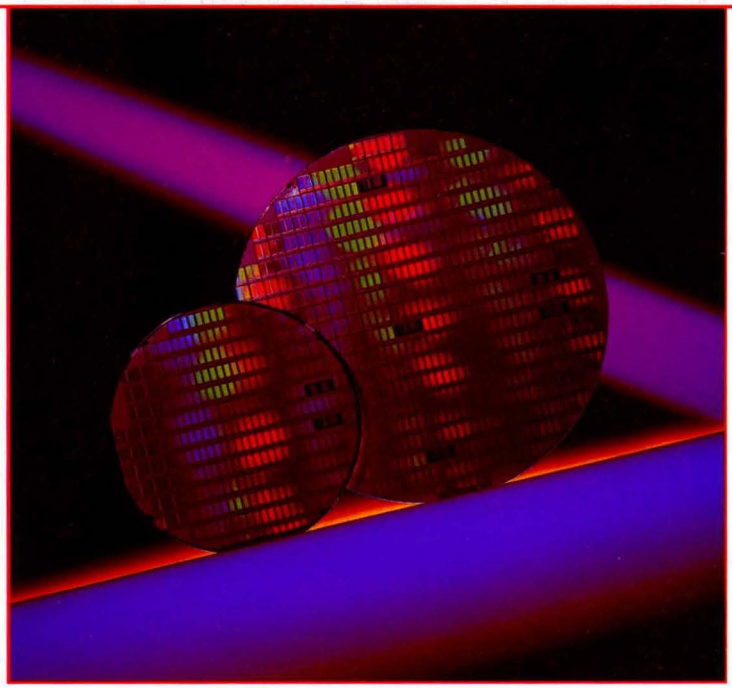
Data Book



Xicor®

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*NOVRAM is Xicor's nonvolatile static RAM device family.
E²POT™ is a trademark of Xicor, Inc.

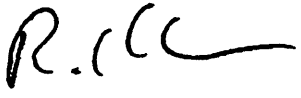
Xicor® DATA BOOK

President's Message

Dear Customer:

For Xicor, the company focus is toward achieving the goal of total customer satisfaction. As part of this effort, being the leader of the exciting field of full-featured E^{2}PROM and NOVRAM memories, Xicor has charted a course to provide the most extensive product offering to cover the needs of your company in the field-programmable nonvolatile area. This data book contains data sheets for full-featured E^{2}PROMs, NOVRAMs, and the revolutionary E^{2}POT potentiometers. These products are typically available in a wide variety of speeds, package types and both parallel and serial interface configurations. The majority of the products are offered with extended temperature range, and many comply with all the requirements of Mil-Std-883 Revision C for Class B products. This data book also contains product and process reliability reports and applications notes.

To date, Xicor has shipped close to 100 million E^{2}PROM and NOVRAM memories to its customers. Our research and development activities are substantial and will enable us to continue to introduce innovative products based on the most optimized technology for full-featured, nonvolatile, field-programmable products. Our worldwide sales, marketing and applications organizations are dedicated to supporting your requirements. We appreciate your business and look forward to supplying your present and future requirements.



Raphael Klein
President
October, 1990

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First Printing
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Fact Sheets contain information on products under development. Xicor reserves the right to change these specifications or modify the product at any time, without notice.

Advanced Data Sheets contain typical product specifications which are subject to change upon device characterization over the full specified temperature range. Xicor reserves the right to change these specifications or modify the product at any time, without notice.

Preliminary Data Sheets contain minimum and maximum limits specified over the full temperature range based upon initial production device characterization. Xicor reserves the right to change these specifications or modify the product at any time, without notice.

Final Data Sheets contain minimum and maximum limits specified over the full temperature range for production devices.

Contact your local Xicor sales representative to obtain the latest specifications prior to order placement.

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U.S. PATENTS
Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976. Foreign patents and additional patents pending.

LIFE RELATED POLICY
In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Precautions for the Handling of MOS Devices

Xicor products are designed with effective input protection to prevent damage to the devices under most conditions. However, any MOS circuit can be catastrophically damaged by excessive electrostatic discharge or transient voltages. The following procedures are recommended to avoid accidental circuit damage.

I. Testing MOS Circuits:

1. All units should be handled directly from the conductive or antistatic plastic tube in which they were shipped if possible. This action minimizes touching of individual leads.
2. If units are to be tested without using the tube carrier, the following precautions should be taken:
   a. Table surfaces which potentially will come in contact with the devices either directly or indirectly (such as through shipping tubes) must be metal or of another conductive material and should be electrically connected to the test equipment and to the test operator (a grounding bracelet is recommended).
   b. The units should be transported in bundled antistatic tubes or metal trays, both of which will assume a common potential when placed on a conductive table top.
   c. Do not band tubes together with adhesive tape or rubber bands without first wrapping them in a conductive layer.

II. Test Equipment (Including Environmental Equipment):

1. All equipment must be properly returned to the same reference potential (ground) as the devices, the operator, and the container for the devices.
2. Devices to be tested should be protected from high voltage surges developed by:
   a. Turning electrical equipment on or off.
   b. Relay switching.
   c. Transients from voltage sources (AC line or power supplies).

III. Assembling MOS Devices Onto PC Boards:

1. The MOS circuits should be mounted on the PC board last.
2. Similar precautions should be taken as in Item I above, at the assembly work station.
3. Soldering irons or solder baths should be at the same reference (ground) potential as the devices.
4. Plastic materials which are not antistatic treated should be kept away from devices as they develop and maintain high levels of static charge.

IV. Device Handling:

1. Handling of devices should be kept to a minimum. If handling is required, avoid touching the leads directly.

V. General:

1. The handler should take every precaution that the device will see the same reference potential when moved.
2. Anyone handling individual devices should develop a habit of first touching the container in which the units are stored before touching the units.
3. Before placing the units into a PC board, the handler should touch the PC board first.
4. Personnel should not wear clothing which will build up static charge. They should wear smocks and clothing made of 100% cotton rather than wool or synthetic fibers.
5. Be careful of electrostatic build up through the movement of air over plastic material. This is especially true of acid sinks.
6. Personnel or operators should always wear grounded wrist straps when working with MOS devices.
7. A 1 meg ohm resistance ground strap is recommended and will protect people up to 5,000 volts AC RMS or DC by limiting current to 5 milliamperes.
8. Antistatic ionized air equipment is very effective and useful in preventing electrostatic damage.
9. Low humidity maximizes potential static problems. Maintaining humidity levels above 45% is one of the most effective ways to guard against static handling problems.

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*NOVRAM is Xicor's nonvolatile static RAM device.

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Memory Overview

Since its founding, Xicor has developed and placed into production a wide range of system-alterable nonvolatile memory devices. These devices, manufactured with Xicor's proprietary state-of-the-art textured triple-poly floating gate process, are available in a variety of architectures (NOVRAM* and E^2PROM), interfaces (nibble-wide, byte-wide and serial), densities, and speeds. Xicor's success as an innovator and leader in system-alterable nonvolatile memory is affirmed with an *Electronic Product Magazine* Product of the Year award in 1980 and again in 1982 for the first 5-volt only NOVRAM and the first 5-volt only full featured E^2PROM, respectively.

Lower density E^2PROMs and NOVRAMs have been readily available for a number of years and have provided unique niche applications solutions. Serial devices have replaced DIP switches in a wide range of products that offer user selectable operating parameters. Nibble-wide and byte-wide NOVRAMs and E^2PROMs are being used in instrumentation and industrial control applications to store calibration data and control information. Communications equipment has implemented these same devices to store phone numbers in repertory dialers and antenna positioning equipment.

The list of first generation applications goes on at length; however, with the second generation represented by the X2864A, the direction of applications began to diverge. The higher density allowed practical usage of E^2PROMs in program and mass data storage. The advent of the X28256 has pushed this application usage even higher.

Xicor strives to serve the marketplace by providing next generation devices in existing product areas as evidenced by the X2864B and X2864H high speed 64K E^2PROMs. Similarly, the X24C16 and X24C04 maintain compatibility with the original X2404 but offer low power operation over a much wider V_{CC} range.

As designers have gained experience implementing the denser E^2PROM devices into system memories, they have given Xicor feedback on features they would like. Xicor has listened.

Xicor's response has been active. The issues addressed by the Xicor design team have been: faster read access time, faster write cycle time, denser memory devices and write protection mechanisms.

Xicor has also implemented added features via software control rather than "dedicated pin" hardware control for optional system use. Xicor is committed to providing solutions that neither hinder nor limit the system designer's imagination. The products and features shown in the data sheets in this data book illustrate Xicor's dedication to listening to you, the designer, in providing memory design solutions.

*NOVRAM is Xicor's nonvolatile static RAM device.

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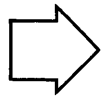


NOVRAM* Data Sheets

1

Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **High Reliability**
  - **—Store Cycles: 10,000**
  - **—Data Retention: 100 Years**

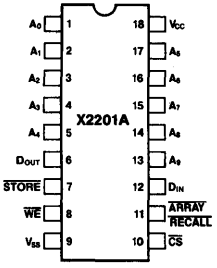
DESCRIPTION

The Xicor X2201A is a 1024 x 1 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2201A is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles and inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATION

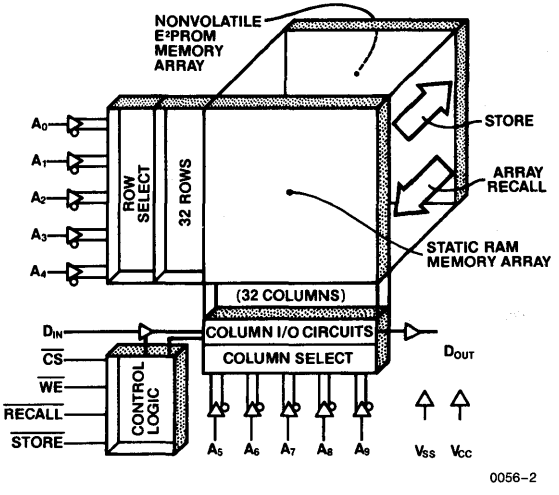


0056-1

PIN NAMES

A_0–A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Out
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL DIAGRAM



0056-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	Power Supply Current		60	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Load Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	1,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	10,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

Inputs				Input Output I/O	Mode
$\overline{CS}$	$\overline{WE}$	ARRAY RECALL	$\overline{STORE}$		
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(4)
H	X	H	L	Output High Z	Nonvolatile Storing(4)

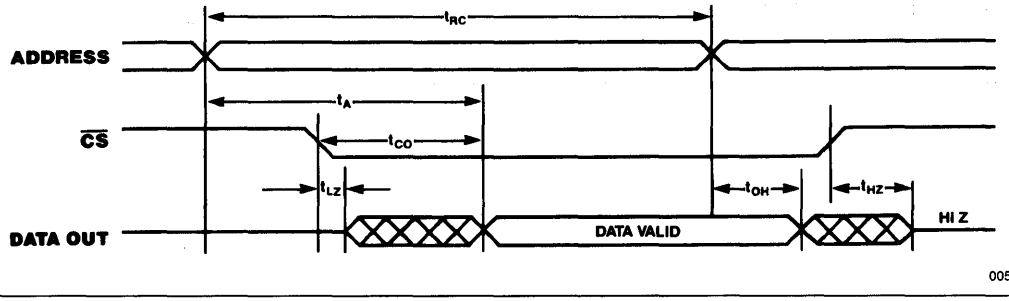
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	300		ns
t_A	Access Time		300	ns
t_{CO}	Chip Select to Output Valid		200	ns
t_{OH}	Output Hold from Address Change	50		ns
t_{LZ}(5)	Chip Select to Output in Low Z	10		ns
t_{HZ}(5)	Chip Deselect to Output in High Z	10	100	ns

Read Cycle



Notes: (3) Chip is deselected but may be automatically completing a store cycle.

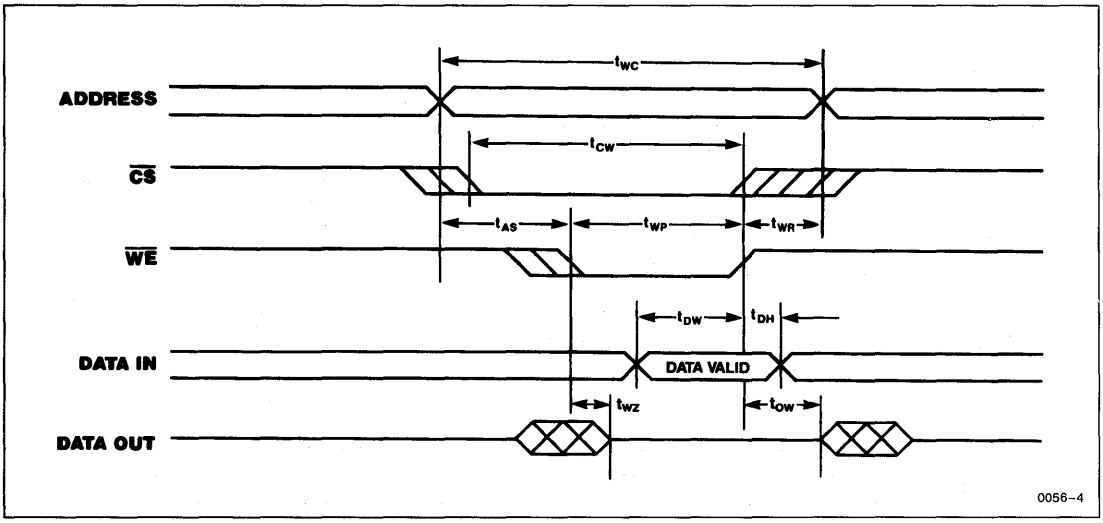
(4) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).

(5) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

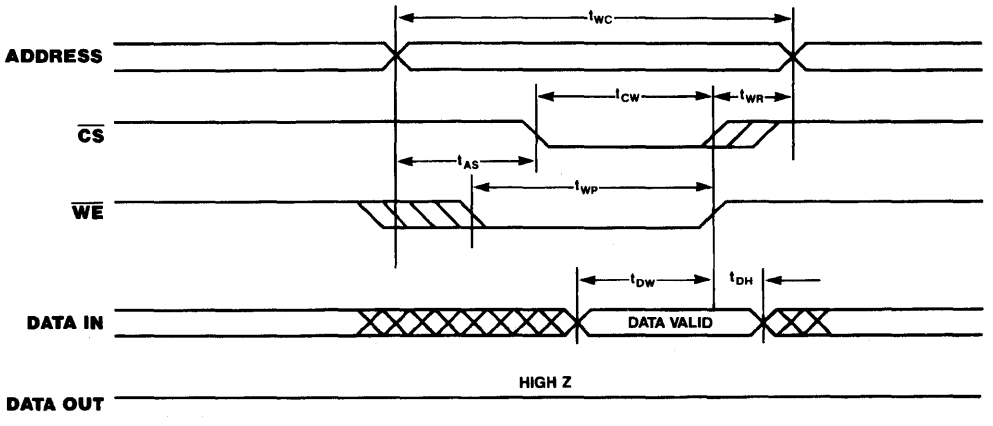
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	300		ns
t_{CW}	Chip Select to End of Write	150		ns
t_{AS}	Address Setup Time	50		ns
t_{WP}	Write Pulse Width	150		ns
t_{WR}	Write Recovery Time	25		ns
t_{DW}	Data Valid to End of Write	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	ns
t_{OW}	Output Active from End of Write	10		ns

Write Cycle



Early Write Cycle



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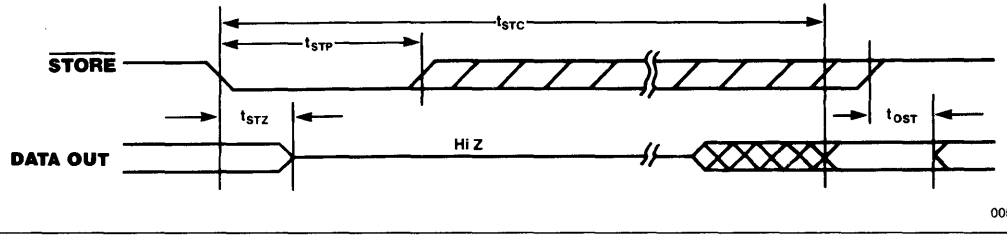
Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Store Time		10	ms
t_{STP}	Store Pulse Width	100		ns
t_{STZ}	Store to Output in High Z		500	ns
t_{OST}	Output Active from End of Store	10		ns

Store Cycle

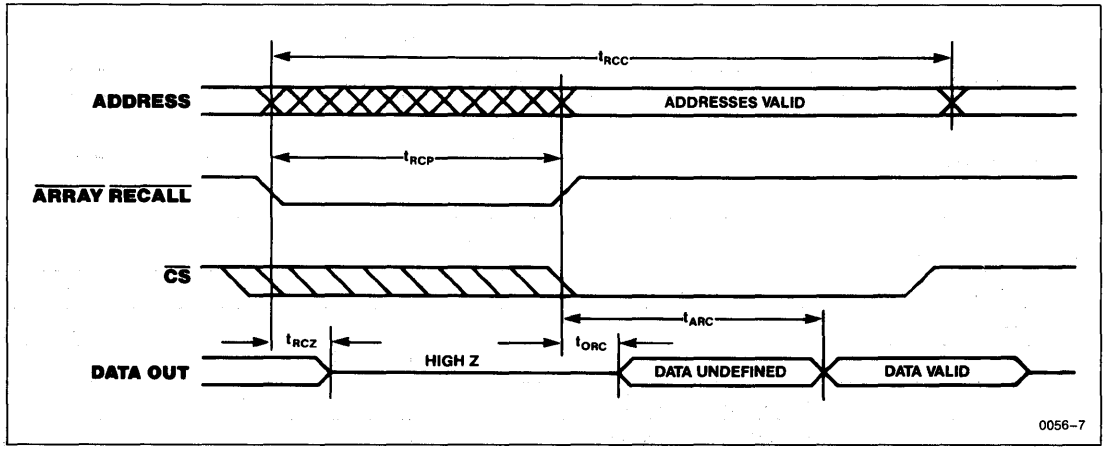


0056-6

Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Cycle Time	1200		ns
t_{RCP}	Recall Pulse Width(6)	450		ns
t_{RCZ}	Recall to Output in High Z		150	ns
t_{ORC}	Output Active from End of Recall	10		ns
t_{ARC}	Recalled Data Access Time from End of Recall		750	ns

Array Recall Cycle



Note: (6) Array Recall rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_9)

The address inputs select a memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read/write operations with the RAM array. $\overline{CS}$ HIGH will place the D_{OUT} in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the D_{OUT} buffer, determining whether a RAM read or write operation is enabled. $\overline{WE}$ HIGH enables a read and $\overline{WE}$ LOW enables a write.

Data In (D_{IN})

Data is written into the device via the D_{IN} input.

Data Out (D_{OUT})

Data from a selected address is output on the D_{OUT} output. This pin is in the high impedance state when either $\overline{CS}$ is HIGH or when $\overline{WE}$ is LOW.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and $\overline{ARRAY\ RECALL}$ inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM.

$\overline{ARRAY\ RECALL}$

The $\overline{ARRAY\ RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{ARRAY\ RECALL}$ is asserted. $\overline{ARRAY\ RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

WRITE PROTECTION

The X2201A has three write protect features that are employed to protect the contents of the nonvolatile memory.

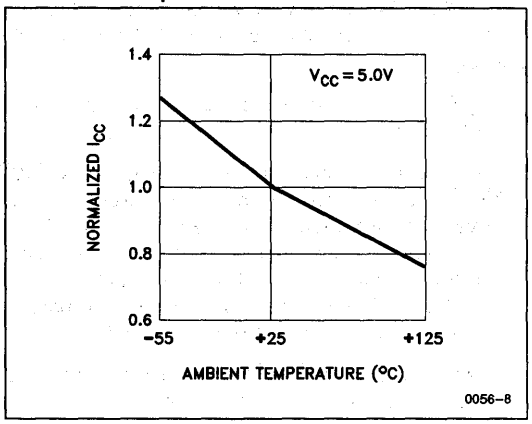
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{ARRAY\ RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained. It should be noted; whichever method is employed, all control inputs should be stable and the device deselected prior to release of the controlling protection signal.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns (typical) will *not* initiate a store cycle.

Part Number	Store Cycles	Data Changes Per Bit
X2201A	10,000	1,000

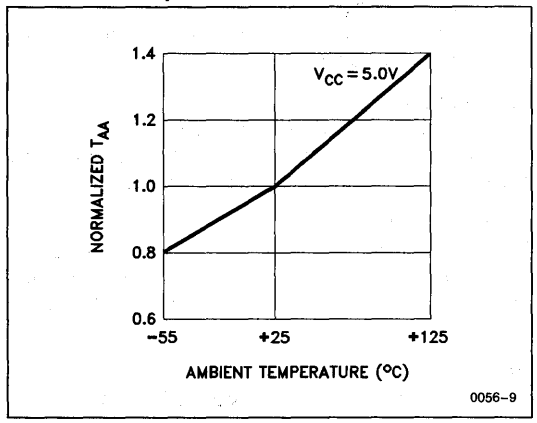
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Normalized Active Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **High Reliability**
  - **—Store Cycles: 100,000**
  - **—Data Retention: 100 Years**
- **JEDEC Standard 18-Pin Package**

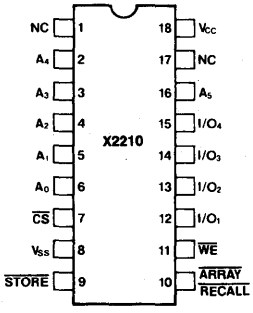
DESCRIPTION

The Xicor X2210 is a 64 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2210 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2210 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 100,000 store cycles and inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATION

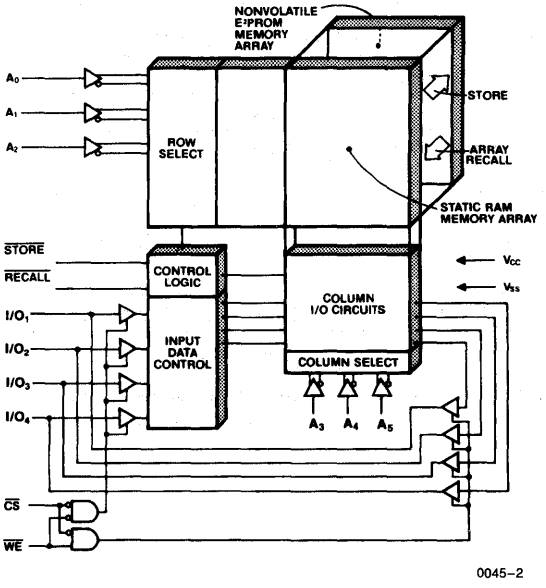


0045-1

PIN NAMES

A_0–A_5	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0045-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2210 ..... −10°C to +85°C
X2210I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2210 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2210I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2210 Limits		X2210I Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	Power Supply Current		50		55	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Load Current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +1.0	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −2 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	10,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	100,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

Inputs				Input Output I/O	Mode
$\overline{CS}$	WE	ARRAY RECALL	STORE		
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(4)
H	X	H	L	Output High Z	Nonvolatile Storing(4)

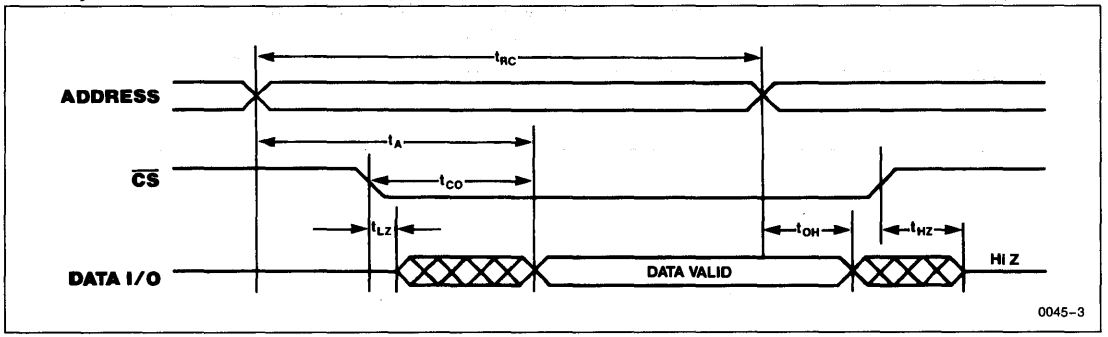
A.C. CHARACTERISTICS

X2210 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2210I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	300		ns
t_A	Access Time		300	ns
t_{CO}	Chip Select to Output Valid		200	ns
t_{OH}	Output Hold from Address Change	50		ns
t_{LZ}(5)	Chip Select to Output in Low Z	10		ns
t_{HZ}(5)	Chip Deselect to Output in High Z	10	100	ns

Read Cycle



Notes: (3) Chip is deselected but may be automatically completing a store cycle.

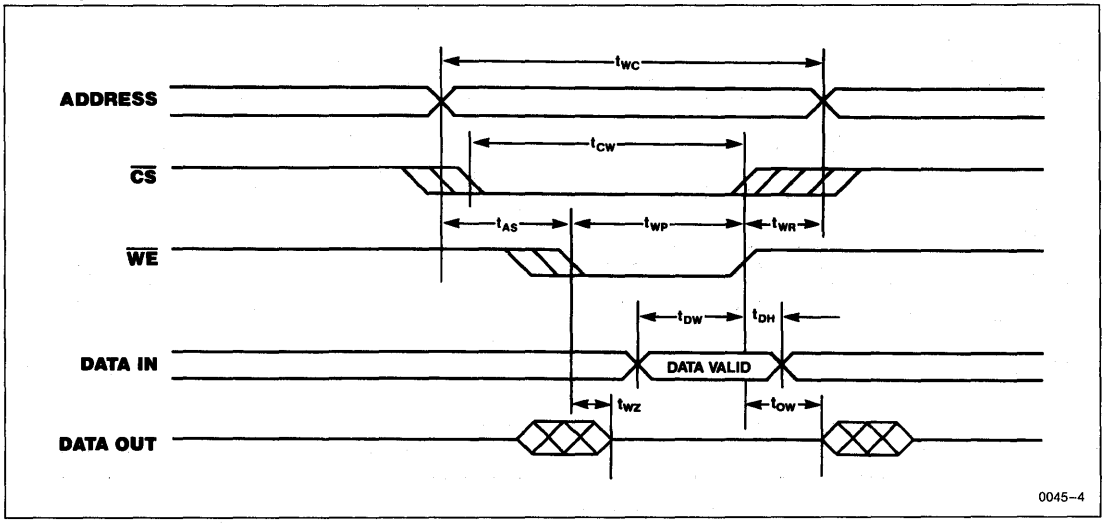
(4) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).

(5) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

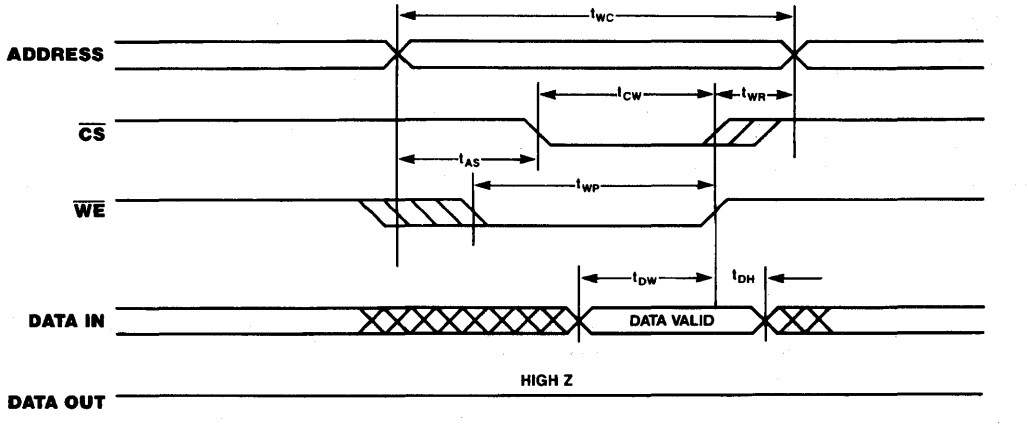
Write Cycle Limits

Symbol	Parameter		Min.	Max.	Units
t_{WC}	Write Cycle Time		300		ns
t_{CW}	Chip Select to End of Write		150		ns
t_{AS}	Address Setup Time		50		ns
t_{WP}	Write Pulse Width		150		ns
t_{WR}	Write Recovery Time		25		ns
t_{DW}	Data Valid to End of Write		100		ns
t_{DH}	Data Hold Time	X2210	0		ns
		X2210I	20		ns
t_{WZ}	Write Enable to Output in High Z		10	100	ns
t_{OW}	Output Active from End of Write		10		ns

Write Cycle



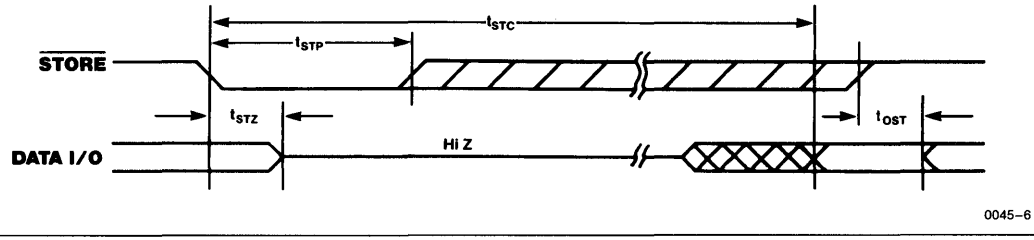
Early Write Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Store Time		10	ms
t_{STP}	Store Pulse Width	100		ns
t_{STZ}	Store to Output in High Z		500	ns
t_{OST}	Output Active from End of Store	10		ns

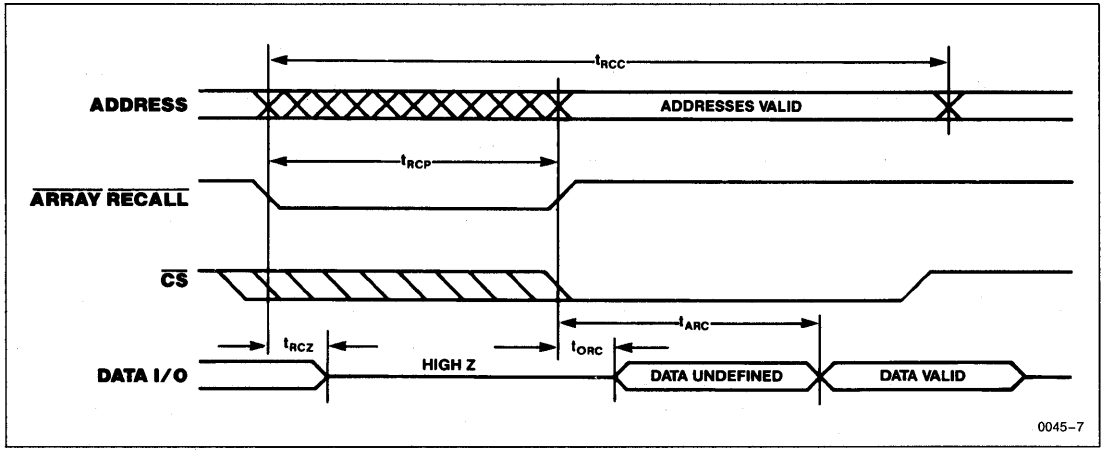
Store Cycle



Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Cycle Time	1200		ns
t_{RCP}	Recall Pulse Width(6)	450		ns
t_{RCZ}	Recall to Output in High Z		150	ns
t_{ORC}	Output Active from End of Recall	10		ns
t_{ARC}	Recalled Data Access Time from End of Recall		750	ns

Array Recall Cycle



Note: (6) Array Recall rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_5)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read/write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. $\overline{WE}$ HIGH enables a read and $\overline{WE}$ LOW enables a write.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X2210 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and $\overline{ARRAY\ RECALL}$ inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM.

$\overline{ARRAY\ RECALL}$

The $\overline{ARRAY\ RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{ARRAY\ RECALL}$ is asserted. $\overline{ARRAY\ RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

WRITE PROTECTION

The X2210 has three write protect features that are employed to protect the contents of the nonvolatile memory.

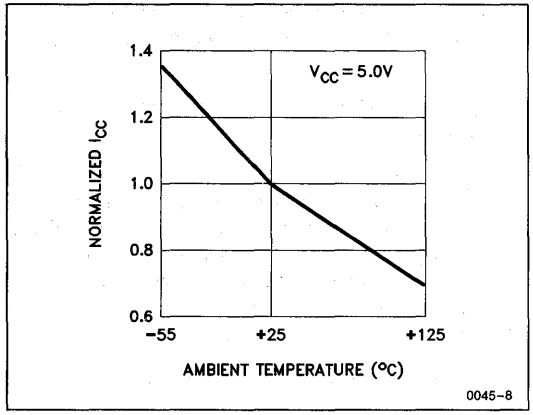
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{ARRAY\ RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained. It should be noted; whichever method is employed, all control inputs should be stable and the device deselected prior to release of the controlling protection signal.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns (typical) will *not* initiate a store cycle.

Part Number	Store Cycles	Data Changes Per Bit
X2210 X2210I	10,000	1,000
X2210/5 X2210I/5	50,000	5,000
X2210/10 X2210I/10	100,000	10,000

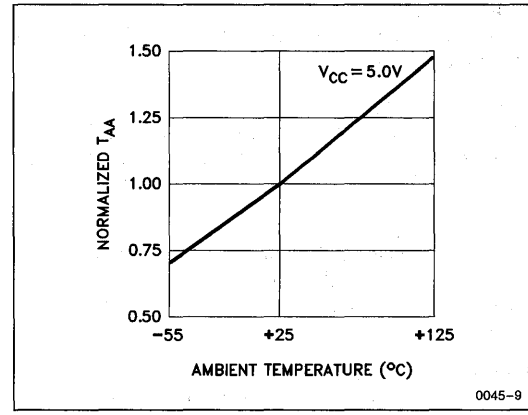
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Normalized Active Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **JEDEC Standard 18-Pin Package**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 250 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **100 Year Data Retention**

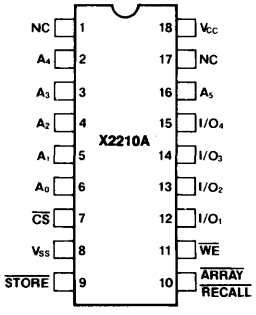
DESCRIPTION

The Xicor X2210A is a 64 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2210A is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2210A features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

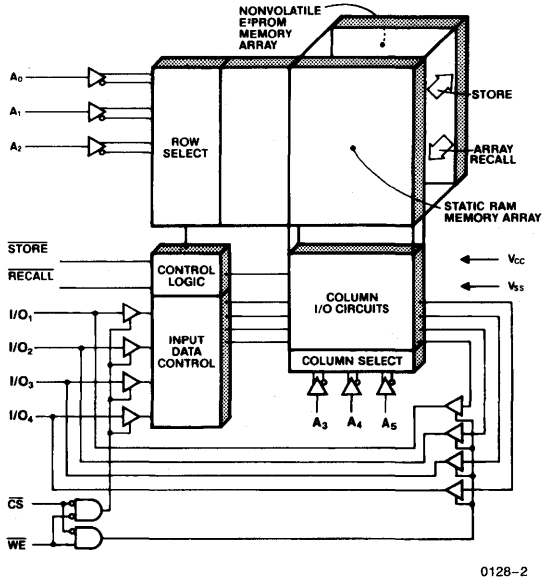


0128-1

PIN NAMES

A_0–A_5	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0128-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	Power Supply Current		50	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Load Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

Inputs				Input Output I/O	Mode
$\overline{CS}$	$\overline{WE}$	ARRAY RECALL	$\overline{STORE}$		
H	X	H	H	Output High Z	Not Selected(2)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(3)
H	X	H	L	Output High Z	Nonvolatile Storing(3)

Notes: (1) This parameter is periodically sampled and not 100% tested.

(2) Chip is deselected but may be automatically completing a store cycle.

(3) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).

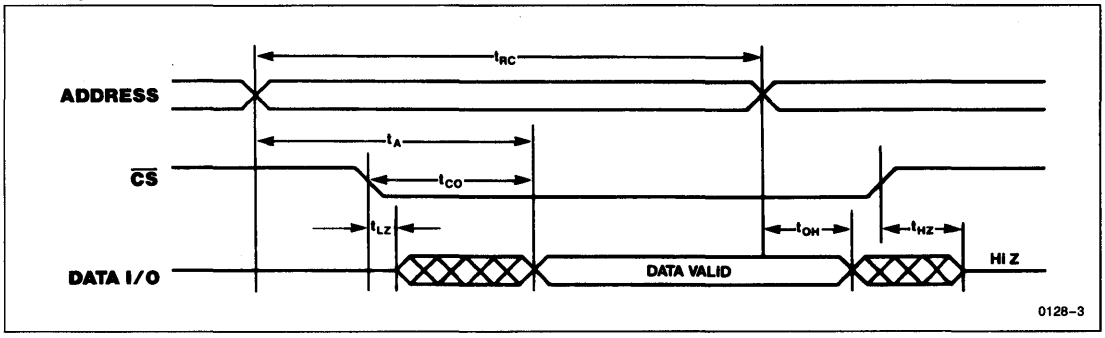
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Select to Output Valid		200	ns
t_{OH}	Output Hold from Address Change	50		ns
t_{LZ}	Chip Select to Output in Low Z	10		ns
t_{HZ}	Chip Deselect to Output in High Z	10	100	ns

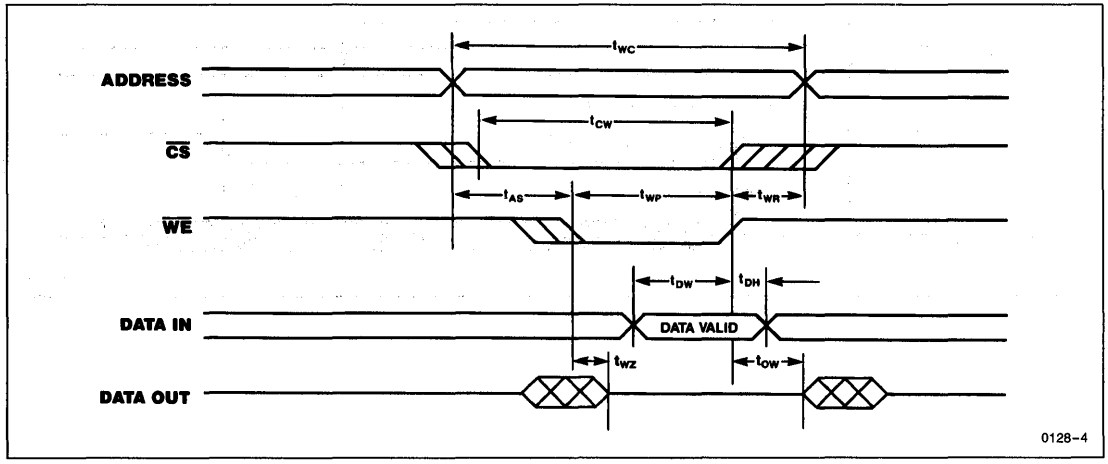
Read Cycle



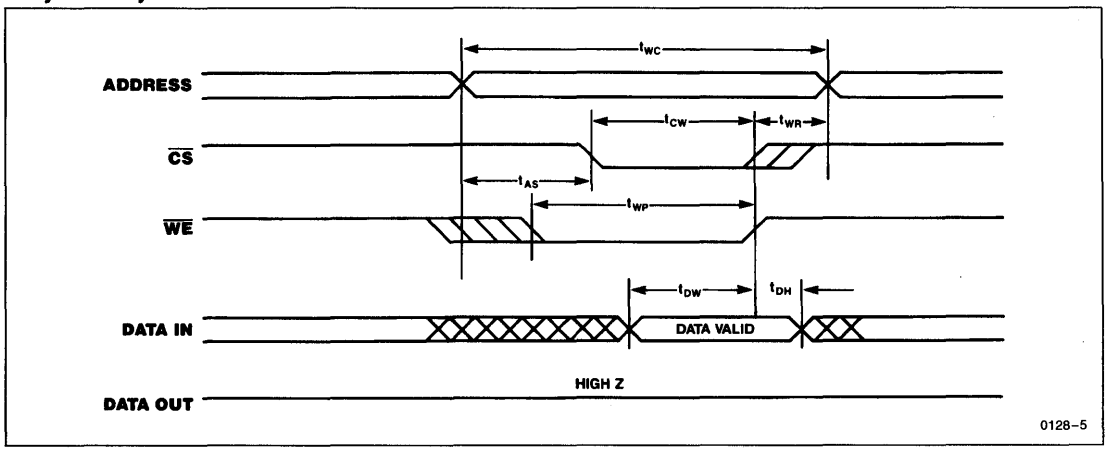
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	250		ns
t_{CW}	Chip Select to End of Write	150		ns
t_{AS}	Address Setup Time	50		ns
t_{WP}	Write Pulse Width	150		ns
t_{WR}	Write Recovery Time	25		ns
t_{DW}	Data Valid to End of Write	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	ns
t_{OW}	Output Active from End of Write	10		ns

Write Cycle



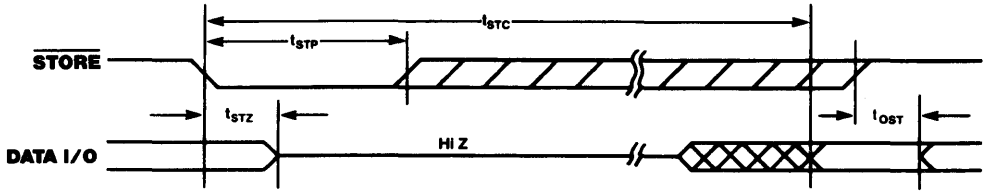
Early Write Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Store Cycle Time		10	ms
t_{STP}	Store Pulse Width	100		ns
t_{STZ}	Store to Output in High Z		500	ns
t_{OST}	Output Active from End of Store	10		ns

Store Cycle

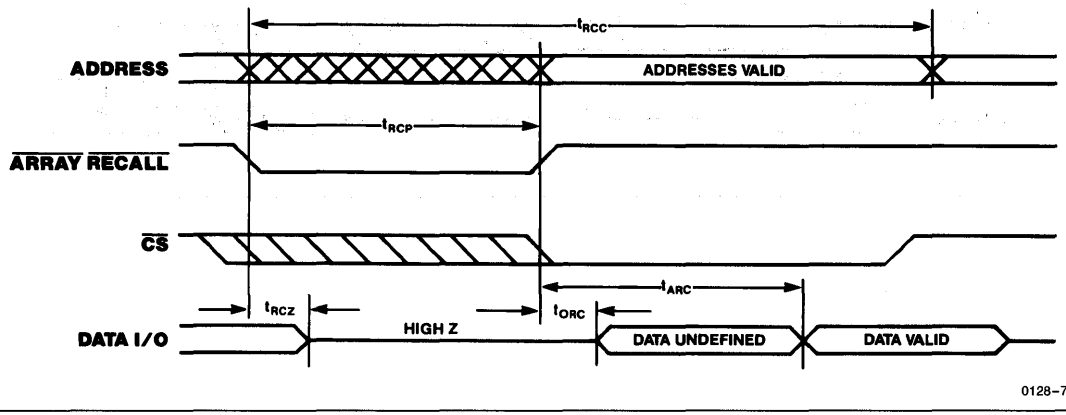


0128-6

Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Cycle Time	1200		ns
t_{RCP}	Recall Pulse Width(4)	450		ns
t_{RCZ}	Recall to Output in High Z		150	ns
t_{ORC}	Output Active from End of Recall	10		ns
t_{ARC}	Recalled Data Access Time from End of Recall		750	ns

Array Recall Cycle



Note: (4) Array Recall rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_5)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read/write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. $\overline{WE}$ HIGH enables a read and $\overline{WE}$ LOW enables a write.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X2210A through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and $\overline{ARRAY\ RECALL}$ inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM.

$\overline{ARRAY\ RECALL}$

The $\overline{ARRAY\ RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{ARRAY\ RECALL}$ is asserted. $\overline{ARRAY\ RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

WRITE PROTECTION

The X2210A has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3V, typically.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns will *not* initiate a store cycle.

ENDURANCE

The endurance specification of a device is characterized by the predicted *first* bit failure to occur in the entire memory (device or system) array rather than the average or typical value for the array. Since endurance is limited by the number of electrons trapped in the oxide during data changes, Xicor NOVRAMs are designed to minimize the number of changes an E²PROM bit cell undergoes during store operations. Only those bits in the E²PROM that are different from their corresponding location in the RAM will be "cycled" during a nonvolatile store. This characteristic reduces unnecessary cycling of any of the rest of the bits in the array, thereby increasing the potential endurance of each bit and increasing the potential endurance of the entire array. Reliability data documented in RR-504, the *Xicor Reliability Report on Endurance*, and additional reports are available from Xicor.

Part Number	Store Cycles	Data Changes Per Bit
X2210A	10,000	1,000

NOTES

Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **High Reliability**
  - **—Store Cycles: 100,000**
  - **—Data Retention: 100 Years**
- **JEDEC Standard 18-Pin Package**

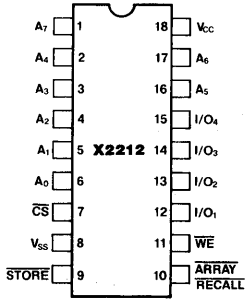
DESCRIPTION

The Xicor X2212 is a 256 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2212 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2212 features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 100,000 store cycles and inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATION

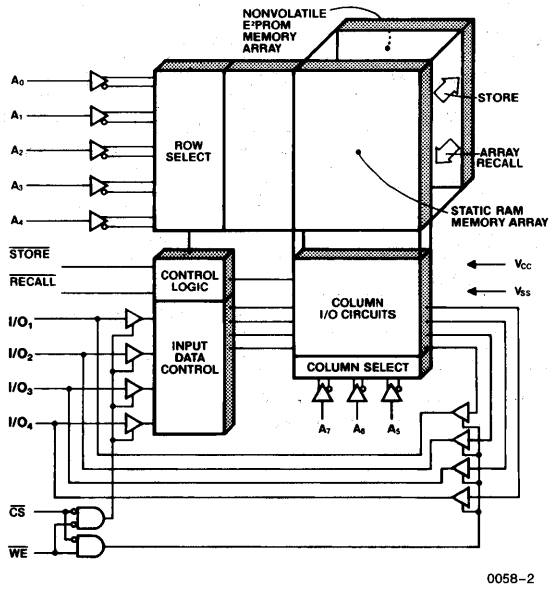


0058-1

PIN NAMES

A_0–A_7	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0058-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2212 ..... −10°C to +85°C
X2212I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2212 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2212I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2212 Limits		X2212I Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	Power Supply Current		60		70	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Load Current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +1.0	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −2 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	10,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	100,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

Inputs				Input Output I/O	Mode
$\overline{CS}$	$\overline{WE}$	ARRAY RECALL	$\overline{STORE}$		
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(4)
H	X	H	L	Output High Z	Nonvolatile Storing(4)

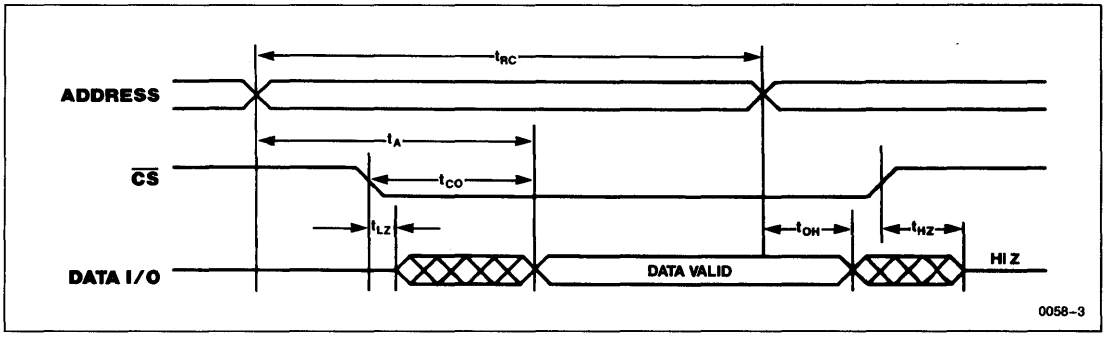
A.C. CHARACTERISTICS

X2212 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2212I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	300		ns
t_A	Access Time		300	ns
t_{CO}	Chip Select to Output Valid		200	ns
t_{OH}	Output Hold from Address Change	50		ns
t_{LZ}(5)	Chip Select to Output in Low Z	10		ns
t_{HZ}(5)	Chip Deselect to Output in High Z	10	100	ns

Read Cycle

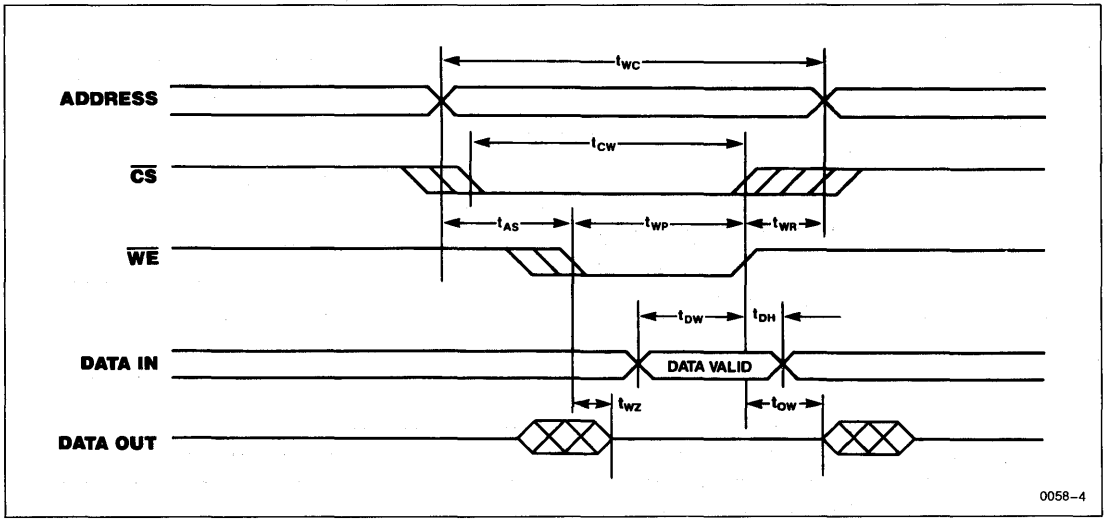


Notes: (3) Chip is deselected but may be automatically completing a store cycle.
(4) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).
(5) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

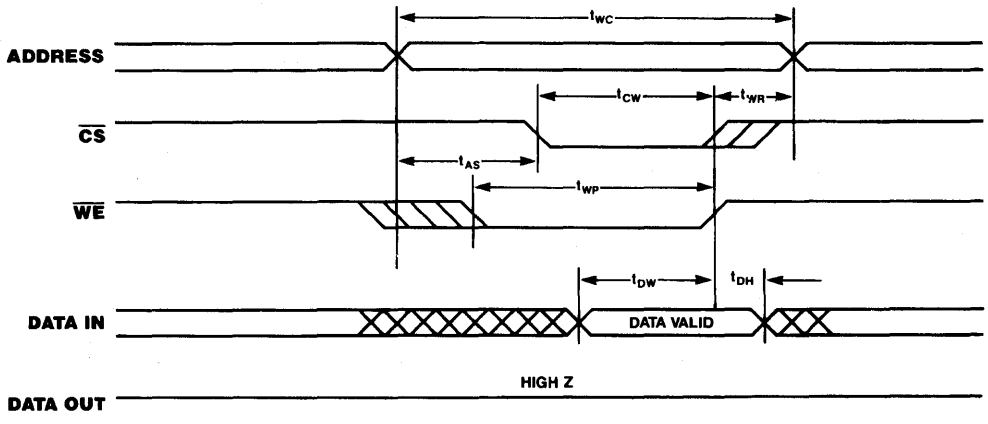
Write Cycle Limits

Symbol	Parameter		Min.	Max.	Units
t_{WC}	Write Cycle Time		300		ns
t_{CW}	Chip Select to End of Write		150		ns
t_{AS}	Address Setup Time		50		ns
t_{WP}	Write Pulse Width		150		ns
t_{WR}	Write Recovery Time		25		ns
t_{DW}	Data Valid to End of Write		100		ns
t_{DH}	Data Hold Time	X2212	0		ns
		X2212I	20		ns
t_{WZ}	Write Enable to Output in High Z		10	100	ns
t_{OW}	Output Active from End of Write		10		ns

Write Cycle



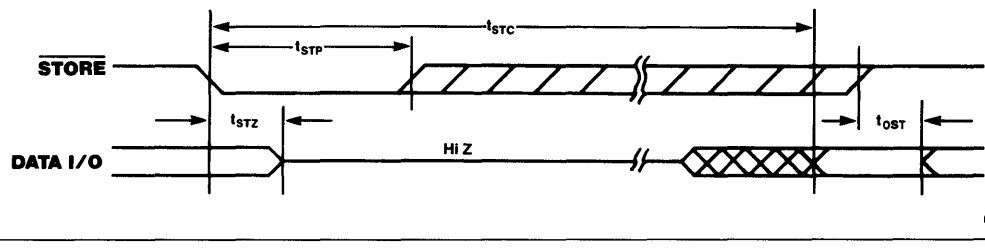
Early Write Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Store Time		10	ms
t_{STP}	Store Pulse Width	100		ns
t_{STZ}	Store to Output in High Z		500	ns
t_{OST}	Output Active from End of Store	10		ns

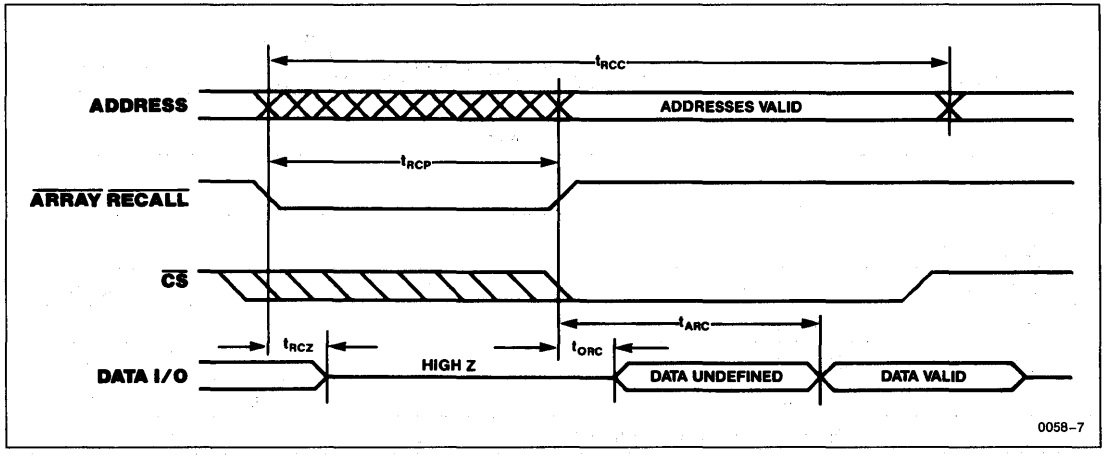
Store Cycle



Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Cycle Time	1200		ns
t_{RCP}	Recall Pulse Width(6)	450		ns
t_{RCZ}	Recall to Output in High Z		150	ns
t_{ORC}	Output Active from End of Recall	10		ns
t_{ARC}	Recalled Data Access Time from End of Recall		750	ns

Array Recall Cycle



Note: (6) Array Recall rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_7)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read/write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. $\overline{WE}$ HIGH enables a read and $\overline{WE}$ LOW enables a write.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X2212 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and $\overline{ARRAY\ RECALL}$ inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM.

$\overline{ARRAY\ RECALL}$

The $\overline{ARRAY\ RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{ARRAY\ RECALL}$ is asserted. $\overline{ARRAY\ RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

WRITE PROTECTION

The X2212 has three write protect features that are employed to protect the contents of the nonvolatile memory.

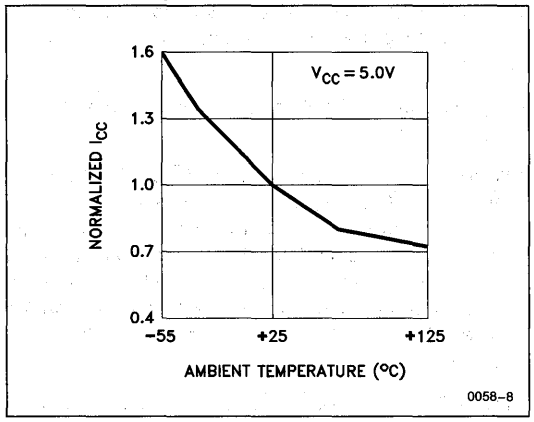
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{ARRAY\ RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained. It should be noted; whichever method is employed, all control inputs should be stable and the device deselected prior to release of the controlling protection signal.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns (typical) will *not* initiate a store cycle.

Part Number	Store Cycles	Data Changes Per Bit
X2212 X2212I	10,000	1,000
X2212/5 X2212I/5	50,000	5,000
X2212/10 X2212I/10	100,000	10,000

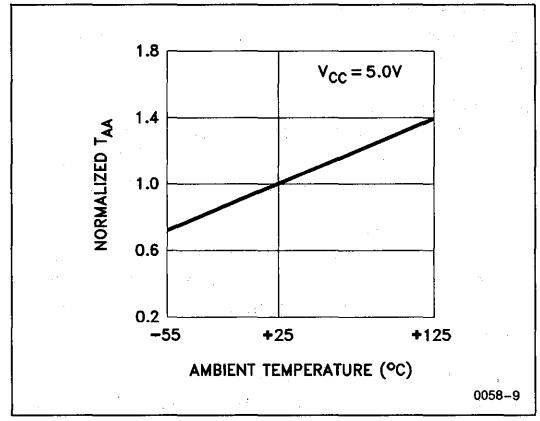
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Normalized Active Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **JEDEC Standard 18-Pin Package**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 250 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **100 Year Data Retention**

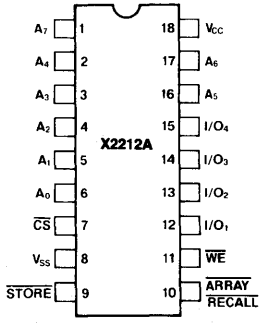
DESCRIPTION

The Xicor X2212A is a 256 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2212A is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories. The X2212A features the JEDEC approved pinout for 4-bit-wide memories, compatible with industry standard RAMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

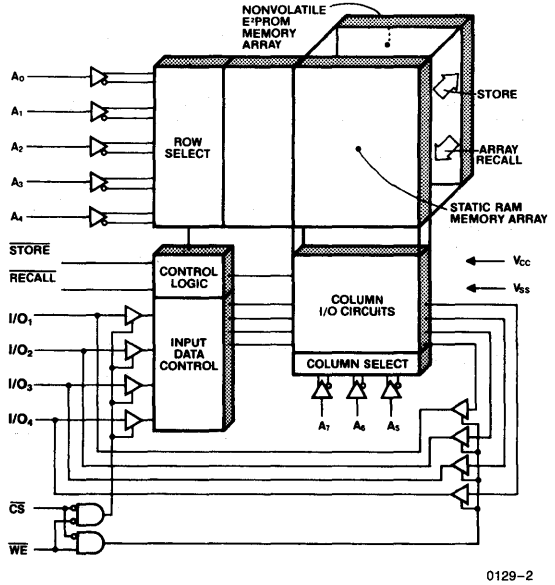


0129-1

PIN NAMES

A_0–A_7	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0129-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	Power Supply Current		60	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Load Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

Inputs				Input Output I/O	Mode
$\overline{CS}$	$\overline{WE}$	ARRAY $\overline{RECALL}$	$\overline{STORE}$		
H	X	H	H	Output High Z	Not Selected(2)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(3)
H	X	H	L	Output High Z	Nonvolatile Storing(3)

Notes: (1) This parameter is periodically sampled and not 100% tested.

(2) Chip is deselected but may be automatically completing a store cycle.

(3) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).

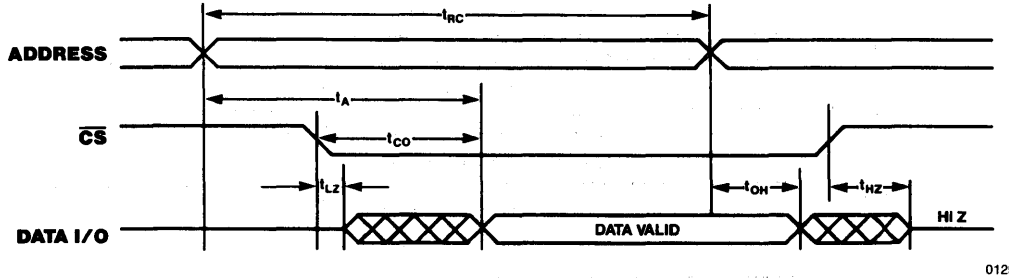
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Select to Output Valid		200	ns
t_{OH}	Output Hold from Address Change	50		ns
t_{LZ}	Chip Select to Output in Low Z	10		ns
t_{HZ}	Chip Deselect to Output in High Z	10	100	ns

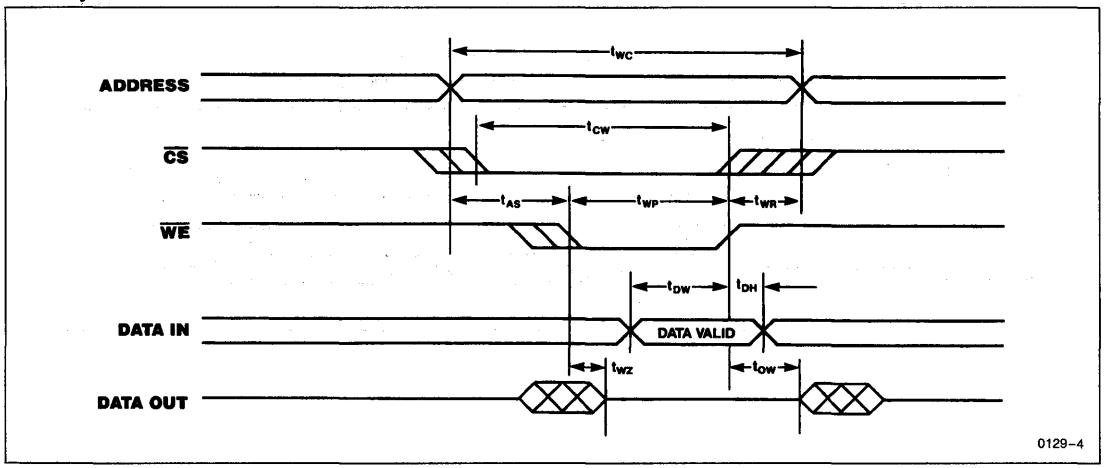
Read Cycle



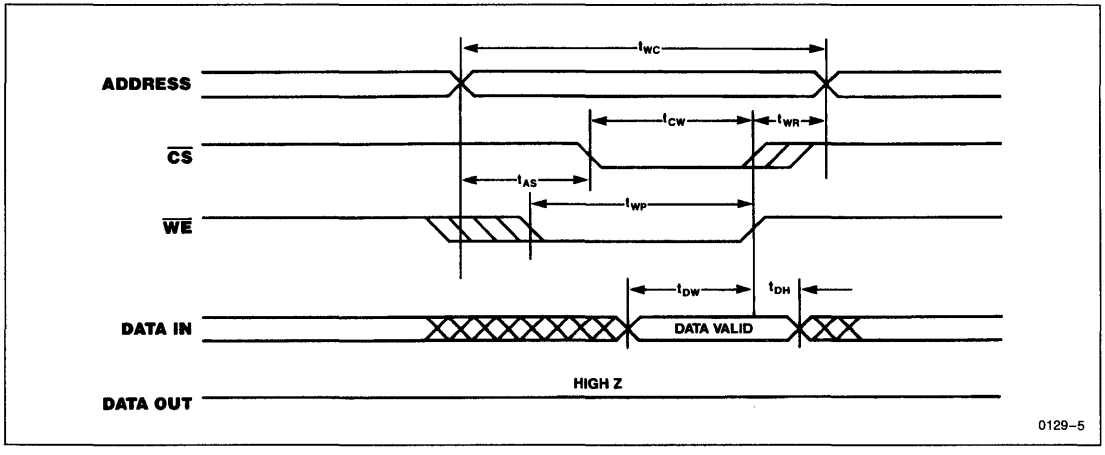
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	250		ns
t_{CW}	Chip Select to End of Write	150		ns
t_{AS}	Address Setup Time	50		ns
t_{WP}	Write Pulse Width	150		ns
t_{WR}	Write Recovery Time	25		ns
t_{DW}	Data Valid to End of Write	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	ns
t_{OW}	Output Active from End of Write	10		ns

Write Cycle



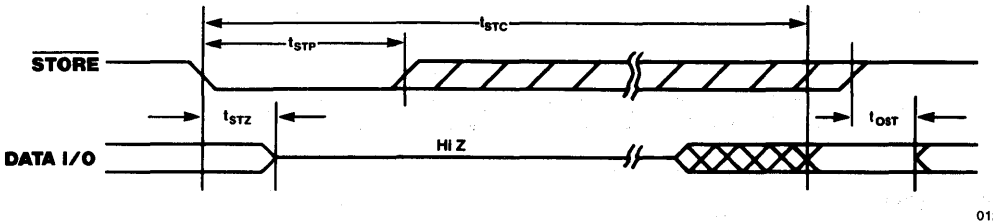
Early Write Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Store Cycle Time		10	ms
t_{STP}	Store Pulse Width	100		ns
t_{STZ}	Store to Output in High Z		500	ns
t_{OST}	Output Active from End of Store	10		ns

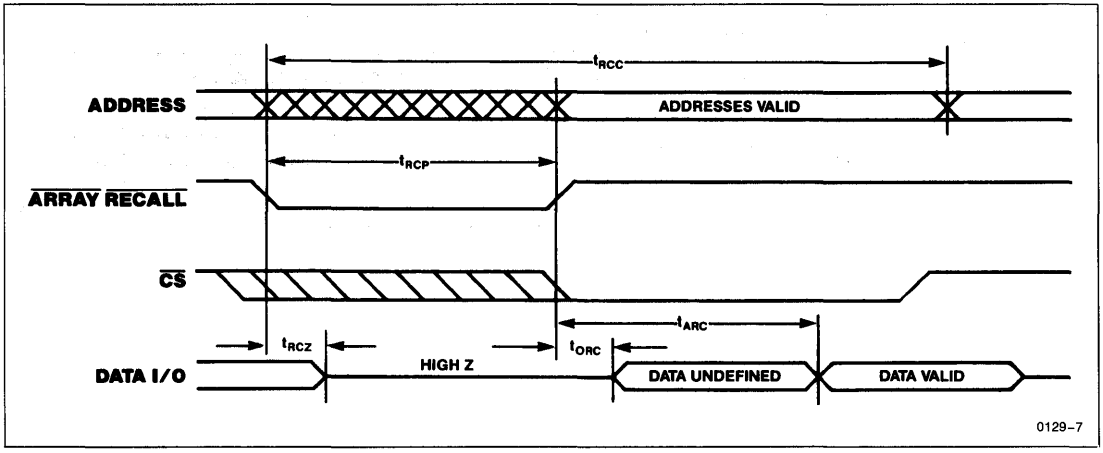
Store Cycle



Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Cycle Time	1200		ns
t_{RCP}	Recall Pulse Width(4)	450		ns
t_{RCZ}	Recall to Output in High Z		150	ns
t_{ORC}	Output Active from End of Recall	10		ns
t_{ARC}	Recalled Data Access Time from End of Recall		750	ns

Array Recall Cycle



Note: (4) Array Recall rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_7)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read/write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. $\overline{WE}$ HIGH enables a read and $\overline{WE}$ LOW enables a write.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X2212A through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E^2PROM array. The $\overline{WE}$ and $\overline{ARRAY\ RECALL}$ inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E^2PROM.

$\overline{ARRAY\ RECALL}$

The $\overline{ARRAY\ RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E^2PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{ARRAY\ RECALL}$ is asserted. $\overline{ARRAY\ RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

WRITE PROTECTION

The X2212A has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E^2PROM data integrity will be maintained.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns will *not* initiate a store cycle.

ENDURANCE

The endurance specification of a device is characterized by the predicted *first* bit failure to occur in the entire memory (device or system) array rather than the average or typical value for the array. Since endurance is limited by the number of electrons trapped in the oxide during data changes, Xicor NOVRAMs are designed to minimize the number of changes an E^2PROM bit cell undergoes during store operations. Only those bits in the E^2PROM that are different from their corresponding location in the RAM will be "cycled" during a nonvolatile store. This characteristic reduces unnecessary cycling of any of the rest of the bits in the array, thereby increasing the potential endurance of each bit and increasing the potential endurance of the entire array. Reliability data documented in RR-504, the *Xicor Reliability Report on Endurance*, and additional reports are available from Xicor.

Part Number	Store Cycles	Data Changes Per Bit
X2212A	10,000	1,000

NOTES

256 Bit Commercial Industrial X22C10 X22C10I 64 x 4 Bit

Nonvolatile Static RAM

FEATURES

- 100% Compatible with X2210
  - —With Timing Enhancements
- Infinite Array Recall, RAM Read and Write Cycles
- High Reliability
  - —Store Cycles: 1,000,000
  - —Data Retention: 100 Years
- High Performance CMOS
  - —120 ns RAM Access Time
  - —Low Power Consumption
    - Active: 40 mA Max.
    - Standby: 100 μA Max.
- Nonvolatile Store Inhibit: V_{CC} = 3.5V Typ
- Fully TTL and CMOS Compatible
- JEDEC Standard 18-Pin 300-mil DIP

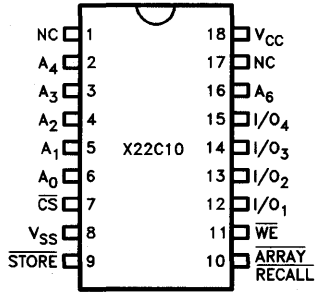
DESCRIPTION

The X22C10 is a 64 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E^2PROM. The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (STORE) and from E^2PROM to RAM (RECALL). The STORE operation is completed within 10 ms or less and the RECALL is typically completed within 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to the RAM, either RECALLs from E^2PROM or writes from the host. The X22C10 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years. Refer to RR-515, RR-504 and RR-520 for details of data retention and endurance characteristics for Xicor nonvolatile memories.

PIN CONFIGURATION

PLASTIC DIP
CERDIP



0123-1

PIN NAMES

A_0–A_5	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X22C10I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Supply Current, RAM Read/Write		40	mA	$\overline{CS}$ = V_{IL}, I/Os = Open, All Others = V_{IH}, Addresses = TTL Levels @ f = 5 MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		2	mA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		100	µA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V_{CC} −0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(4)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(4)	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2.0 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CS}$	WE	$\overline{RECALL}$	$\overline{STORE}$	I/O	Mode
H	X	H	H	Output High Z	Not Selected(2)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(3)
H	X	H	L	Output High Z	Nonvolatile Storing(3)

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) Chip is deselected but may be automatically completing a store cycle.
(3) $\overline{STORE}$ = LOW is required only to initiate the store cycle, after which the store cycle will be automatically completed (e.g. $\overline{STORE}$ = X).
(4) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	100,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	1,000,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

POWER-UP TIMING(5)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	100	μs
t_{PUW}	Power-Up to Write or Store Operation	5	ms

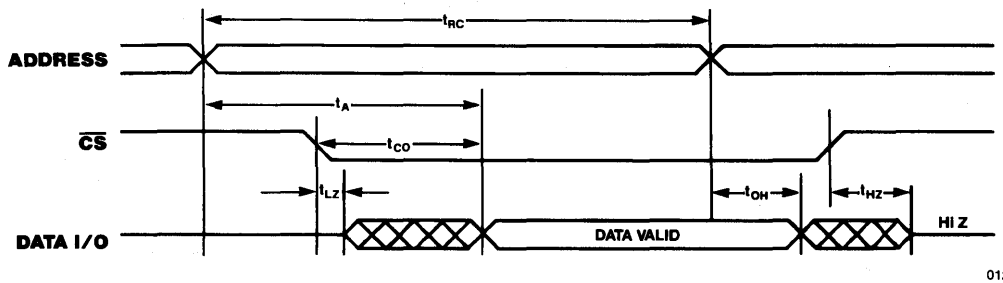
A.C. CHARACTERISTICS

X22C10 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X22C10I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	150		ns
t_{AA}	Access Time		150	ns
t_{CO}	Chip Select to Output Valid		150	ns
t_{OH}	Output Hold from Address Change	0		ns
t_{LZ}	Chip Select to Output in Low Z	0		ns
t_{HZ}	Chip Deselect to Output in High Z		50	ns

Read Cycle

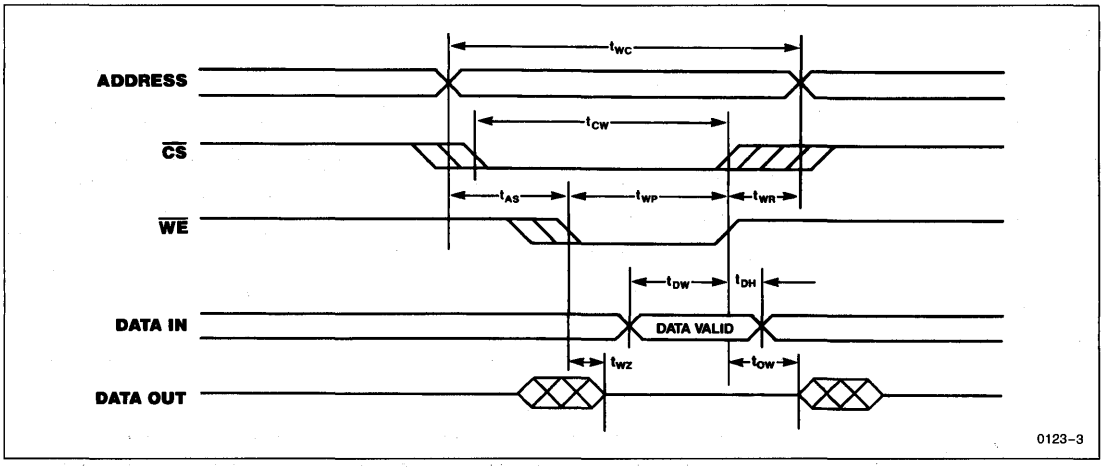


Note: (5) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

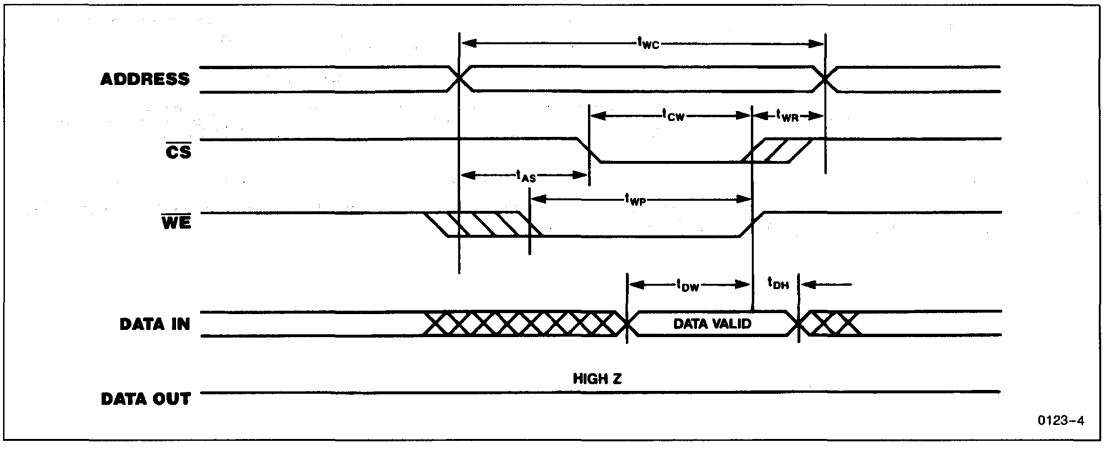
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	150		ns
t_{CW}	Chip Select to End of Write	90		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{WR}	Write Recovery Time	0		ns
t_{DW}	Data Valid to End of Write	40		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z	0	50	ns
t_{OW}	Output Active from End of Write	0		ns

Write Cycle



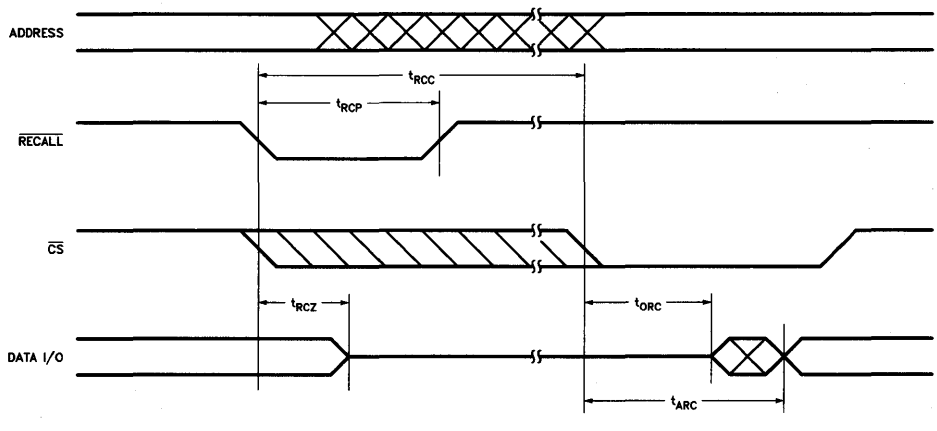
Early Write Cycle



Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Time		1200	ns
t_{RCP}	Recall Pulse Width(6)	90		ns
t_{RCZ}	Recall to Output in High Z		50	ns
t_{ORC}	Output Active from End of Recall	0		ns
t_{ARC}	Recalled Data Access Time from End of Recall		150	ns

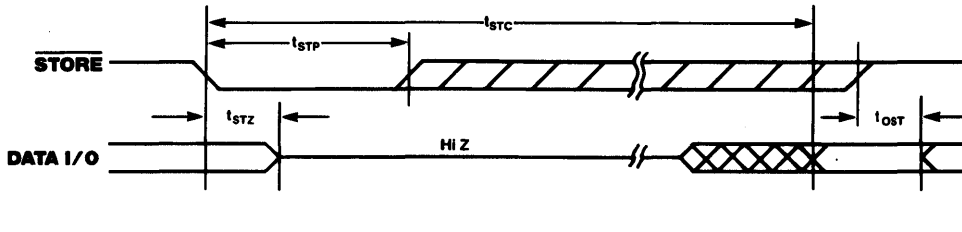
Array Recall Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Internal Store Time		10	ms
t_{STP}	Store Pulse Width	90		ns
t_{STZ}	Store to Output in High Z		50	ns
t_{OST}	Output Active from End of Store	0		ns

Store Cycle



Note: (6) RECALL rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_5)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read or write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH the I/O pins will output data from the selected RAM address location. When both $\overline{CS}$ and $\overline{WE}$ are LOW, data presented at the I/O pins will be written to the selected address location.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X22C10 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and RECALL inputs are inhibited during the store cycle. The store operation is completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM arrays.

$\overline{RECALL}$

The RECALL input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{RECALL}$ is asserted. $\overline{RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

AUTOMATIC RECALL

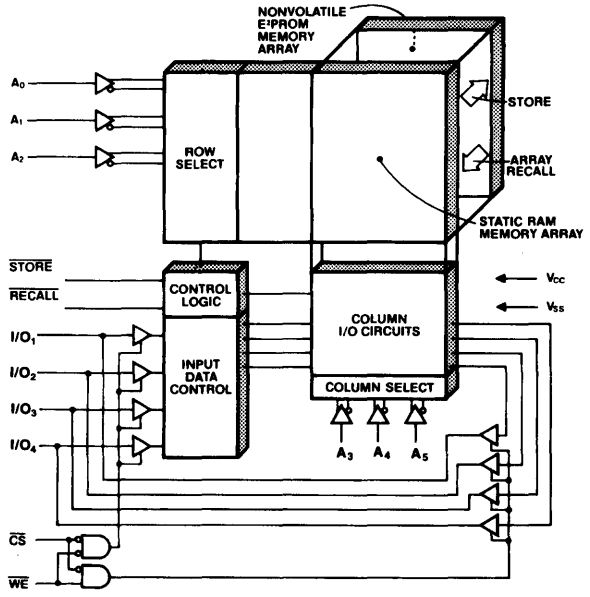
Upon power-up the X22C10 will automatically recall data from the E²PROM array into the RAM array.

WRITE PROTECTION

The X22C10 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V_{CC} Sense—All functions are inhibited when V_{CC} is <3.5V.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns will *not* initiate a store cycle.

FUNCTIONAL DIAGRAM



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

NOTES

FACT SHEET

256 Bit Commercial Industrial X22C11 X22C11I 64 x 4 Bit

Nonvolatile Static RAM

1

FEATURES

- **Autostore™**
  - **—Automatically Stores Data Upon Detection of Power Loss**
- **Store-Lock™**
  - **—Software Enabled Store Lockout**
- **100% Compatible with X2210 and X22C10**
  - **—With Timing Enhancements**
- **Infinite Array Recall, RAM Read and Write Cycles**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**
- **High Performance CMOS**
  - **—120 ns RAM Access Time**
  - **—Low Power Consumption**
    - **Active: 40 mA Max.**
    - **Standby: 100 μA Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3.5V Typ**
- **Fully TTL and CMOS Compatible**
- **JEDEC Standard 18-Pin 300-mil DIP**

DESCRIPTION

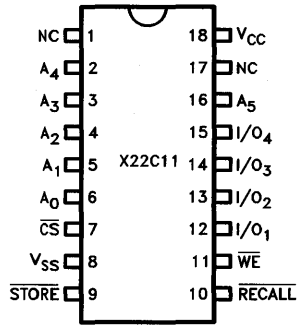
The X22C11 is a 64 x 4 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E^2PROM. The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (STORE) and from E^2PROM to RAM (RECALL). The STORE operation is completed within 10 ms or less and the RECALL is typically completed within 1 μs.

In addition, the X22C11 features Autostore and Store-Lock. Autostore is a user selectable option that will automatically perform a Store operation when power is removed from the X22C11. Store-Lock will lockout all inadvertent store conditions.

Xicor NOVRAMs are designed for unlimited write operations to the RAM; either RECALLs from E^2PROM or writes from the host. The X22C11 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years. Refer to RR-515, RR-504 and RR-520 for details of data retention and endurance characteristics for Xicor nonvolatile memories.

PIN CONFIGURATION

PLASTIC DIP
CERDIP



0124-1

PIN NAMES

A_0–A_5	Address Inputs
I/O_1–I/O_4	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_5)

The address inputs select a 4-bit memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read or write operations with the RAM array. $\overline{CS}$ HIGH will place the I/O pins in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When $\overline{CS}$ is LOW and $\overline{WE}$ is HIGH, the I/O pins will output data from the selected RAM address location. When both $\overline{CS}$ and $\overline{WE}$ are LOW, data presented at the I/O pins will be written to the selected address location.

Data In/Data Out (I/O_1–I/O_4)

Data is written to or read from the X22C11 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CS}$ is HIGH or during either a store or recall operation.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and $\overline{RECALL}$ inputs are inhibited during the store cycle. The store operation is completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM arrays.

$\overline{RECALL}$

The $\overline{RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{RECALL}$ is asserted. $\overline{RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

Automatic Recall

Upon power-up the X22C11 will automatically recall data from the E²PROM array into the RAM array.

Store-Lock

Store-Lock will lockout all attempts to store data from the RAM array into the E²PROM array unless the Store Enable Latch has been set by the user. This feature can eliminate the need for any external power-up/power-down inadvertent store circuits.

The X22C11 is always in the store lockout mode. In order to enable a store operation the user must first bring $\overline{RECALL}$ high and $\overline{STORE}$ low, then write a two byte command sequence to the X22C11 and then bring $\overline{STORE}$ high. The X22C11 is now ready to store data the next time $\overline{STORE}$ is strobed low. After each valid store operation, the Store Enable Latch is reset, protecting the data. A power-up condition will reset the latch regardless of its state prior to power-down.

Autostore

Autostore will automatically store data from the RAM array into the E²PROM array after detecting V_{CC} has fallen below the Autostore threshold. The Autostore Enable Latch is enabled by first bringing $\overline{RECALL}$ high and $\overline{STORE}$ low, then writing a two byte command sequence to the X22C11 and then bringing $\overline{STORE}$ high. At this point the X22C11 is "armed" to perform an autostore operation. The Autostore Enable Latch will be reset upon power-up.

Nonvolatile Static RAM

FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **High Reliability**
  - **—Store Cycles: 100,000**
  - **—Data Retention: 100 Years**
- **Fast Access Time: 200 ns Max.**
- **Automatic Recall on Power-Up**
- **JEDEC Approved Byte-Wide Pinout**

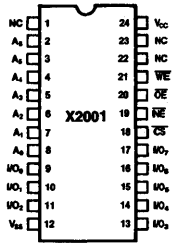
DESCRIPTION

The Xicor X2001 is a byte-wide NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X2001 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2001 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E²PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 100,000 store operations to the E²PROM. Inherent data retention is specified to be greater than 100 years. Refer to RR-520, RR-504 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATION

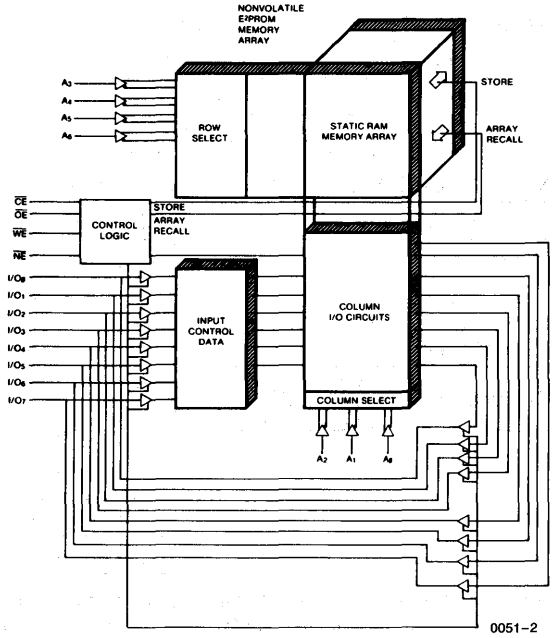


0051-1

PIN NAMES

A_0–A_6	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0051-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2001 ..... −10°C to +85°C
X2001I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2001 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2001I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2001 Limits		X2001I Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		80		100	mA	$\overline{CE}$ = V_{IL}, All Other Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{SB}	V_{CC} Current (Standby)		50		65	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Leakage Current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 µA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	10,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	100,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

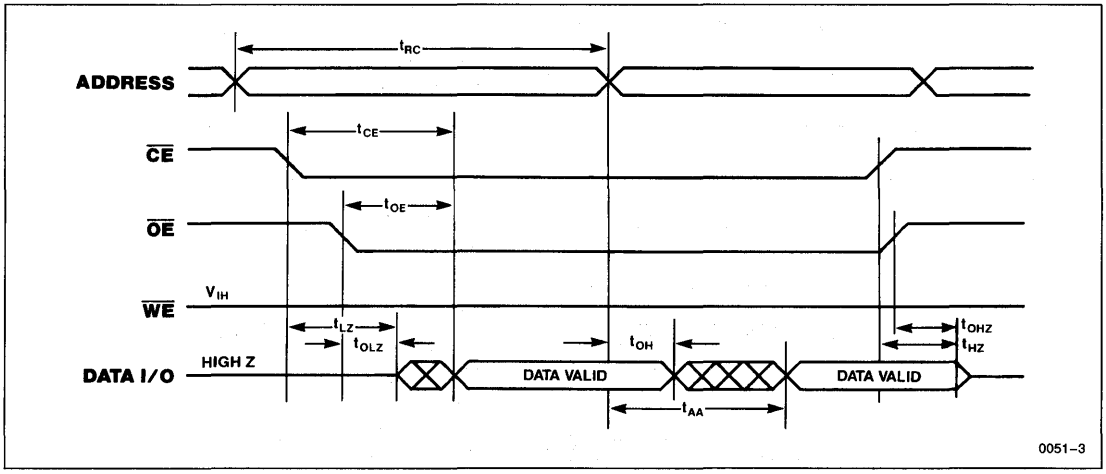
A.C. CHARACTERISTICS

X2001 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2001I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		70		100		150	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	10		10		10		ns
t_{HZ}(3)	Chip Disable to Output in High Z	10	100	10	100	10	100	ns
t_{OLZ}(3)	Output Enable to Output in Low Z	10		10		10		ns
t_{OHZ}(3)	Output Disable to Output in High Z	10	100	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Read Cycle

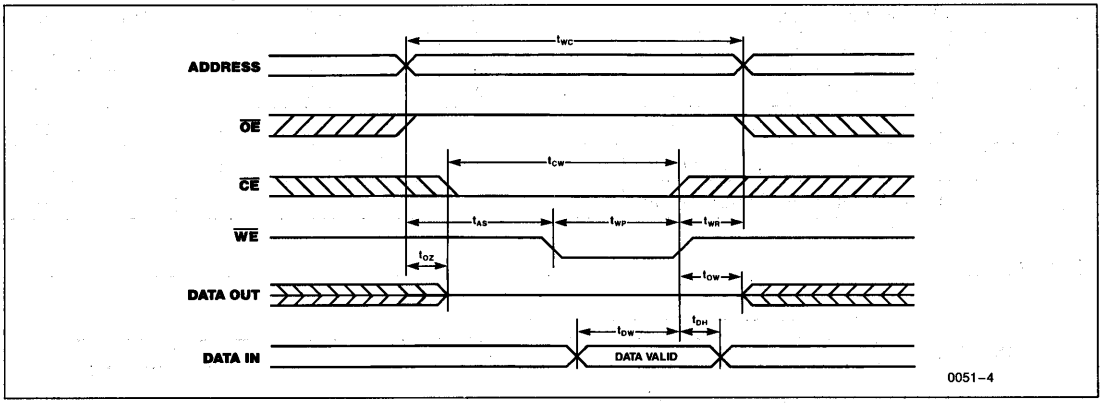


Note: (3) t_{LZ} min., t_{HZ} min., t_{OLZ} min. and t_{OHZ} min. are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

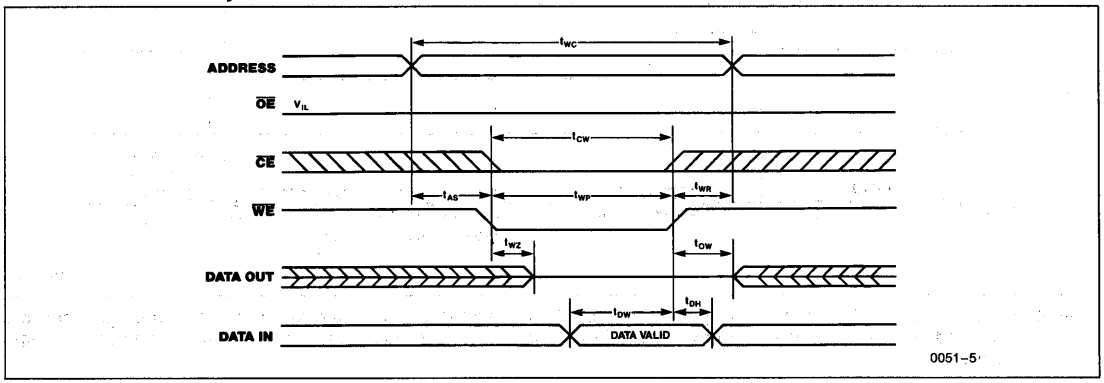
Write Cycle Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	200		250		300		ns
t_{CW}	Chip Enable to End of Write Input	200		250		300		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	120		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	120		150		200		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	10	100	10	100	ns
t_{OW}	Output Active from End of Write	10		10		10		ns
t_{OZ}	Output Enable to Output in High Z	10	100	10	100	10	100	ns

$\overline{WE}$ Controlled Write Cycle



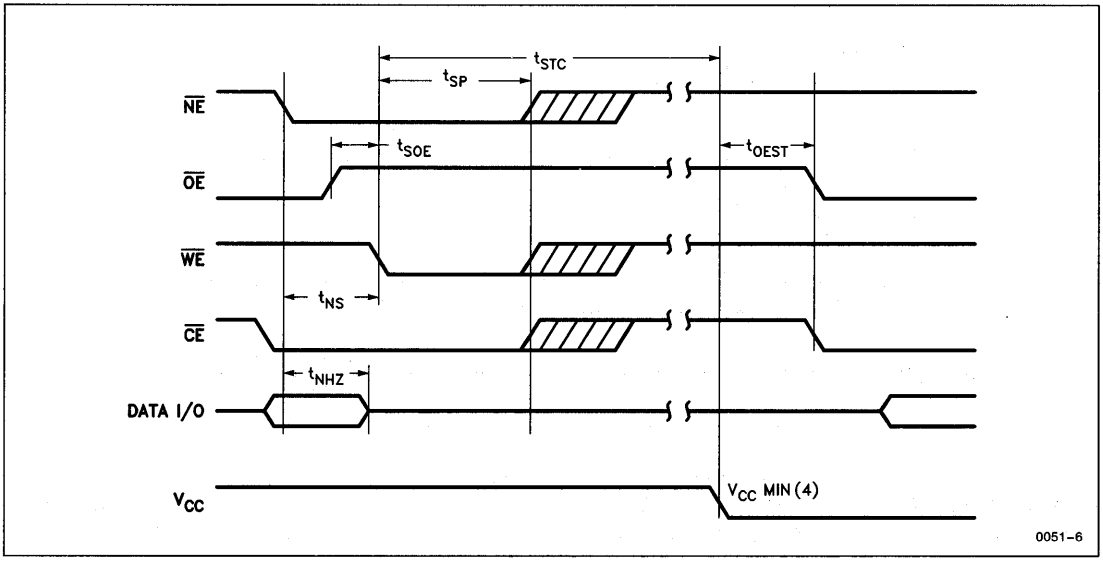
$\overline{CE}$ Controlled Write Cycle



Store Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STC}	Store Time		10		10		10	ms
t_{SP}	Store Pulse Width	120		150		200		ns
t_{NHZ}	Nonvolatile Enable to Output in High Z		100		100		100	ns
t_{OEST}	Output Enable from End of Store	10		10		10		ns
t_{SOE}	$\overline{OE}$ Disable to Store Function	20		20		20		ns
t_{NS}	$\overline{NE}$ Setup Time from $\overline{WE}$	0		0		0		ns

Store Timing



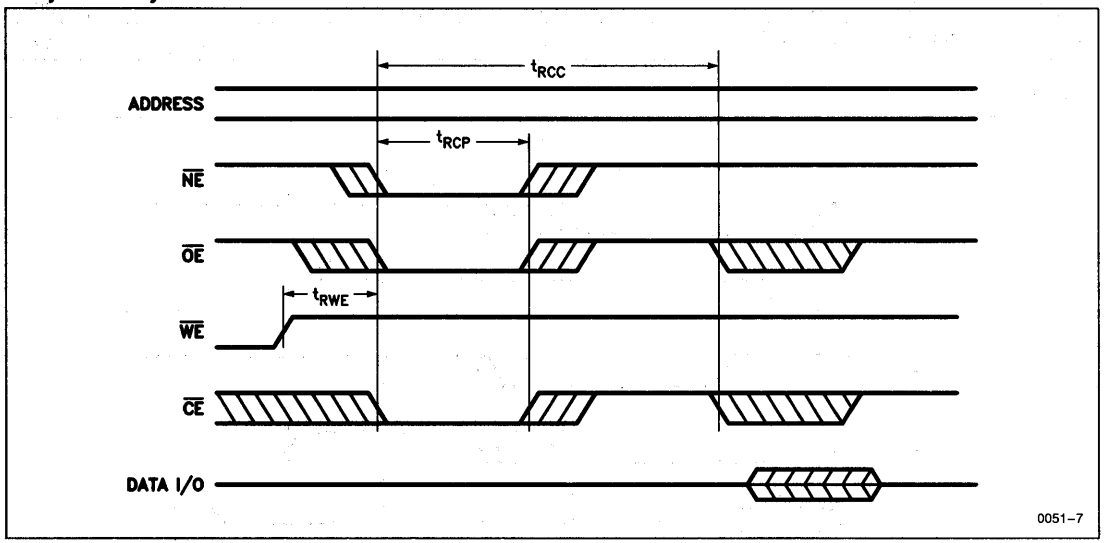
Note: (4) X2001 V_{CC} Min. = 4.75V
X2001I V_{CC} Min. = 4.5V

The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must return HIGH after initiation of and throughout the duration (t_{STC}, 10 ms) of the Store operation. During t_{STC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host system access to other devices in the system.

Array Recall Cycle Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Time		5.0		5.0		5.0	μs
t_{RCP}	Recall Pulse Width to Initiate Recall	120		150		200		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns

Array Recall Cycle



The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must return HIGH after initiation of and through the duration (t_{RCC}, 5 μs) of the Recall operation. During t_{RCC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host access to other devices in the system.

PIN DESCRIPTIONS

Addresses (A_0–A_6)

The address inputs select an 8-bit word during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$ or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2001 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to both the static RAM and stores to the E^2PROM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls all accesses to the E^2PROM array (store and recall functions).

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X2001 operation. The X2001 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM OPERATIONS

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X2001.

NONVOLATILE OPERATIONS

With $\overline{NE}$ LOW, recall and store operations are performed in the same manner as RAM read and write operations. A recall operation causes the entire contents of the E^2PROM to be written into the RAM array. The time required for the operation to complete is 5 μs or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E^2PROM. The time for the operation to complete is 10 ms or less, typically 5 ms.

POWER-UP RECALL

Upon power-up (V_{CC}), the X2001 performs an automatic array recall. When V_{CC} minimum is reached, the recall is initiated, regardless of the state of $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$.

WRITE PROTECTION

The X2001 has three write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

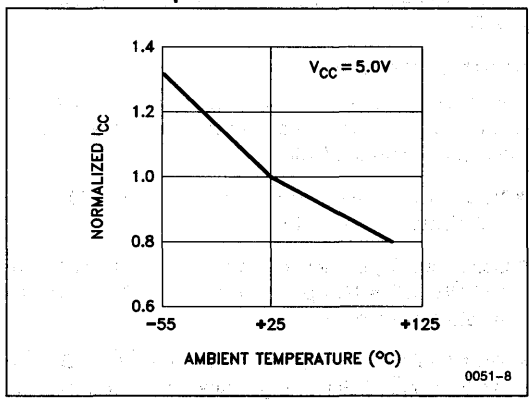
- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will *not* initiate a write cycle.
- Combined Signal Noise Protection—A combined $\overline{WE}$ and $\overline{NE}$ ($\overline{WE} \bullet \overline{NE}$) pulse of less than 20 ns will *not* initiate a store cycle.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, $\overline{CE}$ HIGH or $\overline{NE}$ HIGH during power-up or power-down, will prevent an inadvertent store operation.

Part Number	Store Cycles	Data Changes Per Bit
X2001	100,000	10,000
X2001I	100,000	10,000

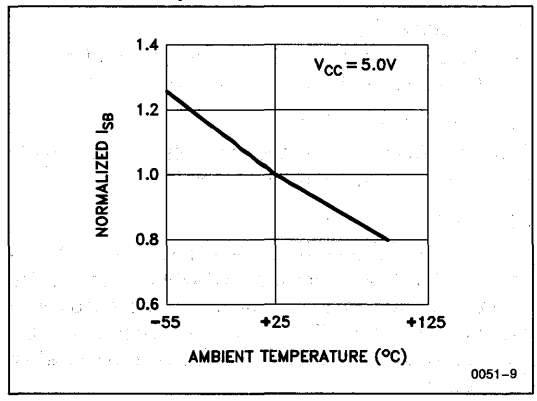
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

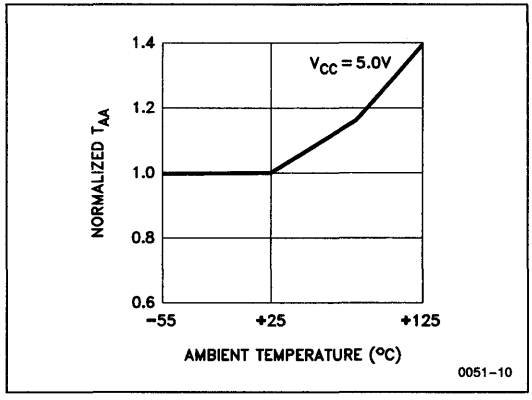
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



Nonvolatile Static RAM

FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E²PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **High Reliability**
  - **—Store Cycles: 100,000**
  - **—Data Retention: 100 Years**
- **Fast Access Time: 200 ns Max.**
- **Automatic Recall on Power-Up**
- **JEDEC Approved Byte-Wide Pinout**

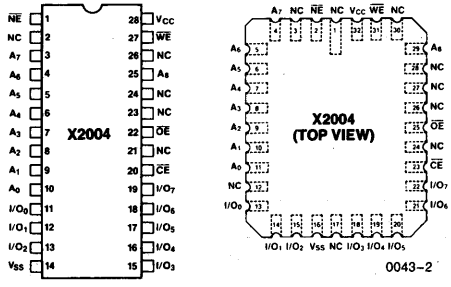
DESCRIPTION

The Xicor X2004 is a byte-wide NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E²PROM). The X2004 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2004 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E²PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and E²PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM, and a minimum 100,000 store operations to the E²PROM. Data retention is specified to be greater than 100 years. Refer to RR-520, RR-504 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATIONS



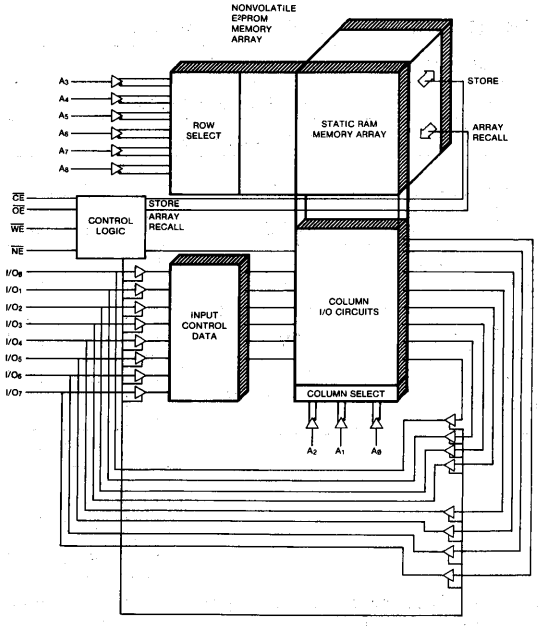
0043-1

0043-2

PIN NAMES

A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0043-3

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2004 ..... −10°C to +85°C
X2004I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2004 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2004I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2004 Limits		X2004I Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		100		120	mA	$\overline{CE}$ = V_{IL}, All Other Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{SB}	V_{CC} Current (Standby)		55		90	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Leakage Current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 µA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	10,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	100,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

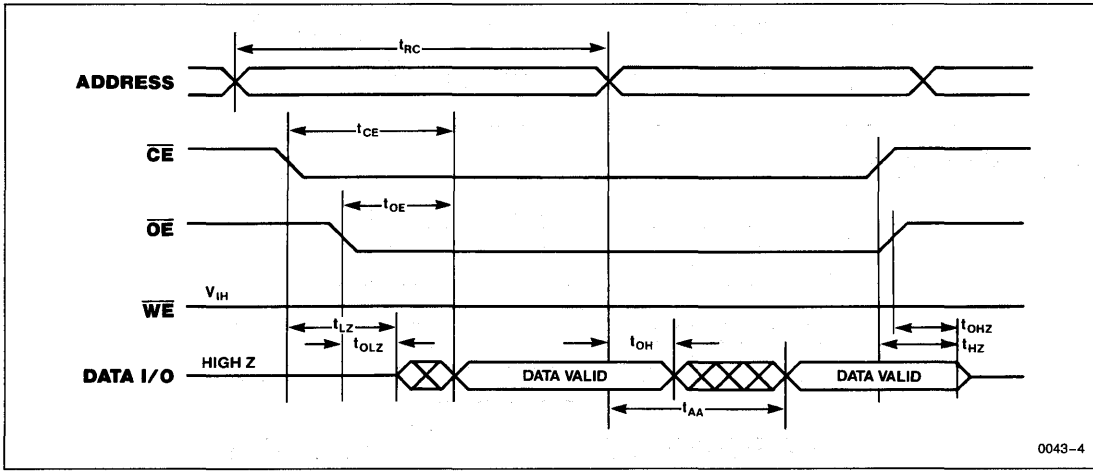
A.C. CHARACTERISTICS

X2004 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2004I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2004-20 X2004I-20		X2004-25 X2004I-25		X2004 X2004I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		70		100		150	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	10		10		10		ns
t_{HZ}(3)	Chip Disable to Output in High Z	10	100	10	100	10	100	ns
t_{OLZ}(3)	Output Enable to Output in Low Z	10		10		10		ns
t_{OHZ}(3)	Output Disable to Output in High Z	10	100	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Read Cycle

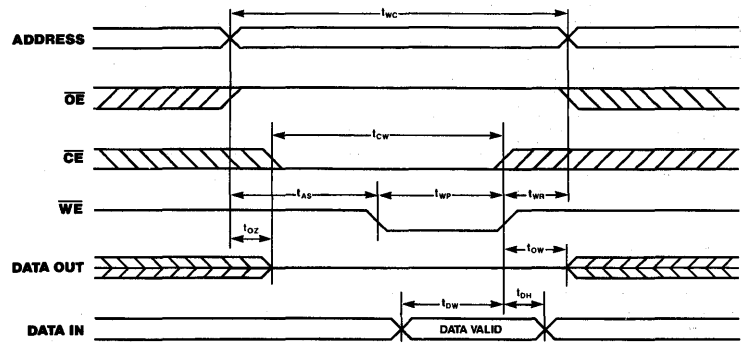


Note: (3) t_{LZ} min., t_{HZ} min., t_{OLZ} min. and t_{OHZ} min. are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

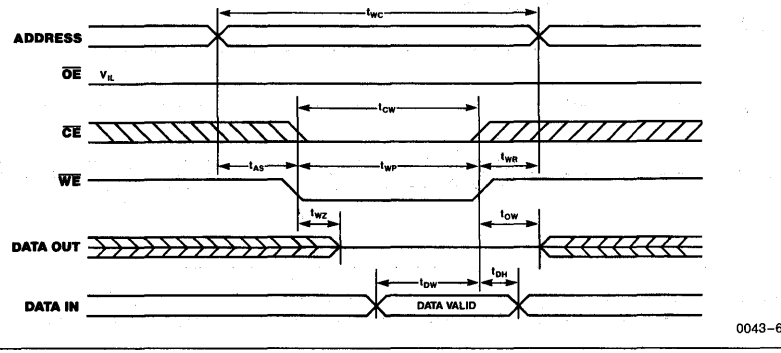
Write Cycle Limits

Symbol	Parameter	X2004-20 X2004I-20		X2004-25 X2004I-25		X2004 X2004I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	200		250		300		ns
t_{CW}	Chip Enable to End of Write Input	200		250		300		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	120		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	120		150		200		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	10	100	10	100	ns
t_{OW}	Output Active from End of Write	10		10		10		ns
t_{OZ}	Output Enable to Output in High Z	10	100	10	100	10	100	ns

$\overline{WE}$ Controlled Write Cycle



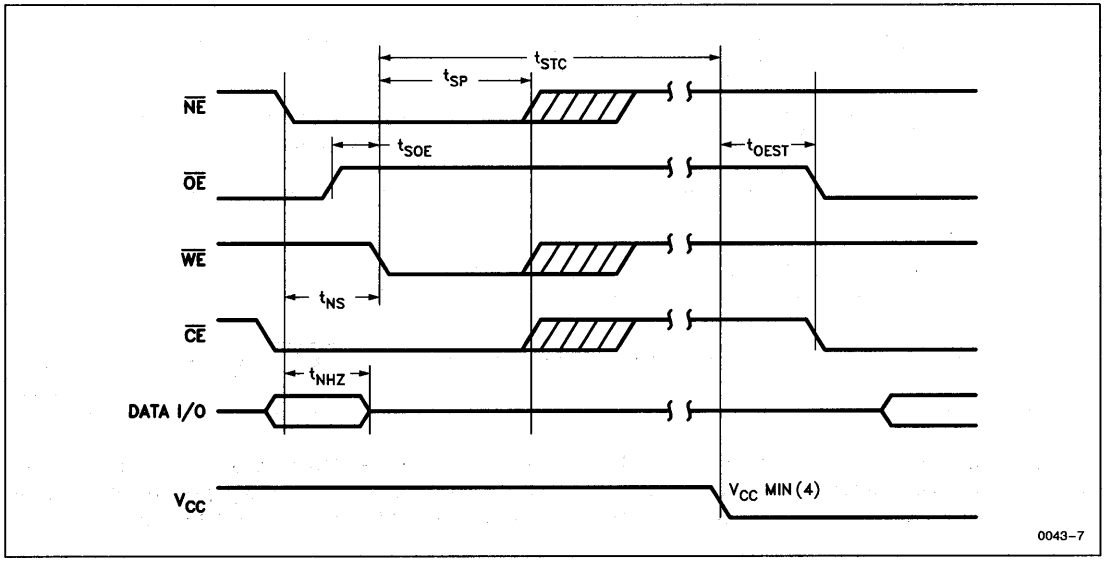
$\overline{CE}$ Controlled Write Cycle



Store Limits

Symbol	Parameter	X2004-20 X2004I-20		X2004-25 X2004I-25		X2004 X2004I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STC}	Store Time		10		10		10	ms
t_{SP}	Store Pulse Width	120		150		200		ns
t_{NHZ}	Nonvolatile Enable to Output in High Z		100		100		100	ns
t_{OEST}	Output Enable from End of Store	10		10		10		ns
t_{SOE}	$\overline{OE}$ Disable to Store Function	20		20		20		ns
t_{NS}	$\overline{NE}$ Setup Time from $\overline{WE}$	0		0		0		ns

Store Timing



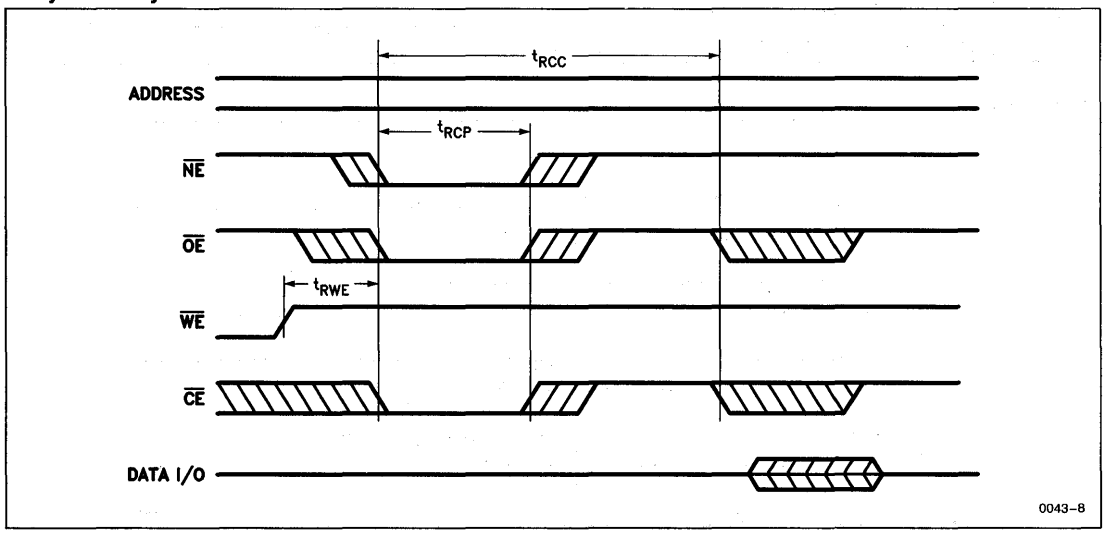
Note: (4) X2004 V_{CC} Min. = 4.75V
X2004I V_{CC} Min. = 4.5V

The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must return HIGH after initiation of and throughout the duration (t_{STC}, 10 ms) of the Store operation. During t_{STC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host system access to other devices in the system.

Array Recall Cycle Limits

Symbol	Parameter	X2004-20 X2004I-20		X2004-25 X2004I-25		X2004 X2004I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Time		5.0		5.0		5.0	μs
t_{RCP}	Recall Pulse Width to Initiate Recall	120		150		200		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns

Array Recall Cycle



The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must return HIGH after initiation of and through the duration (t_{RCC}, 5 μs) of the Recall operation. During t_{RCC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host access to other devices in the system.

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The address inputs select an 8-bit word during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$ or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2004 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to both the static RAM and stores to the E^2PROM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls all accesses to the E^2PROM array (store and recall functions).

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X2004 operation. The X2004 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM OPERATIONS

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X2004.

NONVOLATILE OPERATIONS

With $\overline{NE}$ LOW, recall and store operations are performed in the same manner as RAM read and write operations. A recall operation causes the entire contents of the E^2PROM to be written into the RAM array. The time required for the operation to complete is 5 μs or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E^2PROM. The time for the operation to complete is 10 ms or less, typically 5 ms.

POWER-UP RECALL

Upon power-up (V_{CC}), the X2004 performs an automatic array recall. When V_{CC} minimum is reached, the recall is initiated, regardless of the state of $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$.

WRITE PROTECTION

The X2004 has four write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

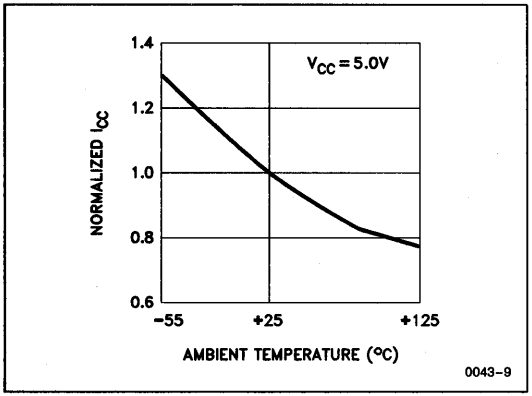
- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will *not* initiate a write cycle.
- Combined Signal Noise Protection—A combined $\overline{WE}$ and $\overline{NE}$ ($\overline{WE} \bullet \overline{NE}$) pulse of less than 20 ns will *not* initiate a store cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$2V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, $\overline{CE}$ HIGH or $\overline{NE}$ HIGH during power-up or power-down, will prevent an inadvertent store operation.

Part Number	Store Cycles	Data Changes Per Bit
X2004	100,000	10,000
X2004I	100,000	10,000

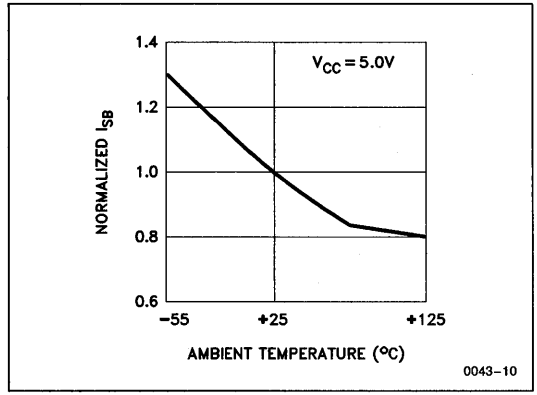
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

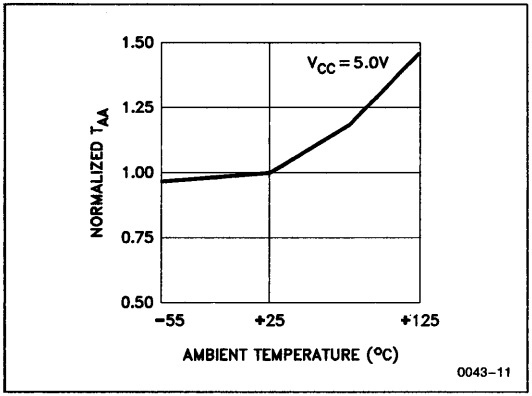
Normalized Active Supply Current vs. Ambient Temperature



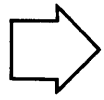
Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature

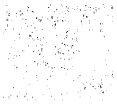


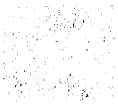
X2444, X2444I 2-1
X24C44, X24C44I 2-11
X24C45, X24C45I 2-19
X2402, X2402I 2-23
X2404, X2404I 2-33
X24C01, X24C01I 2-43
X24C02, X24C02I 2-53
X24C04, X24C04I 2-63
X24C16, X24C16I 2-73



NOVRAM* Data Sheets 1

Serial Products Data Sheets 2





Nonvolatile Static RAM

FEATURES

- **Ideal for use with Single Chip Microcomputers**
  - **—Static Timing**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaces to Microcontroller Ports**
  - **—Minimum Support Circuits**
- **Software and Hardware Control of Nonvolatile Functions**
  - **—Maximum Store Protection**
- **TTL Compatible**
- **16 x 16 Organization**
- **Low Power Dissipation**
  - **—Active Current: 15 mA Typical**
  - **—Store Current: 8 mA Typical**
  - **—Standby Current: 6 mA Typical**
  - **—Sleep Current: 5 mA Typical**
- **High Reliability**
  - **—Store Cycles: 100,000**
  - **—Data Retention: 100 Years**
- **8 Pin Mini-DIP and 8 Lead SOIC Packages**

DESCRIPTION

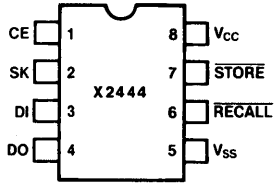
The Xicor X2444 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit for bit with a nonvolatile E^2PROM array. The X2444 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 10 ms or less and a recall operation (E^2PROM data to RAM) is completed in 2.5 μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 100,000 store operations. Data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

COPS™ is a trademark of National Semiconductor Corp.

PIN CONFIGURATION

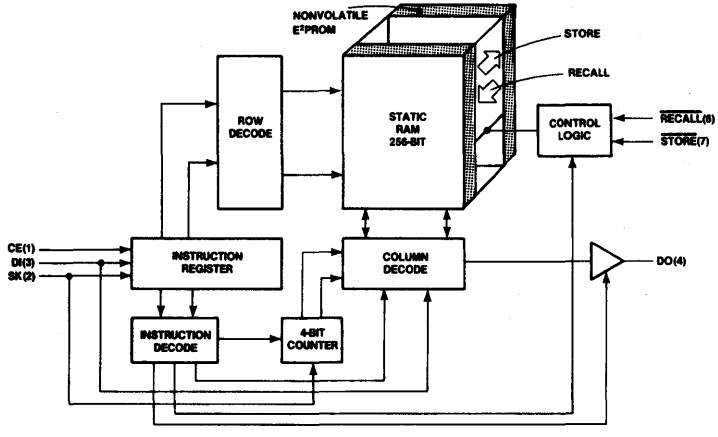


0042-1

PIN NAMES

CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL DIAGRAM



0042-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2444 ..... −10°C to +85°C
X2444I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2444 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2444I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2444 Limits		X2444I Limits		Units	Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	Power Supply Current		15		25	mA	All Inputs = V_{CC}, $I_{I/O}$ = 0 mA
I_{SL}	Sleep Current		7		10	mA	
I_{SB}	Standby Current		10		15	mA	CE = V_{IL}
I_{STO}	Store Current		12		15	mA	
I_{LI}	Input Load Current		10		10	µA	V_{IN} = V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −0.8 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	10,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	100,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

NONVOLATILE OPERATIONS

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	INST	WRITE ENABLE LATCH	Previous RECALL
Hardware Recall	1	0	NOP(3)	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP(3)	SET	True
Software Store	1	1	STO	SET	True

A.C. CHARACTERISTICS

X2444 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2444I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
F_{SK}	SK Frequency		1.0	MHz
t_{SKH}	SK Positive Pulse Width	0.4		μs
t_{SKL}	SK Negative Pulse Width	0.4		μs
t_{DS}	Data Setup Time	0.4		μs
t_{DH}	Data Hold Time	0.08		μs
t_{PD1}	SK ↓ to Data 0 Valid		375	ns
t_{PD}	SK ↑ to Data Valid		375	ns
t_Z	Chip Enable to Output High Z		1.0	μs
t_{CES}	Chip Enable Setup	0.8		μs
t_{CEH}	Chip Enable Hold	0.4		μs
t_{CDS}	Chip Deselect	0.8		μs

Power-Up Timing(4)

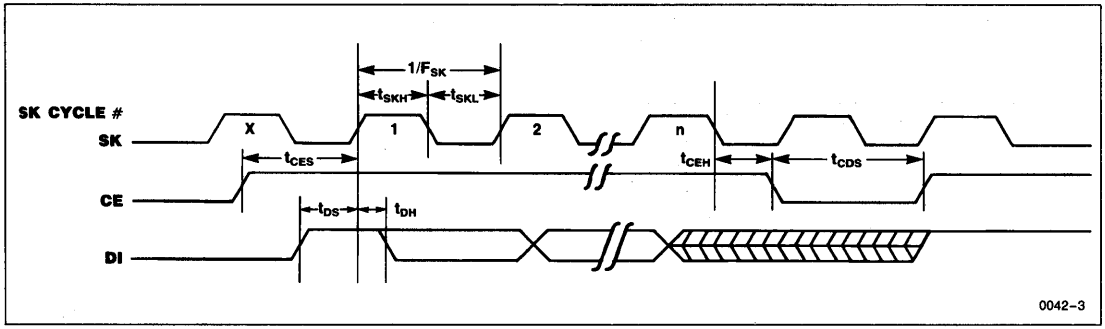
Symbol	Parameter	Typical(5)	Units
t_{PUR}	Power-Up to Read Operation	2.5	μs
t_{PUW}	Power-Up to Write Operation	2.5	μs

Notes: (3) NOP designates when the X2444 is not currently executing an instruction.

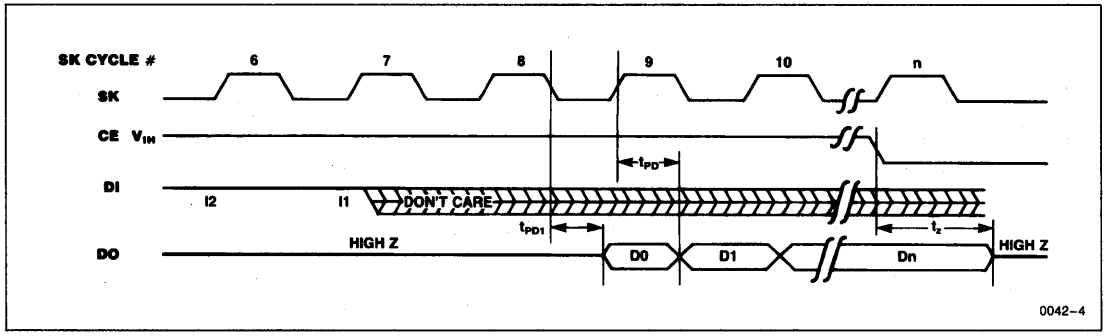
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

(5) Typical values are for T_A = 25°C and V_{CC} = 5V.

Write Cycle



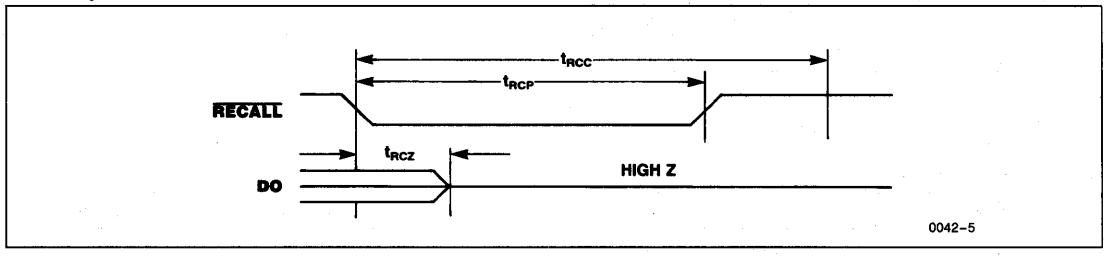
Read Cycle



Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Recall Cycle Time	2.5		μs
t_{RCP}	Recall Pulse Width(6)	1.0		μs
t_{RCZ}	Recall to Output High Z		0.5	μs

Recall Cycle



Note: (6) Recall rise time must be <10 μs.

Store Cycle Limits

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{ST}	Store Time		5	10	ms
t_{STP}	Store Pulse Width	0.2			µs
t_{STZ}	Store To Output High Z			1.0	µs
V_{CC}	Store Inhibit		3		V

Hardware Store

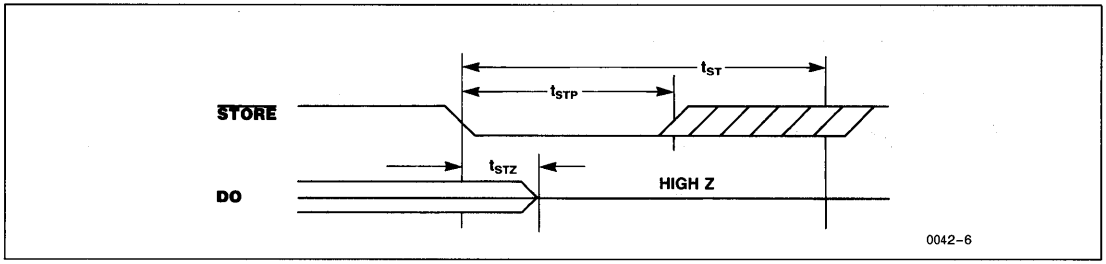
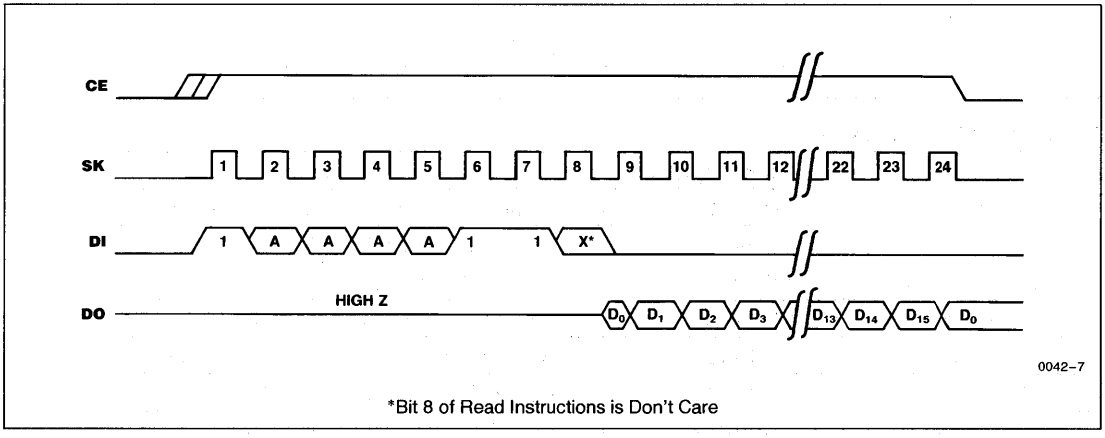


Figure 1: RAM Read



*Bit 8 of Read Instructions is Don't Care

Note: (7) Typical values are for T_A = 25°C and nominal supply voltage.

Figure 2: RAM Write

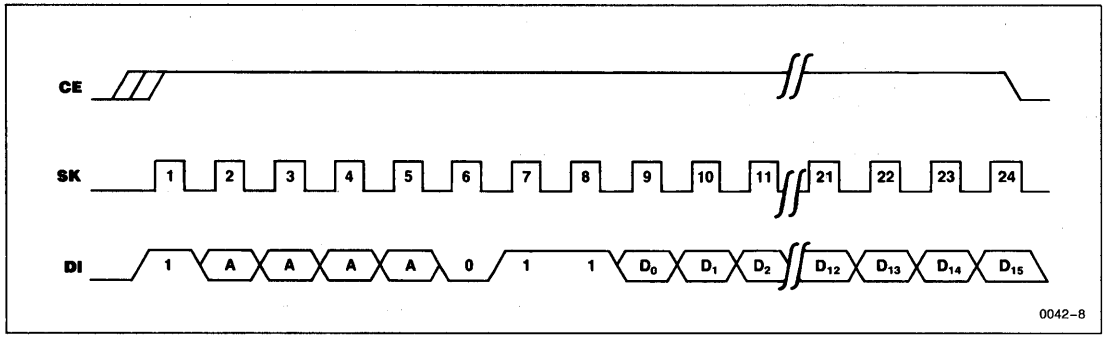


Figure 3: Non-Data Operations

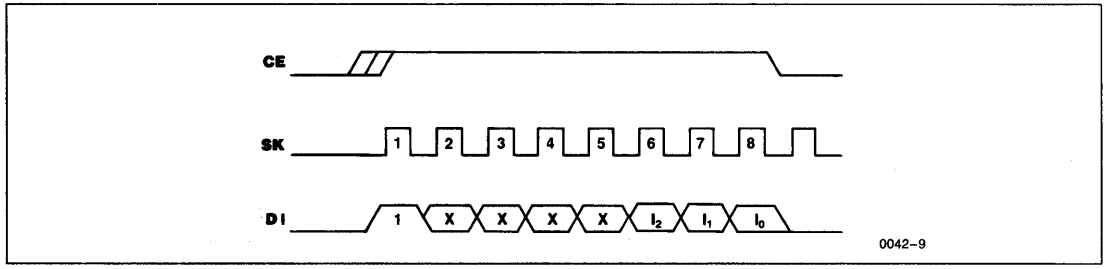


TABLE 1: INSTRUCTION SET

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables writes and stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E²PROM
SLEEP (Figure 3)	1XXXX010	Enter SLEEP Mode
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables writes and stores)
RCL (Figure 3)	1XXXX101	Recall E²PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

X = Don't Care
A = Address Bit

PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X2444 in the standby power mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

$\overline{\text{STORE}}$

$\overline{\text{STORE}}$ LOW will initiate an internal transfer of data from RAM to E^2PROM.

$\overline{\text{RECALL}}$

$\overline{\text{RECALL}}$ LOW will initiate an internal transfer of data from E^2PROM to RAM.

DEVICE OPERATION

The X2444 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a one, bits 6 through 3 are either RAM address (A) or don't care (X) and bits 2 through 0 are the operation codes. The X2444 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X2444 will not begin to interpret the data stream until a one has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X2444 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

WRDS and WREN

Internally the X2444 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E^2PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling *both* RAM writes and E^2PROM stores. The write enable latch is automatically reset on power-up.

SLEEP

The SLEEP instruction removes power from the RAM, placing the X2444 in a very low power quiescent state. Data in the RAM is lost once a SLEEP instruction is issued; however, data from the last store operation is retained in the E^2PROM. The sleep mode can be exited by either a software or hardware recall operation.

RCL and $\overline{\text{RECALL}}$

Either the RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of E^2PROM data into RAM. A recall operation must be performed after a power-up before any store or RAM write operation can be enabled. This recall operation and the recall recovery from the sleep mode guarantees a known state of data in RAM. Both recall operations set an internal "previous recall" latch which must be set to enable any write or store operations.

STO and $\overline{\text{STORE}}$

Either the STO instruction or a LOW on the $\overline{\text{STORE}}$ input will initiate the transfer of data from RAM to E^2PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

1. STO instruction issued or $\overline{\text{STORE}}$ input is LOW;
2. The internal write enable latch must be set (WREN instruction issued);
3. The "previous recall" latch must be set.

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset.

WRITE

The write instruction contains the 4 bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted in will be written to RAM. If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data) the data already shifted in will be overwritten.

READ

The read instruction contains the 4 bit address of the word to be accessed. Unlike the other six instructions, I_0 is a "don't care" for the read instruction. This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

WRITE PROTECTION

The X2444 provides three hardware and software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Down Condition
(when "write enable" latch and "previous recall" latch are not in the reset state):

- Write Inhibit—Holding either $\overline{\text{RECALL}}$ LOW, CE LOW or $\overline{\text{STORE}}$ HIGH during power-down will prevent an inadvertent store.

Power-Up Condition

- Write Enable Latch—Upon power-up the "write enable" latch is in the reset state, disabling any store operation.

Unknown Data Store

- Previous Recall Latch—The "previous recall" latch must be set after power-up and after exiting the sleep mode. It may be set only by performing a recall operation, which assures that data in all RAM locations is valid.

LOW POWER MODES

The X2444 provides two power conservation modes. When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode. Entering the sleep mode removes power from the entire RAM array, placing the device in a very low power quiescent state (sleep mode).

Part Number	Store Cycles	Data Changes Per Bit
X2444	100,000	10,000
X2444I	100,000	10,000

SYSTEM CONSIDERATIONS

Power-Down Data Protection

Because the X2444 is a 5V only nonvolatile memory device it may be susceptible to inadvertent writes to the E²PROM array during power-down cycles. Power-up cycles are not a problem because the previous recall latch and write enable latch are reset, preventing any possible corruption of E²PROM data.

If the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins are tied to V_{CC} through a pullup resistor and only software store operations are performed to initiate stores, there is little likelihood of an inadvertent store. However, if these two lines are under microprocessor control, positive action should be employed to negate the possibility of these control lines bouncing and generating an unwanted store. The safest method is to issue the WRDS command after a write sequence and also following store operations. Note: an internal store may take up to 10 ms; therefore, the host microprocessor should delay 10 ms after initiating the store prior to issuing the WRDS command.

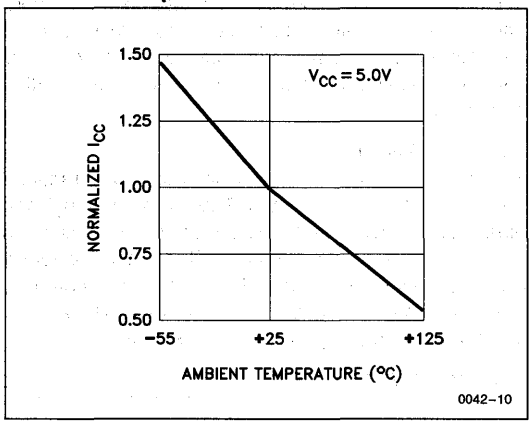
Power-On Recall

The X2444 performs a power-on recall that transfers the E²PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the previous recall latch. During this power-on recall operation, all commands are ignored. Therefore, the host should delay any operation with the X2444 a minimum 2.5 μs (t_{RCC}) after V_{CC} is stable.

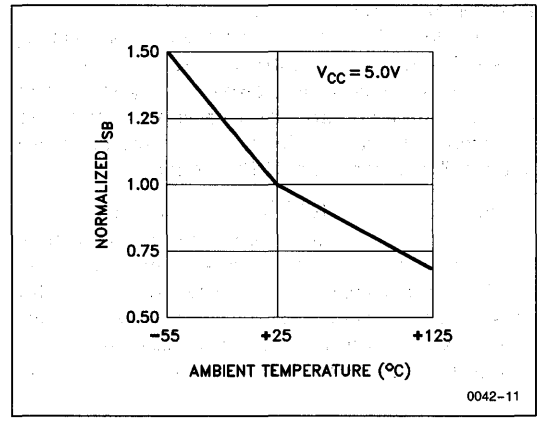
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Xicor®

256 Bit Commercial Industrial X24C44 X24C44I 16 x 16 Bit

Nonvolatile Static RAM

FEATURES

- **Advanced CMOS Version of Xicor's X2444**
- **16 x 16 Organization**
- **Single 5 Volt Supply**
- **Ideal for use with Single Chip Microcomputers**
  - **—Static Timing**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaced to Microcontroller Ports**
- **Software and Hardware Control of Nonvolatile Functions**
- **Auto Recall on Power-Up**
- **TTL and CMOS Compatible**
- **Low Power Dissipation**
  - **—Active Current: 2 mA**
  - **—Standby Current: 50 μA**
- **8 Pin Mini-DIP and 8 Lead SOIC Packages**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**

DESCRIPTION

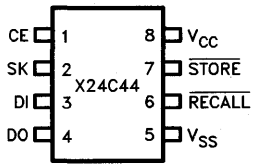
The Xicor X24C44 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit by bit with a nonvolatile E^2PROM array. The X24C44 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 5 ms or less and a recall operation (E^2PROM data to RAM) is completed in 2 μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details of endurance and data retention characteristics for Xicor nonvolatile memories.

COPS™ is a trademark of National Semiconductor Corp.

PIN CONFIGURATION



0121-1

PIN NAMES

CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{RECALL}$	Recall Input
$\overline{STORE}$	Store Input
V_{CC}	+5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24C44 ..... −10°C to +85°C
X24C44I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24C44 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X24C44I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
I_{CC}	V_{CC} Supply Current (TTL Inputs)		2	mA	SK = TTL Levels @ 1 MHz, DO = Open, All Other Inputs = V_{IH}
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		1	mA	DO = Open, CE = V_{IL}, All Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		50	µA	DO = Open, CE = GND, All Other Inputs = V_{CC} − 0.3V
I_{LI}	Input Load Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(1)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(1)	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	100,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	1,000,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS

X24C44 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X24C44I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

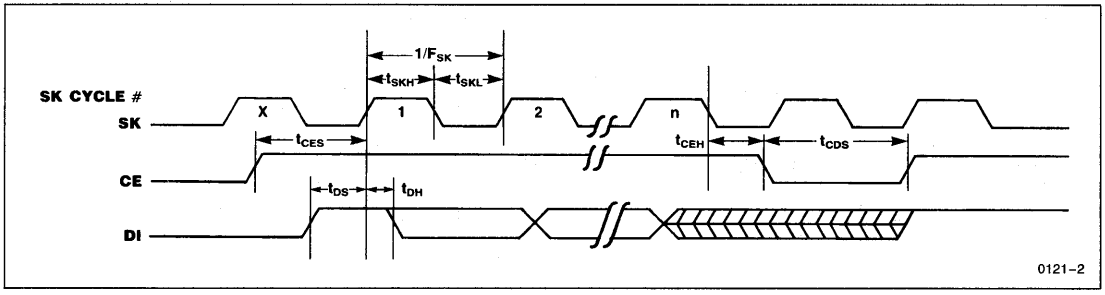
Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
F_{SK}	SK Frequency		1.0	MHz
t_{SKH}	SK Positive Pulse Width	400		ns
t_{SKL}	SK Negative Pulse Width	400		ns
t_{DS}	Data Setup Time	400		ns
t_{DH}	Data Hold Time	80		ns
t_{PD1}	SK to Data Bit 0 Valid		375	ns
t_{PD}	SK to Data Valid		375	ns
t_Z	Chip Enable to Output High Z		1.0	µs
t_{CES}	Chip Enable Setup	800		ns
t_{CEH}	Chip Enable Hold	400		ns
t_{CDS}	Chip Deselect	800		ns

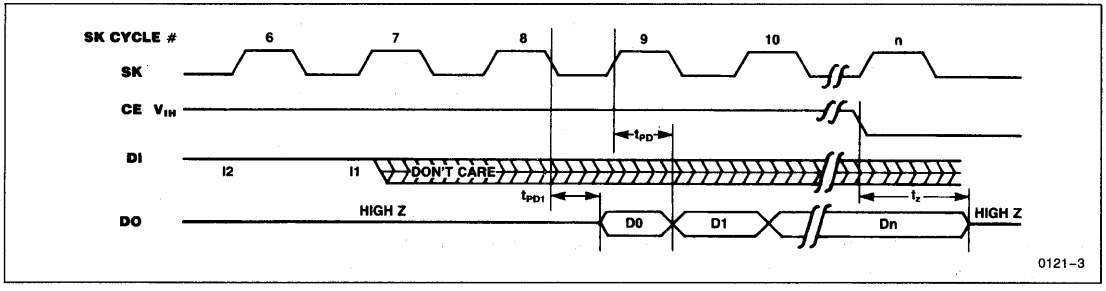
Power-Up Timing(3)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	200	µs
t_{PUW}	Power-Up to Write or Store Operation	5	ms

Write Cycle



Read Cycle



Note: (3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

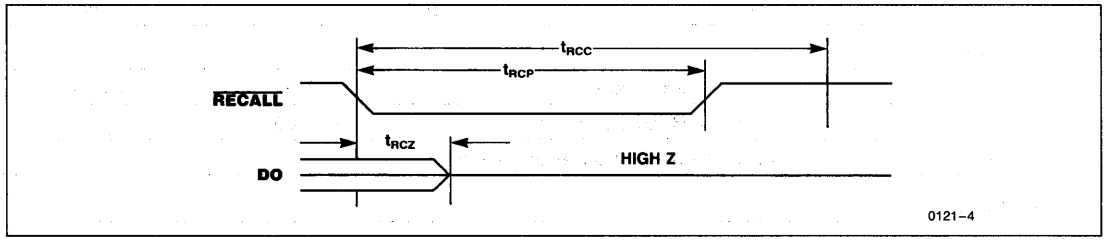
NONVOLATILE OPERATIONS

Operation	$\overline{STORE}$	$\overline{RECALL}$	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware Recall	1	0	NOP(4)	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP(4)	SET	SET
Software Store	1	1	STO	SET	SET

Array Recall Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Recall Cycle Time	2		μs
t_{RCP}	Recall Pulse Width(5)	500		ns
t_{RCZ}	Recall to Output in High Z		500	ns

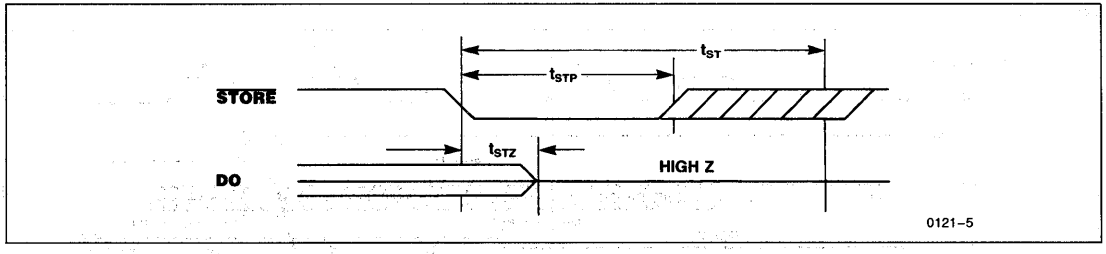
Recall Timing



Store Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{ST}	Store Time		2	5	ms
t_{STP}	Store Pulse Width	200			ns
t_{STZ}	Store to Output in High Z			100	ns
V_{CC}	Store Inhibit		3		V

Store Timing



Notes: (4) NOP designates when the X24C44 is not currently executing an instruction.
(5) Recall rise time must be <10 ns.
(6) Typical values are for T_A = 25°C and nominal supply voltage.

Figure 1: RAM Read

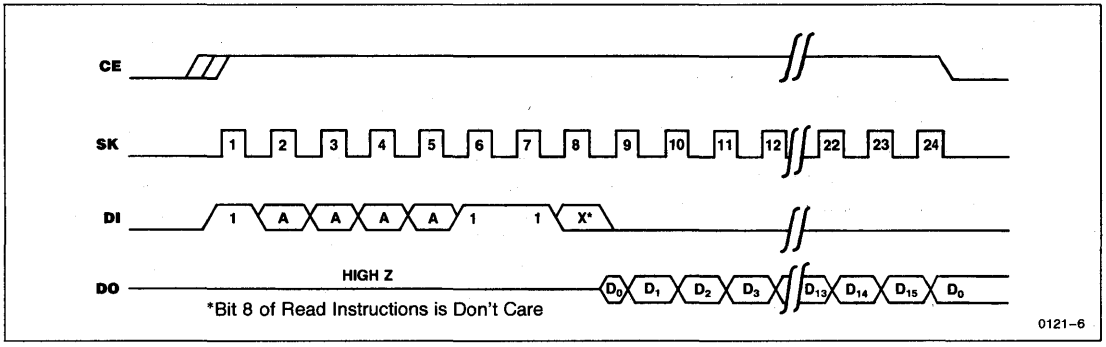


Figure 2: RAM Write

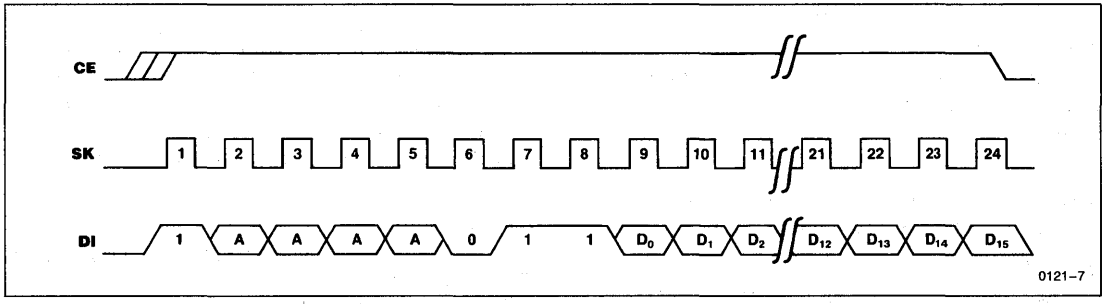


Figure 3: Non-Data Operations

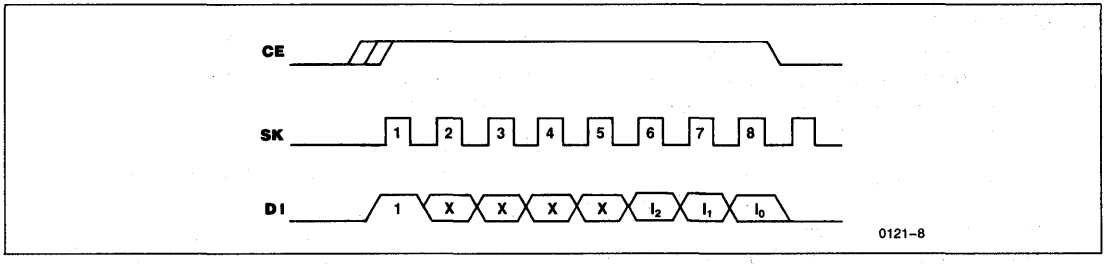


TABLE 1: INSTRUCTION SET

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and Stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E^2PROM
Reserved	1XXXX010	N/A
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and Stores)
RCL (Figure 3)	1XXXX101	Recall E^2PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

X = Don't Care
A = Address

PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C44 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

$\overline{\text{STORE}}$

$\overline{\text{STORE}}$ LOW will initiate an internal transfer of data from RAM to the E^2PROM array.

$\overline{\text{RECALL}}$

$\overline{\text{RECALL}}$ LOW will initiate an internal transfer of data from E^2PROM to the RAM array.

DEVICE OPERATIONS

The X24C44 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address (A) or don't care (X) and bits 2 through 0 are the operation codes. The X24C44 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X24C44 will not begin to interpret the data stream until a logic one has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X24C44 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and $\overline{\text{RECALL}}$

Either a software RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of E^2PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-on and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

WRDS and WREN

Internally the X24C44 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E^2PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E^2PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO and $\overline{\text{STORE}}$

Either the software STO instruction or a LOW on the $\overline{\text{STORE}}$ input will initiate a transfer of data from RAM to E^2PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

1. STO instruction issued or $\overline{\text{STORE}}$ input is LOW.
2. The internal write enable latch must be set (WREN instruction issued).
3. The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

WRITE

The write instruction contains the 4 bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

READ

The read instruction contains the 4 bit address of the word to be accessed. Unlike the other six instructions, I_0 of the instruction word is a "don't care". This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

SLEEP

Because the X24C44 is a low power CMOS device, the SLEEP instruction implemented on the first generation NMOS device has been deleted. For systems converting from the X2444 to the X24C44 the software need not be changed; the instruction will be ignored.

WRITE PROTECTION

The X24C44 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Write Enable Latch. Upon power-up the "write enable" latch is in the reset state, disabling any store operation.

Unknown Data Store

Previous Recall Latch. The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-On Recall

The X24C44 performs a power-on recall that transfers the E²PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-on recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C44 a minimum 200 μs (t_{PUR}) after V_{CC} is stable.

Power-Down Data Protection

Because the X24C44 is a 5V only nonvolatile memory device it may be susceptible to inadvertent stores to the E²PROM array during power-down cycles. Power-up cycles are not a problem because the previous recall latch and write enable latch are reset, preventing any possible corruption of E²PROM data.

Software Power-Down Protection

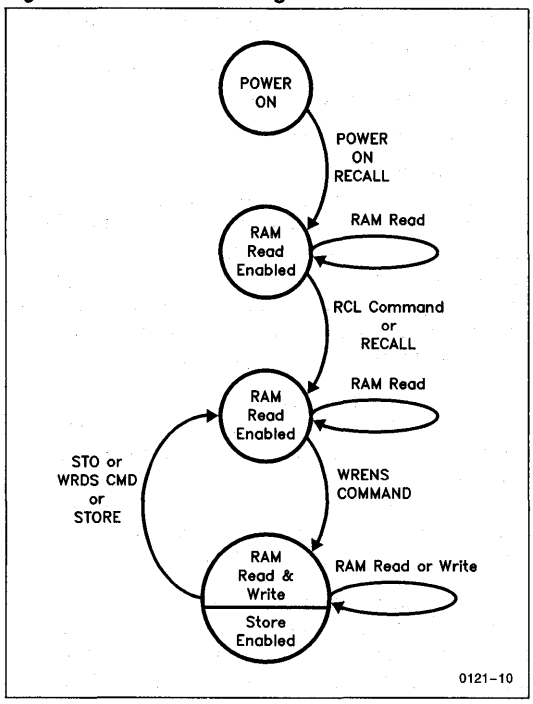
If the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins are tied to V_{CC} through a pullup resistor and only software operations are performed to initiate stores, there is little likelihood of an inadvertent store. However, if these two lines are under microprocessor control, positive action should be employed to negate the possibility of these control lines bouncing and generating an unwanted store. The safest method is to issue the WRDS command after a write sequence and also following store operations. Note: an internal store may take up to 5 ms; therefore, the host microprocessor should delay 5 ms after initiating the store prior to issuing the WRDS command.

Hardware Power-Down Protection

(when the "write enable" latch and "previous recall" latch are **not in the reset state**):

Write Inhibit. Holding either $\overline{\text{RECALL}}$ LOW, CE LOW or $\overline{\text{STORE}}$ HIGH during power-down will prevent an inadvertent store.

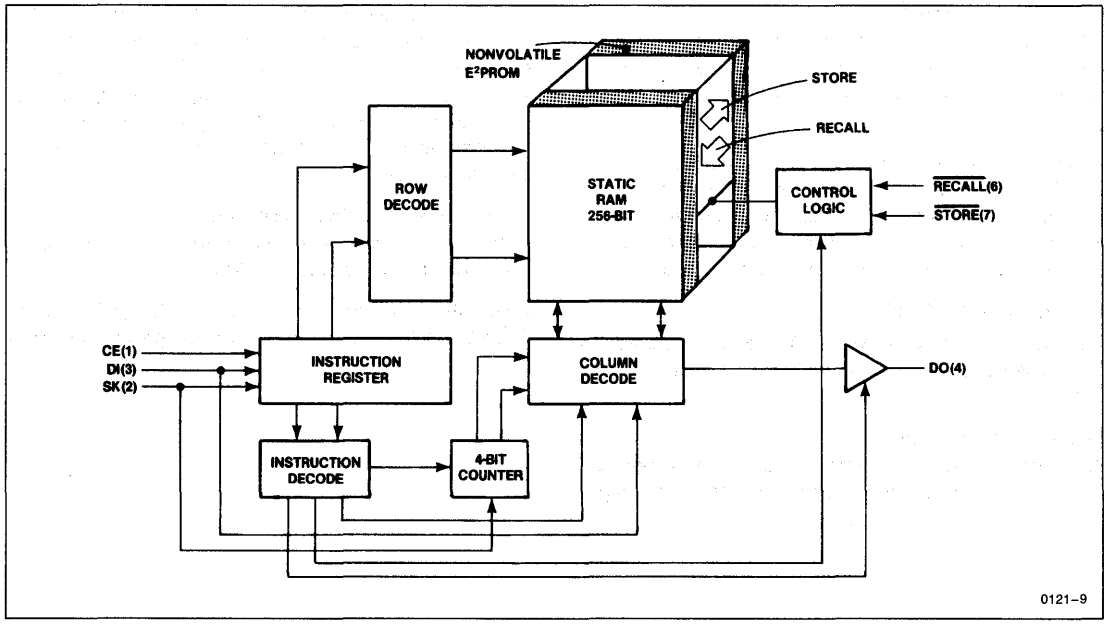
Figure 4: X24C44 State Diagram



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

FUNCTIONAL DIAGRAM



FACT SHEET

256 Bit Commercial Industrial X24C45 X24C45I 16 x 16 Bit

Nonvolatile Static RAM

2

FEATURES

- **Autostore™**
  - **—Automatically Performs a Store Operation Upon Loss of V_{CC}**
- **Single 5 Volt Supply**
- **Ideal for use with Single Chip Microcomputers**
  - **—Minimum I/O Interface**
  - **—Serial Port Compatible (COPS™, 8051)**
  - **—Easily Interfaced to Microcontroller Ports**
- **Software and Hardware Control of Nonvolatile Functions**
- **Auto Recall on Power-Up**
- **TTL and CMOS Compatible**
- **Low Power Dissipation**
  - **—Active Current: 2 mA**
  - **—Standby Current: 50 μA**
- **8 Pin Mini-DIP and 8 Lead SOIC Packages**
- **High Reliability**
  - **—Store Cycles: 1,000,000**
  - **—Data Retention: 100 Years**

DESCRIPTION

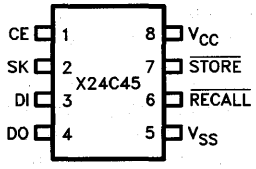
The Xicor X24C45 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit by bit with a nonvolatile E^2PROM array. The X24C45 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E^2PROM) is completed in 5 ms or less and a recall operation (E^2PROM data to RAM) is completed in 2 μs or less.

The X24C45 also features Autostore, a user selectable feature that will automatically perform a store operation when V_{CC} falls below a preset threshold.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details of endurance and data retention characteristics for Xicor nonvolatile memories.

PIN CONFIGURATION



0127-1

PIN NAMES

CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{RECALL}$	Recall Input
$\overline{STORE}$	Store Input
V_{CC}	+5V
V_{SS}	Ground

Autostore™ is a trademark of Xicor, Inc.
COPS™ is a trademark of National Semiconductor Corp.

PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C45 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

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$\overline{\text{STORE}}$

$\overline{\text{STORE}}$ LOW will initiate an internal transfer of data from RAM to the E^2PROM array.

$\overline{\text{RECALL}}$

$\overline{\text{RECALL}}$ LOW will initiate an internal transfer of data from E^2PROM to the RAM array.

DEVICE OPERATIONS

The X24C45 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address (A) or don't care (X) and bits 2 through 0 are the operation codes. The X24C45 requires the instruction to be shifted in with the MSB first.

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In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and $\overline{\text{RECALL}}$

Either a software RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of E^2PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-on and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

WRDS and WREN

Internally the X24C45 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E^2PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E^2PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO and $\overline{\text{STORE}}$

Either the software STO instruction or a LOW on the $\overline{\text{STORE}}$ input will initiate a transfer of data from RAM to E^2PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

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Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

WRITE

The write instruction contains the 4 bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

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D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

AUTOSTORE

The autostore instruction sets the autostore enable latch, allowing the X24C45 to automatically perform a store operation when V_{CC} falls below the autostore threshold.

WRITE PROTECTION

The X24C45 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Write Enable Latch. Upon power-up the "write enable" latch is in the reset state, disabling any store operation.

Unknown Data Store

Previous Recall Latch. The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-On Recall

The X24C45 performs a power-on recall that transfers the E^2PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-on recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C45 a minimum 200 μs (t_{PUR}) after V_{CC} is stable.

NOTES

Electrically Erasable PROM

TYPICAL FEATURES

- **Internally Organized 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Eight Byte Page Write Mode**
  —Minimizes Total Write Time Per Byte
- **Self Timed Write Cycle**
  —Typical Write Cycle Time of 5 ms
- **High Reliability**
  —Endurance: 100,000 Writes Per Byte
  —Data Retention: 100 Years
- **8 Pin Mini-DIP and 14 Lead SOIC Packages**

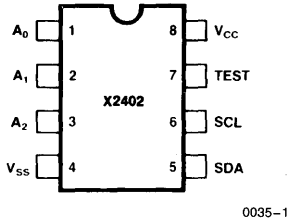
DESCRIPTION

The X2402 is a 2048 bit serial E^2PROM, internally organized as one 256 x 8 page. The X2402 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2402 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 100,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS



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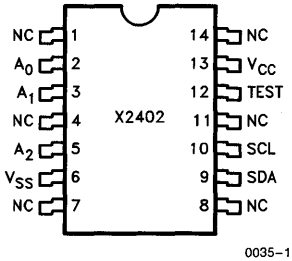


0035-11

PIN NAMES

A_0 to A_2	Address Inputs
V_{SS}	Ground
SDA	Serial Data
SCL	Serial Clock
Test	**Input to V_{SS}**
V_{CC}	Supply Voltage

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2402 ..... −10°C to +85°C
X2402I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2402 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2402I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2402 Limits			X2402I Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Supply Current		20	30		20	35	mA	f_{SCL} = 100 KHz
I_{SB}	V_{CC} Standby Current		15	25		15	30	mA	
I_{LI}	Input Leakage Current		0.1	10		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10		0.1	10	µA	V_{OUT} = GND to V_{CC}
I_{TP}(2)	Test Pin Pull Down Current		16	30		16	30	µA	V_{IN} = V_{CC}
V_{IL}(4)	Input Low Voltage	−1.0		0.8	−1.0		0.8	V	
V_{IH}(4)	Input High Voltage	2.0		V_{CC} +0.5	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 3 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	100,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Test pin has on chip pull down device which sinks 16 µA (typical) to V_{SS}.
(3) This parameter is periodically sampled and not 100% tested.
(4) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS

X2402 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2402I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

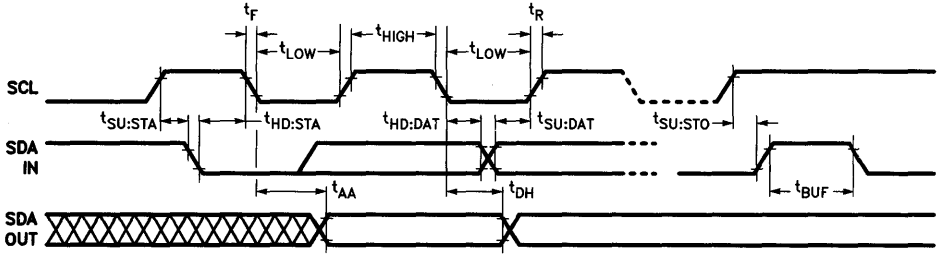
Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	μs
t_{BUF}	Time the Bus Must be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X2402 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Bus Timing



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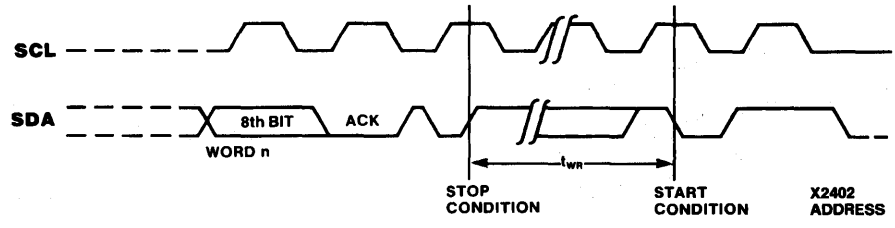
Note: (5) Typical values are for T_A = 25°C and nominal supply voltage.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Address (A_0, A_1, A_2)

The Address inputs are used to set the least significant three bits of the seven bit slave address. The inputs are static, and should be tied HIGH or LOW, forming one unique address per device.

DEVICE OPERATION

The X2402 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X2402 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indication start and stop conditions. Refer to Figures 1 and 2.

Figure 1: Data Validity

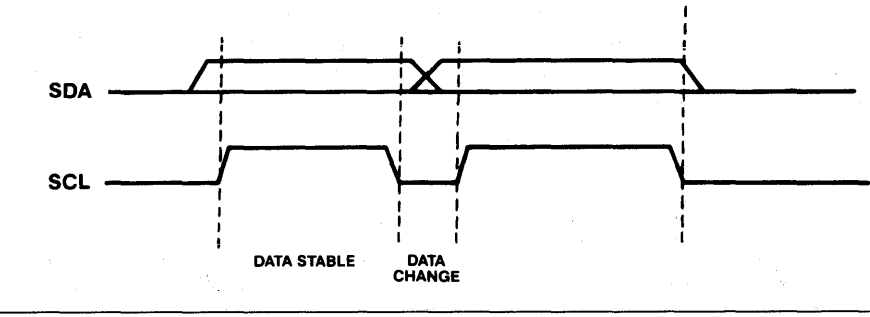
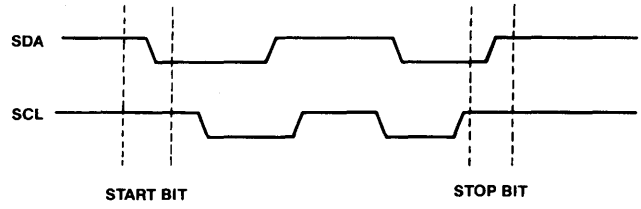


Figure 2: Definition of Start and Stop



Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X2402 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

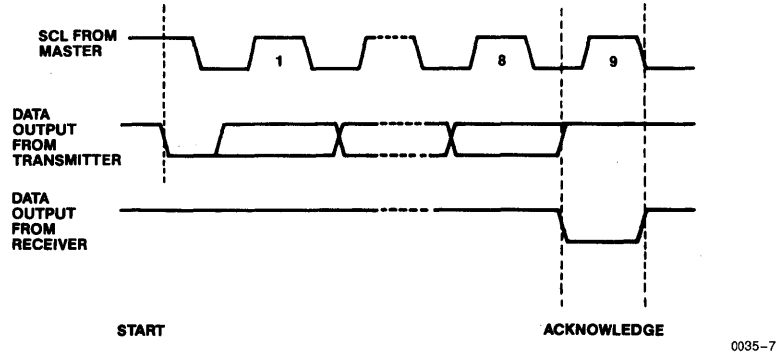
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X2402 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X2402 will respond with an acknowledge after the receipt of each subsequent eight bit word.

Figure 3: Acknowledge Response from Receiver

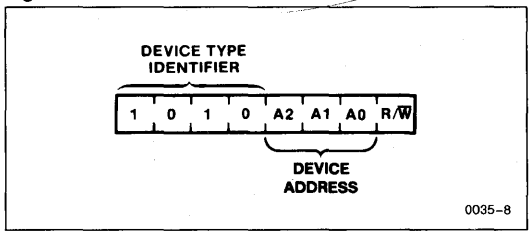


In the read mode the X2402 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X2402 will continue to transmit data. If an acknowledge is not detected, the X2402 will terminate further data transmissions and await the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X2402 this is fixed as 1010[B].

Figure 4: Slave Address



The next three significant bits address a particular device. A system could have up to eight X2402 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A_0, A_1 and A_2 inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected; when set to zero a write operation is selected.

Following the start condition, the X2402 monitors the SDA bus comparing the slave address being transmitted with its address (device type and state of A_0, A_1 and A_2 inputs). Upon a compare the X2402 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X2402 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X2402 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X2402 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X2402 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X2402 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write

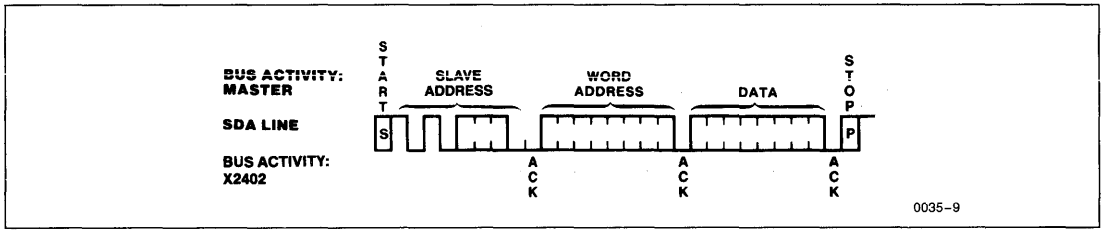
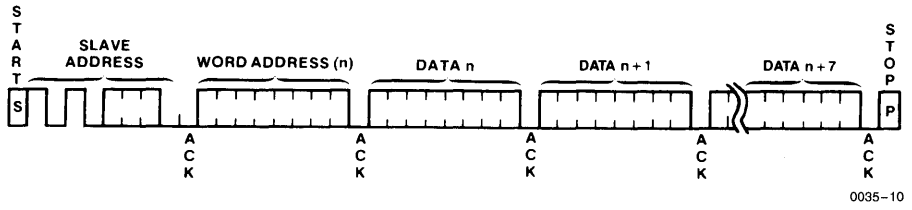


Figure 6: Page Write



NOTE: In this example n = XXXX X000(B); X = 1 or 0

Page Write

The X2402 is capable of an eight byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to seven more words. After the receipt of each word, the X2402 will respond with an acknowledge.

After the receipt of each word, the three low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X2402 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X2402 is still busy with the write operation no ACK will be returned. If the X2402 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Current Address Read

Internally the X2402 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X2402 issues an acknowledge and transmits the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X2402 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Figure 7: Current Address Read

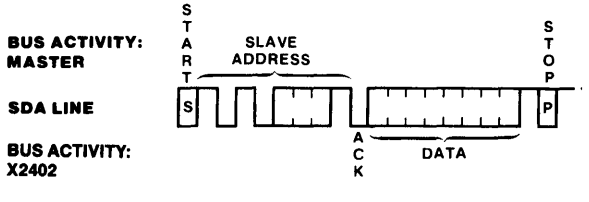
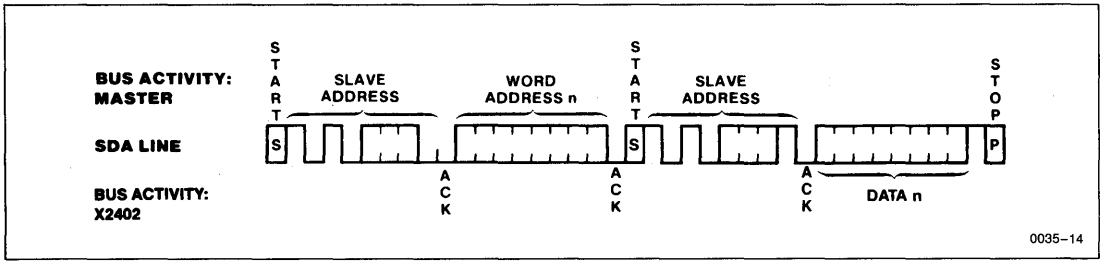


Figure 8: Random Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X2402 and then by the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X2402 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X2402 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all eight address bits, allowing the entire memory contents of the current 256 word page to be serially read during one operation. If more than 256 words are read, the counter "rolls over" and the X2402 continues to output data from the same 256 word page for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9: Sequential Read

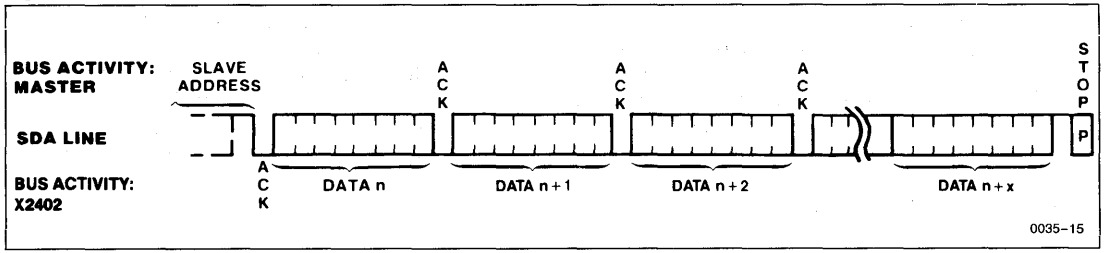
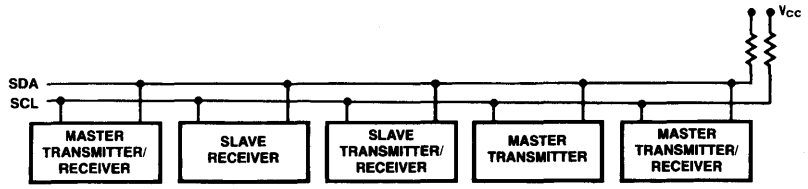
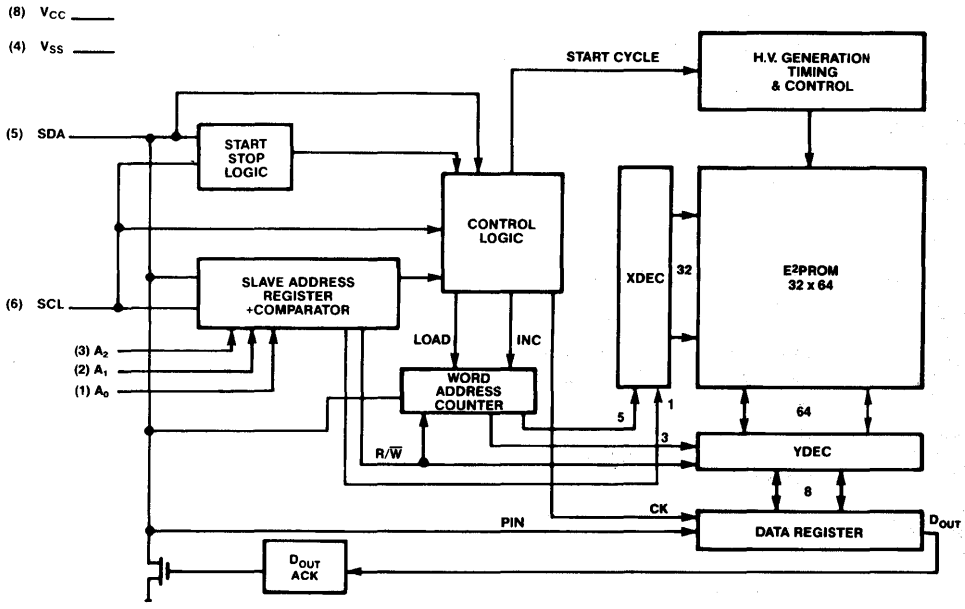


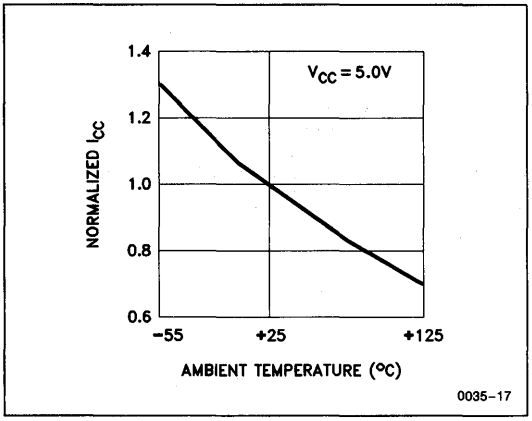
Figure 10: Typical System Configuration



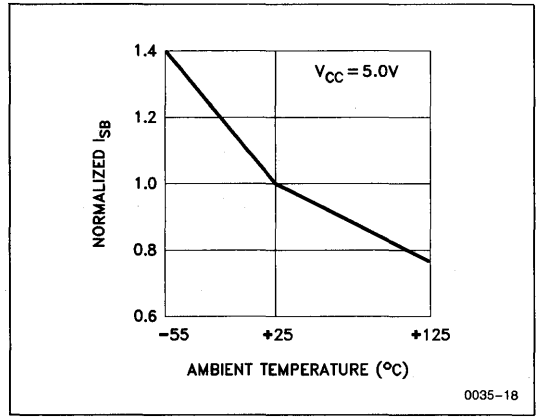
FUNCTIONAL DIAGRAM



Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Electrically Erasable PROM

TYPICAL FEATURES

- **Internally Organized as Two Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Eight Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **High Reliability**
  - **—Endurance: 100,000 Writes Per Byte**
  - **—Data Retention: 100 Years**
- **8 Pin Mini-DIP and 14 Lead SOIC Packages**

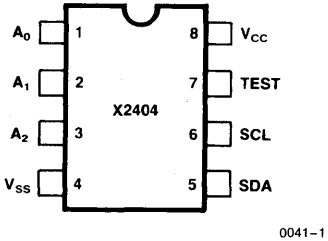
DESCRIPTION

The X2404 is a 4096 bit serial E²PROM, internally organized as two 256 x 8 pages. The X2404 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2404 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 100,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS



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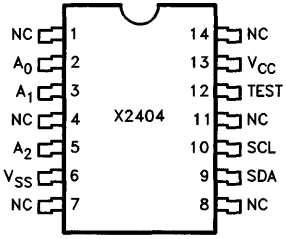


0041-19

PIN NAMES

A_0 to A_2	Address Inputs
V_{SS}	Ground
SDA	Serial Data
SCL	Serial Clock
Test	**Input to V_{SS}**
V_{CC}	Supply Voltage

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2404 ..... −10°C to +85°C
X2404I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2404 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2404I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2404 Limits			X2404I Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Supply Current		20	30		20	35	mA	f_{SCL} = 100 KHz
I_{SB}	V_{CC} Standby Current		15	25		15	30	mA	
I_{LI}	Input Leakage Current		0.1	10		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10		0.1	10	µA	V_{OUT} = GND to V_{CC}
I_{TP}(2)	Test Pin Pull Down Current		16	30		16	30	µA	V_{IN} = V_{CC}
V_{IL}(4)	Input Low Voltage	−1.0		0.8	−1.0		0.8	V	
V_{IH}(4)	Input High Voltage	2.0		V_{CC} +0.5	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 3 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	100,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Test pin has on chip pull down device which sinks 16 µA (typical) to V_{SS}.
(3) This parameter is periodically sampled and not 100% tested.
(4) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

2

A.C. CHARACTERISTICS

X2404 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2404I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X2404 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Address (A_0)

A_0 is unused by the X2404, however, it must be tied to V_{SS} to ensure proper device operation.

Address (A_1, A_2)

The Address inputs are used to set the least significant two bits of the six bit slave address. The inputs are static, and should be tied HIGH or LOW, forming one unique address per device.

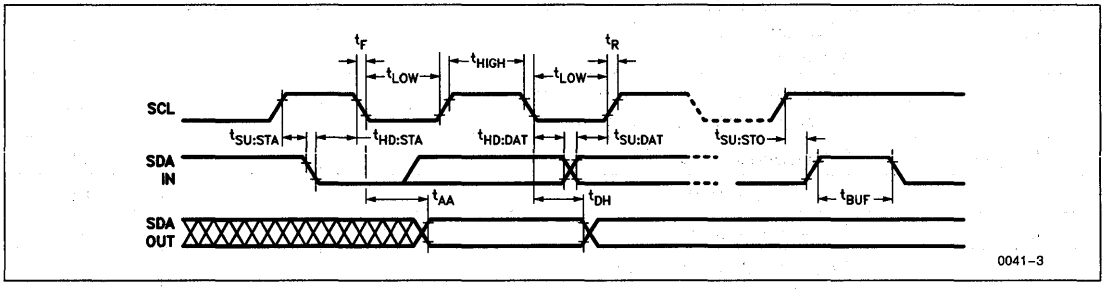
DEVICE OPERATION

The X2404 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X2404 will be considered a slave in all applications.

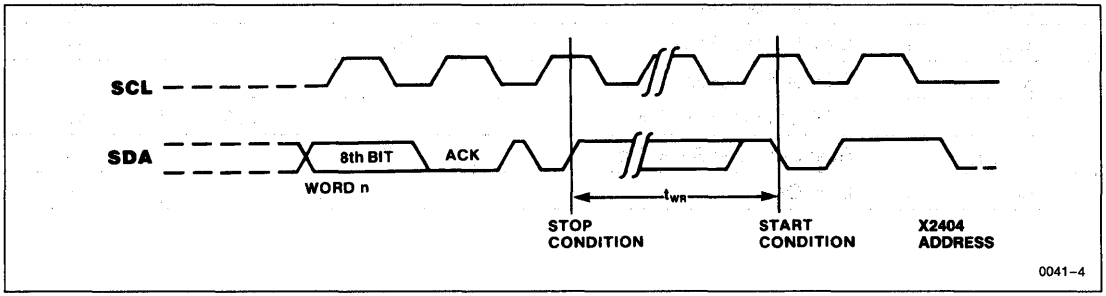
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indication start and stop conditions. Refer to Figures 1 and 2.

Bus Timing



Write Cycle Timing



Note: (5) Typical values are for T_A = 25°C and nominal supply voltage.

Figure 1: Data Validity

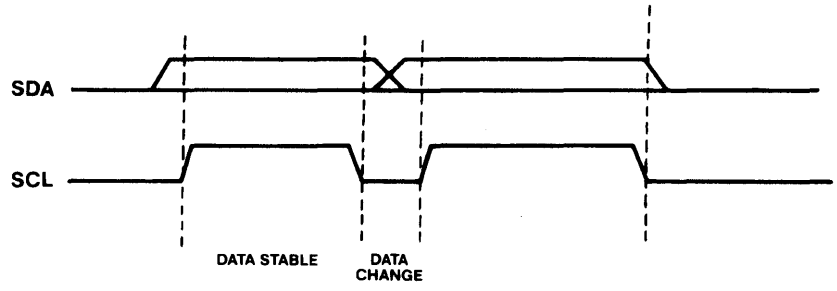
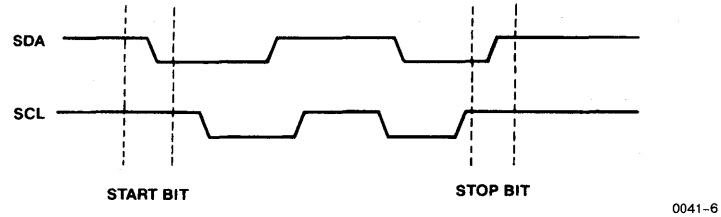


Figure 2: Definition of Start and Stop



Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X2404 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

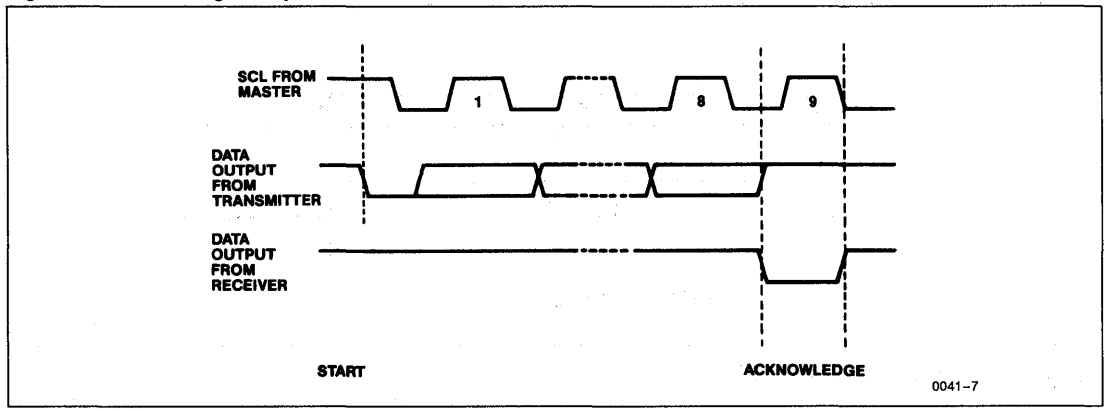
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X2404 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X2404 will respond with an acknowledge after the receipt of each subsequent eight bit word.

Figure 3: Acknowledge Response from Receiver

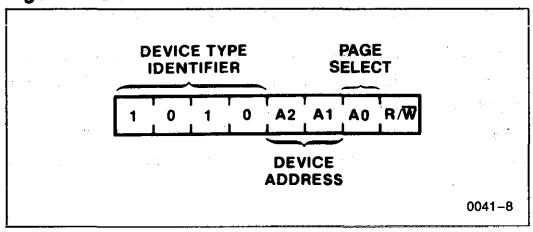


In the read mode the X2404 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X2404 will continue to transmit data. If an acknowledge is not detected, the X2404 will terminate further data transmissions and await the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X2404 this is fixed as 1010[B].

Figure 4: Slave Address



The next two significant bits address a particular device. A system could have up to four X2404 devices on the bus (see Figure 10). The four addresses are defined by the state of the A_1 and A_2 inputs.

The next bit of the slave address field (bit 1) is the page select bit. It is used by the host to toggle between the two 256 word pages of memory.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected; when set to zero a write operation is selected.

Following the start condition, the X2404 monitors the SDA bus comparing the slave address being transmitted with its address (device type and state of A_1 and A_2 inputs). Upon a compare the X2404 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X2404 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X2404 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X2404 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X2404 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X2404 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write

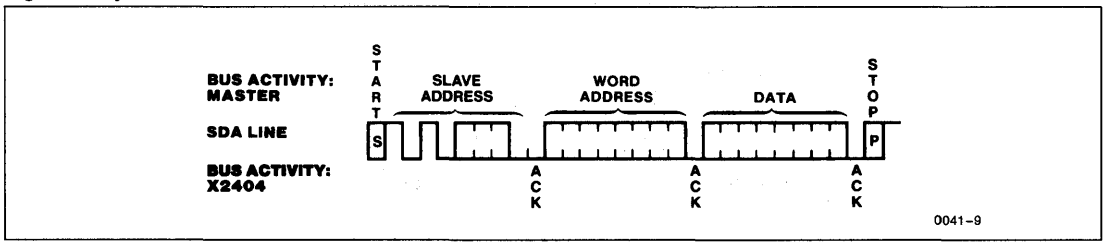
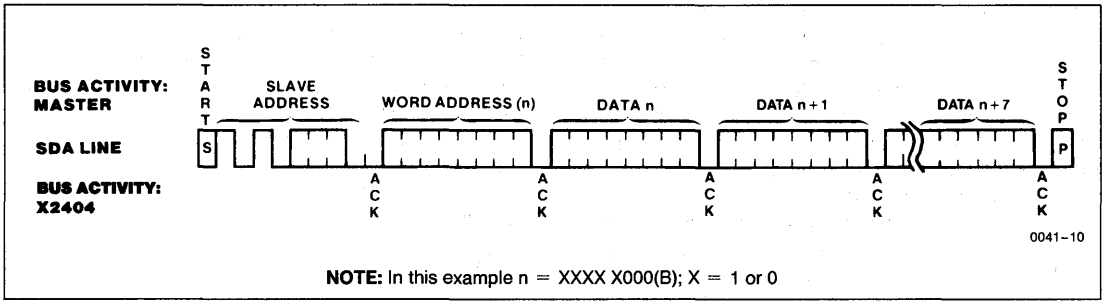


Figure 6: Page Write



NOTE: In this example n = XXXX X000(B); X = 1 or 0

Page Write

The X2404 is capable of an eight byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to seven more words. After the receipt of each word, the X2404 will respond with an acknowledge.

After the receipt of each word, the three low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X2404 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X2404 is still busy with the write operation no ACK will be returned. If the X2404 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

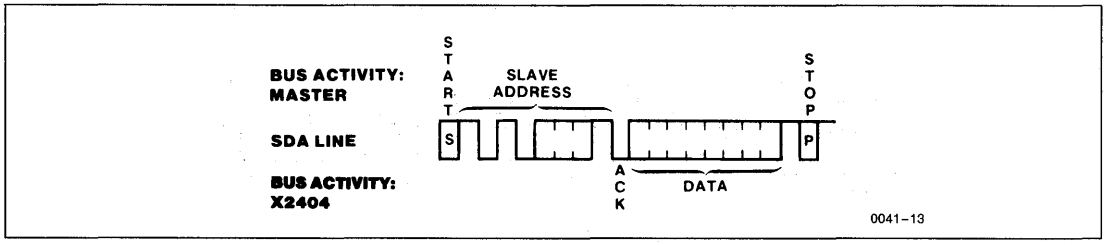
READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Current Address Read

Internally the X2404 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X2404 issues an acknowledge and transmits the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X2404 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Figure 7: Current Address Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X2404 and then by the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X2404 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X2404 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all eight address bits, allowing the entire memory contents of the current 256 word page to be serially read during one operation. If more than 256 words are read, the counter "rolls over" and the X2404 continues to output data from the same 256 word page for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

ENDURANCE

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. The process average for endurance of Xicor E^{2}PROMs is approximately ½ million cycles, as documented in RR504, the *Xicor Reliability Report on Endurance.* Included in that report is a method for determining the expected endurance of the device based upon the specific application environment. RR504 and additional reliability reports are available from Xicor.

Figure 8: Random Read

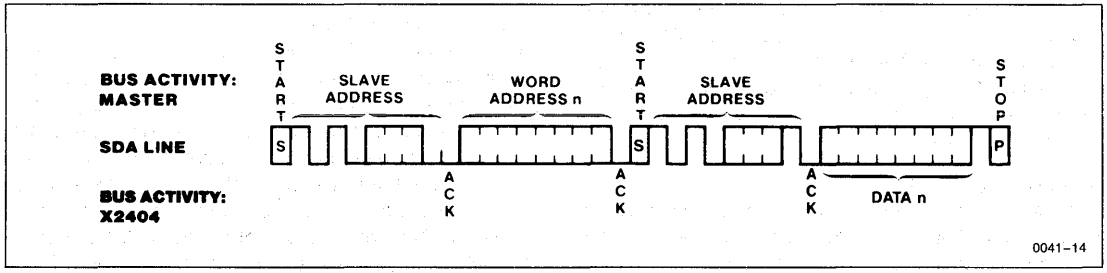


Figure 9: Sequential Read

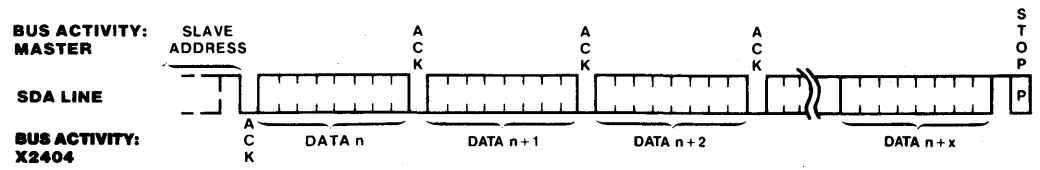
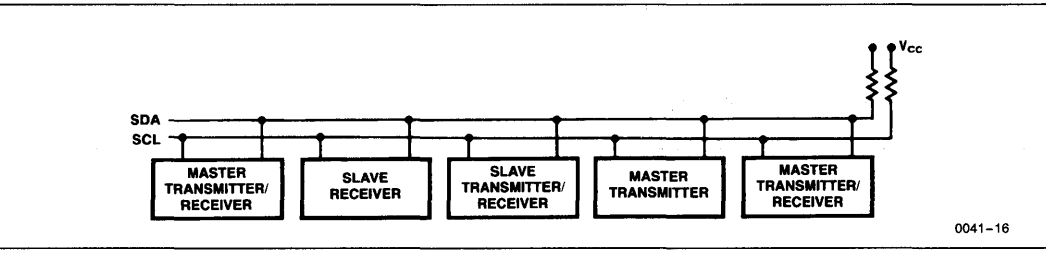
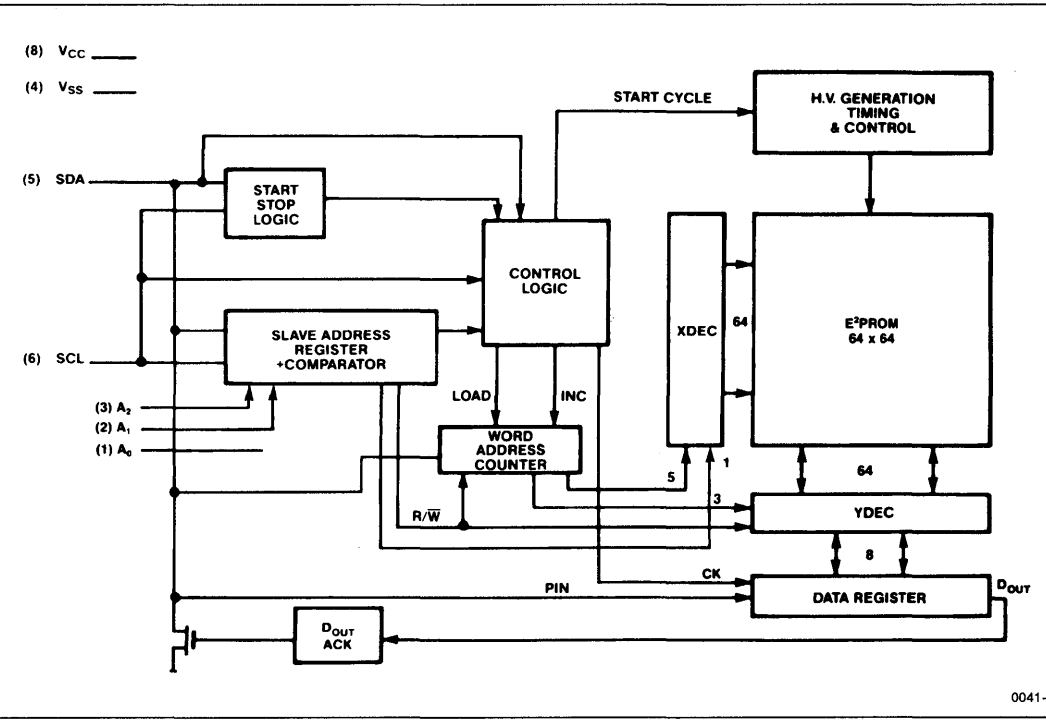


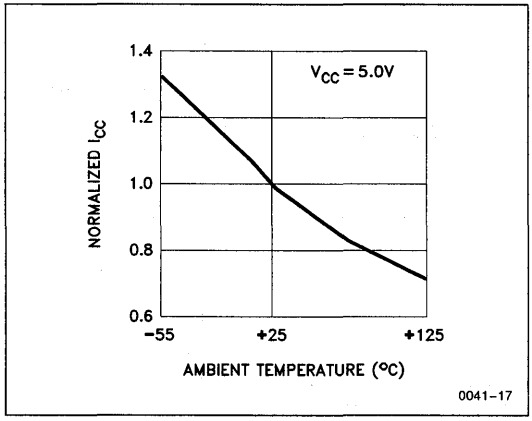
Figure 10: Typical System Configuration



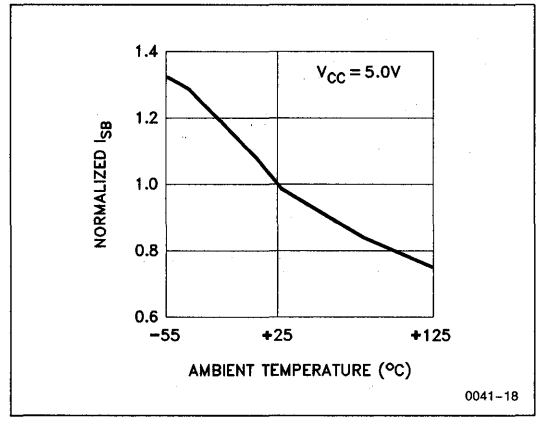
FUNCTIONAL DIAGRAM



Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



1K Commercial Industrial X24C01 X24C01I 128 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **Low Power CMOS**
  - **—Active Current Less Than 1 mA**
  - **—Standby Current Less Than 50 μA**
- **Internally Organized 128 x 8**
- **2 Wire Serial Interface**
  - **—Bidirectional Data Transfer Protocol**
- **Four Byte Page Write Mode**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **High Reliability**
  - **—Endurance: 100,000 Cycles Per Byte**
  - **—Data Retention: 100 Years**
- **8-Pin Mini-DIP and 8-Pin SOIC Packages**

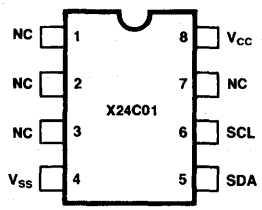
DESCRIPTION

The X24C01 is a CMOS 1024 bit serial E^2PROM, internally organized as 128 x 8. The X24C01 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics, and RR-520 for endurance cycling information for Xicor nonvolatile memories.

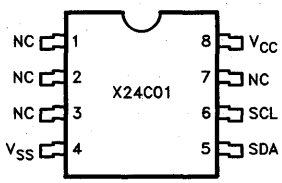
PIN CONFIGURATIONS

PLASTIC



0107-1

SOIC



0107-2

PIN NAMES

NC	No Connect
V_{SS}	Ground
V_{CC}	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24C01 ..... −10°C to +85°C
X24C01I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24C01 T_A = 0°C to +70°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
X24C01I T_A = −40°C to +85°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
V_{CC} range for the X24C01 and X24C01I are defined in the Ordering Information table.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current		1	mA	SCL = CMOS Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V_{CC} − 0.3V
I_{SB1}(1)	V_{CC} Standby Current		100	μA	SCL = SDA = V_{CC}, All Other Inputs = GND or V_{CC}, V_{CC} = 5V ±10%
I_{SB2}(1)	V_{CC} Standby Current		50	μA	SCL = SDA = V_{CC}, All Other Inputs = GND or V_{CC}, V_{CC} = 3.3V ±10%
I_{LI}	Input Leakage Current		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	V_{CC} ×0.3	V	
V_{IH}(2)	Input High Voltage	V_{CC} ×0.7	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Minimum Endurance	100,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS LIMITS

X24C01 T_A = 0°C to +70°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
X24C01I T_A = −40°C to +85°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
V_{CC} range for the X24C01 and X24C01I are defined in the Ordering Information table.

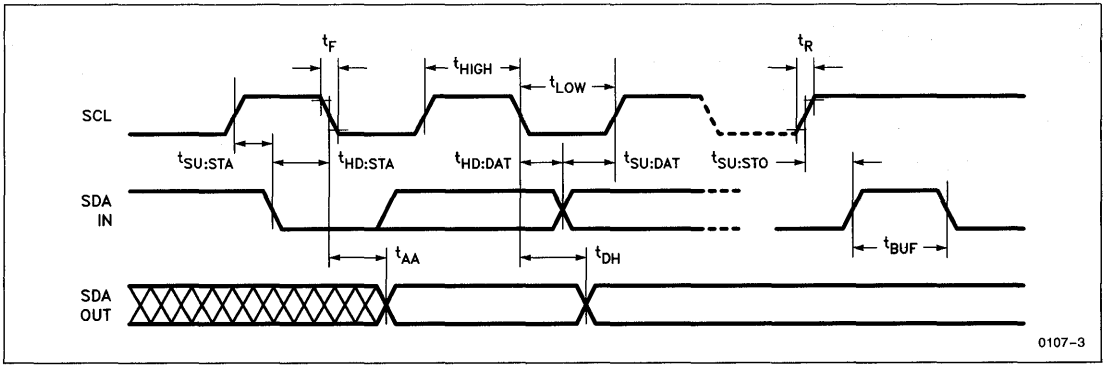
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read Operation	1	ms
t_{PUW}(4)	Power-Up to Write Operation	5	ms

Bus Timing



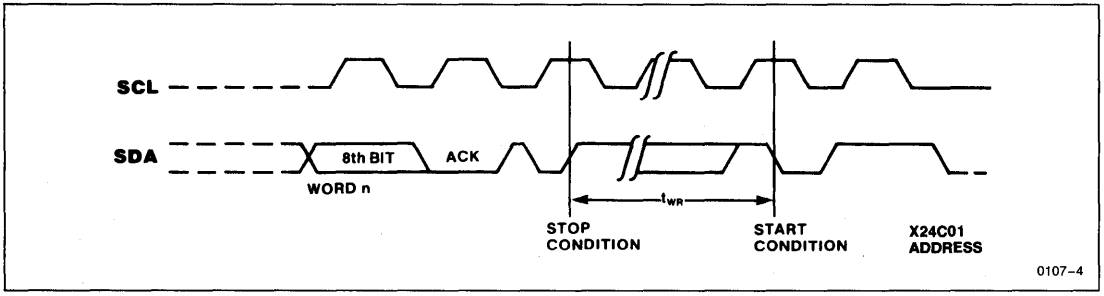
Note: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DEVICE OPERATION

The X24C01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C01 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Figure 1: Data Validity

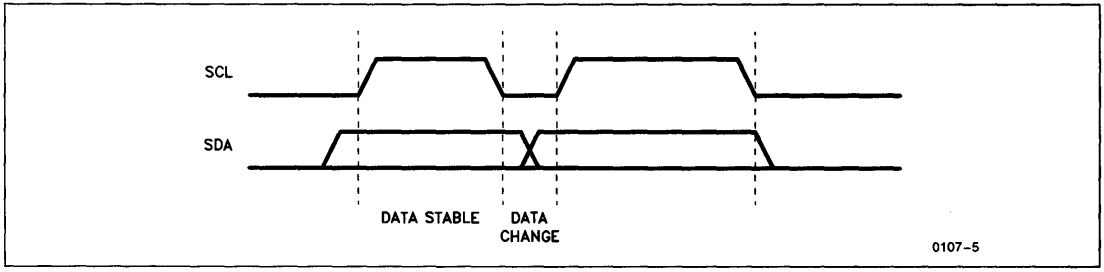
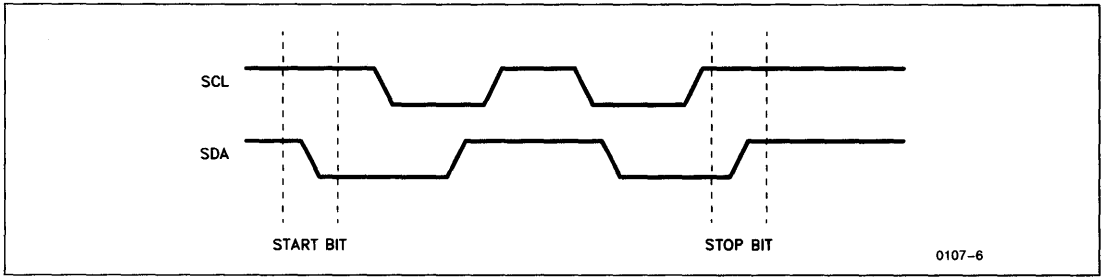


Figure 2: Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

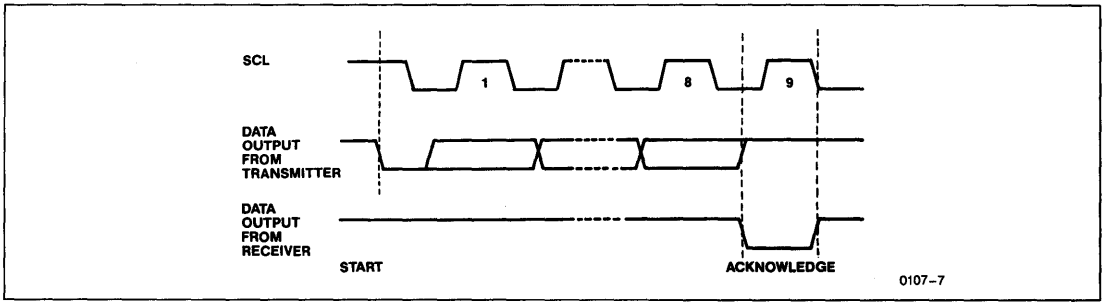
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C01 will respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/$\overline{W}$ bit. If a write operation has been selected, the X24C01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24C01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C01 will continue to transmit data. If an acknowledge is not detected, the X24C01 will terminate further data transmissions. The master must then issue a stop condition to return the X24C01 to the standby power mode and place the device into a known state.

Figure 3: Acknowledge Response From Receiver



WRITE OPERATIONS

Byte Write

To initiate a write operation, the master sends a start condition followed by a seven bit word address and a write bit. The X24C01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C01 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the X24C01 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 4 for the address, acknowledge and data transfer sequence.

Page Write

The most significant five bits of the word address define the page address. The X24C01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the master can transmit up to three more bytes. After the receipt of each data byte, the X24C01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 4: Byte Write

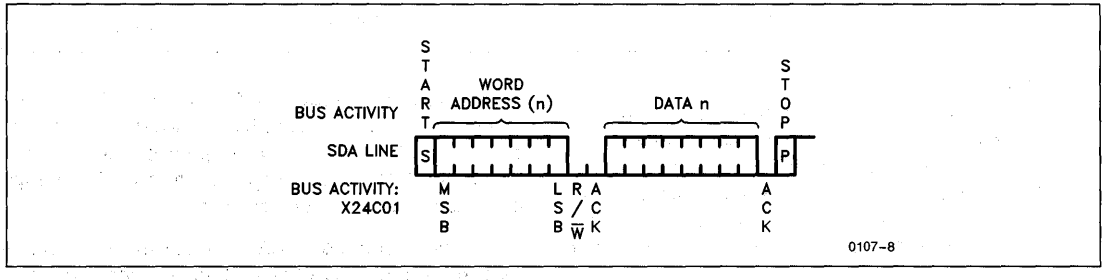
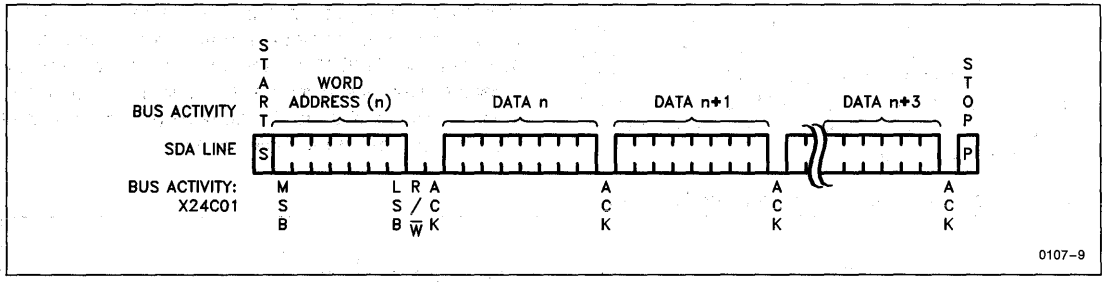


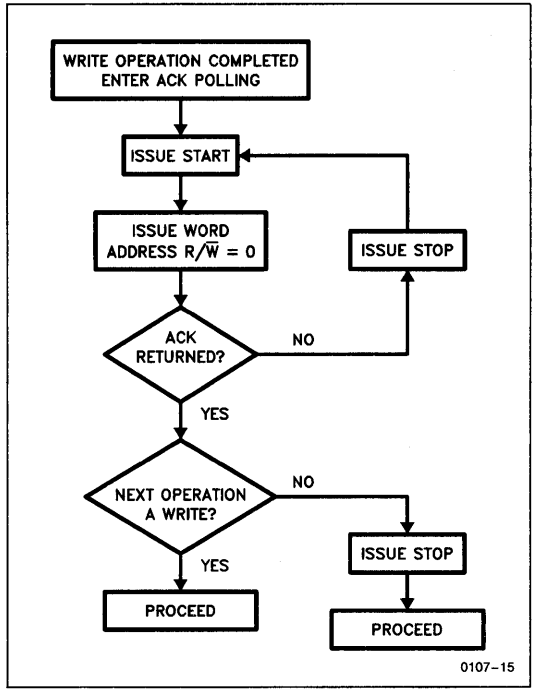
Figure 5: Page Write



Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a **write operation**. If the X24C01 is still busy with the write operation no ACK will be returned. If the X24C01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

Flow 1: ACK Polling Sequence



READ OPERATIONS

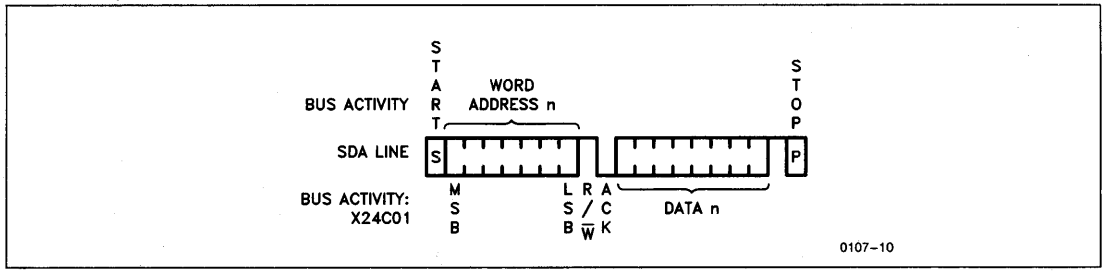
Read operations are initiated in the same manner as write operations with exception that the R/$\overline{W}$ bit of the word address is set to a one. There are two basic read operations: byte read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Byte Read

To initiate a read operation, the master sends a start condition followed by a seven bit word address and a read bit. The X24C01 responds with an acknowledge and then transmits the eight bits of data. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 6 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 6: Byte Read



Sequential Read

Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C01 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 127) the counter "rolls over" to zero and the X24C01 continues to output data for each acknowledge received. Refer to Figure 7 for the address, acknowledge and data transfer sequence.

Figure 7: Sequential Read

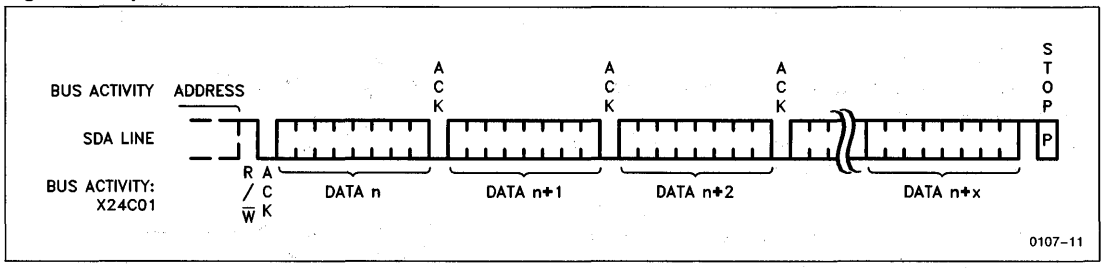
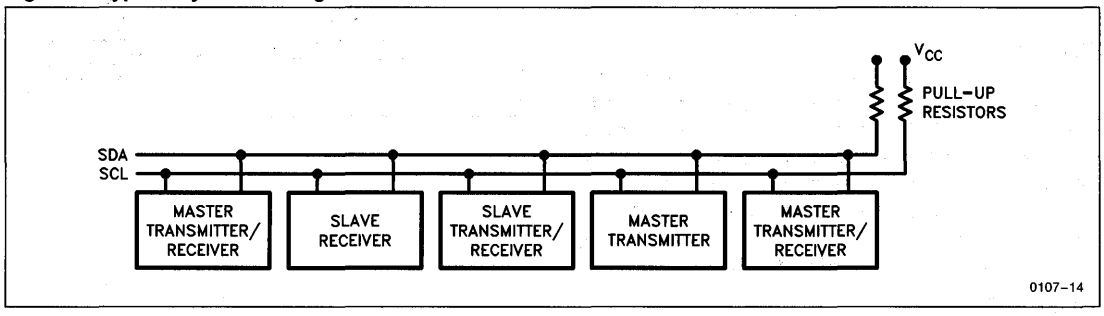
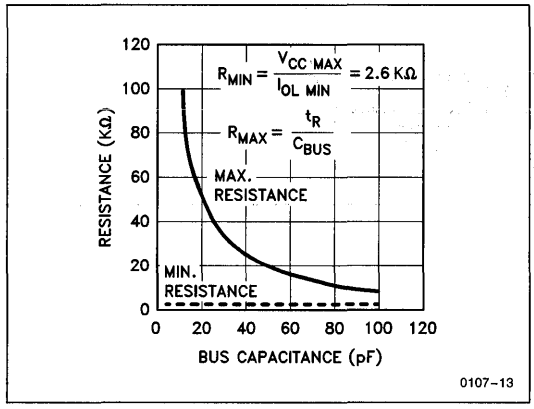


Figure 8: Typical System Configuration



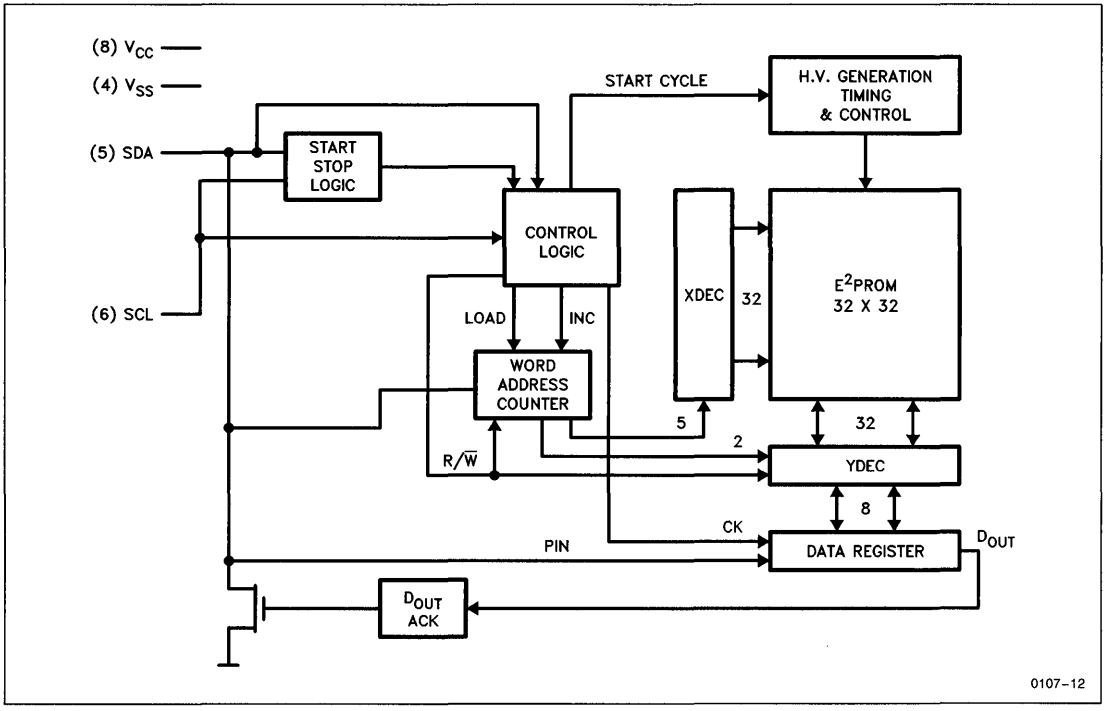
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

FUNCTIONAL DIAGRAM



NOTES

Xicor®

2K	Commercial Industrial	X24C02 X24C02I	256 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **Low Power CMOS**
  - **—Active Current Less Than 1 mA**
  - **—Standby Current Less Than 50 μA**
- **Internally Organized 256 x 8**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **2 Wire Serial Interface**
  - **—Bidirectional Data Transfer Protocol**
- **Four Byte Page Write Operation**
  - **—Minimizes Total Write Time Per Byte**
- **High Reliability**
  - **—Endurance: 100,000 Cycles Per Byte**
  - **—Data Retention: 100 Years**
- **New Hardwire - Write Control Function**

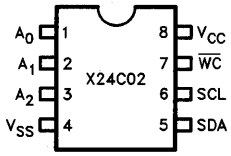
DESCRIPTION

The X24C02 is a 2048 bit serial E^2PROM, internally organized as one 256 x 8 page. The X24C02 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics, and RR-520 for endurance cycling information for Xicor nonvolatile memories.

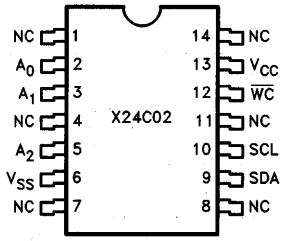
PIN CONFIGURATIONS

PLASTIC
SOIC



0120-12

SOIC



0120-13

PIN NAMES

A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{SS}	Ground
V_{CC}	+5V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24C02 ..... −10°C to +85°C
X24C02I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24C02 T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
X24C02I T_A = −40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.
V_{CC} range for the X24C02 and X24C02I are defined in the Ordering Information table.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	Power Supply Current		1	mA	SCL = CMOS Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V_{CC} − 0.3V
I_{SB}(1)	Standby Current		50	µA	SCL = SDA = V_{IH}, All Other Inputs = V_{IL} or V_{IH}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	V_{CC} ×0.3	V	
V_{IH}(2)	Input High Voltage	V_{CC} ×0.7	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	100,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS LIMITS

X24C02 T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.
X24C02I T_A = −40°C to +85°C, V_{CC} = 5V ±10%, unless otherwise specified.

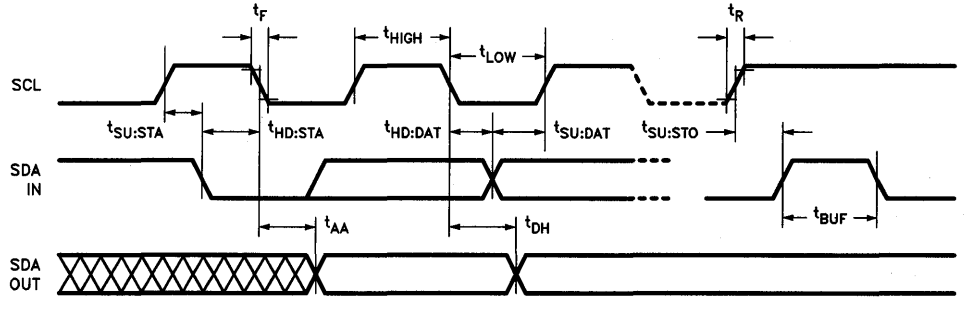
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	1	ms
t_{PUW}	Power-Up to Write Operation	5	ms

Bus Timing



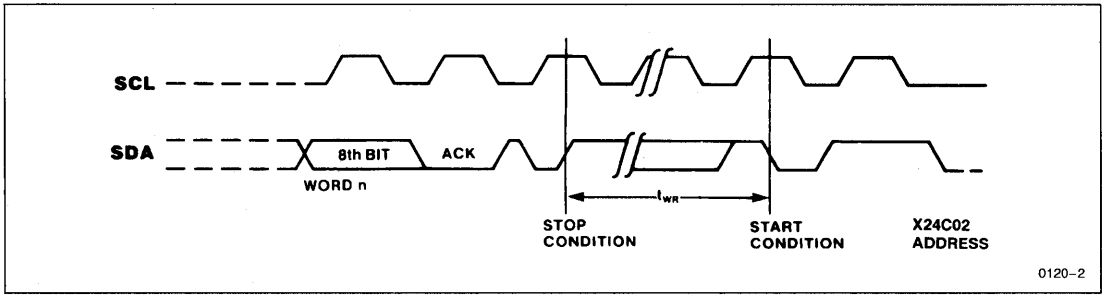
Note: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C02 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A_0, A_1, A_2)

The address inputs are used to set the least significant three bits of the seven bit slave address. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven to V_{SS} or to V_{CC}.

Write Control ($\overline{WC}$)

The Write Control input controls the ability to write to the device. When $\overline{WC}$ is LOW (tied to V_{SS}) the X24C02 will be enabled to perform write operations. When $\overline{WC}$ is HIGH (tied to V_{CC}) the internal high voltage circuitry will be disabled and all writes will be disabled.

DEVICE OPERATION

The X24C02 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C02 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C02 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 1: Data Validity

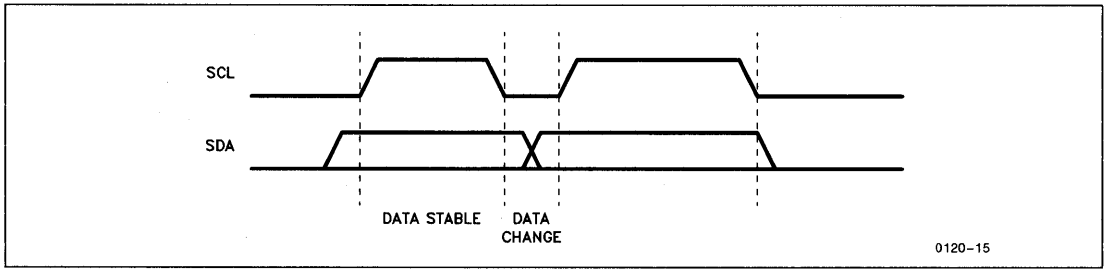
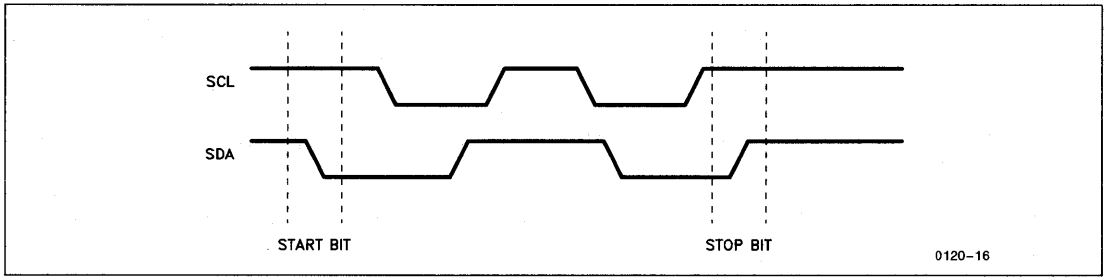


Figure 2: Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C02 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

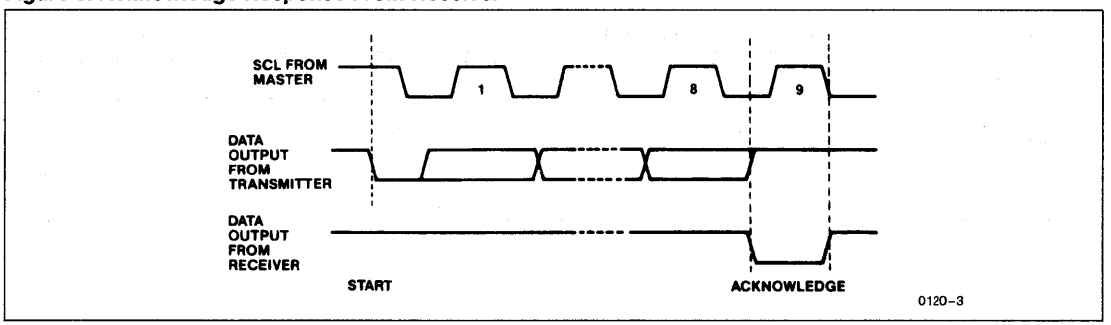
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C02 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C02 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C02 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C02 will continue to transmit data. If an acknowledge is not detected, the X24C02 will terminate further data transmissions. The master must then issue a stop condition to return the X24C02 to the standby power mode and place the device into a known state.

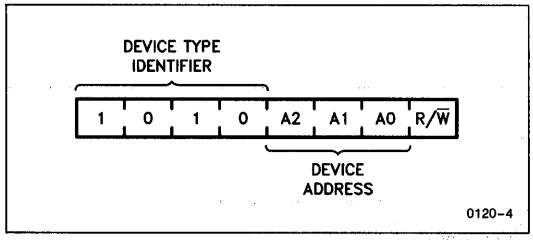
Figure 3: Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24C02 this is fixed as 1010 [B].

Figure 4: Slave Address



The next three significant bits address a particular device. A system could have up to eight X24C02 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A_0, A_1 and A_2 inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Following the start condition, the X24C02 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A_0, A_1 and A_2 inputs). Upon a correct compare the X24C02 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24C02 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24C02 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24C02 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C02 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C02 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write

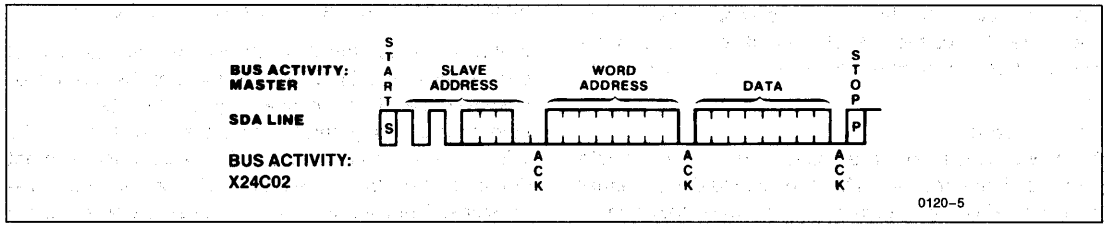
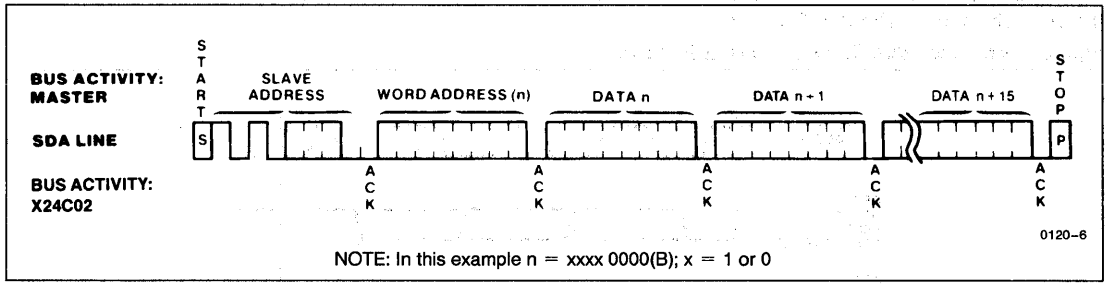


Figure 6: Page Write



NOTE: In this example n = xxxx 0000(B); x = 1 or 0

Page Write

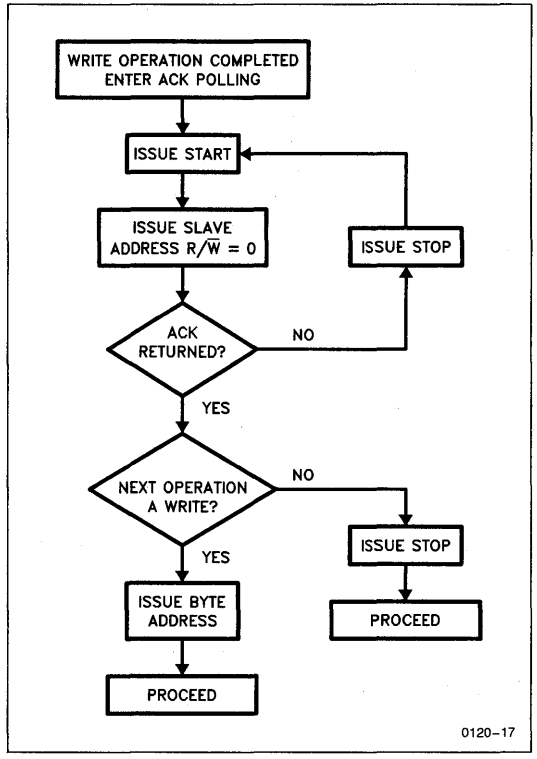
The X24C02 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24C02 will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order six bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a **write operation**. If the X24C02 is still busy with the write operation no ACK will be returned. If the X24C02 has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation.

Flow 1: ACK Polling Sequence



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C02 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the X24C02 issues an acknowledge and transmits the eight bit word during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24C02 and then by the eight bit word. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7: Current Address Read

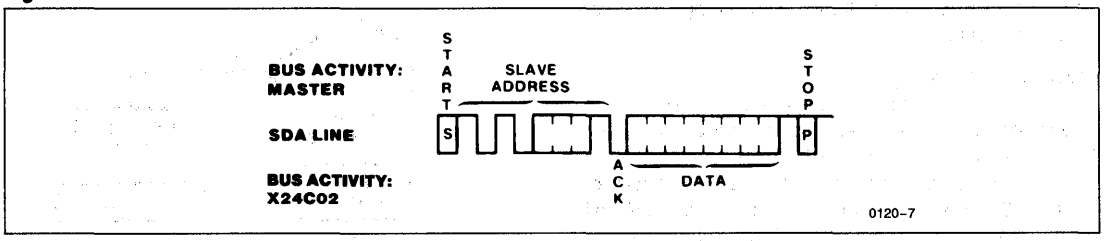
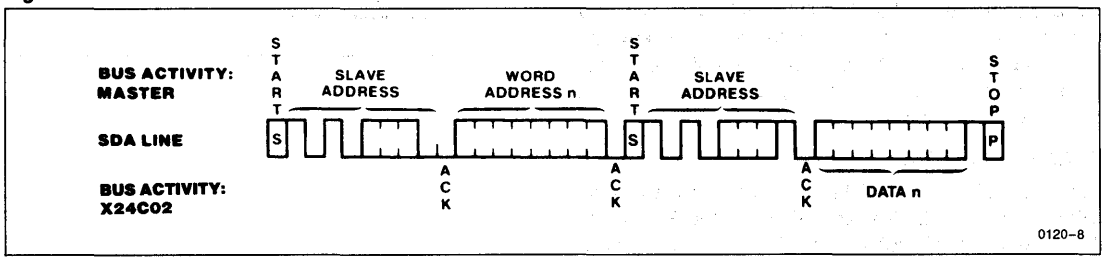


Figure 8: Random Read



Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C02 continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter "rolls over" to 0 and the X24C02 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

2

Figure 9: Sequential Read

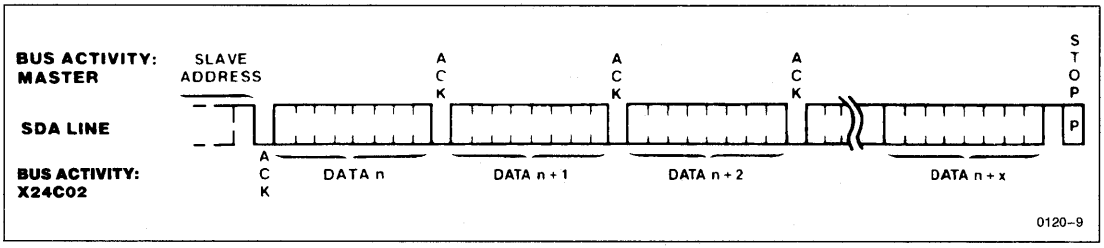
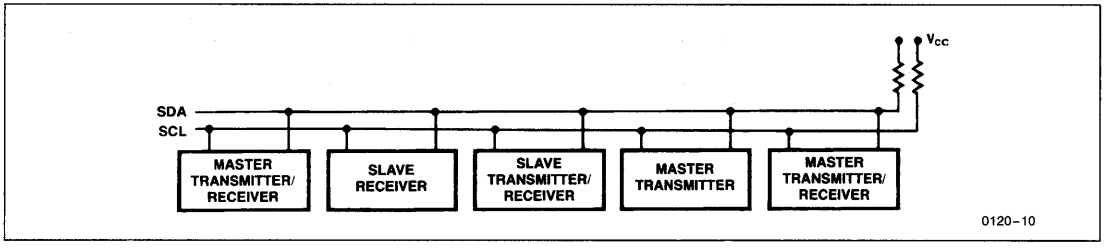
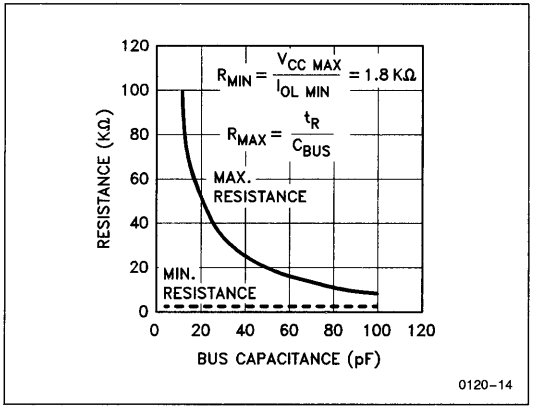


Figure 10: Typical System Configuration



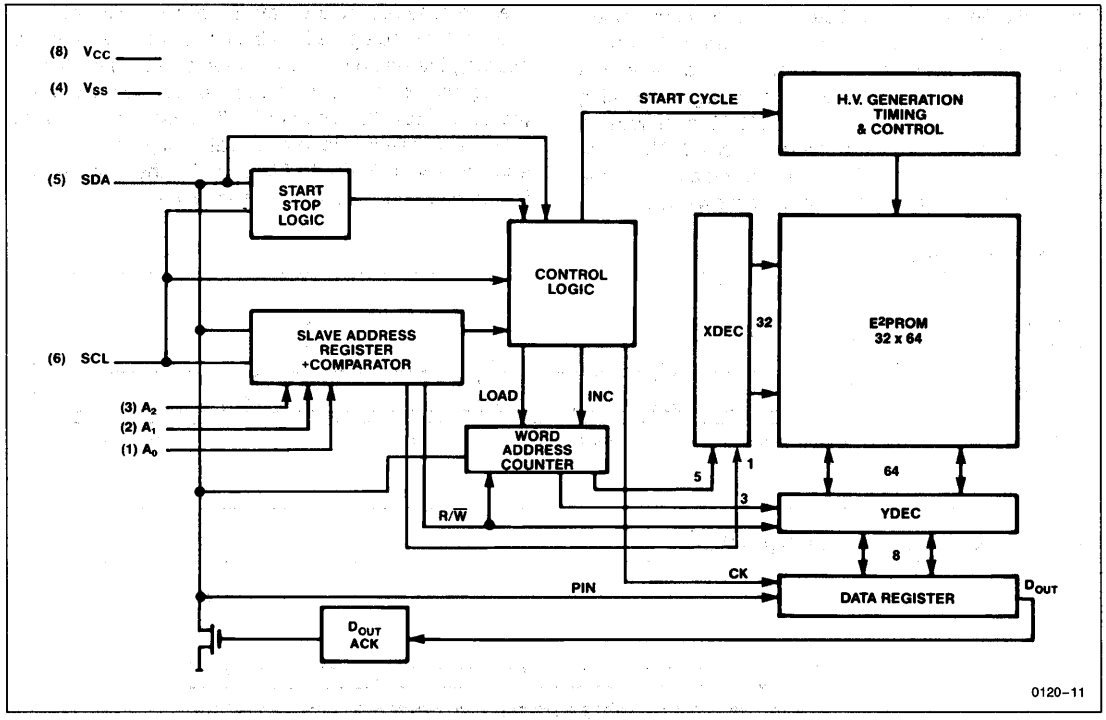
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

FUNCTIONAL DIAGRAM



Electrically Erasable PROM

TYPICAL FEATURES

- **Low Power CMOS**
  - **—Active Current Less Than 1 mA**
  - **—Standby Current Less Than 50 μA**
- **Internally Organized as Two Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
  - **—Bidirectional Data Transfer Protocol**
- **Sixteen Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **High Reliability**
  - **—Endurance: 100,000 Cycles Per Byte**
  - **—Data Retention: 100 Years**
- **8 Pin Mini-DIP and 14 Pin SOIC Packages**

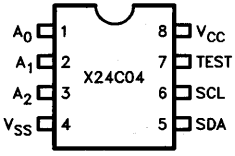
DESCRIPTION

The X24C04 is a CMOS 4096 bit serial E^2PROM, internally organized as two 256 x 8 memory banks. The X24C04 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics and RR-520 for endurance cycling information for Xicor nonvolatile memories.

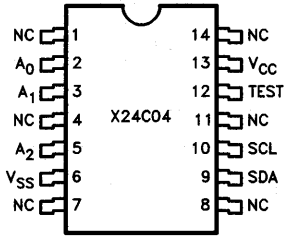
PIN CONFIGURATIONS

PLASTIC
CERDIP



0046-1

SOIC



0046-15

PIN NAMES

A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24C04 ..... −10°C to +85°C
X24C04I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24C04 T_A = 0°C to +70°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
X24C04I T_A = −40°C to +85°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
V_{CC} range for the X24C04 and X24C04I are defined in the Ordering Information table.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current		1	mA	SCL = CMOS Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V_{CC} − 0.3V
I_{SB1}(1)	V_{CC} Standby Current		150	µA	SCL = SDA = V_{CC}, All Other Inputs = GND or V_{CC}, V_{CC} = 5V ±10%
I_{SB2}(1)	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC}, All Other Inputs = GND or V_{CC}, V_{CC} = 3.3V ±10%
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	V_{CC} ×0.3	V	
V_{IH}(2)	Input High Voltage	V_{CC} ×0.7	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Minimum Endurance	100,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS LIMITS

X24C04 T_A = 0°C to +70°C, V_{CC} = 3V to 6V, unless otherwise specified.
X24C04I T_A = −40°C to +85°C, V_{CC} = 3V to 6V, unless otherwise specified.
V_{CC} range for the X24C04 and X24C04I are defined in the Ordering Information table.

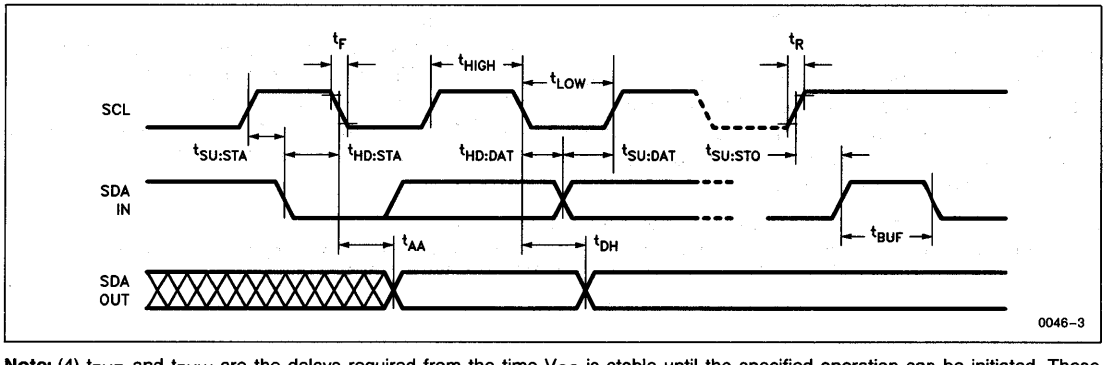
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	1	ms
t_{PUW}	Power-Up to Write Operation	5	ms

Bus Timing



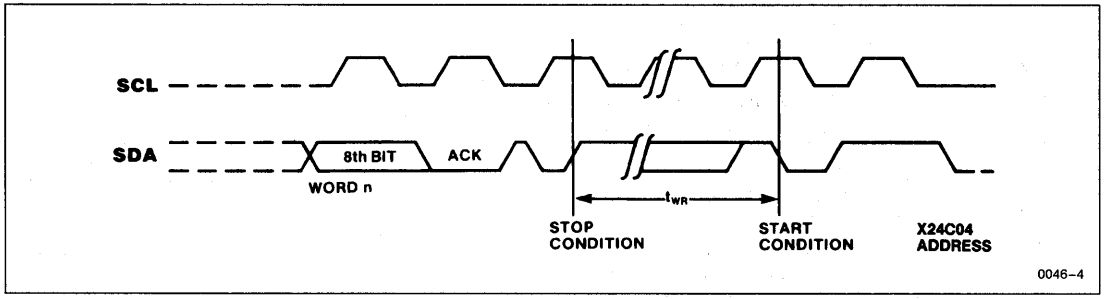
Note: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C04 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

Address (A_0)

A_0 is unused by the X24C04, however, it must be tied to V_{SS} to insure proper device operation.

Address (A_1, A_2)

The Address inputs are used to set the least significant two bits of the six bit slave address. These inputs can be used static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If driven they must be driven to V_{CC} or to V_{SS}.

DEVICE OPERATION

The X24C04 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C04 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C04 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Figure 1: Data Validity

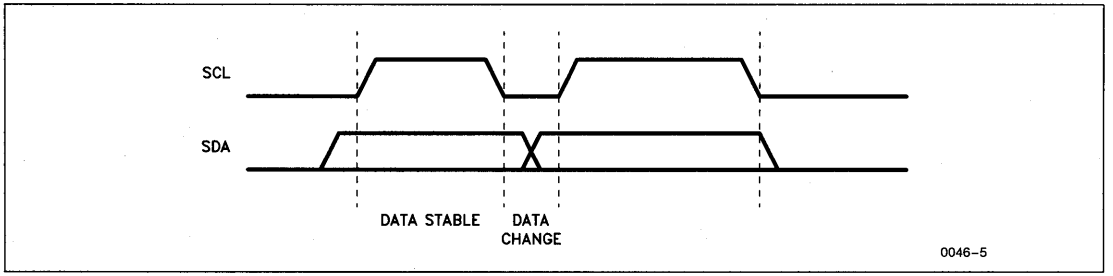
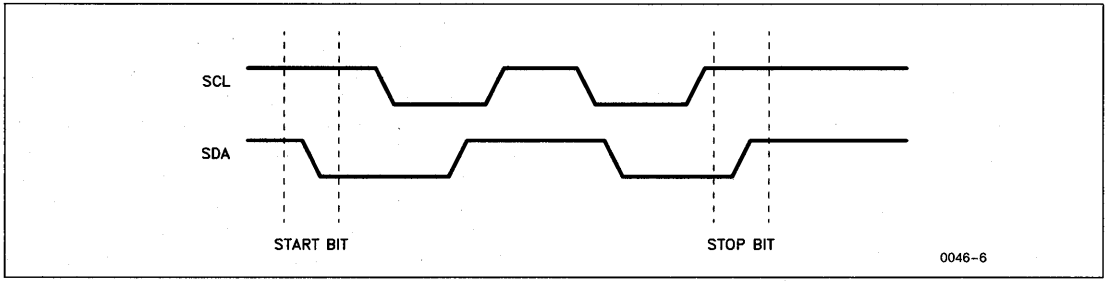


Figure 2: Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

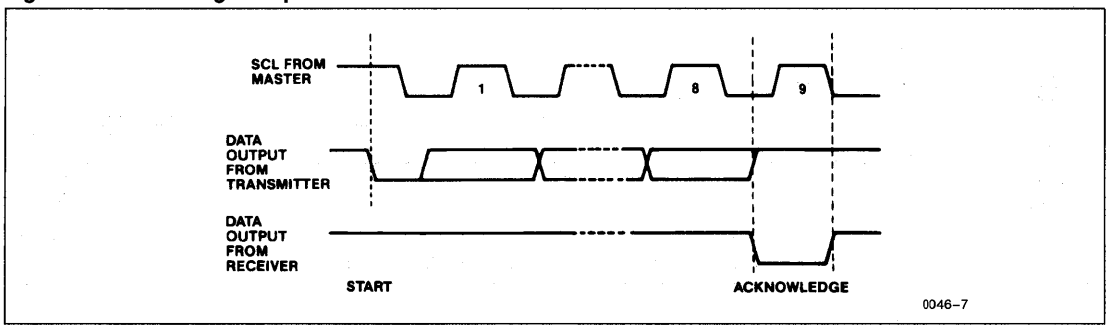
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C04 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C04 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C04 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C04 will continue to transmit data. If an acknowledge is not detected, the X24C04 will terminate further data transmissions. The master must then issue a stop condition to return the X24C04 to the standby power mode and place the device into a known state.

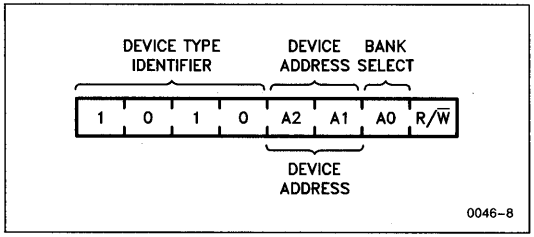
Figure 3: Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24C04 this is fixed as 1010[B].

Figure 4: Slave Address



The next two significant bits address a particular device. A system could have up to four X24C04 devices on the bus (see Figure 10). The four addresses are defined by the state of the A_1 and A_2 inputs.

The next bit of the slave address field (bit 1) is the bank select bit. It is used by the host to toggle between the two 256 x 8 banks of memory. This is, in effect the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Following the start condition, the X24C04 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A_1 and A_2 inputs). Upon a correct compare the X24C04 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24C04 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24C04 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24C04 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C04 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write

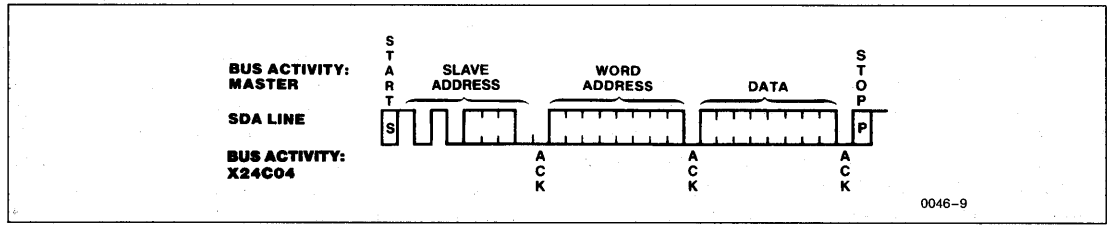
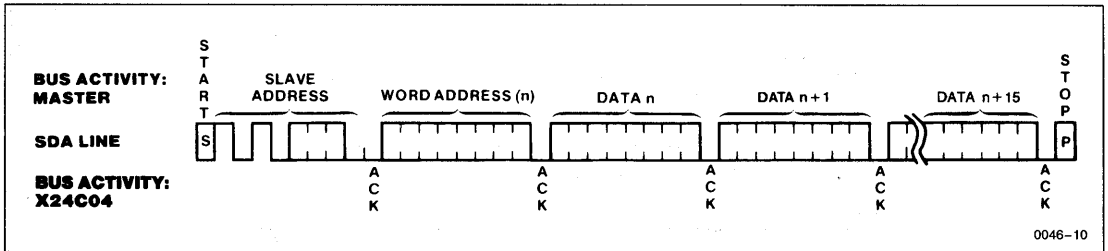


Figure 6: Page Write



NOTE: In this example n = XXXX 0000(B); X = 1 or 0

Page Write

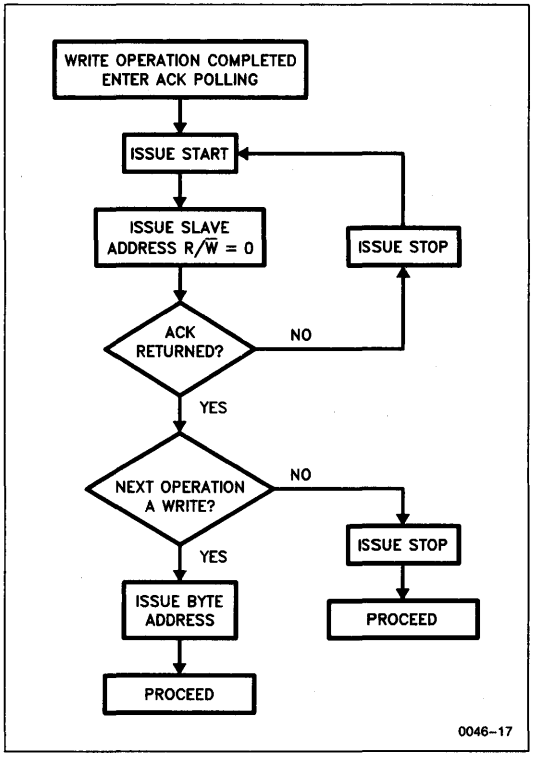
The X24C04 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C04 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C04 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a **write operation**. If the X24C04 is still busy with the write operation no ACK will be returned. If the X24C04 has completed the **write operation** an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

Flow 1: ACK Polling Sequence



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C04 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X24C04 issues an acknowledge and transmits the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24C04 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7: Current Address Read

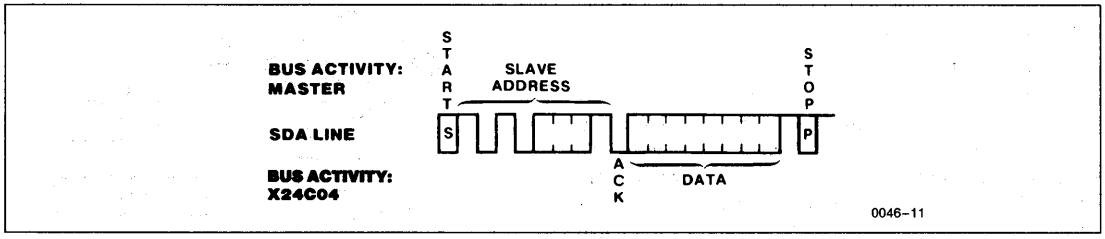
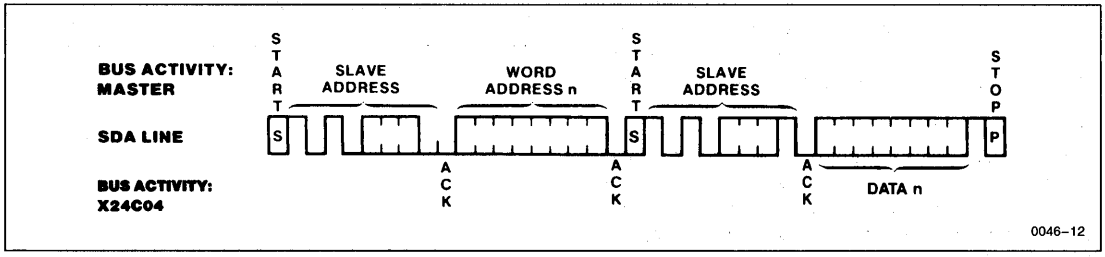


Figure 8: Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C04 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 511), the counter "rolls over" to address 0 and the X24C04 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9: Sequential Read

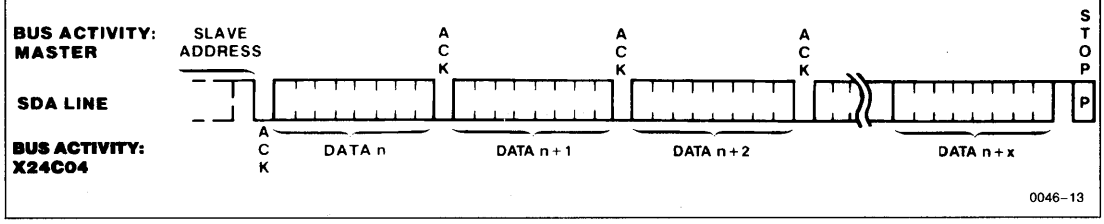
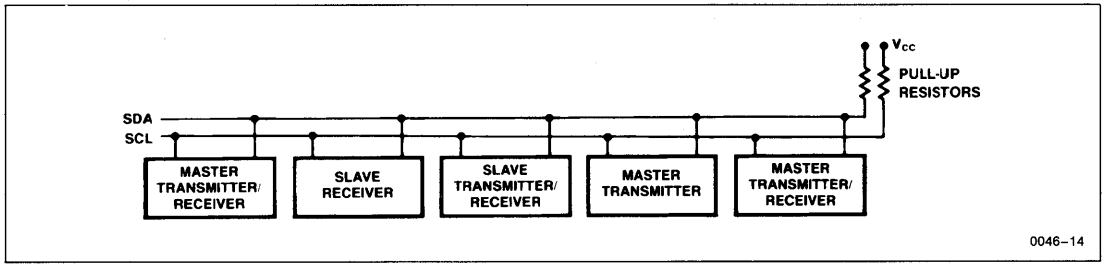
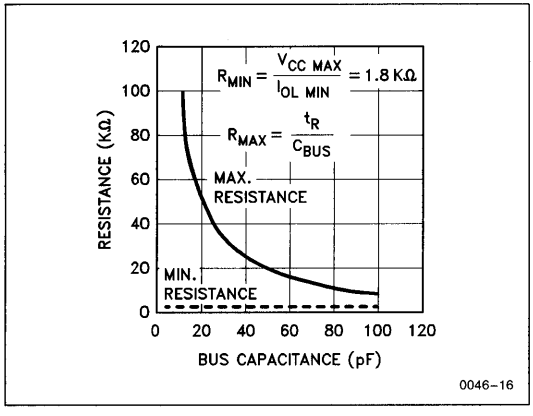


Figure 10: Typical System Configuration



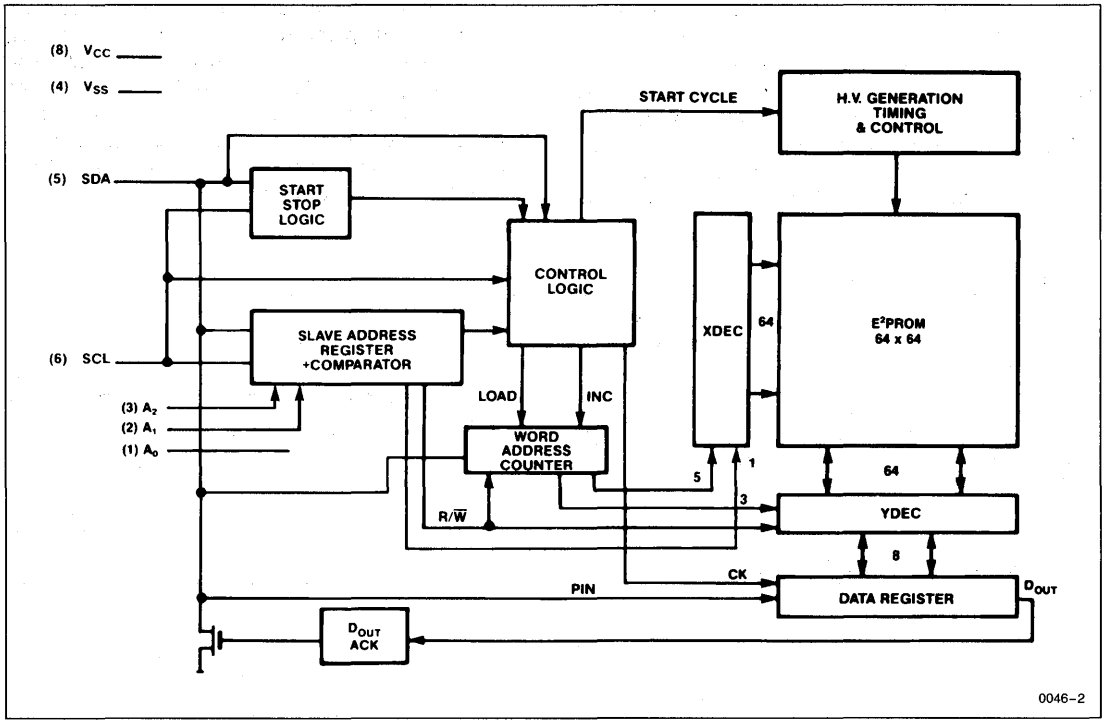
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

FUNCTIONAL DIAGRAM



Electrically Erasable PROM

TYPICAL FEATURES

- **Low Power CMOS**
  - **—Active Current Less Than 1 mA**
  - **—Standby Current Less Than 50 μA**
- **Internally Organized as Eight Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **Sixteen Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **High Reliability**
  - **—Endurance: 10,000 Cycles Per Byte**
  - **—Data Retention: 100 Years**
- **8 Pin Mini-DIP and 14 Pin SOIC Packages**

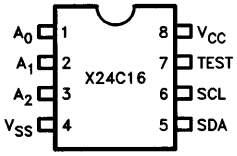
DESCRIPTION

The X24C16 is a CMOS 16,384 bit serial E^2PROM, internally organized as eight 256 x 8 memory banks. The X24C16 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics, and RR-520 for endurance cycling information for Xicor nonvolatile memories.

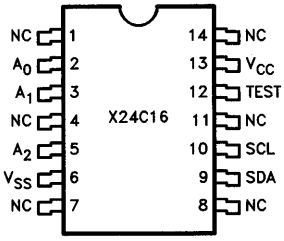
PIN CONFIGURATIONS

PLASTIC CERDIP



0038-1

SOIC



0038-15

PIN NAMES

A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24C16 ..... −10°C to +85°C
X24C16I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24C16 T_A = 0°C to +70°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
X24C16I T_A = −40°C to +85°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
V_{CC} range for the X24C16 and X24C16I are defined in the Ordering Information table.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current		1	mA	SCL = CMOS Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V_{CC} − 0.3V
I_{SB1}(1)	V_{CC} Standby Current		150	μA	SCL = SDA = V_{CC}, All Other Inputs = GND or V_{CC}, V_{CC} = 5V ±10%
I_{SB2}(1)	V_{CC} Standby Current		50	μA	SCL = SDA = V_{CC}, All Other Inputs = GND or V_{CC}, V_{CC} = 3.3V ±10%
I_{LI}	Input Leakage Current		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	V_{CC} ×0.3	V	
V_{IH}(2)	Input High Voltage	V_{CC} ×0.7	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Minimum Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS LIMITS

X24C16 T_A = 0°C to +70°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
X24C16I T_A = −40°C to +85°C, V_{CC} = 3V to 5.5V, unless otherwise specified.
V_{CC} range for the X24C16 and X24C16I are defined in the Ordering Information table.

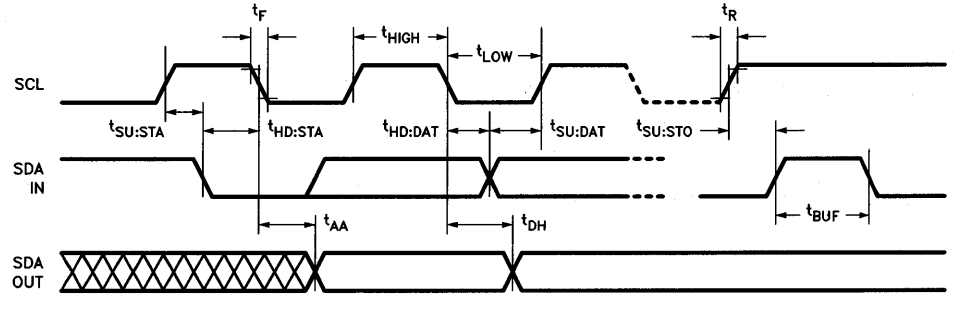
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Power-Up Timing(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	1	ms
t_{PUW}	Power-Up to Write Operation	5	ms

Bus Timing



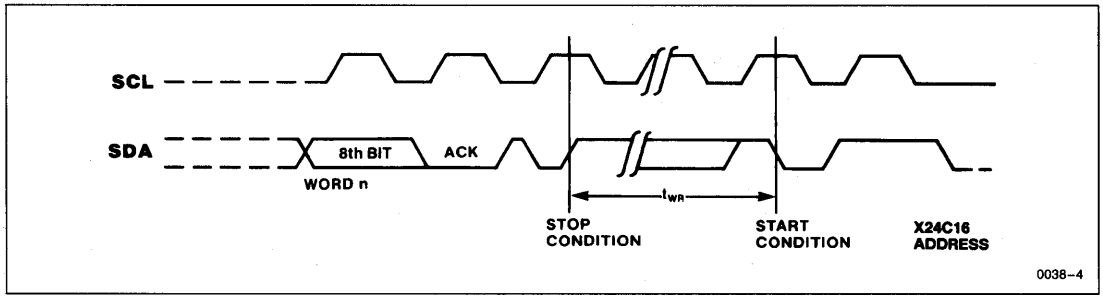
Note: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}(6)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C16 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

Address (A_0, A_1, A_2)

The A_0, A_1 and A_2 inputs are unused by the X24C16, however, they must be tied to V_{SS} to insure proper device operation.

DEVICE OPERATION

The X24C16 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C16 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C16 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Figure 1: Data Validity

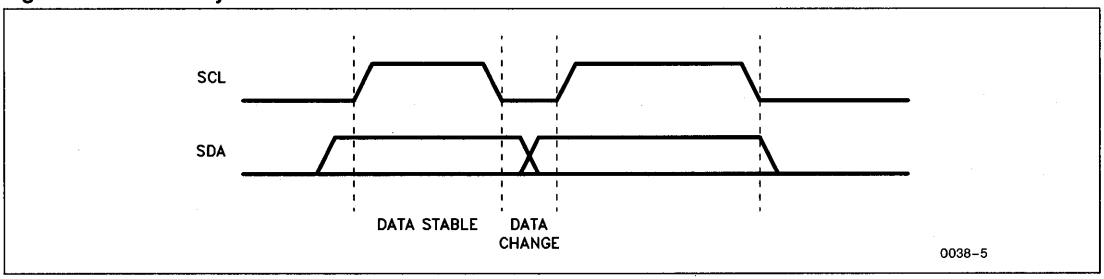
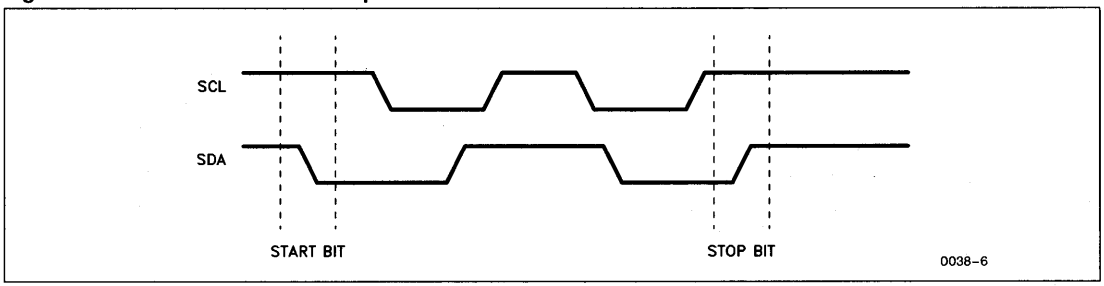


Figure 2: Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

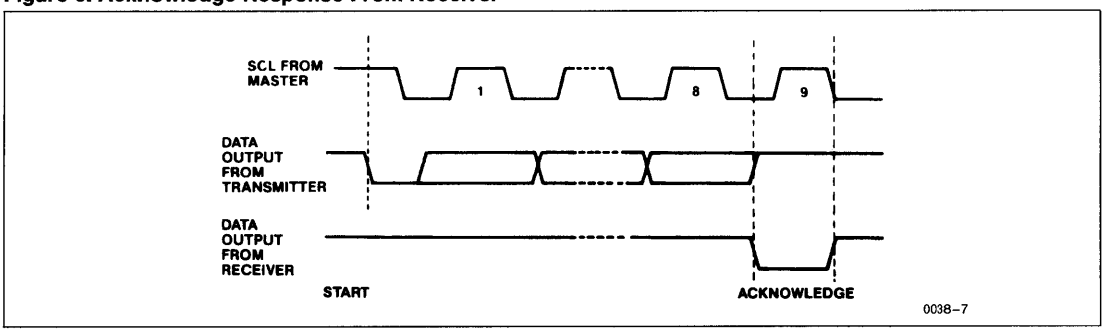
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C16 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C16 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C16 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C16 will continue to transmit data. If an acknowledge is not detected, the X24C16 will terminate further data transmissions. The master must then issue a stop condition to return the X24C16 to the standby power mode and place the device into a known state.

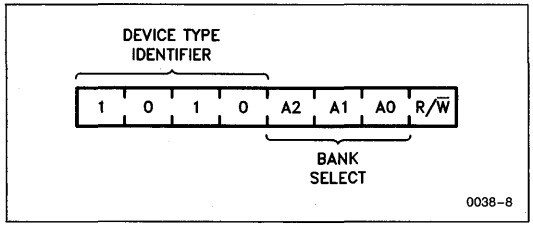
Figure 3: Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24C16 this is fixed as 1010[B].

Figure 4: Slave Address



The next three bits of the slave address field are the page select bits. They are used by the master device to select which of the eight 256 x 8 banks of memory are to be accessed. These bits are, in effect, the three most significant bits of the word address. It should be noted, the protocol limits the size of memory to eight pages of 256 words; therefore, the protocol can support only one X24C16 per system.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

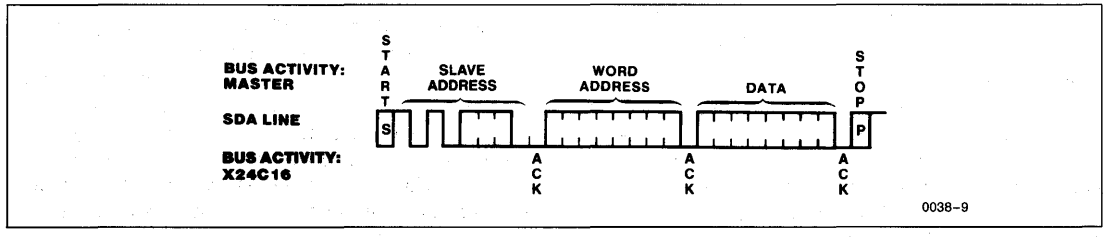
Following the start condition, the X24C16 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24C16 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24C16 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24C16 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the X24C16 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C16 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write



Page Write

The X24C16 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C16 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the word address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C16 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a **write operation**. If the X24C16 is still busy with the write operation no ACK will be returned. If the X24C16 has completed the **write operation** an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

Flow 1: ACK Polling Sequence

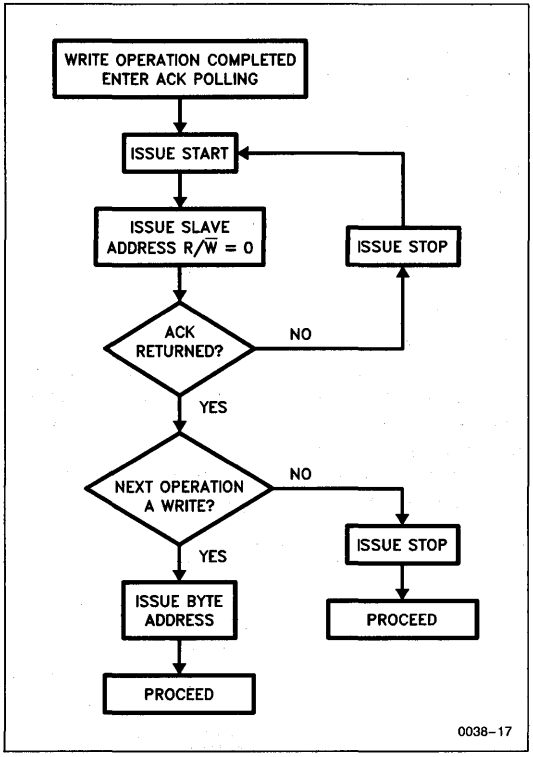
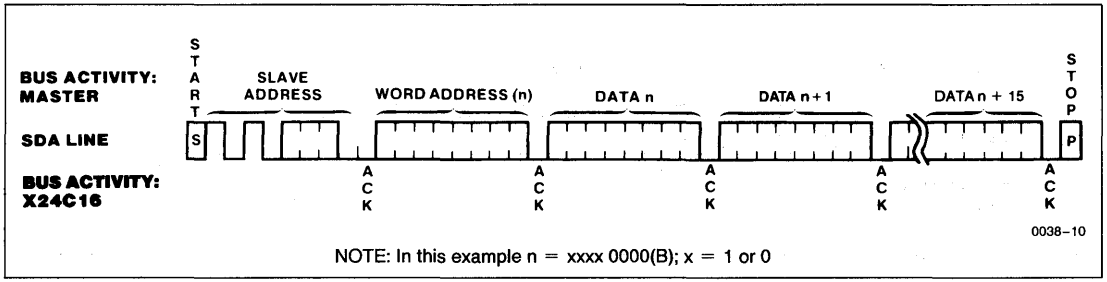


Figure 6: Page Write



NOTE: In this example n = xxxx 0000(B); x = 1 or 0

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C16 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X24C16 issues an acknowledge and transmits the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24C16 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7: Current Address Read

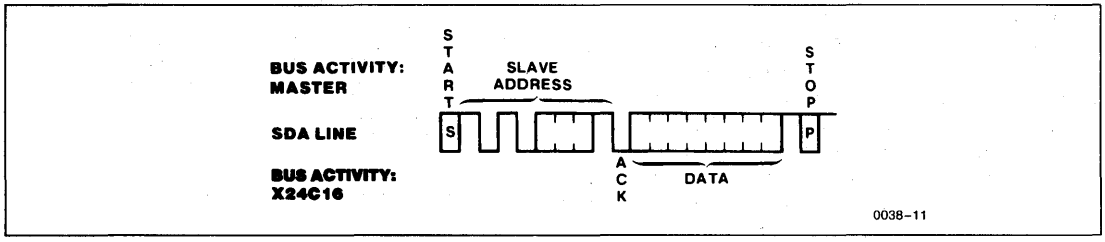
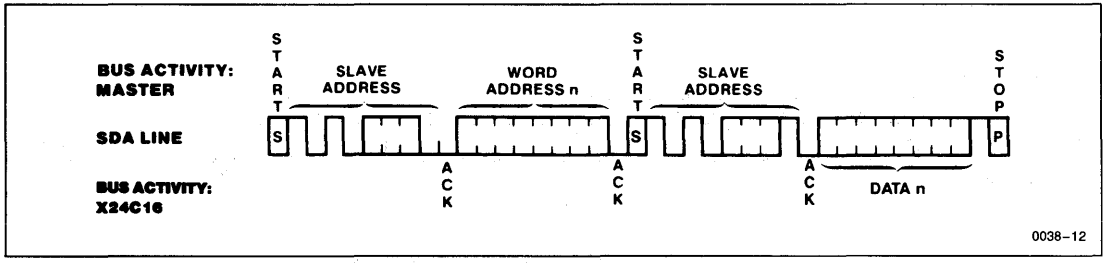


Figure 8: Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C16 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2047), the counter "rolls over" to 0 and the X24C16 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9: Sequential Read

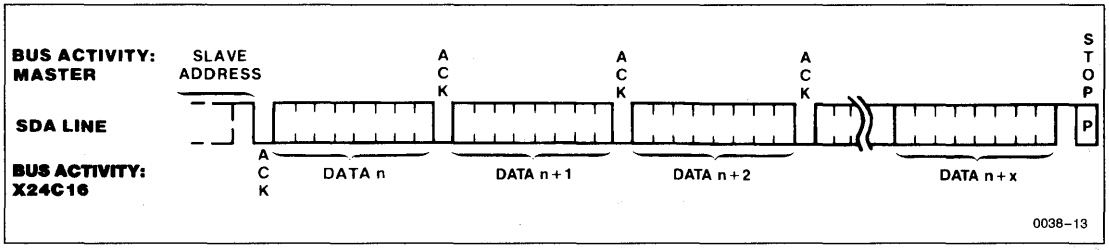
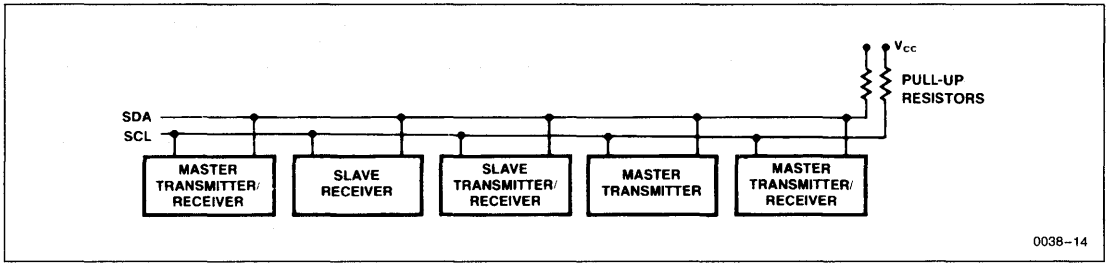
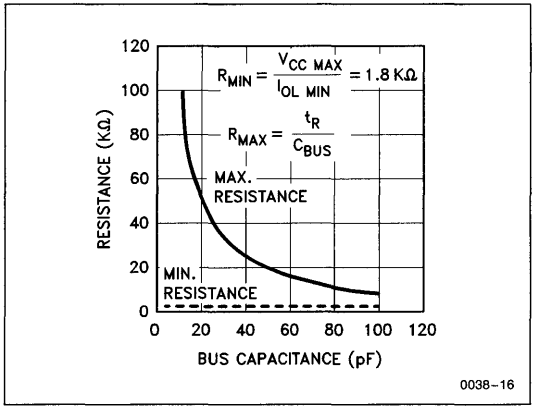


Figure 10: Typical System Configuration



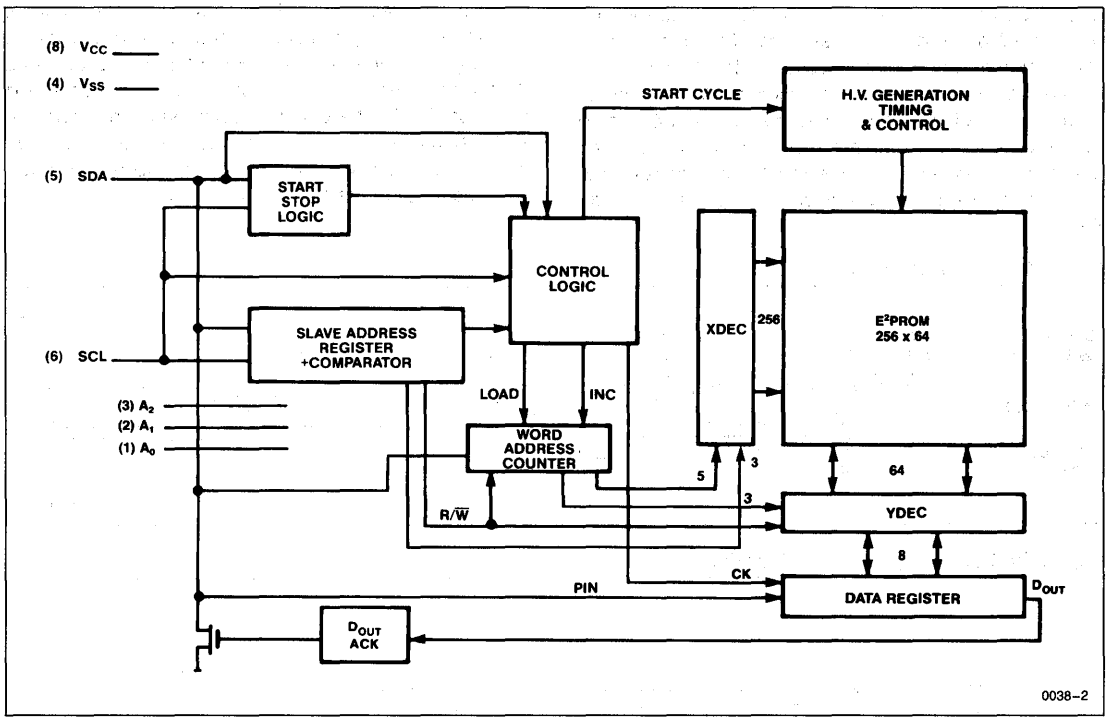
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



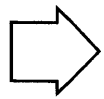
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

FUNCTIONAL DIAGRAM



X2804A, X2804AI 3-1
X2816B, X2816BI 3-9
X2816C, X2816CI 3-19
X2864A, X2864AI 3-29
X2864B, X2864BI 3-39
X2864H, X2864HI 3-47
X28C64, X28C64I 3-55
X28256, X28256I 3-69
X28C256, X28C256I 3-83
X28C512, X28C512I 3-97
X28C010, X28C010I 3-111



NOVRAM* Data Sheets 1

Serial Products Data Sheets 2

E²PROM Data Sheets 3

Electrically Erasable PROM

FEATURES

- **Simple Byte Write Operation**
  - **—Internally Latched Address and Data**
  - **—Self Timed Write**
  - **—Noise Protected $\overline{WE}$ Pin**
- **Reliable N-Channel Floating Gate MOS Technology**
- **Single 5V Supply**
- **High Reliability**
  - **—Endurance: 10,000 Writes Per Byte**
  - **—Data Retention: 100 Years**
- **Byte Write Time: 10 ms Max.**
- **Fast Access Time: 250 ns Max.**
- **Low Power Dissipation**
  - **—Active Current: 80 mA Max.**
  - **—Standby Current: 50 mA Max.**

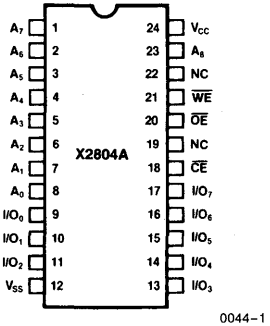
DESCRIPTION

The Xicor X2804A is a 512 x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2804A is compatible with the JEDEC approved pinout for byte-wide memories.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

3

PIN CONFIGURATION

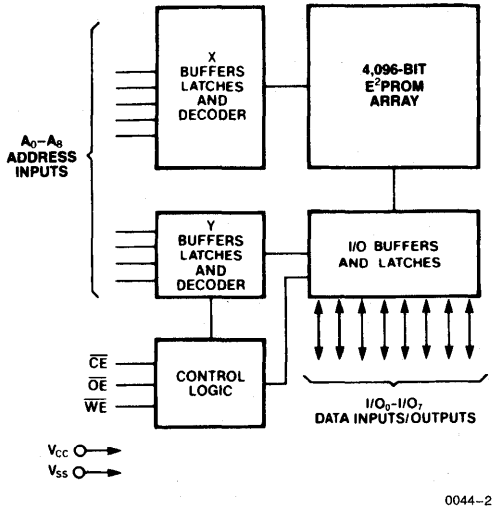


0044-1

PIN NAMES

A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0044-2

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2804A ..... −10°C to +85°C
X2804AI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2804A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2804AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2804A Limits		X2804AI Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		80		100	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50		60	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	μA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +0.5	2.2	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 μA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

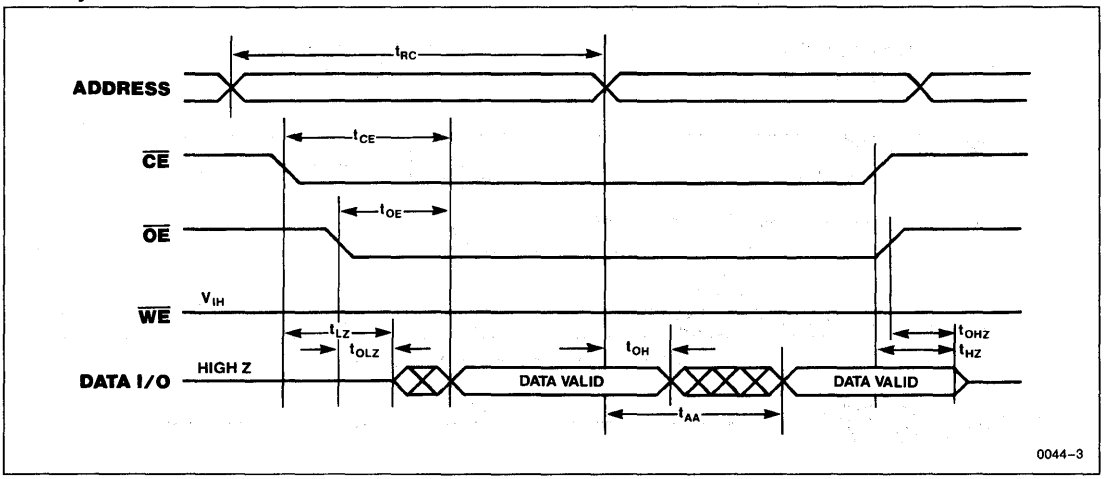
A.C. CHARACTERISTICS

X2804A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2804AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2804A-25 X2804AI-25		X2804A X2804AI		X2804A-35 X2804AI-35		X2804A-45 X2804AI-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		120		120		135		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}(3)	Chip Disable to Output in High Z	10	100	10	100	10	100	10	100	ns
t_{OLZ}(3)	Output Enable to Output in Low Z	50		50		50		50		ns
t_{OHZ}(3)	Output Disable to Output in High Z	10	100	10	100	10	100	10	100	ns
t_{OH}(3)	Output Hold from Address Change	20		20		20		20		ns

Read Cycle

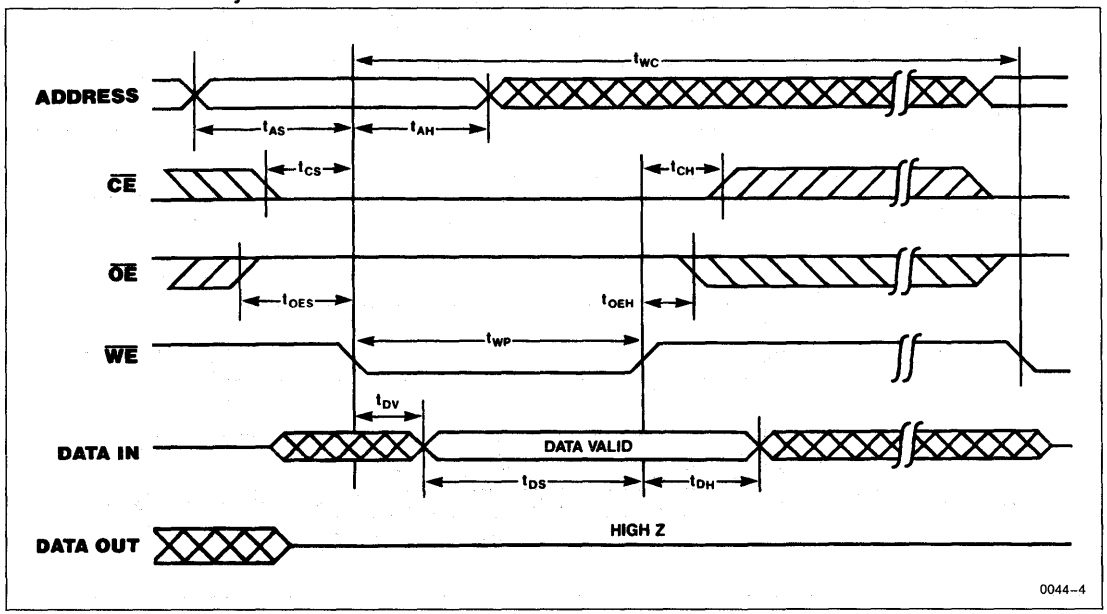


Note: (3) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min., t_{OHZ} min., t_{LZ} min. and t_{OLZ} min. are periodically sampled and are not 100% tested.

Write Cycle Limits

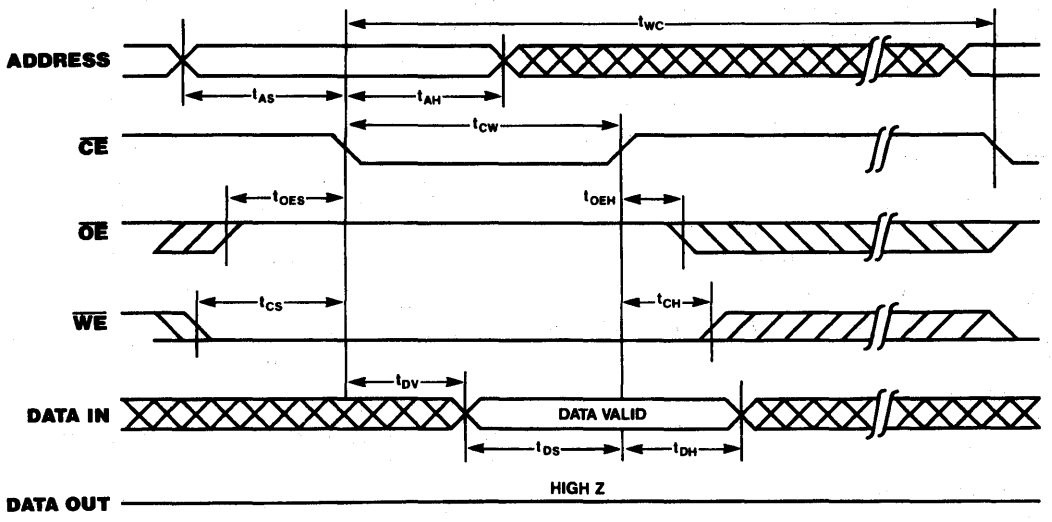
Symbol	Parameter	X2804A-25 X2804AI-25		X2804A X2804AI		X2804A-35 X2804AI-35		X2804A-45 X2804AI-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}(7)	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Setup Time	10		10		10		10		ns
t_{AH}	Address Hold Time	120		120		150		150		ns
t_{CS}	Write Setup Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable to End of Write Input	150		150		175		230		ns
t_{OES}	Output Enable Setup Time	10		10		10		10		ns
t_{OEH}	Output Enable Hold Time	10		10		10		10		ns
t_{WP}	Write Pulse Width	150		150		175		230		ns
t_{WPH}	Write Control Recovery	50		50		50		50		ns
t_{DV}	Data Valid Time		1		1		1		1	μs
t_{DS}	Data Setup Time	120		135		175		230		ns
t_{DH}	Data Hold Time	15		15		20		30		ns

$\overline{WE}$ Controlled Write Cycle



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2804A through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2804A.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X2804A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms. In order to take advantage of the typical write time as opposed to the maximum specified time, the user can poll the X2804A. The I/O pins are placed in the high impedance state during the internal programming cycle. Once the internal cycle is complete, the X2804A may be accessed without any limitations. Therefore, the host can poll an address with known data (preferably with zeroes), as soon as a compare is true, the X2804A is ready for another write cycle.

WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

Because the X2804A is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

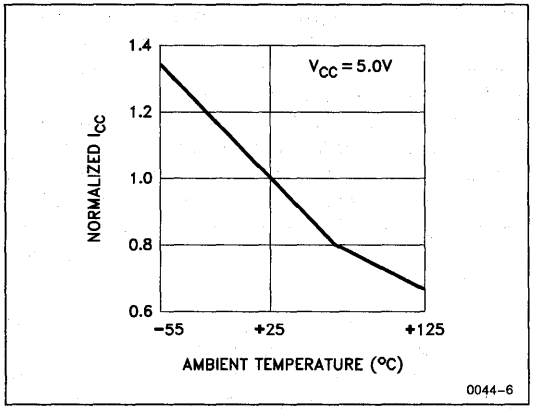
Because the X2804A has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

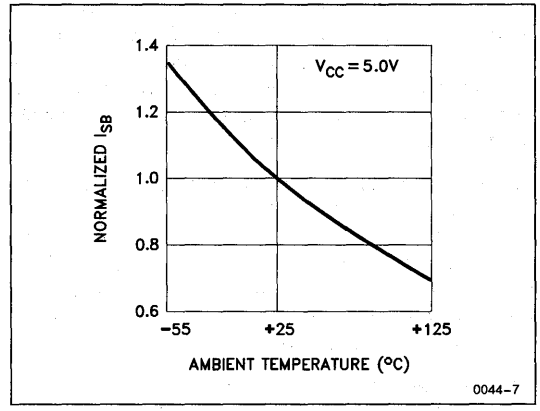
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

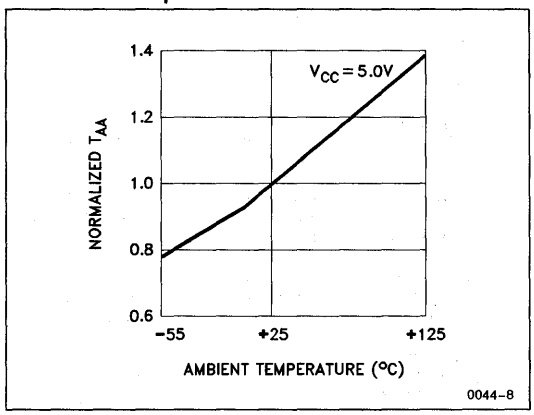
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 640 ms Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- High Reliability
  - —Endurance: 10,000 Writes Per Byte
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

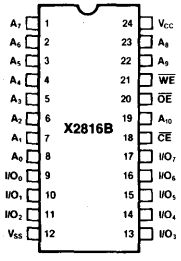
DESCRIPTION

The Xicor X2816B is a 2K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

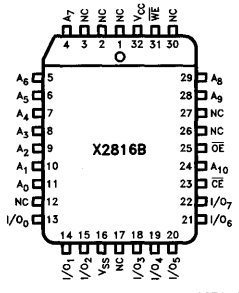
The X2816B supports a 16-byte page write operation, typically providing a 300 μs/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS



0071-1

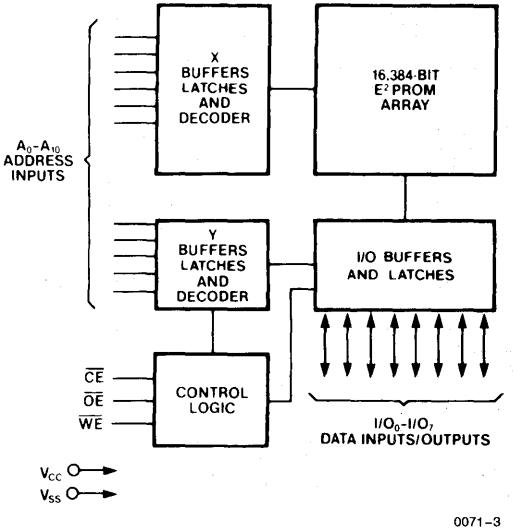


0071-2

PIN NAMES

A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0071-3

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2816B ..... −10°C to +85°C
X2816BI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2816B T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2816BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2816B/X2816B-25 Limits			X2816BI/X2816BI-25 Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	120		80	140	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		45	60		45	70	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(3)	Input Low Voltage	−1.0		0.8	−1.0		0.8	V	
V_{IH}(3)	Input High Voltage	2.0		V_{CC} +1.0	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	1	ms
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

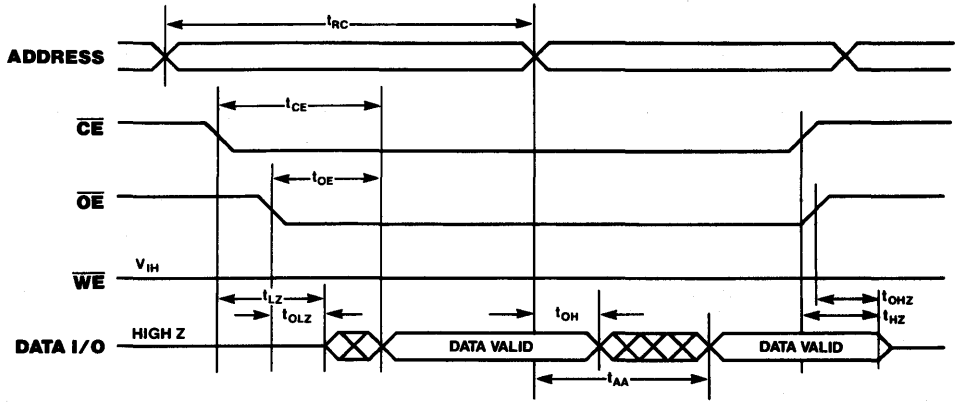
A.C. CHARACTERISTICS

X2816B T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2816BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2816B-25 X2816BI-25		X2816B X2816BI		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		ns
t_{CE}	Chip Enable Access Time		250		300	ns
t_{AA}	Address Access Time		250		300	ns
t_{OE}	Output Enable Access Time		100		100	ns
t_{LZ}(4)	Chip Enable to Output in Low Z	10		10		ns
t_{HZ}(4)	Chip Disable to Output in High Z	10	60	10	80	ns
t_{OLZ}(4)	Output Enable to Output in Low Z	10		10		ns
t_{OHZ}(4)	Output Disable to Output in High Z	10	60	10	80	ns
t_{OH}	Output Hold from Address Change	10		10		ns

Read Cycle

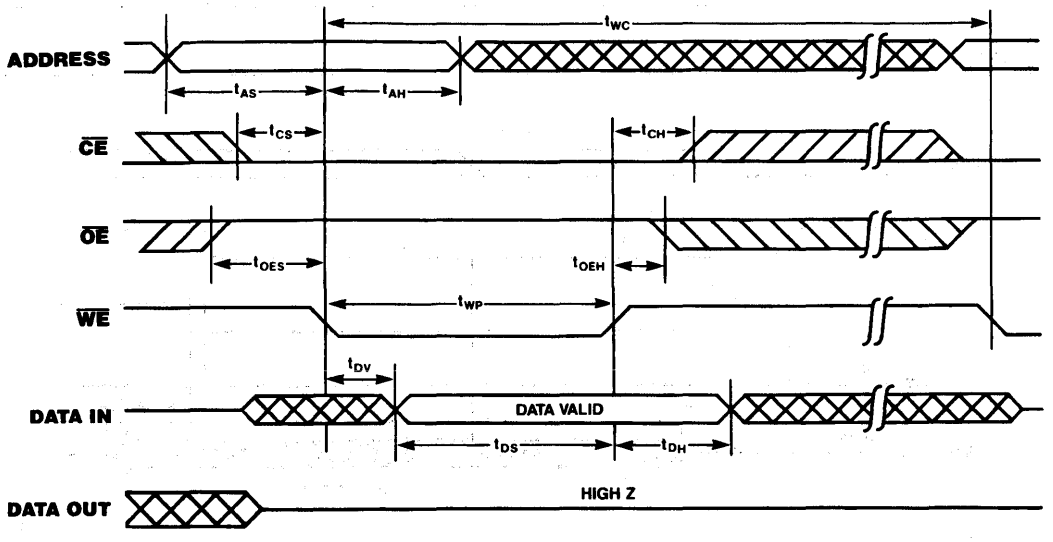


Note: (4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min., t_{OHZ} min., t_{LZ} min. and t_{OLZ} min. are periodically sampled and are not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WC}(6)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	150			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	150			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			300	ns
t_{DS}	Data Setup	100			ns
t_{DH}	Data Hold	15			ns
t_{DW}	Delay to Next Write	500			μs
t_{BLC}	Byte Load Cycle	3		20	μs

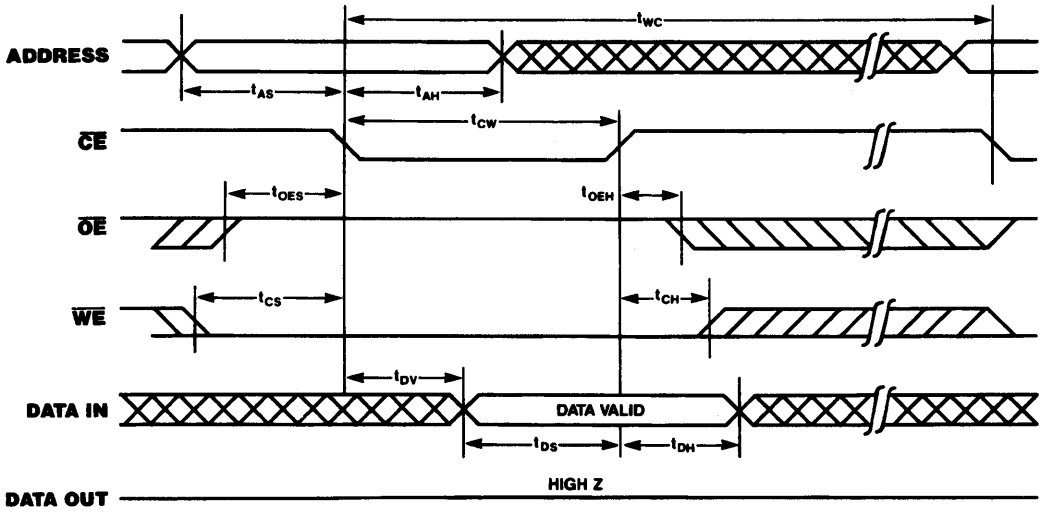
$\overline{WE}$ Controlled Write Cycle



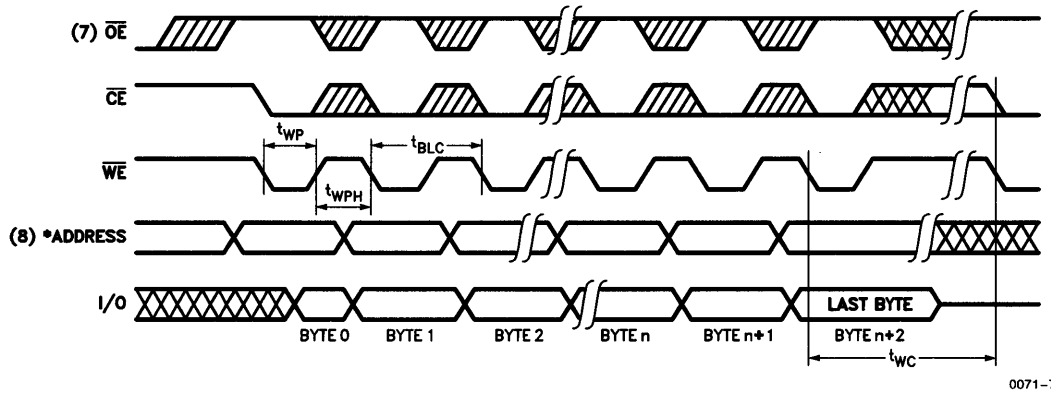
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage.

(6) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

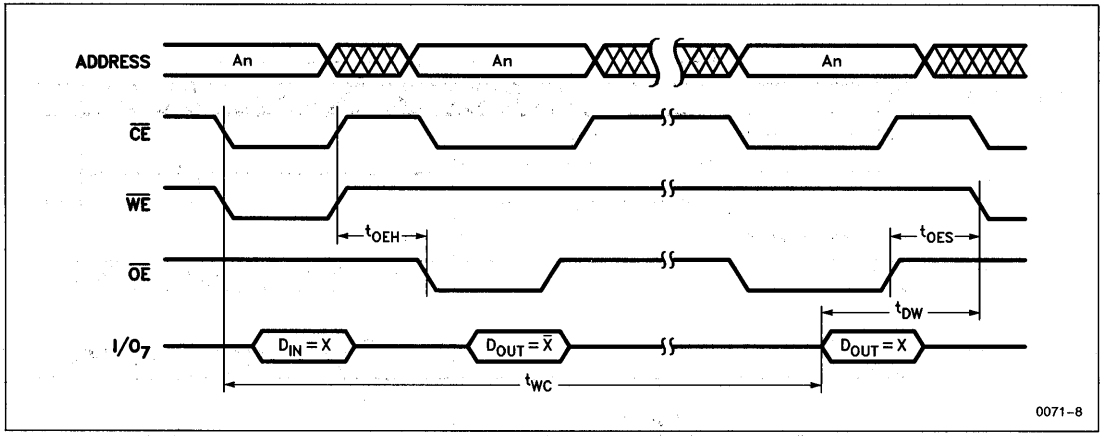


*For each successive write within the page write operation, A_4–A_{10} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[9]



Note: (9) A polling operation by definition is a read cycle and therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{10})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X2816B through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X2816B.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2816B supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X2816B allows the entire memory to be typically written in 640 ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816B prior to the commencement of the internal programming cycle. Although the host system may read data from any location in the system to transfer to the X2816B, the destination page address of the X2816B should be the same on each subsequent strobe of the $\overline{WE}$ and $\overline{CE}$ inputs. That is, A_4 through A_{10} must be the same for each transfer of data to the X2816B during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 20 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20 μs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20 μs.

$\overline{DATA}$ Polling
The X2816B features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2816B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION
There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

Because the X2816B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

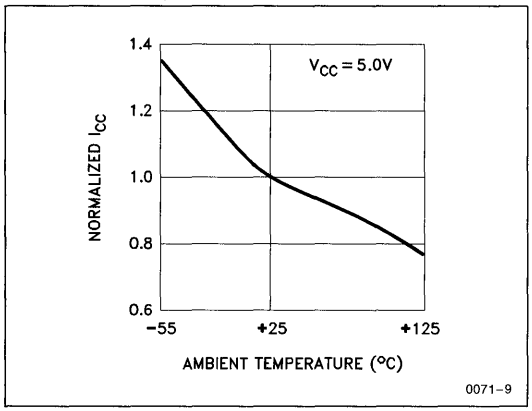
Because the X2816B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

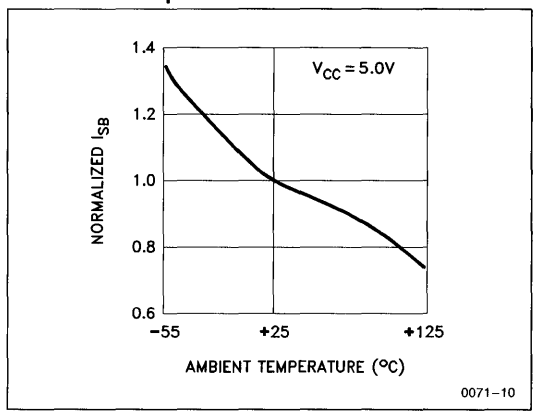
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

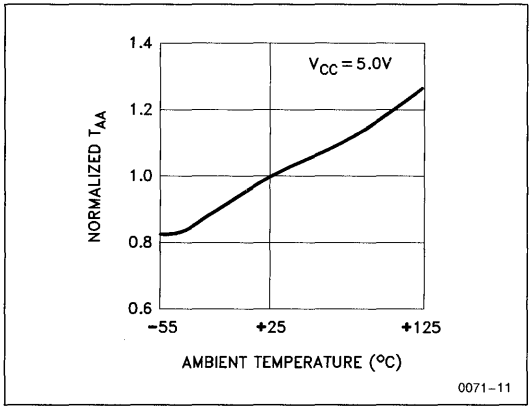
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



3

NOTES

Electrically Erasable PROM

FEATURES

- 200 ns Access Time
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 640 ms Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout
- High Reliability
  - —Endurance: 10,000 Cycles
  - —Data Retention: 100 Years

DESCRIPTION

The Xicor X2816C is a 2K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

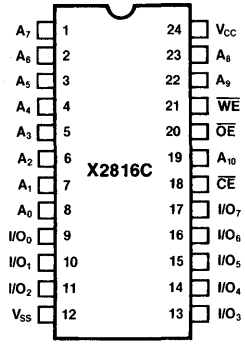
The X2816C supports a 16-byte page write operation, typically providing a 300 μs/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816C also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics for Xicor nonvolatile memories.

3

PIN CONFIGURATIONS

PLASTIC



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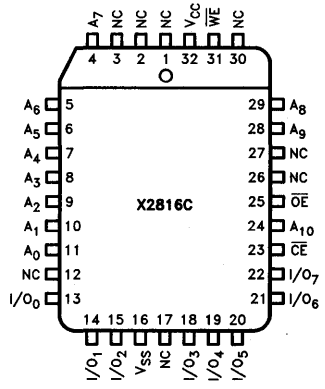
PLCC



0108-2

PIN NAMES

A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2816C ..... −10°C to +85°C
X2816CI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2816C T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2816CI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		70	110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		35	50	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit	Condition
Minimum Endurance	10,000		Cycles/Byte	Reliability Report-520
Data Retention	100		Years	Reliability Report-515

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

A.C. CHARACTERISTICS

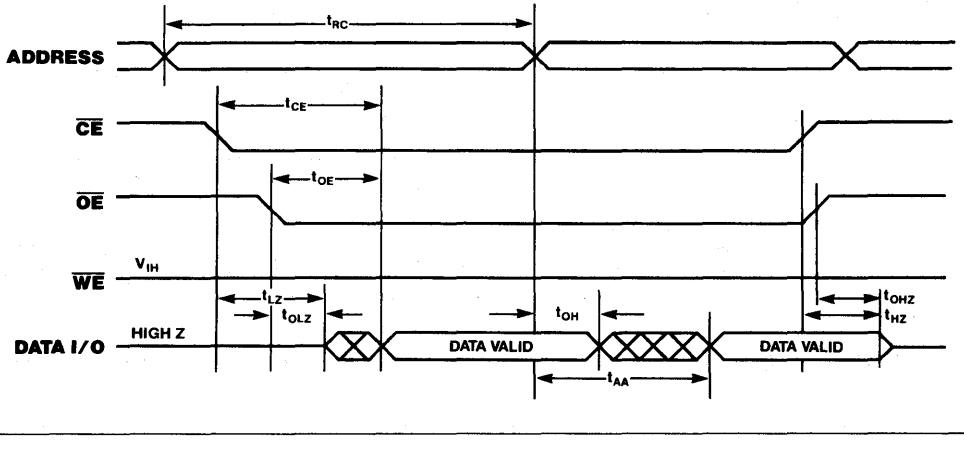
X2816C T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2816CI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

3

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	200		ns
t_{CE}	Chip Enable Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	Output Enable Access Time		100	ns
t_{LZ}(4)	Chip Enable to Output in Low Z	0		ns
t_{HZ}(5)	Chip Disable to Output in High Z	0	60	ns
t_{OLZ}(4)	Output Enable to Output in Low Z	0		ns
t_{OHZ}(5)	Output Disable to Output in High Z	0	60	ns
t_{OH}	Output Hold from Address Change	0		ns

Read Cycle



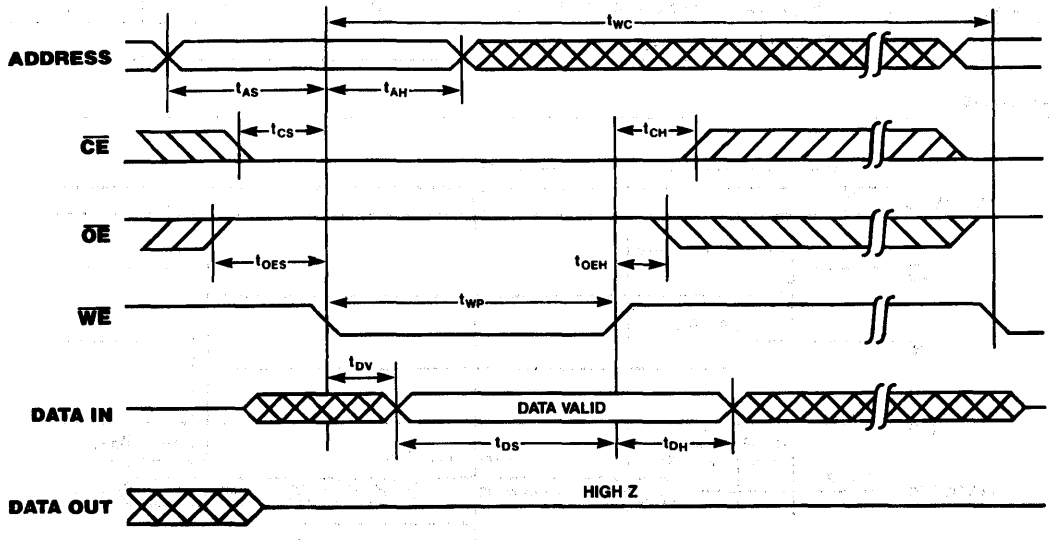
Notes: (4) t_{LZ} min. and t_{OLZ} min. are periodically sampled and not 100% tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	120			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	150			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	150			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	100			ns
t_{DH}	Data Hold	15			ns
t_{DW}	Delay to Next Write	500			µs
t_{BLC}	Byte Load Cycle	3		20	µs

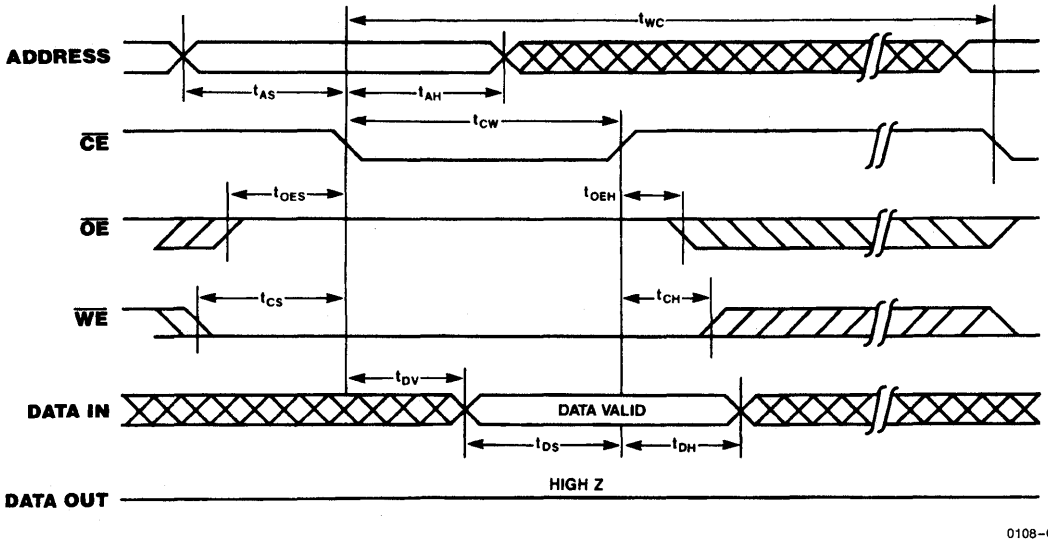
$\overline{WE}$ Controlled Write Cycle



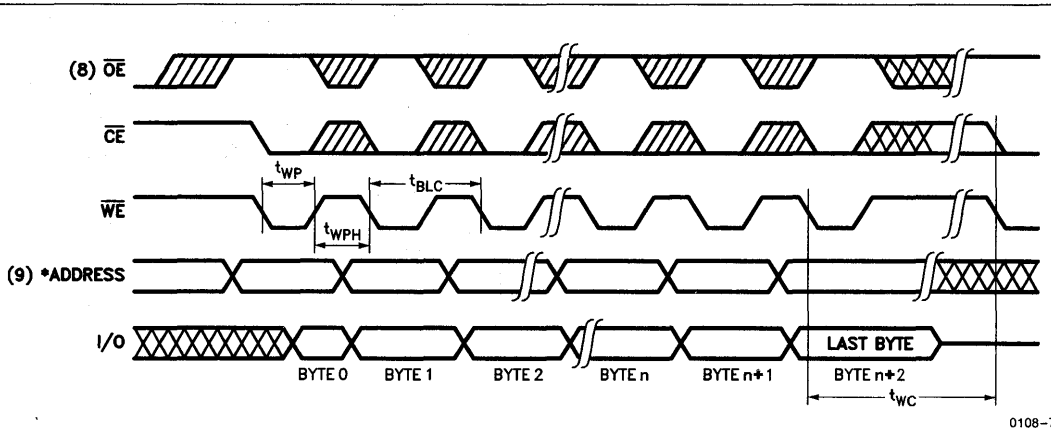
Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.

(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

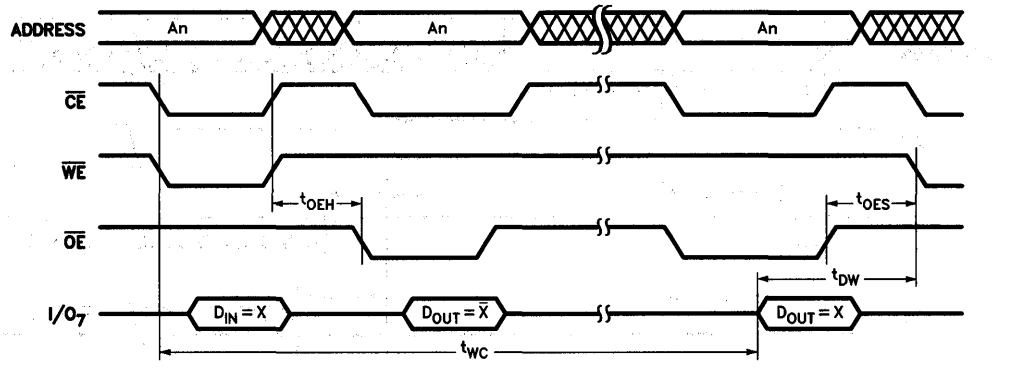


*For each successive write within the page write operation, A_4–A_{10} should be the same or writes to an unknown address could occur.

Notes: (8) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(10)



Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PIN DESCRIPTIONS

Addresses (A_0–A_{10})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X2816C through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X2816C.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2816C supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X2816C allows the entire memory to be typically written in 640 ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816C prior to the commencement of the internal programming cycle. Although the host system may read data from any location in the system to transfer to the X2816C, the destination page address of the X2816C should be the same on each subsequent strobe of the $\overline{WE}$ and $\overline{CE}$ inputs. That is, A_4 through A_{10} must be the same for each transfer of data to the X2816C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 20 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20 μs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20 μs.

$\overline{DATA}$ Polling
The X2816C features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2816C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION
There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse which is typically less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE
Xicor E^2PROMs are designed and tested for applications requiring extended endurance.

SYSTEM CONSIDERATIONS

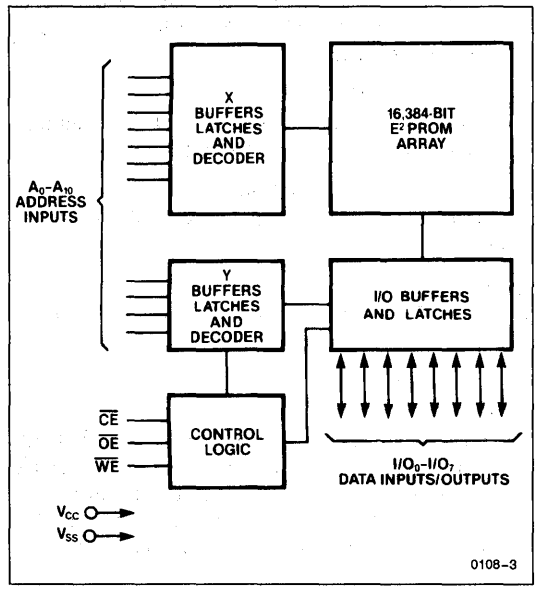
Because the X2816C is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

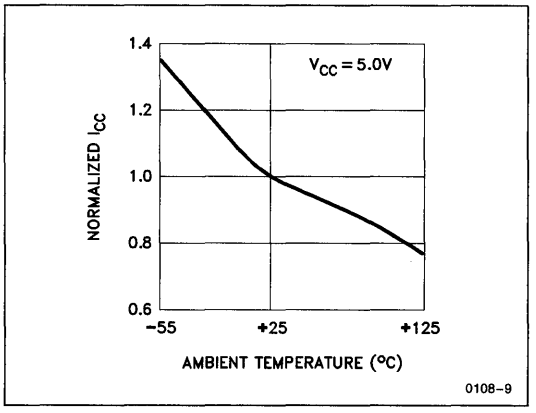
Because the X2816C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

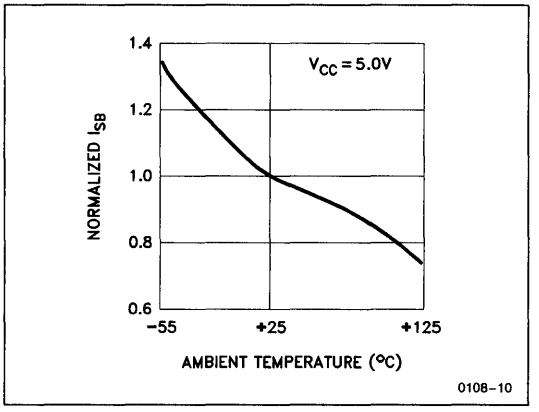
FUNCTIONAL DIAGRAM



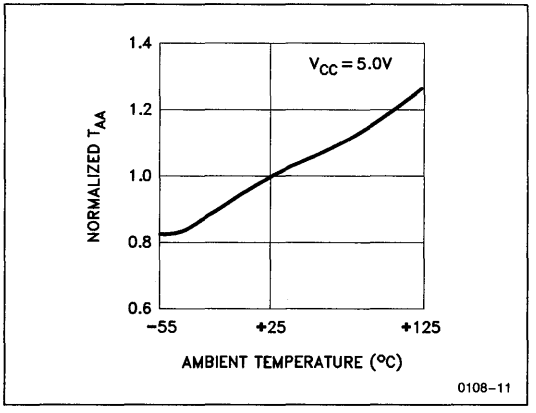
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



NOTES

Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.6 Sec. Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- DATA Polling
  - —Allows User to Minimize Write Cycle Time
- High Reliability
  - —Endurance: 10,000 Writes Per Byte
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Level WE Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

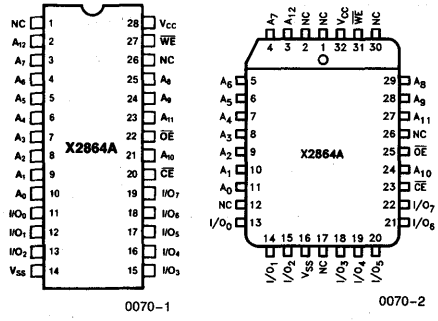
DESCRIPTION

The Xicor X2864A is a 8K x 8 E²PROM, fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2864A features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864A supports a 16-byte page write operation, effectively providing a 300 μs/byte write and enabling the entire memory to be written in less than 2.6 seconds. The X2864A also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS

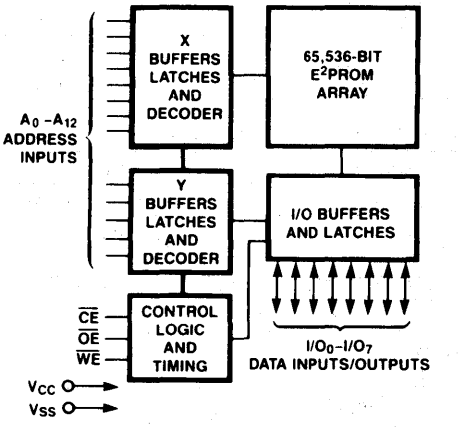


0070-1 0070-2

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0070-3

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864A ..... −10°C to +85°C
X2864AI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2864A Limits		X2864AI Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		140		140	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		60		70	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(3)	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}(3)	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	1	ms
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

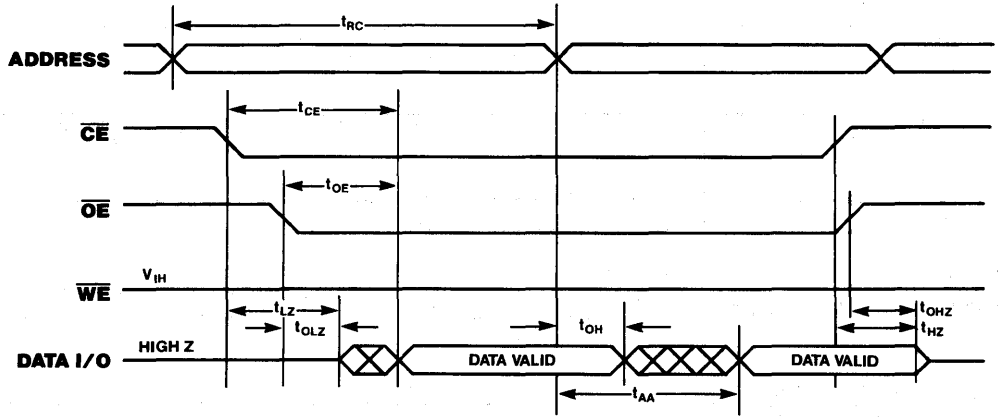
A.C. CHARACTERISTICS

X2864A T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864AI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864A-25 X2864AI-25		X2864A X2864AI		X2864A-35 X2864AI-35		X2864A-45 X2864AI-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		100		100		100		100	ns
t_{LZ}(4)	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}(4)	Chip Disable to Output in High Z	10	60	10	80	10	80	10	100	ns
t_{OLZ}(4)	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}(4)	Output Disable to Output in High Z	10	60	10	80	10	80	10	100	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns

Read Cycle

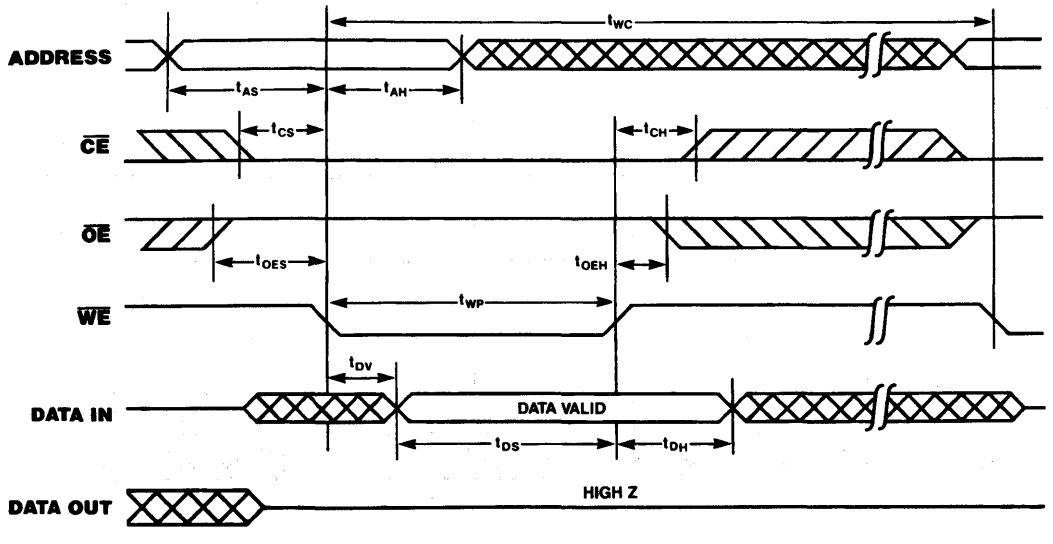


Note: (4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min., t_{OHZ} min., t_{LZ} min. and t_{OLZ} min. are periodically sampled and are not 100% tested.

Write Cycle Limits

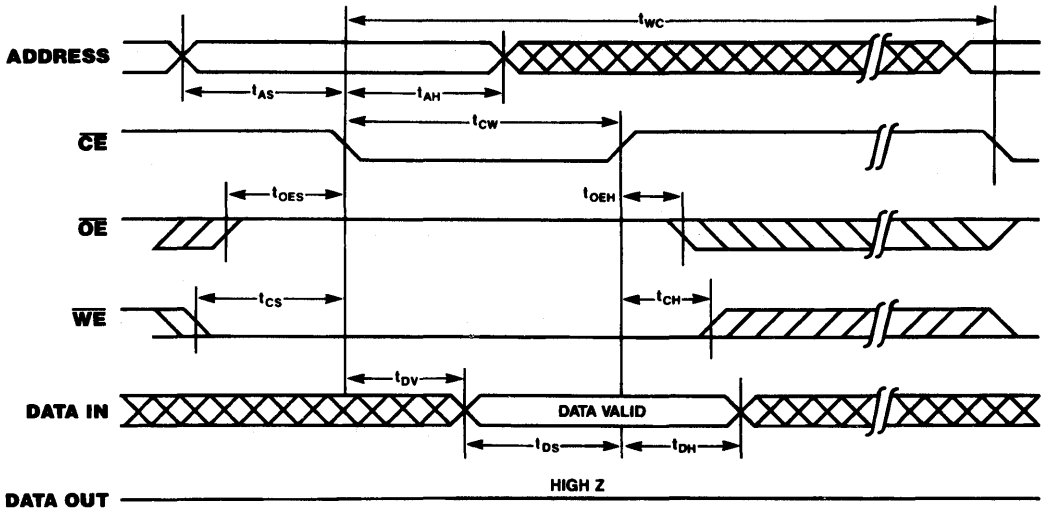
Symbol	Parameter	Min.	Max.	Units
t_{WC}(5)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	200		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	150		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		ns
t_{WPH}	$\overline{WE}$ High Recovery	50		ns
t_{DV}	Data Valid		300	ns
t_{DS}	Data Setup	100		ns
t_{DH}	Data Hold	20		ns
t_{DW}	Delay to Next Write	500		μs
t_{BLC}	Byte Load Cycle	3	40	μs

$\overline{WE}$ Controlled Write Cycle

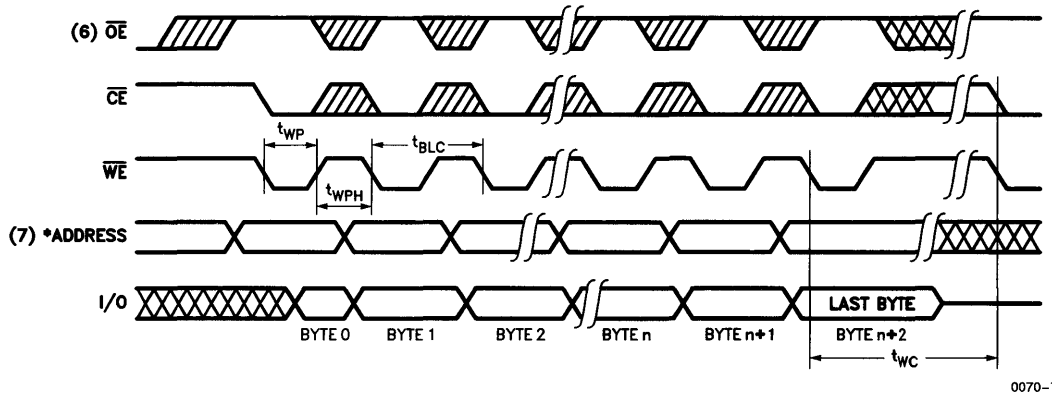


Note: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

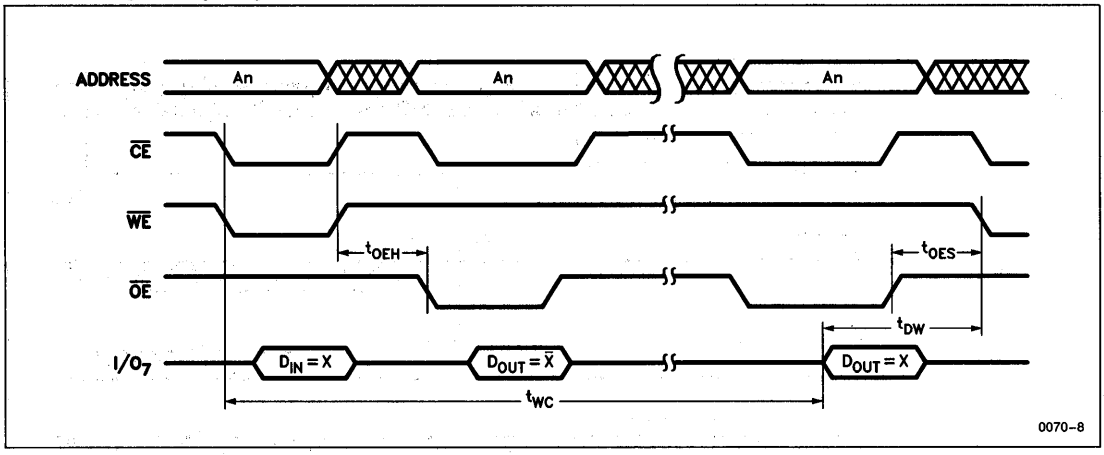


*For each successive write within the page write operation, A_4–A_{12} should be the same or writes to an unknown address could occur.

Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(8)



Note: (8) A polling operation by definition is a read cycle and therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X2864A through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X2864A.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864A supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X2864A allows the entire memory to be written in 2.6 seconds. Page write allows two to sixteen bytes of data to be consecutively written to the X2864A prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_4 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte write cycle must begin within 20 μs of the falling edge of $\overline{WE}$ of the preceding cycle. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20 μs the internal automatic programming cycle will commence.

$\overline{DATA}$ Polling
The X2864A features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864A, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION
There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

Because the X2864A is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

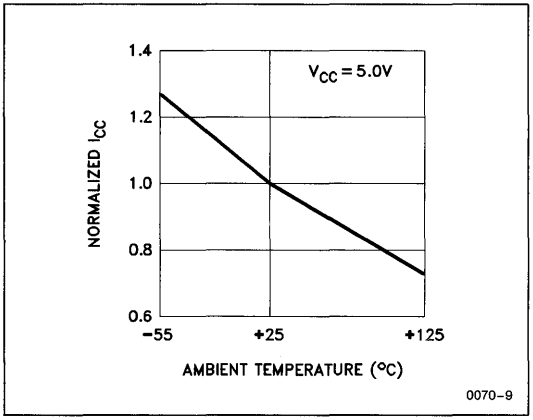
Because the X2864A has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

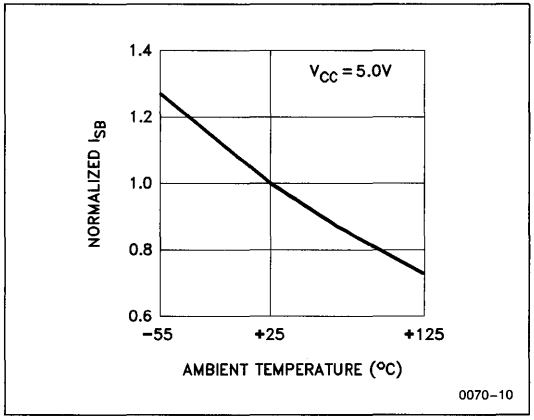
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

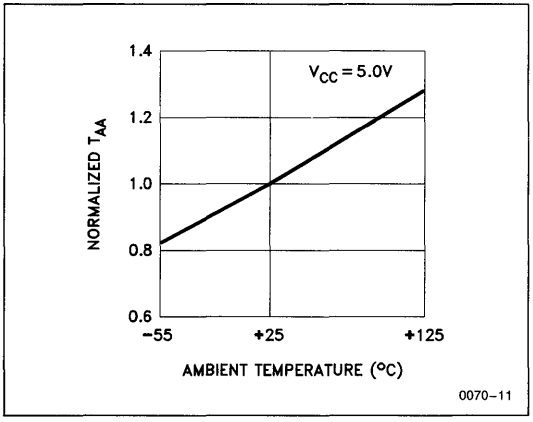
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature



3

NOTES

Electrically Erasable PROM

TYPICAL FEATURES

- 120 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 μs Typical
- $\overline{DATA}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{WE}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout
- High Reliability
  - —Endurance: 10,000 Cycles
  - —Data Retention: 100 Years

DESCRIPTION

The Xicor X2864B is a 8K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

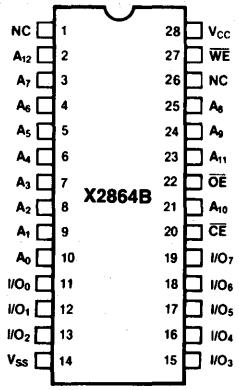
The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features $\overline{DATA}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics for Xicor nonvolatile memories.

3

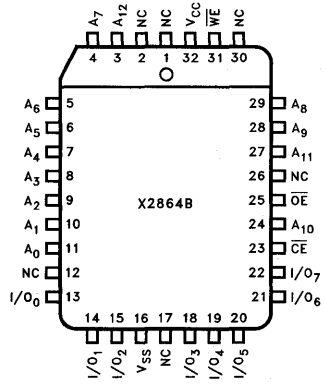
PIN CONFIGURATIONS

PLASTIC CERDIP



0031-1

PLCC



0031-2

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864B ..... −10°C to +85°C
X2864BI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864B T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	140	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	70	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit	Condition
Minimum Endurance	10,000		Cycles/Byte	Reliability Report-520
Data Retention	100		Years	Reliability Report-515

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

A.C. CHARACTERISTICS

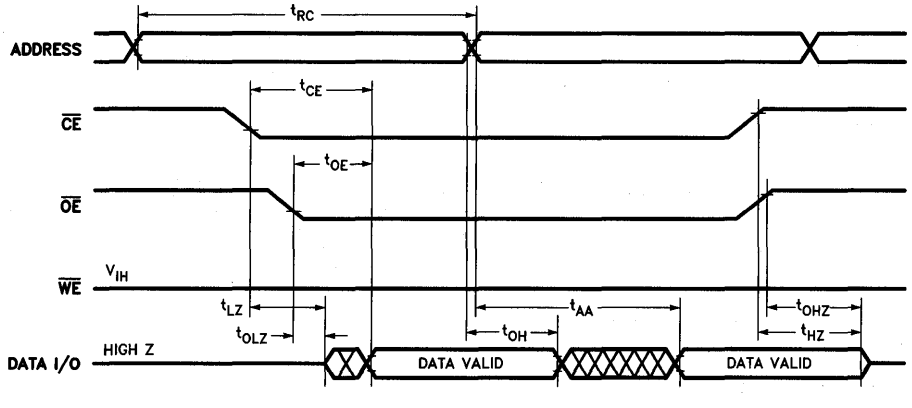
X2864B T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

3

Read Cycle Limits

Symbol	Parameter	X2864B-12 X2864BI-12		X2864B-15 X2864BI-15		X2864B-20 X2864BI-20		X2864B-25 X2864BI-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		70		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



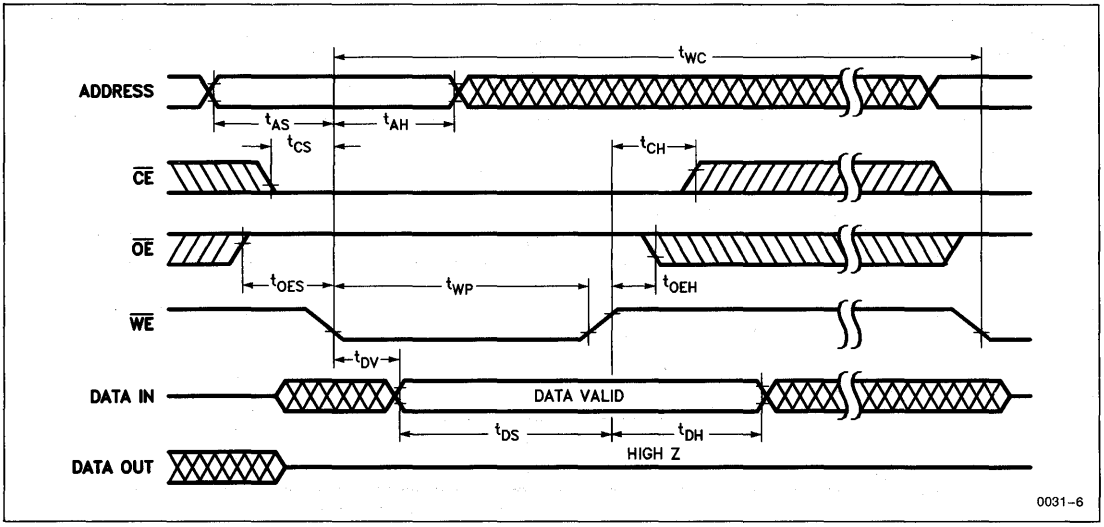
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	5			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			100	μs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	5			ns
t_{DW}	Delay to Next Write	10			μs
t_{BLC}	Byte Load Cycle	1		100	μs

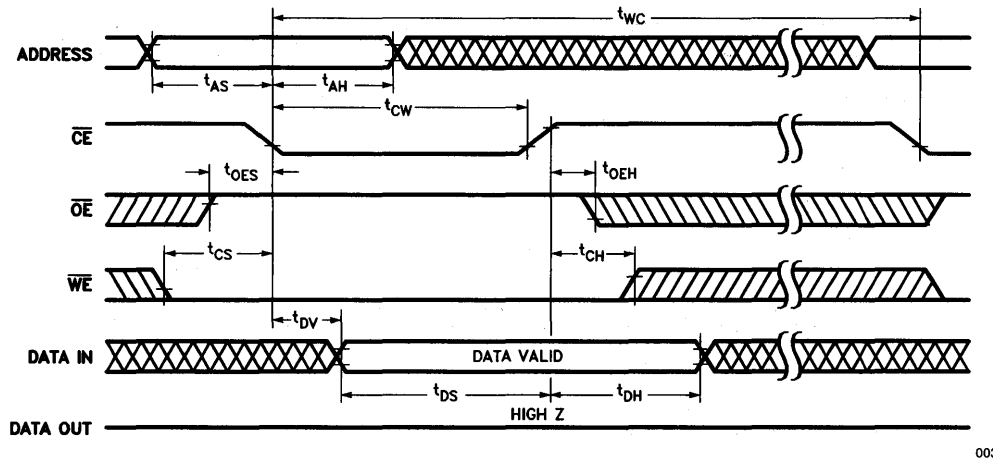
$\overline{WE}$ Controlled Write Cycle



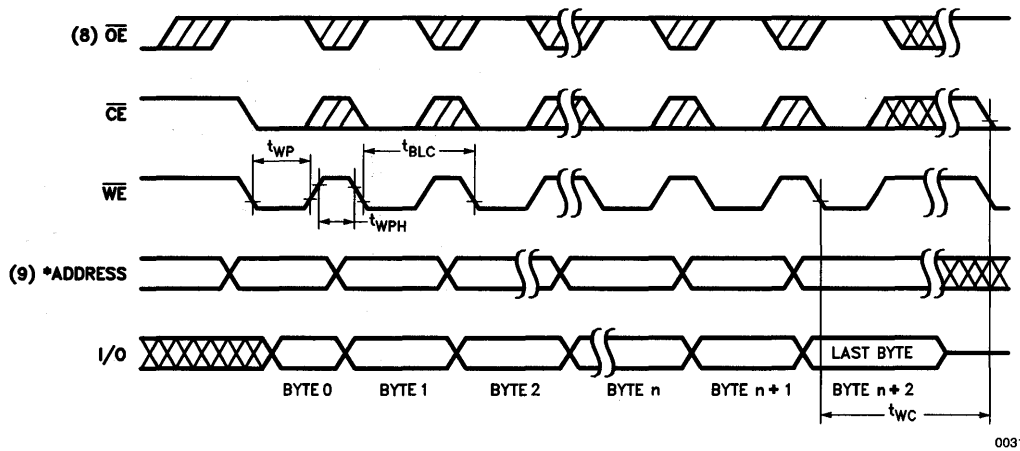
Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.

(7) t_{WC} is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

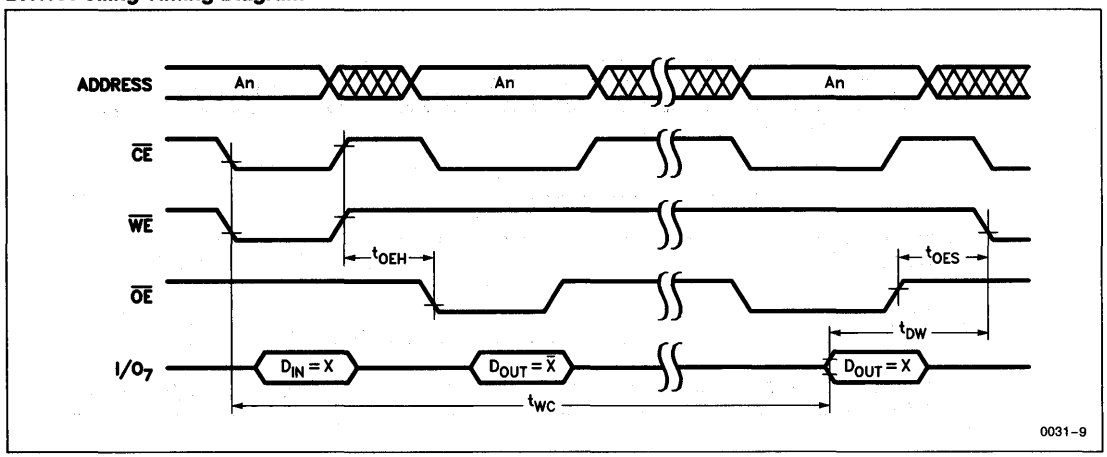


*For each successive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (8) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(10)



Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PIN DESCRIPTIONS

Addresses (A_0–A_{12})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X2864B through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X2864B.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864B supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation
The page write feature of the X2864B allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864B prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide so long as the host continues to access the device within the byte load cycle time of 100 μs.

$\overline{DATA}$ Polling
The X2864B features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION
There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3.5V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

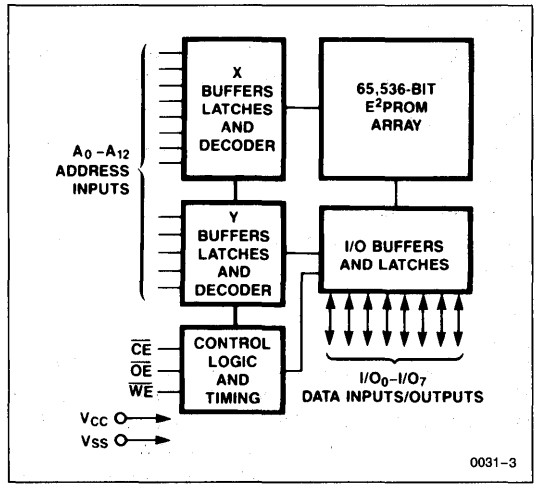
Because the X2864B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



Electrically Erasable PROM

TYPICAL FEATURES

- 70 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 μs Typical
- $\overline{DATA}$ Polling
  - —Allows User to Minimize Write Cycle Time
- High Reliability
  - —Endurance: 10,000 Writes Per Byte
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Level $\overline{WE}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

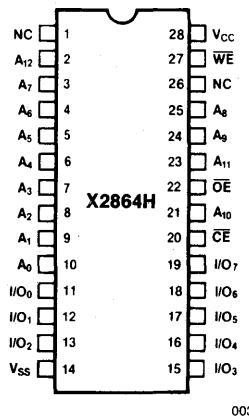
The Xicor X2864H is a high speed 8K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, and EPROMs.

The X2864H supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features $\overline{DATA}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

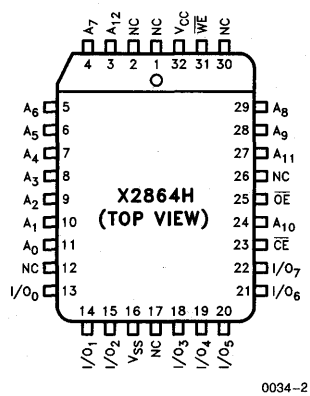
PIN CONFIGURATIONS

PLASTIC CERDIP



0034-1

PLCC



0034-2

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864H ..... −10°C to +85°C
X2864HI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864H T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864HI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	150	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	80	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L = 30 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

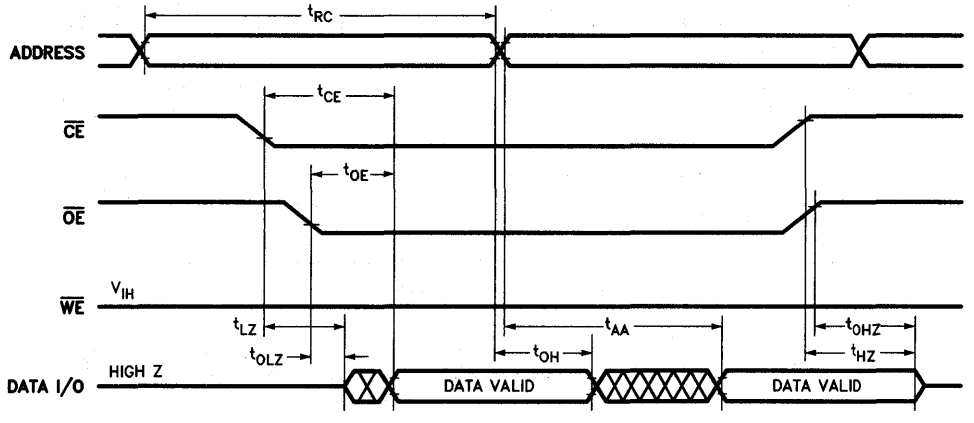
A.C. CHARACTERISTICS

X2864H T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864HI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864H-70 X2864HI-70		X2864H-90 X2864HI-90		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70		90		ns
t_{CE}	Chip Enable Access Time		70		90	ns
t_{AA}	Address Access Time		70		90	ns
t_{OE}	Output Enable Access Time		35		45	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	40	0	40	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	40	0	40	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Read Cycle



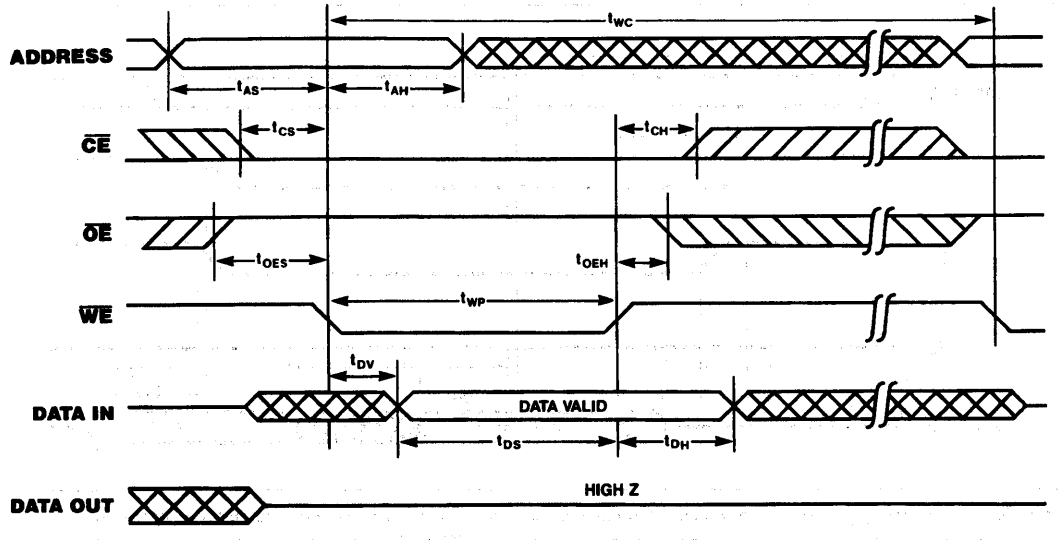
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

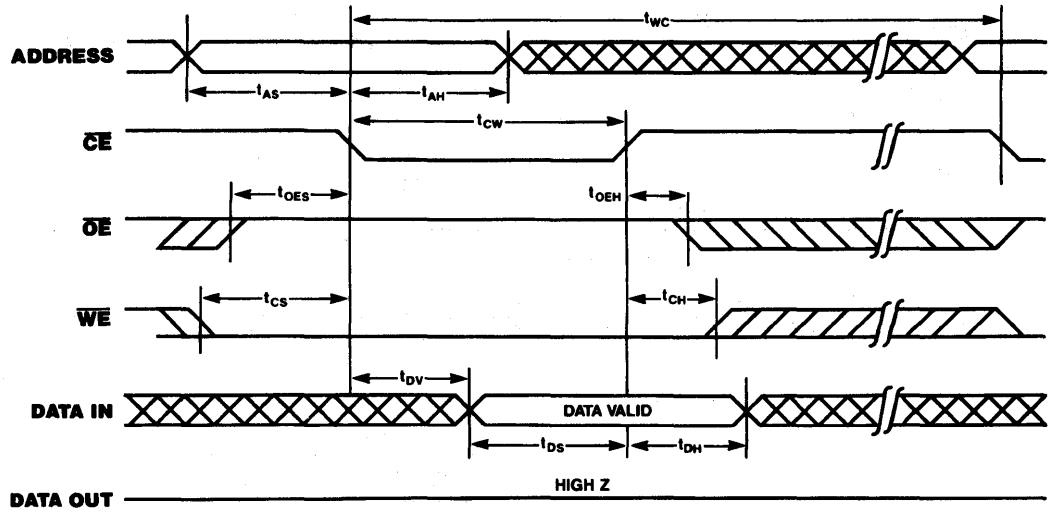
Write Cycle Limits

Symbol	Parameter	X2864H-70 X2864HI-70		X2864H-90 X2864HI-90		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5	ms
t_{AS}	Address Setup Time	5		5		ns
t_{AH}	Address Hold Time	50		50		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width	60		80		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	5		5		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		80		ns
t_{WPH}	$\overline{WE}$ High Recovery	50		50		ns
t_{DV}	Data Valid		100		100	µs
t_{DS}	Data Setup	35		35		ns
t_{DH}	Data Hold	5		5		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

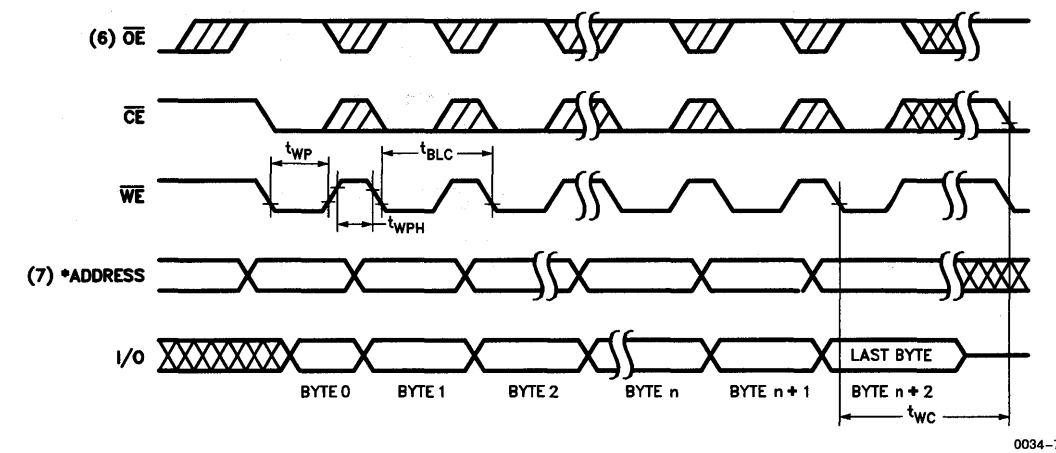
$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

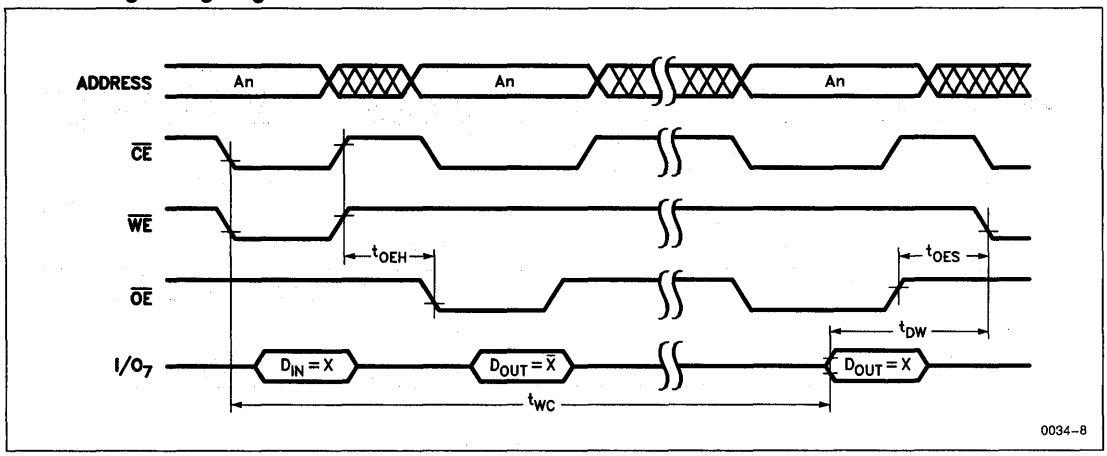


*For each successive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(8)



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (8) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X2864H through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X2864H.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864H supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation
The page write feature of the X2864H allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864H prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the 100 μs byte load cycle time.

$\overline{DATA}$ Polling
The X2864H features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864H, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION
There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$4.0V.
- Write Inhibit—Holding $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

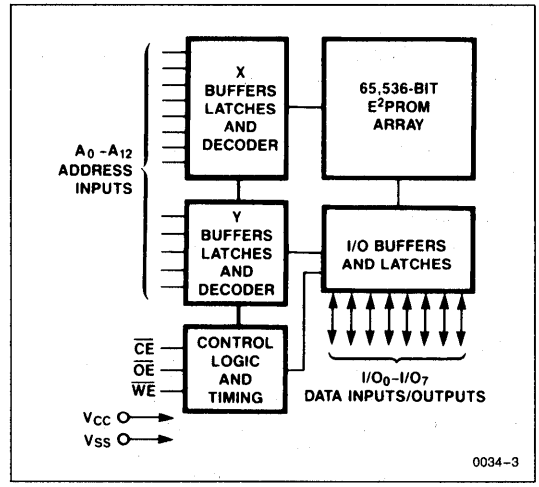
Because the X2864H is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864H has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



Electrically Erasable PROM

FEATURES

- 120 ns Access Time
- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 0.625 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- High Reliability
  - —Endurance: 10,000 Cycles
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

The Xicor X28C64 is a 8K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

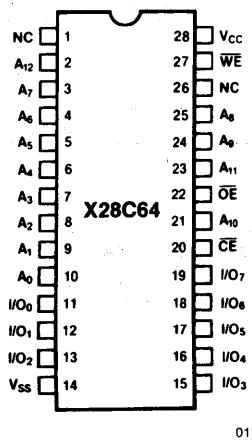
The X28C64 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics for Xicor nonvolatile memories.

3

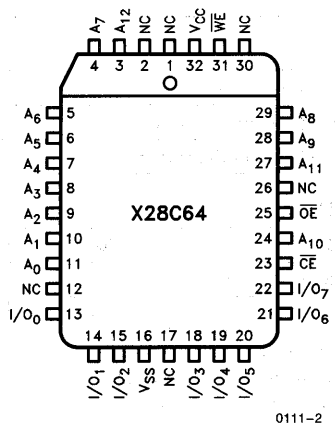
PIN CONFIGURATIONS

PLASTIC CERDIP



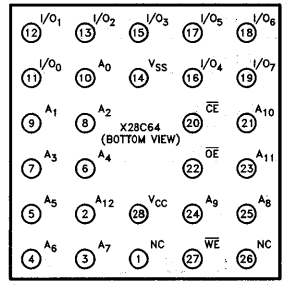
0111-1

PLCC



0111-2

PGA



0111-3

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X28C64 ..... −10°C to +85°C
X28C64I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C64 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C64I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	µA	$\overline{CE}$ = $\overline{WE}$ = V_{CC} − 0.3V All I/O's = Open, Other Inputs = Don't Care
I_{LI}	Input Leakage Current			±10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			±10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit	Condition
Minimum Endurance	10,000		Cycles/Byte	Reliability Report-520
Data Retention	100		Years	Reliability Report-515

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	100	µs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

A.C. CHARACTERISTICS

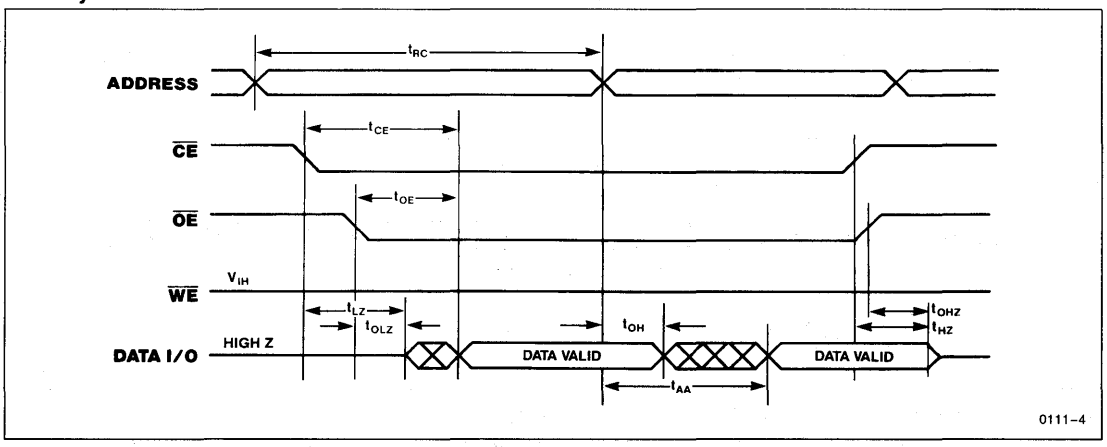
X28C64 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C64I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

3

Read Cycle Limits

Symbol	Parameter	X28C64-12 X28C64I-12		X28C64-15 X28C64I-15		X28C64-20 X28C64I-20		X28C64-25 X28C64I-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		70		80		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



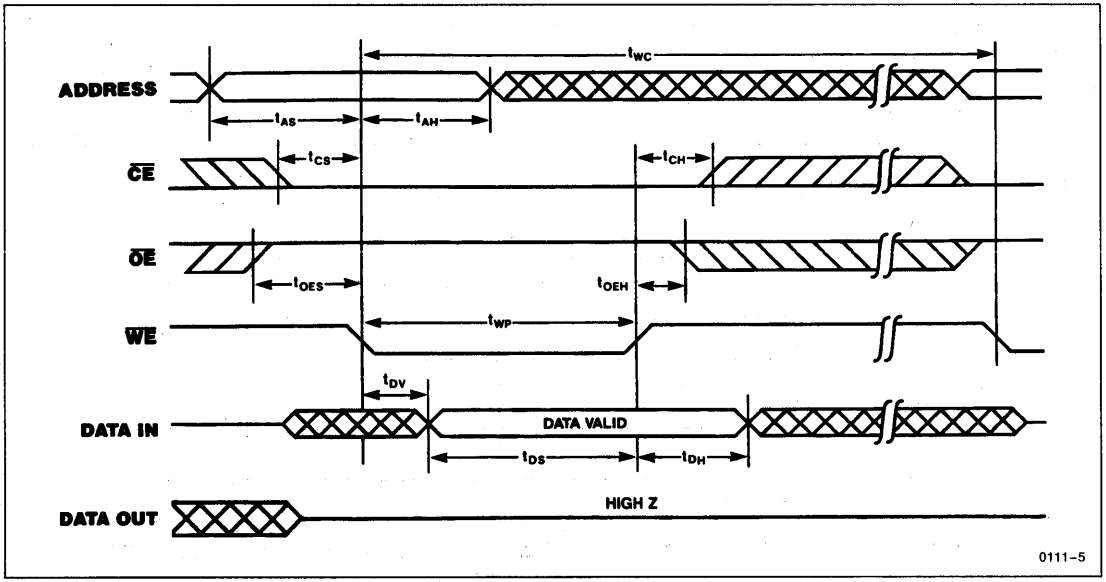
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	100			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{WPH2}(8)	SDP $\overline{WE}$ Recovery	1			µs
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle

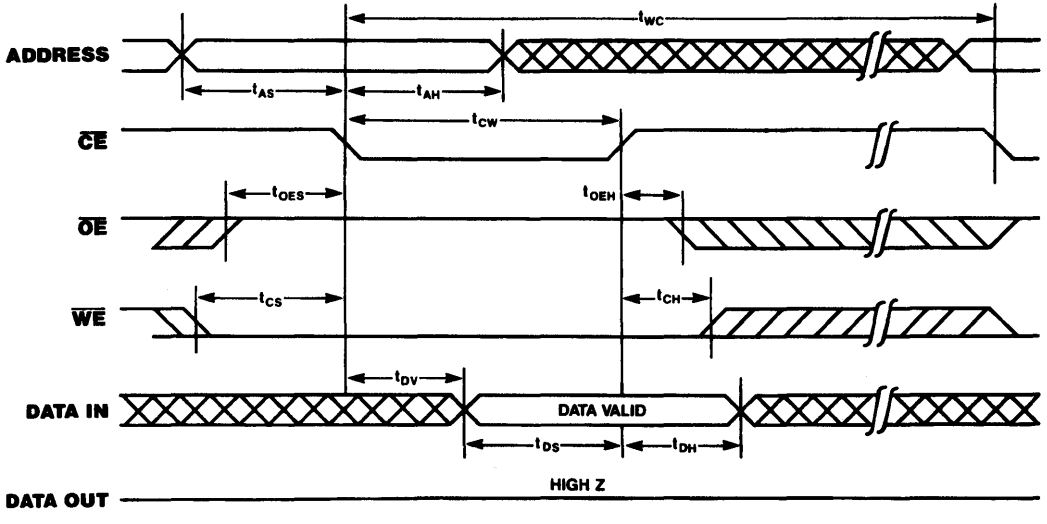


Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.

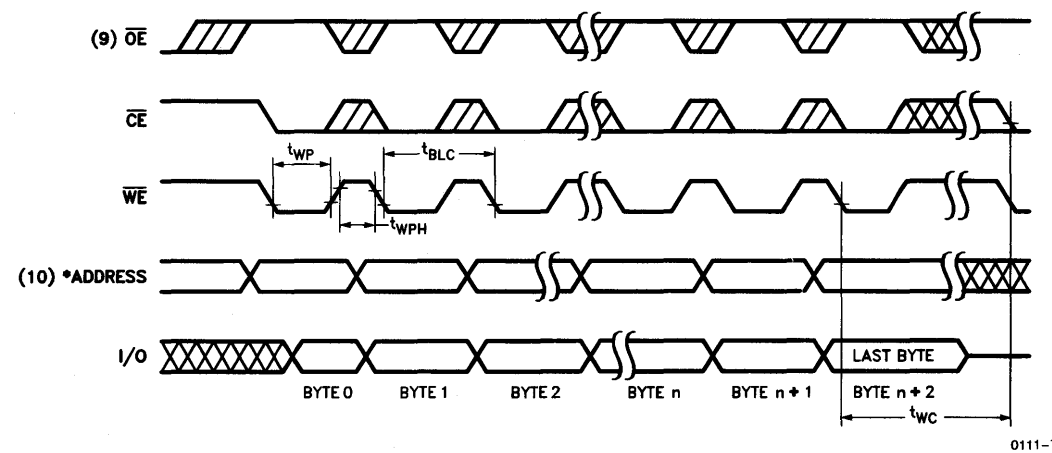
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

(8) t_{WPH} is the normal page write operation $\overline{WE}$ recovery time. t_{WPH2} is the $\overline{WE}$ recovery time needed only after the end of issuing the three byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 4a which illustrates the t_{WPH2} requirement.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

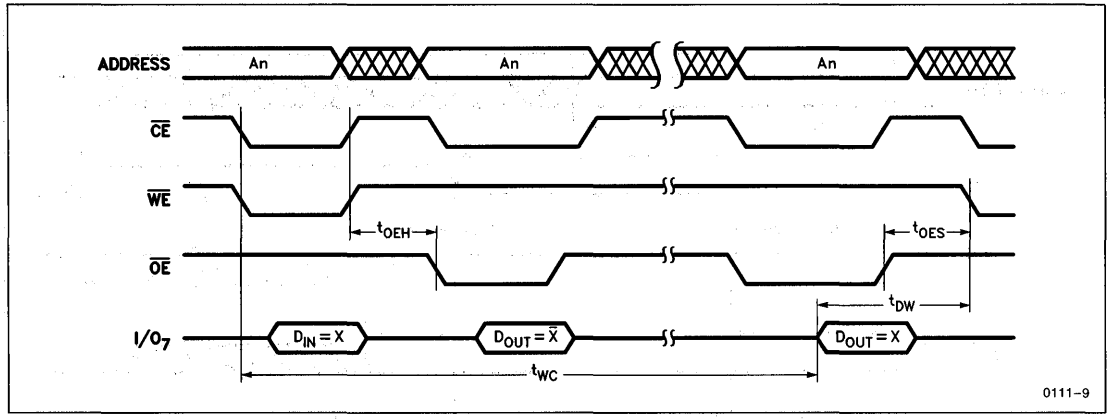


*For each successive write within the page write operation, A_6–A_{12} should be the same or writes to an unknown address could occur.

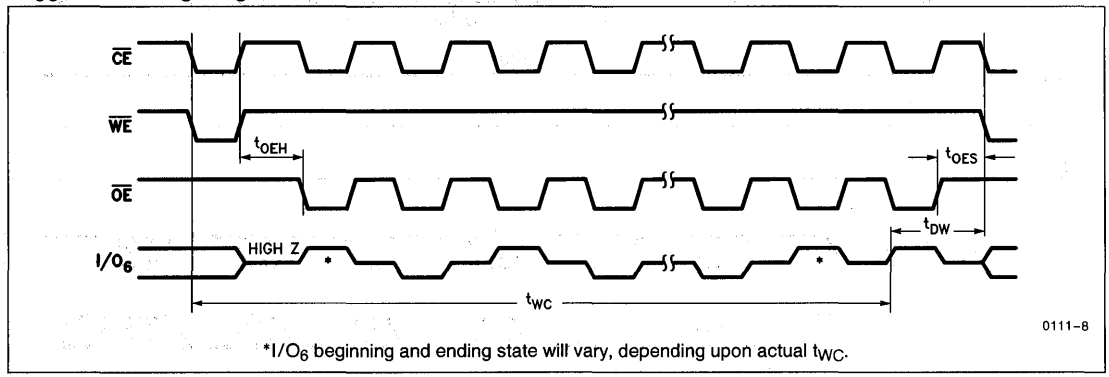
Notes: (9) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(10) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(11)



Toggle Bit Timing Diagram(11)



*I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (11) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X28C64 through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X28C64.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

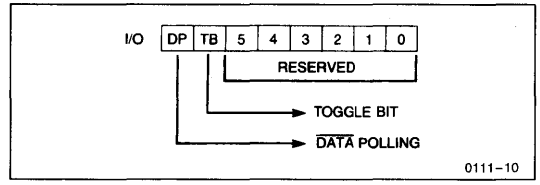
Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)
The X28C64 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)
The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

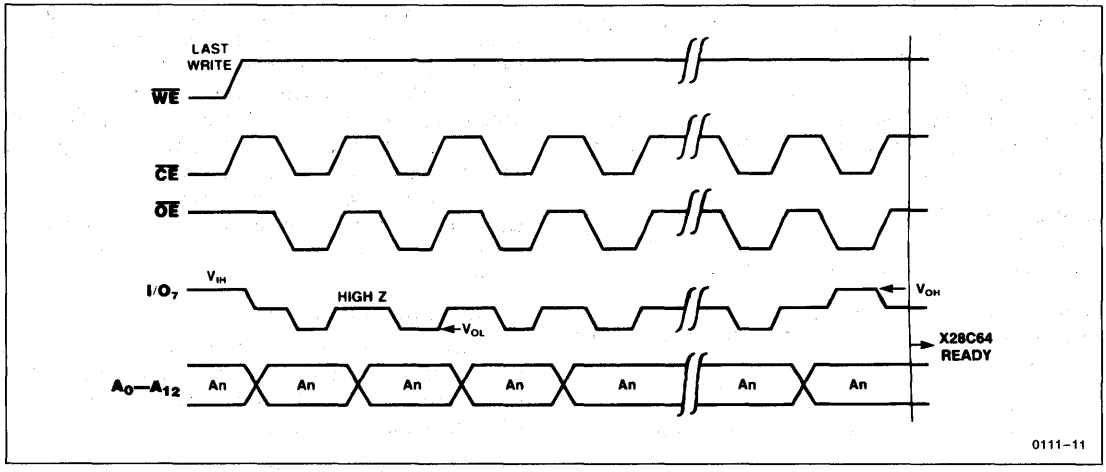
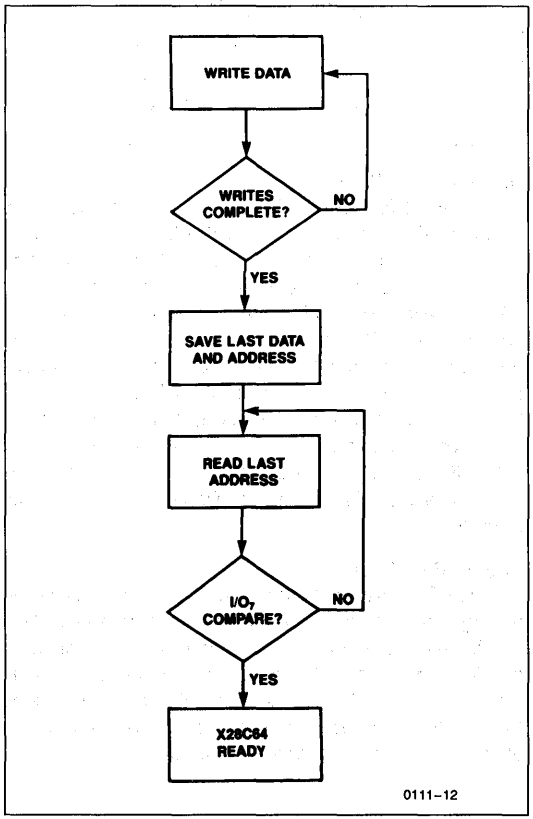


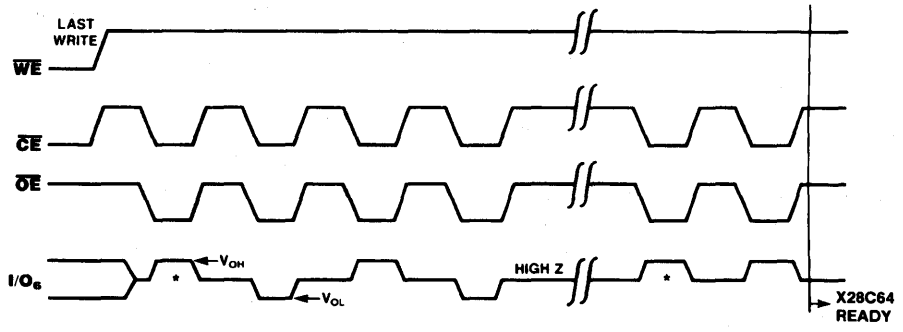
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

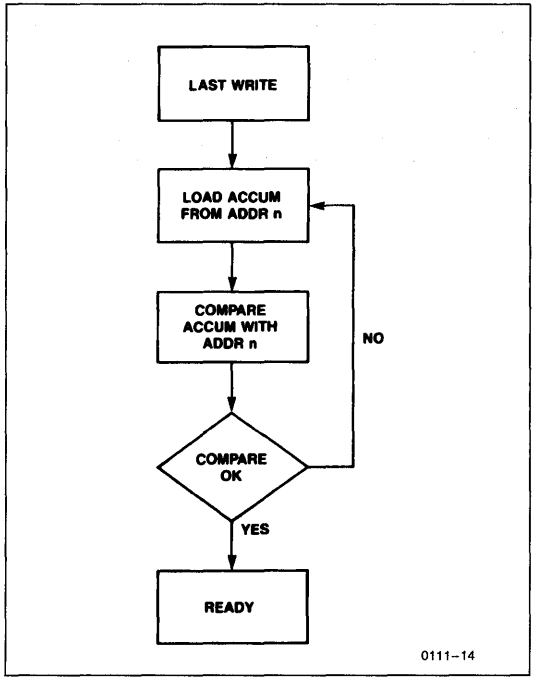
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.(12) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (12) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

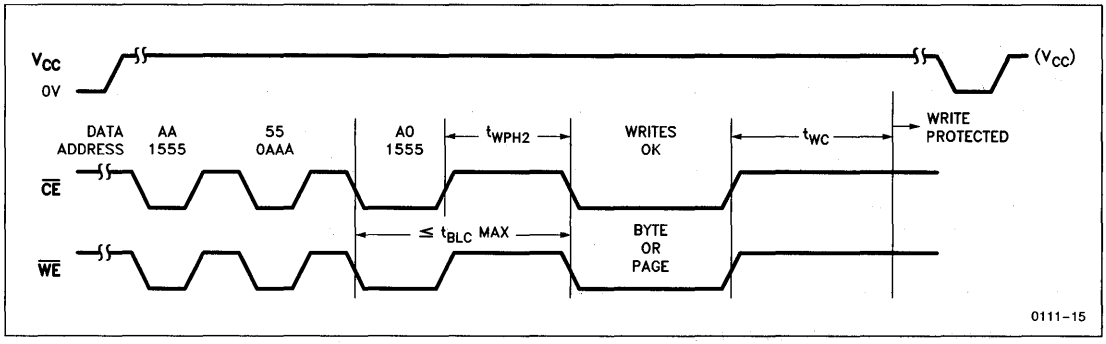
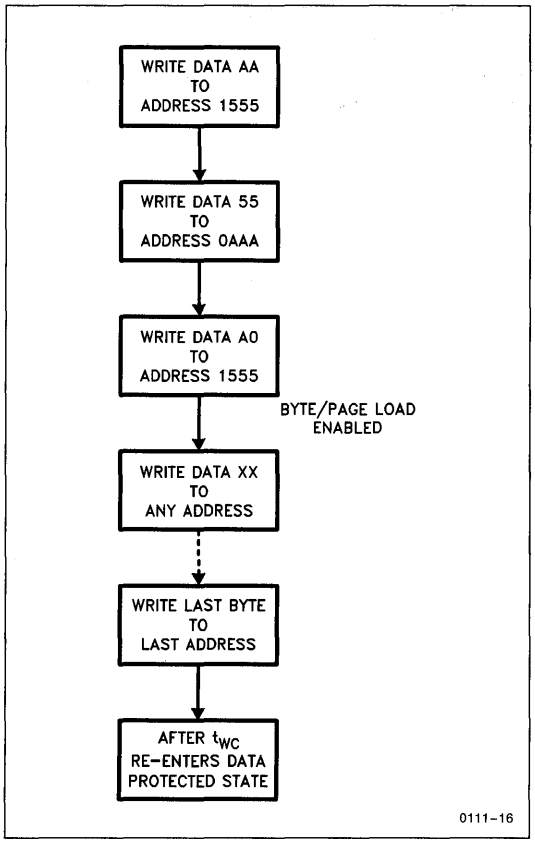


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

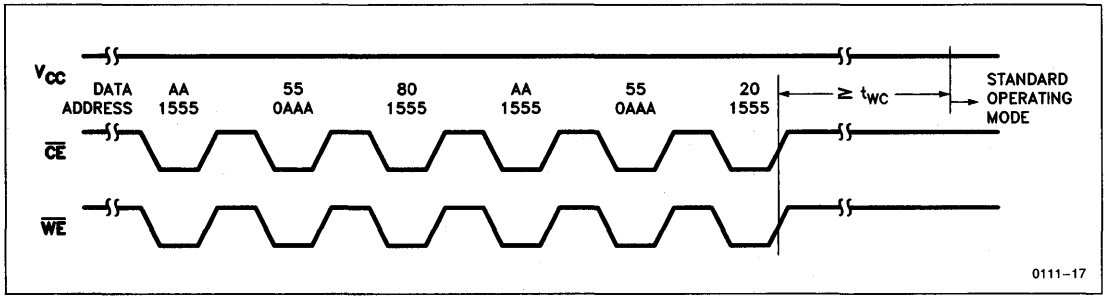
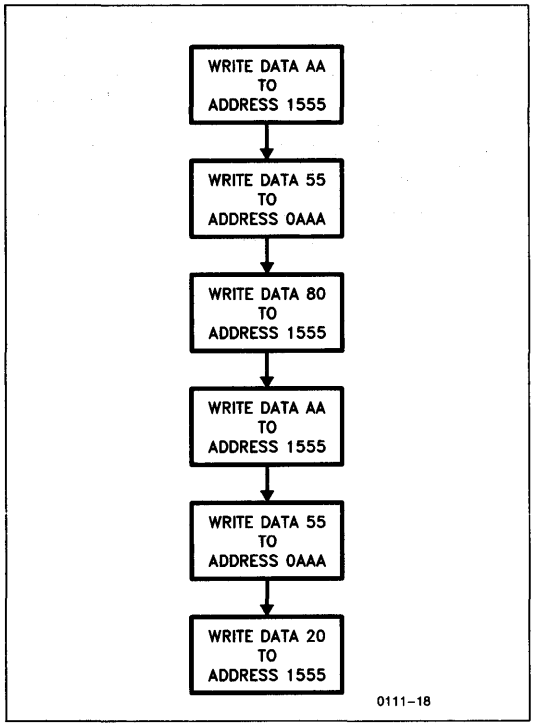


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

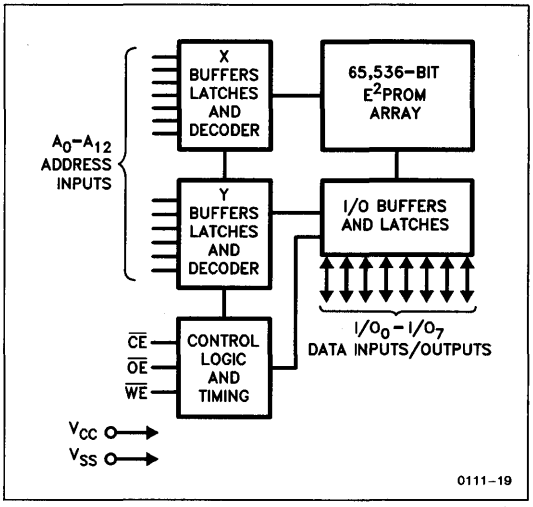
Because the X28C64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



3

NOTES

Electrically Erasable PROM

FEATURES

- 250 ns Access Time
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- High Reliability
  - —Endurance: 10,000 Writes Per Byte
  - —Data Retention: 100 Years
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

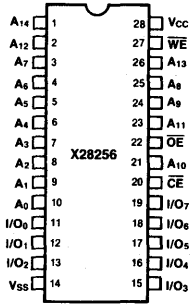
DESCRIPTION

The Xicor X28256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories the X28256 is a 5V only device. The X28256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

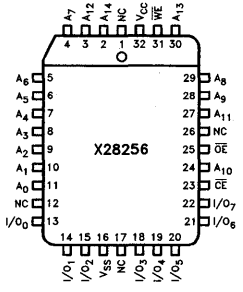
The X28256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 10,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS



0029-1

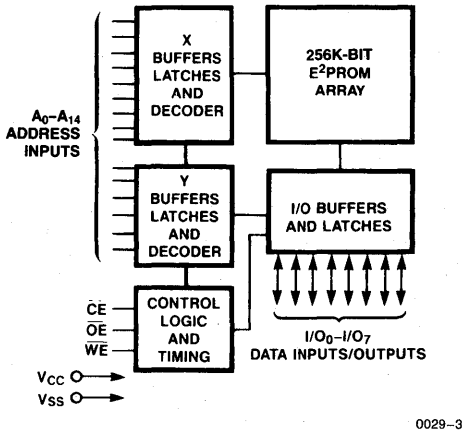


0029-2

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0029-3

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X28256 ..... −10°C to +85°C
X28256I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28256 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X28256I T_A = −40°C to +85°C, V_{CC} = +5V ±5%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		60	120	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		35	60	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(3)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(3)	Input High Voltage	2.0		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	100	μs
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	10,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

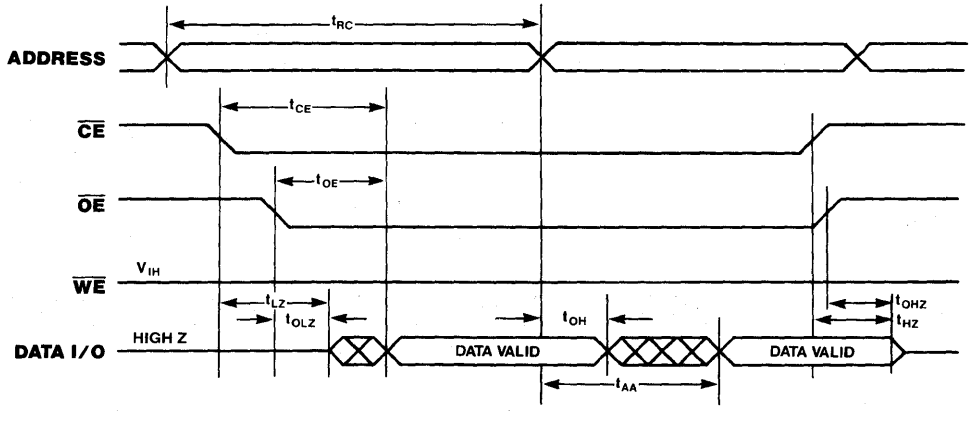
A.C. CHARACTERISTICS

X28256 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X28256I T_A = −40°C to +85°C, V_{CC} = +5V ±5%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28256-25 X28256I-25		X28256 X28256I		X28256-35 X28256I-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		ns
t_{CE}	Chip Enable Access Time		250		300		350	ns
t_{AA}	Address Access Time		250		300		350	ns
t_{OE}	Output Enable Access Time		100		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output	0	80	0	80	0	80	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output	0	80	0	80	0	80	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Read Cycle

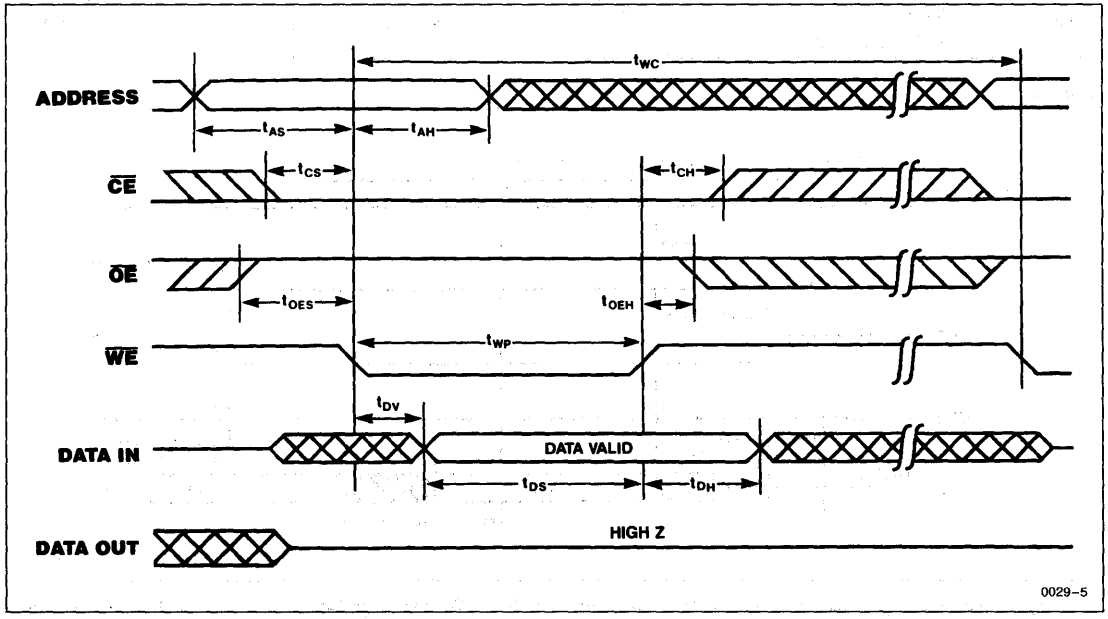


Note: (4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min., t_{OHZ} min., t_{LZ} min. and t_{OLZ} min. are periodically sampled and are not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WC}(6)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	150			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	150			ns
t_{WPH}	$\overline{WE}$ High Recovery	1			µs
t_{DV}	Data Valid			300	ns
t_{DS}	Data Setup	100			ns
t_{DH}	Data Hold	15			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	2		100	µs

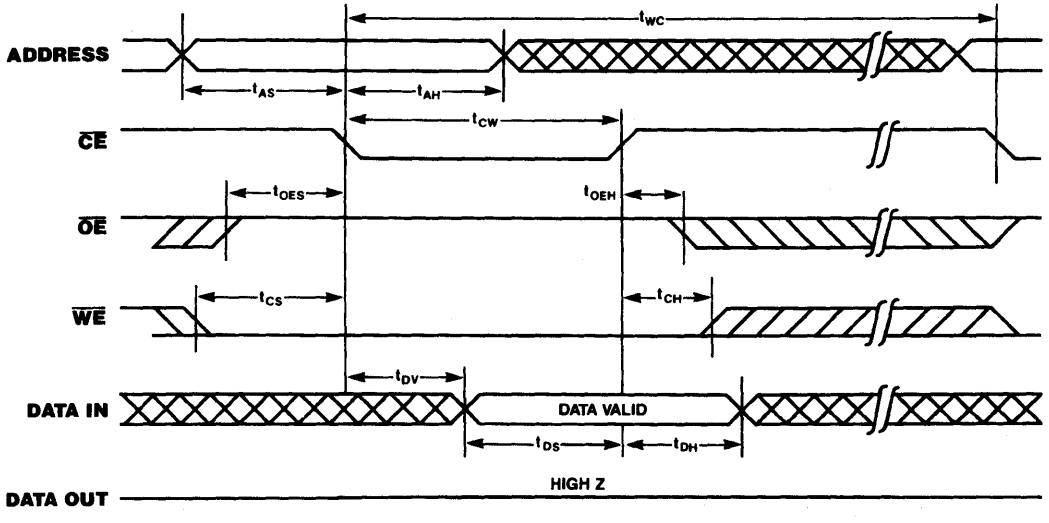
$\overline{WE}$ Controlled Write Cycle



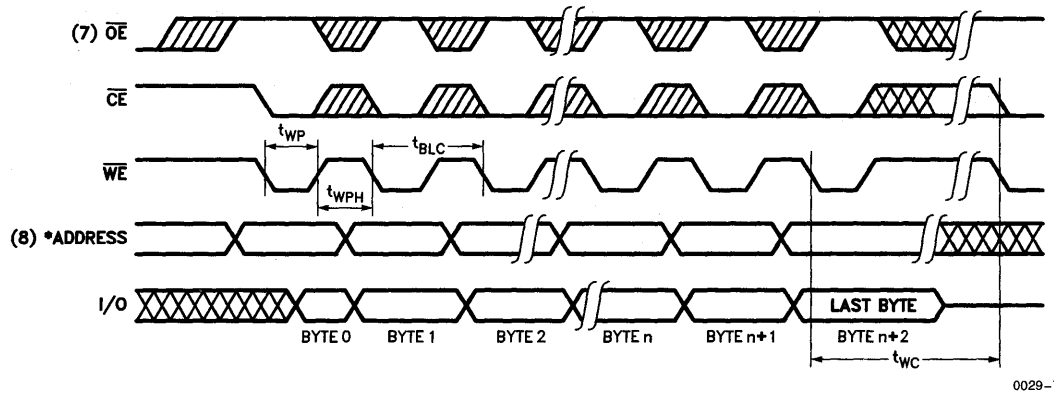
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage.

(6) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

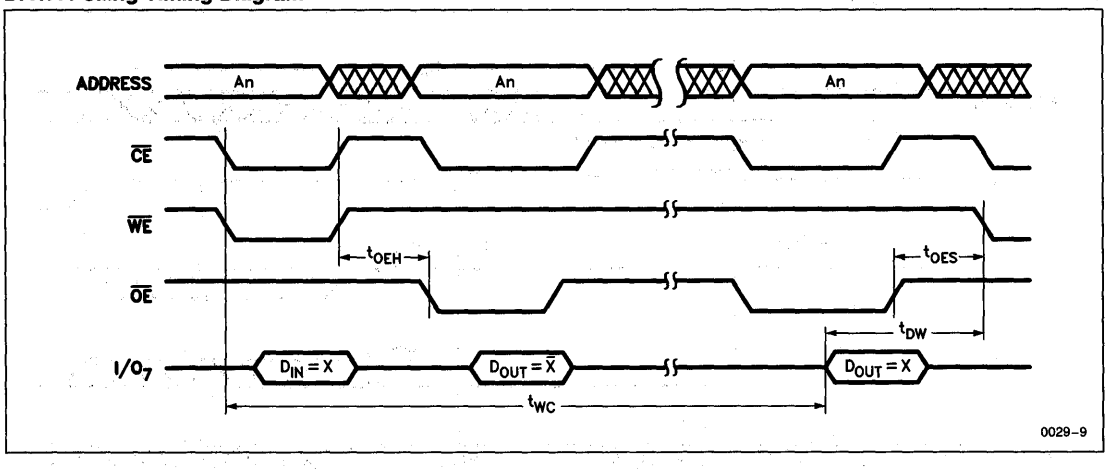


*For each successive write within the page write operation, A_6–A_{14} should be the same or writes to an unknown address could occur.

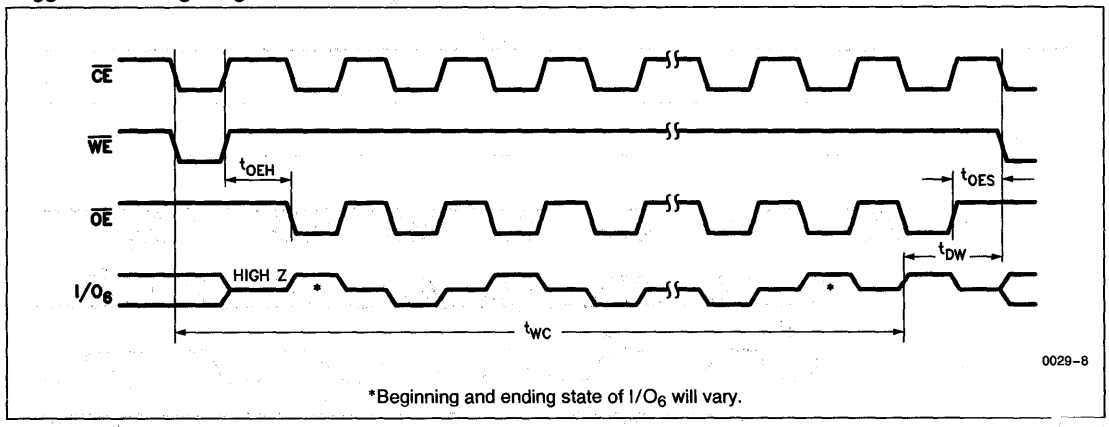
Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



Toggle Bit Timing Diagram(9)



*Beginning and ending state of I/O_6 will vary.

Note: (9) Polling operations by definition are read cycles and therefore are subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{14})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X28256 through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X28256.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

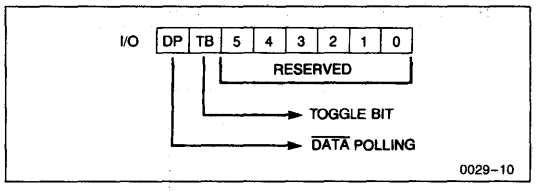
Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)
The X28256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28256 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)
The X28256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

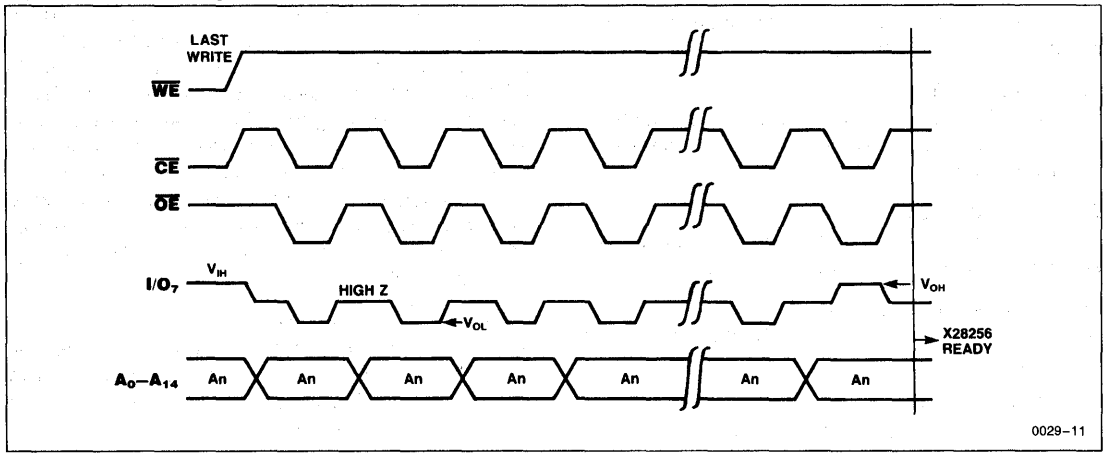
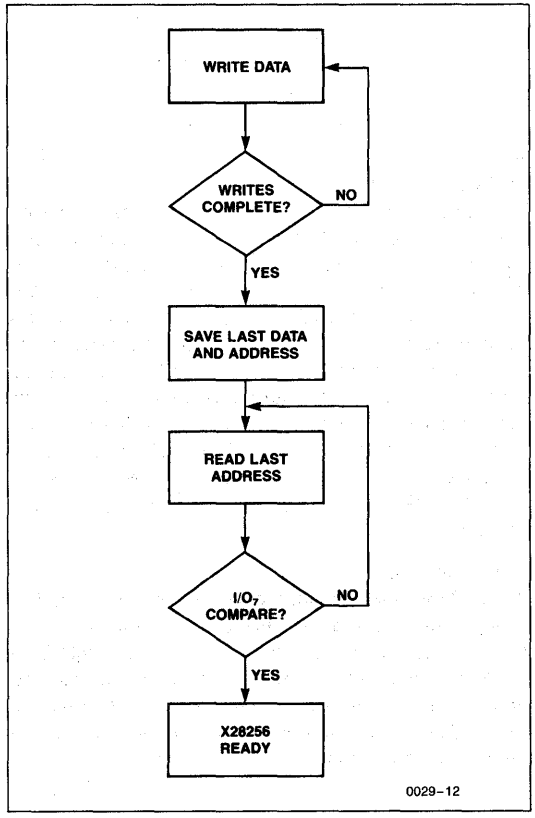


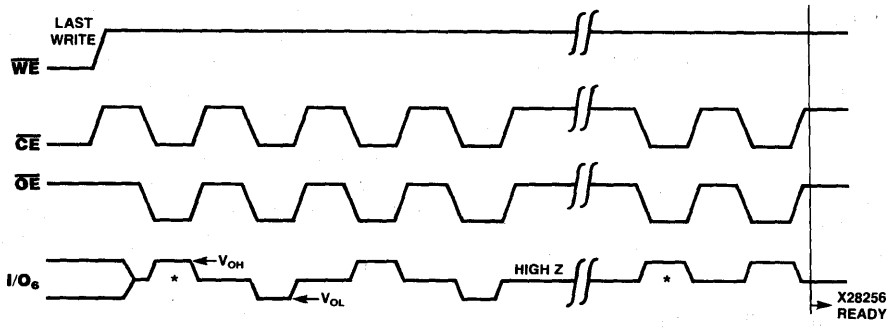
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

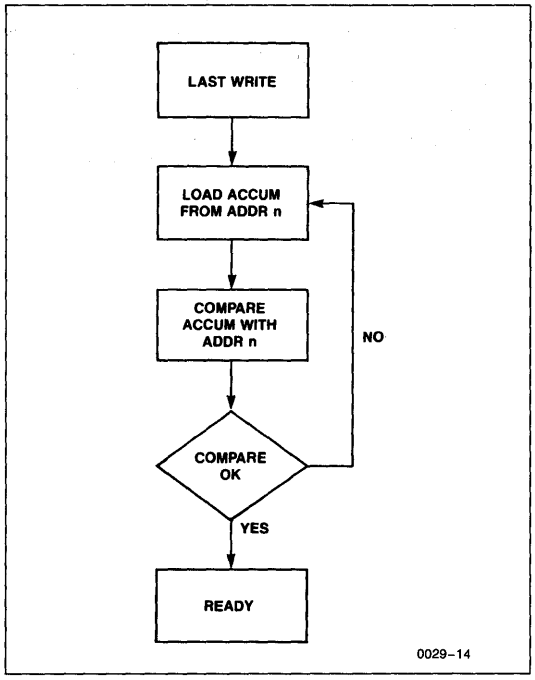
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28256 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28256 offers a software controlled data protection feature. The X28256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.(10) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (10) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

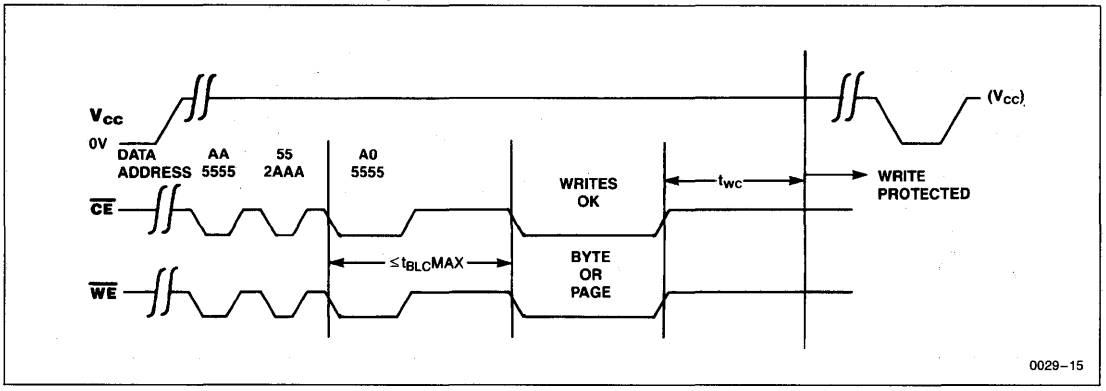
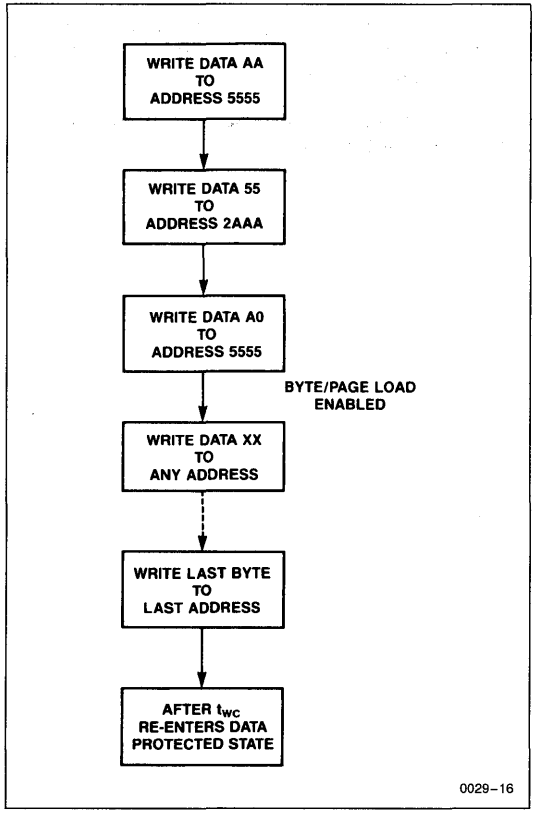


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

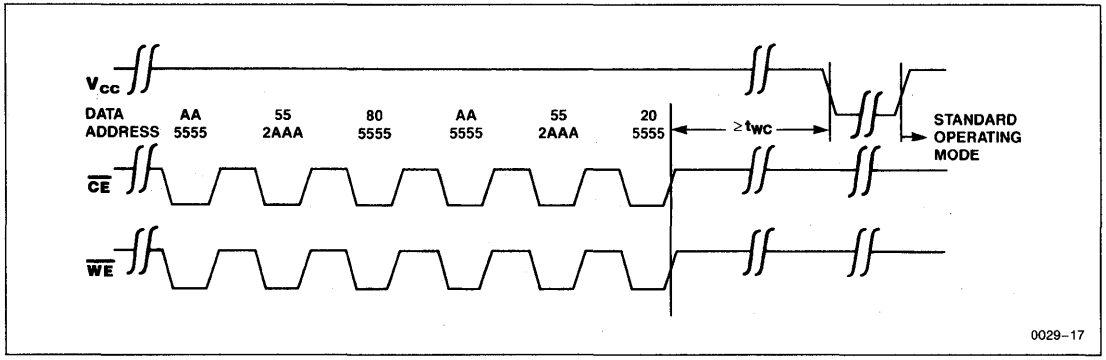
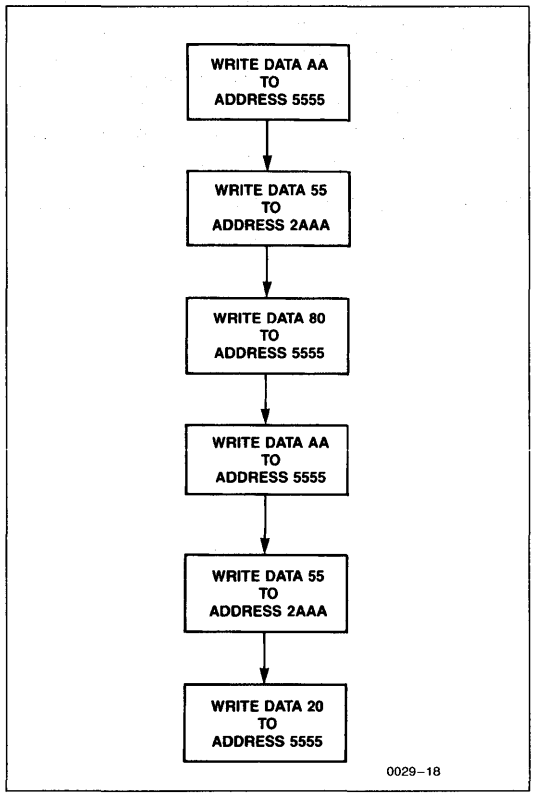


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. The next time the X28256 is powered-up the device will be in the standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the X28256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

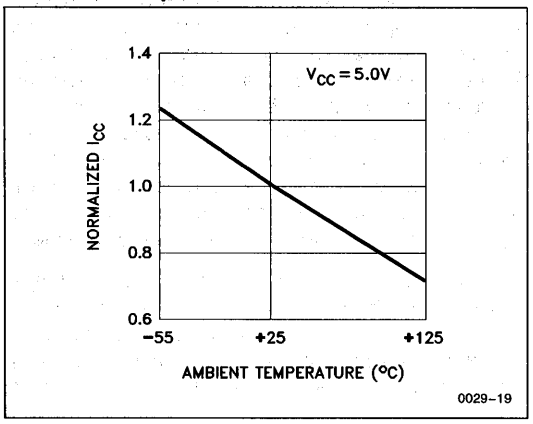
In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

3

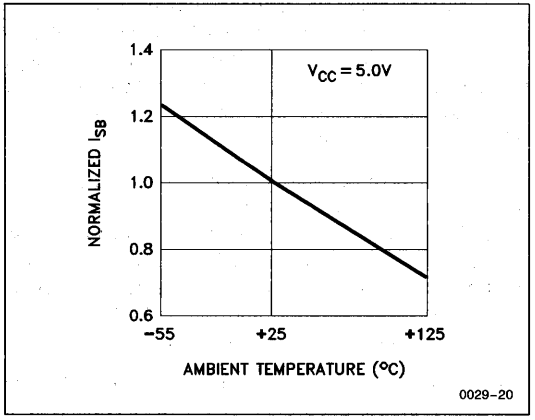
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



Electrically Erasable PROM

FEATURES

- 150 ns Access Time
- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- High Reliability
  - —Endurance: 10,000 Cycles
  - —Data Retention: 100 Years
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

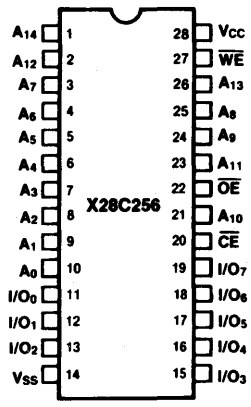
The Xicor X28C256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Refer to RR-515 for details of data retention characteristics for Xicor nonvolatile memories.

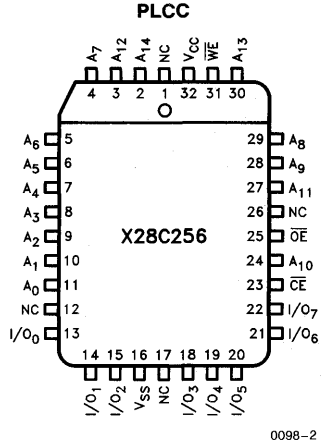
PIN CONFIGURATIONS

PLASTIC CERDIP

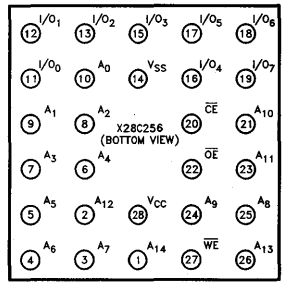


0098-1

PLCC



0098-2



0098-21

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X28C256 ..... −10°C to +85°C
X28C256I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C256 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C256I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	µA	$\overline{CE}$ = V_{CC} − 0.3V, $\overline{OE}$ = GND All I/O's = Open, Other Inputs = V_{CC} − 0.3V
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit	Condition
Minimum Endurance	10,000		Cycles/Byte	Reliability Report-520
Data Retention	100		Years	Reliability Report-515

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read Operation	100	µs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

A.C. CHARACTERISTICS

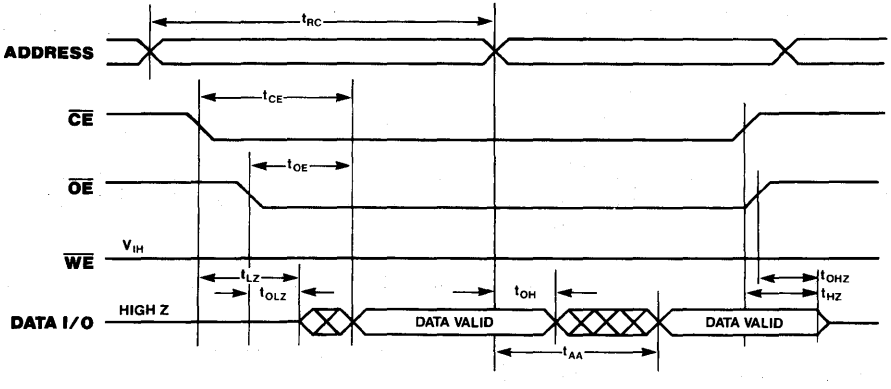
X28C256 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C256I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

3

Read Cycle Limits

Symbol	Parameter	X28C256-15 X28C256I-15		X28C256-20 X28C256I-20		X28C256-25 X28C256I-25		X28C256 X28C256I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		300		ns
t_{CE}	Chip Enable Access Time		150		200		250		300	ns
t_{AA}	Address Access Time		150		200		250		300	ns
t_{OE}	Output Enable Access Time		50		80		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



0098-4

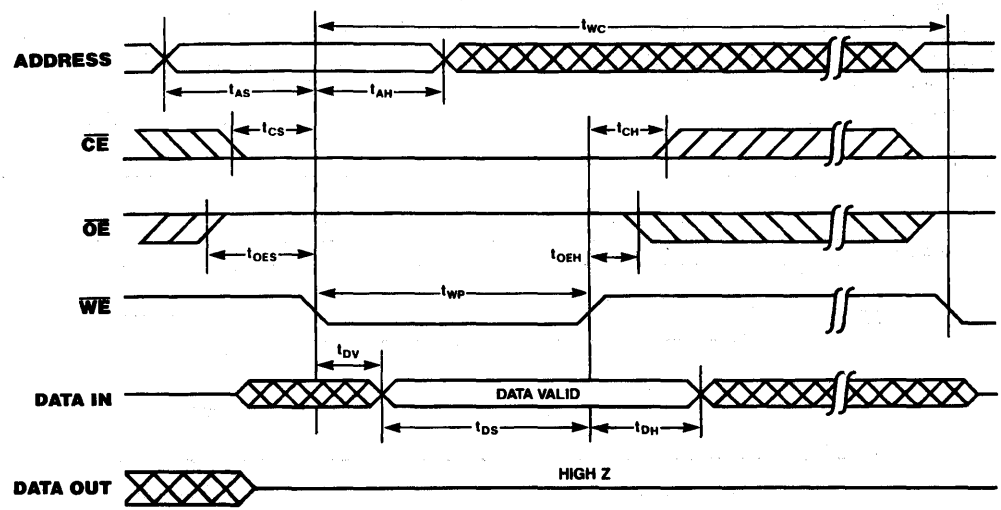
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}(7)	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{WPH2}(8)	SDP $\overline{WE}$ Recovery	1			µs
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle

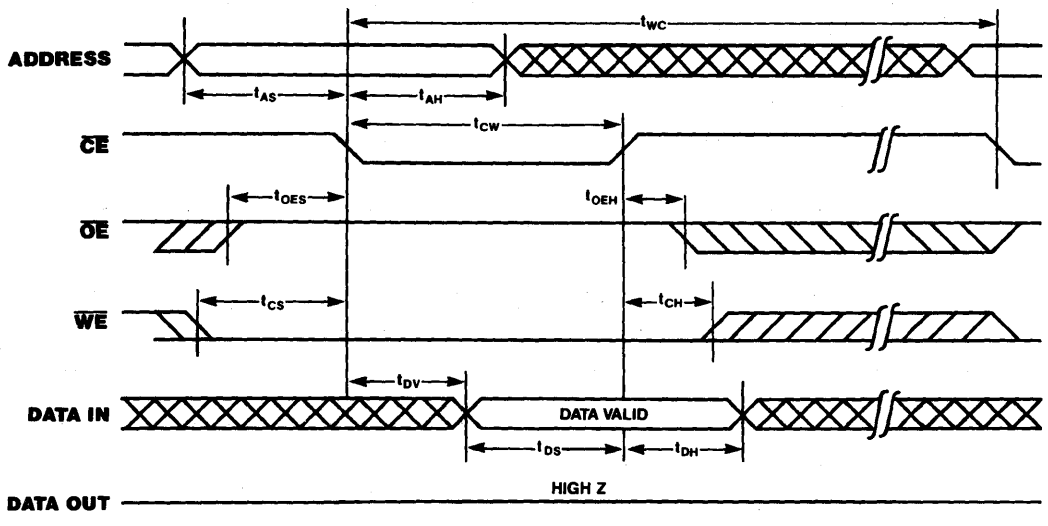


Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.

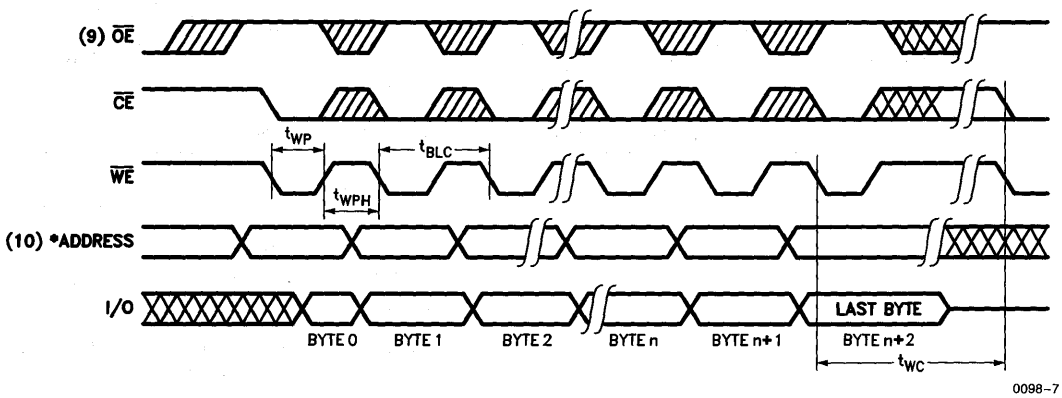
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

(8) t_{WPH} is the normal page write operation $\overline{WE}$ recovery time. t_{WPH2} is the $\overline{WE}$ recovery time needed only after the end of issuing the three byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 4a which illustrates the t_{WPH2} requirement.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

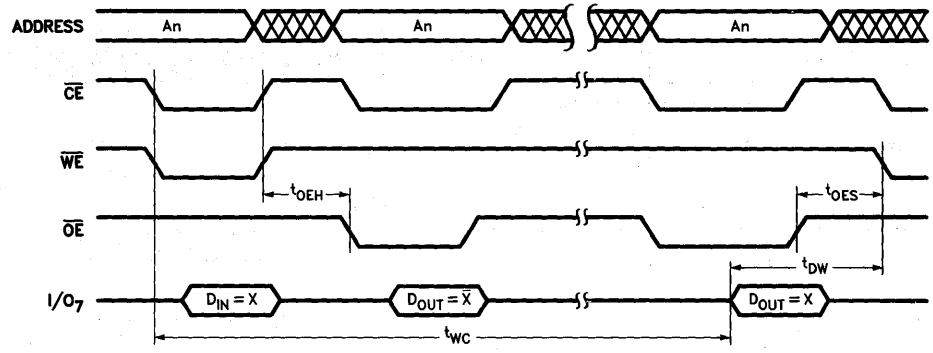


*For each successive write within the page write operation, A_6–A_{14} should be the same or writes to an unknown address could occur.

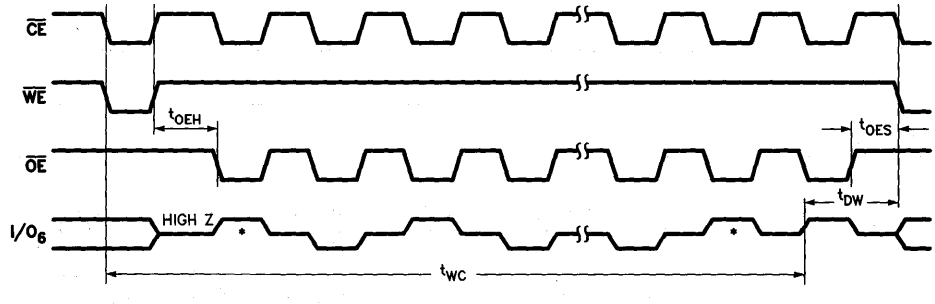
Notes: (9) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(10) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(11)



Toggle Bit Timing Diagram



*I/O6 beginning and ending state will vary, depending upon actual tWC.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (11) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{14})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X28C256 through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X28C256.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

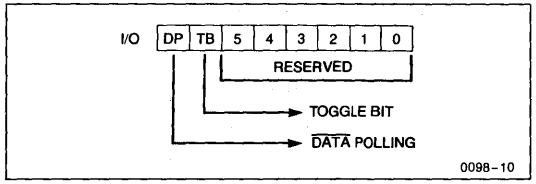
Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)
The X28C256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)
The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2a: $\overline{DATA}$ Polling Bus Sequence

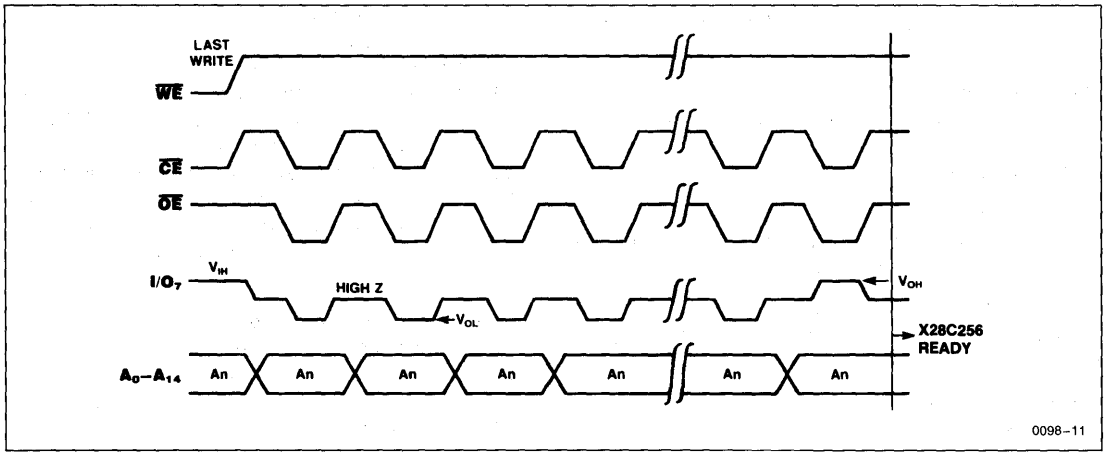
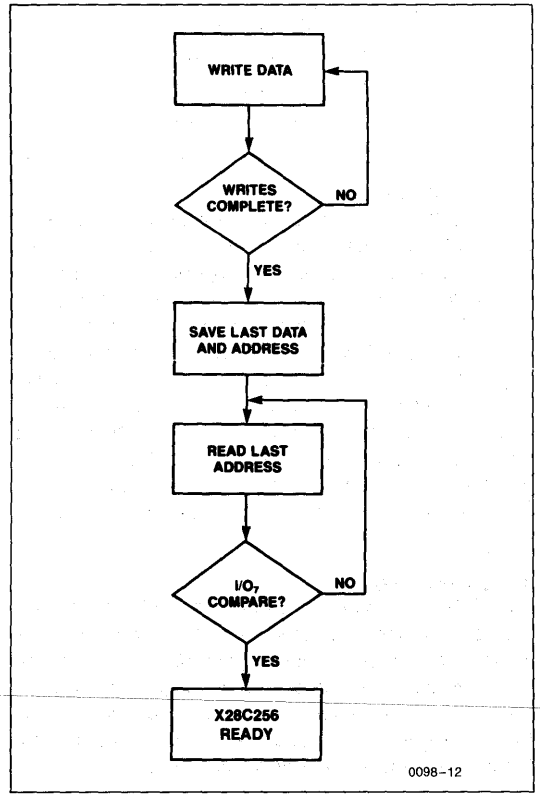


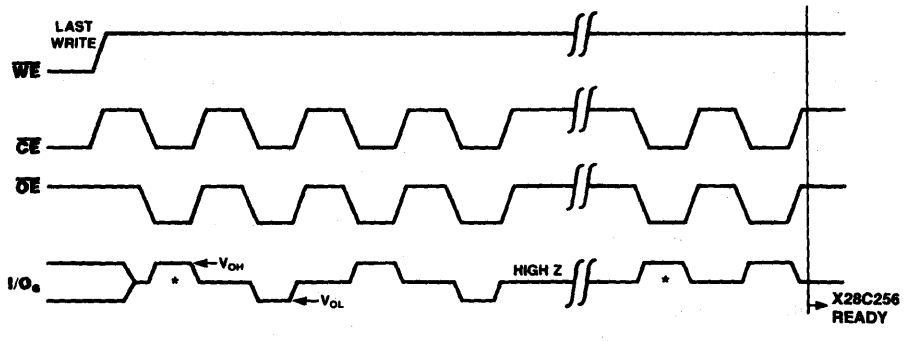
Figure 2b: $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

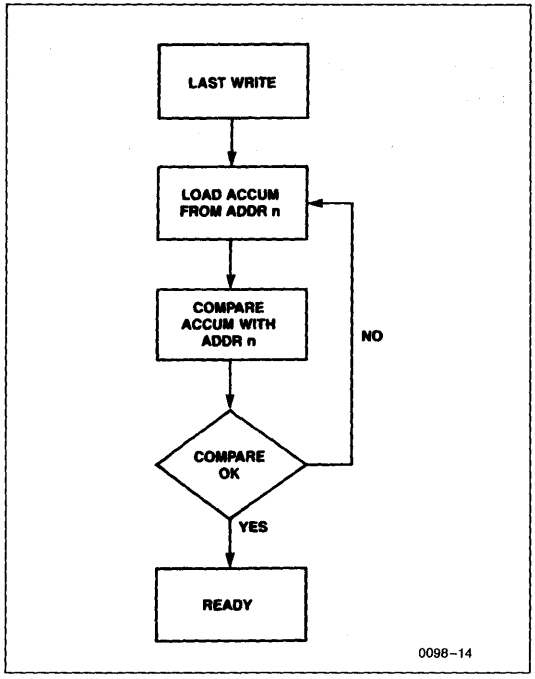
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.(12) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (12) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

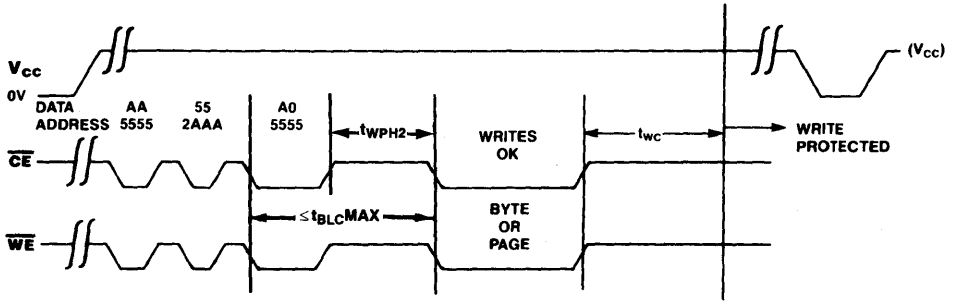
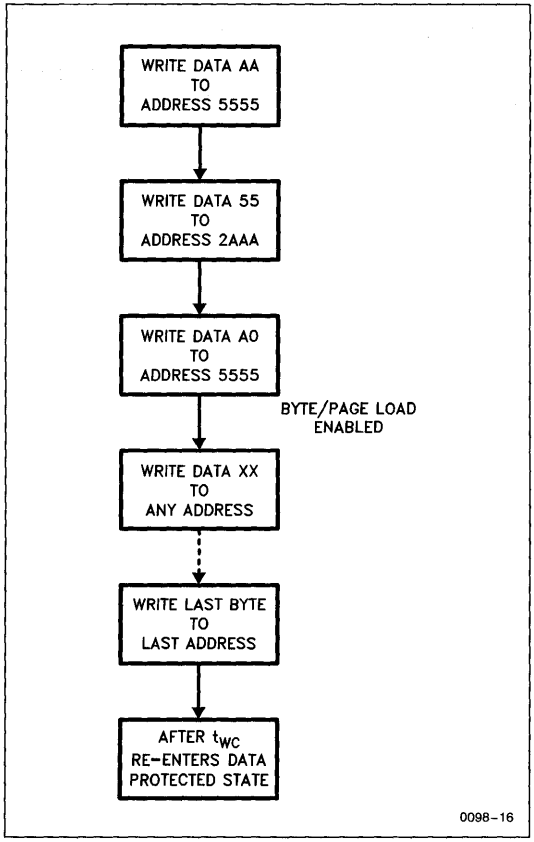


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

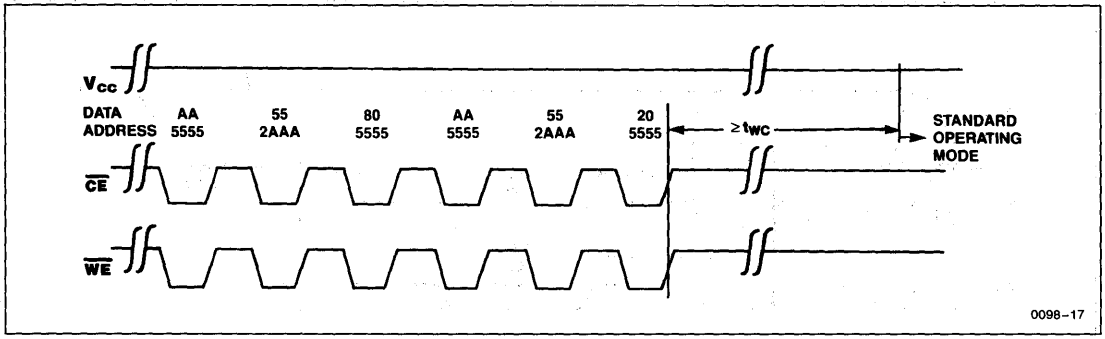
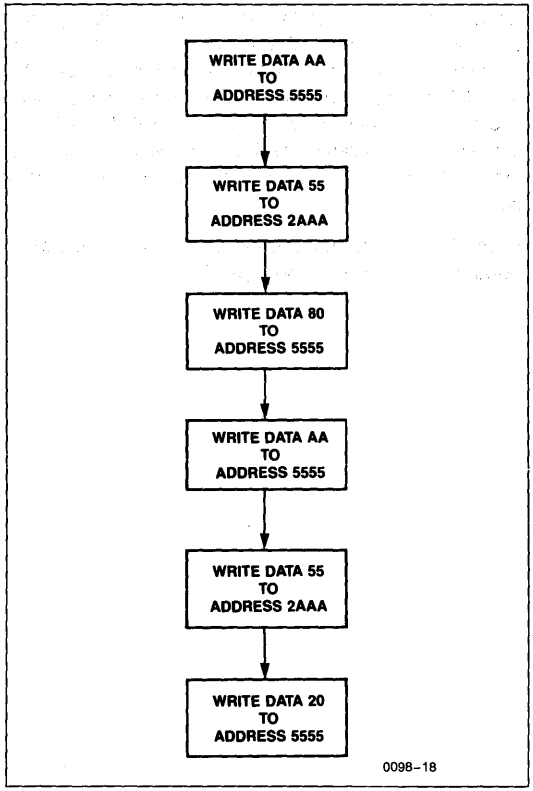


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

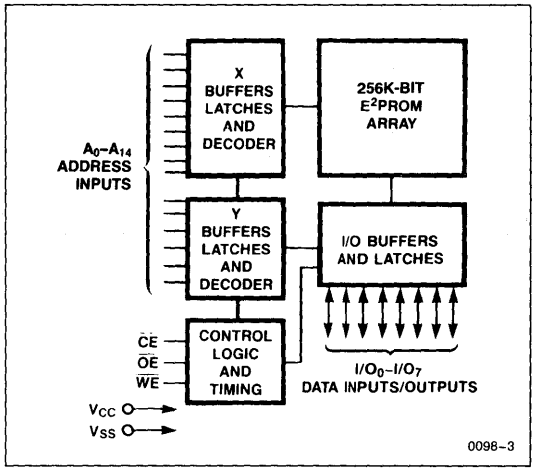
Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

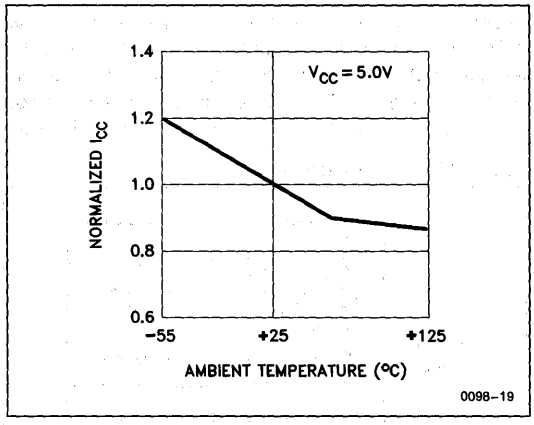
Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

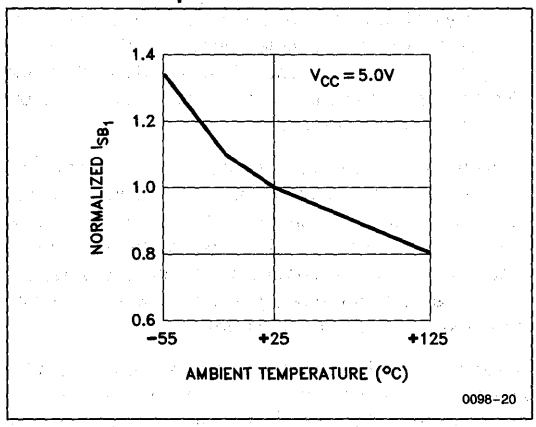
FUNCTIONAL DIAGRAM



Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



512K Commercial Industrial X28C512 X28C512I 64K x 8 Bit

Electrically Erasable PROM

FEATURES

- Low Power CMOS
  - —50 mA Active Current Max.
  - —500 μA Standby Current Max.
- Enhanced, High Speed Page Write Operation
- Fast Write Cycle Times
  - —128-Byte Page Size
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec.
  - —Effective Byte Write Cycle Time: 39 μs
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Testing Preferred for:
    - —Multiprocessor Applications
    - —Large Memory Arrays
    - —Interrupt Driven Systems
- Software Data Protection
- Two PLCC Pinouts
  - —X28C512–UVEPROM Replacements
  - —X28C513–X28C256 Upgrades
- Inherent 100+ Years Data Retention

DESCRIPTION

The Xicor X28C512 is a 64K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C512 is a 5V only device.

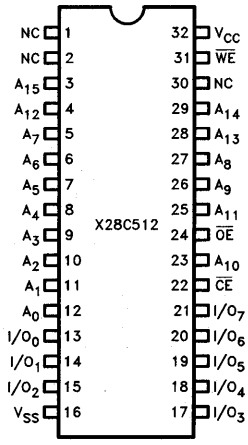
The X28C512 supports a 128-byte page write operation, effectively providing a 39 μs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C512 also features $\overline{\text{DATA}}$ Polling and Toggle Bit testing, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C512 supports the Software Data Protection option.

Xicor E²PROMs are designed and tested for applications requiring extended endurance.

3

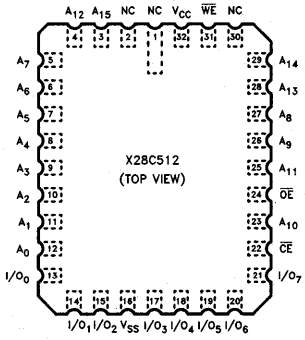
PIN CONFIGURATIONS

SIDE BRAZE FLAT PACK



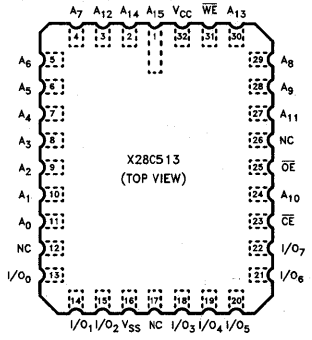
0117-1

PLCC LCC



0117-2

PLCC LCC



0117-3

PIN NAMES

A_0–A_{15}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X28C512 ..... −10°C to +85°C
X28C512I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C512 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C512I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		500	µA	$\overline{CE}$ = V_{CC} − 0.3V, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(1)	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 µA

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read Operation	100	µs
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

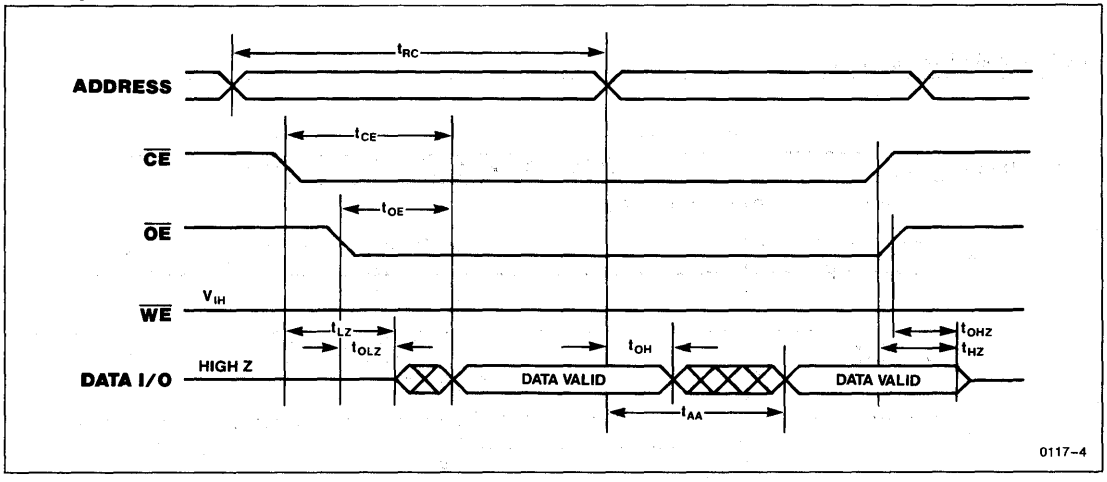
A.C. CHARACTERISTICS

X28C512 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C512I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C512-20 X28C512I-20		X28C512-25 X28C512I-25		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		ns
t_{CE}	Chip Enable Access Time		200		250	ns
t_{AA}	Address Access Time		200		250	ns
t_{OE}	Output Enable Access Time		50		50	ns
t_{LZ}(3)	$\overline{CE}$ Low to Active Output	0		0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Active Output	0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output		50		50	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Read Cycle



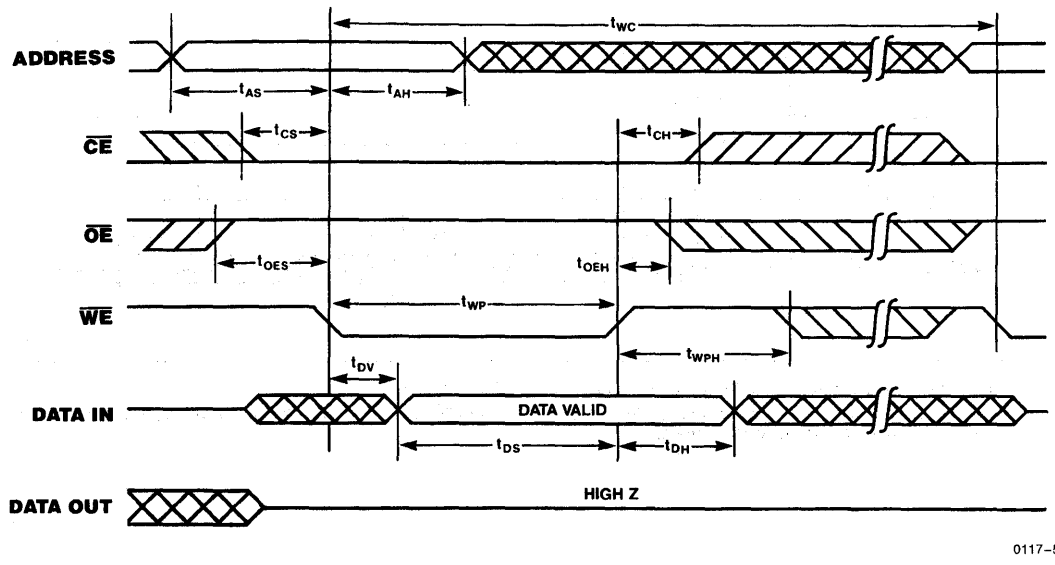
Notes: (3) t_{LZ} min. and t_{OLZ} min. are periodically sampled and not 100% tested.

(4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

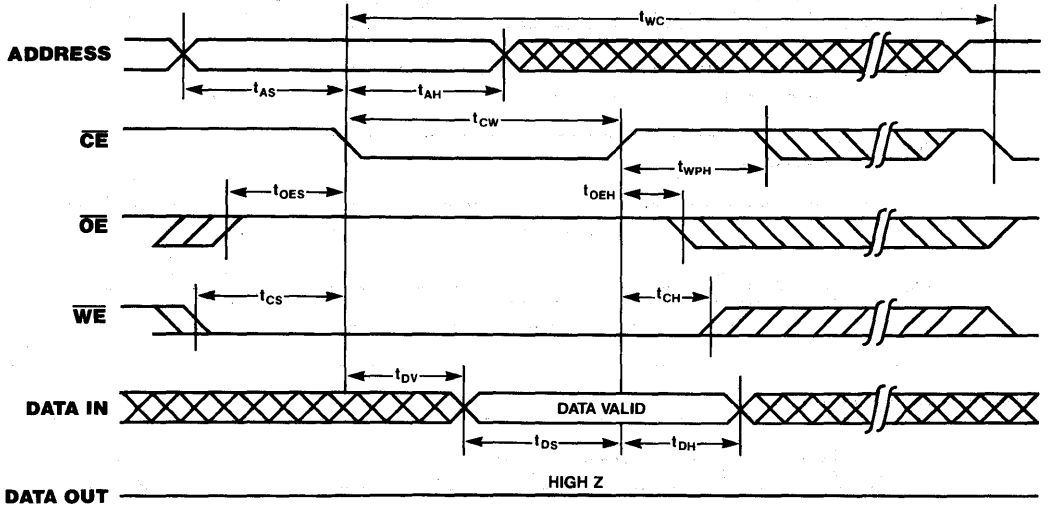
Symbol	Parameter	Min.	Max.	Units
t_{WC}(5)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.20	200	µs

$\overline{WE}$ Controlled Write Cycle

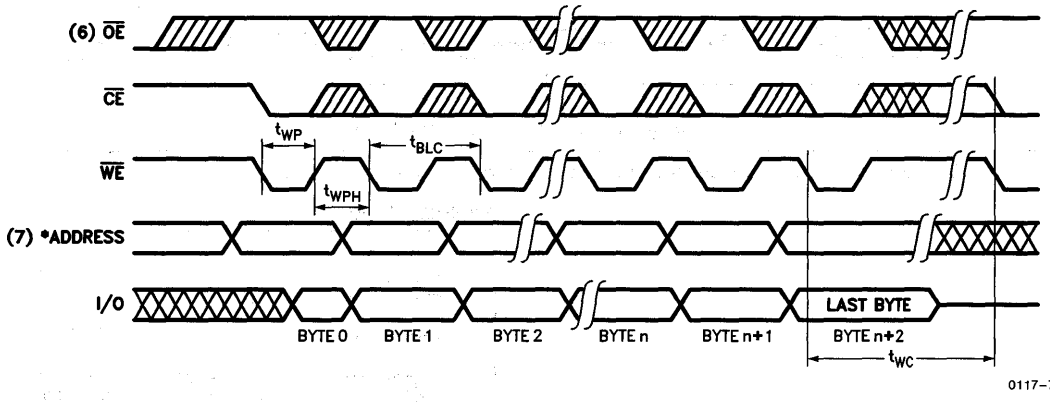


Note: (5) t_{WC} is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

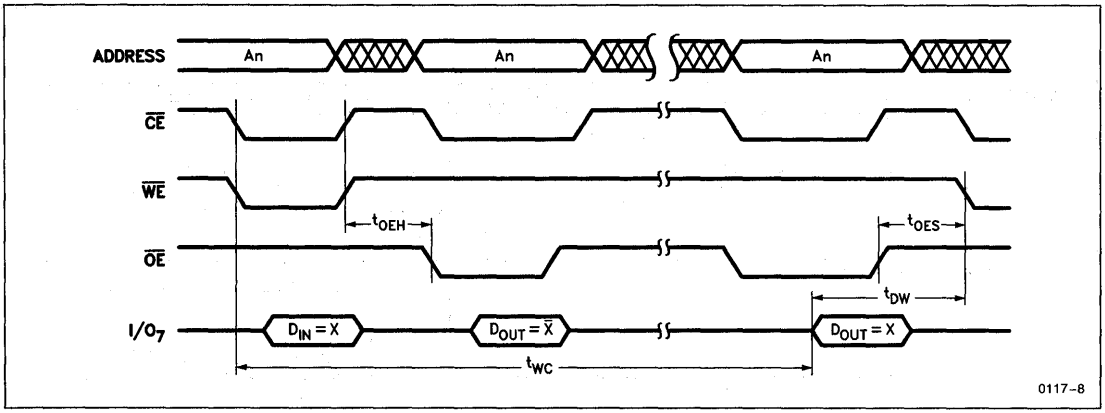


*For each successive write within the page write operation, A_7–A_{15} should be the same or writes to an unknown address could occur.

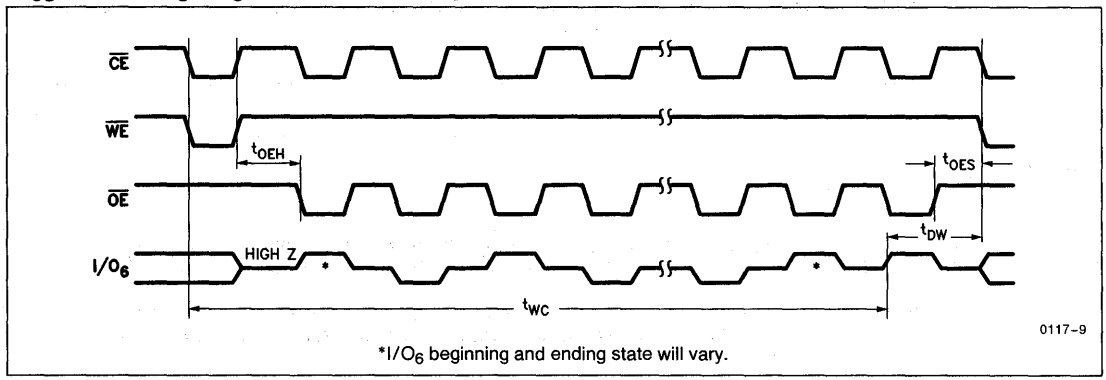
Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(8)



Toggle Bit Timing Diagram



*I/O_6 beginning and ending state will vary.

Note: (8) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PIN DESCRIPTIONS

Addresses (A_0–A_{15})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X28C512 through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X28C512.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

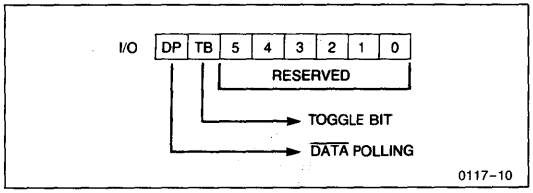
Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C512 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C512 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28C512 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_7 through A_{15}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 200 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 200 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 200 μs.

Write Operation Status Bits
The X28C512 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)
The X28C512 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C512, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)
The X28C512 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will alternate between one and zero on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2a: $\overline{DATA}$ Polling Bus Sequence

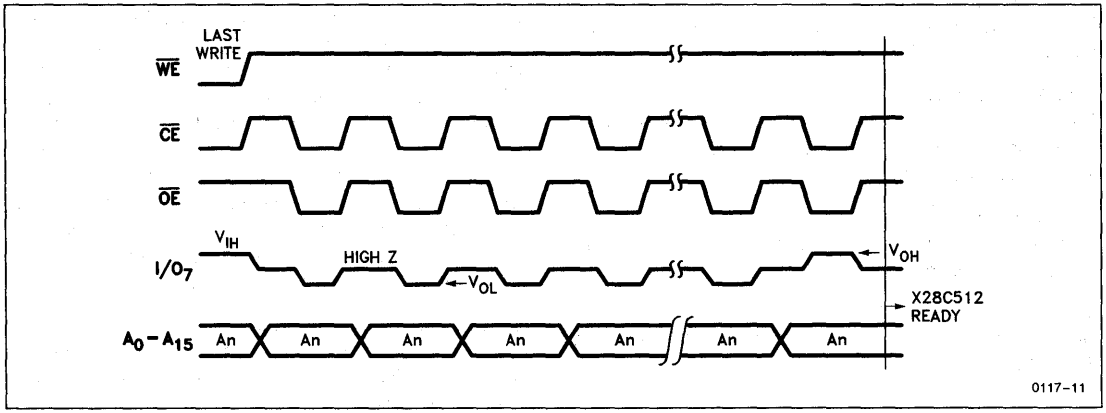
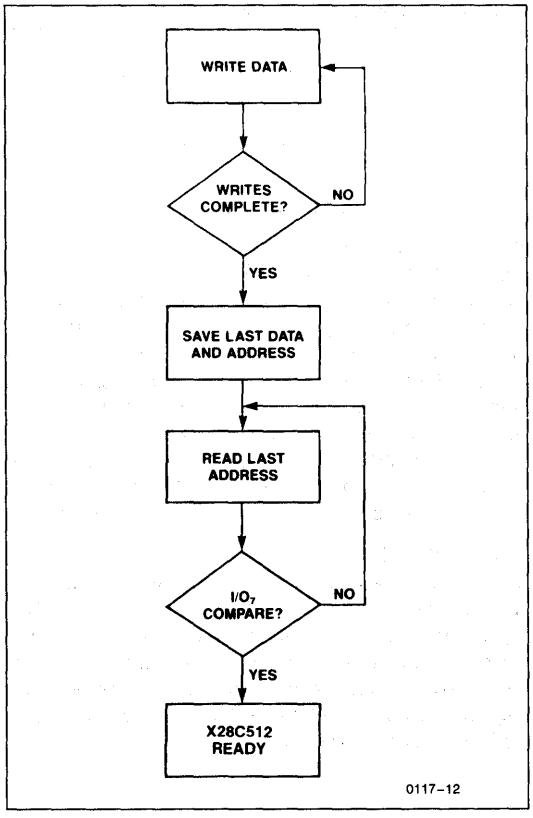


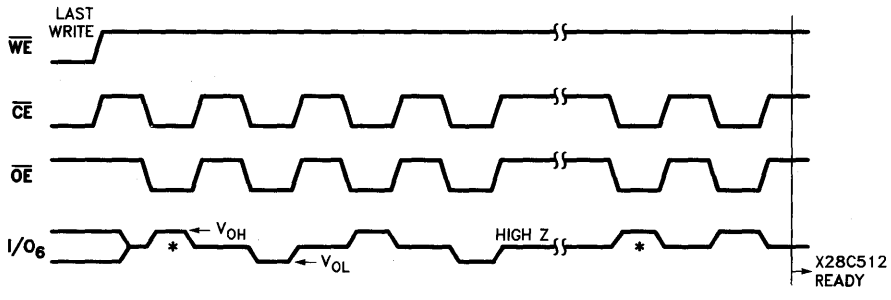
Figure 2b: $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C512. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

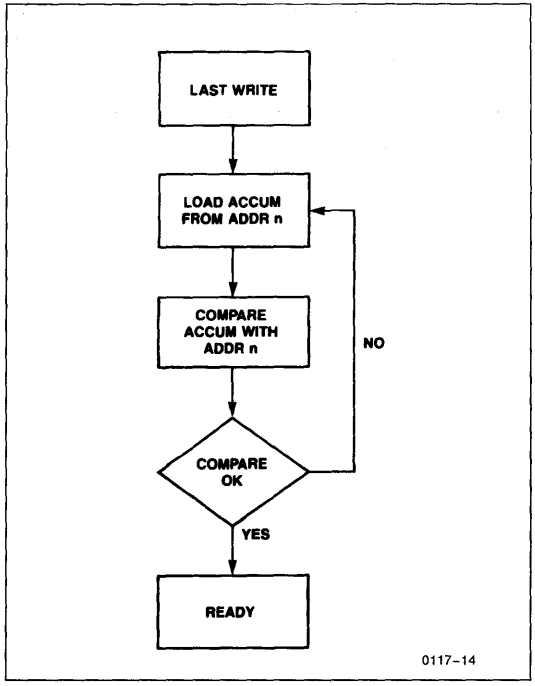
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C512 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

3

HARDWARE DATA PROTECTION

The X28C512 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3.8V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

SOFTWARE DATA PROTECTION

The X28C512 offers a software controlled data protection feature. The X28C512 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C512 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

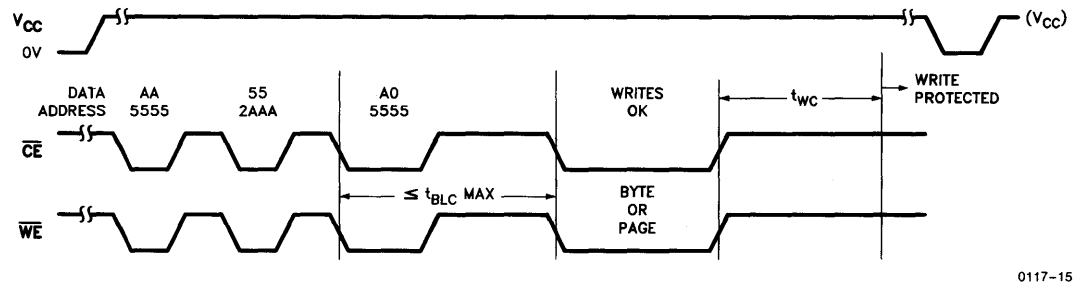
Once the software protection is enabled, the X28C512 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three byte enable sequence is not written to the memory array.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

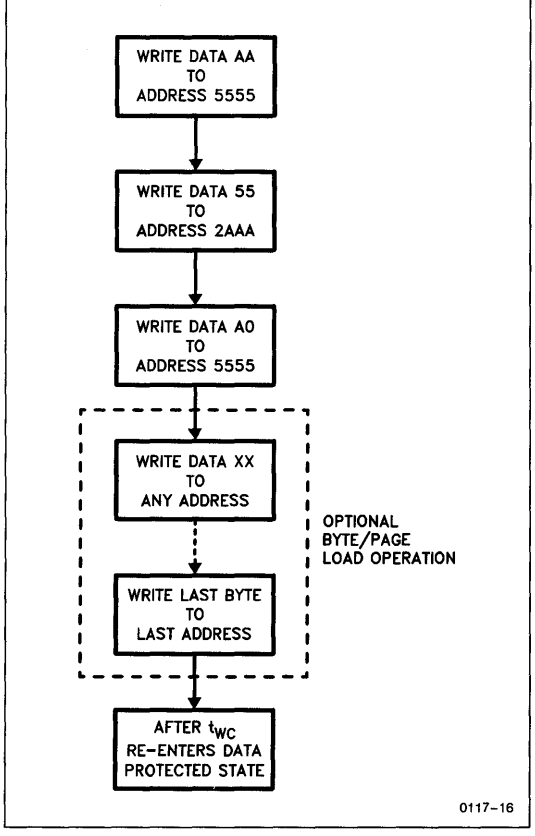
SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Software Data Protect Enable Sequence Followed by Byte or Page Write



NOTE: All other timings and control pins are per page write timing requirements.

Figure 4b: Write Sequence for Software Data Protection

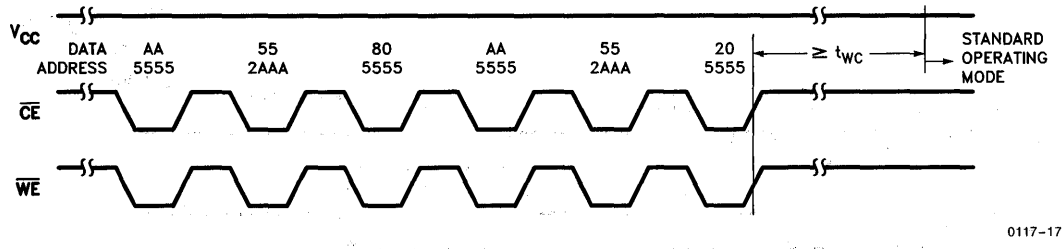


Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C512 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C512 will be write protected during power-down and after any subsequent power-up. The state of A_{15} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

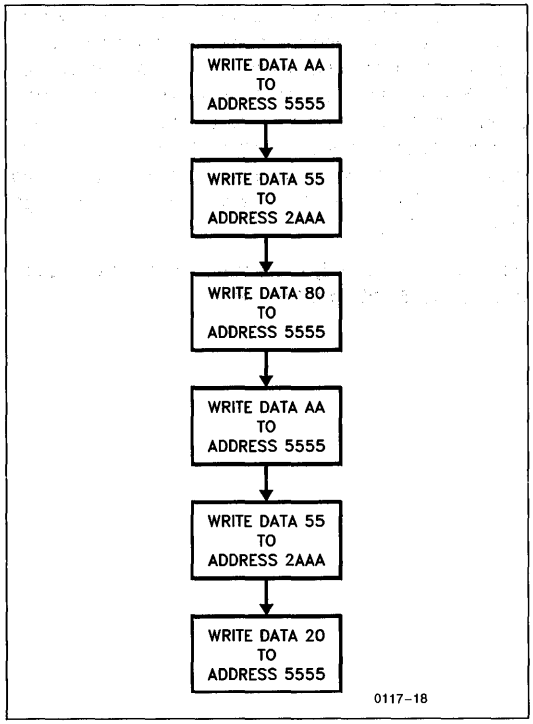
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence



NOTE: All other timings and control pins are per page write timing requirements.

Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C512 will be in standard operating mode. The state of A_{15} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

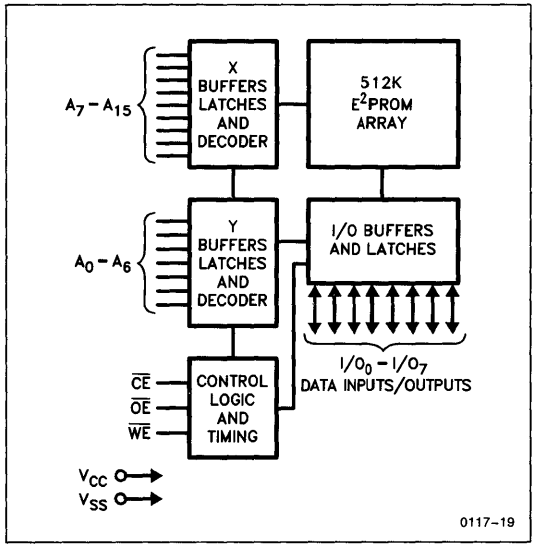
Because the X28C512 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C512 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



3

NOTES

1M Commercial X28C010 128K x 8 Bit

Electrically Erasable PROM

FEATURES

- 200 ns Access Time
- LOW Power CMOS
  - —80 mA Active Current Typical
  - —500 μA Standby Current Typical
- Fast Write Cycle Times
  - —128-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 5 Sec. Typical
  - —Effective Byte Write Cycle Time: 39 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

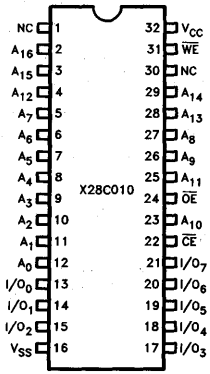
DESCRIPTION

The Xicor X28C010 is a 128K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28C010 supports a 128-byte page write operation, effectively providing a 39 μs/byte write cycle and enabling the entire memory to be typically written in less than 5 seconds. The X28C010 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C010 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

PIN CONFIGURATION

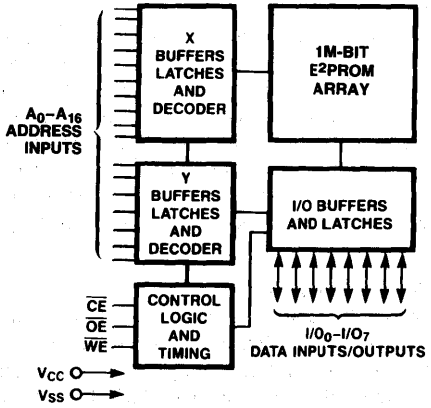


0084-1

PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0084-2

PIN DESCRIPTIONS

Addresses (A_0–A_{16})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the X28C010 through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the X28C010.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

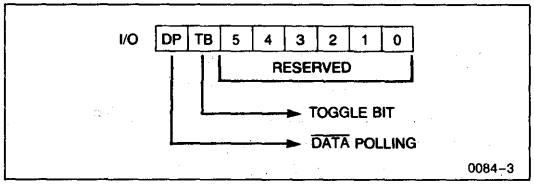
Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation
The page write feature of the X28C010 allows the entire memory to be written in 5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_7 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)
The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)
The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

NOTES

X9MME, X9MMEI 4-1

Xicor®

Commercial **X9MME**
Industrial **X9MMEI**

E²POT™ Digitally Controlled Potentiometer

FEATURES

- **Solid State Reliability**
- **Single Chip MOS Implementation**
- **Three Wire TTL Control**
- **Operates From Standard 5V Supply**
- **99 Resistive Elements**
  - **—Temperature Compensated**
  - **—±20% End to End Resistance Range**
- **100 Wiper Tap Points**
  - **—Wiper Position Digitally Controlled**
  - **—Wiper Position Stored in Nonvolatile Memory Then Automatically Recalled on Power-Up**
- **100 Year Wiper Position Retention**
- **8 Pin Mini-DIP Package**
- **14 Pin SOIC Package**

DESCRIPTION

The Xicor X9MME is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

The X9MME is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element on the array is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and is recalled upon a subsequent power-up.

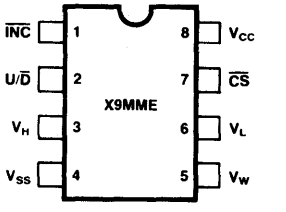
The resolution of the X9MME is equal to the maximum resistance value divided by 99. As an example; for the X9503 (50 KΩ) each tap point represents 505Ω.

Xicor E² products are designed and tested for applications requiring extended endurance. Refer to Xicor reliability reports for further endurance information.

4

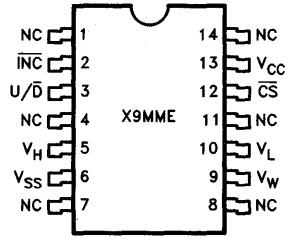
PIN CONFIGURATIONS

PLASTIC



0039-1

SOIC



0039-12

PIN NAMES

V_H	High Terminal of Pot
V_W	Wiper Terminal of Pot
V_L	Low Terminal of Pot
V_{SS}	Ground
V_{CC}	System Power
U/$\overline{D}$	Up/Down Control
$\overline{INC}$	Wiper Movement Control
$\overline{CS}$	Chip Select for Wiper Movement/Storage
NC	No Connect

ANALOG CHARACTERISTICS

Electrical Characteristics

End to End Resistance Tolerance ..... ±20%
Power Rating at 25°C
X9102 ..... 16 mW
X9103, X9503 and X9104 ..... 10 mW
Wiper Current ..... ±1 mA Max.
Typical Wiper Resistance ..... 40Ω at 1 mA
Typical Noise
X9102 ..... < −120 dB/√Hz Ref: 1V
X9103, X9503 and X9104 ..... < −95 dB/√Hz Ref: 1V

Resolution

Resistance 1%

Linearity

Absolute Linearity(1) ..... ±1.0 MI(2)
Relative Linearity(3) ..... ±0.2 MI(2)

Temperature Coefficient

−40°C to +85°C
X9102 ..... ±600 ppm/°C Typical
X9103, X9503 and X9104 ..... ±300 ppm/°C Typical
Ratiometric Temperature Coefficient ..... ±20 ppm

Wiper Adjustability

Unlimited Wiper Adjustment
(Volatile Mode While Chip is Selected)
Nonvolatile Storage of Wiper Position
..... 10,000 Cycles Typical

Environmental Characteristics

Temperature Range
Operating X9MME ..... 0°C to +70°C
X9MMEI ..... −40°C to +85°C
Storage ..... −65°C to +150°C

Physical Characteristics

Marking Includes:
Manufacturer's Trademark
Resistance Value or Code
Date Code

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
Referenced to Ground ..... −1.0V to +7.0V
Voltage on V_H and V_L
Referenced to Ground ..... −8.0V to +8.0V
Lead Temperature (Soldering, 10 Seconds) ..... +300°C
Wiper Current ..... ±1 mA
$\Delta V = |V_H - V_L|$
X9102 ..... 4V
X9103, X9503 and X9104 ..... 10V

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X9MME T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X9MMEI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	Supply Current		25	35	mA	
I_{LI}	Input Leakage Current			±10	µA	V_{IN} = 0V to 5.5V, $\overline{INC}$, U/$\overline{D}$, $\overline{CS}$
V_{IH}	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{IL}	Input Low Voltage	−1.0		0.8	V	
R_W	Wiper Resistance		40	100	Ω	±1 mA
V_{VH}(5)	V_H Voltage	−5.0		+5.0	V	
V_{VL}(5)	V_L Voltage	−5.0		+5.0	V	
C_{IN}(6)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, Input Capacitance			10	pF	

Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

Absolute Linearity = ($V_{W(n)}$(actual) − $V_{W(n)}$(expected)) = ±1 MI Max.

(2) 1 MI = $R_{TOT}/99$ or $\frac{V_H - V_L}{99}$ = Minimum Increment.

(3) Relative Linearity is utilized to determine the actual change in voltage between successive tap position when used as a potentiometer. It is a measure of the error in step size.

Relative Linearity = $V_{W(n+1)} - [V_{W(n)} + MI]$ = ±0.2 MI Max.

Typical values of Linearity are shown in Figures 3, 6, 9 and 12.

(4) Typical values are for T_A = 25°C and nominal supply voltage.

(5) ΔV for X9102 = $|V_H - V_L| \leq 4V$. ΔV for X9103, X9503 and X9104 = $|V_H - V_L| \leq 10V$.

(6) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input	1.5V

MODE SELECTION

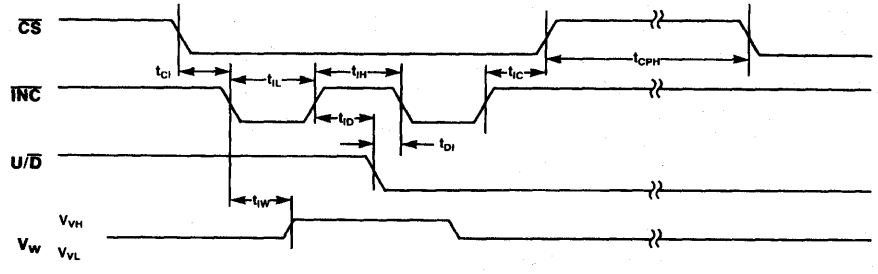
$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↓	H	Wiper Up
L	↓	L	Wiper Down
↑	H	X	Store Wiper Position

A.C. CHARACTERISTICS

X9MME T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X9MMEI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units
		Min.	Typ.(7)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ High to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ Low Period	1			µs
t_{IH}	$\overline{INC}$ High Period	3			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to V_W Change		100	500	µs

A.C. Timing



Note: (7) Typical values are for T_A = 25°C and nominal supply voltage.

PIN DESCRIPTIONS

V_H
The high terminal of the X9MME is capable of handling an input voltage from −5V to +5V.

V_L
The low terminal input is limited from −5V to +5V.

V_W
The wiper terminal series resistance is typically less than 40Ω. The value of the wiper is controlled by the use of U/$\overline{D}$ and $\overline{INC}$.

Up/Down (U/$\overline{D}$)
The U/$\overline{D}$ input controls the direction of the wiper movement and the value of the nonvolatile counter.

Increment ($\overline{INC}$)
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)
The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH with $\overline{INC}$ HIGH.

DEVICE OPERATION
The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. HIGH to LOW transitions on $\overline{INC}$, with $\overline{CS}$ LOW, increment (U/$\overline{D}$ = HIGH) or decrement (U/$\overline{D}$ = LOW) an internal counter. The output of the counter is decoded to position the wiper. When $\overline{CS}$ is brought HIGH the counter value is automatically stored in the nonvolatile memory. Upon power-up the nonvolatile memory contents are restored to the counter.

With the wiper at position 99, additional increments (U/$\overline{D}$ = HIGH) will not move the wiper. With the wiper at position 0, additional decrements (U/$\overline{D}$ = LOW) will not move the wiper.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW, allowing a gross then fine adjustment during system calibration.

If V_{CC} is removed while $\overline{CS}$ is LOW the contents of the nonvolatile memory may be lost.

The end to end resistance of the array will fluctuate once V_{CC} is removed.

APPLICATIONS
The combination of a digital interface and nonvolatile memory in a silicon based trimmer pot provides many application opportunities that could not be addressed by either mechanical potentiometers or digital to analog circuits. The X9MME addresses and solves many issues that are of concern to designers of a wide range of equipment.

Consider the possibilities:

Automated assembly line calibration versus mechanical tweaking of potentiometers.

Protection against drift due to vibration or contamination.

Eliminate precise alignment of PWB mounted potentiometers with case access holes.

Eliminate unsightly access holes on otherwise aesthetically pleasing enclosures.

Product enhancements such as keyboard adjustment of volume or brightness control.

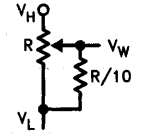
Front panel microprocessor controlled calibration of test instruments.

Remote location calibration via radio, modem or LAN link.

Calibration of hard to reach instruments in aircraft or other confined spaces.

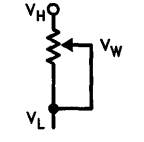
APPLICATION CIRCUITS

Application Circuit #1



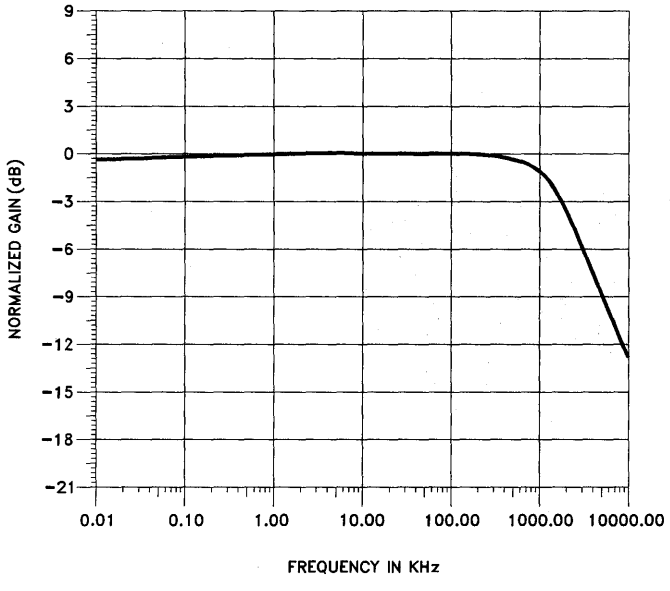
Approximating audio trim with external resistor.

Application Circuit #2



Utilizing the X9MME as a variable resistor.
Note: Maximum Wiper Current = 1 mA.

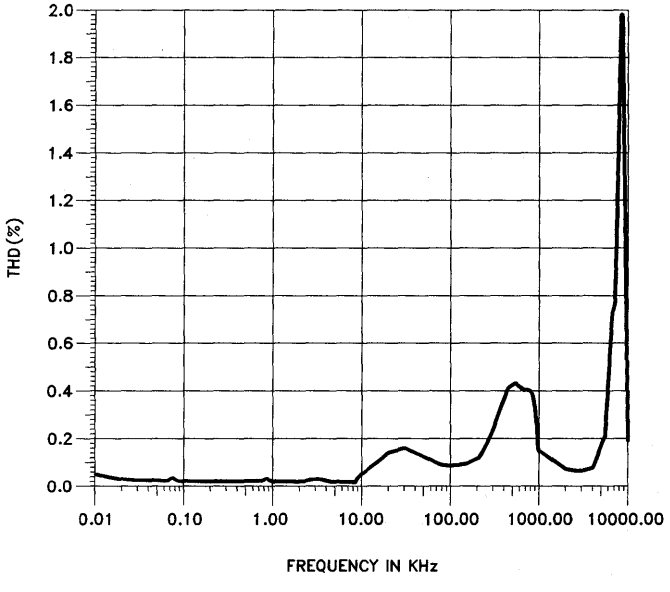
Figure 1: Typical Frequency Response for X9102



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039-13

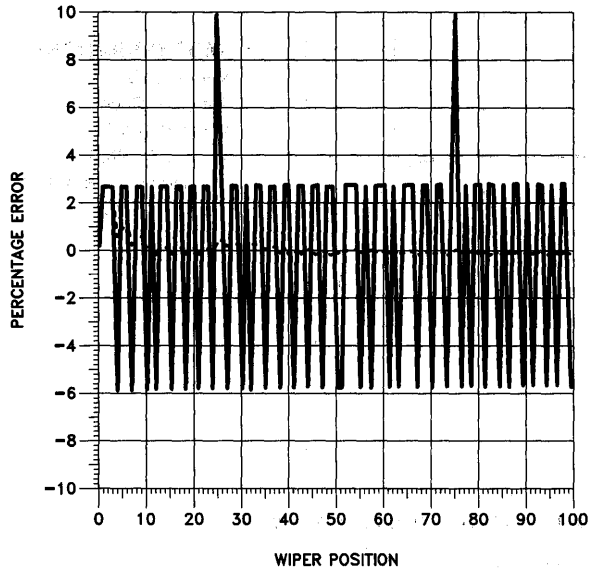
Figure 2: Typical Total Harmonic Distortion for X9102



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 2V RMS
Test Circuit #1

0039-14

Figure 3: Typical Linearity for X9102

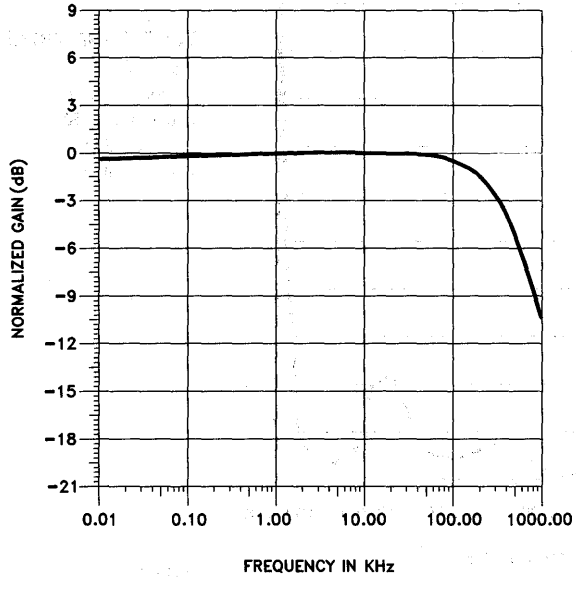


TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Test Circuit #2

KEY:
- - - - - - = ABSOLUTE
——— = RELATIVE
0039-9

0039-15

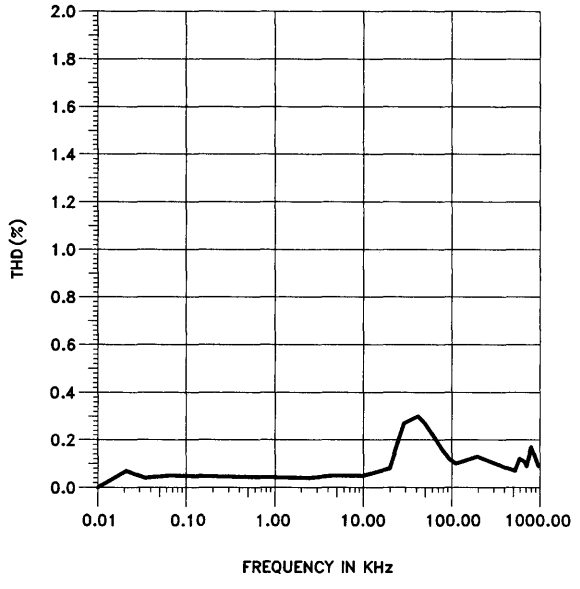
Figure 4: Typical Frequency Response for X9103



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039-6

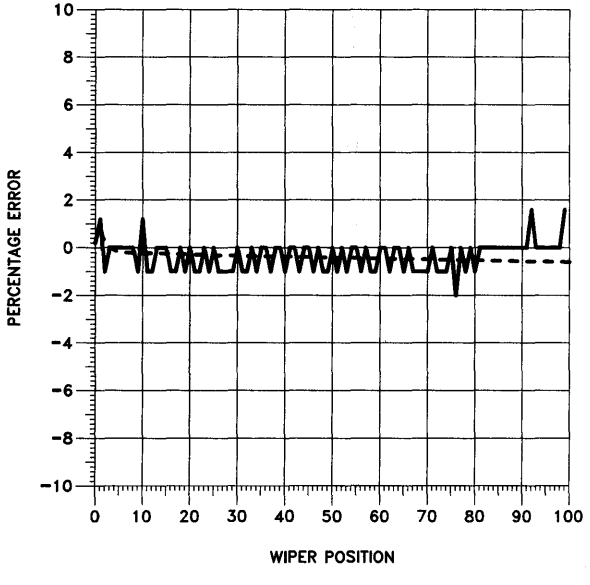
Figure 5: Typical Total Harmonic Distortion for X9103



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 2V RMS
Test Circuit #1

0039-7

Figure 6: Typical Linearity for X9103



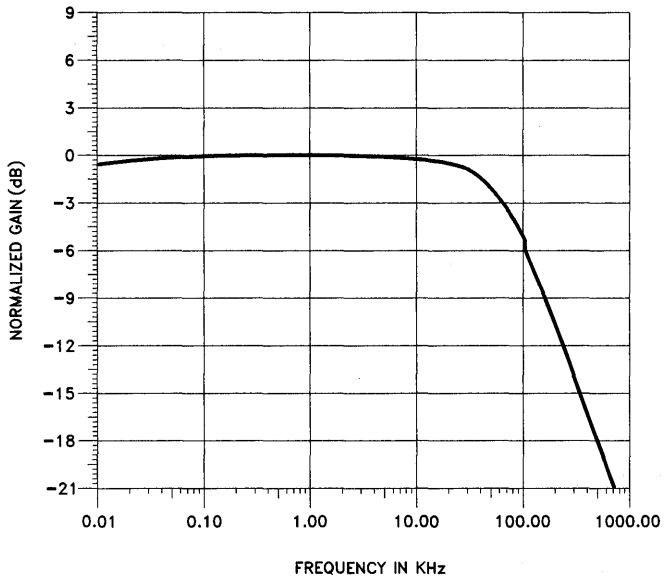
TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Test Circuit #2

KEY:
- - - - - - = ABSOLUTE
——— = RELATIVE

0039-9

0039-8

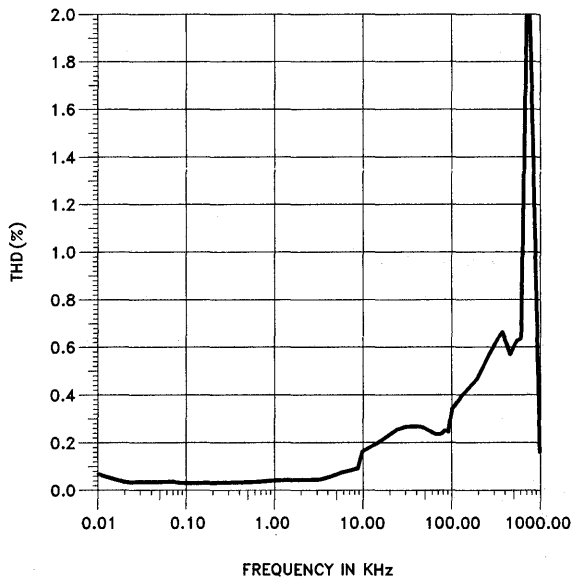
Figure 7: Typical Frequency Response for X9503



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039-16

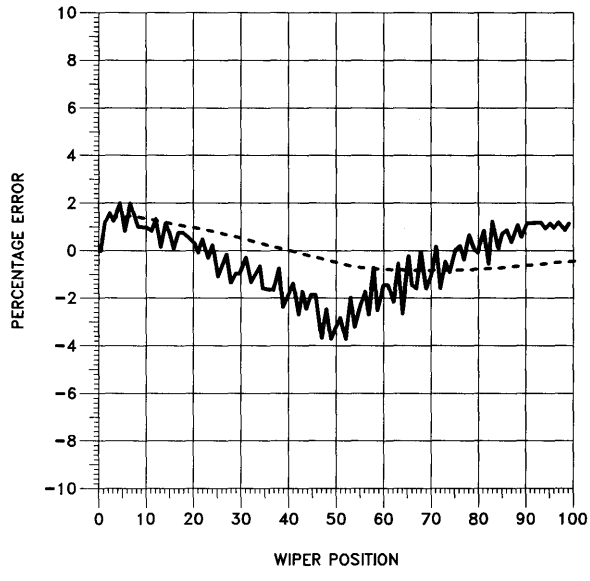
Figure 8: Typical Total Harmonic Distortion for X9503



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 2V RMS
Test Circuit #1

0039-17

Figure 9: Typical Linearity for X9503

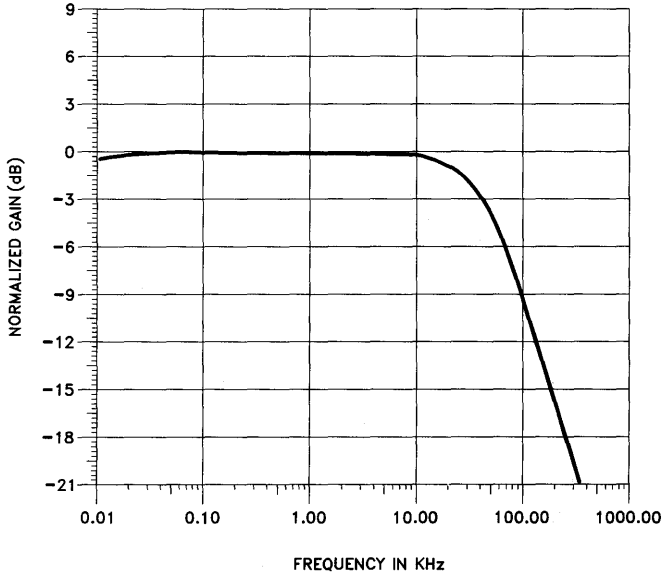


TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Test Circuit #2

KEY:
- - - - - - = ABSOLUTE
——— = RELATIVE
0039-9

0039-18

Figure 10: Typical Frequency Response for X9104



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039-19

Figure 11: Typical Total Harmonic Distortion for X9104

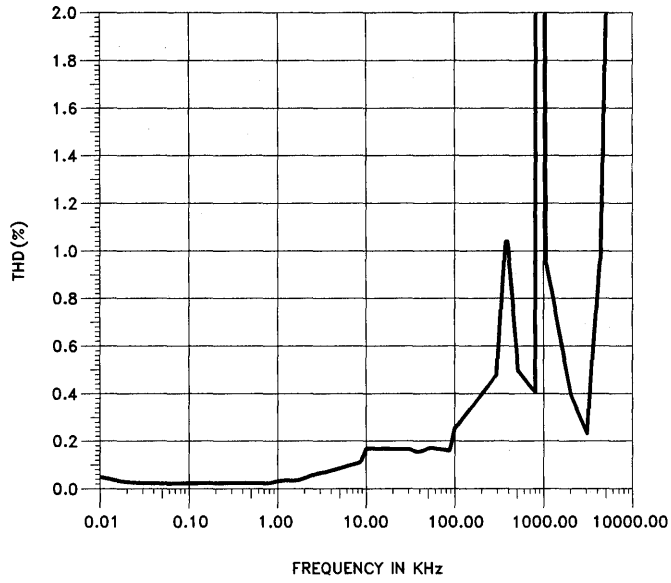
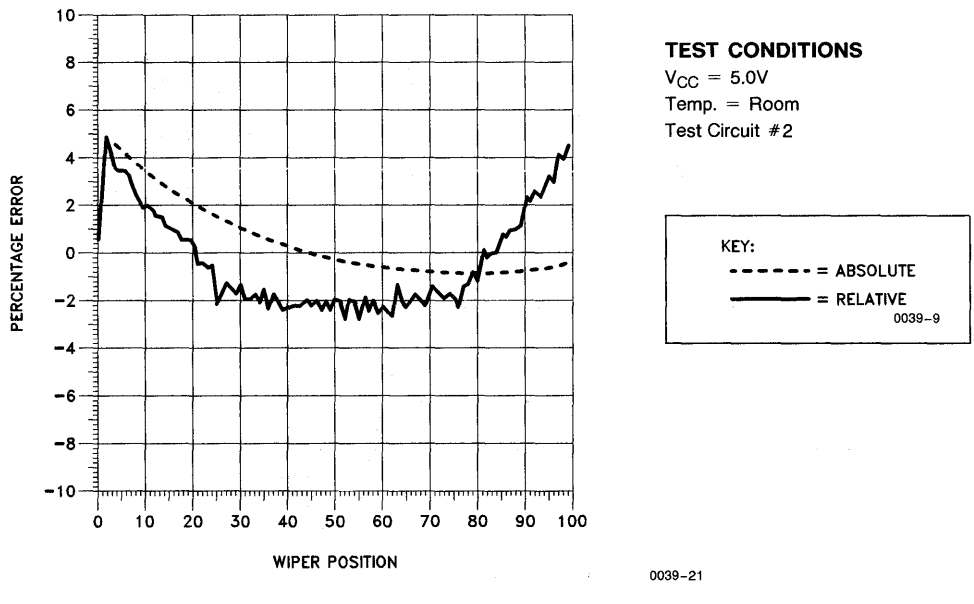
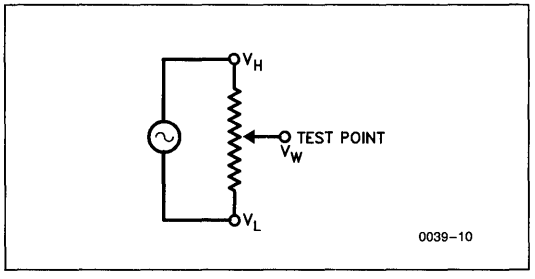


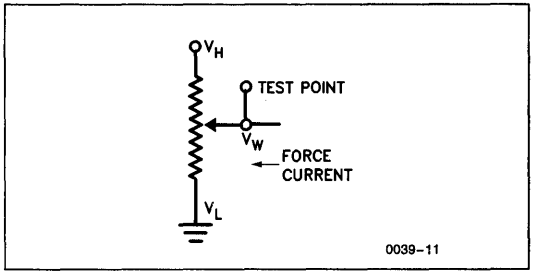
Figure 12: Typical Linearity for X9104



Test Circuit #1



Test Circuit #2

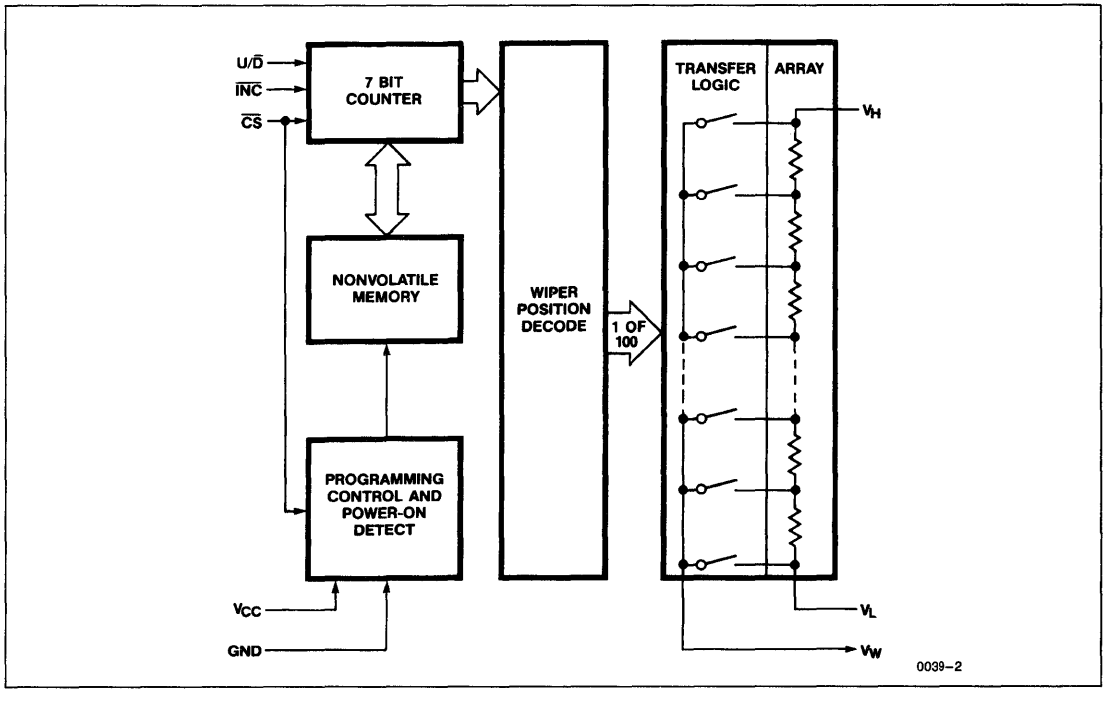


Standard Parts

Minimum Resistance	Wiper Increments	Maximum Resistance	Part Number
40Ω	10.1Ω	1 KΩ	X9102
40Ω	101Ω	10 KΩ	X9103
40Ω	505Ω	50 KΩ	X9503
40Ω	1010Ω	100 KΩ	X9104

4

FUNCTIONAL DIAGRAM



NOTES

X88C64, X88C64I 5-1

64K Commercial Industrial X88C64 X88C64I 8192 x 8 Bit

E² Micro-Peripheral

FEATURES

- **Concurrent Software Execution While Writing**
  - **—Dual Plane Architecture**
    - **Isolates Read/Write Functions Between Planes**
    - **Allows Continuous Execution of Code From One Plane While Writing in the Other Plane**
- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 8-Bit Microcontrollers, e.g.**
    - **Intel MCS®-51 Family**
    - **Motorola M6801/03, M68HC11 Family**
- **High Performance CMOS**
  - **—Fast Access Time, 120 ns**
  - **—Low Power**
    - **40 mA Active**
    - **100 μA Standby**
- **Software Data Protection**
  - **—Protect Entire Array During Power-Up/-Down**
- **Block Protect Register**
  - **—Individually Set Write Lock Out in 1K Blocks**
- **Toggle Bit**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 32 Bytes to be Written in One Write Cycle**

DESCRIPTION

The X88C64 is an 8K x 8 E²PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X88C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X88C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

The X88C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are 8 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to the Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

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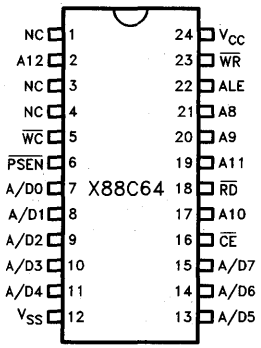
PIN CONFIGURATION



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PIN NAMES

ALE	Address Latch Enable
AD_0–AD_7	Address Inputs/Data I/O
A_8–A_{12}	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
V_{SS}	Ground

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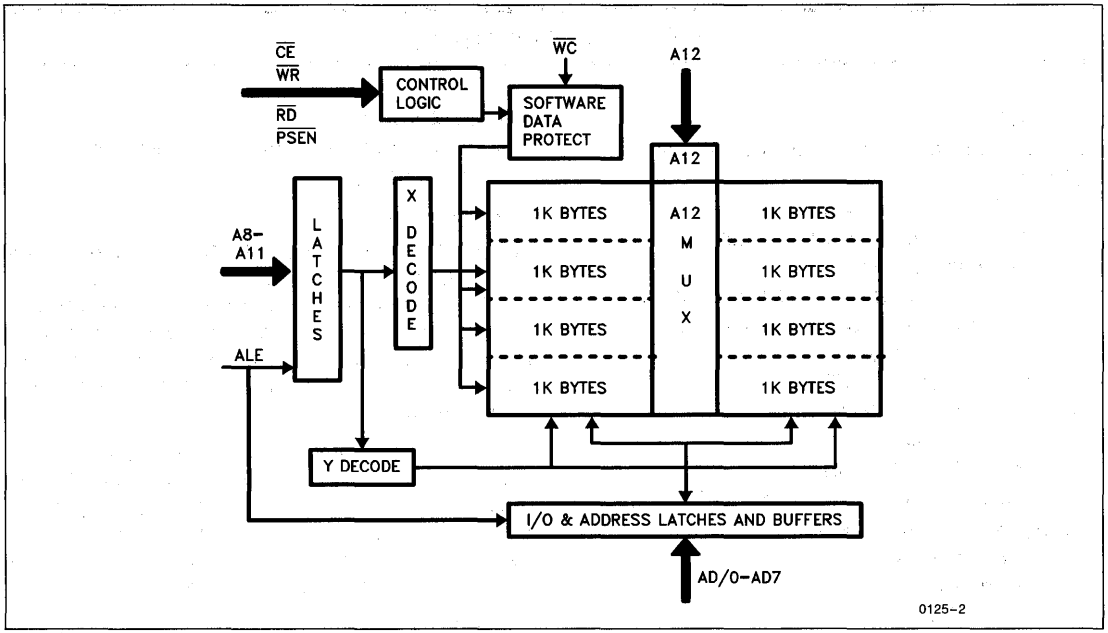
FUNCTIONAL DIAGRAM



PRINCIPLES OF OPERATION

The X88C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88C64 provides 8K bytes of 5-volt E^{2}PROM which can be used either for Program Storage, Data Storage or a combination of both in systems based upon Harvard (80XX) or Von Neumann (68XX) architectures. The X88C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X88C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88C64 into both the Program and the Data Memory address map.

The X88C64 is internally organized as two independent arrays of 4K bytes of memory with the A_{12} input selecting which of the two blocks of memory are to be accessed. While the processor is executing code out of one block, write operations can take place in the other block; allowing the processor to continue execution of code out of the X88C64 during a byte or page write to the device.

The X88C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88C64 also features a Write Control input, which serves as an external control over the completion of a previously initiated page load cycle.

The X88C64 also features the industry standard 5-volt E^{2}PROM characteristics such as byte or page mode write and toggle-bit polling.

PIN DESCRIPTIONS

Address/Data (AD_0–AD_7)

Multiplexed low-order addresses and data. The Addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$ and $\overline{CE}$.

Addresses (A_8–A_{12})

High order addresses flow into the device when ALE = V_{IH} and are latched when ALE = V_{IL}.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH and ALE is HIGH, the X88C64 is placed in the low power standby mode.

Program Store Enable ($\overline{PSEN}$)

When the X88C64 is to be used in a MCS-51 based system, $\overline{PSEN}$ is tied directly to the microcontroller's $\overline{PSEN}$ output.

When the X88C64 is used in any other type of system, $\overline{PSEN}$ should be tied LOW.

Read ($\overline{RD}$)

When the X88C64 is to be used in a MCS-51 based system, $\overline{RD}$ is tied directly to the microcontroller's $\overline{RD}$ output. When used with a MC6801 or MC6803 the $\overline{RD}$ input is tied directly to the E output of the microcontroller.

Write ($\overline{WR}$)

When the X88C64 is to be used in a MCS-51 based system, $\overline{WR}$ is tied directly to the microcontroller's $\overline{WR}$ output. When used with a MC6801 or MC6803 the $\overline{WR}$ input is tied directly to the R/$\overline{W}$ output of the microcontroller.

Address Latch Enable (ALE)

Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

Write Control ($\overline{WC}$)

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E^2PROM. If the Write Control input is driven HIGH immediately after Write ($\overline{WR}$) goes HIGH, the write cycle will be aborted. When $\overline{WC}$ is LOW (tied to V_{SS}) the X88C64 will be enabled to perform write operations. When $\overline{WC}$ is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

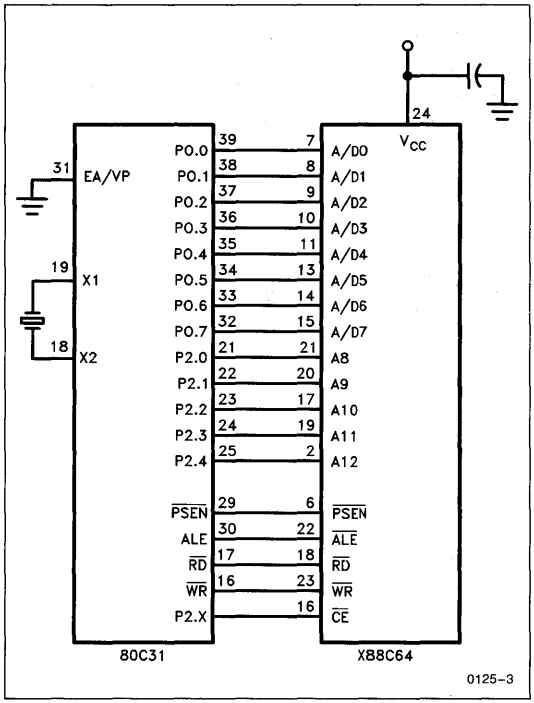
DEVICE OPERATION

MCS-51 Modes

Mixed Program/Data Memory

By properly assigning the address spaces, a single X88C64 can be used as both the Program and Data Memory. This would be accomplished by connecting all the MCS-51 control outputs to the corresponding inputs of the X88C64.

In this configuration, one plane of memory could be dedicated to Program Store and the other plane dedicated to Data Store. The Data Store can be fully protected by enabling block protect write lock out.



Program Memory Mode

This mode of operation is read only. The $\overline{PSEN}$ and ALE inputs of the X88C64 are tied directly to the $\overline{PSEN}$ and ALE outputs of the microcontroller. The $\overline{RD}$ and $\overline{WR}$ inputs are tied HIGH.

When ALE is HIGH, the AD_0–AD_7 and A_8–A_{12} addresses flow into the device. The addresses, both low and high order, are latched when ALE transitions LOW (V_{IL}). $\overline{PSEN}$ will then go LOW and after t_{PLDV}, valid data is presented on the AD_0–AD_7 pins. $\overline{CE}$ must be LOW during the entire operation.

Data Memory Mode

This mode of operation allows both read and write functions. The $\overline{PSEN}$ input is tied to V_{IH} or to V_{CC} through a pullup resistor. The ALE, $\overline{RD}$ and $\overline{WR}$ inputs are tied directly to the microcontroller's ALE, $\overline{RD}$ and $\overline{WR}$ outputs.

Read

This operation is quite similar to the Program Memory read. A HIGH to LOW transition on ALE latches the addresses and the data will be output on the AD pins after $\overline{RD}$ goes LOW (t_{RLDV}).

Write

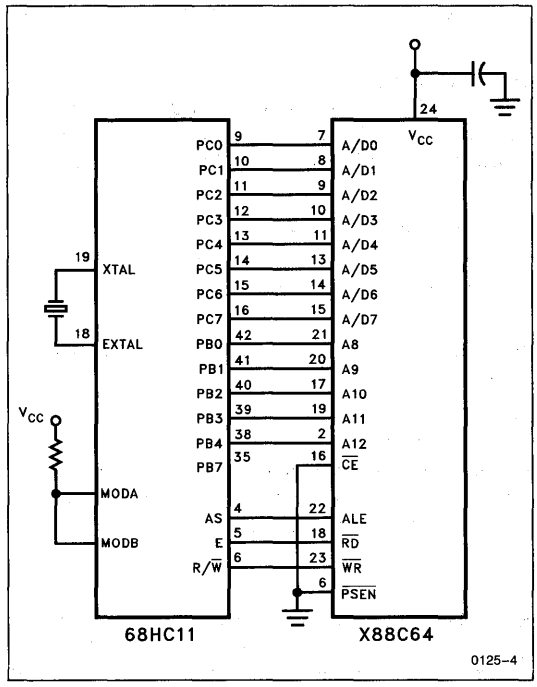
A write is performed by latching the addresses on the falling edge of ALE. Then $\overline{WR}$ is strobed low followed by valid data being presented at the AD_0–AD_7 pins. The data will be latched into the X88C64 on the rising edge of $\overline{WR}$.

MOTOROLA MEMORY MODE

Motorola 68XX operation is slightly different. The X88C64 internal logic requires $\overline{PSEN}$ to be tied to V_{SS}; the microcontroller's AS, E and R/$\overline{W}$ outputs tied to the X88C64 ALE, $\overline{RD}$ and $\overline{WR}$ inputs respectively.

The falling edge of AS will latch the addresses for both a read and write operation. The state of R/$\overline{W}$ output determines the operation to be performed, with the E signal acting as a data strobe.

If R/$\overline{W}$ is HIGH and $\overline{CE}$ LOW (read operation) data will be output at AD_0–AD_7 after E transitions HIGH. If R/$\overline{W}$ and $\overline{CE}$ are LOW (write operation) data presented at AD_0–AD_7 will be strobed into the X88C64 on the HIGH to LOW transition of E.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X88C64 ..... −10°C to +85°C
X88C64I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X88C64 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X88C64I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	V_{CC} Current (Active)		50	80	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's Open, Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		200		µA	$\overline{CE}$ = V_{IL} −0.3V, All I/O's Open, Other Inputs = V_{CC} −0.3V
$I_{SB2(TTL)}$	V_{CC} Current (Standby)			6	mA	$\overline{CE}$ = V_{IH}, All I/O's Open, Other Inputs = V_{IH}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{RD}$ = V_{IH}
V_{IL}	Input Low Voltage	−1.0		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}$	Mode	I/O	Power
V_{CC}	X	X	X	Standby	High Z	Standby (CMOS)
V_{IH}	X	X	X	Standby	High Z	Standby (TTL)
V_{IL}	V_{IL}	V_{IH}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	V_{IH}	⌐	Write	D_{IN}	Active
⌐	V_{IH}	V_{IH}	V_{IL}	Write	D_{IN}	Active

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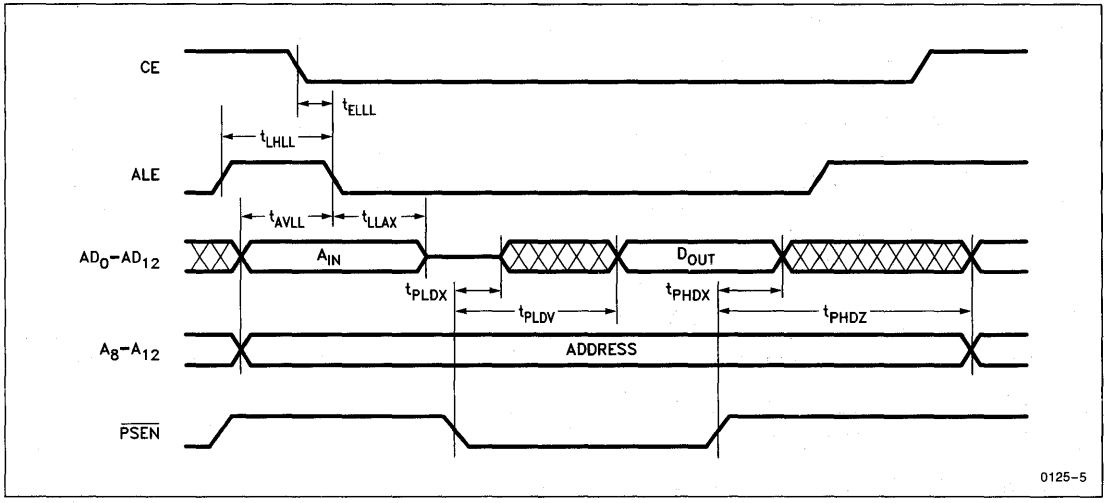
A.C. CHARACTERISTICS

X88C64 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X88C64I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{ELLL}	Chip Enable Setup Time		7		ns
t_{LHLL}	ALE Pulse Width		80		ns
t_{AVLL}	Address Setup Time		20		ns
t_{LLAX}	Address Hold Time		30		ns
t_{PLDX}	$\overline{PSEN}$ to Output in High Z		0		ns
t_{PHDX}	Data Hold Time		0		ns
t_{PHDZ}	$\overline{PSEN}$ Disable to Output in High Z		0		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120		ns

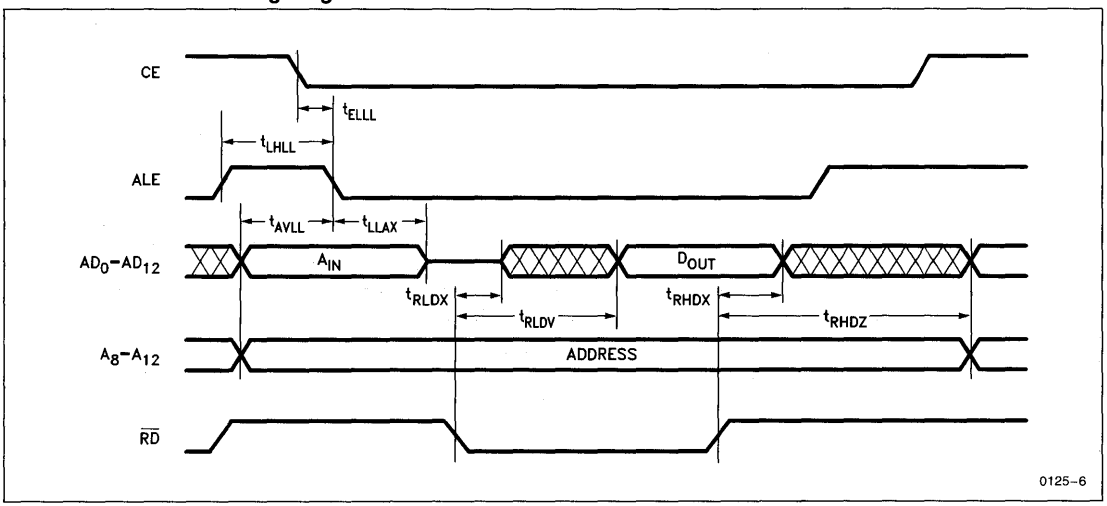
$\overline{PSEN}$ Controlled Read Timing Diagram



$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{ELLL}	Chip Enable Setup Time		7		ns
t_{LHLL}	ALE Pulse Width		80		ns
t_{AVLL}	Address Setup Time		20		ns
t_{LLAX}	Address Hold Time		30		ns
t_{RLDX}	$\overline{RD}$ to Output in High Z		0		ns
t_{RHDX}	Data Hold Time		0		ns
t_{RHDZ}	$\overline{RD}$ Disable to Output in High Z		0		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120		ns

$\overline{RD}$ Controlled Read Timing Diagram



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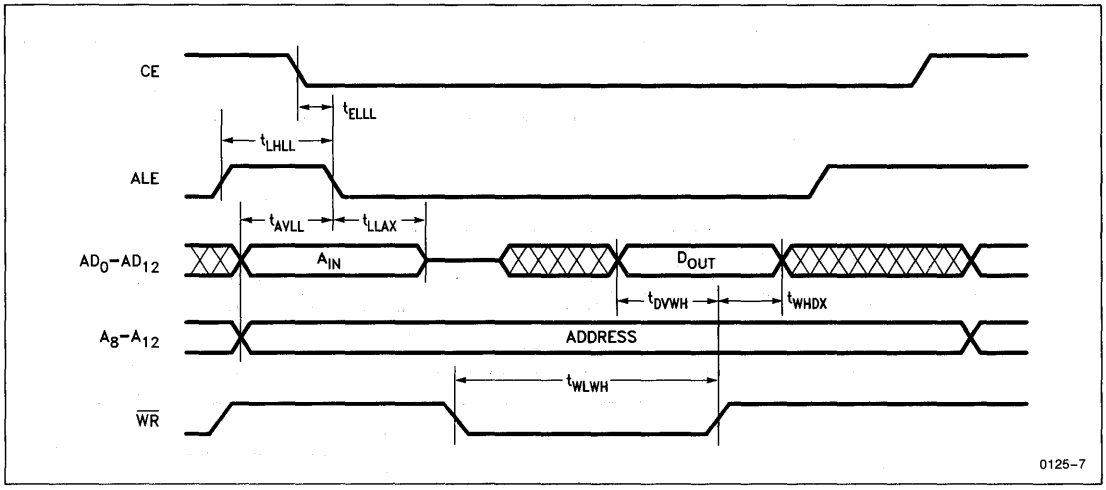
$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{ELLL}	Chip Enable Setup Time		7		ns
t_{LHLL}	ALE Pulse Width		80		ns
t_{AVLL}	Address Setup Time		20		ns
t_{LLAX}	Address Hold Time		30		ns
t_{DVWH}	Data Setup Time		50		ns
t_{WHDX}	Data Hold Time		20		ns
t_{WLWH}	$\overline{WR}$ Pulse Width		50		ns

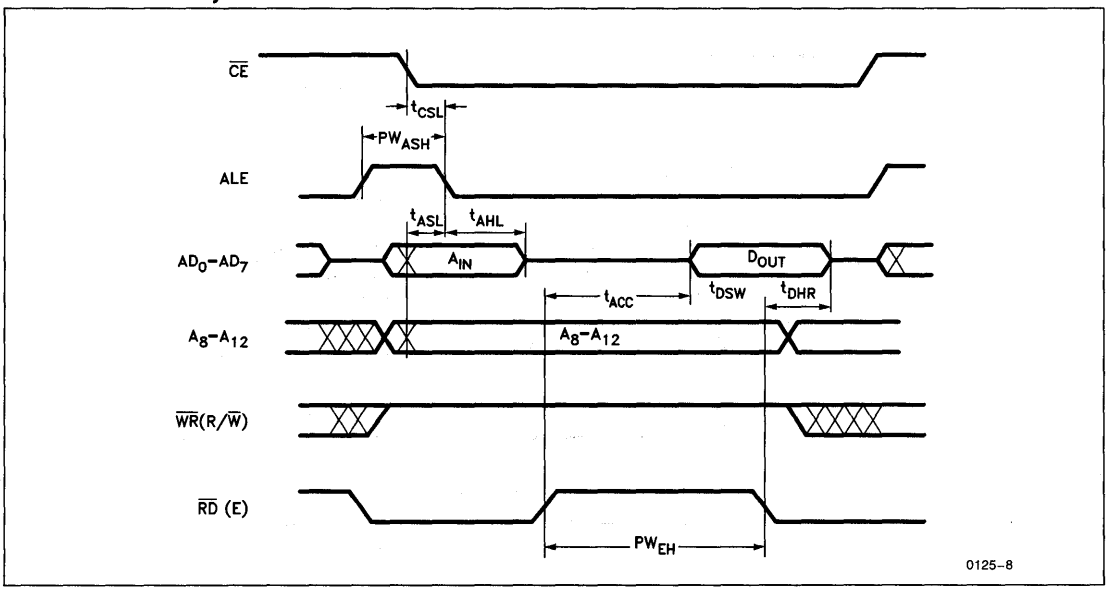
$\overline{WR}$ Controlled Write Timing Diagram



E Controlled Read Cycle

Symbol	Parameter	Min.	Typ.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width		75		ns
t_{ASL}	Address Setup Time		20		ns
t_{AHL}	Address Hold Time		15		ns
t_{ACC}	Data Access Time		120		ns
t_{DHR}	Data Hold Time		0		ns
t_{CSL}	$\overline{CE}$ Setup Time		7		ns
PW_{EH}	$\overline{E}$ Pulse Width		50		ns

E Controlled Read Cycle



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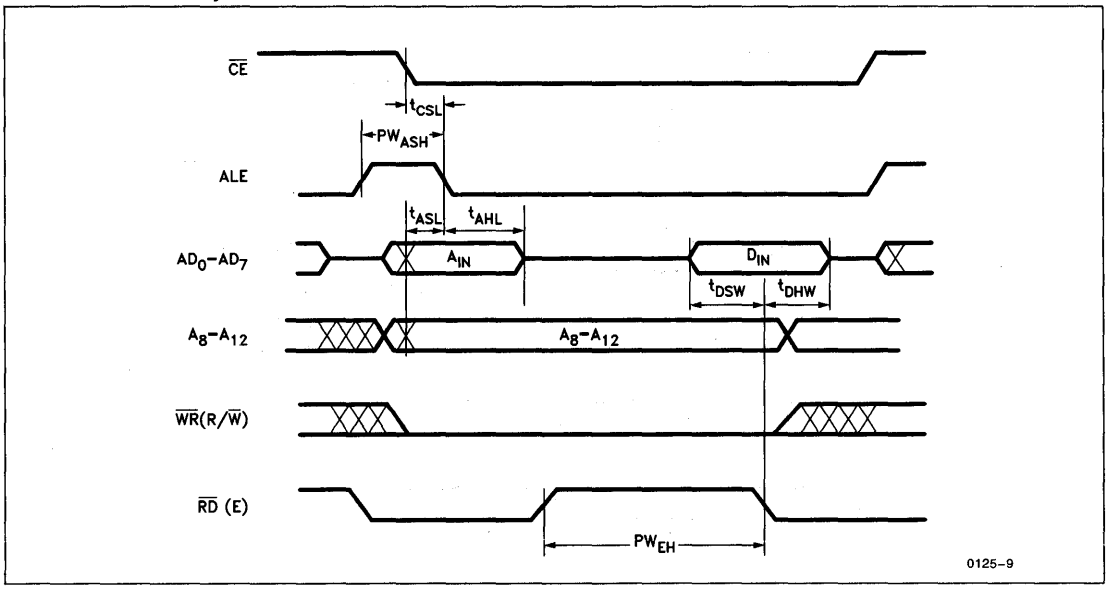
E Controlled Write Cycle

Symbol	Parameter	Min.	Typ.	Max.	Units
PW_{ASH}	Address Strobe Pulse Width		75		ns
t_{ASL}	Address Setup Time		20		ns
t_{AHL}	Address Hold Time		15		ns
t_{DSW}	Data Setup Time		50		ns
t_{DHW}	Data Hold Time		20		ns
t_{CSL}	$\overline{CE}$ Setup Time		7		ns
PW_{EH}	$\overline{E}$ Pulse Width		50		ns

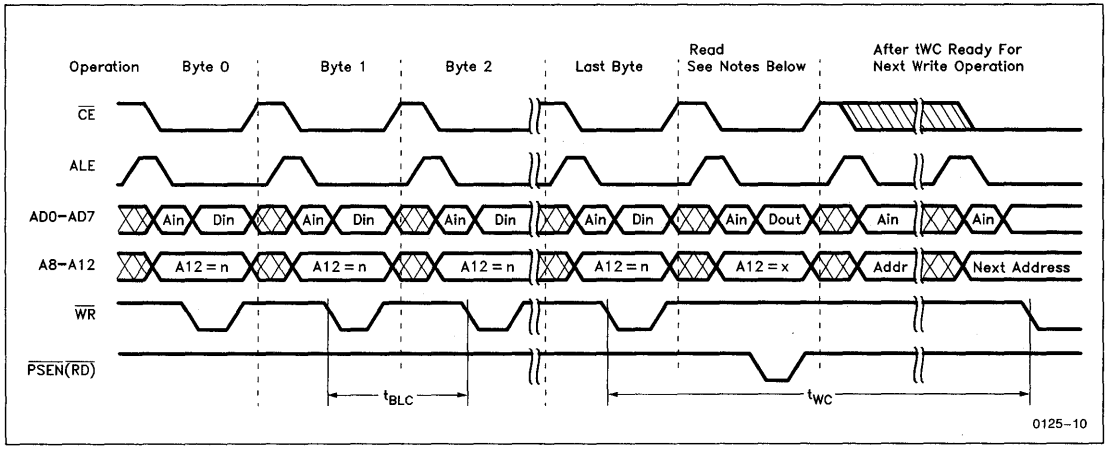
E Controlled Write Cycle



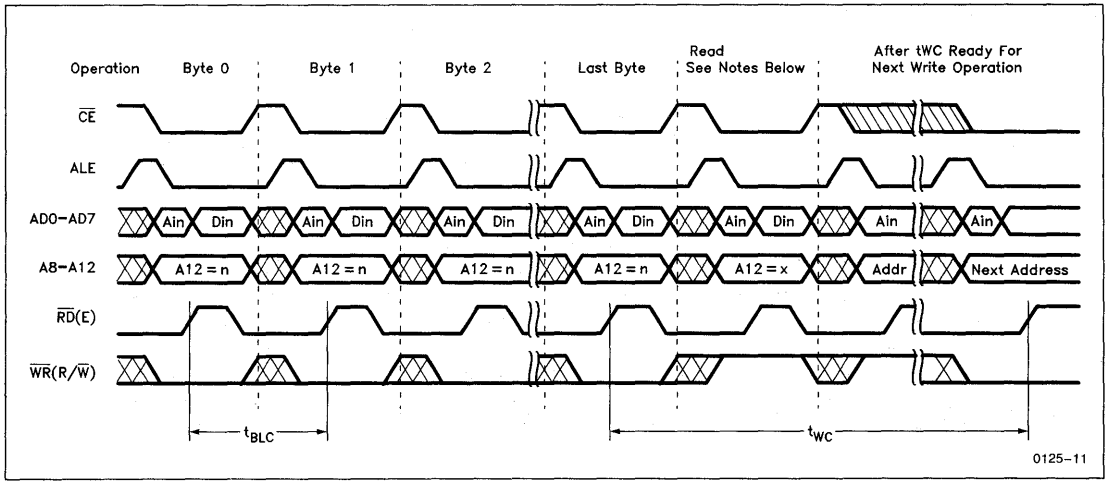
Page Write Operation

Regardless of the microcontroller employed, the X88C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C64. Each individual write within a page write operation must conform to the byte write timing requirements. The falling edge of WR (rising edge of E) starts a timer delaying the internal programming cycle 100 μs. Therefore, each successive write operation must begin within 100 μs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for WR Controlled Operation



Page Write Timing Sequence for E Controlled Operation



Notes: (1) For each successive write within a page write cycle A_6–A_{12} must be the same.

(2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible:

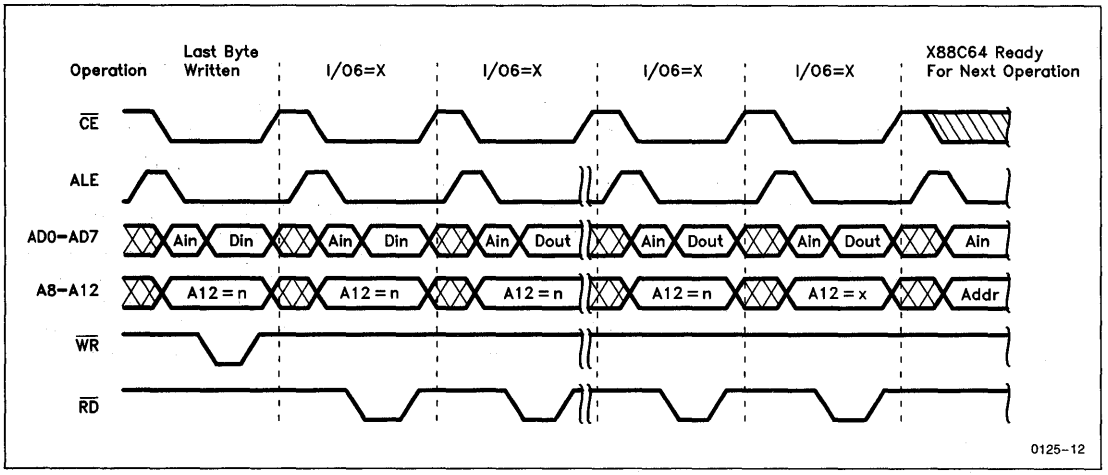
a. Reading from the same half plane being written (A_{12} of Read = A_{12} of Write) is effectively a Toggle Bit Polling operation.

b. Reading from the opposite half plane being written (A_{12} of Read ≠ A_{12} of Write) true data will be returned, facilitating the use of a single memory component as both program and data store.

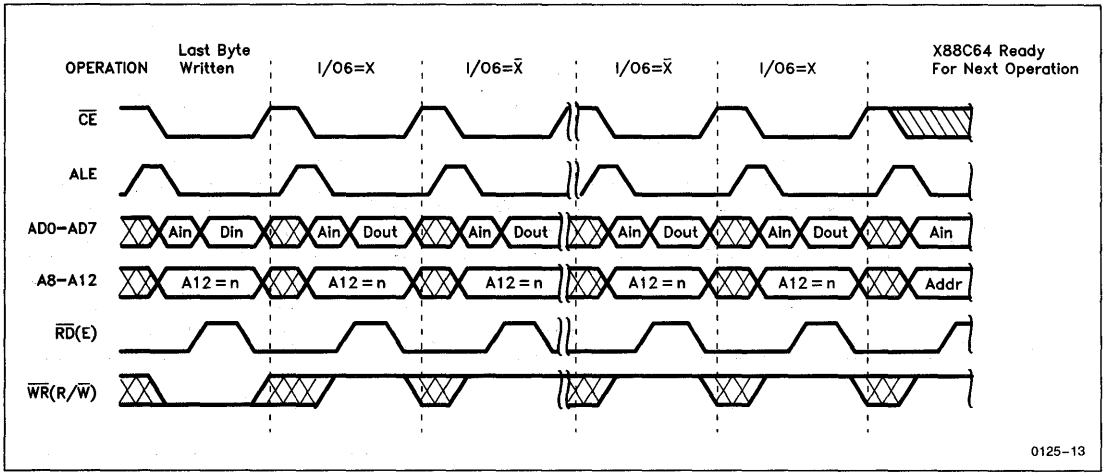
Toggle Bit Polling

Because the X88C64 typical write timing is less than the specified 10 ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that was written; that is, the state of A_{12} during write must match the state of A_{12} during polling.

Toggle Bit Polling $\overline{RD}/\overline{WR}$ Control



Toggle Bit Polling E and R/$\overline{W}$ Control



DATA PROTECTION

The X88C64 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E²PROMs and a new Block Protect write lock out protection providing a second level data security option.

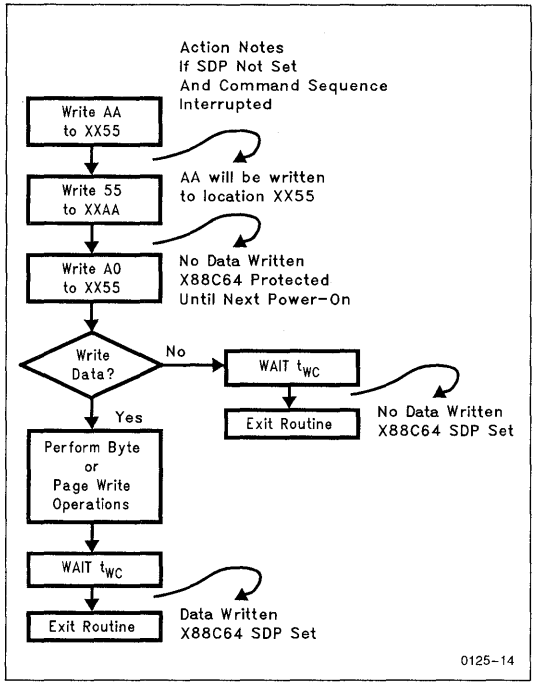
Software Data Protection

Software data protection (SDP) can be employed to protect the entire array against inadvertent writes during power-up/power-down operations. The X88C64 is shipped from the factory with SDP off. Enabling SDP requires the X88C64 to be written a three byte command sequence. This operation writes to an E²PROM bit, providing nonvolatile store of the user selected SDP condition. With SDP enabled, inadvertent attempts to write to the X88C64 will be blocked.

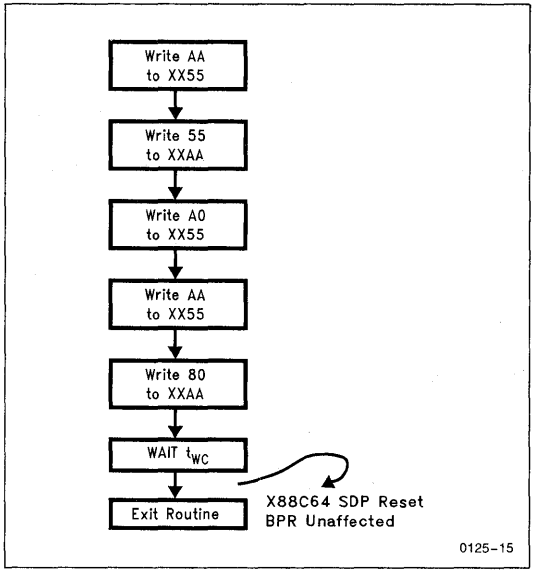
The system can still write data, but only when the write operation (page or byte) is preceded by the three byte command sequence. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

Once SDP is set on the X88C64 it can only be reset by issuing a five byte command sequence.

Setting SDP/Writing with SDP Set



Resetting SDP



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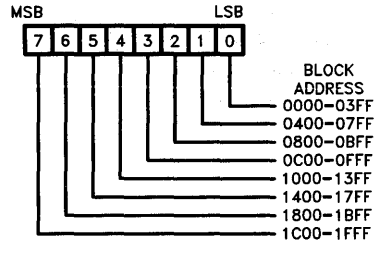
Block Protect Write Lockout

The X88C64 provides a second level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lock out writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lock out all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Store and another portion is used as Data Store.

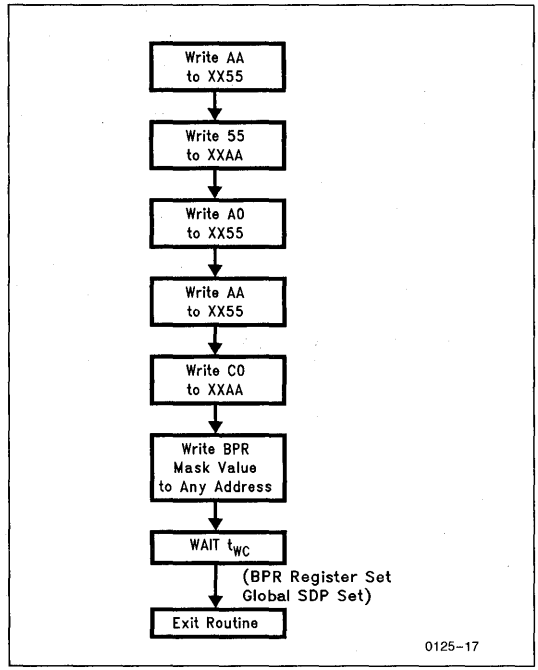
Setting write lockout is accomplished by writing a five byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written the user writes to the BPR selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements. It should be noted that accessing the BPR automatically sets the upper level SDP. If for some reason the user does not want SDP enabled, they may reset it using the normal reset command sequence. This will **not** affect the state of the BPR and any 1K x 8 blocks that were set to the write lockout state will remain in the write lockout state.

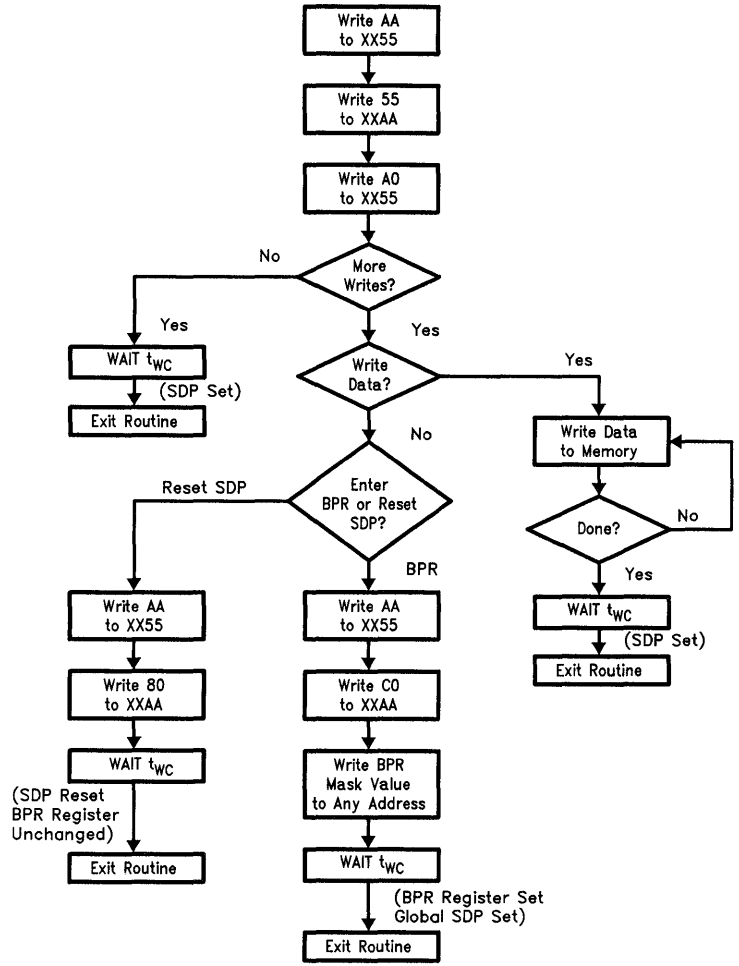
Block Protect Register Format



1 = Protect, 0 = Unprotect Block Specified

Setting BPR Command Sequence




Write AA to XX55
Write 55 to XXAA
Write A0 to XX55
More Writes?
No
Yes
WAIT t_{WC}
(SDP Set)
Exit Routine
Write Data?
Yes
No
Write Data to Memory
Done?
No
Yes
WAIT t_{WC}
(SDP Set)
Exit Routine
Enter BPR or Reset SDP?
Reset SDP
BPR
Write AA to XX55
Write 80 to XXAA
WAIT t_{WC}
(SDP Reset BPR Register Unchanged)
Exit Routine
Write AA to XX55
Write C0 to XXAA
Write BPR Mask Value to Any Address
WAIT t_{WC}
(BPR Register Set Global SDP Set)
Exit Routine
0125-18

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NOTES

XM28C010, XM28C010I 6-1
XM28C020, XM28C020I 6-15

NOVRAM* Data Sheets 1

Serial Products Data Sheets 2

E²PROM Data Sheets 3

E²POT™ Data Sheets 4

Microcontroller Peripheral Products 5

Memory Subsystems 6

1Megabit Module XM28C010 128K x 8 Bit

Electrically Erasable PROM

FEATURES

- **High Density 1Megabit (128K x 8) E²PROM Module**
- **Access Time of 250 ns at −55°C to +125°C**
- **Base Memory Component: Xicor CMOS X28C256**
- **JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package**
- **Pin Compatible with the X28C010 1Megabit Monolithic CMOS E²PROM**
- **Fast Write Cycle Times Supported by:**
  - **—Internal Program Cycle 10 ms Max.**
  - **—64-Byte Page**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Status Bit**
- **High Rel Module Available with:**
  - **—100% MIL-STD-883 Compliant Components**
  - **—100% Screening and MIL-STD-883 Processing of Modules**
- **Software Data Protection**

DESCRIPTION

The XM28C010 is a high density 1Megabit E²PROM comprised of four X28C256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28C010.

The XM28C010 is available in commercial, industrial and military temperature ranges. The military temperature range module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28C010 supports a 64-byte page write operation, this, combined with $\overline{\text{DATA}}$ Polling or Toggle Bit testing, effectively provides a 78 μs/byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C010 provides the same high endurance and data retention as the base memory components.

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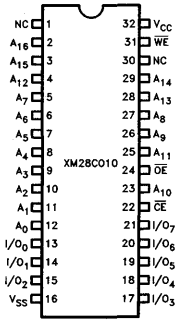
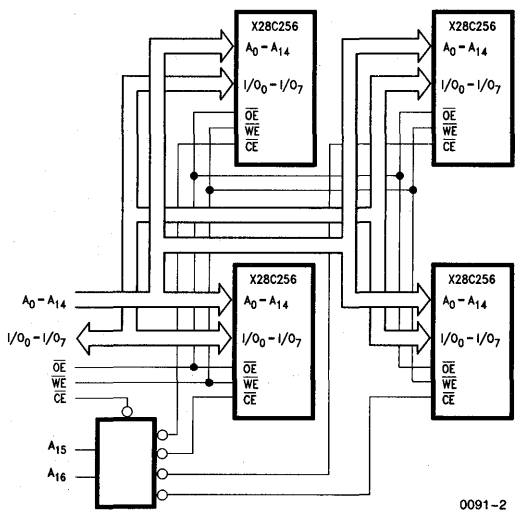
PIN CONFIGURATION



PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

XM28C010 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010M T_A = −55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		70	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)		15	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		800	μA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}	Input Low Voltage	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	100	μs
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	40	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	24	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.

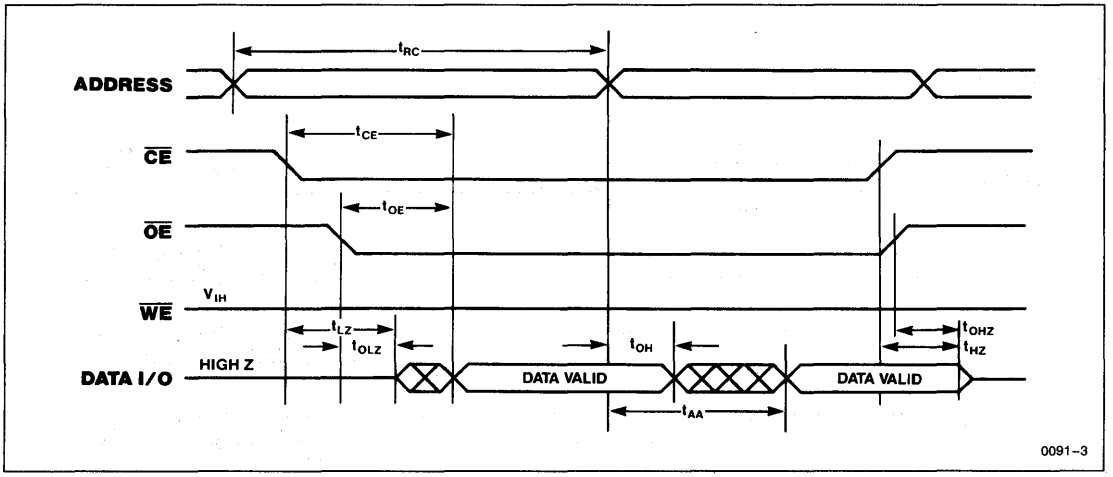
A.C. CHARACTERISTICS

XM28C010 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010M T_A = −55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	XM28C010-25		XM28C010		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		ns
t_{CE}	Chip Enable Access Time		250		300	ns
t_{AA}	Address Access Time		250		300	ns
t_{OE}	Output Enable Access Time		100		100	ns
t_{LZ}	$\overline{CE}$ Low to Active Output	0		0		ns
t_{OLZ}	$\overline{OE}$ Low to Active Output	0		0		ns
t_{HZ}(3)	$\overline{CE}$ High to High Z Output	0	100	0	100	ns
t_{OHZ}(3)	$\overline{OE}$ High to High Z Output	0	100	0	100	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Read Cycle

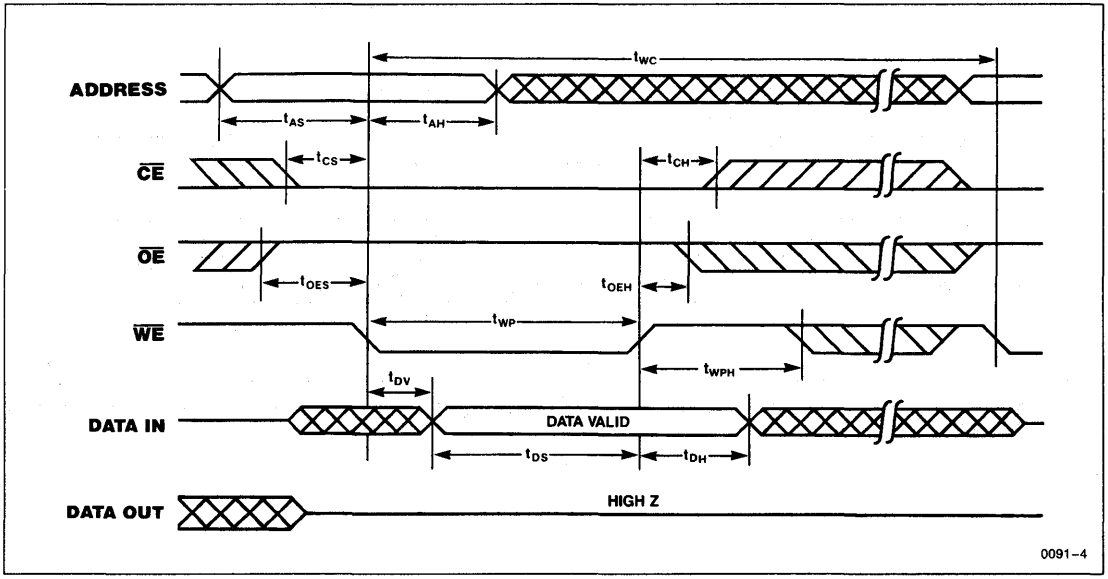


Note: (3) t_{HZ} and t_{OHZ} are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

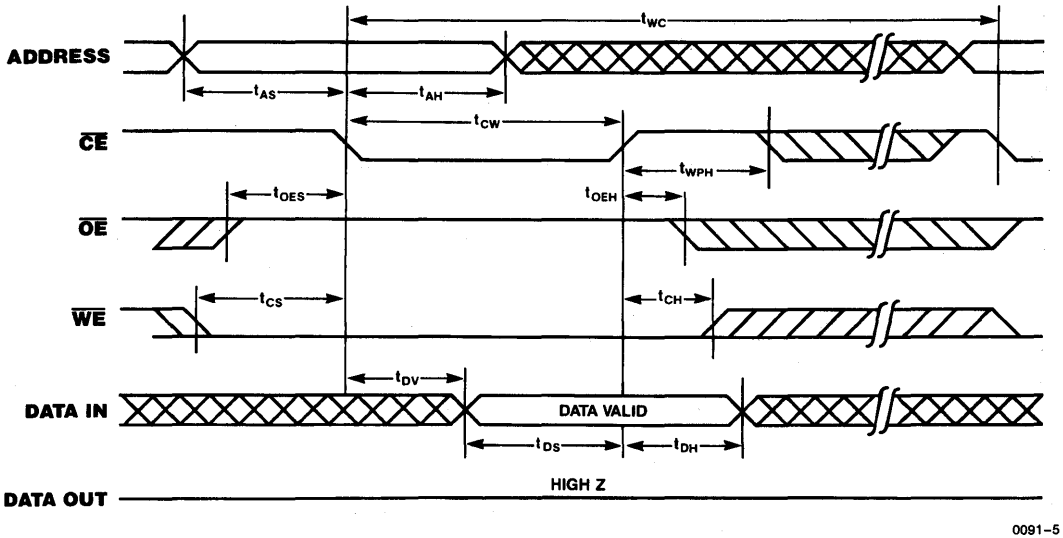
Symbol	Parameter	$\overline{WE}$ Controlled Write		$\overline{CE}$ Controlled Write(4)		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	150		175		ns
t_{CS}	Write Setup Time	25		0		ns
t_{CH}	Write Hold Time	0		25		ns
t_{CW}	$\overline{CE}$ Pulse Width	125		100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		35		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		125		ns
t_{WPH}	$\overline{WE}$ High Recovery	1		1		µs
t_{DV}	Data Valid		1		1	µs
t_{DS}	Data Setup	50		50		ns
t_{DH}	Data Hold	10		35		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

$\overline{WE}$ Controlled Write Cycle

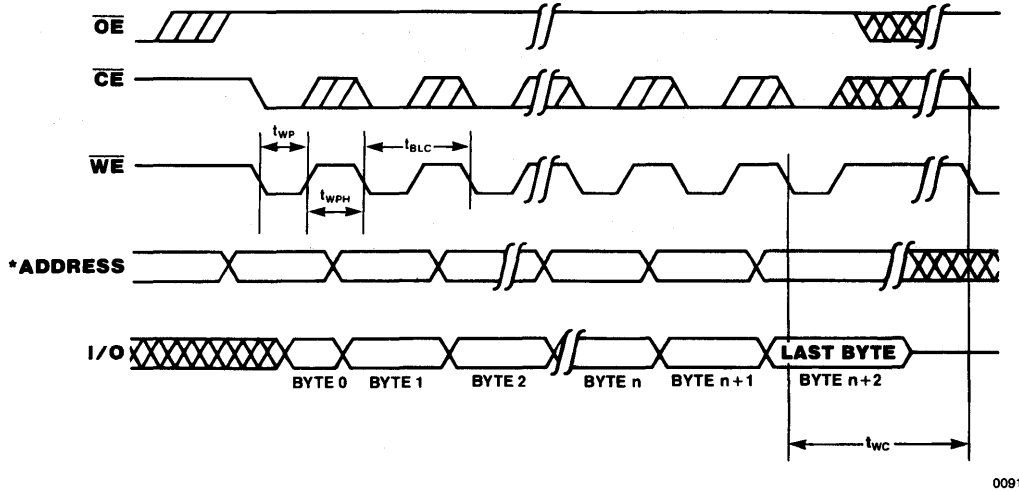


Note: (4) Due to the inclusion of the decoder IC on board the module the $\overline{WE}$ and $\overline{CE}$ write controlled timings will vary. When utilizing the $\overline{CE}$ controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a $\overline{WE}$ controlled write operation $\overline{CE}$ must be a minimum 125 ns to accommodate the additional setup time required.

$\overline{CE}$ Controlled Write Cycle



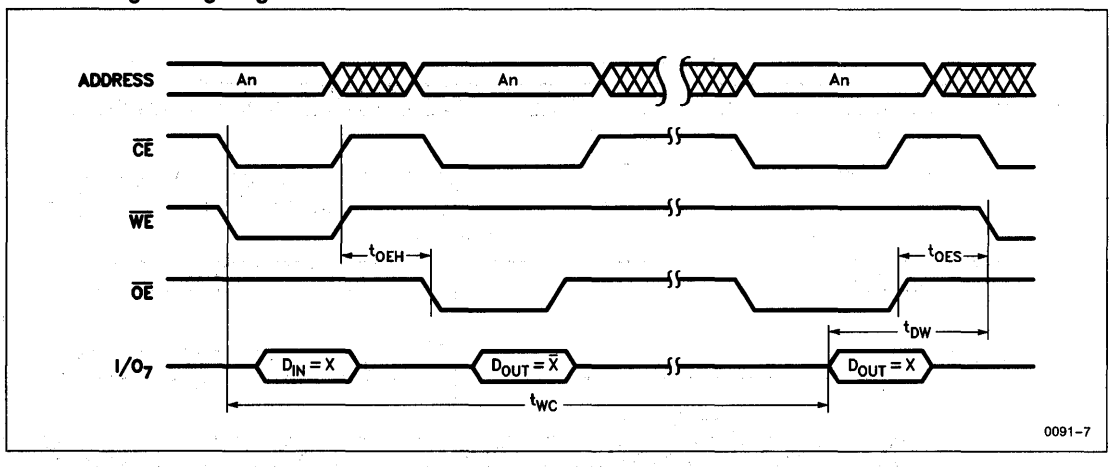
Page Write Cycle



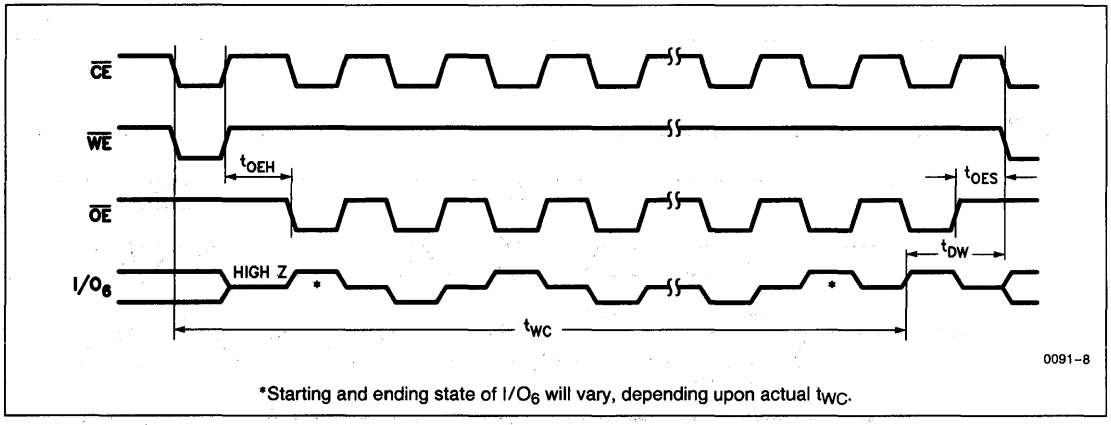
*For each successive write within the page write operation, A_6–A_{16} should be the same or writes to an unknown address could occur.

6

$\overline{\text{DATA}}$ Polling Timing Diagram



Toggle Bit Timing Diagram



*Starting and ending state of I/O_6 will vary, depending upon actual t_{WC}.

PIN DESCRIPTIONS

Addresses (A_0–A_{16})
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)
The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced (see Note 4).

Output Enable ($\overline{OE}$)
The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)
Data is written to or read from the XM28C010 through the I/O pins.

Write Enable ($\overline{WE}$)
The Write Enable input controls the writing of data to the XM28C010.

DEVICE OPERATION

Read
Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

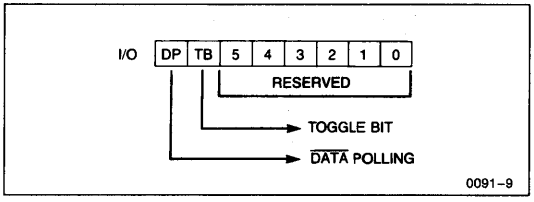
Write
Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The XM28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

Page Write Operation
The page write feature of the XM28C010 allows the entire memory to be written in 10 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the XM28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits
The XM28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)
The XM28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the XM28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the XM28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)
The XM28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2a: $\overline{DATA}$ Polling Bus Sequence

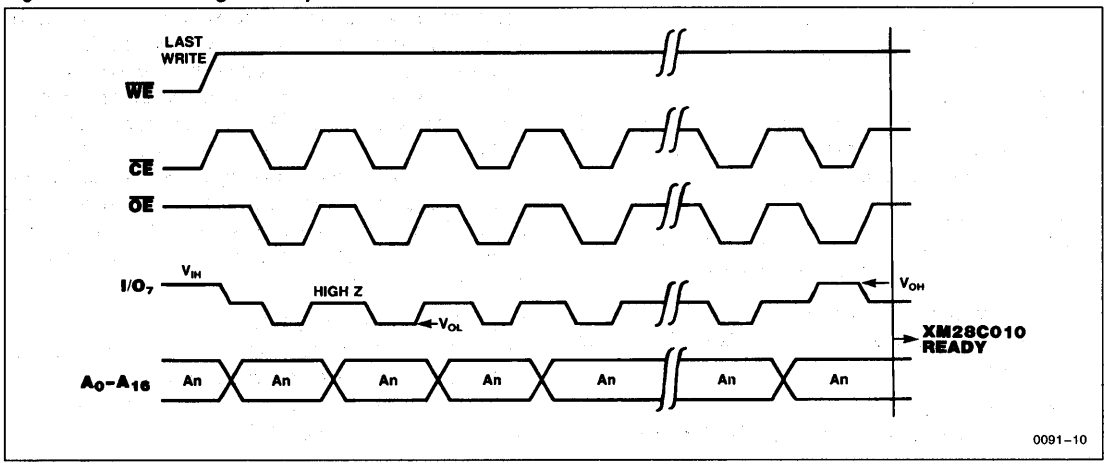
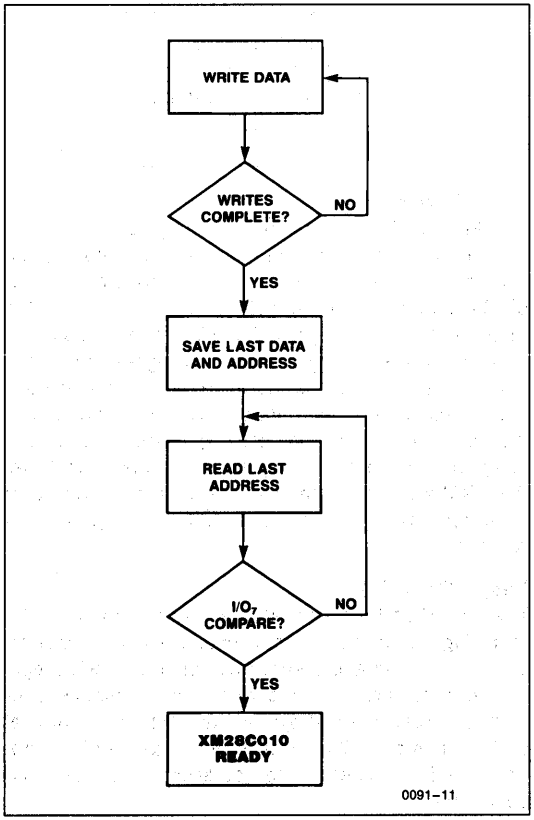


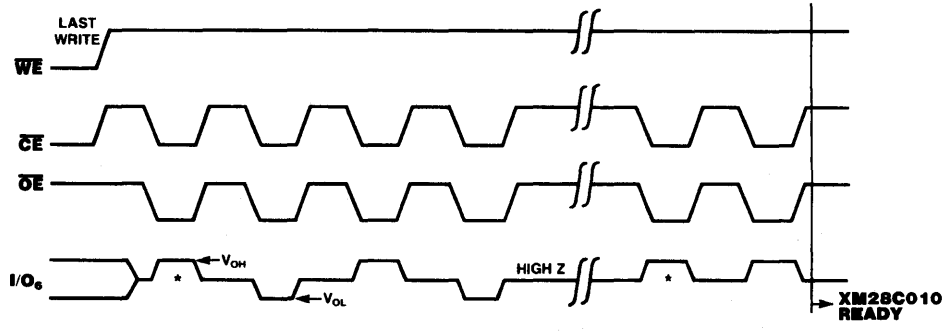
Figure 2b: $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the XM28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

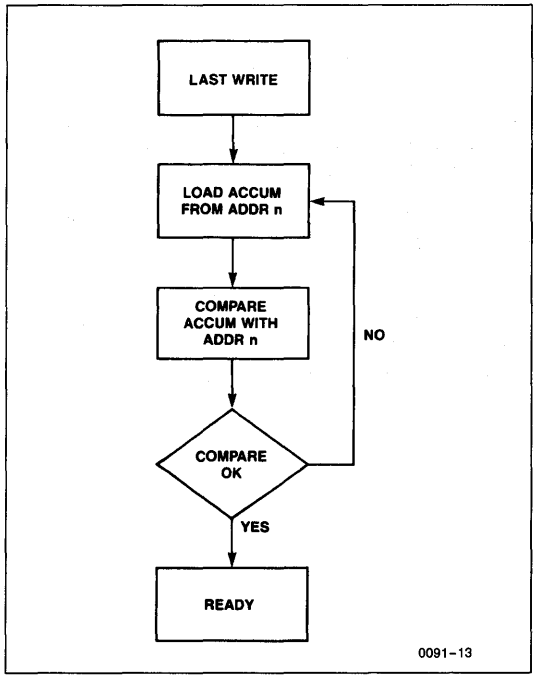
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple XM28C010 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

6

HARDWARE DATA PROTECTION

The XM28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding $\overline{OE}$ LOW will prevent an inadvertent write cycle during power-on and power-off.

SOFTWARE DATA PROTECTION

The XM28C010 does provide the Software Data Protection (SDP) feature. Because the module is comprised of four discrete X28C256 LCCs, the algorithm will differ from the algorithm employed for the monolithic 1Megabit X28C010.

The module is shipped from Xicor with the Software Data Protect NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once V_{CC} is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described below.

SOFTWARE COMMAND SEQUENCE

A_{15} and A_{16} are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

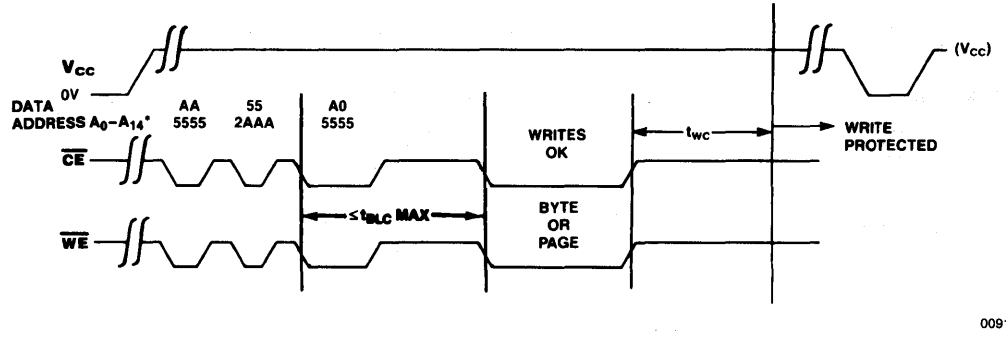
Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 4a and 4b. Because this involves writing to a nonvolatile bit the device will become protected after t_{WC} has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 5a and 5b. This is a nonvolatile operation, and the host will have to wait a minimum t_{WC} before attempting to write new data.

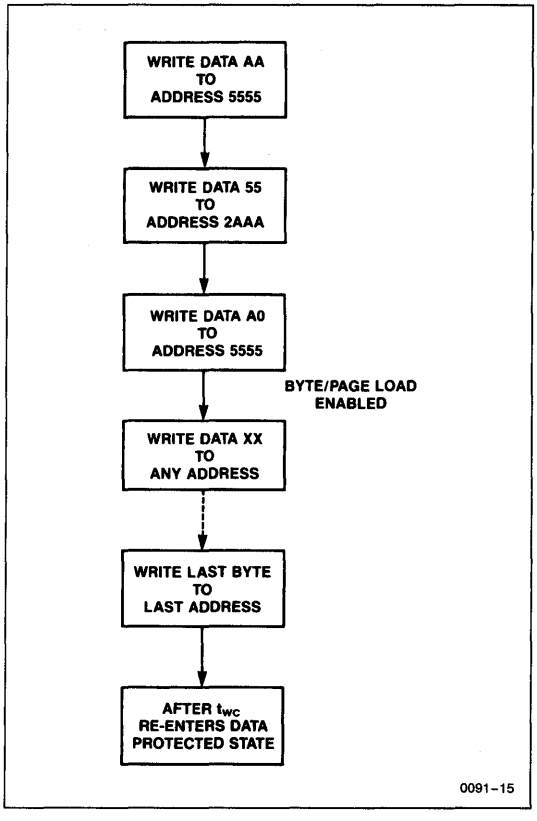
SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write



*A_{15} & A_{16} select one of four devices on the module.

Figure 4b: Write Sequence for Software Data Protection

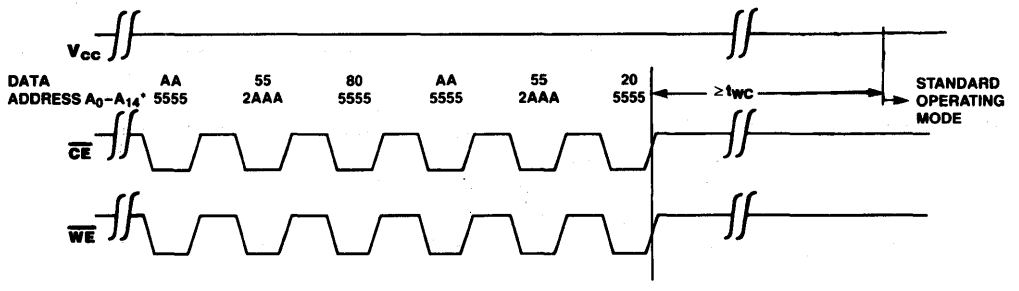


Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

6

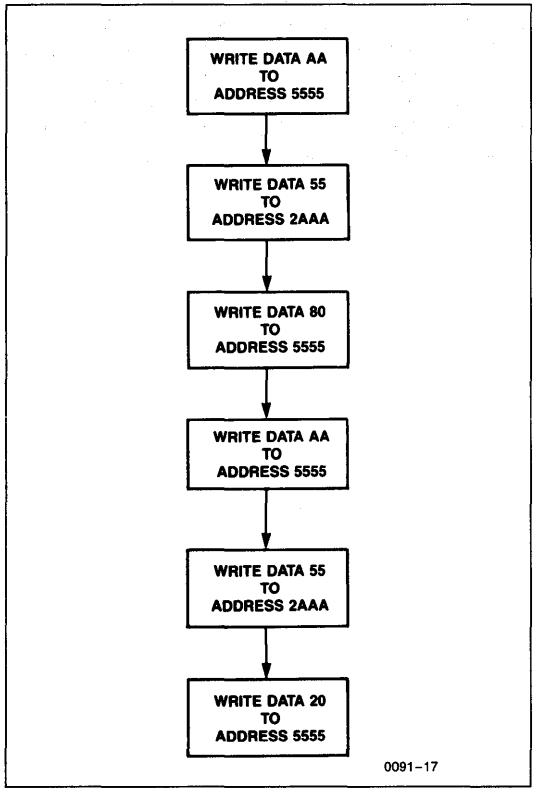
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence



*A_{15} & A_{16} select one of four devices on the module.

Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the device will be in standard operating mode.

SYSTEM CONSIDERATIONS

Because the XM28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

6

NOTES

FACT SHEET

2Megabit Module XM28C020 256K x 8 Bit

Electrically Erasable PROM

FEATURES

- **High Density 2Megabit (256K x 8) E²PROM Module**
- **Access Time of 200 ns at −40°C to +85°C**
- **Base Memory Component: Xicor CMOS X28C513**
- **JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package**
- **Fast Write Cycle Times Supported by:**
  - **—Internal Program Cycle 10 ms Max.**
  - **—128-Byte Page**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Status Bit**
- **Software Data Protection**

DESCRIPTION

The XM28C020 is a high density 2Megabit E²PROM comprised of four X28C513 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C020 is configured 256K x 8 bit.

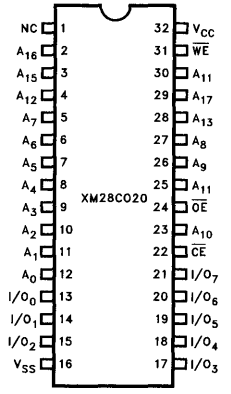
The XM28C020 is available in commercial and industrial temperature ranges.

The XM28C020 supports a 128-byte page write operation. This, combined with $\overline{\text{DATA}}$ Polling or Toggle Bit testing, effectively provides a 40 μs/byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C020 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C020 provides the same high endurance and data retention as the base memory components.

PIN CONFIGURATION

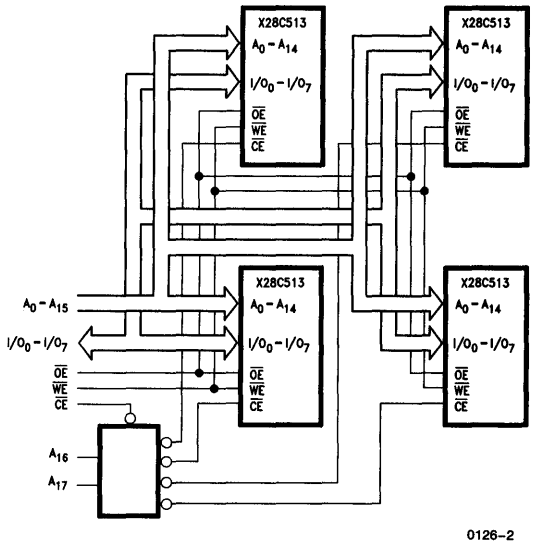


0126-1

PIN NAMES

A_0–A_{17}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



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NOTES

Die Products 7-1

Die Products

FEATURES

- **High Performance Advanced NMOS Technology**
- **0°C to 70°C Operating Temperature**
- **100 Year Data Retention**
- **95% Yield Excluding Assembly Related Losses**
- **Standard Thickness Between 20 to 22 mils**
- **Commercial Data Sheet Parameters (except input levels)**
- **Die Inspected to 883C 2010.7 Condition B**

DESCRIPTION

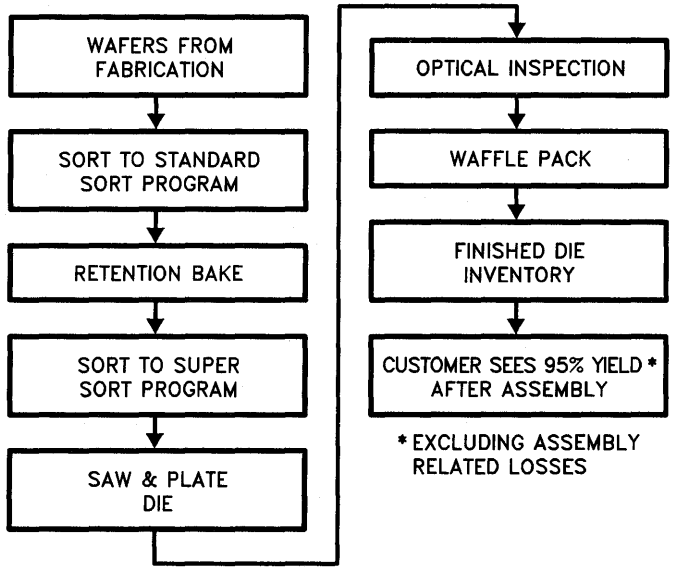
Xicor die products are fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories, they are 5V only devices.

Xicor die products are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

Products to be shipped in die form follow the flow shown below. This insures a 95% yield (excluding assembly related losses) to the commercial data sheet with the access times per the Die Products Reference Guide. All A.C. parameters and D.C. parameters except input and output voltages are guaranteed.

Bonding diagrams, die size and other information required for use of die can be obtained from your local Xicor sales representative.

TEST FLOW



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DIE PRODUCTS REFERENCE GUIDE

E²PROMs

Part Number	Organization	Page Size (Bytes)	Access Time (ns)	Power Requirements (mA)	
				Active (Max.)	Standby (Max.)
X2804AH	512 x 8	N/A	450	80	50
X2816BH	2K x 8	16	450	120	60
X2864AH	8K x 8	16	450	140	60
X2864BH	8K x 8	32	200	150	80

NOVRAMs

Part Number	Organization	Access Time (ns)	Store Cycles	Power Requirements (mA)	
				Active (Max.)	Standby (Max.)
X2004H	512 x 8	300	100,000	100	55

Serial E²PROMs

Part Number	Organization	Page Size (Bytes)	Clock Frequency	Power Requirements (mA)	
				Active (Max.)	Standby (Max.)
X2402H	256 x 8	8	100 KHz	30	25
X2404H	512 x 8	8	100 KHz	30	25

Serial NOVRAMs

Part Number	Organization	Clock Frequency	Store Cycles	Power Requirements (mA)		
				Active	Standby	Sleep
X2444H	16 x 16	1 MHz	100,000	15	10	7

Digital Potentiometers

Part Number	End to End Resistance	Maximum Voltage (V_H, V_L)	Power Requirements (mA)
X9103H	10 KΩ	±5V	35
X9503H	50 KΩ	±5V	35
X9104H	100 KΩ	±5V	35

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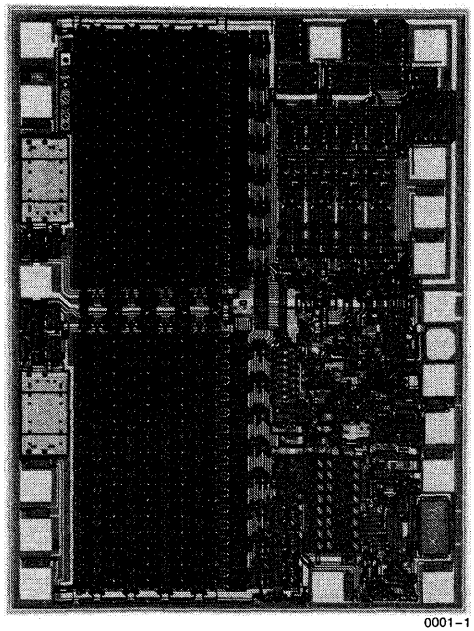

0001-1

XICOR NOVRAMs* EASIER THAN EVER TO USE

By Applications Staff

8

*NOVRAM is Xicor's nonvolatile static RAM device.

Introduction

The purpose of this application note is to take the user through the internal operation of NOVRAMs as well as their external operation. These devices are finding their way into many diverse applications due to their ease of use. The major features of the XICOR family of NOVRAMs are 1) only 5 volts is required for all operations including programming, 2) only TTL signals are required and 3) all pulse widths are short (< 450 ns).

Basically a NOVRAM is a memory device that has a static RAM overlaid with an EEPROM (Electrically Erasable Programmable ROM). The operation of the RAM is identical with other popular static RAMs such as the 2102A and the 2114. Figure 1 shows the block diagram of the XICOR NOVRAM family. NOVRAMs have $\overline{CS}$ and $\overline{WE}$ pins in common with their standard static RAM cousins but also have two additional control pins: $\overline{STORE}$ and $\overline{RECALL}$. The $\overline{STORE}$ and $\overline{RECALL}$ pins control movement of data between the RAM and the EEPROM.

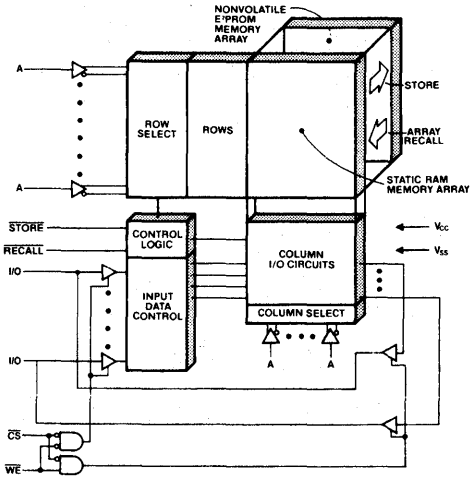

Figure 1) Block diagram of the XICOR NOVRAM family.

The $\overline{STORE}$ pin is used to transfer the contents of the RAM to the EEPROM in a single operation. The entire contents of the RAM are transferred with one STORE operation. After a STORE operation is completed the original data is still in the RAM as well as the EEPROM.

The $\overline{RECALL}$ pin is used to transfer the contents of the EEPROM back to the RAM. When this is done, whatever data were in the RAM prior to the RECALL operation are totally replaced by the contents of the EEPROM. The STORE and RECALL operations function on the entire contents of the memory and not on a word by word basis. After either operation the contents of both the RAM and the EEPROM will be the same.

This may seem too good to be true; however, with XICOR's family of NOVRAMs the life of the systems designer is made even easier. Only a single five volt power supply is required for all operations including the STORE and RECALL operations. All addresses, data lines and control pins are TTL compatible and all pulse widths are short enough that most microprocessors do not require wait states. There are no high voltages or long pulse widths required which will inhibit the designer from designing a system with clean operation.

Technology

The XICOR NOVRAM stores its nonvolatile data during periods of power off by the absence or presence of charges on floating polysilicon gates. This is the same structure that is widely used in UV-EPROMS. The floating gate is an island of polysilicon surrounded by oxides with thicknesses of about 800 A°. Charge can be injected or removed from the floating gate by applying electric fields of sufficient strength to cause electron tunneling through the oxides. At normal field strengths the charges are permanently trapped on the floating gate even when power is removed.

The XICOR family of NOVRAMs uses three layers of polysilicon; the second layer is the floating gate. This structure employs a phenomenon known as Fowler-Nordheim tunneling. This form of tunneling is described in Vol. 40 No. 1 (Jan. 1969, pg. 278) of the Journal of Applied Physics and Vol. 27 No. 9 (Nov. 1975, pg. 505) of the Applied Physics Letters. In XICOR NOVRAMs this tunneling is enhanced by the use of textured polysilicon surfaces to generate higher field strengths at the surface to enhance electron injection into the oxide. The alternative to field enhancement by textured surfaces is to use ultrathin oxide layers in order to conduct the charge. The use by XICOR of standard oxide thickness gives XICOR a very manufacturable product, thus ensuring its low cost and volume delivery.

Figure 2. shows the circuit of the NOVRAM cell containing a conventional 6 transistor static RAM cell and a floating gate EEPROM cell with 2 additional transistors to control the action of data transfer. The floating gate (POLY 2) is connected to the rest of the circuit only through capacitance. Electrons are moved to the floating gate by tunneling from POLY 1 to POLY 2 and removed by tunneling from POLY 2 to POLY 3.

The capacitance ratios are the key to the operation of the transfer of data from RAM to EEPROM. If node

N1 is LOW, transistor Q7 is turned OFF. This allows the junction between CC2 and CC3 to float. Since the combined capacitance of CC2 and CC3 are larger than CP the floating gate follows the Internal Store Voltage node. When the voltage on the floating gate is high enough electrons are tunneled from POLY 1 to POLY 2 and the floating gate is negatively charged.

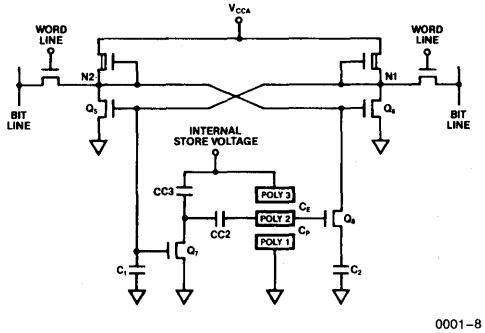

Figure 2) Circuit diagram of a NOVRAM cell.

If node N1 is HIGH, transistor Q7 is turned ON which grounds the junction between CC2 and CC3. Since CC2 is larger than CE, CC2 holds the floating gate near ground when the Internal Store Voltage node is pulled HIGH. This creates a sufficient field between POLY 2 and POLY 3 to tunnel electrons away from the floating gate leaving it with a positive charge.

The RECALL operation also takes advantage of capacitance ratios. The value of C2 in Figure 2 is larger than that of C1. When the external RECALL command is received, the internal power supply, VCCA, is first pulled LOW to equalize the voltage on N1 and N2. When the internal power node is allowed to rise, the node which has the lighter loading will rise more rapidly and the gain of the flip-flop will cause it to latch HIGH and the opposite node to latch LOW. If the floating gate has a positive charge C2, is connected to N2 through Q8 and N2 will latch LOW. If the floating gate has a negative charge Q8, is turned OFF and N1 will have the heavier loading.

The Xicor NOVRAM Family

XICOR's family of NOVRAMs contains three members with identical operating characteristics. The three parts offer the designer a choice of memory organization. The X2201A, X2210 andX2212 are organized 1024 x 1, 64 x 4 and 256 x 4 respectively. All three devices are packaged in 18 pin DIPs with 300 mil centers. Figure 3 shows the pin configuration of the three different NOVRAMs.

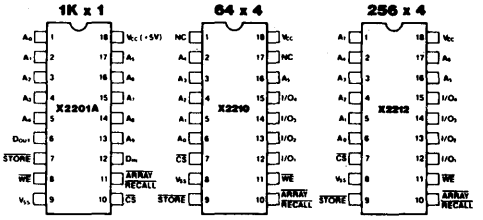

Figure 3) Pin configuration of the XICOR NOVRAM family.

The only functional difference between the three devices is that the X2201A has separate Data I/O lines while the two 4 bit wide parts have common I/O. Additionally, the X2210 and the X2212 are pin compatible. The two unused pins on the X2210 are used for the two higher order addresses on the X2212. The control pins $\overline{STORE}$, $\overline{RECALL}$, $\overline{CS}$ and $\overline{WE}$ operate identically on all three parts.

Write Operation

The WRITE operation is initiated by applying valid addresses followed by both $\overline{CS}$ and $\overline{WE}$ going LOW. On the 300ns version access time version, at least one of these two signals must remain HIGH until the addresses are valid. $\overline{CS}$ and $\overline{WE}$ must remain LOW simultaneously for 100ns.

An easy way to look at this is to consider the internal write command as the simultaneous LOW of $\overline{CS}$ and $\overline{WE}$. The internal write command is started by the last edge down and terminated by the first edge up. Valid addresses must overlap this internal write command. Data must be referenced to the first positive edge of $\overline{CS}$ or $\overline{WE}$. The timing required for writing to the RAM is shown in Figure 4.

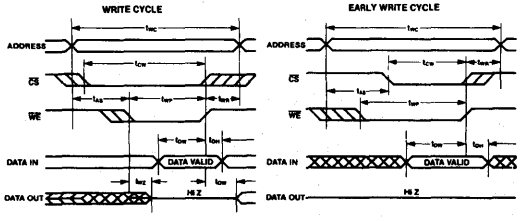

Figure 4) Timing diagram for Writing to the RAM.

0001-3

Read Operation

The READ operation is the easiest of the four operations performed by the NOVRAM. In the case of the 300ns access time version, data will be valid at the outputs 300ns after valid addresses or 200ns after $\overline{CS}$ goes LOW, whichever is later.

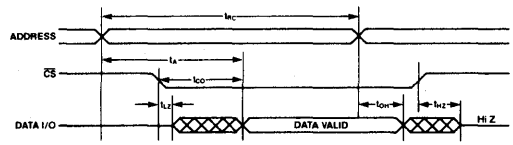

Figure 5) Timing diagram for Reading from the RAM.

Store Operation

The STORE operation is initiated by the application of an active LOW TTL pulse of 100ns or greater on the $\overline{STORE}$ pin. As long as the power supply remains within its specification for 10ms after the beginning of the STORE pulse the contents of the RAM will have been transferred to the EEPROM in total. The STORE operation cannot be terminated once initiated except by removing the power supply. This can not be counted upon to rapidly terminate the STORE operation since the user cannot determine how far the STORE operation the device has progressed. Additionally, if the power supply drops below the specification during the 10ms the integrity of the STORE operation is not assured. Figure 6 shows the timing diagram for transferring data from the RAM to the EEPROM.

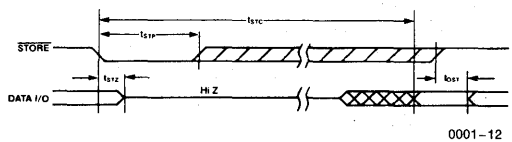

Figure 6) Timing diagram for the STORE operation where data is transferred from the RAM to the EEPROM.

The STORE operation takes precedence over all other operations except the RECALL operation. If the RECALL operation has begun, any STORE command is ignored as long as the $\overline{RECALL}$ pin remains LOW. Once the STORE operation has started, taking the $\overline{RECALL}$ pin LOW has no effect and the STORE operation will be completed. If a READ or WRITE cycle is in progress when a STORE command is received, that cycle is terminated. The data in the selected RAM address during an interrupted WRITE cycle would be indeterminate.

During the 10ms of the STORE operation the NOVRAM should not be accessed for any other operation as it would not be known if the internal STORE operation was completed or not. If the internal STORE operation was completed before the 10ms and another operation command was entered, that command would be executed. However, if the internal STORE operation was not completed and another operation command was received, the later command would be ignored. During the STORE operation the outputs of the NOVRAM are in the floating state.

Recall Operation

The RECALL operation is initiated by the application of an active LOW TTL pulse of 450ns or greater on the $\overline{RECALL}$ pin. The positive going edge of this pulse determines when it is possible to read data from the RAM. Valid data from the RAM can be viewed on the outputs of the NOVRAM 750ns after the rising edge of $\overline{RECALL}$ or 300ns after application of valid addresses, whichever comes latest. FIGURE 7 shows the timing requirements for transferring data from the EEPROM to the RAM.

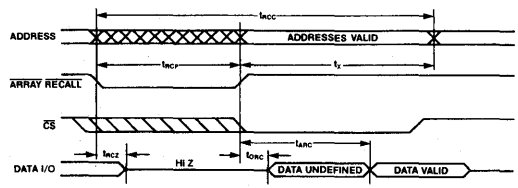

Figure 7) Timing diagram for the RECALL operation.

The RECALL operation takes precedence over all other operations. RECALL will terminate a READ or WRITE cycle if applied in the middle of either cycle. The RECALL operation can take precedence over the STORE operation only if the RECALL command was received prior to the STORE command.

Hooking up the NOVRAM

Now that the basics of the four NOVRAM operations have been described, we may discuss using these unique parts in a system. Let's first discuss a system in in which we connect the NOVRAMs to a 6502. We'll assume that the system powers up and down cleanly. The problem of systems where this does not occur will be dealt with later.

0001-4

The 6502 microprocessor uses memory space for I/O functions. The design uses one set of addresses for the READ and WRITE operations and other blocks of addresses to initiate the STORE and RECALL operations. An APPLE II* computer was used as the 6502 computer because it has address space already decoded for I/O functions and convenient card slots to communicate with these decoder outputs.

The RAM was placed in the address space starting at HEX address $C800 by connecting pin 20 on the APPLE II peripheral connector to the $\overline{CS}$ on the NOVRAM. This pin is activated when any of the 2048 bytes starting at $C800 are accessed. Peripheral slot 2 was selected for the NOVRAM design. On slot 2 pin 41 is activated whenever the 16 bytes located at HEX address $C0A0 are accessed. This address space is sent only to slot 2 and was tied to the $\overline{STORE}$ pin on the NOVRAM. PIN 1 also has a unique address space for slot 2 and was tied to the RECALL pin. This space is the 256 bytes starting at HEX address $C200.

Figure 8 shows the connections of the card to be plugged into peripheral card slot 2. Reading and writing are accomplished from the BASIC programming language by PEEK and POKE instructions to HEX addresses starting at $C800. The STORE operation is called by either a PEEK or a POKE instruction to any of the 16 addresses starting at $C0A0. $\overline{RECALL}$ is initiated by accessing any of the 256 bytes starting at $C200.

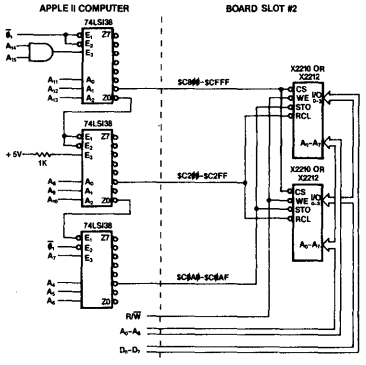

Figure 8) Connections for operating the NOVRAM on the I/O Bus of an APPLE II computer.

The APPLESOFT* program in Table 1 demonstrates how a NOVRAM can be accessed easily. The statement 210 is a Write operation to HEX address $C200 while statement 310 is a Write to HEX address $C0A0. The $\overline{CS}$ pin is activated with statement 430 and statement 580 respectively. This program was written for the X2210 but it could be easily modified for the X2212 or even eight X2201s.

```
5  TEXT : HOME
10 A$ = "#1 WELCOME TO THE WORLD'
    S EASIEST TO USENONVOLATILE
    STATIC RAM!!"
20 B$ = "#2 ONLY A SINGLE 5 VOLT
    POWER SUPPLY IS REQUIRED FOR
    OPERATIONS!"
30 C$ = "#3 ALL INPUTS AND OUTPUT
    S REQUIRE ONLY TTL INTERFAC
    E SIGNALS!!!"
40 F$ = "#4 ALL TIMING SIGNALS AR
    E MICROPROCESSORCOMPATIBLE-N
    O STRETCHING!"
50 G$ = "#5 3 SIZES AVAILABLE: (X2
    201)1024X4;    (X2212)256X4
    ;(X2210)64X4"
60  VTAB 5: HTAB 11: PRINT "E1COR
    P X2210 DEMO"
75  PRINT : PRINT : HTAB 5: PRINT
    "1=RECALL": HTAB 25: PRINT
    "3=READ"
80  PRINT : HTAB 5: PRINT "2=STOR
    E";: HTAB 25: PRINT "4=WRITE
    "
85  PRINT : HTAB 17: PRINT "5=EXI
    T"
90  VTAB 15: HTAB 12: INPUT "SELE
    CT ONE?";A
100  IF A < 1 OR A > 5 THEN  HOME
     : VTAB 5: HTAB 5: PRINT "ONE
    Y 1-5 ALLOWED---TRY AGAIN": GOTO
     75
110  ON A GOTO 200,300,400,500,60
    0
200  REM  ######################
201  REM  # RECALL SUBROUTINE #
202  REM  ######################
210  POKE  - 15872,0
215  HOME : VTAB 5: HTAB 14
216  PRINT "RECALL COMPLETE"
218  FOR I = 1 TO 1000: NEXT I
220  HOME : GOTO 60
300  REM  ######################
301  REM  # STORE SUBROUTINE #
302  REM  ######################
310  POKE  - 16204,0
315  HOME : VTAB 5: HTAB 14: PRINT
    "STORE COMPLETE"
320  FOR I = 1 TO 1000: NEXT I
325  HOME : GOTO 60
400  REM  ######################
401  REM  # READ SUBROUTINE #
402  REM  ######################
422  HOME
423  VTAB 5: HTAB 12: PRINT "RESU
    LTS FROM RAM": PRINT : PRINT
425  FOR I = 1 TO 64
430  PRINT  CHR$ ( PEEK ( - 14336
     + I));
435  NEXT I
440  FOR I = 1 TO 5000: NEXT I
445  HOME : GOTO 60
500  REM  ######################
501  REM  # WRITE SUBROUTINE #
502  REM  ######################
505  HOME : VTAB 5: HTAB 8: PRINT
    "PRESELECTED MESSAGES (1-5)"
    : PRINT : PRINT
515  PRINT : PRINT : HTAB 4: PRINT
    "ENTER MESSAGE FROM KEYBOARD
    (6)"
520  PRINT : PRINT : HTAB 11: INPUT
    "SELECT ONE (1-6)?";A
525  ON A GOTO 531,532,533,534,53
    5,540
531  D$ = A$: GOTO 540
532  D$ = B$: GOTO 540
533  D$ = C$: GOTO 540
534  D$ = F$: GOTO 540
535  D$ = G$: GOTO 540
540  PRINT : PRINT : HTAB 5: PRINT
    "INPUT MESSAGE-64CHARACTERS
    MAX": INPUT D$
545  D$ = D$ + "
                                "
548  HOME : VTAB 5: HTAB 12: PRINT
    "WRITTEN INTO RAM": PRINT : PRINT

550  D$ = LEFT$ (D$,64)
570  FOR I = 1 TO 64
575  Z$ =  MID$ (D$,I,1):Z = ASC
    (Z$)
580  POKE  - 14336 + I,Z
582  PRINT Z$;
585  NEXT I
590  FOR I = 1 TO 5000: NEXT I
595  HOME : GOTO 60
600  END
```

Table 1) An APPLESOFT BASIC program for demonstrating the four operations of NOVRAMs.

* APPLE II and APPLESOFT are trademarks of Apple Computers.

8

Protection Against Inadvertent Store

The circuit described in the previous section assumes that the system is powered up and down in an orderly manner. This would mean that the microprocessor would never generate addresses unless they were part of the program. Unfortunately real systems do not operate in this ideal manner. Although the circuit described above has not produced a fault during extensive testing, the possibility exists that the hex addresses $C0A0-$C0AF could come up during power up, or during a brown out when the supply dropped below the operating specification, or during a power failure.

Several methods can be used to insure that the NOVRAM does not react to errors produced by the system when it is out of its operating specification. Setting the $\overline{\text{RECALL}}$ pin LOW to block a STORE operation is the easiest. Holding the $\overline{\text{STORE}}$ pin between VIH MIN and the falling power supply is another.

Most microprocessors are not totally under control for the first few cycles after power up. Their early addresses depend on what is in the registers after the System Reset pulse terminates. There is a possibility that these registers can cause one of the early addresses to be the same selected for a STORE operation. In this case the circuit shown in Figure 8 could cause the EEPROM to be written with false data during the power up operation. Figure 8 allows the STORE operation to be initiated if any of 16 addresses is selected for either a read or a write.

Although microprocessors can put out uncontrolled addresses they do not put out uncontrolled write commands. By ANDing the System Write line with the System STORE command, the NOVRAM would recognize a STORE operation only on a machine write cycle.

A potential danger in the use of the above schemes is the fact that three state TTL gates are not under total control while the power supply is coming up. This could produce glitches on the STORE pin even though no Write command was received at the input of the gate. A more positive way to insure that the $\overline{\text{STORE}}$ pin follows the power supply as the voltage increases is to use an open collector NAND gate with one of the inputs provided by a signal that determines power supply status (Circuitry for power supply status will be covered later in this application note). If one input of an open collector NAND gate is held LOW the output transistor is turned OFF since it can not receive base current. Pulling the output of this gate to the power supply of the NOVRAM through a pullup resistor will then insure that the output follows the power supply with no glitches.

Carrying the use of a power supply status signal one step further, would be to use it to hold the $\overline{\text{RECALL}}$ pin LOW in addition to holding the $\overline{\text{STORE}}$ pin HIGH. A direct connection of this status signal to the $\overline{\text{RECALL}}$ pin is all that is necessary as shown in Figure 9. This circuit has a more positive control of the NOVRAM since it takes two actions to prevent an inadvertent STORE operation.

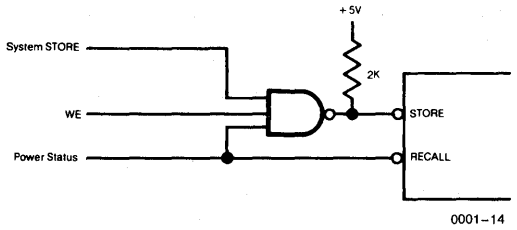

Figure 9) A power supply status line held LOW can insure that both the $\overline{\text{RECALL}}$ pin is held LOW and the $\overline{\text{STORE}}$ pin is held HIGH.

An example of a basic circuit to monitor the power supply status is shown in Figure 10. The output of this two-stage circuit is held LOW whenever the power supply is below 4.5 Volts. This same technique can be used with a Zener diode and an operational amplifier. The designer is cautioned to consider temperature effects.

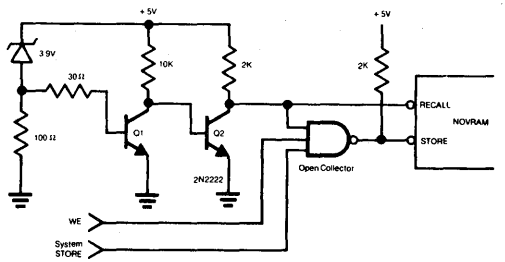

Figure 10) The Zener power supply detector is used in combination with the open collector on the $\overline{\text{STORE}}$ pin to provide protection against an inadvertent STORE operation during power up and power down.

Another method of power supply status is to assume that the only power supply fault which requires insuring that wrong data is not stored is the loss of the AC line voltage. Many commercially available AC line fault monitors are on the market. Two of these line fault monitors are the MID 400 Power Line Monitor from General Instrument and the SG1547 from Silicon General. Additionally, many commercially available power supplies have a power fail signal either as a standard feature or as an option.

The circuit shown in Figure 11 shows another type of power supply status detector. This circuit is a low cost solution but it should be used only to take the $\overline{\text{RECALL}}$

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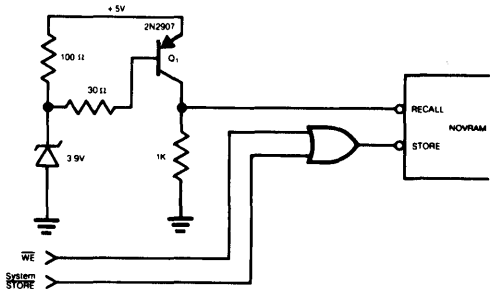
pin LOW because it does not provide adequate drive for a TTL gate.



0001-16

Figure 11) Another form of power supply status detector to drive the RECALL pin LOW when the supply drops below 4.5Volts.

Some other schemes to protect against inadvertent STORE operations are the use of jumpers, cables and/or switches. The STORE signal is transmitted through the jumper or switch which is normally open unless it is desired to change the data in the EEPROM. During normal operation the only component attached to the $\overline{\text{STORE}}$ pin is a resistor to the power supply.

A more comprehensive discussion of power supply status circuitry can be found in XICOR's Ap Note #102. This note covers those requirements that STORE data at power failure.

Applications

Most microprocessor systems have need for some form of nonvolatile memory to store important data such as:

1) Calibration constants
2) Set-up configuration information
3) User system ID
4) Changeable programs/firmware
5) System status
6) Accounting information
7) Error conditions

The types of equipment that are today being designed to include NOVRAMs vary through the complete line of electronic equipment. Some of these systems are:

1) Computer peripherals/terminals etc.
2) Automatic tellers/transaction terminals
3) Point-of-sale terminals
4) Smart scales
5) Vending machines and games (i.e. arcade games, slot machines)
6) Meters (i.e. utilities, taxi, gas pumps)
7) Process control
8) Robots
9) Instruments (musical, medical, test, avionics)
10) Communications
11) Transducers/load cells
12) Automotive: odometers, engine control
13) Office equipment: copiers, word processors
14) Military products

Some of the competitive products being replaced by NOVRAMs in systems are:

1) DIP switches
2) Thumbwheel switches
3) CMOS with batteries
4) EAROM
5) EEPROM
6) Potentiometers

One should let his imagination soar when thinking applications for these unique NOVRAMs. XICOR is always interested in application ideas that represent both normal and off-beat uses of these NOVRAMs. Any ideas sent to XICOR will be greatly appreciated.

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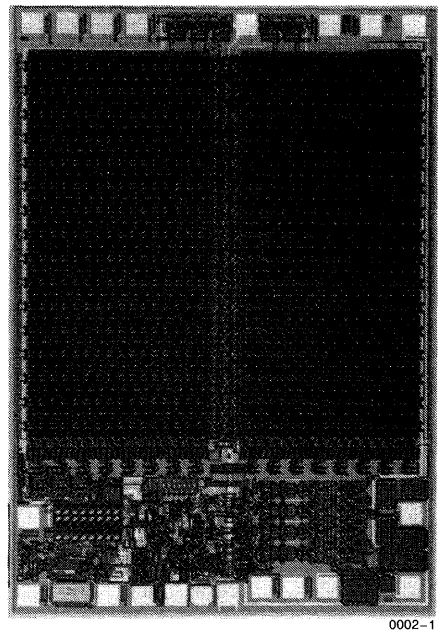
NOTES



0002-1

XICOR REPLACES DIP SWITCHES AND TRIMMERS WITH NOVRAM* MEMORIES

By Applications Staff

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*NOVRAM is Xicor's nonvolatile static RAM device.

Introduction

The desire to replace mechanical components in electronic systems for purposes of increased reliability, lower costs and ease of maintainability has spread to DIP switches and trimming potentiometers or trimmers. The component that makes this replacement possible is the NOVRAM memory from Xicor. The NOVRAM memory is a device that has two memories in parallel, a standard static RAM and a nonvolatile electrically erasable programmable read only memory (EEPROM). The EEPROM portion of the NOVRAM memory holds data that is equivalent to the settings of the now obsolete DIP switches and trimmers.

What Is A NOVRAM Memory?

A NOVRAM memory, as stated previously, is two memories in a single unit. The standard static RAM has a nonvolatile EEPROM cell associated with each RAM cell. Figure 1 shows a block diagram of a typical NOVRAM memory.

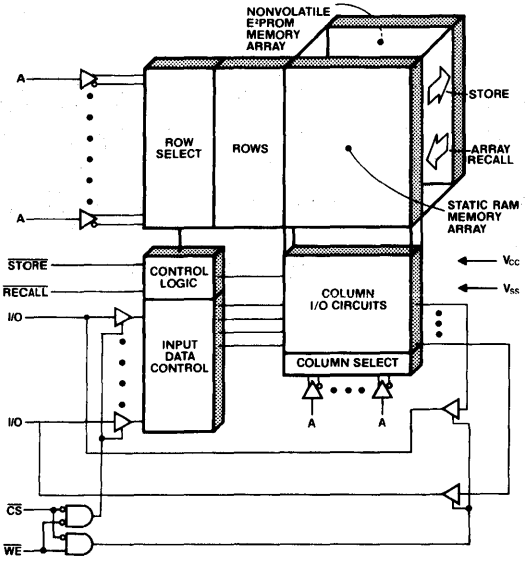

Figure 1) NOVRAM memory block diagram.

There are two additional pins on a NOVRAM memory device that do not appear on an ordinary static RAM. These two pins are called $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$. The $\overline{\text{STORE}}$ pin is used to transfer the entire contents of the RAM to the EEPROM as a single block. This operation is performed in parallel. The $\overline{\text{RECALL}}$ pin is used to transfer the entire contents of the EEPROM back to the RAM. At the end of either operation, the contents of the two memories are identical.

Access to the EEPROM data is through the RAM portion. To alter the contents of the EEPROM, the data must first be written into the RAM and then transferred to the EEPROM with a Store operation. To use the contents of the EEPROM in the system, perform a Recall operation and then the contents of the RAM may be read. Once data is stored in the EEPROM, the RAM can be used as an entirely separate and independent memory. Some users put configuration data into the EEPROM and then use the RAM as a separate scratchpad.

Besides these operational features, the NOVRAM memory has some unique electrical features. These devices are the world's easiest-to-use nonvolatile components in that they operate with only a single 5-volt power supply, simple TTL level pulses and short pulse widths (<450 ns). Even for operations such as the Store operation, which takes 10 ms to complete, it only requires a low level TTL pulse of 100 ns or greater to initiate. During the remaining time, the NOVRAM memory is not on the bus, which frees the microprocessor and the bus for other tasks. Complete details of the operation of NOVRAM memories can be found in the individual data sheets and application note AN101.

Replacing DIP Switches With NOVRAM Memories

DIP switches and thumbwheel switches have been used in systems to provide alterable, nonvolatile data. Some uses of this data are to set up configuration parameters and to provide calibration constants. The apparent low cost of these components is one of their attractive features. The drawback is that costs of these components do not end with installation.

The biggest cost of these mechanical, nonvolatile components is in post-installation service. A simple change of a DIP switch setting can require a technician to visit the equipment, disassemble the unit, throw the switch and reassemble the equipment. This could easily run the total use costs to well over 10 times the installed cost. A solution to the problems presented by DIP switches is to use a NOVRAM memory to hold valuable configuration or calibration data. In addition to a lower-cost, easier, and more secure method of changing data, NOVRAM memories cost less at the installed level.

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The disadvantages of using DIP switches in modern electronic systems accumulate through each step of the manufacturing process. The first stage of NOVRAM memory advantages starts right at system concept and design. Since the density of NOVRAM memories is significantly greater (up to 1024 switches in a single low-cost DIP package), more functional options can be added to enhance the total value of the system. Features such as electronic unit type signature can be added for a small software cost, with no extra components. No special access needs to be provided to change the NOVRAM memory, as all changes can be made from a keyboard or over phone lines. This can not be said for DIP switches, which require disassembly or special doors or hatches to provide access.

At incoming inspection it is difficult to completely test a package of DIP switches for all possible combinations, or even as individual switches. The NOVRAM memory, on the other hand is tested by automatic test equipment both quickly and thoroughly. The NOVRAM memories are 100% tested by Xicor and can be further tested at whatever levels the user desires, including the quick testing of all the options that were designed into the equipment. In the case of the DIP switch, this would require manually setting each option, rather than have the final system test equipment take care of the task.

The assembly operation is made more difficult when trying to wave solder or clean a board containing DIP switches. These operations can cause contamination in the degreasing step. This is true, even on the components that have tape or other cover for protection, as these are extra items to handle or become lost. Again, the NOVRAM memory exhibits none of these problems in that they are in sealed packages like the rest of the semiconductor components that make up the bulk of the system.

Once the system is in the field, the advantages of the NOVRAM memory are further enhanced. The basic reliability improvement of semiconductors over mechanical components is well known. Equipment warranties can be enforced since there is no need for a customer to open the equipment. The greatest advantage of all comes in service. No longer is it necessary for a technician to travel to the users site to change the setting on DIP switches as this can be accomplished over a phone hookup.

In addition to all of the above cost savings and system benefits in using NOVRAM memories, the basic component cost is also very low. Figure 2 shows a typical interface for DIP switches in a microprocessor system. Each package of 8 switches requires a decoder port and 8 diodes to provide isolation from other switches.

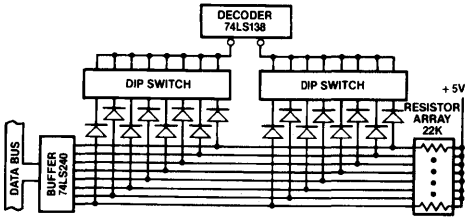

Figure 2) Typical DIP switch interface for multiple packages.

An octal buffer and 8 pull up resistors are required for any quantity of switch packages in a given system. Matrix schemes could be applied to reduce the decoder ports at the cost of more buffers but, by then, the costs will be much greater than those of using NOVRAM memories.

The assembly costs include incoming inspection, handling, inventory, board real estate, and final inspection. These costs are variable depending on volume and other factors.

The interface of a NOVRAM memory to a microprocessor is shown in Figure 3.

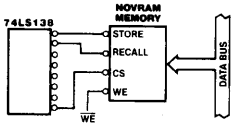

Figure 3) The typical NOVRAM memory interface requires only 3 decoder ports for any number of switches up to 1024.

This setup requires 3 decoder ports for any number of switches up to 1024 and then starts adding a single port for each additional package of 256 or 1024 switches.

The plot in Figure 4 shows that system costs using NOVRAM memories remain constant as the equivalent packages of DIP switches required are increased. These costs include the costs of all associated components, assembly and testing.

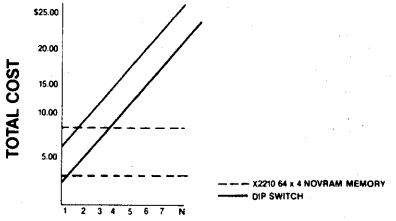

Figure 4) Relative costs of using NOVRAM memories as opposed to DIP switches as a function of packages of 8 switches required.

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The plot shows that whenever the required number of DIP switch packages of 8 switches exceeds 1, the NOVRAM approach is lower in cost at the systems level.

The cost of using DIP switches rises constantly as the number of required packages increases. An actual cost crossover occurs between 1 and 2 packages of 8 switches. Designers can derive their actual costs by calculating the two approaches based on the costs at their firm. These costs should include, in addition to the component costs, all costs associated with incoming inspection, warehousing, assembly and system tests. One will find that the crossover between 1 and 2 packages of 8 switches is consistent and favors the NOVRAM memory approach.

Where And Why Trimmers Are Used

The trimming potentiometer or trimmer is a 3-terminal device that can be connected in many different configurations. The purpose of the trimmer in the analog circuit is to make a fine adjustment of a current or a voltage. This current or voltage is then used in analog circuits to compensate for component variations in frequency, gain, offset, voltage or current.

Like the DIP switch, the trimmer appears quite inexpensive when one considers only the purchased price. In actuality it can be one of the most expensive components on the card when the costs of field calibration are taken into consideration. It takes only one service call (considered by some to cost approximately $200) due to a changed setting caused by vibration, humidity or even well-intentioned user tampering, to run the cost of using the trimmer to high levels. In addition, the trimmer requires equipment disassembly and the skilled use of a screwdriver. This skill adds to the cost of owning the equipment.

Taking an 'all costs considered' approach is one way manufacturers are reducing the cost of equipment ownership as a function of performance. Although the end customer wants equipment that is low in purchase price and service costs while delivering a high level of performance, they will purchase a more expensive piece of equipment if they believe that the service costs and possible downtime will be reduced.

The functions of the trimmer can be duplicated quite well by a NOVRAM memory combined with a Digital-to-Analog Converter (DAC). A DAC is a device that delivers a voltage at the output that is a function of a digital signal at the input. In a microprocessor system, this is a variable voltage source that is under the control of the program. While the DAC cannot exactly duplicate the 3 terminals of the trimmer, the circuit can be modified to provide equivalent results.

The NOVRAM memory provides settings for the DAC that are free from problems of humidity and vibration, as well as holding onto those settings during times of no power. Once the NOVRAM memory/DAC combination is in the circuit, the calibration can be made automatic by closing the loop since all mechanical adjustments are eliminated. A self-calibrating system can eliminate all expensive service calls for recalibration.

Duplicating The Function Of The Trimmer

This section will demonstrate a few simple concepts for using a NOVRAM memory and a DAC in combination to modify important circuit parameters. As previously mentioned, a trimmer adjusts small variations of frequency, gain, offset, voltage or current. By properly interfacing the output voltage of a DAC in the analog circuit, these functions can be easily duplicated.

The first example shown will demonstrate how to effect a small adjustment in voltage that can be used as a reference or for some other need. Figure 5 shows an operational amplifier connected to provide a small amount of trim to the output. The 9.9k and 100 ohm resistors provide a division by 100 of the DAC output.

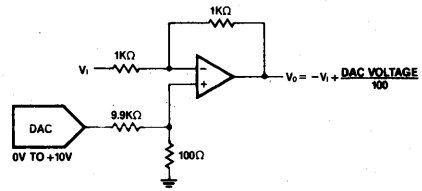

Figure 5) The DAC output provides up to 100 millivolts of trim for the operational amplifier output voltage.

If the DAC can be adjusted from 0 to 10 volts, this voltage divider provides an offset of up to 100 millivolts. The operational amplifier offset adds this amount to the output, providing up to 100 millivolts of reference voltage trim.

The next example will show how to provide a small offset for a fixed gain amplifier. Figure 6 shows the operational amplifier connected as an inverting amplifier with a gain of 10.

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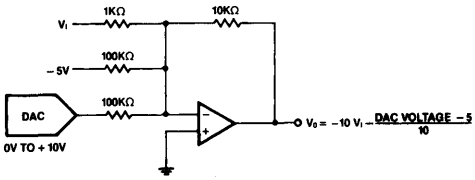

Figure 6) The DAC output provides an offset of 0.5 volt for a fixed gain amplifier.

The fixed gain is established by the 1K and 10K resistors. As the DAC output is varied from 0 through 10 volts, this voltage, combined with the −5 volts, reduces the amplifier output by $^1/_{10}$ of the difference. This gives a fixed offset of up to 0.5 volt in either direction.

The third example will show a different use of a DAC to change the operational amplifier gain. This example uses a CMOS DAC with the ladder network in the amplifier feedback loop.

A short course in CMOS DACs is in order at this time. Figure 7 shows a simple 3-switch CMOS DAC.

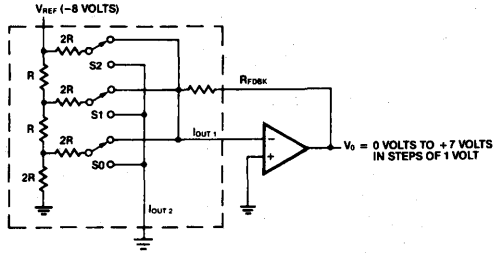

Figure 7) A simplified 3-switch CMOS DAC.

The outputs of a CMOS DAC are in the form of current. The sum of the two output currents is always a constant. In the case of Figure 7, this sum is $^7/_8$ x V_{REF}/R. Both current outputs must look into a ground potential. In Figure 7 the I_{OUT1} pin is tied to the summing junction of an operational amplifier while the I_{OUT2} pin is tied to system ground. The internally provided feedback resistor should be used with an amplifier since its temperature coefficient is identical to the other resistors on the DAC chip. The DAC switches are operated by standard 5 volt logic levels. The amplifier output in Figure 7 will vary from 0 to 7 volts in 1 volt increments depending on the setting of switches S0, S1 and S2. These switches in the 'up' position add 1, 2 and 4 volts, respectively, to the amplifier output. In the positions shown, the amplifier output is 7 volts.

Figure 8 shows the CMOS DAC of Figure 7 in a slightly different configuration.

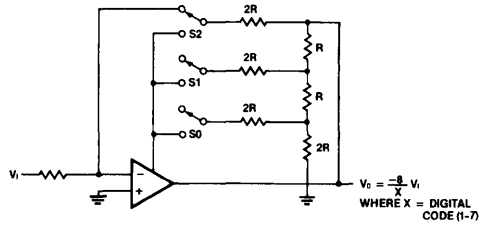

Figure 8) A CMOS DAC used in the amplifier feedback loop to adjust the amplifier gain.

The ladder network provides the feedback to the amplifier while the internal feedback resistor is used as the input resistor. If one goes through the equations, the result for Figure 8 is VO = VI x 8/X, where X is the digital code for the switch settings from 1 to 7. The circuit gain runs from a low of $^8/_7$ for the switches in the indicated position, to a gain of 8 when S0 is high and the other switches are low. Table 1 shows a listing of the gains obtainable.

S2	S1	S0	GAIN
L	L	H	8
L	H	L	4
L	H	H	$2^2/_3$
H	L	L	2
H	L	H	$1^3/_5$
H	H	L	$1^1/_3$
H	H	H	$1^1/_7$

Table 1) Gains of the circuit in Figure 5 as a function of the switch settings.

Analog Circuit Examples

This section will present some actual circuit examples for using a NOVRAM memory combined with a DAC. The circuits that appear in this section have been built and tested. The concepts presented may be useful to stimulate ideas which will help to solve the reader's system problems and may even be of immediate use. Figure 9 shows how the NOVRAM memory/DAC combination provides a voltage or a current for the application.

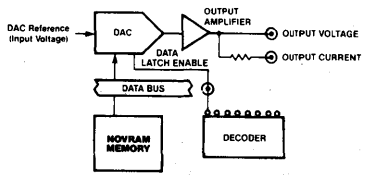

Figure 9) A NOVRAM memory DAC combination provides a voltage or a current to correct analog circuits.

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It is, of course, possible for a single NOVRAM memory to provide the address setting for multiple DACs. The DAC size used is selected for the user's application, depending on the accuracy and resolution required. There are even multiple DACs available in a single package such as the SAB 3013 from Philips for more cost sensitive applications.

Tuneable Crystal Oscillator

The first application example of a NOVRAM memory used in combination with a DAC is that of a quartz crystal oscillator. These circuits find application in many areas, including aviation and nautical navigation, as well as time measuring due to high stability. The oscillator is normally trimmed with a small padding capacitor in shunt or series with the crystal. This trim is used to 'pull' the resonance point of the crystal by a few parts per million (PPM) to set the operating frequency of the circuit. The capacitor may have to be adjusted in the field to retrim for the aging effects of the crystal and its associated circuitry.

The circuit in Figure 10 uses a NOVRAM memory/DAC combination to provide the trim voltage for a varactor.

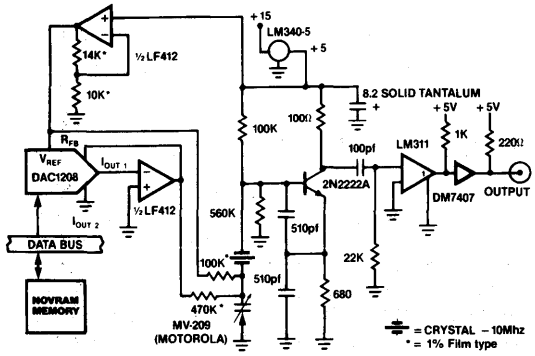

Figure 10) Tuneable crystal oscillator.

A varactor is a diode whose capacitance is a function of the applied voltage. This varactor in series with the crystal provides the actual trim function. The fixed operating point for the varactor is supplied through the 100K resistor. Variable bias for the diode is supplied by the DAC through the 470K resistor. Figure 11 shows that a 50 PPM frequency trim range is achievable with the 12-bit DAC used.

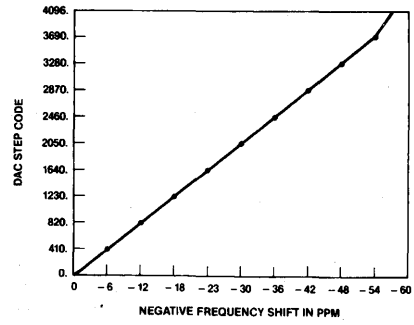

Figure 11) Tuning range of the tuneable crystal oscillator of Figure 10.

The frequency shift is down so it is recommended to specify the crystal approximately 25 PPM higher than the desired frequency. Initial trimming and re-trimming is easily accomplished by changing the DAC address settings as stored in the NOVRAM memory.

Software Programmable Voltage Reference

Many systems (such as DVMs, test equipment, data acquisition systems and most forms of measurement and control apparatus) require a voltage reference that places a limit on total system performance. Figure 12 shows how a NOVRAM memory/DAC combination can provide a means of adjusting the ouput of a precision 10 volt reference.

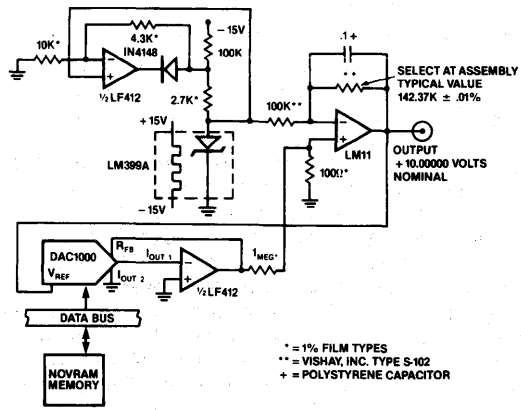

Figure 12) Software programmable voltage reference.

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An LM399A 6.95 volt reference is used in a bootstrap configuration to supply bias to the LF412 amplifier which in turn drives the LM399A. The 100K resistor insures start-up. The reference supplies bias to the LM11 amplifier, which supplies the circuit's output.

The NOVRAM memory/DAC-1000 combination supplies an offset voltage for the LM11 of 1 millivolt full scale in 1 microvolt increments. The 0.1 µF capacitor insures dynamic stability and low noise at the LM11 output. To calibrate the output to within 1 microvolt, one sets the DAC to half scale and selects the feedback resistor of the LM11 until the output is within a few hundred microvolts of the desired value. Then the RAM portion of the NOVRAM memory is exercised, providing new inputs for the DAC until the desired value is achieved. This setting is then stored in the EEPROM portion of the NOVRAM memory. If a wider trim range is desired, the 1 megohm resistor can be reduced, but this degrades the setpoint resolution appropriately.

Self-Calibrating, Interchangeable Probe Thermometer

A standard industrial temperature sensor with high linearity and long term stability is obtained using platinum resistance temperature detectors (RTDs). The RTD is specified in terms of its resistance at 0° centigrade (as this is a function of the manufacturing process), while the gain slope is relatively constant from unit to unit. A constant gain amplifier with an offset to compensate for the changing impedance at 0° centigrade is shown in Figure 13.

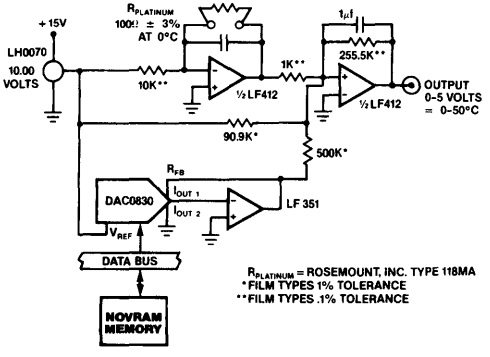

Figure 13) Self-calibrating, interchangeable probe thermometer.

The NOVRAM memory/DAC combination is used to modify the offset voltage of the amplifier to allow full interchangeability of probes in the field.

The plantinum RTD shown has a ±3% tolerance at 0°C (±7.5°C) and is driven with a 1 milliampere constant current source by placing it in the feedback loop of the LF412 amplifier. The constant current is provided by the 10 volt reference IC. The amplifier output will be a linear function of the sensed temperature at the RTD. The 1 µF capacitor limits noise pickup and also insures that the RTD, a wirewound device with parasitic inductance, does not cause amplifier oscillations. The second half of the LF412 provides a fixed gain to the signal.

The 90.9K resistor provides a current to the summing junction of the amplifier to move beyond the correction for the worst case sensor. The NOVRAM memory/DAC pair then pull enough current from the summing junction to correct for the inserted RTD. Over a 0°C to 55°C range, this circuit is accurate to within ±0.25°C while allowing the use of probes with a ±7.5°C tolerance specification.

Automatic Scale Calibration

The scale normally does not worry about a zero-level reading from its sensor, since it may have a wide variety of items on the platform such as wrapping paper or containers. An algorithm is usually required to automatically zero the scale before loading the material into the container. The transducer used in scale applications has a large variation in gain slope which must be corrected before shipping the scale or when changing the load cell. Figure 14 shows a circuit for providing these necessary corrections for the gain slope of the sensor.

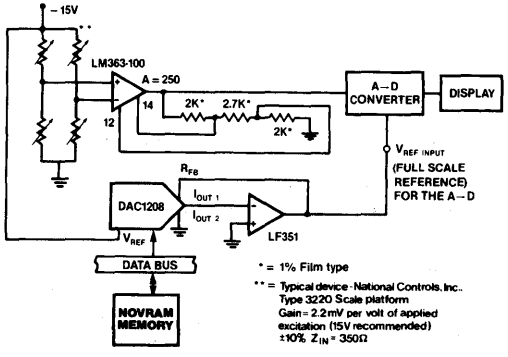

Figure 14) Automatic scale calibration.

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The transducer shown, combined with the fixed gain amplifier, can produce outputs of 7.424 volts to 9.075 volts for full load depending on the transducer selected. To bring this result to the required value, the NOVRAM memory/DAC combination is used to vary the reference of an analog-to-digital converter. Since the DAC and the platform bridge are driven from the same supply, the measurement is ratiometric and no stable voltages are necessary. As the −15 volt supply changes, the readout on the display will not vary. To calibrate a new platform, the scale is first zeroed out using the internal algorithm and then a fixed known weight is added to the platform. Then the NOVRAM memory/DAC unit is exercised until the correct readout is obtained. This calibration can be called from the scale's keyboard. Security for this adjustment can be in a software access code which is also stored in the NOVRAM memory.

Gain Trimming For Photomultiplier Tube

The last example handles gain variations in a slightly different manner. The gain of a photomultiplier tube varies over time, temperature and power supply for a given input level. The output is a current from a high impedance source. A circuit to trim the changing gain is shown in Figure 15.

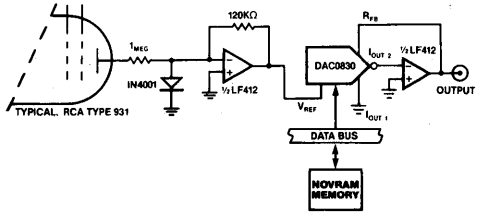


Figure 15) Gain trimming for photomultiplier tubes.

This current is converted to a voltage by the amplifier on the left side of the figure. For a full scale current of 100 μA, the output voltage of this amplifier is 12 volts. This voltage output is used as the reference input for a NOVRAM memory/8-bit DAC combination which amplifies the reference from $^1/_{256}$ through 1 depending on DAC setting. This gain can be varied in steps of $^1/_{256}$. The currents out of the photomultiplier tube are normally accurate to only 1% once the calibration is complete. Some applications, however, may require smaller steps in resolution. If this is the case, one could use a 10-bit DAC. Another method of obtaining fine resolution is to use an 8-bit DAC connected as shown in Figure 8 in place of the DAC arrangement of Figure 15. If the feedback resistor of the left-hand amplifier is changed to 50K, very fine tuning (around a voltage gain of 2) is possible. This gain of 2 is established when the DAC is set for midrange of the digital value which gives a fine tuning range.

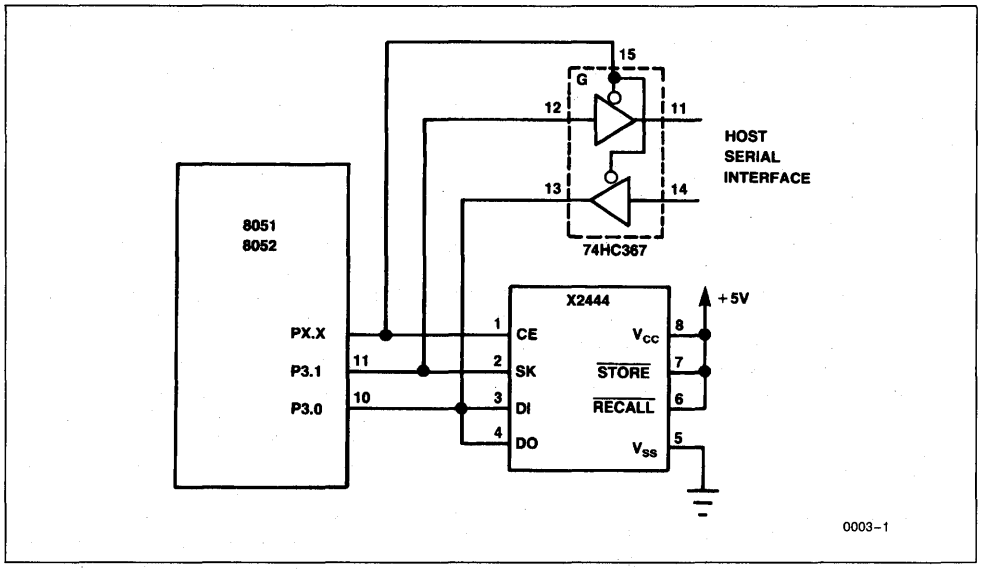
Conclusion

This application note has shown how the NOVRAM memory can be used to replace commonly used mechanical components such as trimmers and DIP switches. This replacement improves reliability and reduces service costs for recalibration and resetting. In addition, actual equipment costs can be reduced.

Once a single NOVRAM memory is in the system, it is easy to include additional features in the unused portions. For example, a system designer could use a NOVRAM memory to replace DIP switches used for configuration data and then place calibration data for DACs in the unused memory. If even more unused space exists, storage of other desired data such as ID numbers or a service log would be possible.

The possible uses of NOVRAM memories are limitless. The designer is encouraged to build upon the ideas presented by this application note.

0002-8



THE X2444 SERIAL NOVRAM* TEAMS UP WITH THE 8051 MICROCONTROLLER FAMILY

Add scratch pad RAM and nonvolatile parameter store via the 8051 serial port and still maintain full use of the serial port as a UART.

Application from Rick Orlando
Written by Richard Palm

8

*NOVRAM is Xicor's nonvolatile static RAM device.

INTRODUCTION

The X2444 is a 256 bit serial NOVRAM internally configured as sixteen 16-bit words of RAM overlaid bit for bit with a nonvolatile E^2PROM. The X2444 has the standard hardware RECALL and STORE inputs plus the ability to perform these same operations under software control, thereby freeing two microcontroller port pins for other tasks. The serial interface allows the X2444 to be packaged in a low cost space saving 8-pin mini DIP.

When teamed with the 8051 family of microcontrollers, the X2444's small physical size, software instruction set and serial interface make it an ideal parameter store and scratch pad memory while maintaining full use of the 8051 serial port as a UART.

SCOPE

This application note describes interfacing the X2444 with the 8051 family of microcontrollers. Emphasis will be placed on the timing considerations of the interface, and explaining the modifications to the instruction words for normal device operation. This note assumes the reader has access to a Xicor Data Book and Intel *Microcontroller Handbook.*

SERIAL PORT OPERATION

Port 3 on the 8051 provides a serial port that can be used in two basic configurations, full duplex and half duplex. This note examines the half duplex (mode 0) operation in interfacing to the X2444. Port 3 pin 1 (P3.1) is the clock output for both transmit and receive modes and Port 3 pin 0 (P3.0) is used for bidirectional data transfers.

The clock output frequency is 1/12 of the XTAL oscillator input frequency. To simplify timing calculations this note will assume an input frequency of 12 MHz resulting in a symmetrical 1 MHz output on P3.1.

The P3.1 and P3.0 pins when inactive (neither transmitting nor receiving) are always a logic 1 (HIGH). When a data transfer commences P3.1 will be LOW during machine cycle states S3, S4 and S5 and will be HIGH during states S6, S1 and S2. When transmitting, data is shifted out on P3.0 during S6P2 (state 6 phase 2) LSB first. When receiving, data is sampled during S5P2. Refer to Figure 1 for the basic 8051 serial port timing.

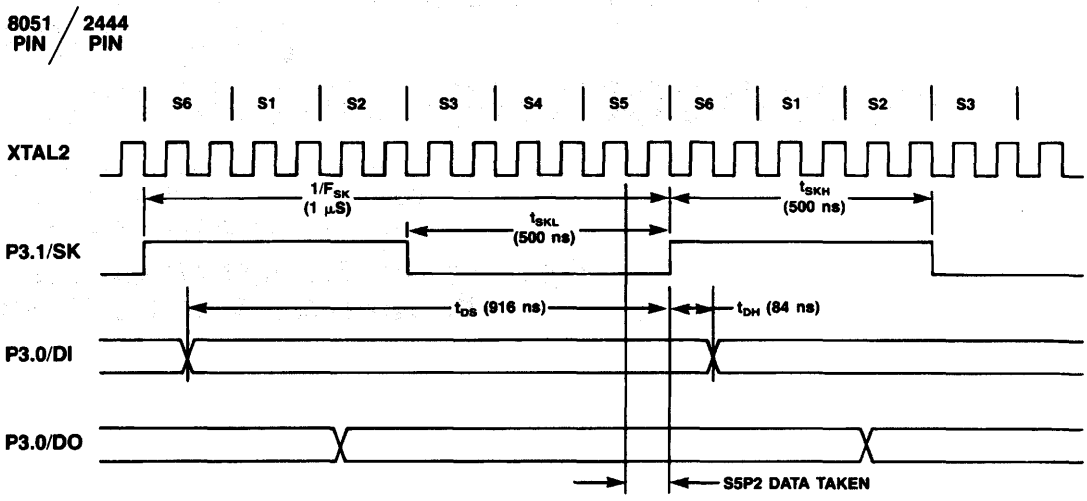


Figure 1. 12 MHz 8051 Serial Port Mode 0 and X2444 Timing

0003-2

HARDWARE CONNECTIONS

The X2444 directly interfaces with the 8051 with no external circuitry required. DI and DO of the X2444 are both tied to P3.0, SK is tied to P3.1, CE is tied to any free port pin configured as an output and STORE and RECALL are tied to V_{CC} (see Figure 2).

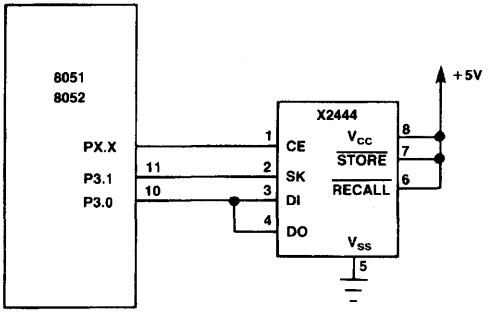


Figure 2. Basic Configuration

X2444 OPERATIONS REVIEW

The X2444 is a serial device and in this application all chip functions are handled via the software instructions. The 8051 transmits data LSB first but the instruction format for the X2444 shows the instruction to be transmitted MSB first. This requires a simple transposition of the instruction, MSB for LSB. The memory is effectively a FIFO, so the data to be stored need not be transposed.

Internally the X2444 increments a bit (clock) counter. This is used to indicate the end of an instruction and if a read or write instruction is received, to increment a bit position pointer. This pointer enables individual RAM cells for writing and reading. The counter for the pointer increments from zero to fifteen. If CE remains HIGH and SK continues to clock, the counter will rollover from fifteen to zero. The word address does not increment; therefore, during a write operation if SK continues to clock and CE is HIGH, a 25th rising clock edge (8 edges for instruction + 16 edges for the data word + 1) would cause bit position zero to be overwritten.

SYSTEM CHARACTERISTICS

Under normal operating conditions the X2444 expects CE to transition LOW to HIGH when SK is LOW in order that the first bit of data can be clocked into the X2444 on the first rising edge of SK. The data is sampled to see if it is "0" (a don't care state) or a "1" which is recognized as an instruction start. The 8051, however, places both P3.1 and P3.0 in the HIGH state when not actively transmitting. ***THIS IS OK.*** The X2444 internally gates CE and SK; therefore, toggling the port pin controlling CE to a HIGH effectively generates the first rising edge of SK, and also clocks in the HIGH present at P3.0 (DI).

What this does is clock a "1" into the X2444 indicating the start of an instruction prior to any shifting operation by the 8051 serial port. This will require dropping the leading "1" from the instruction. See Table 1 for the WAS/IS conditions for the equivalent instructions to be used by the 8051.

INSTRUCTION	WAS								IS							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
WRDS	1	X	X	X	X	0	0	0	X	0	0	0	X	X	X	X
STO	1	X	X	X	X	0	0	1	X	1	0	0	X	X	X	X
SLEEP	1	X	X	X	X	0	1	0	X	0	1	0	X	X	X	X
WRITE	1	A	A	A	A	0	1	1	X	1	1	0	A	A	A	A
WREN	1	X	X	X	X	1	0	0	X	0	0	1	X	X	X	X
RCL	1	X	X	X	X	1	0	1	X	1	0	1	X	X	X	X
READ*	1	A	A	A	A	1	1	X	1	X	1	1	A	A	A	A

*Note: bit 7 of the READ command should be a "1" to avoid bus contention.

Table 1. Reconfigured Instruction Format

The 8051 will still generate eight rising clock edges on P3.1 for each byte loaded into the shift register (SBUF), effectively providing the X2444 with nine clocks for the first byte. For the single byte instructions the ninth clock and data are ignored by the X2444. Refer to Figure 3 for the single byte instruction timing.

0003-3

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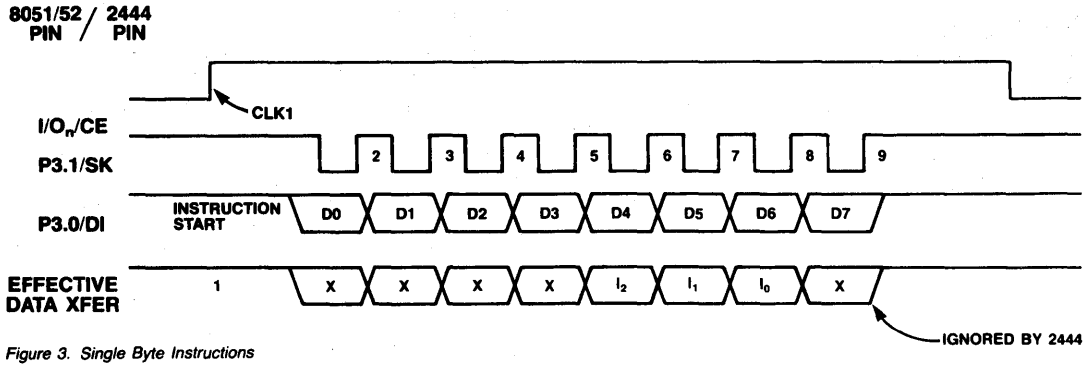

Figure 3. Single Byte Instructions

WRITING

Writing to the RAM array is straightforward. The write instruction is issued by the 8051 in the same manner as the single byte instructions. The MSB (eighth bit) of the instruction byte is clocked in on the equivalent ninth clock rising edge. This bit is recognized as the first data bit transfer and is initially written into the addressed word's bit position zero. The 8051 will continue to transmit two more bytes of actual data. The LSB (bit "0") of the first byte will be physically located in bit position "1" and all subsequent bits will also be offset by one. The MSB (sixteenth data bit) of the word will be written into bit position zero, overwriting the last bit of the instruction byte. Refer to Figure 4 for the sequence of operations.

READING

Reading data back from the RAM array is quite similar. The X2444 begins to shift data out during the instruction cycle (more on this later). After the instruction is shifted out, the 8051 must turn around P3.0 and configure it as an input. CE and SK are static during this period and the DO output will remain unchanged until after the rising edge of the first 8051 receive data clock. Therefore, the first data shifted into the 8051 will be from bit position "1", equivalent to the LSB originally written. Refer to Figure 5 for the sequence of operations.

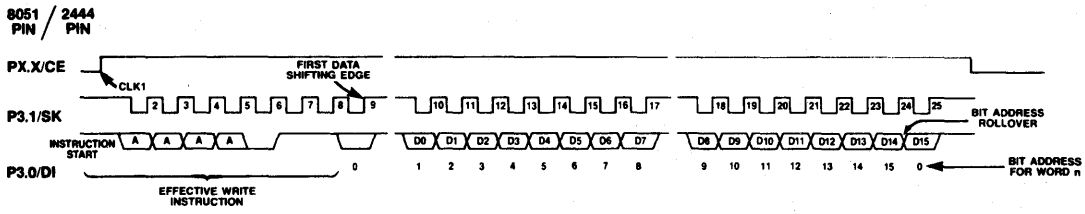

Figure 4. Write Cycle Sequence

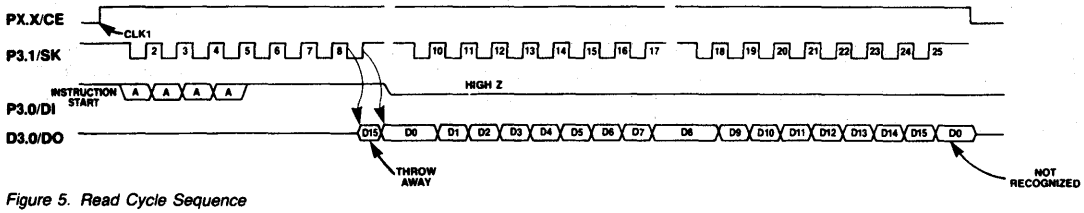

Figure 5. Read Cycle Sequence

0003-4

BUS CONTENTION

There will not be any bus contention for single byte instructions or the write command. However, for the Read command there could be contention. While the 8051 is still shifting out the instruction byte the X2444 begins to output data on the same line. Refer to Figure 5, just after the falling edge of clock eight.

The 8051 shifts out data at S6P2. If the data changes state from "0" to "1" a high current enhancement FET is turned on for two 8051 system clock cycles. This is used to provide a fast rise time. At the end of this two cycle period, the enhancement FET is turned off and the output is held HIGH by a depletion mode FET that essentially looks like a resistor pullup (Refer to Intel's *Microcontroller Handbook* [1984] pages 6-6 and 6-7). Note that the high drive circuit is enabled only for data state changes from "0" to "1"; therefore, if the output is already a "1" and another "1" is shifted out on P3.0, the high drive will *not* be turned on. This depletion FET can source a maximum of 250μA if the port pin is grounded.

The instruction table indicates that bit seven for the READ instruction should be a "1". The reason for this is to guarantee that the high drive period is off before the X2444 begins to output data. If bit seven were a "0", the 8051 would turn on the high drive circuit to return P3.0 to the inactive state, possibly generating a high current contention problem with the DO output of the X2444. Figure 6 illustrates the timing involved during clock eight. The high drive period of the 8051 is turned off well before the X2444 begins to output data.

VERSATILITY

The DO output of the X2444 is always in the high impedance state unless it is outputting data in response to a READ command. Therefore, the serial port of the 8051 need not be dedicated solely to a serial memory interface.

Figure 7 illustrates the versatility this affords. This figure depicts the basic system components required in a remote location controller. Notice that the 8051 serial port has access to both the X2444 and through the use of the CE control line maintains full use of the serial port as a UART. Therefore, it can receive downloaded parameters from a host, re-enable the serial port for X2444 communication, then store the data either temporarily in the X2444 RAM array or permanently in the X2444 E²PROM array.

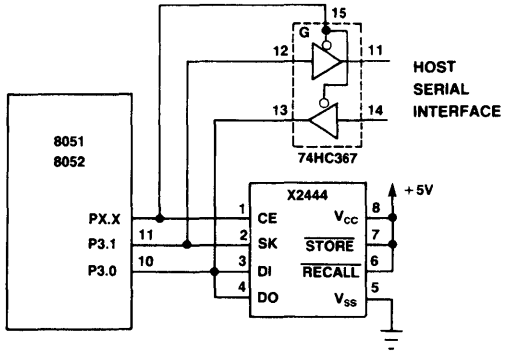

Figure 7. Shared Serial Port

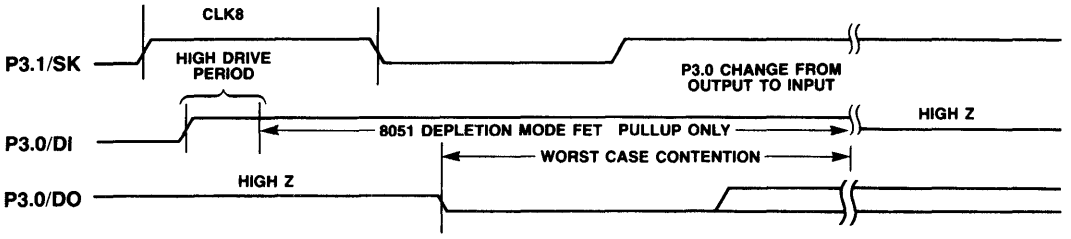

Figure 6. Worst Case Bus Contention

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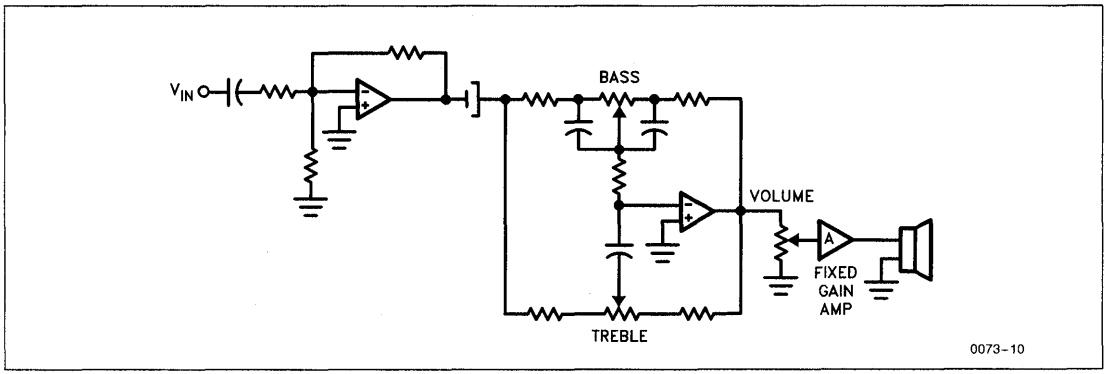
CONCLUSION

This application note has shown that with no extra hardware the X2444 interfaces directly with the 8051 family of microcontrollers, providing a non-volatile memory store and scratch pad memory and maintaining full 8051 UART capabilities. It is the ideal solution for applications where extra memory is required but few port pins are available for implementation.

0003-6



E²POT™ DIGITALLY CONTROLLED POTENTIOMETER BRINGS MICROPROCESSOR CONTROL TO AUDIO SYSTEMS—ADDS FEATURES

By Jeff Randall

8

E²POT™ is a trademark of Xicor, Inc.

INTRODUCTION

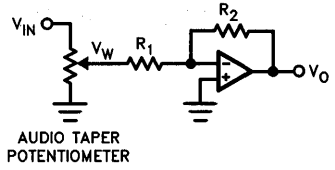
Control of most audio circuits is still accomplished the same way it has been for the last fifty years or so. From the volume control knob to the sliders on an equalizer, the control is human, the feedback is through the ears, and the control element is the mechanical potentiometer. Microprocessors have entered nearly every other segment of electronics, and as they enter the audio segment, they slam headlong into the mechanical potentiometer.

While this article focuses on microprocessor control of conventional audio circuits through the use of digitally controlled potentiometers, it should become clear how these devices can be applied to many other applications as well.

CONVENTIONAL AUDIO CONTROL

A look at conventional methods for audio control should help to illustrate the situation:

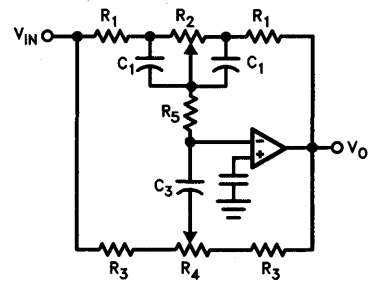
Designs incorporating mechanical potentiometers are still found in the majority of audio applications. For example, the volume control on most car stereos is a rotary potentiometer. Volume control circuits generally resemble Figure 1. In this design, the potentiometer is used to control the signal reaching a fixed gain amplifier section. A potentiometer in this application would likely have a logarithmic taper, since volume is a logarithmic function.



0073-1

Figure 1: Conventional Potentiometer Volume Control

Tone controls can vary from single pot and capacitor circuits to complex active filters. The Baxandall filter network has been the workhorse of the audio industry for years. This design, illustrated in Figure 2, utilizes two linear taper potentiometers to control the gain of an active filter. In this configuration, the potentiometer replaces a portion of both the input and feedback resistors. By moving the position of the wiper, both resistors change in opposite directions.



0073-2

Figure 2: Baxandall Tone Control Circuit

Graphic equalizers are one of the fastest growing modes of audio control. A graphic equalizer contains a group of band pass filters, usually seven. Each filter has a potentiometer controlling the gain to that band pass. Potentiometers generally appear as sliders on the face of the equalizer.

A typical graphic equalizer schematic is shown in Figure 3. EQs are used to compensate for the imperfections of a listening environment by boosting or cutting gain at specific frequencies. By using a spectrum analyzer and a "pink" noise generator, the response of an audio system can be customized for a particular room or concert hall. This is accomplished by inputting a desired response to the system—generally flat across the audio band, with some attenuation at higher frequencies, often referred to as "pink" noise. The equalizer is then adjusted until the system output, displayed on the spectrum analyzer, closely matches the pink noise input.

This process of matching a system to a room is often referred to as environmental calibration. It is a process requiring the listener to read the display of the spectrum analyzer and manually adjust the potentiometer/sliders of the equalizer.

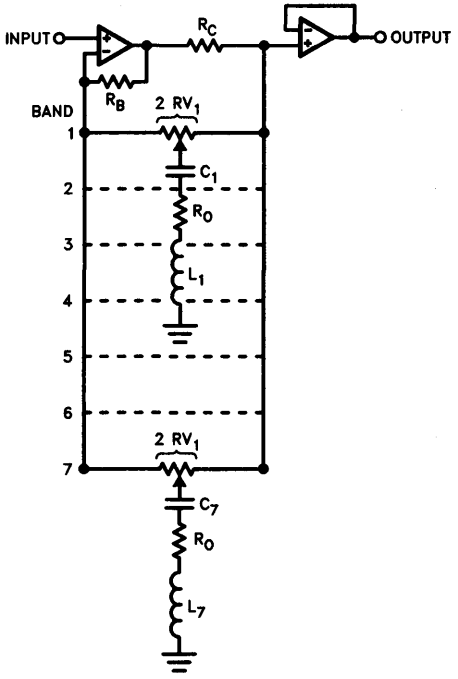


Figure 3: Graphic Equalizer Configuration

The heart of the control of each of the circuits described earlier is the mechanical potentiometer. Automated control of these devices is a challenge. Clearly, microprocessor control of these functions is desirable. The control elements utilized for automated control are discussed below.

AUTOMATED CONTROL ELEMENTS

While these devices are primarily used for industrial control applications, motorized potentiometers offer a relatively straightforward approach to simple audio control circuits. In these devices, a DC reference voltage, or a digital signal representing position is input to a small motor assembly that is linked to a rotary potentiometer. Drawbacks to this type of system are numerous, including noise caused by the motor assembly as well as the increased space and power requirements of placing a motor on an audio PC board.

D/A converters can also be used to control and manipulate analog circuit functions, but introduce more complexity. These devices are the choice of high fidelity digital audio controls due to their high precision. But for the analog circuit designer, they can be a little intimidating. For example, one way to control volume with D/A converters is illustrated in Figure 4. In this circuit, the signal is sampled with a A/D converter, manipulated by a microprocessor, and returned to the analog world with a D/A converter. This design entails sampling, real-time processing, as well as A/D and D/A conversions. Not only may the analog designer be faced with portions of his circuit that may be unfamiliar, the results may be overkill.

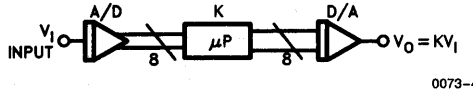


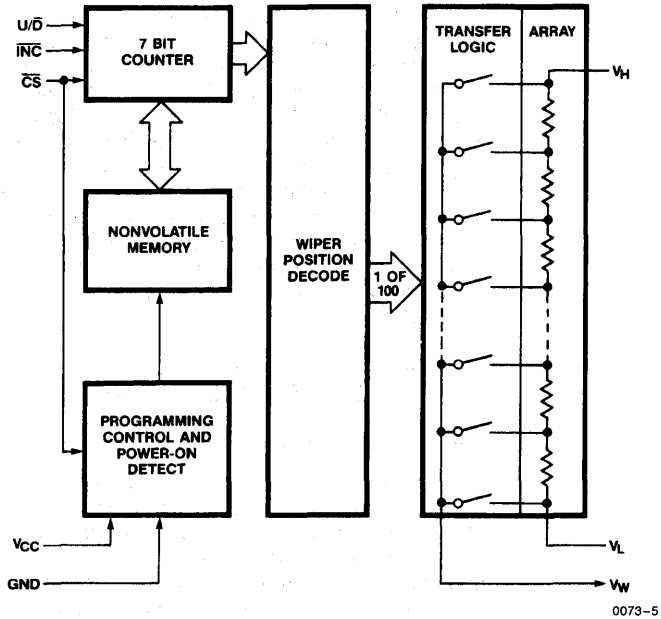
Figure 4: Volume Control Using D/A Conversion

An array of resistors with a wiper tap that can be selected with digital control offers many advantages of the microprocessor world without the complexity of D/A conversion. These are referred to as digitally controlled potentiometers. Logic circuits, counters, and memory circuits are often teamed up with resistor arrays to accomplish an approximation of potentiometer control. Recently, a few manufacturers have introduced devices which incorporate many of these functions in one device. Examples are Xicor's X9MME, Toshiba's TO9169AP, and National's LMC835.

The Toshiba and National parts are designed around specific audio applications and are distinctively different from the Xicor device. They incorporate features that lend well to audio designs, but are not intended for general purpose potentiometer replacement. Moreover, they offer only a limited number of wiper positions.

Xicor's X9MME combines a single 99 position potentiometer with three line digital controls. Figure 5 contains a functional diagram, pin description and mode selection for the device. In addition to the internal counter circuitry for wiper position control, this part also incorporates nonvolatile memory to retain wiper position. It has been designed as a digitally controlled replacement for the mechanical potentiometer. With its conventional three terminal potentiometer design, it integrates easily into existing analog designs.

Functional Diagram



Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↓	H	Wiper Up
L	↓	L	Wiper Down
↑	H	X	Store Wiper Position

Pin Configuration

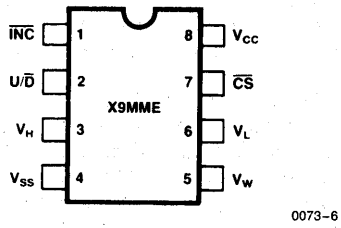


Figure 5: The X9MME Digitally Controlled Potentiometer

Pin Names

V_H	High Terminal of Pot
V_W	Wiper Terminal of Pot
V_L	Low Terminal of Pot
V_{SS}	Ground
V_{CC}	System Power
U/$\overline{D}$	Up/Down Control
$\overline{INC}$	Wiper Movement Control
$\overline{CS}$	Chip Select for Wiper Movement/Storage

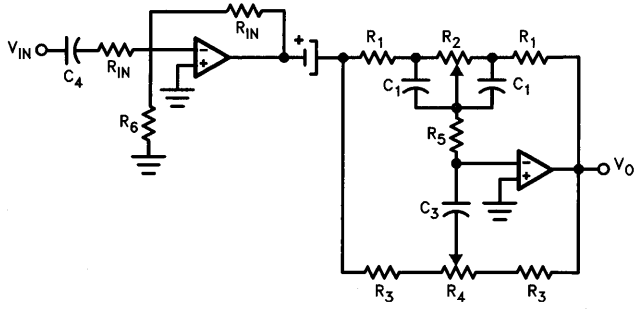
To illustrate digital control of potentiometer circuits, the X9MME from Xicor was used to replace mechanical potentiometers in a well known audio circuit. The following should demonstrate the ease of designing with the X9MME as well as the advantages of microprocessor control in audio circuits.

THE X9MME IN AN AUDIO CIRCUIT

The Baxandall tone control circuit is the basis for the designs shown here. The following sections will discuss the principles behind the Baxandall circuit and then walk through the design utilizing the X9MME. Special design considerations for the X9MME will be discussed, and the performance and operation will be evaluated.

The Baxandall circuit, its response, and equations for gains and filter frequencies are shown in Figure 6. This circuit contains two active filters whose gain is controlled by two potentiometers. Figure 7 illustrates the bass portion of the circuit. The maximum gain of this circuit is at low frequencies, where the capacitors in the circuit can be considered to be open circuits. The capacitors have been omitted for clarity. (The treble portion of the circuit, not illustrated here, follows along similar lines.)

Schematic



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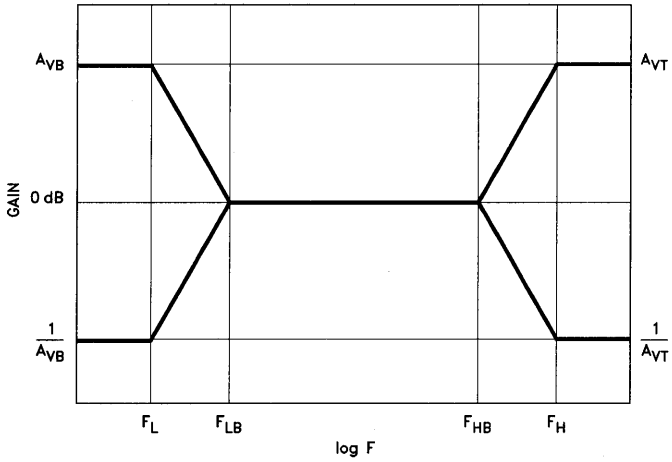
System Frequency Response



0073-8

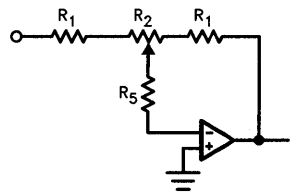
$$F_L = \frac{1}{2\pi R_2 C_1} \qquad F_H = \frac{1}{2\pi R_3 C_3}$$

$$F_{LB} = \frac{1}{2\pi R_1 C_1} \qquad F_{HB} = \frac{1}{2\pi (R_1 + R_3 + 2R_5) C_3}$$

$$A_{VB} = 1 + \frac{R_2}{R_1} \qquad A_{VT} = 1 + \frac{2R_5 + R_1}{R_3}$$

Figure 6: Active Audio Preamplifier

With the addition of another potentiometer on the output of the Baxandall network, the system represents a single channel of an audio preamplifier. The circuit contains three potentiometers which control volume, treble and bass. These pots would appear as knobs on the face of a home or car stereo, to be adjusted by hand to control and shape the sound reaching the amplifier and speakers.



0073-9

$$\left|A_{VB}\right| = \frac{R_1 + R_2}{R_1} \qquad \text{Maximum Bass Boost}$$

Figure 7: Bass Portion of Active Preamp Circuit

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Neglecting the digital control lines and 5V power for the X9MME, the circuit is shown in Figure 8. The X9MME will replace bass, treble and volume potentiometers. Note that this does not alter analog design considerations.

It should be noted that R_2 and R_4 are both linear taper pots. Since the X9MME is also a linear taper pot, it is a direct replacement. R_V, the volume potentiometer, is specified as an audio taper pot, since it is used for volume control. By placing a small resistor from wiper to low on any linear pot, as shown in Figure 9, an audio taper can be approximated. In this case a resistor of one-tenth the total pot resistance is a close approximation of an audio pot (EDN Nov. 13, 1986).

This circuit is designed to have a gain of one across the entire audio range, with the potential for a boost or cut of 20 dB at the frequencies selected by the designer.

THE DESIGN

The design chosen is intended for car stereo applications. It should therefore operate from a single ended, 12V supply and adapt well to speakers that are commonly used in automobiles. Considering the limited bass response of most car speakers, the bass boost or cut should not be so low that the speakers cannot reproduce the sound.

The desired circuit would operate from a 12V power supply, have a ±20 dB boost or cut at 100 Hz (bass) and 10 KHz (treble). The available resistor values for the X9MME are 10K, 50K, and 100K. The following steps outline the design:

1. $R_2 = 50\ K\Omega$ (arbitrary, X9503)

   The design must start somewhere. This value was actually determined after running through the design a couple of times and comparing the values determined for the potentiometers with those available.

2. $A_{VB} = 1 + R_1/R_2$; for 20 dB (10),

   $R_1 = R_2/9 = 5.6\ K\Omega$

   The bass portion of the circuit must have a maximum boost of 20 dB. This is determined with the bass pot all the way to the input side. A quick look at Figure 8 will illustrate this.

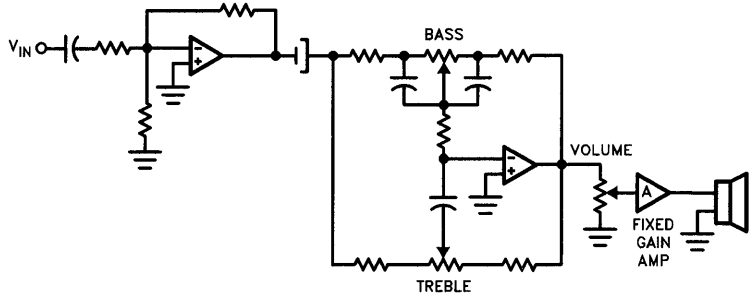
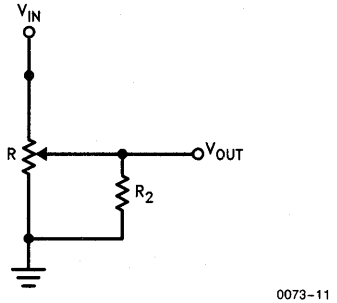


Figure 8: Active Preamp with Bass, Treble and Volume Controls



For Audio Taper, Use $R_2 = \frac{R}{10}$.

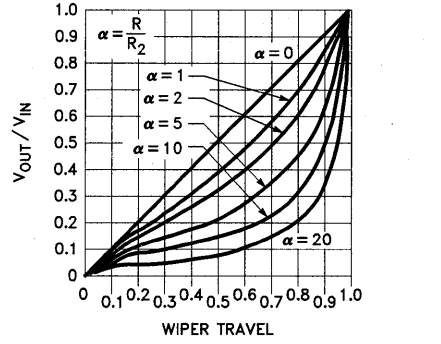


Figure 9: Utilizing External Resistors to Vary Potentiometers Trim (EDN Nov. 13)

3. $F_L = 100\ Hz$, $F_{LB} = 1\ KHz$

$$C_1 = \frac{1}{2\pi F_{LB} R_1} = \frac{1}{2\pi(1000)(5.6K)}$$

$$= 2.84 \times 10^{-8}\ F$$

Here, the formulas for the cutoff frequencies of the active filters are broken down to determine the element values to use.

4. $R_5 = 2.2\ K\Omega$ (arbitrary)

5. $A_{VT} = 1 + \frac{R_1 + 2R_5}{R_3} = 10,$

$$R_3 = \frac{R_1 + 2R_5}{9} = 1.1K$$

Use 1 KΩ

Here, the maximum treble gain is calculated in similar fashion to the maximum bass gain.

6. $C_3 = \frac{1}{2\pi F_H R_3} = \frac{1}{2\pi(10K)(1K)} = 1.6 \times 10^{-8}$

7. $R_4 \geq 10\ (R_3 + R_1 + 2R_5) = 110\ K\Omega$

Use 100 KΩ

8. $R_V = 10\ K\Omega$ (arbitrary)

The circuit with the X9MME inserted is shown in Figure 10. These are the values that were used in lab experiments and for demonstration purposes.

It should be noted that some considerations in the design had to be altered when the X9MME was inserted into the circuit. The X9MME is a source of high frequency noise. There are internal voltage generators on the device which are used to operate switches internally as well as to store information into the device's nonvolatile memory. The principle noise frequencies begin at approximately 150 KHz, and while this is beyond the audio range, it can still be a source of problems in the circuit. For this reason, capacitors were added around the X9MME to filter noise. These are included in Figure 10.

DIGITAL CONTROL

The digital control lines of the X9MME are $\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$. $\overline{CS}$ (chip select) allows the wiper to be moved. U/$\overline{D}$ (Up/Down) determines the direction in which the wiper will move, and $\overline{INC}$ (increment) initiates movement on its falling edge. $\overline{CS}$ is also used to store the wiper position in nonvolatile memory. When $\overline{CS}$ is returned high, a store operation is commenced.

When initially designing with the part, it was helpful to assemble a simple switch system for controlling the parts. A 555 timer was used to generate a fairly slow clock pulse and connected through a momentary switch to the increment pin of each X9MME. With pull up resistors on each digital line, a grounding switch was connected to U/$\overline{D}$ and another to $\overline{CS}$. To move the wiper up, $\overline{CS}$ was set to

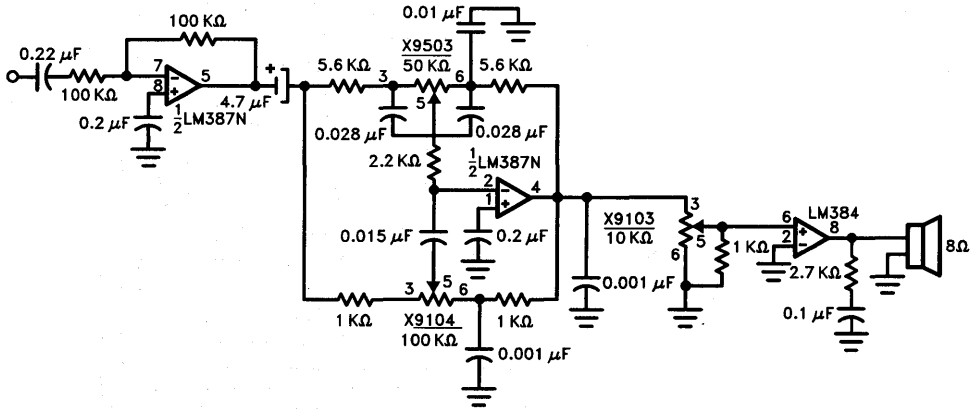


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Figure 10: E²PREAMP with Three X9MME—No Digital Controls Shown

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ground, U/$\overline{D}$ to 5V and $\overline{INC}$ pulsed with the clock. Each step of the clock produced a 1% change in wiper position. Figure 11 illustrates the switching network that was utilized for controlling all three X9MMEs.

This initial procedure allowed the analog portion of the design to be separated from the digital. Once the circuit was functioning adequately with the switch network controlling the X9MMEs, microprocessor interface was relatively simple.

MICROPROCESSOR INTERFACE

With three devices on the board, 9 control lines are required. To simplify interface to an 8 bit microprocessor, the $\overline{INC}$ lines for all three parts were connected to the same pin.

The pin configuration used for interface to the 6502 microprocessor system is as follows:

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
NC	$\overline{INC}$	$\overline{CS}_1$	U/$\overline{D}_1$	$\overline{CS}_2$	U/$\overline{D}_2$	$\overline{CS}_3$	U/$\overline{D}_3$

#1 = Volume
#2 = Bass
#3 = Treble

To move the wiper of a given pot, that pot's $\overline{CS}$ is brought low, the U/$\overline{D}$ for the appropriate pot is asserted H or L depending on the direction of wiper movement, and $\overline{INC}$ is toggled. For example, to increase the volume the following two patterns are alternated to the port connected to the E²PREAMP.

NC	$\overline{INC}$	$\overline{CS}_1$	U/$\overline{D}_1$	$\overline{CS}_2$	U/$\overline{D}_2$	$\overline{CS}_3$	U/$\overline{D}_3$
1	0	0	1	1	1	1	1
1	1	0	1	1	1	1	1

Note that $\overline{CS}$ has been selected, U/$\overline{D}$ set to 1 and $\overline{INC}$ toggled. Bass and treble settings are altered in a similar manner.

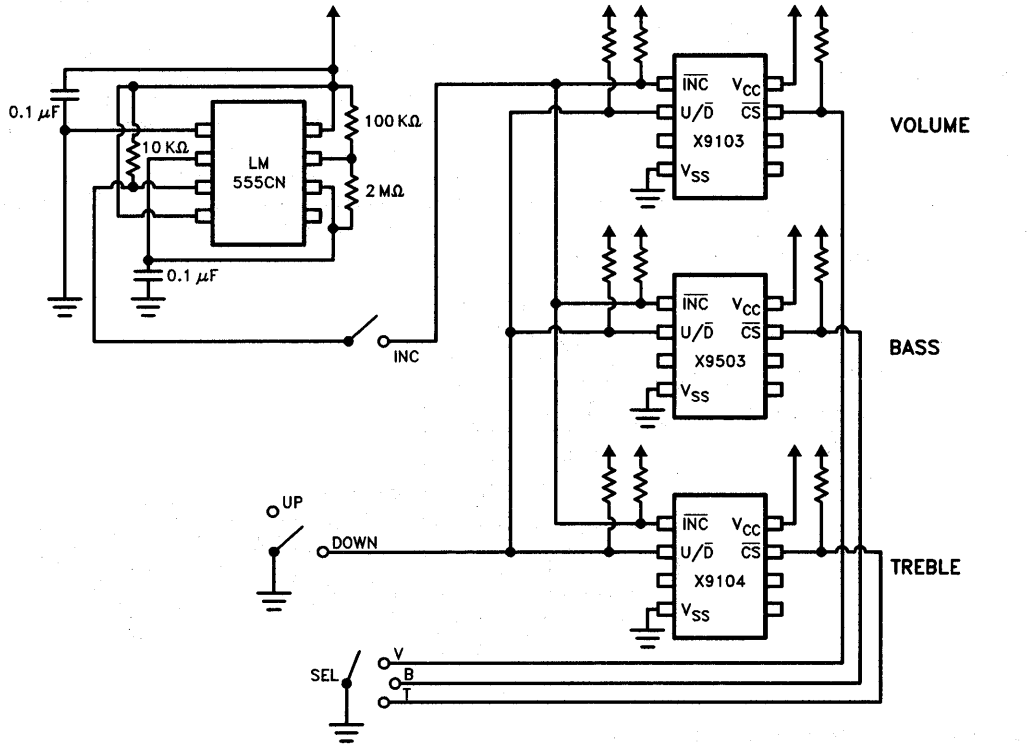

Figure 11: Switch Network for Manual Operation

The microprocessor system used in the lab consists of a 6502 based keyboard monitor. The controlling program scans the keyboard for a recognized ASCII character which transfers control to the specified subroutine. For any given input, the appropriate increment is toggled 10 times before returning to the controlling program.

An example of a volume, bass, or treble adjusting program follows:

```
      LDX  #00        Load counter with zero
0333  LDA  0006       Load accumulator with first
                        pattern
      STA  A000       Output pattern
      JSR  ED2C       5 ms wait
      LDA  0007       Load 2nd pattern
      STA  A000
      JSR  ED2C
      INX
      CPX  0008       Compare counter to 10
      BNE  0333
      RTS
```

In addition to the adjustment subroutines, an initialization subroutine can also be called up. This subroutine sets the volume to zero and bass and treble to 50%. This is used to reset the controls. It would be used only during installation of the system.

This first section of the one time initialization program sets all pots to zero.

```
      LDX  #00        Load counter with zero
0111  LDA  0000       Load accumulator with first
                        pattern (80h)
      STA  A000       Output pattern
      JSR  ED2C       5 ms wait
      LDA  0001       Load 2nd pattern (C0h)
      STA  A000
      JSR  ED2C
      INX
      CPX  0008       Compare counter to 100
      BNE  0111
```

This section sets the bass and treble pots to 50% and returns control to the controlling routine.

```
      LDX  #00        Load counter with zero
012C  LDA  0003       Load accumulator with first
                        pattern (85h)
      STA  A000       Output pattern
      JSR  ED2C       5 ms wait
      LDA  0004       Load 2nd pattern (F5h)
      STA  A000
      JSR  ED2C
      INX
      CPX  0005       Compare counter to 50
      BNE  0333
      RTS
```

OPERATION AND PERFORMANCE

The E²PREAMP circuit operates much like many sophisticated home stereo systems today. All controls are digital switches—in this case, a keyboard for demonstration purposes only. There are no moving parts beyond the switches, and the entire system is relatively free from problems with vibration or jarring (potential hazards in mechanical pot systems).

Keys 1 through 6 on the keyboard represent the up down controls for the circuit. By depressing 1, the volume is increased by 10 steps. Key 2 decreases volume in the same way; 3 is treble up; 4 is treble down; 5 is bass up; 6 is bass down. The I key calls the initialization routine. Beyond allowing control of step size and the auto zero or initialize function, the present system does not take advantage of the versatility of microprocessor control.

Performance of the system was nearly identical to the same circuit with mechanical potentiometers. The X9MME is quiet to −65 dB below a 1V signal, which is fair for audio quality devices. For audiophile quality, this number should be around −120 dB, but in car stereo or communication equipment applications this device works adequately.

Aside from the obvious advantage of a lack of moving parts, the ability to choose step size in adjusting the controls has shown to be the most useful added feature. Ten steps per adjustment proved to be an easy value with which to work.

Having demonstrated the ability of the X9MME to replace mechanical potentiometers in analog circuits, more complex circuits may now be considered. With microprocessor control, advanced circuit design and digital control simply becomes an extension of the principles discussed so far.

Microprocessor control of this and other analog circuits is simple when utilizing a digitally controllable potentiometer. The gain of the entire circuit, or the boost or cut of a given frequency range is instantly alterable via microprocessor commands. Once control is assumed by the microprocessor, any parameter of the analog circuit that is controllable by a potentiometer is available to the programmer.

For example, the graphic equalizer/spectrum analyzer combination discussed earlier can easily be automated once microprocessor control is assumed. By controlling the position of potentiometers that control the gain of the individual equalizer bands, the system frequency response can be calibrated to any room or listening environment. Here is

just one scenario: A "Calibration" button is depressed on the equalizing circuit. This activates a "pink" noise generator which sends a short burst of sound to the system. The spectrum analyzer in the system then decides which frequencies require adjustment, changes the positions on the appropriate potentiometers, and the system is calibrated. No sliders need to be adjusted; no separate (and expensive) spectrum analyzer; moreover, a relatively unsophisticated user can now perform an accurate environmental calibration of the system.

A simpler version of an auto calibration circuit could be incorporated into home and car stereos as a one time only installation adjustment. The scenario would be as follows. When a car stereo is first installed, the installer would push the calibration button on the back of the unit. This would adjust a compensation circuit, separate from the main tone controls. The settings would then remain in the nonvolatile memory of the digital pots until the system were upgraded or installed into another car. Thus the same unit would be customized for different speakers, different amplifiers, and even different auto interiors.

X9MME ADVANCED FEATURES

The Xicor device utilized in this design is suitable for audio applications, but it is a general purpose device that may be even better suited for other analog applications.

The X9MME has 99 steps across its range. In most audio applications, this high resolution is inaudible. However, when used in auto zero and balancing circuits, this resolution is invaluable.

The device's nonvolatile memory may be of limited use in some of the applications mentioned here, since a listener may not want to retain previous audio settings. But when used in a once-only calibration circuit, the nonvolatile memory eliminates any need for preventing a customer from changing the factory settings of a mechanical potentiometer. In a television cable decoder, for example, potentiometers abound. If cable companies used nonvolatile digital potentiometers in place of mechanical pots, the incessant headache of having to make adjustments because of jarred equipment or tampering could be eliminated.

The X9MME's convenient packaging and inherent digital control characteristics can be used to advantage on the assembly line. Manufacturing of devices requiring manual adjustment of potentiometers is always limited by the speed of the laborers and equipment used to set the pots. In addition, units often must remain partially assembled, or allow access holes for screwdriver adjustment of pots. The X9MME's conventional 8 pin DIP package can be automatically inserted with handlers used for other DIP devices, and trimmed to an appropriate value with an assembly line computer or by an internal microprocessor.

CONCLUSION

Microprocessor control of analog circuits is now easier than ever. The X9MME from Xicor is more than a simple DAC. Not only can this device be used as a precision voltage source, it can replace any resistive element in nearly any analog circuit. Without altering existing analog circuit designs, the designer now has the ability to manipulate analog circuit functions with the digital potentiometer as his control element.

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4. Stremler, Ferrel G., *Introduction to Communication Systems,* Reading, MA: Addison-Wesly Publishing Co., 1982; pp. 93.
5. National Semiconductor Corp., "Product Data Sheet, LMC835", April, 1984.
6. Toshiba Corp., "Product Data Sheet, TC9169AP-TC9170AP" June 1985.

Application Brief

NONVOLATILE DATA INTEGRITY: INADVERTENT WRITE/STORE ELIMINATION

By Applications Staff

Xicor's nonvolatile memory products are backed by designed-in protection features which ensure data integrity. These include:

- **Onboard V_{CC} Sensor**
  All operations inhibited when $V_{CC} \leq 3.0V$.
- **Noise Filter**
  A feature which blocks noise spikes on control lines.
- **Orderly Power Transition**
  The device will not self-generate inadvertent write/store operations.
- **Write/Store Inhibited Control Pins**
  Multi-pin write/store command signal requirements provide both data security *and* design flexibility.

New Design Features

- Software Write Protection
- Previous Recall Latch
- Command Sequence

With Xicor nonvolatile memories, data is maintained through power-on, power-off, power-down, system crash, and the entire range of system conditions when some simple design rules are observed. Often nonvolatile system designers are frustrated by inadvertent system command signals during power-up and power-down operations. Being nonperiodic in nature, these elusive culprits can lead the designers to the false conclusion that the memory device is malfunctioning. This, however, is rarely the case. The system is more often sending an unintended write/store command. This problem can be easily resolved as shown in this application brief.

GIGO[1] Going to Sleep

Just as a person falling asleep at the wheel can inadvertently command his vehicle into an undesirable situation, digital systems transitioning from normal operation to a power-off state or vice versa can distribute random data, addresses, and control signals along the way.

Since Xicor nonvolatile memories accurately and reliably store data as instructed, data stored at power-down will be impeccably retained and available upon power-up. (That's nonvolatile GIGO.)

Protection-Conscious Design

Data integrity is a major criterion with Xicor products and several superb features were designed into Xicor's memories to ensure it.

- **V_{CC} Sensor**
  An onboard sensor establishes a threshold supply voltage of 3.0V below which write operations on E^2PROMs and store operations on NOVRAMs are blocked. Above this voltage, write and store operations are available and therefore must be protected from unplanned instructions.
- **Orderly Supply Transitions**
  As a system powers up or down, the possibility of unintentional, internally generated control signals increases dramatically. The Xicor nonvolatile memory family has designed-in protection to eliminate self-generated write/store commands.
- **Noise Filter**
  An additional feature designed into Xicor's E^2PROM family is a noise filter to prevent glitches on the $\overline{WE}$ line from initiating a write cycle. This feature filters pulses of less than 20ns duration insuring noise spikes are not misconstrued as write commands.

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- **Write/Store Inhibit Control Pins**
  Xicor nonvolatile memories require combinational control pin conditions in order to execute a write/store command. By disallowing any one of the required pin conditions, the user can prevent unplanned nonvolatile data changes so that data integrity is maintained.

Write/Store Pin Conditions

$\overline{\text{ARRAY RECALL}}$[2]	$\overline{\text{STORE}}$	STORE CAPABILITY
X	H	STORE OPERATION DISABLED
L	X	ARRAY RECALL BLOCKS STORE INITIATION (SEE FOOTNOTE 2)
H	L	STORE OPERATION EXECUTED[3]

Figure 1: X2200 NOVRAM Family

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	WRITE CAPABILITY
X	X	H	($\overline{\text{WE}}$) WRITE INHIBIT*
X	L	X	($\overline{\text{OE}}$) WRITE INHIBIT
H	X	X	($\overline{\text{CE}}$) WRITE INHIBIT
L	H	L	WRITE OPERATION EXECUTED[3]

* Hard to control during power cycling.

Figure 2: E²PROM Family

External Hardware Implementations

Solution I—"Hold-Low" Protection

The simplest solution is to pull the $\overline{\text{OE}}$ (or ARRAY RECALL) to a logic "0" whenever the supply voltage is below the (5.0-10%) system threshold.

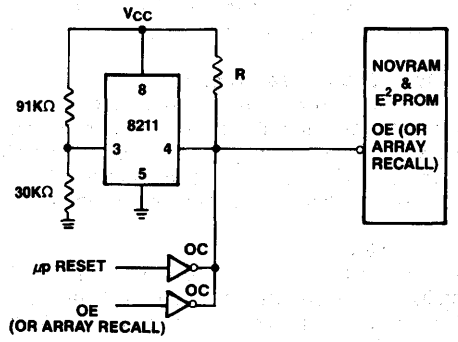

Figure 3: "Hold-Low" Protection

The Intersil[4] ICL 8211 programmable voltage reference is an inexpensive 8-pin mini DIP which will sense a selected voltage threshold and output a logic "0" when the supply is below that threshold. Conversely, as the sensed voltage rises above the selected threshold, the 8211 outputs a logic "1" following its supply voltage level.

Solution II—"Hold-High" Protection

The second method of data protection during power supply transitions is to keep the NOVRAM $\overline{\text{STORE}}$ pin (or the $\overline{\text{WE}}$ and/or $\overline{\text{CE}}$ pins in the E²PROM family) near the power supply voltage. By preventing the low condition of these pins which is necessary for a write or store operation, inadvertent stores will be eliminated.

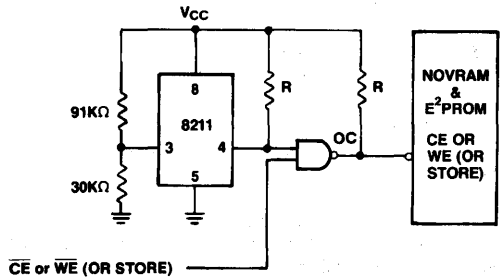

Figure 4: "Hold-High" Protection

The graph in Figure 5 shows the performance of the Intersil ICL 8211. The top plot is a sawtooth which is connected to "5V supply" as shown in the Solution I and Solution II schematic diagrams. The bottom plot is the output of the ICL 8211. Note that when the supply is above 4.50V, the ICL 8211 output tracks it at logic "1". When the supply sawtooth is below 1.56V, the ICL 8211 output tracks the power supply. However, since the Xicor memory family has internal protection inhibiting write/store operations when V_{CC} is below 3V, no inadvertent write/stores will occur in this range. In the critical range between 3V, where internal protection stops, and 4.5V, where normal operation begins, the ICL 8211 insures a 0V output.

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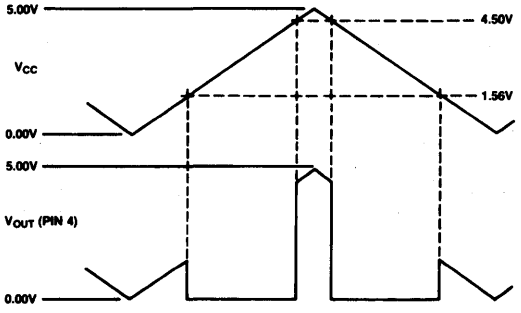

Figure 5: Intersil ICL 8211 Programmable Voltage Reference/Supply and Output Waveforms

As an alternate approach to the 8211, some designers may prefer to incorporate the SGS L487. This device is a 500 mA precision 5V voltage regulator which includes an open collector power-on, power-off reset output pin, which can protect the nonvolatile memories just as the 8211 does. The timing diagram in Figure 6 shows the voltage on this reset output pin as the supply voltage transitions through power-up and power-down.

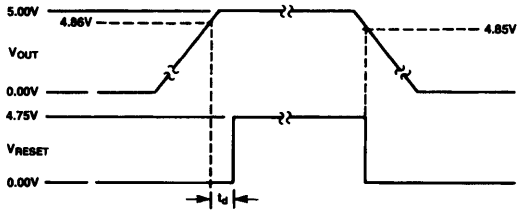

Figure 6: SGS L487 Precision Voltage Regulator/Output and Reset Waveforms

New Protect Features

Serial Device Protection X2444

A Previous Recall latch and Write Enable latch have been incorporated in the X2444 Serial NOVRAM.

Upon power-up, both latches will be in the reset state. Both latches must be set in order to enable either a write RAM operation or store to E²PROM operation.

A recall operation copies data from the E²PROM array into the RAM array. This operation places known data in all RAM locations and sets the previous recall latch. This prevents the user from inadvertently writing one word to RAM and performing a store operation with unknown data in all other locations.

The WREN instruction sets the Write Enable latch, enabling (if the Previous Recall latch is set) write and store operations. The WRDS instruction resets the latch, disabling write and store operations.

Therefore, total data integrity can be maintained through the use of software commands. The device is inherently protected during power-up and, through proper software control, is protected during power-down.

X2404 Serial E²PROM

Due to the nature of the software protocol involved in writing to the X2404, inadvertent stores are highly unlikely. During power-up or power-down the possibility of the bus duplicating the start condition, slave address and transmitting data successfully is so remote as to be unmeasurable.

Software Write Protection

Future E²PROM products will contain a register which is accessible through a software sequence algorithm. This feature provides the user control in selecting the level of write protection required by their application. Refer to the X28256 data sheet for details.

Figure 7 indicates the write protection features incorporated in all Xicor products.

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GENERIC DEVICE TYPE	V_{CC} SENSE	NOISE FILTER	SELF-GENERATE PROTECT	INHIBIT CONTROL	PREVIOUS RECALL	SOFTWARE PROTECTION	COMMAND SEQUENCE
X2201A	X	X	X	X			
X2210	X	X	X	X			
X2212	X	X	X	X			
X2001	X	X	X	X			
X2004	X	X	X	X			
X2444	X	X	X	X	X		
X2804A	X	X	X	X			
X2816A	X	X	X	X			
X2816B	X	X	X	X			
X2864A	X	X	X	X			
X2864B	X	X	X	X			
X2864H	X	X	X	X			
X28256	X	X	X	X		X	
X28C256	X	X	X	X		X	
X2404	X	X	X	X			X
X24C04	X	X	X	X			X
X24C16	X	X	X	X			X

Figure 7: Product Protection Matrix

Footnotes

[1] GIGO is an acronym popular in the computer world for "Garbage In Garbage Out".

[2] ARRAY RECALL blocks all control inputs but does not halt a store in process.

[3] These are the *only conditions* allowing nonvolatile data change.

[4] See Intersil ICL 8211, ICL 8212 Programmable voltage reference data sheet in Intersil Data Book.

0027-4

Xicor®

Application Brief

REPLACING DIP SWITCHES WITH NONVOLATILE TECHNOLOGY

By Rick Orlando

One of the most prevalent applications for small nonvolatile memories is that of replacing DIP switches. The advantages of the nonvolatile memories is clear. They take up less room, are easier to use, and lend themselves to automated board assembly. 256 bits of information, or the equivalent of 32, 8-bit DIP switches can be implemented in a single package.

Xicor's new X2444 Serial NOVRAM adds yet another feature—low cost. When coupled with the serial device's minimal interface requirements, the X2444 takes DIP switches head on, and is obviously the cost/performance leader. The purpose of this brief is to describe how easy it is to replace a DIP switch with an X2444 NOVRAM.

DIP Switch Interface

There are two common types of DIP switch interfaces.

I/O Port

The first uses an I/O port with internal pullup resistors. Figure 1a shows a typical circuit that could be used either with a single chip microcomputer or with an I/O port on a microprocessor bus. In either case, the internal pullups present a logic "1" to the input as long as the DIP switch is open. To use an X2444 Serial NOVRAM in the DIP switch socket, one only needs to tie pins 14, 15, and 16 of the 16-pin socket to V_{CC}.

One then plugs an X2444 part in the uppermost half of the socket, and the circuit becomes that shown in Figure 1b. V_{CC}, STORE, and RECALL are tied hard to 5 volts, so that all nonvolatile operations are controlled through software. The four interface lines from the X2444 are connected to the four least significant I/O lines of the port.

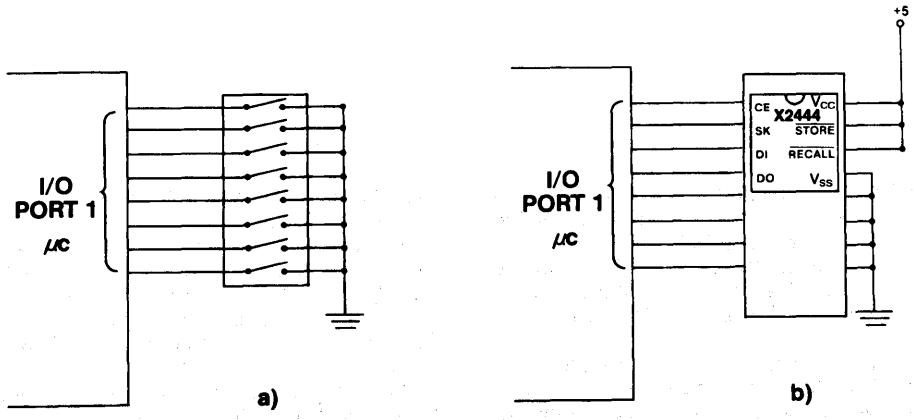

Figure 1. Microcomputer with Internal Pullups

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No Internal Pullups

The second type of interface uses ports which do not have internal pullups. In this instance, the X2444 can be plugged into the top section of the pullup resistor socket, with a jumper from pin 13 of the 16-pin site to ground, for the V_{SS} on the serial part. Again, V_{CC}, STORE, and RECALL are tied to +5V through the connections used for the resistor pack. The DIP switch socket simply remains empty. See Figure 2.

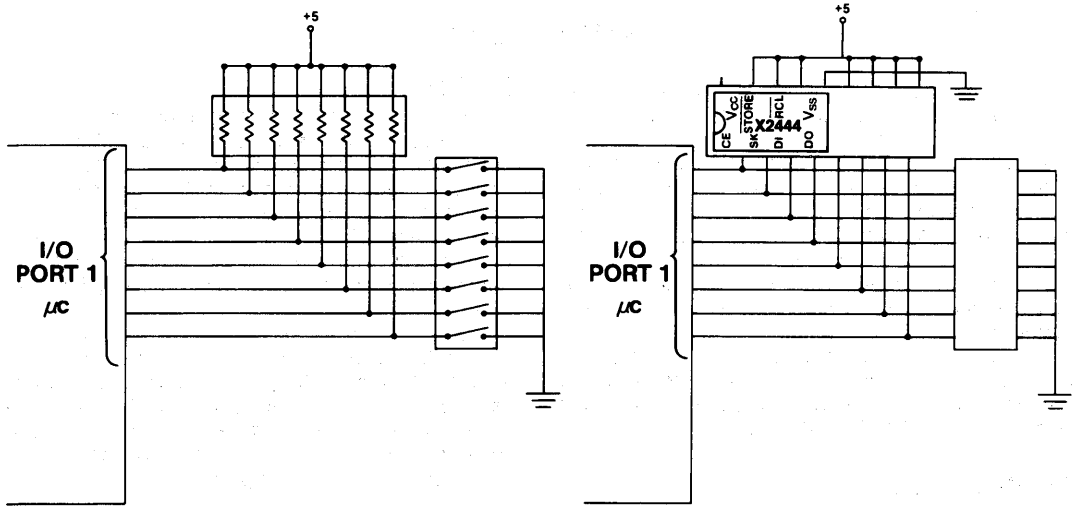

Figure 2. Microcomputer without Internal Pullups

Both of these implementations free up four more I/O lines to be used elsewhere. They also require the same software to drive the X2444.

Assume that the processor is a 6801 with the X2444 replacing a DIP switch. The procedure "INIT" initializes the port (see Section 1, "X2444 Driver Program for 6801").

Serial output is accomplished by loading the data to be output into the A Accumulator. A loop routine then shifts a bit into the carry, sets the serial data out (Data in for X2444) to either a "1" or "0" depending upon the state of the carry and toggles the clock. (See Section 2 Procedure "SHIFT1" of X2444 Driver Program for further details).

The serial input is performed by a loop which examines the state of the serial data in, (Data out for X2444) sets the carry accordingly, shifts the carry into the accumulator and toggles the clock. (See Section 3 Procedure "SHIFTIN" of X2444 Driver Program for further details).

The complete software is as follows, and it occupies about 100 bytes of code. As one can see, the X2444 is indeed a value replacement for DIP switches.

0006-2

```
;*****************************************************************************
;                          6801 X2444 DRIVER
;       ASSUME THAT PORT1 IS USED AS THE 2444 INTERFACE
;       PORT1'S REGISTERS ARE LOCATED AS FOLLOWS
;               DATA DIRECTION          HEX  0000
;               PORT                    HEX  0002
;                               PORT1           X2444
;       I/O 0                   SERIAL CLOCK    SERIAL CLOCK
;       I/O 1                   SERIAL OUT      SERIAL IN
;       I/O 2                   SERIAL IN       SERIAL OUT
;       I/O 3                   2444 SELECT     CHIP SELECT
;
;       COMMANDS ARE PASSED TO THE X2444 ROUTINE BY A PARAMETER IN THE
;       A ACCUMULATOR, WHILE THE ADDRESS IF NEEDED IS PASSED ON THE STACK
;       SERIAL DATA IN OR OUT USES THE TEMPORARY LOCATION TEMP1,
;       WHICH IS A SIXTEEN BIT WORSD.  THE X2444 COMMANDS ARE ENCRYPTED AS
;       FOLLOWS.
;       COMMAND CODE                    INSTRUCTION     OPCODE
;       0                               READ            1AAAA11X
;       1                               WRITE           1AAAA011
;       2                               RESET WRITE ENABLE  11111000
;       3                               STORE           11111001
;       4                               SLEEP           11111010
;       5                               SET WRITE ENABLE    11111100
;       6                               RECALL          11111101
; '1'S ARE USED INSTEAD OF DON'T CARE TO DISTINGUISH BETWEEN DATA AND
;  NON DATA OPERATIONS.
;*****************************************************************************

DIRECTION1      .EQU        00.
PORT1           .EQU        02.
TEMP1           .EQU        080H    ;RAM STORAGE FOR DATA
COUNT           .EQU        082H    ;COUNTER VARIABLE
DATUM           .EQU        084H    ;DATA STORAGE
ADDRESS         .EQU        086H    ;ADDRESS STORAGE
ERRORDATA       .EQU        088H     ;ERROR DATA

;*****************************************************************
;               PROCEDURE INIT
;       THIS PROCEDURE INITIALIZES THE X2444 INTERFACE
;*****************************************************************
INIT    LDAA    #1BH            ; B=1011, I/O 0,1 AND 3 OUTPUTS, 2 INPUT
        STAA    DIRECTION1      ; WRITE TO DATA DIRECTION REGISTER
        CLRA                    ;SET CE TO 0(INACTIVE), DOUT AND SK TO 0
        STAA    PORT1           ;AND STORE IN DATA PORT
        RTS                     ;

;*****************************************************************************
;       SHIFTER ROUTINE- SHIFT1
; THIS ROUTINE TAKES THE DATA IN THE A ACCUMULATOR AND CLOCKS IT MOST
; SIGNIFICANT BIT FIRST INTO THE X2444.  THE FLOW IS SHIFT A BIT, TOGGLE
; THE SERIAL OUTPUT(6801) ACCORDING TO STATE, AND TOGGLE SERIAL CLOCK
;*****************************************************************************

SHIFTOUT LDAB   #08.            ;LOAD THE BIT COUNT WITH 8
        STAB    COUNT           ;STORE IN COUNTER
SHIFT1  ROLA                    ;SHIFT BIT INTO CARRY BIT
        LDAB    #14H            ;WE SET DATA OUT TO ZERO, WHILE SETTING CHIP
                                ;ENABLE.  SERIAL CLOCK IS LOW.
        BCC     TRANS           ;IF BIT IS A ZERO, THEN TRANSMIT
        ORAB    #02H            ;IF IT IS A ONE, THEN SET DATA OUT
TRANS   STAB    PORT1           ;STORE THE DATA INTO THE PORT
        ORAB    #01H            ;AND SET THE CLOCK FOR A TRANSITION
        STAB    PORT1           ;BY WRITING A 1 TO SERIAL CLOCK
        ANDB    #1AH            ;KEEP THE DATA VALID, BUT SET SK TO ZERO
        STAB    PORT1           ;AND STORE IN THE PORT
        LDAB    #14H            ;TOGGLE CLOCK DOWN, SET DOUT TO 0, BUT KEEP
        STAB    PORT1           ;X2444 SELECTED
        DEC     COUNT           ; DECREMENT THE BIT COUNTER
        BNE     SHIFT1          ;IF COUNT IS NOT ZERO, TRANSMIT NEXT BIT
        ROLA                    ;ONE MORE ROTATE TO PRESERVE INSTRUCTION
        RTS                     ;RETURN FROM SUBROUTINE
;*****************************************************************************
;               SHIFTIN ROUTINE
; THIS SUBROUTINE SHIFTS IN 8 BITS OF DATA INTO THE A ACCUMULATOR FROM THE
; X2444. THE METHOD IS TO ENTER WITH THE CLOCK LOW, TOGGLE THE SERIAL CLOCK,
; EXAMINE THE INPUT DATA, AND SHIFT IT INTO THE A ACCUMULATOR.  THIS IS DONE
; 8 TIMES.  THE ROUTINE IS EXITED WITH THE CHIP DESELECTED, AND THE BYTE
; READ FROM THE CHIP IN THE A ACCUMULATOR
;*****************************************************************************
SHIFTIN LDAB    #8.             ;LOAD THE BIT COUNT
        STAB    COUNT           ;AND STORE IT IN THE COUNTER
                                ;AT THIS POINT THE X2444 SHOULD BE SELECTED
                                ;THEREFORE, WE DO NOT NEED TO SELECT CHIP
NEXT    LDAB    #04             ;MASK BIT FOR I/O 2 OF PORT
        BITB    PORT1           ;CHECK TO SEE IF INPUT IS A ONE OR ZERO
        CLC                     ;CLEAR THE CARRY
        BEQ     CLOCK           ;IF IT IS A ZERO, LEAVE CARRY AT 0
        SEC                     ;OTHERWISE SET CARRY TO LOAD INTO A
CLOCK   LDAB    #15H            ;SEND A CLOCK TO X2444,BUT KEEP CHIP SELECT HIGH
        STAB    PORT1           ;BY WRITING A 1 TO SERIAL CLOCK OUTPUT
SHIFT   LDAB    #14H            ;SET UP TO CLEAR CLOCK, BUT KEEP X2444 SELECTED
        STAB    PORT1           ;AND STORE
        ROLA                    ;ROTATE CARRY INTO LSB OF ACCUMULATOR A
        DEC     COUNT           ;DECREMENT COUNTER
        BNE     NEXT            ;IF NOT ZERO, THEN WE ARE NOT DONE, GET NEXT
        RTS                     ;AND RETURN FROM SUBROUTINE
```

Section 1

Section 2

Section 3

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```
;*************************************************************************
;       X2444 DRIVER ROUTINE
; IT IS ASSUMED THAT THE INSTRUCTION IS PASSED IN THE A ACCUMULATOR.  AN
; ADDRESS, IF NEEDED, IS PASSED ON THE STACK(CURRENT SP-2)
; DATA TO BE READ OR WRITTEN WILL BE HELD IN TEMP1
;*************************************************************************
DRIVE   CMPA    #0F8H           ;CHECK TO SEE IF IT IS READ OR WRITE
        BGE     NONDATA         ;IF NOT, THEN BRANCH AROUND
        TSX                     ;TRANSFER STACK TO INDEX REGISTER
        ORAA    2,X             ;THE ADDRESS SHOULD BE SP+2
        JSR     SHIFTOUT        ;OUTPUT THE INSTRUCTION
        ANDA    #04H            ;CHECK TO SEE IF IT IS A READ OR WRITE
        BNE     RD              ;IF AC3]=1, IT IS A READ

WRT     LDAA    TEMP1           ;IF IT IS A WRITE, GET THE FIRST BYTE
        JSR     SHIFTOUT        ;WRITE THE FIRST BYTE
        LDAA    TEMP1+1         ;GET THE SECOND BYTE
        JSR     SHIFTOUT        ;WRITE THE SECOND BYTE
        BRA     DONE            ;WRITE INSTRUCTION COMPLETE
RD      JSR     SHIFTIN         ;GET THE FIRST BYTE
        STAA    TEMP1           ;STORE IN TEMP1
        JSR     SHIFTIN         ;GET THE SECOND BYTE
        STAA    TEMP1+1         ;STORE IN TEMP1+1
        BRA     DONE            ;READ COMPLETE
NONDATA JSR     SHIFTOUT        ;OUTPUT THE INSTRUCTION
DONE    CLRA
        STAA    PORT1           ;DESELECT THE X2444 BY MAKING CS 0
        RTS                     ;RETURN FROM SUBROUTINE
;*************************************************************************
;                       MAIN INSTRUCTION ROUTINES- COULD BE MACROS
;*************************************************************************
;*************************************************************************
;       READ ROUTINE
; ASSUMES THAT THE ADDRESS IS IN THE A ACCUMULATOR, DATA IS LEFT IN X REGISTER
;*************************************************************************
READ    ASLA                    ;SHIFT THE ADDRESS 3 TIMES TO LINE IT
        ASLA                    ;UP WITH THE INSTRUCTION FIELD
        ASLA
        PSHA                    ;PUSH ADDRESS ON THE STACK
        LDAA    #087H           ;LOAD INSTRUCTION INTO A ACCUMULATOR
        JSR     DRIVE           ;PERFORM INSTRUCTION
        LDX     TEMP1           ;GET THE RESULT IN THE INDEX REGISTER
        PULA                    ;CLEAN UP THE STACK
        RTS                     ;AND RETURN
;*************************************************************************
;                               WRITE ROUTINE
; ASSUMES THAT THE ADDRESS IS IN THE A ACCUMULATOR, DATA TO WRITE IS IN THE
; X REGISTER.
; ALSO CALLS SET WRITE ENABLE LATCH ROUTINE(SWREN) TO ENABLE THE WRITE OPERATION
;*************************************************************************
WRITE   ASLA                    ;SHIFT THE ADDRESS 3 TIMES
        ASLA
        ASLA
        PSHA                    ;PUSH ADDRESS ONTO THE STACK
        JSR     SWREN           ;SET THE WRITE ENABLE LATCH
        LDAA    #083H           ;LOAD WRITE INSTRUCTION
        STX     TEMP1           ;STORE DATA IN TEMP1
        JSR     DRIVE           ;PERFORM INSTRUCTION
        PULA                    ;CLEAN UP STACK
        RTS
;*************************************************************************
RWREN   LDAA    #0F8H           ;LOAD THE INSTRUCTION
        JSR     DRIVE           ;AND EXECUTE
        RTS
;*************************************************************************
STORE   LDAA    #0F9H           ;LOAD THE INSTRUCTION
        JSR     DRIVE           ;PERFROM OPERATION
        RTS                     ;AND RETURN
;*************************************************************************
SLEEP   LDAA    #0FAH           ;LOAD THE INSTRUCTION
```

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Application Brief

USING $\overline{\text{DATA}}$ POLLING IN AN INTERRUPT DRIVEN ENVIRONMENT

By Rick Orlando

The use of interrupt driven system design has become increasingly popular in many applications. Interrupt driven systems usually can achieve higher performance and improved user friendliness. An interrupt driven system can perform a variety of tasks while waiting for a certain condition to occur, rather than constantly looping and waiting for the occurrence. Writing to E^2PROMs is no exception. Since the devices take a relatively long period to complete a Write Cycle, the system could perform a variety of tasks in the meantime.

$\overline{\text{DATA}}$ Polling was introduced on the X2864A to allow notification to the processor of Write Cycle completion. The manner in which it works is quite simple. The processor first writes a byte of data into the E^2PROM. Any subsequent reads to any location of the chip will produce the complement of the data last written (hence, the name $\overline{\text{DATA}}$ Polling) until the E^2PROM's internal Write Cycle is complete. At this point, reads to any location in the E^2PROM will result in the valid data at that location. It can be seen that one can simply write a byte, and then perform frequent compares of the data in the location just written. The data will not be correct until the chip has completed its internal Write Cycle, and the $\overline{\text{Data}}$ circuitry is disabled.

In applications where the processor does not have anything to do during the Write Cycle, the software can simply perform compare loops until the Write Cycle is complete, and then write the next byte. In applications which are more processing time limited, a test loop can be placed in the main program loop, which will check the status of a previous Write Cycle on each pass through the main or outermost software loop. Almost all microprocessor applications software has such a top level loop. $\overline{\text{DATA}}$ Polling is obviously adequate in these environments.

The interrupt intensive applications may not have a main control loop nor can they usually afford the processing time for the processor to sit and loop until the Write Cycle is complete. In these applications, it would be ideal if the Write Cycle completion notification could be interrupt controlled. Although it is not obvious, $\overline{\text{DATA}}$ Polling can be used in these applications as well.

It should be noted that the whole reason for Write Cycle notification is because the typical write times for the E^2PROMs are substantially shorter than the specified maximums. The magnitude of the delta between the typical and the maximum values determines the importance of the Write Cycle notification. One can easily see that if the maximum Write Cycle time and the typical were equal, one would only have to time a fixed interval for each Write Cycle, either from a software loop or a hardware timer. The hardware timer would generate an interrupt 10 msec after the Write Cycle was initiated, and the next byte could be written. Keep in mind that the discussion of write times for E^2PROMs are in terms of msec rather than the μsec in which the processor executes instructions. A few μsecs here or there are not important when compared to the Write Cycle time of about 10 msec.

$\overline{\text{DATA}}$ Polling does not require any additional hardware interface in order to be used. It is an exclusively software oriented method for determining Write Cycle completion. Even in an interrupt environment, no additional circuitry is required, since all of the interface to the chip occurs through the data and address bus.

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In order to use $\overline{\text{DATA}}$ Polling in an interrupt driven system, one only needs a time-based interrupt generator. This could be a programmable timer or even something as simple as an AC frequency interrupt. The key is that the processor does not check to see if the device has completed the Write Cycle until the interrupt occurs. The interrupt routine simply compares the data last written to the E^2PROM to the data coming from the E^2PROM. If the two match, the device can be written again. If not, the processor simply returns from the interrupt routine to where it was and continues processing until the next interrupt. The interrupt source is maskable which prevents the overhead of servicing the periodic interrupt during the intervals when a write has not been performed.

A programmable timer or counter is the most elegant solution. Figure 1 shows the hardware configuration of a typical system with the E^2PROM and the programmable timer on the bus. It should be noted that no unusual circuitry is needed from the E^2PROM socket, which preserves its usefulness as a truly universal socket. The timer interrupt output drives one of the processor's interrupt lines. Many systems already have such a timer on the bus, and as a result require no additional hardware changes to implement this method.

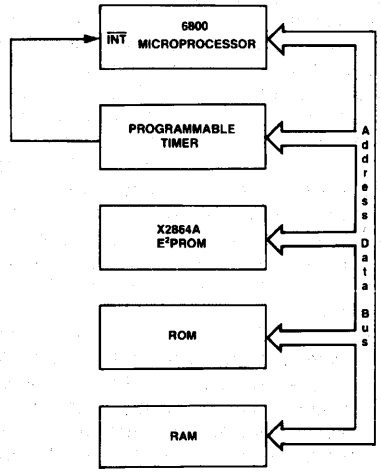

Figure 1: Hardware Configuration of a Typical System with the E^2PROM and the Programmable Timer on the Bus

The software implementation is rather simple. Figure 2 shows an example of how it might be done using a 6800 microprocessor and a simple timer. The timer control and data registers are mapped into the memory locations described in the initial header along with the temporary RAM variables, which are used to store the last data written and its address.

The write routine (WEEPROM) initially checks to see if the E^2PROM is ready to perform a write. If not, it simply exits with an error code to show that the write has not taken place. If the write is performed, the timer is loaded with the initial count for 4 msec, and the timer interrupt is enabled. The processor then goes off and performs its normal duties until the interrupt takes place. At that point, the interrupt routine (CKEEP) is entered. It first checks for the proper data that was written to see if the write is complete, using $\overline{\text{DATA}}$ Polling. If it is, the ready flag is set, and the routine is exited. If not, the counter is loaded with a smaller increment, such as 500 μsec until the chip's Write Cycle is completed. This essentially allows the majority of the Write time to pass (4 msec) before the processor checks at the more frequent interval of every 500 μsec.

Five hundred μsec has been chosen in this example for the interrupt granularity. The value used for a particular application should be chosen based upon the actual system requirements.

One can see that this implementation is rather easy and can be performed with hardware that already may exist in the system. By using the periodic interface approach, the system has the advantage of using an interrupt driven write algorithm, while maintaining only a software interface to the E^2PROM. Most of the "bookkeeping" sections of the example code are the same as one would use with any method of write termination notification. The end result of using $\overline{\text{DATA}}$ Polling in an interrupt environment is optimization of the Write Cycle period as well as preservation of the pinout of the universal 28-pin socket for expansion through the 256K bit level for E^2PROMs.

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```
PAGE -   1  DATA_COD
File: :DATA_CODE.TEXT              CODE FOR DATA POLLING IN INTERRUPT ENVIRONMENT, 6800 VERSION

0000:                                      .PROC DATA_CODE
Current memory available:    4380
0000:                      ;*************************************************************************
0000:                      ;       SAMPLE CODE FOR USING DATA POLLING IN INTERRUPT ENVIRONMENT
0000:                      ;   THIS CODE SHOWS AN EXAMPLE OF HOW TO USE DATA POLLING IN A
0000:                      ; INTERRUPT DRIVEN WRITE MODE
0000:                      ;*************************************************************************
0000:                      ;                    MEMORY LOCATIONS
0000: 0100                 TIMER   .EQU    0100H   ;LOCATION OF TIMER DATA REGISTER(COUNT DOWN VALUE)
0000:                                              ;16 BIT VALUE(2 BYTES)
0000: 0102                 CTIMER  .EQU    0102H   ;TIMER CONTROL REGISTER
0000: 0103                 LASTA   .EQU    0103H   ;RAM LOCATION FOR LAST WRITTEN DATA
0000: 0104                 TEMP    .EQU    0104H   ;RAM LOCATION FOR LAST ADDRESS WRITTEN
0000: 0106                 ERROR   .EQU    0106H   ;ERROR FLAG FOR WRITE
0000: 0107                 READY   .EQU    0107H   ;MEMORY READY FOR NEXT WRITE FLAG
0000: 0108                 CONFIG  .EQU    0108H   ;TIMER CONFIGURATION BYTE
0000:
0000:                                  .ORG 0F000H
F000:                      ;*************************************************************************
F000:                      ;                    EEPROM WRITE ROUTINE
F000:                      ;   THIS ROUTINE WRITES A BYTE OF DATA PASSED IN THE A ACCUMULATOR INTO
F000:                      ; THE EEPROM AT LOCATION POINTED TO BY THE VALUE IN THE X INDEX REGISTER.
F000:                      ; THE ROUTINE THEN INITIALIZES THE DATA IN THE COUNTER TO 4096, SINCE THE TIMER
F000:                      ; COUNTS AT A 1 MHZ FREQUENCY.  THIS WILL TIME OUT THE INITIAL 4 MSEC OF THE WRI
F000:                      ; WRITE CYCLE.  THE ROUTINE THEN ENABLES THE INTERRUPTS AN RETURNS CONTROL TO
F000:                      ; THE CALLING ROUTINE
F000:                      ;*************************************************************************
F000: C6 00                WEEPROM LDAB    #00H    ;COMPARE TO SEE IF THE MEMORY IS READY FOR WRITE
F002: F1 0107                      CMPB    READY   ;CHECK MEMORY LOCATION READY
F005: 27 **                        BEQ     WRITE   ;IF READY THEN WRITE
F007: C6 00                        LDAB    #00H    ;OTHERWISE SET THE ERROR FLAG
F009: F7 0106                      STAB    ERROR   ;AND STORE IT IN ERROR
F00C: 20 **                        BRA     EXIT    ;AND EXIT
F00E: A7 00                WRITE   STAA    0,X     ;WRITE THE DATA IN A TO LOCATION X
F010: B7 0103                      STAA    LASTA   ;STORE DATA IN RAM AT LASTA
F013: FF 0104                      STX     TEMP    ;AND STORE LOCATION IN EEPROM AT TEMP
F016: C6 10                        LDAB    #10H    ;LOAD THE FIRST BYTE OF 4096 HEX INTO B ACCUMULATOR
F018: F7 0100                      STAB    TIMER   ;WRITE TO TIMER DATA REGISTER
F01B: C6 00                        LDAB    #00H    ;LOAD THE SECOND BYTE OF 4096 HEX
F01D: F7 0101                      STAB    TIMER+1 ;STORE IN THE LSB OF TIMER REGISTER
F020: F6 0108                      LDAB    CONFIG  ;GET THE TIMER INITIALIZATION CODE
F023: F7 0102                      STAB    CTIMER  ;STORE IT IN THE TIMER CONTROL REGISTER
F026: 0E                           CLI             ;CLEAR INTERRUPT MASK TO LET TIMER INTERRUPT
F027: 39                   EXIT    RTS             ;RETURN FROM SUBROUTINE
F028:                      ;*************************************************************************
F028:                      ;              CHECK EEPROM ROUTINE
F028:                      ;   THIS ROUTINE CHECKS TO SEE IF THE EEPROM IS DONE.  IT IS ENTERRED
F028:                      ; EVERY TIME THAT THE INTERRUPT IS GENERATED FROM THE TIMER.  IT COMPARES
F028:                      ; THE DATA AT LOCATION TEMP IN THE EEPROM WITH THE DATA THAT IS STORED IN
F028:                      ; LASTA LOCATION IN RAM.  IF THE COMPARISON FAILS, THEN THE EEPROM IS NOT
F028:                      ; DONE  YET , AND THE TIMER IS RESET TO TIME 1/2 MSEC(OR 512 USEC).  THE
F028:                      ; ROUTINE IS THEN EXITED.
F028:                      ;*************************************************************************
F028: B6 0103              CKEEP   LDAA    LASTA   ;GET THE LAST DATA WRITTEN
F02B: FE 0104                      LDX     TEMP    ;GET THE ADDRESS FOR THE BYTE IN EEPROM
F02E: A1 00                        CMPA    0,X     ;COMPARE TO SEE IF THE WRITE IS COMPLETE
```

```
PAGE -   2  DATA_COD
File: :DATA_CODE.TEXT              CODE FOR DATA POLLING IN INTERRUPT ENVIRONMENT, 6800 VERSION

F030: 26 **                                BNE     REINIT  ;IF NOT EQUAL REINITIALIZE THE TIMER
F032: 86 00                                LDAA    #00     ;SET THE READY FLAG
F034: B7 0107                              STAA    READY   ;AND STORE IT IN READY
F037: 20 **                                BRA     RET     ;AND RETURN FROM SUBROUTINE
F039: 86 02                    REINIT      LDAA    #02H    ;LOAD THE FIRST BYTE FOR COUNTER
F03B: B7 0100                              STAA    TIMER   ;WRITE TO TIMER DATA REGISTER
F03E: 86 00                                LDAA    #00H    ;LOAD THE SECOND BYTE
F040: B7 0101                              STAA    TIMER+1 ;WRITE TO LSB OF TIMER DATA REGISTER
F043: 3B                       RET         RTI             ;RETURN FROM INTERRUPT
F044:                          ;*************************************************************************
F044:                              .END
```

```
SYMBOL TABLE DUMP
      CODE FOR DATA POLLING IN INTERRUPT ENVIRONMENT, 6800 VERSION

AB - Absolute     LB - Label      UD - Undefined    MC - Macro
RF - Ref          DF - Def        PR - Proc         FC - Func
PB - Public       PV - Private    CS - Consts       RS - Residents

CKEEP    LB F028:  CONFIG   AB 0108:  CTIMER
LASTA    AB 0103:  READY    AB 0107:  REINIT
WEEPROM  LB F000:  WRITE    LB F00E:

AB 0102:  DATA_COD PR -----:  ERROR    AB 0106:  EXIT     LB F027
LB F039:  RET      LB F043:  TEMP     AB 0104:  TIMER    AB 0100
```

Figure 2: Software Implementation for 6800 Microprocessor and a Simple Timer

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NOTES

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Application Brief

E²PROM PROVIDES THE SOLUTION TO FIELD ALTERABLE SOFTWARE

By Rick Orlando

The advent of the 5-volt E²PROM has brought about many changes in the manner in which the designer views his software. Such devices allow for in-field reprogrammability, which greatly reduces the cost and impact of software changes or upgrades. The 5 volt E²PROM allows the designer the capability to completely upgrade or change his software from a remote location rather than through the replacement of the system ROMs or EPROMs, a costly and inconvenient method at best. Complete infield programmability requires that the entire program store of the system be implemented in E²PROM. An alternative is a "hybrid" system.

A "hybrid" approach refers to a design which utilizes both EPROMs or ROMs in conjunction with E²PROMs to yield a design which features the best of both approaches: the low cost of a full ROM implementation, while maintaining the flexibility of a full E²PROM approach.

The secret to this approach is to analyze the software requirements of the end system from two distinct levels. That of the machine code routines which perform the simple tasks, and that of the higher level routines which call the lower level routines to perform an algorithm. The order in which the low level routines are called is determined by the higher level routines or program flow. This "Top-Down" programming approach is more efficient and structured, and is the basis for many high level languages. The fact that it can be used in machine language coding should not come as a surprise to designers, since the decomposition of a complex task into many simple tasks is quickly learned in programming, even if it is not called "structured programming" per se. The decomposition of the end task can sometimes lead to many different levels of program structure, but for the simplicity of discussion, this brief will limit itself to the most simple approach, that of two level program structure.

The lower level code consists of the machine dependent routines such as that required to fetch a character from an I/O link. The buffering of multiple characters from this link might also be a low level routine. The interpretation of the buffered character string will be implemented in the higher level code, since it simply calls the lower level routines and determines the action to take based upon their results.

A basic example is that of the executing of multiple character command entered by the operator from a keyboard. The lowest level routine simply gets a character from the keyboard if a key is depressed. The next level of the software "buffers" the input to make the system more "user-friendly". This routine looks at the input string, eliminates misplaced blanks or other characters, and forms a character string which the high level program can understand. As a result, the "parsing" task is broken into three distinct levels.

The first involves the inputting of a single character from the keyboard into a character buffer. The second level continually calls the first routine until an end-of-input character is detected (such as a Carriage Return). The top most level of the code takes the parsed command and determines if it is a valid command by searching a table of valid commands. If the command is valid, the address of the routine to execute is fetched out of the table, and the processor performs a jump. Most of the input processing is handled at the lowest level, thereby reducing the overhead in the outermost routine.

As more and more of the processing tasks are pushed "down" into low level routines, the main procedure in the high-level segment becomes very short and simple. In fact, it can be reduced to a simple list of jump-to-subroutine instructions. This structured approach not only eases the software development task, but it also minimizes the debugging time required for the software since it is built upon other routines which have already been debugged.

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If one completely decomposes the task to be performed by a particular segment of the systems main program, it becomes a list of procedure calls to lower level segments. This method lends itself very well to a system which can use E²PROM. Since the "outermost" program store is quite compact, it can be implemented in E²PROM while the majority of the machine code in the lower levels can be implemented in ROM or EPROM. Changes to the software then become as simple as changing the jump location in the E²PROM, and the order of execution of the lower level routines can be altered in such a manner.

Using this method, one can also reserve a section of the E²PROM for low-level "patch" alterations to the software. If a low level routine is found to be in error or needs updating, the new version of the machine code is loaded into the reserved section of the E²PROM. The jump instructions in the high level code in the E²PROM are simply changed to "jumps" to the new routine now residing in the E²PROM as opposed to the old routine in the ROM or EPROM. Figure 1 shows a typical memory map where the E²PROM is used to store the high-level routines which perform a variety of jump to subroutines to control the program flow. The low level machine language routines are stored in the EPROM as shown. Figure 2 shows how a patch is made to replace the old routine in EPROM called "PARSE" with a new version loaded into the E²PROM. The jump-to-subroutine addresses in the E²PROM are updated to point to the new routine in E²PROM. The actual update or "patch" can be performed remotely, thereby eliminating the need for in field EPROM replacements for both the remedying of software bugs as well as the upgrading of systems in the field to take advantage of new features or capabilities.

Since both the valid character and the valid command tables reside in the E²PROM, new entries can be made to allow for additional command selection. New command character strings are simply added to the valid command list. The low-level code for the new command can either be loaded into the E²PROM patch area or utilize routines which already exist in the ROM or EPROM. The appropriate address is appended to the new command string.

If an error is discovered in an existing command, the valid command list is updated to point to the new command routine which is loaded into the patch area of the E²PROM. Figure 3 depicts the memory map after such a change has been made.

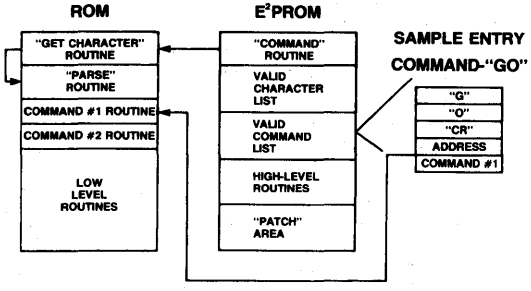

Figure 1: Memory Map Original Configuration

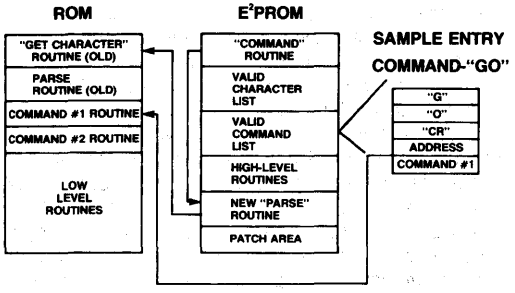

Figure 2: Memory Map After Routine Patch

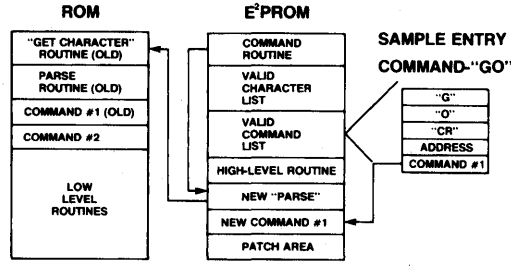

Figure 3: Memory Map After New Command Patch

Ultimate flexibility can be attained through a complete E²PROM design. It can also be shown that a minimal amount of E²PROM can add great flexibility to the system not only in terms of software alteration, but also in its intrinsic ability to store user alterable parameters such as configuration data. The actual ratio of EPROM to E²PROM must be determined based upon the systems' requirements. The advantage of the "hybrid" approach is that it requires that only the "top level" portion of the code be resident in E²PROM, and as such is usually limited to a series of procedure calls, which are very code efficient.

In the cases where the software is to be updated remotely, perhaps through the use of a modem, certain factors must be considered. The key point is that while the processor is executing programs in the E²PROM, it is unadvisable to write into that particular device. The reason for this is that while the device is performing the write cycle, any reads, such an opcode fetch, will result in a high impedance bus.

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The important issue is that the download of the new code must not reside in the E²PROM to be modified.

This can be accomplished in two different ways. The first implements the download program segment in the low level ROM or EPROM. In this case, the actual instructions will be present from the memory throughout the download sequence. Figure 4 shows such an approach where the download software is kept in the ROM. This routine writes the new bytes into the E²PROM and then enters a software loop to time out the E²PROM write cycle.

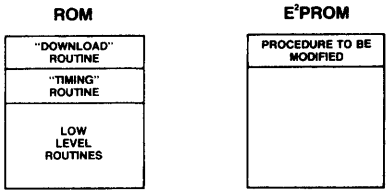

Figure 4: Memory Map-Download and Timing Resident in ROM

In some applications, this method may not be adequate, especially if the actual download routine is to be modified. In these cases, this program segment must be stored in the E²PROM, and hence, cannot be directly executed from the E²PROM to be modified. In this situation, a possible approach is to copy the download program segment from the E²PROM into RAM. The program then jumps to the RAM location, where the copy of the old code resides. This RAM routine loads the new program segment into the proper E²PROM locations, timing out the necessary E²PROM write cycle. Once the download is complete, the program executing out of the RAM then jumps back to the main program, and the download routine section of the E²PROM will contain the new code. Figure 5 shows the various stages of this operation in terms of the contents of the various memories and the program execution flow.

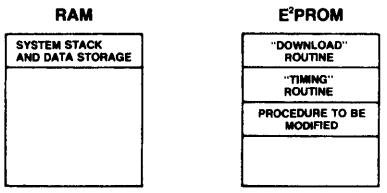

Figure 5a: Memory Map Prior to Download

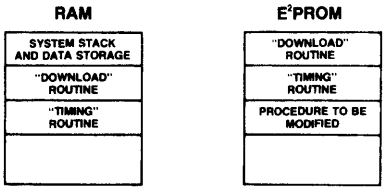

Figure 5b: Memory Map Download Routine Transferred to RAM

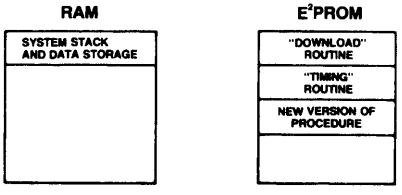

Figure 5c: Memory Map RAM Erased After Transfer Complete

As one can see, the "hybrid" approach to software design, utilizing a combination of both E²PROMs and ROMs or EPROMs, can result in a system which exhibits the advantages of the field alterability of E²PROMs. As the cost of the development and maintenance of the system software becomes more dominant in the overall cost of the system, such methods as those presented in this brief will become more commonplace in system design.

0008-3

8

NOTES

Xicor®

Application Brief

"t_{DV}"—WHAT IS IT?

By Richard Palm

E²PROMs, RAMs and EPROMs all being memory devices have similar specifications. However, one of the specifications unique to E²PROMs is t_{DV} (Data Valid Time).

The E²PROM requires a relatively lengthy period of time to tunnel charge onto or off of the floating gate to complete the write cycle. This time is specified as t_{WC}. In order to more closely emulate RAM write timing, Xicor introduced "self timed" write operations. Xicor E²PROMs latch the address on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and latch data on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. The falling edge of the write operation not only latches the address of the byte (or page) to be written but also starts a number of internal timers that control the programming cycle. In page mode, subsequent $\overline{WE}/\overline{CE}$ falling edges will restart the timers. But it is these timers that require specifying t_{DV}.

In most microprocessor based systems, t_{DV} can be ignored because t_{WP} will be less than t_{DV}. However, in applications employing slower microprocessors and microcontrollers t_{WP} might be quite long. The actual internal programming cycle could begin before either $\overline{CE}$ or $\overline{WE}$ returned high, thereby missing valid data even though t_{DS} was met.

Once the internal timers initiate the programming cycle, the I/Os will be disabled. Therefore, valid data must be present on the bus before the I/Os are disabled. As an example, refer to Figure 1 illustrating the sequence of events.

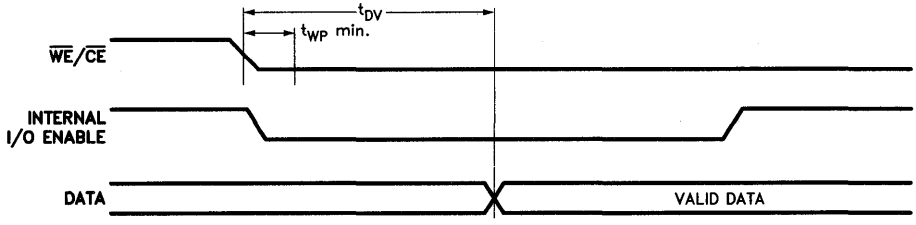

Figure 1: External/Internal Timing

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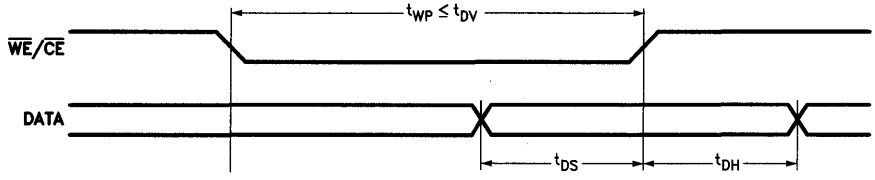
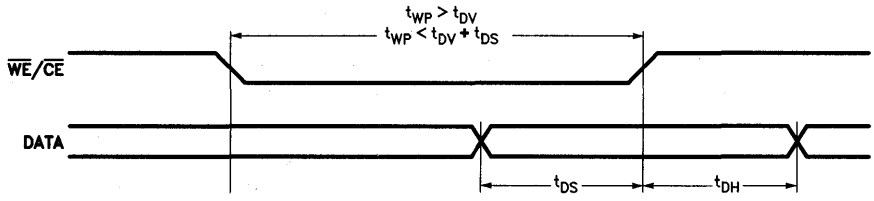
t_{DV} is the maximum time to elapse from the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever occurs first) before valid data have to be presented to the E²PROM.

How does this impact your design? The following timing diagrams cover the three possibilities. Notice that in all the examples t_{DH} must still be met.



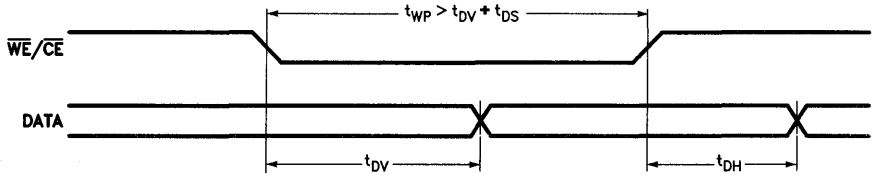
0060-2

Example 1: If t_{WP} is equal to or greater than t_{WP} min but less than t_{DV}, then t_{DS} and t_{DH} must be met.



0060-3

Example 2: If t_{WP} is greater than t_{DV} but less than t_{DV} plus t_{DS}, then t_{DS} and t_{DH} must be met.



0060-4

Example 3: If t_{WP} is greater than t_{DV} plus t_{DS}, then t_{DV} and t_{DH} must be met.

In summary, the data must be valid on the bus for the worst case timing parameters; whether that is t_{DV} or t_{DS} and always valid for t_{DH}.

Glossary

t_{DV}	Data Valid Time
t_{WC}	Write Cycle Time
t_{DS}	Data Setup
t_{WP}	$\overline{WE}$ Pulse Width
t_{DH}	Data Hold

Xicor

Understand your application in choosing NOVRAM, EEPROM

Richard Orlando, Xicor Inc., Milpitas, CA

As appeared in EDN Magazine

May 12, 1983

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Understand your application in choosing NOVRAM, EEPROM

Examining how NOVRAMs and EEPROMs serve various applications illustrates the memory devices' capabilities and simplifies device selection.

Richard Orlando, Xicor Inc

If your system design calls for electrically erasable nonvolatile data storage, you can simplify the selection of semiconductor memory for that task by choosing from among four basic types—NOVRAM, EEPROM, EAROM and battery-backed CMOS RAM. Assuming that you've examined the system-level tradeoffs among these memory types (EDN, April 14, pg 135) and have narrowed your choice to the first two, use the information presented here to understand the detailed tradeoffs and design considerations underlying NOVRAM and EEPROM use. In some application classes, either memory type functions adequately; in others, you have a clearcut choice. And in still others, consider taking advantage of both—an approach that often results in cost reductions and enhanced features.

NOVRAMs use multiple technologies

First, however, understand how each memory type works. Nonvolatile static RAM (NOVRAM) combines two memory technologies on one monolithic chip. In **Fig 1,** the NOVRAM shown contains 1k bits of static RAM and 1k bits of electrically erasable PROM (EEPROM). The device comprises cells that in turn each contain one cell of each memory type, rather than housing two separate memory arrays (see **box,** "Anatomy of a NOVRAM cell").

In this NOVRAM, data gets read and written exactly as in a standard static RAM. In addition, the $\overline{\text{Store}}$ signal transfers each RAM cell's data into a shadowing EEPROM cell; EEPROM-stored data gets reloaded into the RAM via the $\overline{\text{Recall}}$ signal. Note that the EEPROM-cell portion is accessible only through the RAM portion.

One of this device type's most powerful features is its ability to transfer the entire RAM contents into nonvolatile storage in one operation, initiated by bringing the TTL-compatible $\overline{\text{Store}}$ LOW. The operation takes less than 10 msec, and once data is stored in this manner, only another store operation can alter it—even if the chip loses power.

Generating $\overline{\text{Store}}$ in the event of a power failure therefore saves the RAM contents, subject only to power remaining on the chip for the next 10 msec. RAM data can also be changed without disturbing the shadowing EEPROM, allowing the system to manipulate two separate groups of data.

EEPROMs offer greater density, fewer features

EEPROM, your other major memory choice, resembles UV-erasable EPROM. Unlike EPROM, however, it can be written electrically in circuit; it needs no prior erasure by exposure to ultraviolet radiation.

First-generation EEPROMs are merely electrically

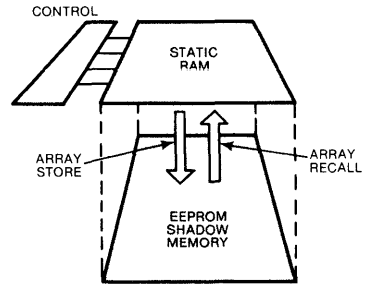

Fig 1—Nonvolatile static RAM (NOVRAM) *is organized so that each static-RAM bit is overlaid on a bit of nonvolatile electrically erasable PROM (EEPROM).*

Careful analysis simplifies the EEPROM vs NOVRAM choice

alterable ROMs (EAROMs). They're reprogrammable only after an entire memory array (or at least one page) is electrically erased. Similarly, second-generation devices require erasure of individual bytes before programming. Third-generation EEPROMs, however, automatically and internally erase a to-be-written byte as part of the write cycle; they also contain much of the required voltage-generating and pulse-shaping functions on chip.

Two examples of third-generation EEPROMs currently in production are the Intel 2817 and the Seeq 5213. The 2817 latches the data to be written and eliminates the need for prewrite erasure. However, it requires an external high-voltage supply as well as a timing capacitor for deriving internal timing signals.

TABLE 1—EEPROM/NOVRAM COMPARISONS

	NOVRAM (X2212)	EEPROM (X2816A)
Density (bits)	1024	16,384
Price (1k level)	$9.00	$23.00
Cost/bit	$0.0088	$0.0014

The 5213 generates the high voltage on chip but requires external latches that hold the data and address valid during erase and write operations.

Fourth-generation EEPROMs are characterized by

Anatomy of a NOVRAM cell

NOVRAM-cell operation depends on a phenomenon termed Fowler-Nordheim tunneling. In the NOVRAM, a layer of oxide isolates a gate from an underlying section of polysilicon. Applying a large positive voltage to this floating gate while holding the underlying polysilicon near ground programs the gate.

Specifically, electrons attracted to the floating gate's significantly higher potential tunnel across the separating oxide. As a result, the floating gate acquires a net negative charge from the tunneled electrons.

The cell is erased in a similar manner: The floating gate is held at a low potential while the potential of the top polysilicon layer is raised; the electrons then tunnel across the oxide from the floating gate to the neighboring polysilicon sandwich.

The EEPROM technology employed in Xicor's NOVRAM uses a 3-layer polysilicon sandwich that, when coupled with a 6-transistor static-RAM cell, results in the NOVRAM circuit shown in **Fig A.** The state of the static-RAM cell determines whether the EEPROM cell is programmed or erased during a store cycle.

Capacitance ratios are the key to the data transfer from RAM to EEPROM. If node N_1 is LOW, Q_7 is turned off, allowing the junction between capacitors C_3 and C_4 to float. Because the combined capacitance of C_3 and C_4 is larger than C_P, the floating gate follows the Store-node voltage. When the voltage on the floating gate is sufficiently high, electrons tunnel from $POLY_1$ to $POLY_2$, and the

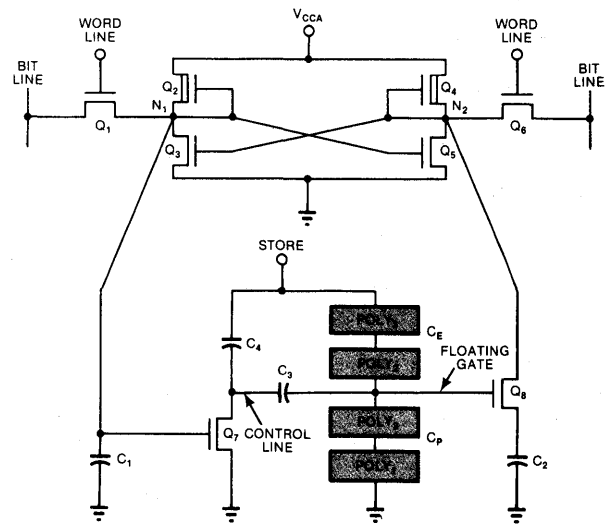

Fig A—A NOVRAM cell *consists of two sections: a 6-transistor RAM and a shadowing 2-transistor EEPROM.*

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on-chip generation of all high-voltage and wave-shaping functions in addition to their use of on-chip latches and self-timing features. Their byte-write requirements are identical to those of static RAM except that the EEPROM write cycle, once initiated by normal static-RAM timings, takes as long as 10 msec. Once a byte-write operation begins, the EEPROM is self supporting, freeing the processor and all external circuitry for other tasks. Read timing to the EEPROM is identical to that of a standard EPROM, RAM or ROM.

An important feature of a fourth-generation EEPROM is its compatibility with currently used RAM, EPROM and ROM. An EPROM- or ROM-based system needs only an additional Write Enable line to each socket to provide retrofitting for EEPROM. This control line allows the changing of data tables and program store without removing the component from the system, as required with EPROMs.

Choosing between NOVRAM and EEPROMs

Many application requirements can be satisfied by either of the two memory types. However, note that although NOVRAM is the most versatile in terms of features and capabilities, the price you pay for its greater intelligence is increased cell size.

Specifically, a fourth-generation EEPROM's cell is small and simple, allowing much higher density storage than in a NOVRAM. The EEPROM is also more efficient as memory-array area increases, thanks to the

gate becomes negatively charged.

If node N_1 is HIGH, Q_7 turns on, grounding the junction between C_3 and C_4. C_3, larger than C_E, holds the floating gate near ground when the Store node gets pulled HIGH. This action creates a sufficiently large field between $POLY_2$ and $POLY_3$ to tunnel electrons away from the floating gate, leaving it with a positive charge.

The recall operation also depends on capacitance ratios. C_2 is larger than C_1. When the cell receives the external $\overline{\text{Recall}}$ command, the internal power supply (V_{CCA}) first goes LOW to equalize the voltages on N_1 and N_2. When V_{CCA} is allowed to rise, the node with the lighter capacitive load rises more rapidly. The flip flop's gain causes the lightly loaded node to latch HIGH and the opposite side to latch LOW. If the floating gate has a positive charge, C_2 is connected to N_2 through Q_8, and N_2 latches LOW. If the floating gate has a negative charge, Q_8 gets turned off and N_1 experiences the heavier loading.

A major task in the development of the NOVRAM was to reduce the amplitude and simplify the waveform of external voltages needed for programming or erasure. Earlier devices required carefully shaped pulses with amplitudes exceeding 20V.

The first step in the cell design was to reduce the internal voltage level presented to the cell to initiate electron tunneling. The voltage magnitude required for programming a floating gate is related to the intensity of the electric field generated at the oxide-polysilicon interface by that voltage.

Electric-field strength at the oxide-polysilicon interface can be increased by using an extremely thin oxide, on the order of 100Å. A second technique uses textured polysilicon to locally enhance the field at the surface and achieve Fowler-Nordheim tunneling. It achieves better data retention.

Once the internal voltage-level requirement was reduced, a key achievement in device design was the on-chip generation of the high-voltage pulses needed to program or erase an individual cell. A Store-voltage generator **(Fig B)** provides the solution; it uses a 32-stage capacitor/transistor charge pump.

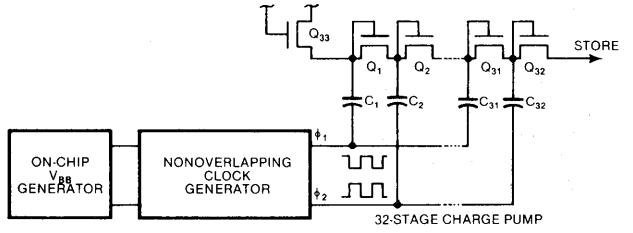

Fig B—A 32-stage charge pump *internally generates a NOVRAM's high Store voltage, allowing the device's NOVRAM and EEPROM sections to operate from 5V.*

Each NOVRAM cell combines RAM and EEPROM

TABLE 2—EEPROM/NOVRAM DATA-CAPTURE SPEEDS

	NOVRAM (X2212)	EEPROM (X2816A)
Byte-Write Time	256 × 1 μsec	256 × 10 msec
Store Time	10 msec	0
Total Time	10.26 msec	2.56 sec

decrease in the relative proportion of support-circuitry area required. Therefore, EEPROMs are more likely to be the device of choice if your application needs large amounts of memory.

The larger cell size and more extensive on-chip support that gives NOVRAM its added capabilities also results in a higher cost per bit, which might not be justified in applications that don't require all of a NOVRAM's features. Consider, for example, the cost-per-bit comparison between the X2212 256×4-bit NOVRAM and the X2816A 2k×8-bit EEPROM (**Table 1**): NOVRAM cost per bit is more than six times greater than that of EEPROM.

However, cost-per-bit ratios can be deceiving for systems requiring a minimum amount of nonvolatile memory. Lower density nonvolatile memories often are more cost effective in a NOVRAM configuration. The smallest NOVRAM currently available, the 64×4 X2210, is also the least expensive 5V device.

Another selection factor to consider is the required write time. An EEPROM requires a relatively long write time (10 msec/byte max), while NOVRAM write time is that of a typical static RAM. Therefore, NOVRAMs are more suited for applications requiring frequent memory-data changes, while EEPROMs most suit applications calling for infrequent memory writes.

A NOVRAM is also better suited to data-capture applications. **Table 2** compares two 256×4-bit NOVRAMs organized in a byte-wide configuration with a 2k×8 EEPROM in terms of the time needed to store 256 bytes of information. These times assume a 1-μsec/byte max processor write-cycle time. You can see that the NOVRAM's single-store operation makes it much faster. A NOVRAM system can update and store 10,000 bytes of data in the time needed to store two bytes of EEPROM information.

Another important NOVRAM feature is the device's ability to initiate and complete a nonvolatile store of data under external-signal control. This feature can be a key decision criterion in real-time applications such as power-fail re-entrant systems.

Both types serve power-fail-tolerant controllers

As noted, however, many applications can profitably use either device type. One common application in this class centers on retaining important system information in the event of a power loss. In most systems, power failures require reinitialization of the entire system, necessitating the temporary loss of system operation. In real-time control applications, this loss of control can cause expensive and sometimes dangerous failures of the process or equipment being controlled.

Such an application's main requirement is therefore some type of nonvolatile storage upon power failure. A prime consideration in this type of environment is the storage of a fixed amount of data upon receipt of an

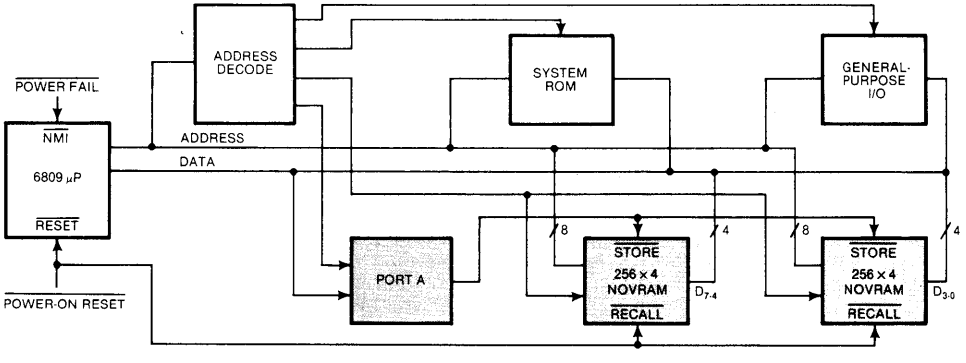

Fig 2—In this controller, *a NOVRAM retains the μP state in the event of a power failure.*

```
;*****************************************************************************
; AN EXAMPLE OF THE POWER-DOWN AND POWER-ON CODE FOR THE 6809 USING
; THE NOVRAM FOR PROCESSOR STATUS STORAGE.
;*****************************************************************************
; LOCATION DEFINITIONS
NVRAMLO         .EQU    0000H
NVRAMHI         .EQU    NVRAMLO + 256.
; THE NOVRAM IS LOCATED AT THE BOTTOM OF THE 6809 MEMORY MAP
DIRTY           .EQU    NVRAMHI ;TEST BYTE FOR POWER FAIL CONDITION
OLDSTK          .EQU    NVRAMHI-6 ;STACK POINTER NONVOLATILE LOCATION
STACK           .EQU    NVRAMHI-7 ;PROCESSOR STACK BEGINNING LOCATION
TEMP1           .EQU    NVRAMHI-1 ;IMPORTANT PROCESS PARAMETERS
TEMP2           .EQU    NVRAMHI-2
TEMP3           .EQU    NVRAMHI-3
PORTA           .EQU    8000H   ;LOCATION OF DATA REGISTER FOR PORT
                .ORG 0F800H
;*****************************************************************************
;                       POWER FAILURE ROUTINE
;*****************************************************************************
PFAIL           STS     OLDSTK  ;WRITE CURRENT STACK POINTER INTO NOVRAM
; AT THIS POINT, THE POWER FAIL INTERRUPT HAS PUSHED ALL OF THE
; CURRENT VALUES OF THE PROCESSOR REGISTERS ONTO THE STACK. THE
; STACK POINTER POINTS TO THESE VALUES.
                LDA     #0A5H   ;LOAD ACCUMULATOR WITH POWER FAIL FLAG
                STA     DIRTY   ;STORE FLAG IN NOVRAM
                LDA     #00.    ;WRITING A 0 TO THE PORT GENERATES
                STA     PORTA   ;A STORE SIGNAL TO THE NOVRAM
LOOP            BRA     LOOP    ;SIT AND WAIT UNTIL POWER DISAPPEARS
;*****************************************************************************
;                       POWER-ON RESET ROUTINE
;*****************************************************************************
RESET           LDA     #0FFH   ;SET ALL OUTPUTS TO A "1"
                STA     PORTA   ;WRITE TO PORT TO KEEP STORE HIGH
                LDA     DIRTY   ;LOAD FLAG TO SEE IF POWER FAILED
                CMPA    #0A5H   ;IT WILL BE A 0A5H IF IT DID
                BNE     INIT    ;IF NOT DO NORMAL INITIALIZATION
                LDA     #00H    ;CLEAR THE POWER FAILURE FLAG
                STA     DIRTY   ;IN THE NOVRAM
                LDA     #00H    ;AND GIVE A STORE SIGNAL
                STA     PORTA   ;TO STORE THE NEW FLAG
                LDA     #0FFH   ;RESET PORT.
                LDS     OLDSTK  ;LOAD OLD STACK VALUES
                RTI             ;RETURN FROM POWER FAIL INTERRUPT
INIT  ;NORMAL INITIALIZATION CODE
;                       .

;                       .

;                       .

                .ORG 0FFCH
                .WORD   PFAIL   ;POWER FAILURE INTERRUPT VECTOR
                .WORD   RESET   ;POWER-ON RESET INTERRUPT VECTOR
                .END
```

Fig 3—A power-failure-tolerant controller's 6809-μP assembly-language routines *handle both failure store and recovery. NOVRAM handles the stack and other temporary storage.*

NOVRAM doubles as bootstrap and global memory

external $\overline{\text{Power Fail}}$ signal. You can use an EEPROM for this purpose if the processor has sufficient time to recognize the power failure and respond by writing the data into memory. Otherwise, a NOVRAM is the device of choice because it captures data in one nonvolatile store operation.

Fig 2 shows a simple controller that uses a NOVRAM to retain the state of a μP in the event of a power failure. The $\overline{\text{Power Fail}}$ signal generates a μP interrupt, and the NOVRAM stores the contents of all RAM including the μP stack.

Upon interrupt acknowledgement, the μP registers are pushed onto the stack as program control branches to the interrupt routine (**Fig 3**). The routine writes the current stack pointer and a test byte to the NOVRAM, signifying that a power failure has occurred, and then generates a $\overline{\text{Store}}$ signal. The power supply is designed to ensure that the V_C level remains above 4.5V for 10 msec after it generates the $\overline{\text{Power Fail}}$ signal.

Once power is restored, the $\overline{\text{Power-On Reset}}$ signal generates a $\overline{\text{Recall}}$ signal to the NOVRAM. The power-on routine in the μP checks the state of the test byte to see if a process was interrupted by a power failure. If so, the stack pointer gets loaded with the address of the saved processor state, a return from interrupt is executed, and the process resumes.

NOVRAM stores terminal configurations

An application in which NOVRAM is the device of choice lies in the storage of terminal-configuration information, consisting of such parameters as baud rate, data format and parity method. The conventional approach to this task (**Fig 4**) stores data in DIP switches on a pc board somewhere in the terminal; the user must have a terminal manual handy for decoding switch settings to change any of the preset features.

One alternative uses menu-driven configuration modes to set the terminal and a NOVRAM to store the terminal-configuration parameters. The user can easily change the configuration information for specific tasks and retain this data until the terminal loses power.

Upon power-up, a set of predefined default parameters stored in the NOVRAM's EEPROM section goes to RAM, and the terminal is configured. The NOVRAM also allows the user to change default parameters for subsequent sessions by transferring the modified RAM data to EEPROM—in either a general or privileged user environment. The NOVRAM's ability to manipulate two sets of data proves important here because the terminal software operates on the data in the NOVRAM's RAM section, regardless of whether the terminal is in the default configuration or a user-entered one.

In **Fig 4**'s conventional approach, an 8-section DIP switch holds the configuration information. If a switch position is open, the pull-up resistor causes a ONE to appear at the buffer input; a closed switch denotes a ZERO. Decoding the buffer's address and reading the data provides the switch information. If the system needs more than eight bits, the design requires additional switches, resistors, buffers and logic.

If a block of memory addresses is reserved for configuration information, the granularity of the address decoding increases with the number of DIP

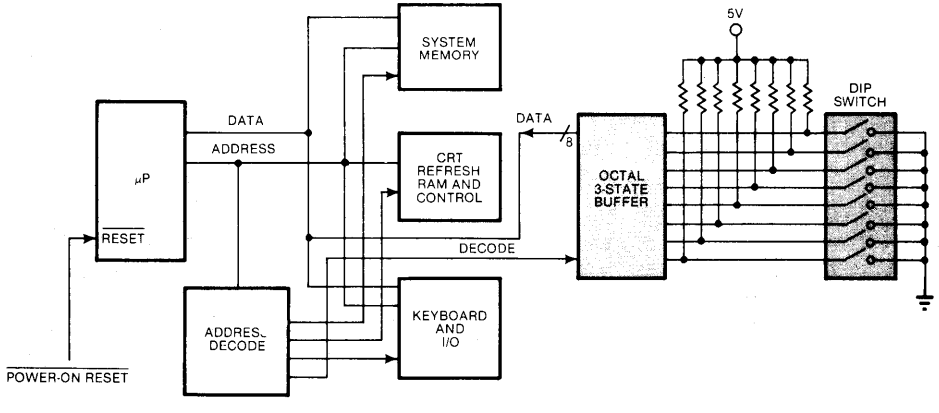

Fig 4—A conventional terminal configuration *uses an 8-section DIP switch to program the terminal's operating parameters.*

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switches required. And you can change the default data only by altering individual switch positions.

The NOVRAM implementation of this system (**Fig 5**) permits the storage of 1k bits of configuration information in one 18-pin X2212. If you reserve an 8k memory-address block for configuration storage, the NOVRAM requires only a single chip-select decode. The only restriction in this arrangement is that four parameter bits get read simultaneously, rather than eight. Note that storing the same amount of information using the conventional approach calls for 128 DIP switches and octal buffers, 1024 resistors and sufficient address decoding to provide 128 separate locations within the 8k field—an address granularity of 64.

A terminal user employs the keyboard to enter operational parameters into the NOVRAM. The user enters a configuration mode when the terminal is in the off-line or local mode. A menu display shows the current terminal configuration; the user moves the cursor and/or strikes a control key to alter the current values. Once the configuration is established, the user exits the configuration mode, and the terminal operates according to the new parameters. The user can also change the default parameters by entering a control signal that places the new configuration mode in the NOVRAM's EEPROM section.

In this application, very few terminals would ever require the NOVRAM's full storage capacity for configuration information. You could therefore employ the unused portion to store other operational and maintenance parameters.

NOVRAM loader provides reusable memory

A system that employs a bootstrap loader during initialization is another prime NOVRAM application candidate. Examples of such applications include single-chip μCs operating in external-memory modes and full-blown systems requiring the maximum allowable memory space. A common approach to this requirement stores the bootstrap program in ROM or EPROM. However, the program occupies memory space that might be used for other purposes during system operation. Because most initialization routines use a relatively small amount of memory space, this approach can be particularly wasteful in space-limited systems.

As an alternative, you can preprogram the bootstrap into the EEPROM section of a NOVRAM. Upon reset, the system generates a $\overline{\text{Recall}}$ signal to the NOVRAM, loading the bootstrap into RAM. The bootstrap program executes, and the NOVRAM RAM section then becomes free for other uses. This design feature even allows bootstrap-program alteration via external control for servicing or software updates.

Fig 6 shows a simple disk-oriented system that uses NOVRAM as a bootstrap memory. After booting, the NOVRAM becomes a global RAM. The device—and

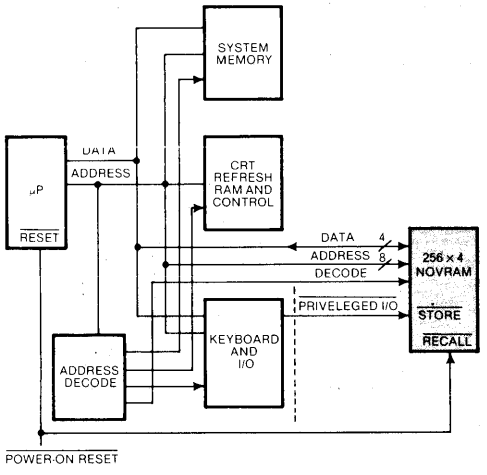


Fig 5—Replacing a DIP switch with a NOVRAM *results in greater versatility for programming terminal operating parameters.*

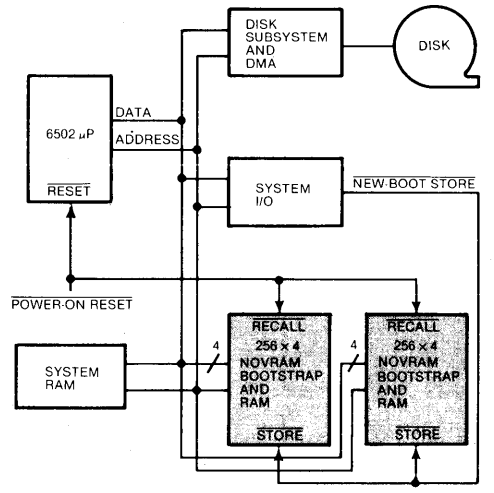


Fig 6—This disk-oriented system uses two NOVRAMs *as bootstrap memory. Once loading is complete, the NOVRAM functions as global RAM.*

```
;*****************************************************************************
; THIS PROGRAM SEGMENT DEMONSTRATES THE OPERATION OF A SYSTEM WHICH
; USES A BOOTSTRAP PROGRAM PRELOADED INTO THE NOVRAM'S EEPROM. UPON
; POWER-ON RESET, THIS BOOT IS RECALLED INTO THE EEPROM'S RAM. THE
; BOOTSTRAP PORGRAM CONFIGURES THE SYSTEM, AND THEN USES THE NOVRAM'S
; RAM AS REGULAR RAM. THE NOVRAM IS LOCATED AT THE BOTTOM OF THE
; 6502'S MEMORY MAP SO THAT THE HIGHEST LOCATIONS CAN CONTAIN THE
; PROCESSOR'S INTERRUPT VECTORS. ACTUAL LOADING OF THE OPERATING
; SYSTEM INTO MAIN MEMORY IS ACCOMPLISHED BY A DMA CONTROLLER, WHICH
; LOADS THE PROGRAM FROM THE DISK.
;*****************************************************************************
DMADATA         .EQU    0C000H  ;DMA DATA REGISTER
DMACTRL         .EQU    0C001H  ;DMA CONTROL REGISTER
PROGRAM         .EQU    00200H  ;START OF PROGRAM MEMORY

                .ORG    0FF00H
; THIS PROGRAM SECTION IS LOADED INTO THE EEPROM SECTION OF THE
; NOVRAM, AND IS RECALLED UPON POWER-UP.
BOOT            LDX     #0FFH   ;LOAD THE X INDEX REGISTER WITH FF
                TXS             ;TRANSFER TO STACK POINTER AT 01FF
CONFIGUR        ; THIS CODE SECTION CONFIGURES THE DMA CONTROLLER,
                ; AND SETS THE INITIAL LOAD LOCATION AT 0200H, SO
                ; THAT PROGRAM DATA WILL NOT OVERWRITE THE STACK.
SEEK            ; THIS CODE SECTION TELLS THE DMA CONTROLLER WHAT
                ; DISK SECTION IT SHOULD GET THE PROGRAM FROM, AS
                ; WELL AS HOW MUCH DATA TO LOAD.
GO              LDA     #01.    ; 01 IN THE DMA CONTROL REGISTER
                                ; WILL INDICATE DISK DATA LOADING
                STA     DMADATA ; STORE IN THE DMA CONTROL REGISTER
                LDA     #0A5H   ; WRITE TO TEST BYTE TO SIGNIFY BOOT
                STA     TEST    ; IF WE SEE A #0A5H,WE ARE IN BOOT
LOOP            JMP     LOOP    ; LOOP UNTIL DMA CONTROLLER INTERRUPTS
;*****************************************************************************
; NMI FROM DMA INTERRUPT WILL VECTOR HERE. THIS ROUTINE CHECKS THE
; STATUS FROM THE DISK SUBSYSTEM AND DMA CONTROLLER TO INSURE THAT
; THE REQUESTED DATA HAS BEEN LOADED. ONCE A SUCCESSFUL BOOT HAS
; TAKEN PLACE, THE SYSTEM CAN CHANGE THE NMI VECTOR SINCE THE NOVRAM
; NOW FUNCTIONS AS A REGULAR RAM.
;*****************************************************************************
INTERRUPT       LDA     DMACTRL ; CHECK TO SEE IF THE DESIRED PROGRAM
                                ; HAS BEEN SUCCESSFULLY LOADED. IF SO,
                                ; ALL WILL BE ZEROES EXCEPT D0 WHICH
                                ; WILL BE SET TO SIGNIFY THAT AN
                                ; INTERRUPT WAS GIVEN.
                CMP     #01     ; ARE WE LOADED?
                BNE     BOOT    ; IF NOT, WE HAVE AN ERROR, RE-BOOT.
                LDA     TEST    ; GET TEST BYTE TO SEE IF IN A BOOT.
                CMP     #0A5H   ; IF SO, TEST BYTE WILL BE A5 HEX.
                BEQ     PROGRAM ; AND JUMP TO PROGRAM BEGINNING.
ERROR           ;OTHERWISE WE HAVE AN ERROR.
TEST            .BYTE   00.     ; A ZERO IS STORED IN TEST INITIALLY.
                .ORG    0FFFAH
NMI             .WORD   INTERRUPT; NMI WILL GO TO SYSTEM START ROUTINE.
RESET           .WORD   BOOT    ; POWER-ON RESET WILL CAUSE AUTO BOOT.
```

Fig 7—A 6502-µP assembly-language boot routine *is located temporarily in NOVRAM, which forms the highest 256 bytes of memory in this system.*

hence the bootstrap routine—is in the highest memory segment so it can hold all the interrupt vectors. μPs such as the 6502 and 6800 use these locations for reset and interrupt pointers.

In the bootstrap program (**Fig 7**), the reset vector for the 6502 μP points to the boot routine. **Fig 6**'s two NOVRAMs reside in the highest 256 bytes of the address map. Upon power-up, the NOVRAM's EEPROM section gets loaded into the device's RAM section. The μP then initializes the stack pointer, and the DMA controller begins a data transfer from the disk. A test byte gets set to show that a boot process is under way.

Once the DMA transfer begins, the μP loops until an interrupt signifies that the operation is complete. The μP vectors to the interrupt-handling routine, which determines if a valid DMA has occurred. If an error has occurred, the program causes a jump to location Program, where the first byte of the loaded program resides. The NOVRAM RAM is then free for general use. Note that you must take care not to accidentally overwrite the interrupt and reset vectors, located in the highest memory locations.

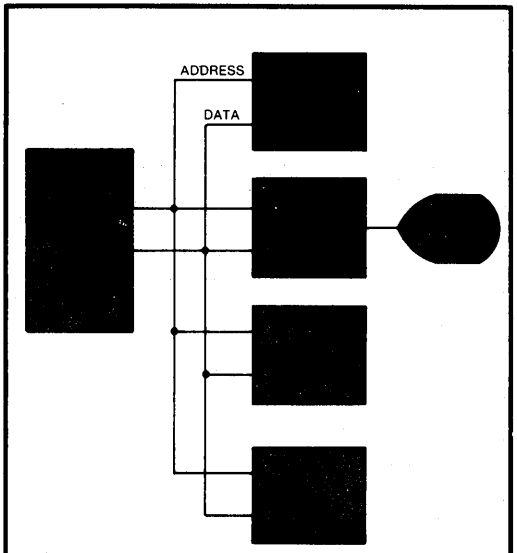


Fig 8—A self-learning video game uses EEPROM *to change difficulty levels after play is completed.*

EEPROM stores controller parameters

Turn now to some applications in which an EEPROM is the device of choice. One such task is the storage of coefficients in PID (proportional integral-differential) controllers.

Modern control applications such as the PID algorithm are characterized by two basic qualities. First, they are computationally intense. Second, their ability to precisely control a set condition is based on their knowledge of the effects of their outputs. This knowledge results from deriving the various controller coefficients via calculations: Each controller output must be calculated with reference to the previously defined term.

If a PID system loses power, it must resynthesize all data before it approaches the level of performance exhibited before the power loss. The data tables for each control task are fairly large and require a substantial amount of memory. Therefore, a controller might use EEPROM for algorithm-coefficient storage.

Note also that most PID-controller deviations result from the sensitivity of the system's sensors as well as the response time and accuracy of the control outputs. These variables might change in a particular unit but are usually the same when power returns to the controller; they need only be updated occasionally as the system runs. An EEPROM's slow write time and fast read time make it ideally suited for this infrequent-write application.

Finally, note that parameters stored in EEPROM are available to the system whenever it's running—whether programmed into the system during initialization or resulting from previous system operation. An EEPROM implementation of such a system thus results in shorter system-interrupt recovery time as well as self-recalibration upon component replacement.

Self-learning video games use EEPROMs

Another potential EEPROM application centers on the storage of self-teaching or self-modifying code, through which a process or algorithm can tailor itself based on the results of previous executions. Such applications are characterized by updates to program storage, which usually occur relatively infrequently. This high read-to-write ratio of memory access, as well as the densities required in the program store, generally dictate an EEPROM implementation.

An example of this application category is a self-learning video game (**Fig 8**). Such a game's success depends largely on its ability to keep a player interested by continually increasing the level of challenge after repeated plays.

At the end of a certain period (**Fig 9**), the game analyzes the scores and modifies its program (including timing loops and difficulty factors) to present a more complex play to the next group of players. The learning algorithm also makes the game easier to play under

certain conditions, preventing unwarranted increases in difficulty.

The initial game code includes several routines that make the game progressively more difficult to play. These routines get bypassed in the initial program execution by always-executable branch instructions. At

```
;*****************************************************************************
; THIS IS AN EXAMPLE OF 6809 GAME CODE WITH BRANCH NEVERS
;*****************************************************************************
PLAY            ;THIS SECTION OF CODE IS THE EASIEST
;                       .
;                       .
SECT1           BRA     SECT2   ;WE START OUT BY BYPASSING THIS SECTION
                ;THIS SECTION OF CODE IS MORE DIFFICULT
SECT2           BRA     SECTN   ;WE ALSO BYPASS THIS SECTION
;                       .
SECTN           BRA     ENPLAY  ;WE HAVE N DIFFICULT ROUTINES
;                       .
ENPLAY          LDA     TEST    ;CHECK THE END OF GAME FLAG
                CMPA    #0FFH   ;IT WILL BE AN FF IF GAME IS OVER
                BNE     PLAY    ;IF GAME NOT OVER, GO BACK TO MAIN LOOP
                BRA     FINISH  ;IF IT IS, GO TO FINISH SECTION

FINISH          ;THIS IS THE AREA FOR THE END OF THE GAME CODE. IT MAY
                ;CALL PROCEDURES TO MAKE THE GAME HARDER IF THE
                ;ANALYSIS OF PAST SCORES WARRANTS.
;*****************************************************************************
; THIS SECTION OF CODE INCREASES THE DIFFICULTY LEVEL OF THE GAME BY
; REPLACING ONE OF THE BRANCHES AROUND THE MOST DIFFICULT ROUTINES
; WITH A DUMMY BRANCH OR BRANCH NEVER INSTRUCTION. THIS ROUTINE ALSO
; INCREASES A GLOBAL DIFFICULTY FACTOR, ON WHICH MANY OF THE GAME
; PLAYING ALGORITHMS ARE COMPUTED, BY ONE.
;*****************************************************************************
DIFCULT         .BYTE   00      ;DIFFICULTY FACTOR
;               TABLE OF BRANCH LOCATIONS
TABLE           .WORD   SECT1
                .WORD   SECT2
;                       .
;                       .
TABLEND         .WORD   SECTN

MAKEHARD        LDX     #TABLE  ;START LOOKING THROUGH TABLE AT THE TOP
LOOK            CMPX    #TABLEND  ;ARE WE AT THE END OF THE TABLE?
                BEQ     NEXT    ;IF SO, GAME CAN'T BE MADE HARDER!
                LDA     [X++]   ;LOOK AT THE OPCODE AT THE BRANCH, AND
                                ;INCREMENT INDEX REGISTER FOR NEXT LOOK
                                ;(AUTO INCREMENT BY 2 INDEXED)
                CMPA    #21H    ;CHECK TO SEE IF IT IS A BRANCH NEVER
                BNE     LOOK    ;IF NOT, THEN CHECK THE NEXT ONE
                STA     [0,X]   ;OTHERWISE MAKE THE GAME HARDER BY
                                ;INCLUDING A ROUTINE BY STORING A BRANCH
                                ;NEVER (INDEXED INDIRECT)
                INC     DIFCULT ;INCREMENT DIFFICULTY FACTOR
ATTRACT         ;ENTER THE ATTRACT MODE FOR THE GAME
;                       .
;                       .
NEXT            ;WE CAN'T MAKE THE GAME HARDER, SO WHAT DO WE DO??
                .END
```

Fig 9—Written in 6809-μP assembly language, *this self-learning video-game program changes branch instructions based on previously obtained scores.*

the end of each play, the system determines from the score whether to make the algorithm more difficult. If so, it eliminates some of the branches around difficult parts of the game software. A simple table stores all of these branches. Other features, including speed parameters and energy levels, can also be stored to make the game more difficult as scores improve. Storing them in EEPROM provides the additional advantage of easy updates and changes in the basic table.

EEPROM and NOVRAM team up

As a final example, consider how you might combine EEPROM and NOVRAM in an automobile navigational system that could direct a driver to a location within a specific city or area. Proponents of this approach envision beacons located throughout an area, notifying each in-car computer of the car's current location. Provided with this information, a local electronic map and the desired destination, the computer would direct the driver along the most efficient route.

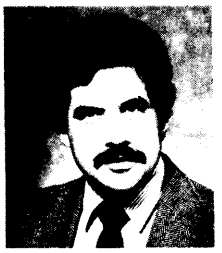
Data-storage requirements would be extensive, implying the use of EEPROM. After all, the system must not only be programmed with a map of the area roads but must also be able to select between many possible alternatives based upon continuously changing factors such as time of day and known construction areas. Using EEPROM would allow the car's driver to load the navigational computer upon entering a location such as a filling station.

A NOVRAM would also prove critical to this application. It would contain rapidly changing current information, which would get transferred to the NOVRAM's EEPROM section upon reaching a destination. The approach allows power removal from the system while the car is parked, eliminating battery drain. Restarting the vehicle would transfer the current data from the NOVRAM's EEPROM section back to its RAM section.

Fig 10 shows how the hardware could be implemented. Map information, stored in EEPROM, gets changed as necessary via the map-download controller, a serial interface over which the data is transmitted. The transmission rate is low because the map data is written into EEPROM, which specs a slow write cycle.

The system has two main interfaces—to the driver and to the vehicle. The former consists of a keyboard for input and a CRT for display of the map and other information. The latter receives data such as mileage and speed so that the system can monitor the driver's progress along a given route. **EDN**

Author's biography



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Article Interest Quotient (Circle One)
***High* 476 *Medium* 477 *Low* 478**

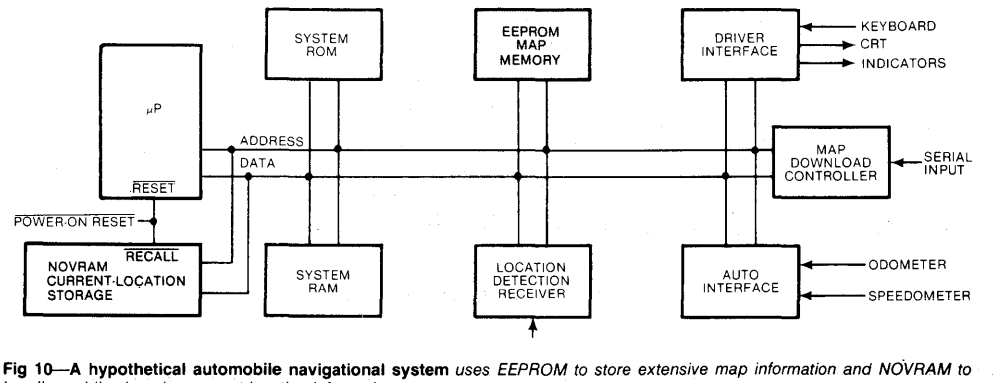


Fig 10—A hypothetical automobile navigational system *uses EEPROM to store extensive map information and NOVRAM to handle rapidly changing current-location information.*

Non-volatile memories keep appliances out of the dark

Richard Orlando, Xicor Inc., Milpitas, CA

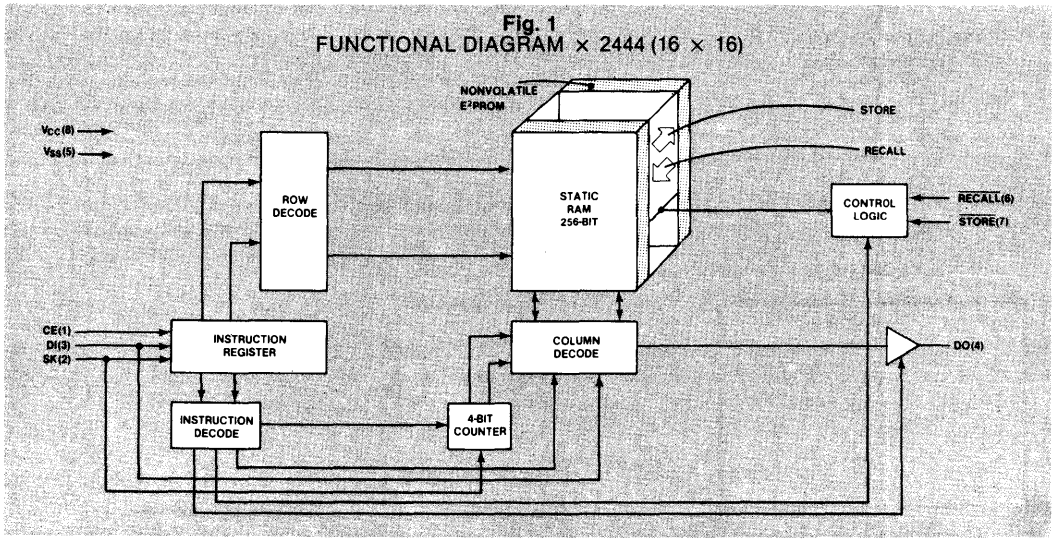
Appliance design has undergone a revolution in recent years. The advent of the low-cost, single-chip microcomputer has opened many applications for these small computers in the appliance market. Initial applications were based upon new types of appliances where digital control was a necessity. Today one sees even the venerable "white goods" using single-chip microcomputers to add features and capabilities to the end products. With this migration to digital control, a need for non-volatile memory has developed, and many new non-volatile memory devices have been made available to the designer.

Appliance control applications have gone through an orderly evolution. The design methods of the past used electromechanical devices, such as switches, relays, mechanical timers and, of course, wafer switches. The requirements of older appliances could be easily satisfied by these devices. Washing machines, for example, using multiplane wafer switches driven by a simple timer could initiate, time and terminate the different cycles of the laundry washing process. And the electronic range allowed simple electromechanical timing of a cooking cycle.

Since the appliance industry has been subject to the whims and attitudes of the consumer, the desired capabilities of appliances have grown as a function of added features. A simple example is the evolution of the home stove controller: first, accurate control over cooking temperature, then the ability to turn off the oven after a programmed time, and, finally, the complete programmable oven that not only turns itself off after a programmed time has elapsed, but also initiates the cooking cycle at a certain time of day.

The increased capabilities of the appliances coupled with the availability of low-cost, single-chip micro-

Fig. 1
FUNCTIONAL DIAGRAM × 2444 (16 × 16)



8

computers has led to the final step in the evolution, that of full digital control. The use of the microcomputer as a control mechanism allows the designer increased flexibility, reliability and precision in the control process, not easily attainable with the older design methods. Decreased development costs are also possible since a flexible digital controller can be used in a variety of different products, or models of the same product.

Microcomputer designs were not free of their own unique problems, however. The microcomputer interface required to perform the actual control functions was somewhat complex. New issues had to be addressed in terms of product reliability, since the semiconductor devices introduced different failure modes than those exhibited by electromechanical devices. The microcomputer also had a major disadvantage over prior design techniques due to its inherent volatile nature: when the power was removed from the appliance, the microcomputer not only stopped functioning, it lost any data it had maintained based upon the current state of the system.

One advantage that the older electromechanical timers possessed was that if the power went off to the appliance, the control system would maintain the state it was in when the power was interrupted. When the power was restored to the appliance, it would continue from where it left off. One can easily appreciate the irritation of a homemaker who, having left a roast in the oven, returns from errands to find that it had not resumed cooking after a blackout.

Emergence of non-volatility

With many appliance designs, there is a definite need to prevent such untoward situations. Some type of non-volatility is a necessity in appliance design. Since the cost of the appliance is a great concern, this non-volatility must be cost-effective. One of the earlier approaches was that of battery backup on the microcomputer itself, or on a separate CMOS memory in the system. The disadvantages of this approach are based simply on the limitations of batteries and the cost of implementation. Unfortunately, there were not many alternatives until now.

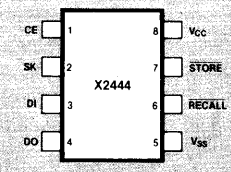
The past five years have seen a remarkable evolution in the emergence of semiconductor non-volatile memories. Unlike the battery backup of the data in either on-board or external RAM, these devices were able to retain data without the external power, in a manner similar to that of an EPROM. The main difference between these devices and the EPROM was their ability to be "rewritten" in-circuit, as opposed to being removed from the circuit, erased, and then "reprogrammed" before they were put back into the circuit.

Unfortunately, these early devices were expensive and difficult to use. They required multiple "programming" voltages, extensive support circuitry, and were quite unreliable. These devices, for the most part, were organized for microprocessor "bus" applications, and as such required too many I/O lines for efficient interfacing to single-chip microcomputers, where I/O lines are a precious commodity.

The development of 5v floating-gate, NMOS non-volatile memories eliminated many of the disadvantages of semiconductor non-volatile devices. These devices not only decreased the support circuitry required for their use, but increased the reliability of the devices. Unfortunately, these devices were also designed for "bus" applications and were relatively expensive due to their large densities (>1K bits). A need was recognized in the appliance and other industries for an inexpensive and reliable non-volatile memory designed exclusively for interfacing to single-chip microcomputers.

The Xicor X2444 answers this need. The device is a low-cost 16 × 16 non-volatile static RAM (NOVRAM for short) which features serial interface designed for interfacing to a single-chip microcomputer with a minimum requirement for both I/O

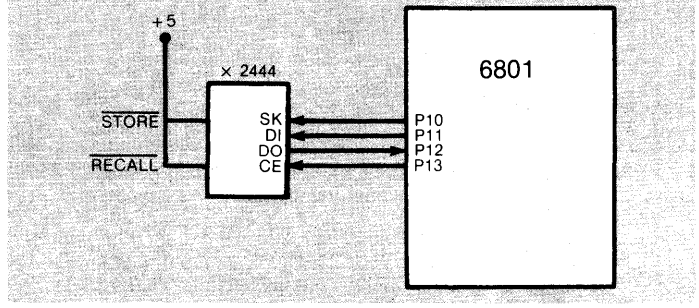
Fig. 2
PIN CONFIGURATION
8-PIN DIP. 300"



PIN NAMES

CE	CHIP ENABLE
SK	SERIAL CLOCK
DI	SERIAL DATA IN
DO	SERIAL DATA OUT
$\overline{\text{RECALL}}$	RECALL
$\overline{\text{STORE}}$	STORE
V_{CC}	+5V
V_{SS}	GROUND

Fig. 3
×2444-6801 INTERFACE



lines and software. Housed in an eight-pin mini-DIP, the X2444 provides inexpensive non-volatile data storage for both operational and configuration parameters. Its low cost (less than $4.00 in unit quantities) makes it the least expensive non-volatile storage on the market, even rivalling the DIP switch in unit cost, while providing the equivalent of 32 DIP switches in terms of data capacity.

The NOVRAM concept

The NOVRAM idea is not new. Xicor invented this type of memory more than three years ago. The concept is quite simple. Figure 1 shows a block diagram of the X2444. It consists of a 256-bit (16 × 16) static RAM with a 256-bit 5v E^2PROM array overlaid bit for bit in a "shadow" type manner. Two signals, $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$, control the transfer of data between the E^2PROM array and the static RAM. The STORE function replicates the data which is currently in the RAM into the non-volatile E^2PROM array. In a similar manner, the RECALL function transfers the non-volatile data in the E^2PROM array into the RAM. One can see that by simply performing a STORE during power failure, the data is then retained in the non-volatile E^2PROM , and can be restored to the RAM using the RECALL once power is returned to the system.

The X2444's serial interface method is ideal for microcomputer applications. Figure 2 shows the pinout and signal designation for the X2444. The four-line serial interface consists of a Chip Select (CS), a Serial Clock (SC), a Data In (DI) line, and a Data Out (DO) line. The Data In and Data Out timings are designed to allow the implementation of a single Serial Data line by typing both Data In and Data Out to a single I/O line from the microcomputer, reducing the I/O lines to three. All data transfer to and from the X2444 are performed over this serial interface by either synchronous 8-bit instructions or 16-bit data operations. The X2444 has two external pins, $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$, for performing the non-volatile operations via hardware control in the event of power failure. The X2444 also includes distinct STORE and RECALL instructions over the serial interface to allow only software control over the non-volatile operations.

The serial interface is accomplished using discrete "bit-banging" from the single-chip micro. An instruction is performed by loading an accumulator with the proper bit pattern, and shifting it out through an I/O line while toggling the serial clock low and then high again between each bit.

The software for this interface is simple, and an example of a 6801 implementation is shown in Figure 3. The software assumes that the X2444 is connected to bits 0, 1, 2 and 3 of the 6801 I/O Port 1. The interconnect between the 6801 and the X2444 is shown in Figure 4. The three main parts of the software segment are three subroutines, SHIFTIN, SHIFTOUT and DRIVE. The SHIFTOUT routine takes the eight bits of data in the A accumulator, and shifts it out through Bit 1 of Port 1. Between each data bit output the clock is toggled. This routine is used for either instruction or data output to the X2444.

The SHIFTIN subroutine gives the X2444 eight clock cycles, and shifts the data from the X2444 into the A accumulator. This routine is used only in the READ instruction. The DRIVE subroutine actually provides the driver to interpret the desired operation and issue the proper sequence of commands to the X2444. It should be noted that this sample interface uses the software-controlled STORE and RECALL commands and leaves the X2444 STORE and RECALL inputs tied to Vcc.

E.g. . . . microwave oven controller

One of the newest appliances in the consumer environment is the microwave oven. This also proves to be an ideal example for the application of a non-volatile memory.

The microwave oven started with a control mechanism which was no more than the simple electromechanical timer borrowed from electric ranges. Since the microwave oven cooks in times which are orders-of-magnitude faster than a conventional stove, it became apparent that an accurate and precise control mechanism was needed. The microwave was one of the first appliances to embrace full digital control using a single-chip microcomputer.

Figure 5 shows a typical microwave oven control system based upon the 6801 microcomputer. The user interface includes a keyboard, alarm and display, while the oven interface includes the magnetron control, door interlock, and an optional temperature probe. Non-volatile memory has been added to the system design through the use of an X2444. The interface method to the 6801 and the driving software are similar to that above. The key difference to note is the addition of an external signal to drive the $\overline{\text{STORE}}$ input. This allows the controller to automatically store the data in the RAM into the E^2PROM upon Power-Failure. The circuitry in the power supply senses a loss of power by monitoring either the ac or unregulated dc levels. Once a power failure has been detected, the power supply circuitry pulls the $\overline{\text{STORE}}$ input low. The power supply circuitry need only ensure that Vcc is held valid to the X2444 for 10 msec, and all of the data in the RAM will be stored into the E^2PROM array. Upon Power-on-Reset, the 6801 issues a RECALL command to the X2444, and all of the data is restored.

The remainder of the microwave control circuitry is fairly standard. A 4 × 4 keyboard provides an input mechanism for the user, while the status indicators and display provide visual feedback. A two-line magnetron control allows the use of variable power levels in the cooking process. Timing is performed using the 6801's internal 16-bit timer which is driven off the 60-Hz reference from the power supply. Standard features include a safety door

interlock and alarm. Optional features are provisions for a temperature probe for magnetron control or temperature-based cooking algorithms. The a-d converter used for temperature sensing has a serial interface similar to that of the X2444, and is placed on the same serial bus. Distinct chip selects enable the X2444 or the a-d converter to be accessed. Many such devices are currently on the market including the new TLC540 from Texas Instruments.

The X2444's non-volatile memory serves many functions in this application. Frequently used recipes or cooking sequences can be stored so that the microwave will sequence through a complex cooking algorithm automatically. The X2444's ability to store the data currently in the RAM into the E²PROM is very useful here. As the cooking process takes place, the 6801 keeps a copy of the preset time and power setting in the X2444's RAM. As cooking time elapses, a location in the X2444 is updated to show the elapsed time. In the event of a power failure, the current values of these variables are automatically stored into the E²PROM section of the X2444. Once power is restored to the microwave, the data in the E²PROM is loaded into the RAM section of the X2444, and cooking continues from where it was interrupted. Intelligence can be added to the control algorithm to compensate for the continued cooking (due to retained heat) that occurs after the power outage.

The X2444's unique NOVRAM architecture makes such an application feasible. Since current E²PROM technology has limitations on the number of times that the non-volatile data can be changed, one would not want to change the contents of the E²PROM each time the timer was incremented. If one were to use a typical E²PROM with a write limitation of 10,000 writes, the device would be worn out in a relatively short period of time at a write rate of one per second. Instead, the X2444 allows the system to update the E²PROM section of the chip only in the event of a power failure while using the unlimited RAM write capability of the X2444 every time the counter value changes.

The X2444's can also be used for a variety of other purposes in microwave design. As was mentioned earlier, one can save development time and money if a universal controller is designed. Many different models could use the same controller simply by adding circuitry

Fig. 5
6801 MICROWAVE CONTROLLER

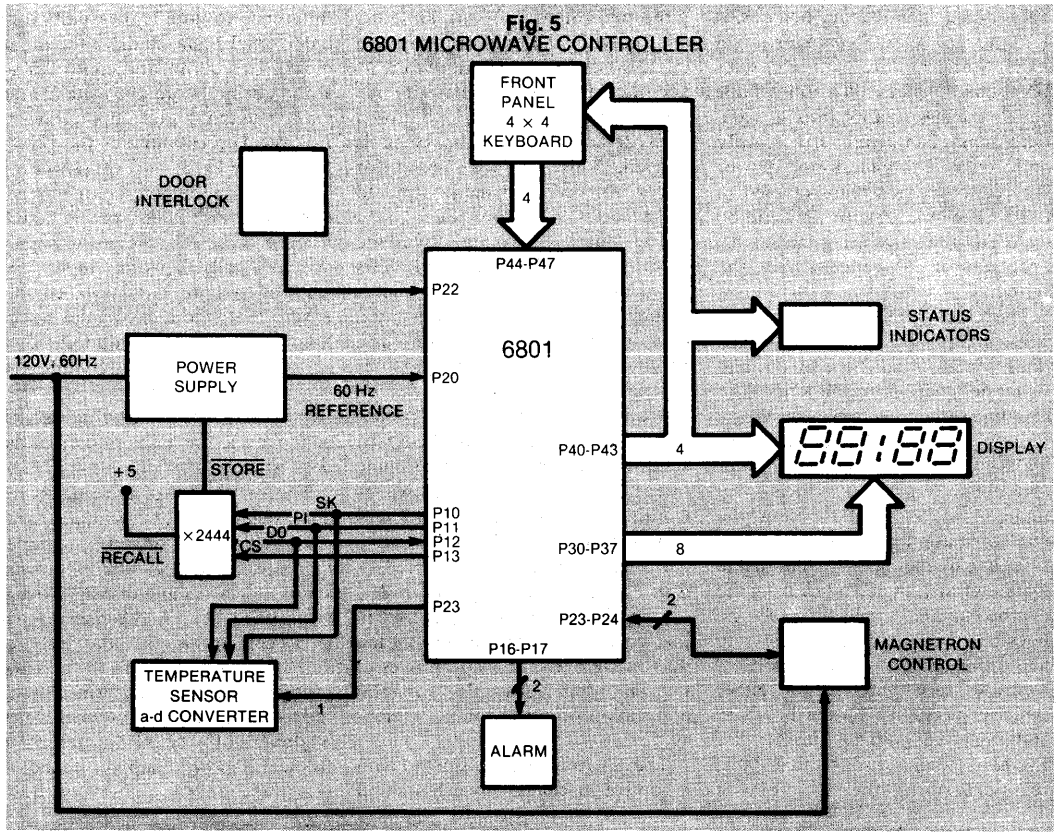


Fig. 4
X2444 DRIVER PROGRAM FOR 6801

```
PAGE -  1                X2444 DRIVER PROGRAM FOR 6801
File: X2444          CODE AS OF AUGUST 22, 1983   Minimal Driver for X2444, 6801 Version 3.0

0000:                          .TITLE "X2444 DRIVER PROGRAM FOR 6801"
0000:                          .ABSOLUTE
Z blocks for procedure code  7440 words left
0000:                          .PROC X2444
Current memory available:    7992
0000:                          .ORG  1000H
1000:                        ;*********************************************************************************
1000:                        ;                        6801 X2444 DRIVER
1000:                        ;       ASSUME THAT PORT1 IS USED AS THE 2444 INTERFACE
1000:                        ;       PORT1'S REGISTERS ARE LOCATED AS FOLLOWS .
1000:                        ;                  DATA DIRECTION          HEX  0000
1000:                        ;                  PORT                    HEX  0002
1000:                        ;                                PORT1              X2444
1000:                        ;       I/O 0                    SERIAL CLOCK       SERIAL CLOCK
1000:                        ;       I/O 1                    SERIAL OUT         SERIAL IN
1000:                        ;       I/O 2                    SERIAL IN          SERIAL OUT
1000:                        ;       I/O 3                    2444 SELECT        CHIP SELECT
1000:                        ;
1000:                        ;       COMMANDS ARE PASSED TO THE X2444 ROUTINE BY A PARAMETER IN THE
1000:                        ;       A ACCUMULATOR, WHILE THE ADDRESS IF NEEDED IS PASSED ON THE STACK
1000:                        ;       SERIAL DATA IN OR OUT USES THE TEMPORARY LOCATION TEMP1,
1000:                        ;       WHICH IS A SIXTEEN BIT WORSD.  THE X2444 COMMANDS ARE ENCRYPTED AS
1000:                        ;       FOLLOWS.
1000:                        ;       COMMAND CODE                INSTRUCTION        OPCODE
1000:                        ;       0                           READ               1AAAA11X
1000:                        ;       1                           WRITE              1AAAA011
1000:                        ;       2                           RESET WRITE ENABLE 11111000
1000:                        ;       3                           STORE              11111001
1000:                        ;       4                           SLEEP              11111010
1000:                        ;       5                           SET WRITE ENABLE   11111100
1000:                        ;       6                           RECALL             11111101
1000:                        ; '1'S ARE USED INSTEAD OF DON'T CARE TO DISTINGUISH BETWEEN DATA AND
1000:                        ;  NON DATA OPERATIONS.
1000:                        ;*********************************************************************************
1000: 0000                   DIRECTION1      .EQU        00.
1000: 0002                   PORT1           .EQU        02.
1000: 0080                   TEMP1           .EQU        080H    ;RAM STORAGE FOR DATA
1000: 0082                   COUNT           .EQU        082H    ;COUNTER VARIABLE
1000: 0084                   DATUM           .EQU        084H    ;DATA STORAGE
1000: 0086                   ADDRESS         .EQU        086H    ;ADDRESS STORAGE
1000: 0088                   ERRORDATA       .EQU        088H    ;ERROR DATA
1000:                        ;*********************************************************************************
1000:                        ;                       PROCEDURE INIT
1000:                        ;       THIS PROCEDURE INITIALIZES THE X2444 INTERFACE
1000:                        ;*********************************************************************************
1000: 86 1B                  INIT    LDAA        #18H            ; B=1011, I/O 0,1 AND 3 OUTPUTS, 2 INPUT
1002: 97 00                          STAA        DIRECTION1      ; WRITE TO DATA DIRECTION REGISTER
1004: 4F                             CLRA                        ;SET CE TO 0(INACTIVE), DOUT AND SK TO 0
1005: 97 02                          STAA        PORT1           ;AND STORE IN DATA PORT
1007: 39                             RTS                         ;
1008:
1008:                        ;*********************************************************************************
1008:                        ;       SHIFTER ROUTINE- SHIFT1
1008:                        ; THIS ROUTINE TAKES THE DATA IN THE A ACCUMULATOR AND CLOCKS IT MOST
1008:                        ; SIGNIFICANT BIT FIRST INTO THE X2444.  THE FLOW IS SHIFT A BIT, TOGGLE
1008:                        ; THE SERIAL OUTPUT(6801) ACCORDING TO STATE, AND TOGGLE SERIAL CLOCK
1008:                        ;*********************************************************************************
PAGE -  2  X2444             X2444 DRIVER PROGRAM FOR 6801
File: X2444          CODE AS OF AUGUST 22, 1983   Minimal Driver for X2444, 6801 Version 3.0

1008: C6 08                  SHIFTOUT LDAB       #08.            ;LOAD THE BIT COUNT WITH 8
100A: D7 82                          STAB        COUNT           ;STORE IN COUNTER
100C: 49                     SHIFT1  ROLA                        ;SHIFT BIT INTO CARRY BIT
100D: C6 14                          LDAB        #14H            ;WE SET DATA OUT TO ZERO, WHILE SETTING CHIP
100F:                                                            ;ENABLE.  SERIAL CLOCK IS LOW.
100F: 24 xx                          BCC         TRANS           ;IF BIT IS A ZERO, THEN TRANSMIT
1011: CA 02                          ORAB        #02H            ;IF IT IS A ONE, THEN SET DATA OUT
1013: D7 02                  TRANS   STAB        PORT1           ;STORE THE DATA INTO THE PORT
1015: CA 01                          ORAB        #01H            ;AND SET THE CLOCK FOR A TRANSITION
1017: D7 02                          STAB        PORT1           ;BY WRITING A 1 TO SERIAL CLOCK
1019: C4 1A                          ANDB        #1AH            ;KEEP THE DATA VALID, BUT SET SK TO ZERO
101B: D7 02                          STAB        PORT1           ;AND STORE IN THE PORT
101D: C6 14                          LDAB        #14H            ;TOGGLE CLOCK DOWN, SET DOUT TO 0, BUT KEEP
101F: D7 02                          STAB        PORT1           ;X2444 SELECTED
1021: 7A 0082                        DEC         COUNT           ; DECREMENT THE BIT COUNTER
1024: 26 E6                          BNE         SHIFT1          ;IF COUNT IS NOT ZERO, TRANSMIT NEXT BIT
1026: 49                             ROLA                        ;ONE MORE ROTATE TO PRESERVE INSTRUCTION
1027: 39                             RTS                         ;RETURN FROM SUBROUTINE
1028:                        ;*********************************************************************************
1028:                        ;                       SHIFTIN ROUTINE
1028:                        ; THIS SUBROUTINE SHIFTS IN 8 BITS OF DATA INTO THE A ACCUMULATOR FROM THE
1028:                                 TO ENTER WITH THE CLOCK LOW
                                                    OUTPUT TO THIS
```

external to the 6801 microcomputer. Configuration information can be stored in the X2444 at time of manufacture which the 6801 can then determine upon Power-on-Reset to control the features and functions of its particular microwave. Additional X2444s can be added on the serial bus as user or model options. These optional X2444s require only an additional chip select, and can be used for such features as increased recipe storage or operational modes. The X2444's non-volatile memory also can be used for calibrating the temperature probe and storing the response time of the magnetron to allow quick calibrations or more complex and precise temperature-control algorithms.

General applications

There are many other areas in the appliance field which are natural applications for the X2444. Since most electronic appliance controllers utilize the single-chip microcomputer, the X2444's serial bus is the ideal solution their non-volatile storage needs.

"User-programmable" parameters such as favorite stations, cooking algorithms or preset time-of-day events all make the appliances more "user-friendly" especially if these parameters are retained in the event of power loss. System configuration parameters can be stored in the X2444 to allow the design of appliances in a modular fashion, substantially reducing development costs while increasing the reliability of each new product. System status saved in the X2444 in the event of a power failure is restored upon Power-On so that the system can complete interrupted tasks as well as ensure that the appliance is left in a safe and stable state.

The availability of the new 5V non-volatile memories allows the appliance designer to add more features and capabilities for a minimum cost. Whether it be used for power-failure data storage, or as user set-up information, the X2444 will make appliance designs less complex, more cost-effective, more fault-tolerant, and easier to use. □

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NONVOLATILE MEMORY GIVES NEW LIFE TO OLD DESIGNS

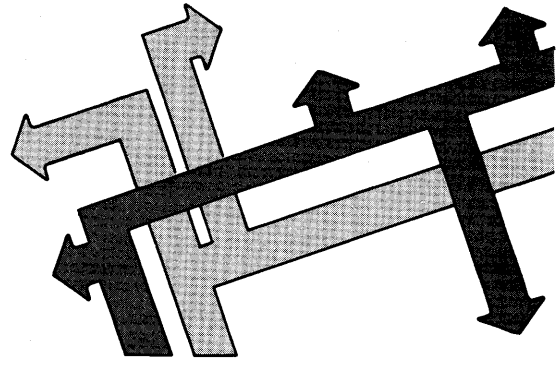
Terminals and other equipment can be made more flexible, and product life can be extended by upgrading and customizing with NOVRAMs and EEPROMs.

by Richard Orlando, *Xicor, Inc., Milpitas, Calif.*

The recent appearance of low cost, 5-V nonvolatile memories has led to design applications that can be broken into two distinct classes. One class uses nonvolatile memory to store such data as configuration or calibration parameters. This information can be updated and then stored in the device for access on power-up. The second application uses nonvolatile memory for program storage. Here, the nonvolatile memory's main advantage is that content can be updated or changed remotely, rather than by device replacement.

Unfortunately, many end products completed prior to the availability of these devices are threatened by newer designs. The latter take advantage of the added flexibility and features afforded by nonvolatile memory. There are, however, ways to add nonvolatile memory to existing designs without a major redesign.

For example, consider the schematic of an intelligent terminal design, which will be used to illustrate methods that improve the flexibility of almost any microprocessor-based design (Fig 1). Here, the 6800 processor is the source of the "intelligence" in the design. The serial communication channel is through a 6551 asynchronous communication interface adapter (ACIA), which features an onchip baud rate generator. A 2716 erasable PROM is the program store for the 6800, and the two 2114 RAMs provide 1 Kbyte each of buffer, stack, and parameter storage. The keyboard is an ASCII-encoded type whose inputs are fed through one port of a 6821 peripheral interface adapter (PIA). The other port of the 6821 receives the dual inline package (DIP) switch settings for such user-defined operational parameters as baud rate, parity, and protocol selections.



Video control is provided by a 68045 (or 6845) CRT controller. The display RAM interface is set up as a tightly coupled, shared RAM interface. The timing

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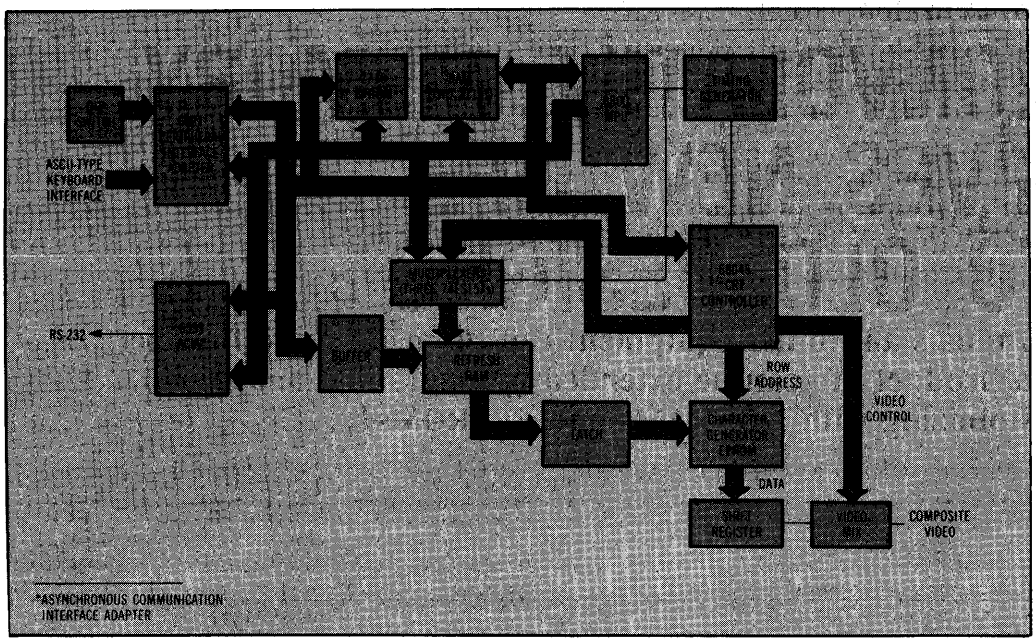

Fig 1 The original terminal design has dual inline package (DIP) switch settings that must be read by the processor. They are then parsed to determine setup parameters invoked from the terminal program contained in the EPROM.

is such that the CRT controller only accesses the data in the display RAM during the bus "dead" time of the 6800. This allows the processor to access the data in the display RAM at any time, regardless of the state of the CRT controller. The CRT controller can access the RAM transparent to the processor, and thus can relieve the processor of any access arbitration tasks.

Improving the design

Although the design serves its initial purpose, several areas, which will make it more flexible and possibly extend the life of the product, can be improved. Intended for use in a variety of applications, the original design relies primarily on software for its characteristics and "feature set." Simple changes to the erasable PROM containing the 6800's software allow such terminal "customization." This approach is adequate when end-user needs are known prior to manufacture. However, if a user wants to upgrade an existing terminal, someone must perform a costly EPROM change in the field. The same penalty applies to the manufacturer who wishes to "upgrade" the software of the existing units in the field, in order to increase performance or to eliminate possible errors.

The second area in need of improvement is the DIP switch used for the input of user-definable parameters. It creates many manufacturing problems, since most DIP switches cannot be handled by automated assembly equipment, such as insertion machines and wave solderers. Additionally, because someone must manually toggle the switch through a sequence of positions in order to fully test the boards, DIP switches slow down automated board testing. Also, to change parameters, a DIP switch requires the terminal user to remove an access panel and manipulate switch toggles while referring to a manual. As the range of user-definable parameters expands to include such features as emulation modes, the problem becomes even more awkward.

In the example terminal, added features and enhancements can be made in two ways. The first involves replacing the DIP switch with an X2443 serial NOVRAM, which is used to store user-defined setup and configuration parameters. The second replaces the EPROM with an electrically erasable PROM.

The NOVRAM, a 256-bit serial device, is organized as 16 words of 16 bits each. All communication between the device and the processor is done in a bit-serial fashion using the data in input, data out output, and the synchronous clock lines shown in Fig 2. All operations are controlled by the microprocessor through the serial interface. Read and write operations are executed through the transmission of a specific 8-bit instruction code with an embedded address of the word to be accessed. In the write operation, the processor follows the write command with 16 bits of data to be written. In the

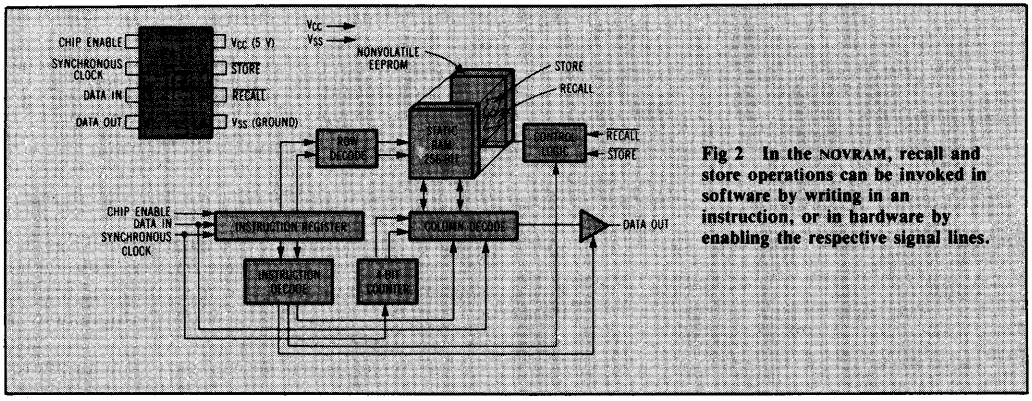

Fig 2 In the NOVRAM, recall and store operations can be invoked in software by writing in an instruction, or in hardware by enabling the respective signal lines.

read operation, the processor supplies the read instruction, and then gives the X2443 16 clock cycles, which the device uses to output the data to be read. The NOVRAM also includes several non-data types of instructions to control the nonvolatile operation of the part, the part's power consumption, and the write/store lockout feature.

The X2443 is designed to interface with single-chip microcomputers when the main consideration is minimizing I/O lines and software overhead. This device also works well in microprocessor-based designs requiring upgrading with minimal design changes. It consists of a serial static RAM overlaid or "shadowed" bit-for-bit with a 5-V EEPROM array, as shown in Fig 2. The execution of a store operation, either from the input $\overline{\text{STORE}}$ or by the execution of the software store instruction, transfers the current contents of the SRAM *en masse* into the nonvolatile EEPROM array. In a similar manner, the execution of a recall operation, via the $\overline{\text{RECALL}}$ input, transfers the contents of the nonvolatile EEPROM array into the SRAM array. On power-up, the contents of the EEPROM array are automatically loaded into the RAM array for a default configuration.

When using the X2443 to replace an existing DIP switch, it is advantageous to drop the NOVRAM into the existing switch "footprint." Fig 3 shows the simple conversion of the existing site or socket (a) to accept the X2443 (b). Four of the eight 6821 I/O lines used to read the DIP switch are already mapped into pins 1 through 4 of the NOVRAM.These lines originally input the current settings of the DIP switches, but can be configured through the 6821's data direction register to serve as the three outputs and one input needed for interfacing the NOVRAM. Since hardware $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ signals are not needed in this application, they are simply tied to V_{CC}. All nonvolatile operations occur through software control, whose requirements are relatively

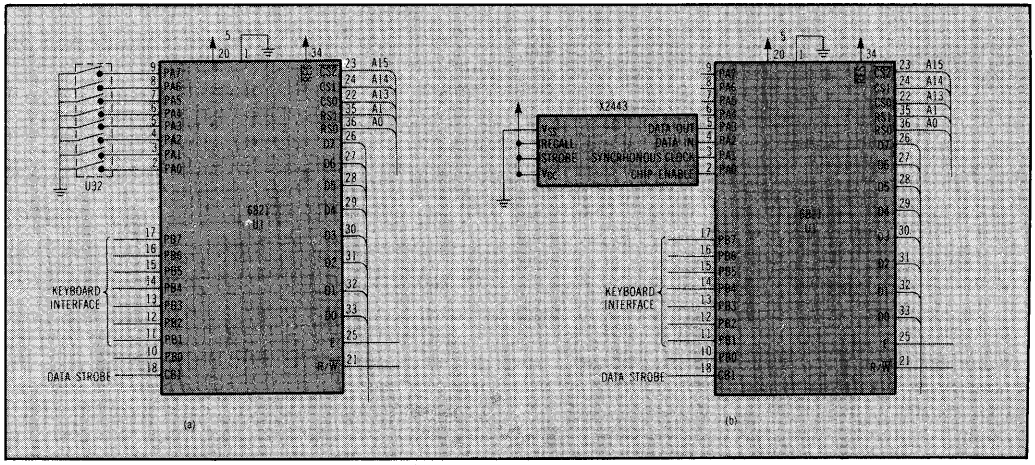

Fig 3 Within both the original DIP interface (a) and the X2443 implementation (b), the interface is serial. Therefore, only the clock, enable, data input, and data output lines need to be used.

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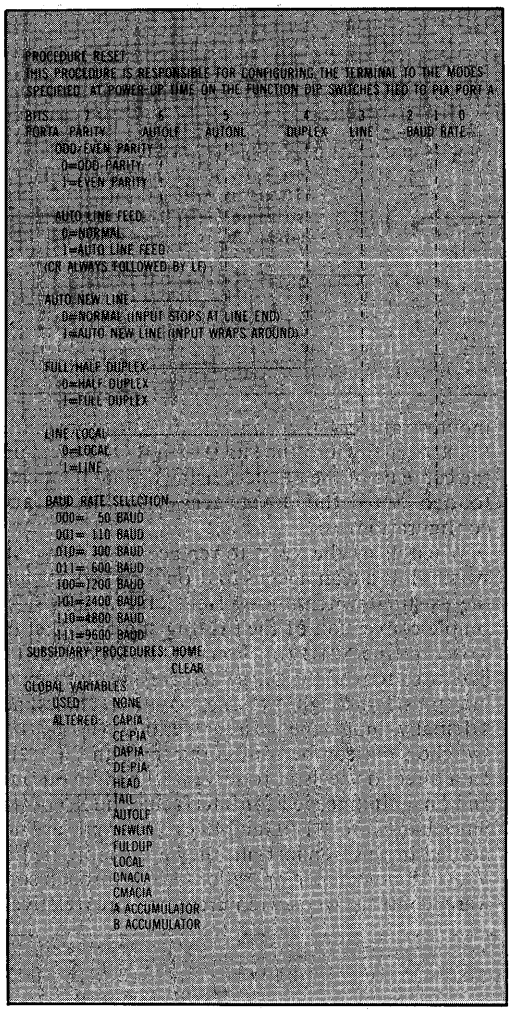

Fig 4 When using a header for a parsing program used with the DIP switch configuration, the possible parameters are limited to 8 bits, and an elaborate software routine is needed to interpret them.

straightforward (as described). With this software in place, the communication between the processor and the device simply becomes a series of reads or writes to the appropriate serial device locations.

The original design only allowed eight user-definable inputs, since only one DIP switch is used in the terminal. The meaning of the various input conditions is shown in the DIP switch map portion of the program header in Fig 4. Since the single 8-bit input is used for so many functions, parsing the input byte into the appropriate setup parameters requires an extensive piece of code. The problem with this implementation is the extensive software required to make switch operation straightforward in the user's manual.

Replacing the DIP switch with the NOVRAM has several significant advantages. The 256-bit nonvolatile storage leaves adequate room for storing an "image" of all interface circuit registers. Thus, the parsing problem of the DIP switch implementation is eliminated. Even the control registers that do not need to be user-programmable can benefit from this imaging, since they can be changed remotely in the field for hardware or software updates. This method simplifies field upgrading when compared with the usual method of storing these register images in the program store ROM or EPROM.

New images can either be down-loaded remotely or loaded through a diagnostic mode using a direct-connect RS-232 interface. Examples of where this capability is beneficial are numerous, and include changing interface protocols, data formats, or other hardware, interface, or networking options.

The use of the device for storing setup parameters also allows a more user-friendly operator interface. Software in the original design includes routines that allow random placement of the cursor or text through the use of a "go to X-Y" routine. It becomes a fairly trivial task to implement a menu-driven setup mode. After entering a certain escape sequence, the user is placed in the configuration mode, which presents an English menu.

The return key increments the cursor position to the next setup area where the current setting is displayed, and the spacebar key increments that setting through all possible choices. Once the user has set up the parameters for a particular session, depressing the escape key writes the current settings into the RAM section of the NOVRAM. With this operation, the user can set up a temporary configuration without changing the default parameters in the EEPROM section of the NOVRAM. Default settings are changed only when the user executes a certain control sequence (such as control X and then the escape). In some applications, it may be desirable to allow only certain users to change these default parameters before entering a special code.

Replacing the DIP switch with the NOVRAM allows increased design flexibility, as well as reduced manufacturing and testing costs.

Since the X2443 has a much larger capacity than actually needed for this application, the remainder of the nonvolatile storage can hold such data as serial number of the individual unit, revision level, and hardware configuration diagnostic parameters. Otherwise, it can be reserved for future expansion. The Table shows a sample address map for the

NOVRAM Address Map

Location	Bit map	Interpretation
0	XXXXXXXSWWXBBBB	S = Stop Bit Control WW = Word Length BBBB = Baud Rate
1	XXXXXXXXPPPETTRD	PPP = Parity Check Controls E = Normal/Echo Mode TT = Transmit Controls R = Receiver Interrupt Enable D = Data Terminal Ready Control
2	XXXXXXXXEEEEEEEE	E = Emulation Designator (1 of 256)
3	SSSSSSSSSSSSSSSS	S = Serial Number
4	RRRRRRRRRRRRRRRR	R = Revision Level
5	XXXXXXXXXXXXXXXX	L = Latch data from keyboard on high-to-low or low-to-high

X = Don't Care

device, with the associated data stored in each of the 16-bit locations. The end results of replacing the DIP switch with the NOVRAM are increased design flexibility, as well as reduced manufacturing and testing costs.

Program storage considerations

The second aspect of improving the terminal design involves the program store for the 6800 microprocessor. The original design uses a 2716 EEPROM since the software requirements for the terminal are not extensive. The feature set of the X2816A EEPROM makes the replacement easier because EEPROMs of the X2816A generation incorporate high voltage generation, address and data latching, and the write-cycle timing circuitry on the memory chip. During read operations, the device functions just like the 2716 EPROM in its use of chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) signals. During a write operation, the X2816A latches the addresses on the bus during the high to low transition of the write enable ($\overline{WE}$) signal, and then latches the data to be written on the rising edge of the $\overline{WE}$ signal.

The duration of this signal is not important, since the EEPROM only uses it to initiate the write cycle; the timing for the write operation is generated on-chip. The processor needs only to ignore the EEPROM for 10 ms during the write cycle, and the device does the rest. The latched and self-timed nature of the X2816A allows it to be placed in a 16-K SRAM socket and be read and written with the same signals used for the SRAM.

The read operation of the X2816A is the same as that of the 2716 EPROM, so this part of the EEPROM operation is of no concern. The only changes required to the existing circuitry involve the write operation. The first change allows the processor to write to the EEPROM, and the second protects the EEPROM from unwanted write operations during power-up and power-down.

The memory map for the original design was not very full, so only large blocks of the address map are decoded for each memory device and I/O chip on the bus. The 2716 logically resides at addresses F800 through FFFF since the 6800 reset vectors must be included. The physical decoding for the 2716 includes the address range of F000-FFFF since only the microprocessor's two most significant address lines A15 and A14 are used for the decoding.

Since line A14 is used to drive the $\overline{OE}$ line of the 2716, the EPROM is selected whenever A15 is a logical one. Possible conflict with the system RAM residing at 8000-81FF is avoided by restricting the processor's access to the 2716 in the logical F800-FFFF range. Since the processor can now read and write to the logical address range of the 2716 socket, the $\overline{CE}$ must also be derived from the A15 and A14 address lines. And, since $\overline{CE}$ is active low and the address line is active high, a simple NAND gate will suffice (Fig 5). Luckily, an extra NAND gate in the

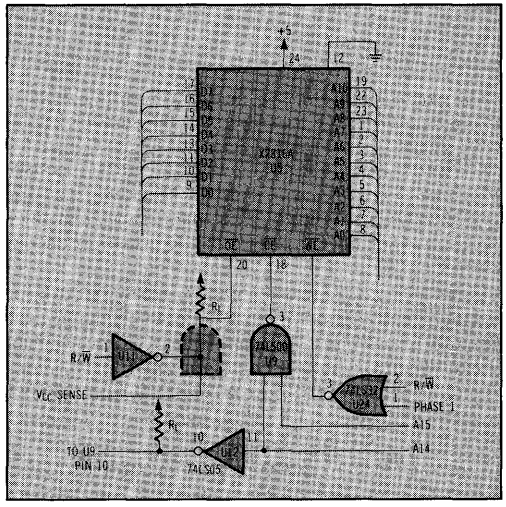

Fig 5 The EEPROM control logic uses the processor's high order address lines to map the device into the proper address range and enable it at the same time.

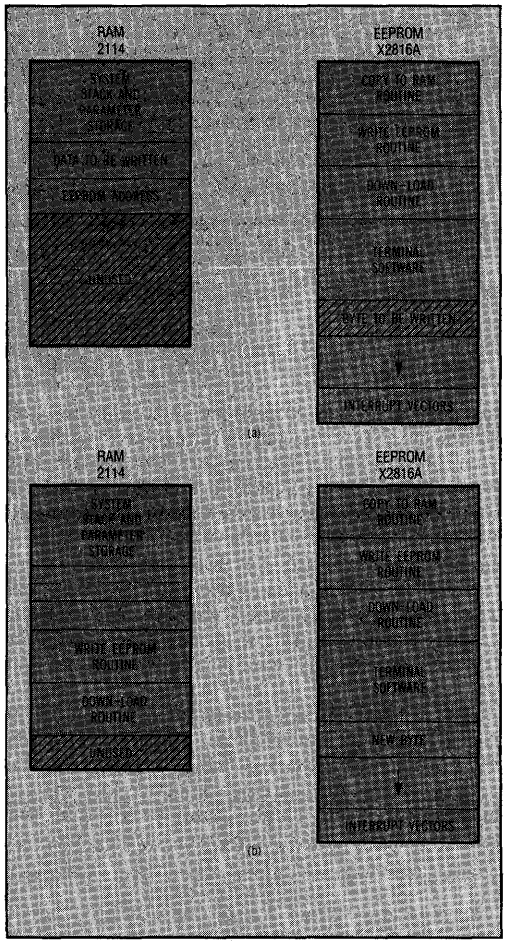

Fig 6 Address maps for updating EEPROM software are kept in EEPROM (a) and copied to RAM (b) when needed.

design can be used as an inverter. The inverter used for the $\overline{CE}$ is no longer needed, and therefore can replace the NAND gate. The inverter on A14 must remain intact since it is used in the 2114 RAM decode circuit.

The $\overline{WE}$ line for the X2816A EEPROM can be derived from the composite RAM write signal used for the 2114 RAMs. This signal is the logical OR or the R/$\overline{W}$ output from the 6800 and the Phase 1 clock signal. This qualification of the R/$\overline{W}$ line ensures that the addresses are valid on the high to low transition of the $\overline{WE}$ signal. Therefore, they can be latched into the EEPROM. This ORing connection also guarantees that the data to be written is valid on the rising edge of the composite $\overline{WE}$ signal. The $\overline{OE}$ signal on the EEPROM can simply be driven from the complement of the R/$\overline{W}$ signal from the processor. This technique requires that all accesses to the EEPROM be made in the logical address range of F800-FFFF to avoid bus contention with the system RAM.

Discussion of the circuitry needed for the $\overline{OE}$ signal also must include another important issue: ensuring that the chip does not experience an accidental write cycle during power-up or power-down. Even though the chance of $\overline{CE}$ and $\overline{WE}$ going low during power-up or power-down is rather remote, the possibility must be eliminated.

The EEPROM simplifies write protection by including an onchip voltage sensor that monitors the V_{CC} input level and automatically disables writes from occurring when V_{CC} falls below 3 V. Also, a noise filter on the $\overline{WE}$ input prevents a write from being initiated by a low spike. Functional interaction of the control inputs on the chip allows a low level on the $\overline{OE}$ to disable any write operations regardless of the state of the $\overline{CE}$ and $\overline{WE}$ inputs. By holding $\overline{OE}$ low while V_{CC} is between 3 and 4.75 V, inadvertent write cycles are inhibited.

The power supply must be modified to generate an active low signal whenever V_{CC} is below a specific level. This signal disables the write operation during both power-up and power-down. Because this signal is wire-ANDed with the control signal driving the $\overline{OE}$ signal, all writes to the chip are disabled when V_{CC} is below the 4.75-V limit.

Software modification

Once hardware changes have been made, in-factory modifications and in-field modifications must be addressed in order to take full advantage of an X2816A. In-factory modifications can be handled in many ways. If the terminal configuration is known at assembly time, the appropriate software can be loaded into the EEPROM through the use of a standard PROM programmer. However, this method does not take full advantage of the features of the in-circuit reprogrammability inherent in the X2816A. A more advanced approach also makes automated board testing easier.

For example, the EEPROM can be initially installed with a diagnostic program for testing the completed terminal board with an automated test system. Once the board has been tested, the tester controls the 6800 processor by holding it in a quiescent state such as reset or halt. The tester then assumes control over the terminal bus and writes the actual terminal software into the EEPROM. This greatly reduces the overhead required to manufacture a variety of different configurations or "models" on a single assembly line. In-line programming also allows for the verification of the EEPROM write operation and control circuitry.

The real advantages of the EEPROM surface when it comes to modifying software in the field. In this case, the terminal is placed in a down-load mode,

and the software revision is loaded through the RS-232 interface, either from a service "box" or remotely via a modem. The X2816A allows the terminals in the field to be called over phone lines for loading new operating software, thereby greatly reducing the cost and impact of a software update.

Although full-featured EEPROMs such as the X2816A simplify this task significantly, there remains one software issue to be resolved. While the EEPROM is performing its internal write cycle, it is unavailable for further writes or reads. For example, the processor, executing out of a program stored in the EEPROM, might perform a write cycle to the chip and then fetch the next instruction. Since the X2816A is occupied with its internal write cycle, the next instruction fetch will yield a high impedance bus. The processor will take this data as its next instruction and enter the "catch fire and die" mode of operation.

To avoid this situation, a very compact routine fetches the byte to be written into the EEPROM from a given location, writes the byte into the EEPROM, and then enters a timing loop to wait the 10-ms period required to complete the write. Since the RS-232 interface supports full handshaking, there is no chance of overrun from the down-loaded data. This routine is initially loaded into the EEPROM, but it is never executed from this device. Instead, another "copy to RAM" routine copies the routine from EEPROM into RAM, from which it is executed.

Since the terminal has 1 Kbyte of RAM capacity, there is ample room for storing such a routine during the EEPROM write cycle. Fig 6 shows address maps for both the EEPROM (a) and the RAM (b) prior to and during the execution of the EEPROM write routine. This method works especially well with the 6800 since its architecture is that of a von Neumann machine, and can therefore execute program segments out of the memory space reserved for RAM data storage.

In-field terminal upgradeability has two important benefits. If the terminal software is upgraded or revised after the unit is sold, the new software can be added to the existing units in the field at minimal cost. This method also eases the addition of optional hardware in the field, since the new software supporting the hardware option can be down-loaded instead of replacing the terminal EPROM.

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NOTES

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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Save volatile data during power loss

8

Save volatile data during power loss

Nonvolatile-storage devices give you a medium in which to store data during power loss. By combining these devices with power-sensing circuits and supplying the necessary control signals, you can design a system that transfers data securely between volatile and nonvolatile memory during power loss.

Xicor, Inc.

To protect volatile data during power loss, you need to transfer that data reliably to nonvolatile memory during the transient and return it to RAM after power is restored. A system that performs this function includes two subsystems. The first reports power status, indicating when power is lost and when it is restored; the second handles the data transfer, using the power-status signal to generate the appropriate store and retrieve commands.

Sense power failure

To transfer data reliably after power loss, a system must have enough time to copy data from RAM to nonvolatile memory before the supply voltage drops below a certain level. The sensing circuit must recognize the power loss and generate a power-loss signal promptly, giving the storage subsystem enough time to effect the data transfer. In fact, in some systems, you may have to complete your transfer within a single write cycle to ensure a reliable transfer.

Your first step in designing the sensing subsystem is to choose a sensing point. You could use the 5V regulator's output as a sensing point, but this output will not indicate power loss as quickly as will either the ac input line to the power supply or the unregulated dc voltage supplied to the regulator.

To sense ac loss on the power supply's ac input line, you can monitor either the input or the output to the power transformer. If you monitor the transformer's input side, you must electrically decouple the sensing circuit's signal from the system's dc portions (by using optoelectronic isolators, for example). If you monitor

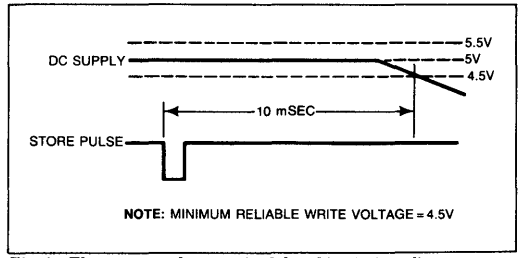

Fig 1—The system characterized by this timing diagram *must detect a power loss early enough to allow it to generate a store pulse 10 msec before the dc supply drops to 4.5V.*

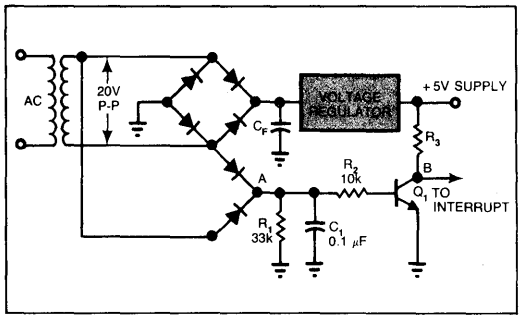

Fig 2—This zero-crossing detector *monitors power-supply status at the transformer's ac output. The two diodes isolate the detector from the main power supply's unregulated dc bus.*

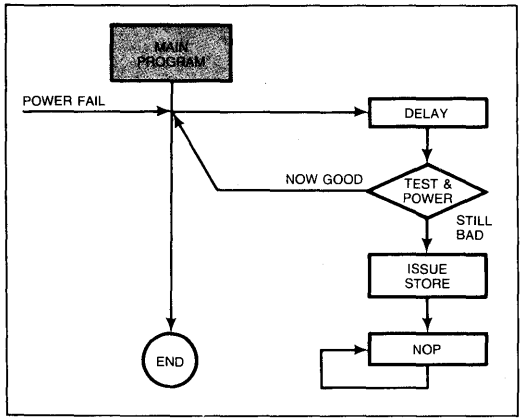

Fig 3—In a typical μP system *that tests for power loss, once the processor receives an interrupt indicating a power loss, the system initiates a subroutine that tests for a true power loss. The subroutine first produces a delay of about 2 msec; then the system looks again at the power detector's output. If that output is still asserted, the system decides that the power loss is real and sends a store pulse to the nonvolatile RAM.*

the output side, you must isolate the detector circuit from the main power supply's filtered unregulated dc circuit, because that circuit's response to a line fault is slow. To isolate the circuit, you can use either a separate transformer tap or two extra diodes between the bridge and the detector.

Alternatively, you can use the unregulated dc voltage ahead of the regulator as a sensing point. The regulator maintains its regulated output as long as its input voltage remains within a certain range. To make sure that the system will have time to respond to a power loss, you should set your trip point below the normal input voltage. This allows you to send your store signal early enough to ensure a reliable transfer to nonvolatile memory. Consider, for example, the timing diagram in **Fig 1** and assume that the minimum reliable write voltage of the memory in the system it characterizes is 4.5V. Because this system's dc supply drops to 4.5V 10 msec after initiation of the store pulse, the system must complete a write operation to nonvolatile memory within this 10-msec period.

Once you've chosen a sensing point, you must choose a detector. If you've chosen to detect ac loss, consider one of the following four methods. The first is a low-cost zero-crossing detector (**Fig 2**), in which two diodes isolate the detector circuit from the filter capacitor (C_F) that's ahead of the regulator. When a power loss occurs, the full wave's rectified ac drops to zero, inhibiting base current to transistor Q_1. This causes Q_1's output to go high, thereby generating an interrupt signal at point B.

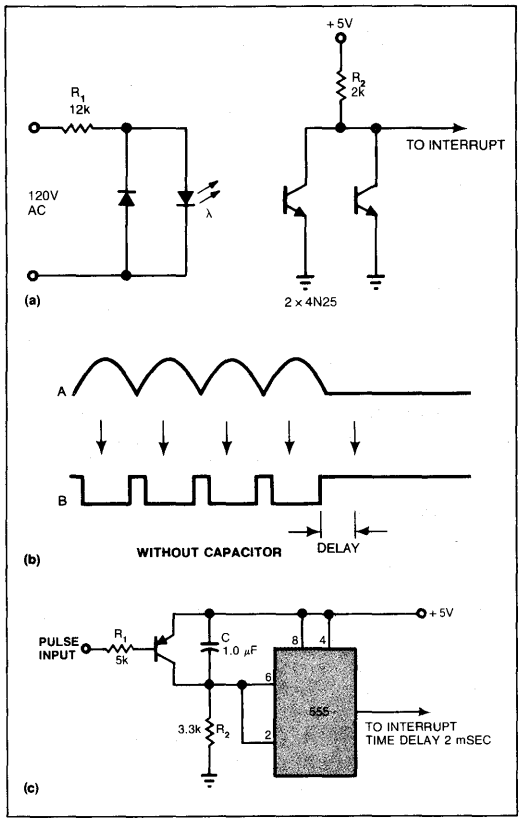

Fig 4—You can connect a detector like this one, *(which contains optoelectronic isolators with their diodes connected back-to-back) directly to the ac line through a resistor* ***(a).*** *The circuit produces an output pulse that can interrupt a μP each time the input waveform crosses zero, or every 8.3 msec* ***(b).*** *Instead of allowing the sensor to interrupt the μP every 8.3 msec, you can feed these pulses first to a 555 timer that's configured as a missing-pulse detector. It issues an interrupt only when the input pulse train is interrupted* ***(c).***

8

To ensure that you'll be able to transfer data reliably from RAM to EEPROM, you need to maintain power for at least 10 msec after a power loss.

When it receives an interrupt, the system initiates a subroutine that tests for a true power loss (**Fig 3**). The subroutine delays the store signal for about 2 msec and then looks at the detector again. If the output is still high, the system decides that the power loss is real, and it sends a store pulse to the nonvolatile RAM. Resistor R_2 in **Fig 2** limits the transistor base current.

Capacitor C_1 is essential in this circuit because it filters the power supply's half-cycle pulses before they're applied to Q_1. (If you were to fail to filter these pulses, the μP would receive an interrupt signal every 8.3 msec, whether or not a power loss had occurred. Without C_1, as much as 25% of your available processor time would be spent responding to false interrupts generated by the power-loss detector.) The value that you choose for C_1 depends on the power supply's holdup time, the values of R_1 and R_2, and the delay that you want between the loss of ac and the triggering of the store signal.

Use optoisolators

The second technique for sensing ac power loss uses two optoelectronic isolators between the detector and the ac power line (**Fig 4a**). This technique produces a positive output pulse at each zero crossing on the ac line, or at 8.3-msec intervals (**Fig 4b**). The problem with Fig **4a**'s circuit is that the interrupt signal occupies the μP's time while the rest of the system is resampling the detector's output. To solve this problem, you can add a missing-pulse detector similar to the one shown in **Fig 4c.**

A third detector that relies on direct ac-line connection uses General Instrument's MID 400 power-line monitor. When you use this device, you need to add only two resistors to ensure a clean interrupt signal (**Fig 5**). You can adjust turn-on and turn-off delays by adding a capacitor across R_2.

The fourth detector (**Fig 6**) uses a CMOS Schmitt trigger as a full-wave, low-voltage, missing-pulse detector. To avoid latch-up, and possible damage to the CMOS circuits, you must make sure that the input voltage to the CMOS Schmitt trigger does not exceed the 5V supply voltage. You can meet this requirement by inserting a resistor between the Schmitt trigger and the bridge's output. To obtain narrow pulse widths from the first gate, keep the ac input voltage as high as possible. R_3 and C_1 determine the output's delay, which must be longer than the first gate's pulse width.

Sensing dc power loss

If you've decided to sense dc loss instead of ac loss, you don't have to worry about capacitor delays or missing pulses. Consider the sensor in **Fig 7a,** for instance. The sensor generates a negative interrupt pulse when it senses dc loss; it uses a zener diode to set the trigger point. On one hand, you should set the

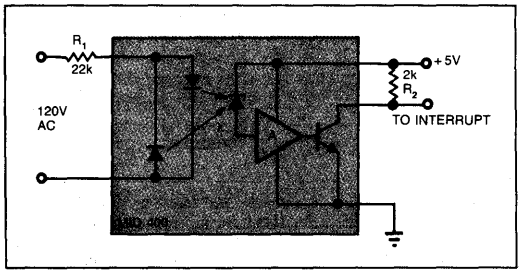

Fig 5—To incorporate the MID 400 detector *in your sensing subsystem, you need to add only two external resistors that you connect directly to the ac line. You can control the on and off delays at the output by connecting a capacitor across R_2.*

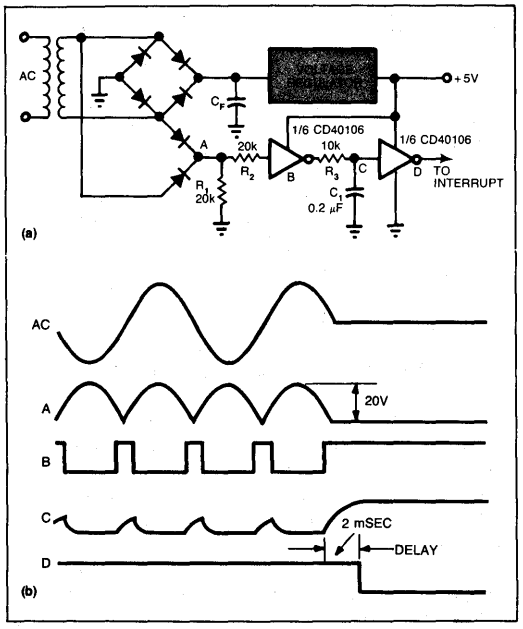

Fig 6—When you use two Schmitt triggers *to detect ac loss (**a**), the delay produced by R_4 and C_1 must be longer than the first gate's output pulse width. The timing diagram (**b**) shows the circuit waveforms.*

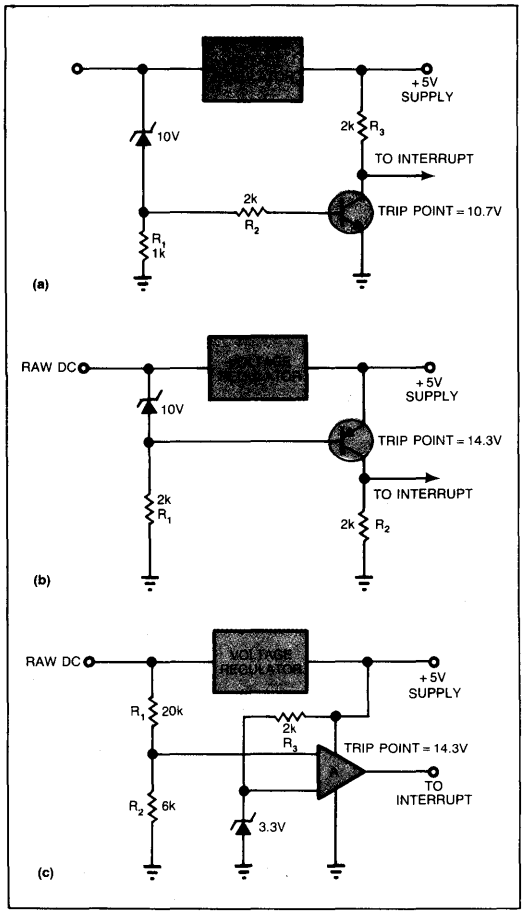

Fig 7—Using zener diodes *you can configure a power-supply detector circuit to produce either a negative* ***(a)*** *or a positive* ***(b)*** *interrupt pulse when the trigger point is reached. You can configure the op amp shown in* ***c*** *to produce either a positive or a negative output pulse polarity.*

trigger point as high as possible (to allow the circuit to sense the power loss as early as possible). On the other hand, you must still set the trigger point low enough to fall below the lower boundary of the supply's upper unregulated limit (to prevent false triggering). Remember that the diode's voltage rating should equal the desired trip-point voltage minus the 0.7V base-emitter drop.

In the dc detector circuit shown in **Fig 7b,** when the unregulated dc voltage drops, a pnp transistor turns on and produces a positive pulse. Here, the zener diode's rating is equal to the trip-point voltage minus 5V, plus 0.7V for the base-emitter drop.

The circuit in **Fig 7c** trips when the dc level at R_1's and R_2's junction drops to the zener's voltage rating. You can provide either a positive or a negative interrupt signal, depending on the operational amplifier's input configuration.

To ensure that the regulator operates long enough to perform a reliable transfer to nonvolatile memory once a store pulse is sent, you need to use a large filter capacitor. The capacitance depends on the desired trip point, the lowest input voltage to the regulator, and the load. For example, a system with a 10-msec transfer time, a 300-mA load, a 15V trip point, and a minimum regulator input of 7V requires a 375-μF capacitor; you can derive the capacitor's value from the equation i=Cdv/dt.

Once you've chosen a sensing point and a sensing circuit, the next step is to develop a subsystem that uses the power-status signal to generate save and

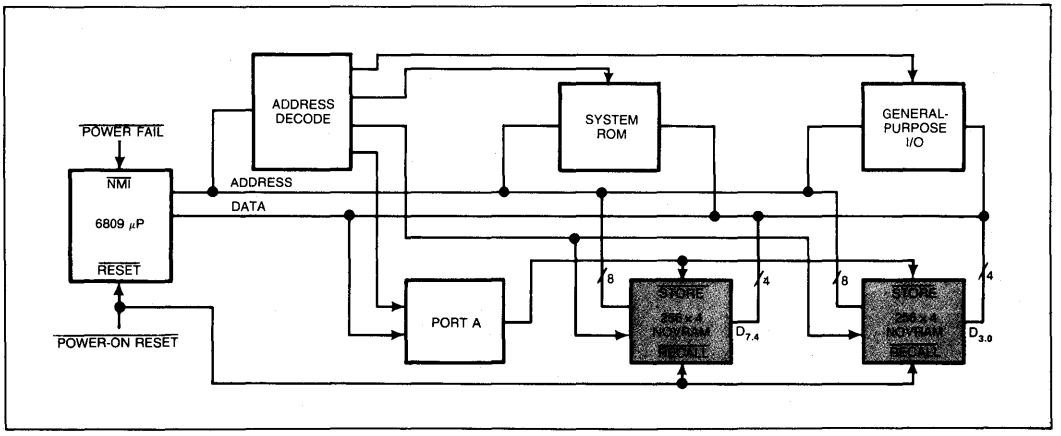

Fig 8—This industrial controller's storage architecture *uses a NOVRAM as both the volatile and nonvolatile system storage elements.*

Monitoring the ac line in front of the main supply's power transformer gives you the fastest warning of a power loss.

restore signals. These signals tell the storage subsystem to transfer data from RAM to nonvolatile memory during power loss and return data to RAM after power has been restored.

The type of system you design will depend largely on the type of nonvolatile storage that you plan to use with that system. For instance, you could use battery-backed RAM, or you could use a NOVRAM like the one used in the industrial controller shown in **Fig 8.** The industrial-controller design takes advantage of the nonvolatile RAM's ability to transfer data between RAM and EEPROM in a 10-msec single write cycle (see **box,** "NOVRAM architecture").

The nonvolatile RAM provides both the system storage (RAM portion) and the nonvolatile program storage (EEPROM portion) for power losses. The μP supplies a low-going TTL store signal (100-nsec min duration) to the nonvolatile RAM's store input. During the 10 msec that the nonvolatile RAM requires to complete its data transfer, you must keep the power supply's voltage within the specified operating tolerance. Once the system initiates a store cycle, the store cycle can't be terminated.

When the system loses power, the sensor sends a power-failure-detection interrupt to the μP. Once the processor acknowledges the interrupt, it branches to an interrupt routine that writes the current stack pointer and a test byte to the nonvolatile RAM (to signify that a power failure has occurred) and generates a store signal. The power supply holds V_{CC} above 4.5V for 10 msec after it generates the power-fail signal. During the store operation, the nonvolatile RAM I/O lines maintain high impedance, allowing the μP to complete other tasks. After the system completes a store operation, it must drive the store input high before performing subsequent store operations.

When power is restored, the power-on-reset routine sends a recall signal to the nonvolatile RAM. The routine in the μP then checks the nonvolatile RAM's test byte to see if the previous process had been interrupted by a power failure. If so, the processor saves the current processor state and loads the address

NOVRAM architecture

A NOVRAM (nonvolatile RAM) is a memory device comprising a static RAM overlaid bit for bit with an EEPROM (electrically erasable programmable ROM). A typical nonvolatile RAM, the Xicor X2212, contains 2k bits organized as a conventional 1k-byte static RAM overlaid with a 1k-byte EEPROM.

The operation of the RAM portion is identical to that of other static RAMs. However, in addition to CS (chip select) and WE (write enable) pins, nonvolatile RAMs also have store and recall pins that control data transfers between the RAM and EEPROM. Because the pulse widths of the control and data inputs are less than 450 nsec, most μP-based systems don't require wait states during the data transfers.

A store operation transfers the entire RAM contents to the EEPROM in a single 10-msec write cycle. After the NOVRAM completes the store operation, the original data will reside in both the RAM and the EEPROM.

The NOVRAM uses a recall operation to transfer data in the EEPROM to the RAM, replacing the RAM's prior content. Instead of moving data on a word-by-word basis, store and recall operations transfer the entire content of the memory simultaneously.

NOVRAMs don't require high-voltage pulses or high-voltage supplies: The devices operate from a single 5V power source and have no battery backup. All inputs and outputs are TTL compatible. The RAM portion's cycle time is 300 nsec, and the common data input/output is 4 bits wide.

On-chip protection

A built-in V_{CC} sensor protects the NOVRAM from spurious signals often initiated during power-up and power-down. The sensor establishes a threshold supply voltage of 3V. When the supply voltage falls below 3V, store operations to the EEPROM and write operations to the nonvolatile RAM are blocked.

A noise filter built into the EEPROM prevents glitches on the WE line from initiating a write cycle. This filter makes the device ignore pulses of less than 20 nsec so that noise spikes will not be interpreted as write commands.

An alternative to monitoring ac power at the power transformer is monitoring the unregulated dc power to the regulator.

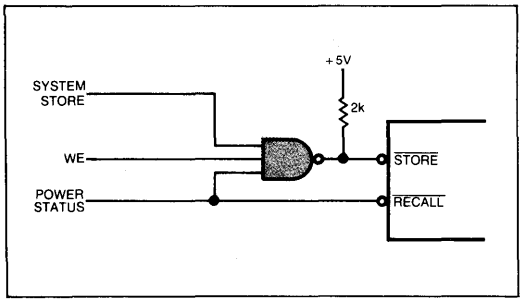

Fig 9—By NANDing the store, WE, and power-status signals *you can protect the NOVRAM from false store commands. In this configuration, all three inputs must be true for a store operation to occur.*

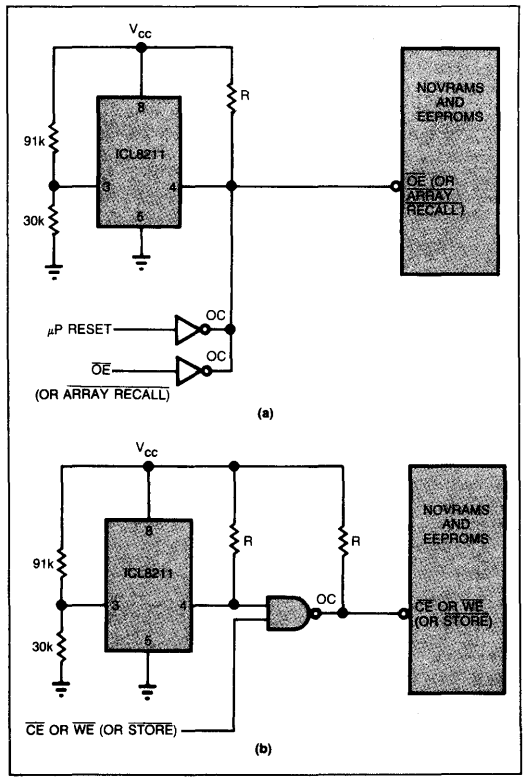

Fig 10—In a hold-low protection scheme (a), *a nonvolatile memory's array-recall pin is pulled to logical zero when the supply voltage falls below 5V. In hold-high protection* ***(b),*** *when power is lost, either the WE or CE pins are held high.*

of the saved processor state onto the stack. It then executes a return from interrupt and resumes the previously interrupted process.

Beware false commands

One of the biggest obstacles you'll face in deriving reliable store and save signals will be to avoid false store commands. Because most µP-based systems don't operate in ideal environments, they often generate false signals during power-ups, power-downs, brown-outs, and power failures. However, these signals are generally nonperiodic in nature, so the system usually recognizes them as by-products of a faulty memory device and disregards them.

Sometimes, however, these signals are periodic and turn out to be unintended write/store commands. After a system reset, for example, the µP's erratic behavior may cause the registers that usually contain the system information to contain false write-store commands instead. Therefore, when the system addresses those registers, those registers issue a false store command.

You can use several system techniques to avoid these errant commands. (For a discussion of on-chip protection features, see **box,** "NOVRAM architecture.") One technique for protecting the NOVRAM from errant commands takes advantage of the fact that even though most µPs can issue spurious addresses, they don't usually issue false write commands. By ANDing the system write command with the system store command, you can make sure that the nonvolatile RAM will respond to a store signal only during a write cycle.

Nevertheless, glitches can still appear at the store pin during power up, even if no write command is received at any of the 3-state TTL gate inputs. One way to solve this problem is to use an open-collector NAND gate, one of whose inputs indicates the power supply's status (**Fig 9**). This method ensures that the store pin's voltage follows the power supply's voltage as the voltage increases.

If you hold one NAND gate's open-collector input low, the output transistor is turned off. Pulling the gate's output voltage to the nonvolatile RAM's power supply through a pullup resistor ensures that the output follows the power supply with no glitches. You can also use the power supply's status signal to hold the recall pin low and the store pin high. This technique gives you better control over the nonvolatile RAM because it uses two conditions to prevent an inadvertent store operation. All you need to do is to connect the status signal directly to the recall pin.

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Two additional methods of preventing unintentional nonvolatile data changes during power transitions are hold-low and hold-high protection. When you use hold-low protection (**Fig 10a**), the array recall pin is pulled to logical zero whenever the supply voltage falls below the 5V−10% threshold. The Intersil ICL8211, an 8-pin miniature DIP, provides the voltage reference and gives a zero output whenever the supply falls below its threshold. When the sensed voltage rises above the selected threshold, the device produces a logical one.

(**Fig 10b**) gives an example of hold-high protection. ICL8211 keeps the voltage on the nonvolatile RAM's store pin (or the $\overline{WE}$ or $\overline{CE}$ pins) near the power supply's voltage level. This blocks the low pin voltage that's necessary for a write or store operation.

The power-supply output that ICL8211 senses is a sawtooth waveform. ICL8211's output is a logical 1 while the supply output is above 4.5 volts. Below 3V, the nonvolatile RAM's internal protection circuitry prevents inadvertent writes or stores. In the critical unprotected range between 3 and 4.5V, ICL8211 provides a zero output to prevent writes or stores.

An alternative to ICL8211 in these applications is the SGS L487. The SGS L487 is a 500-mA precision 5V voltage regulator that includes an open-collector power-on/power-off reset output pin that protects nonvolatile memory the same way the ICL8211 does.

Other schemes that protect systems from inadvertent store operations employ jumpers, cables, and switches. You transmit the store signal through a jumper or switch that you hold open unless you're changing data in the EEPROM. During normal operation, the only component attached to the store pin is a resistor to the power supply. **EDN**

Author's biography

Christopher Lopes is an applications engineer at Xicor (Milpitas, CA), where his duties include system-level evaluation, product-application development, and customer technical assistance. A member of the IEEE, Chris holds a BS in electrical and electronic engineering from California State University at Sacramento and is currently enrolled in the MBA program at the University of Santa Clara. He enjoys windsurfing, skiing, and tennis.

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THICK OXIDE BEATS THIN FILM IN BUILDING BIG EEPROMS

8

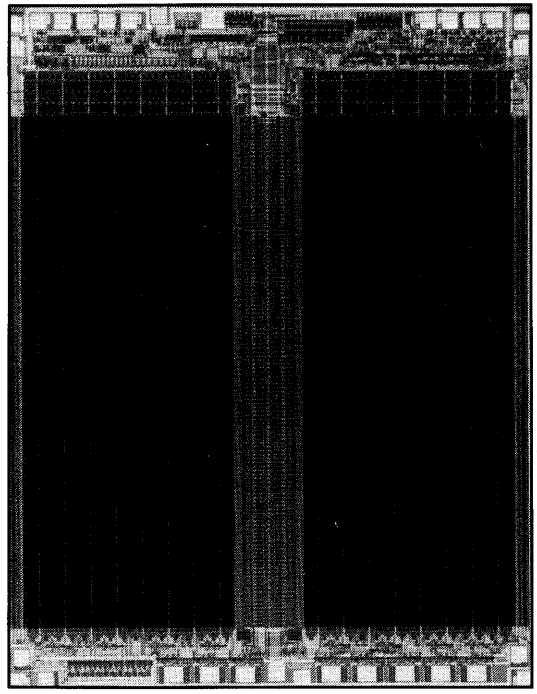
INSIDE TECHNOLOGY

THICK OXIDE BEATS THIN FILM IN BUILDING BIG EEPROMS

XICOR USES IT TO SOLVE 3-D SCALING PROBLEMS IN 256-K CHIPS

By abandoning the conventional thin-film route to fabricating high-density electrically erasable programmable read-only memories, Xicor Inc. may have overcome the problems that have kept the parts from climbing above the 64-K density level. The Milpitas, Calif., company employed a conservative 2-μm process and standard off-the-shelf 5× stepper lithographic equipment to build a 256-K EEPROM.

The key to doing this was the use of a thick oxide and a unique triple-polysilicon floating-gate cell, says William Owen, Xicor's vice president of research and development. The process is inherently more reliable and easier to scale to submicron dimensions, he claims, although it was more difficult for the Xicor engineers to master. They were less familiar with it than with the thin-oxide double-poly technology derived from EPROM manufacture.



1. SMALL DIE. Equivalent in size to many thin-oxide 64-K parts, Xicor's 256-K EEPROM die measures about 64,000 mils².

Conventionally used thin-oxide floating gates are relatively easy to manufacture, but cannot be scaled down easily without introducing significant reliability problems. This unpleasant consequence of the laws of physics is one reason many EEPROM houses are having difficulty moving to densities beyond 64-K to the 256-K level. To do so requires pushing minimum line widths on the oxides down to 1 μm using advanced photolithography.

"The problem with scaling EEPROMs lies in the fact that it is necessary to scale in three dimensions—in the vertical as well as horizontal directions," says Owen. "To achieve 256-K densities, not only must thin-oxide EEPROMs be scaled from 2 or 3 μm down to 1 to 1.5 μm in the horizontal direction, but from 90 to 100 Å down to about 70 to 80 Å in the vertical direction." To achieve similar densities in its 256-K EEPROM, Xicor found it necessary only to scale down from 3 to 2 μm horizontally and from 600 to 800 Å down to 400 Å vertically.

The thick oxide enabled Xicor's designers to form a basic EEPROM cell with a triple-poly structure that puts the programming portion atop the erase mechanism. This resulted in horizontal cell dimensions smaller than the thin-oxide structure.

Another factor in the smaller size was the use of a proprietary textured thick-oxide surface on the programming elements. The textured surface's electrical potential per unit area is greater than conventionally used smooth surfaces, producing cells that are inherently smaller than comparable thin-oxide cells, but with the same effect. The oxide can be shaved off without affecting cell reliability, making vertical scaling relatively easy.

The first 256-K EEPROM fabricated with the 2-μm process is the 32-K-by-8-bit n-MOS X28256. It features a chip area of about 64,000 mils² (Fig. 1), equal in size to many thin-oxide 64-K parts fabricated using 1.5-μm design rules, and half the size of thin-oxide 256-K EEPROMs designed with 1- to 1.2-μm geometries. Soon to follow will be a CMOS version, the X28C256. Both parts feature 150-ns access times and support 64-byte page-write operations. A write cycle takes 31 μs per byte, enabling the entire memory to be written in less than 1 second.

In Xicor's triple-poly cell (Fig. 2), the floating gate sits between the upper and lower poly layers, forming the thick-oxide tunnel structures for erasure and programming. Compared with the 80- to 120-μm² cells of conventional 1-μm thin-oxide designs, the electrically erasable cell in Xicor's 2-μm 256-K parts measure only 68 μm².

The programming tunnel mechanism occurs between the first and second floating-gate poly layers; the erase tunneling action occurs between the second and third (Fig. 3, left). As in the thin-oxide approach, a selection transistor isolates the selected cell on a column while a capacitor develops, through capacitive coupling, enough voltage across a tunneling device to make electrons tunnel on and off the floating gate. This voltage is sensed by a MOS transistor, whose gate is formed by the second poly layer.

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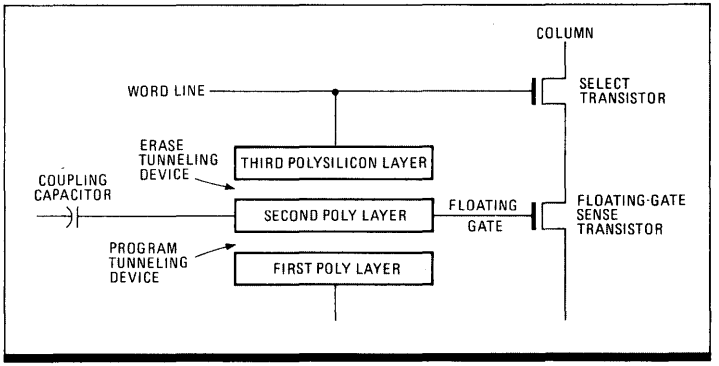


2. TRIPLE POLY. Key to the small die area is a unique triple-poly floating-gate cell. The gate, between the upper and lower poly layers, performs erasure and programming.

Because capacitance increases linearly as oxide thickness decreases, tunnel devices made with very thin oxides—80 to 100 Å thick—rate 5 to 10 times higher than tunnel devices made with 500- to 800-Å-thick oxides. Consequently, cells using thin oxide have to push photolithography requirements to the limit of available equipment and processes in order to make the thin-oxide tunneling devices as small as possible. The coupling capacitor, which must be made from a thicker, nontunneling oxide, ends up relatively large to obtain efficient coupling.

In contrast, thick-oxide tunnel devices inherently have very low capacitance. Therefore they can be made with reasonable feature sizes and still produce a small cell with good coupling-capacitor efficiency. Since the feature sizes used in the tunnel devices are compatible with the lithography requirements of the rest of the cell, they can be readily scaled down as advances in lithography technologies become available for manufacturing.

What makes this structure work is its surface, which Xicor describes as textured with hillocks (Fig. 3, right). Also called asperities, these odd-looking features were at first considered an undesirable side effect of MOS processing, and occur because oxidation progresses faster along some crystal directions than others. Because crystal orientation is random in deposited poly, there are points on the surface of an integrated circuit where oxide growth is enforced. The temperature of the oxide controls the size and shape of the hillocks.

Through the use of carefully designed and controlled fabrication techniques, Xicor exploits this phenomenon to build EEPROM transistors using thicker silicon dioxide layers that can still discharge the floating gate. Because the oxidation is a well controlled step, the properties of the emitters are exceptionally regular. They are shaped so that the electric field increases at the crest of the hills, substantially enhancing the emission of electrons.

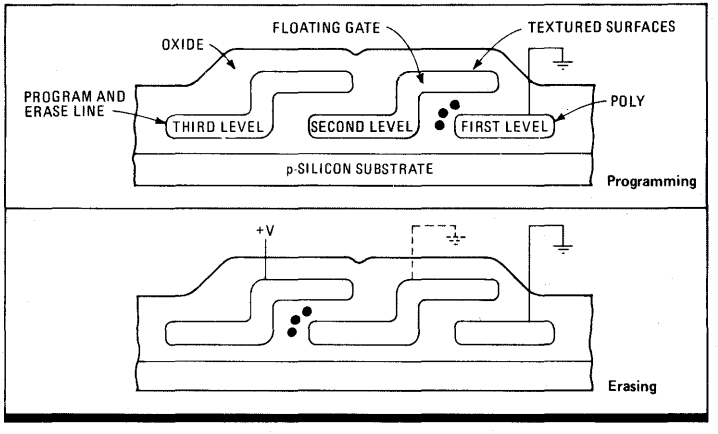
The poly electrodes are separated by oxide layers about 500 to 800 Å thick. Without the hillocks, Xicor says, 100 V would need to be applied to produce effective tunnel current. With the textured surfaces, the voltage required for tunneling is only 10 to 20 V, low enough to be generated easily on chip with an internal charge-pump circuit.

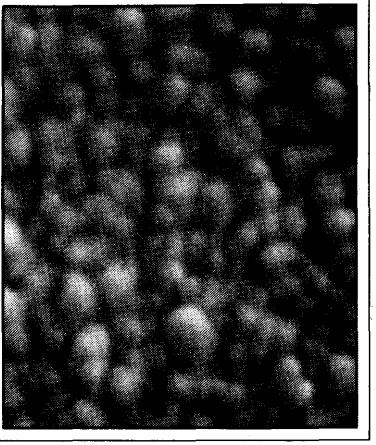
The coupling capacitor's size also contributes to the smaller cell area. To induce tunneling, the floating-gate voltage is raised or lowered through capacitive coupling to a bias-voltage supply. To avoid excessively high bias voltages, efficient coupling to the floating gate must be achieved by making the coupling capacitance much higher than all other floating-gate capacitances combined. These other capacitances include that of the MOS sense transistor, and especially that of the tunnel devices.

To electrically program a cell, electrons must tunnel onto the floating gate. In Xicor's triple-poly enhanced-emission cell, this is accomplished by applying a bias voltage to the coupling capacitor to capacitively pull the floating gate high and develop a voltage across the program tunneling device. When this voltage reaches the tunnel voltage, electrons tunnel from the first poly level's surface through the programming device to the second-level floating gate. When the applied voltages are brought back to normal reading levels, the programmed floating gate carries a negative voltage because of the extra electrons on it. When read, the MOS floating-gate sense transistor is turned off by the negative voltage and a 0 is produced at the EEPROM's output.

To electrically erase a cell, electrons must tunnel off the floating gate. In Xicor's triple-poly cell, this is done by capacitively coupling the second poly level's floating gate low while the third poly level's word line, which forms the other end of the erase tunneling device, is brought high. When the voltage across the erase tunneling device reaches the tunnel voltage,

3. TUNNELS AND TEXTURE. In Xicor's cell design, programming by tunneling action occurs between layers 1 and 2 and erasure between layers 2 and 3 (left). The thick-oxide cell approach uses a "textured" floating gate surface to enhance electron emission.





electrons tunnel from the second poly floating gate to the third poly word line. When the applied voltages are brought back to normal reading levels, this erased floating gate has a net positive voltage because of the lack of electrons on its surface. When read, the MOS floating-gate sense transistor is turned on by this positive voltage and a 1 is produced at the EEPROM's output.

Other advantages of the thick-oxide approach, says Owen, include improved data retention and endurance, or the number of data changes a nonvolatile memory can sustain before the first bit fails. Because the floating gates in the Xicor design are completely surrounded by thick thermal oxides, similar to an EPROM, data retention is excellent even at very high temperatures. "In fact, the only way retention can be measured on the thick-oxide devices is by subjecting them to temperatures over 300°C for several weeks," Owen says. "If these measurements are extrapolated, the typical retention for a Xicor EEPROM is more than 2 million years at 125°C." But for the record, the company is much more conservative, guaranteeing data retention of only 100 years at 125°C.

The data-retention advantages of the textured thick-oxide approach are retained—or even improved—as devices are scaled, he says. This is due to the fact that lower programming voltages are needed in order to scale the memory properly, so isolation widths and device channel lengths can be reduced in both the memory array and in the peripheral circuitry. However, for a typical part, which stores data in 3 ms and must retain it for 10 years, the tunneling current under storage and reading conditions must be reduced by at least 10^{11} than under programming conditions because the retention time is 10^{11} times longer than the storage time.

For planar nontextured tunneling structures, this is a difficult design constraint because the slope of the current voltage curve—that is, the relationship between the current and voltage of the tunneling device—is fixed. This means that the maximum allowable read voltage drops with the programming voltage on a volt-for-volt basis, not proportionately.

On the other hand, a textured-surface tunneling structure has a much steeper current-voltage curve; that is, for each increment of change in one voltage, there is an amplified increment of change in the other. In addition, the curve is not fixed, which means the relationship between the current and voltage can be tailored to yield steeper curves if necessary. This means that for a given maximum read voltage, a textured surface requires a lower programming voltage than a planar thin-oxide structure, leading to better scaling.

With regard to endurance, recent data on Xicor's EEPROMs indicates an expected failure-in-time rate of 0.015% per 1,000 hours, or 150 FIT, in systems requiring 10,000 data changes per byte over a 10-year period, says Owen. "Thus for many applications, the endurance-related fallout is actually similar to or lower than other semiconductor-related failure rates."

To achieve 1-Mb densities, Owen believes that although it will require moving to 1-μm geometries horizontally, only a few "tens of angstroms" reduction will be necessary in the vertical direction. "In thin-oxide EEPROMs, this is a reduction of 10% to 15% down to the operational limits of the floating-gate mechanism," he says. By comparison, Xicor's thick-oxide approach requires a reduction on the order of a few percentage points. "Moreover, the scaling is well within the limits of the Xicor cell design," he says. "As a matter of fact, we think we can continue to scale for several generations before we run into any of the problems our competitors are running into with thin-oxide EEPROMs." □

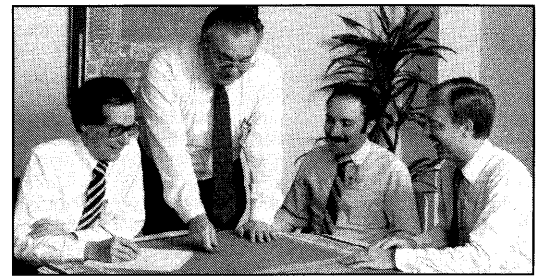
XICOR: FROM LONG SHOT TO LEADER

Life is sweet these days for Raphael Klein, Julius Blank, William Owen III, and Wallace E. Tchon, who all helped found Xicor Inc. in 1978. But they can recall the time when the Milpitas, Calif., company's chance of survival was considered a long shot.

"The problem was that few in the industry thought we had a technological edge except us," says Owen, vice president of research and development. "There was Intel Corp., with its thin-oxide approach to fabricating electrically erasable programmable read-only memories, and there was Xicor, with the thick-oxide approach. Everybody seemed to be going the thin-oxide route." All that is changing now.

First of all, it is becoming clear that the company is at least a generation ahead of its competition with its thick-oxide approach. While everyone else is pushing to 1-μm geometries to achieve 256-K products, Xicor is coasting along with a relatively conservative 2 μm to achieve the same density.

Second, thin-oxide advocate Intel has entered into a long-term agreement with Xicor for joint development of advanced EEPROMs. The deal also calls for mutual second-sourcing of EEPROMs and related products. As part of the agreement with Intel, Xicor has received $6.5 million and may receive an additional $500,000 as well as a $10 million lease guarantee.



COMING UP ROSES. The commitment to thick-oxide EEPROMs finally starts paying off for Xicor Inc.'s Tchon (left), Blank, Klein, and Owen.

Third, the company continues to dominate the market it created, 5-V-only EEPROMs. Sales have grown from $2.8 million in 1982 to $39 million in 1984. Estimates for 1986 range as high as $55 million.

Finally, Xicor had profitable operations during all four quarters of 1984 plus Q1 of 1985. It owns about 50% of the market for 5-V EEPROMs and Novrams, static random-access memories backed by nonvolatile EEPROM cells.

Klein, now chief financial officer and chairman of the board, is a graduate physicist from the Israeli Institute of Technology and performed in a variety of technical management positions at Fairchild, Intel, Monolithic Memories, and National Semiconductor before starting Xicor as its first president. He holds two patents.

Owen, who joined the company to direct its development of advanced memories in 1978, holds an MS in electrical engineering and previously worked at Intel. As a process engineer and senior design manager, he was involved in the development and design of Intel's HMOS memory products.

Strategic planning vice president Tchon, who joined Xicor to aid in the development of its initial memories, is now principally involved in business planning, patent activity, and investor relations. With an MS in physics, Tchon holds 10 patents. Before Xicor, he held engineering positions at Honeywell Information Systems and Intel.

Blank, one of the original eight founders of Fairchild Semiconductor Corp. in 1957, has been a member of the Xicor board of directors since its founding.

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MACHINE DESIGN

A PENTON/IPC PUBLICATION

TECH BRIEFS

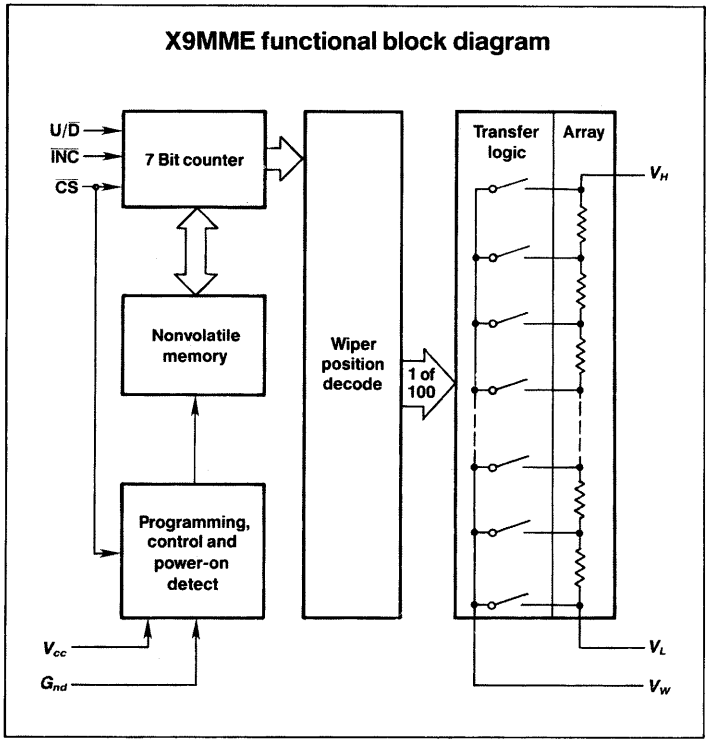
SOLID-STATE POTENTIOMETER

RICHARD PALM
Applications Engineer
Xicor Inc.
Milpitas, CA

Potentiometers play a vital role in circuit design, yet they have a number of problems. Their settings can change when exposed to vibration. They are difficult to use with automatic insertion and soldering equipment. And trimming must be done by hand.

A solid state potentiometer solves these problems. Packaged in an eight-pin minidip, an electrically erasable (E^2) device called the X9MME digitally controls resistance trimming. The device has three-wire TTL control and operates from a standard 5-V power supply. Packaged in the dip is a 99-resistor array. Tap points are between the resistive elements and at the ends of the array. A tap point can be connected to the wiper output V_W.

X9MME functional block diagram



Because the resistive elements are all equal, each has 1/99 the total resistance of the array. In a voltage divider application, moving the wiper up or down the array produces a linear output on V_W, with a resolution of 1%.

The tap point on the array is selected with three TTL inputs on the digital portion of the device. These inputs control a seven-bit up/down counter. To move the wiper tap point, the "chip select" line must be activated (CS = LOW), the wiper direction selected (U/D, up = HIGH, down = LOW), and a clock pulse provided to the INC input. Counter output is decoded to select one of 100 tap points.

Mechanical potentiometers essentially have a nonvolatile memory; resistance does not change until the wiper is moved. In the X9MME, seven bits of nonvolatile E^2 memory retain the resistance value. When the device is deselected after a wiper position change, the counter output is stored in memory. If power is re-

8

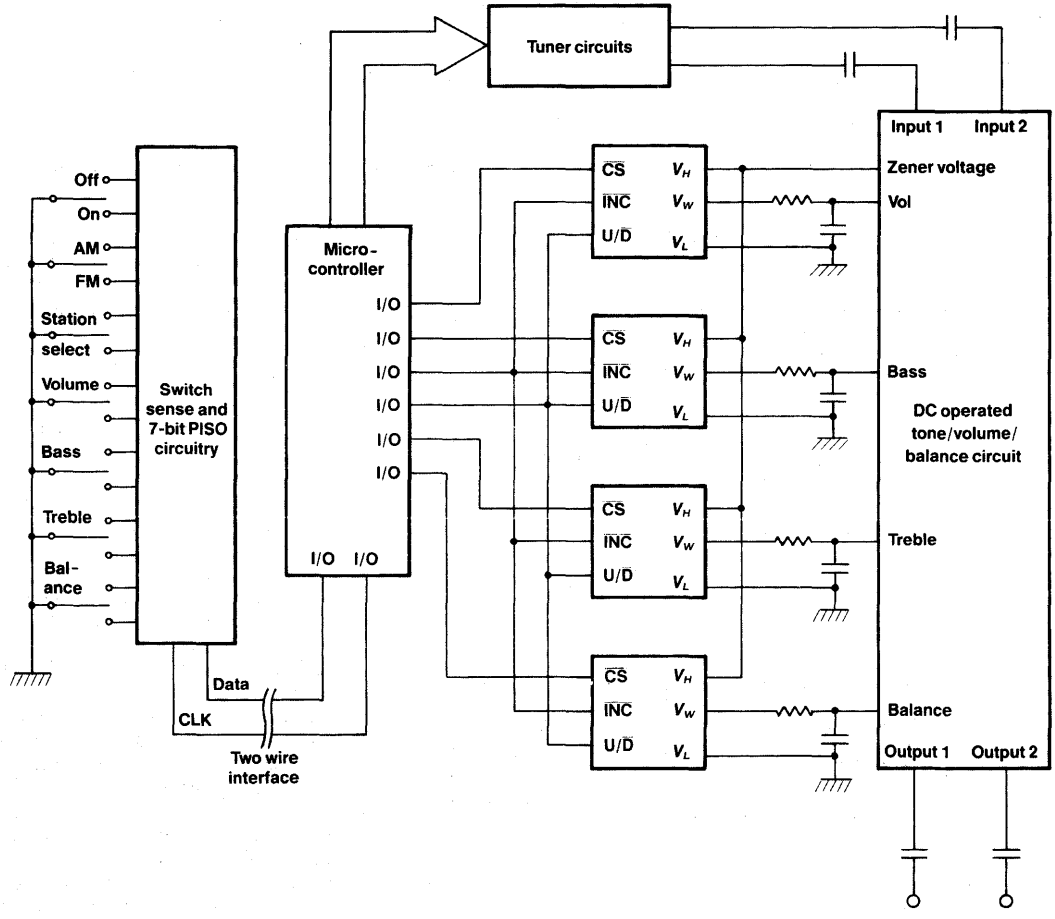
moved and subsequently restored, the nonvolatile memory contents are transferred to the counter and the last stored wiper position decoded. Wiper position retention is 100 years.

The manufacturing and test cost of equipment produced in high volumes can be reduced when solid state pots are used. Because automatic insertion equipment can be used, the device is soldered and cleaned just like other electronic components. This eliminates special handling and cleaning steps. During board testing, automatic test equipment (ATE) can check the device and set wiper position. Hand operations are reduced, and the cost of supplemental test equipment is eliminated.

Operator convenience can also be of prime concern in circuit design. If the equipment operator or field technician must access the pot to make adjustments, the design process is complicated. The X9MME, in contrast, can be placed anywhere in the circuit and still be controlled through keyboards or a microprocessor.

As an example of how circuitry can be simplified, consider a hypothetical car radio system. Control might be by miniature rocker switches mounted on the steering wheel. The switch sense and 7-bit parallel-in-serial-out circuit could be implemented in either discrete TTL circuits or as a standard cell or programmable logic device. The microcontroller interface would be two wires, one for the shift clock and another for the interrupt and data transfer. The microcontroller actuates off/on, AM/FM selection, and tuning. Six port lines control volume, bass, treble and balance. ■

Microprocessor controlled radio



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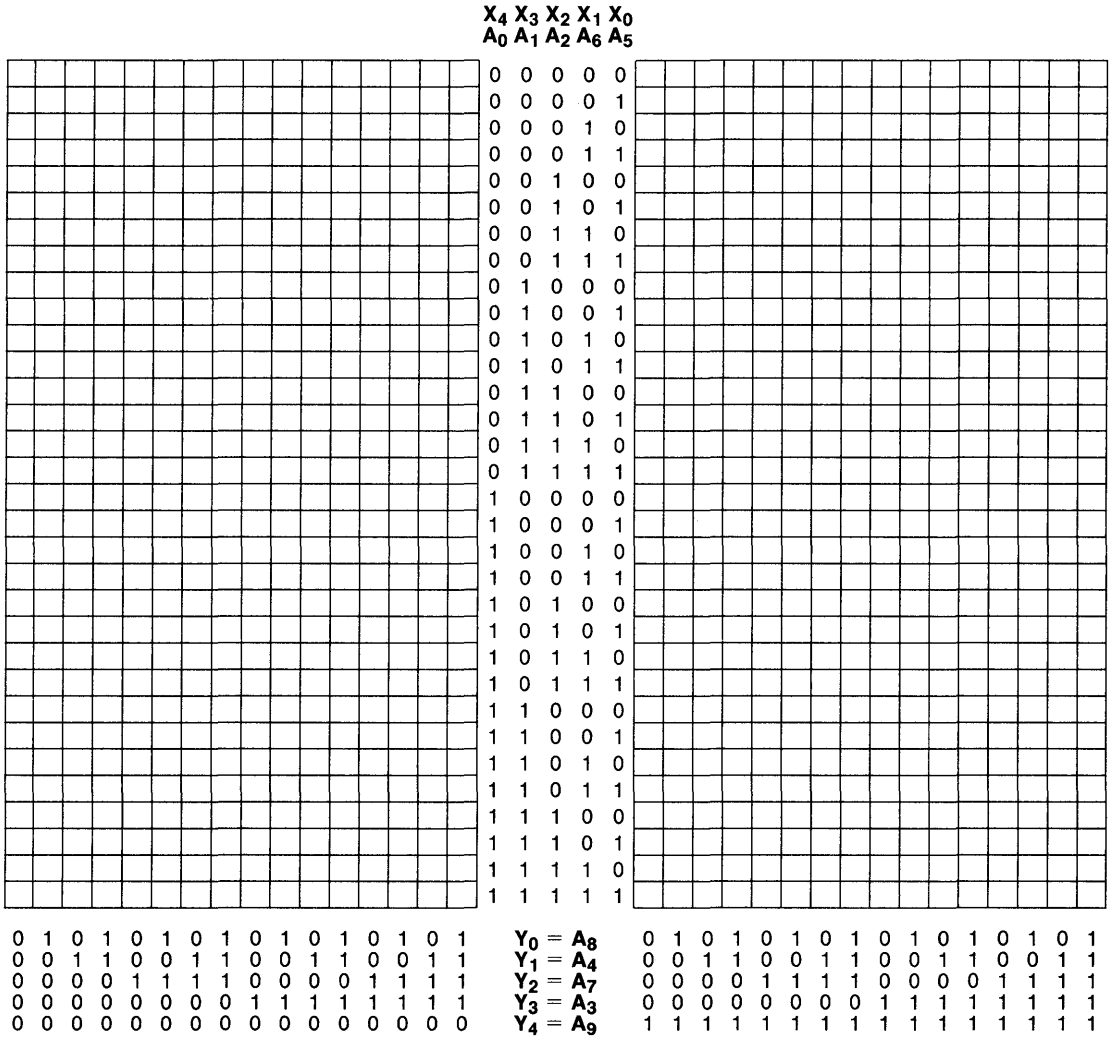
Nonvolatile Static RAM

On the following pages are individual device bit maps. These bit maps are supplied to aid in the development of test programs.



0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

$Y_0 = A_8$
$Y_1 = A_4$
$Y_2 = A_7$
$Y_3 = A_3$
$Y_4 = A_9$

0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1
0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1
0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

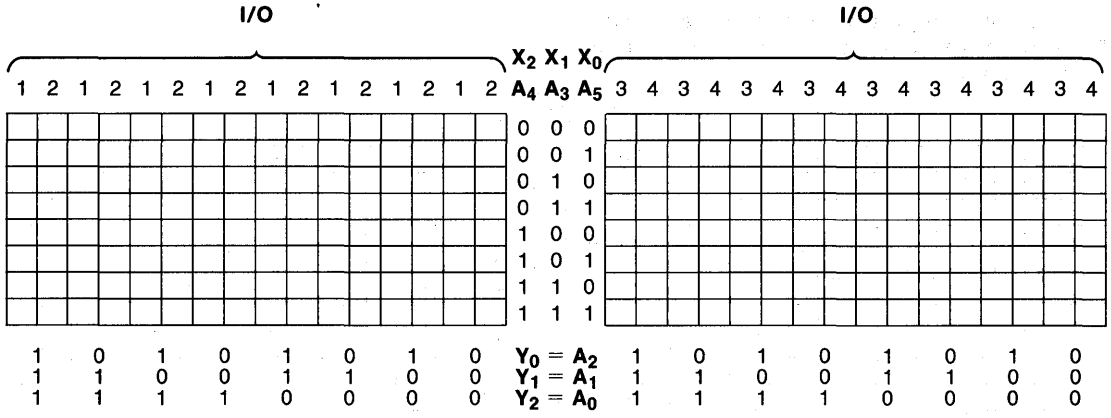
Each Square Equals One Bit.

Address to XY Key

A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Y_4	Y_0	Y_2	X_1	X_0	Y_1	Y_3	X_2	X_3	X_4

8

Nonvolatile Static RAM

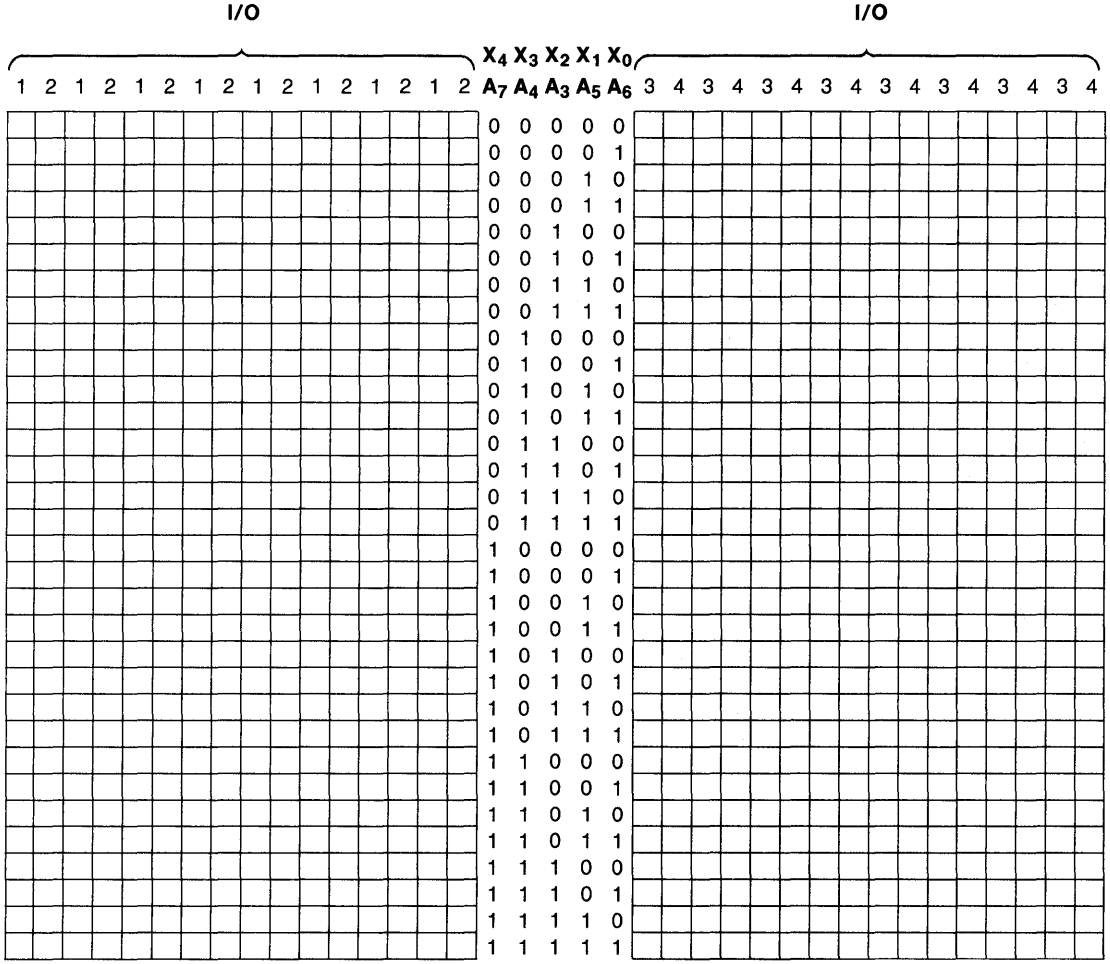


Each Square Equals One Bit.

Address to XY Key

A_5	A_4	A_3	A_2	A_1	A_0
X_0	X_2	X_1	Y_0	Y_1	Y_2

Nonvolatile Static RAM



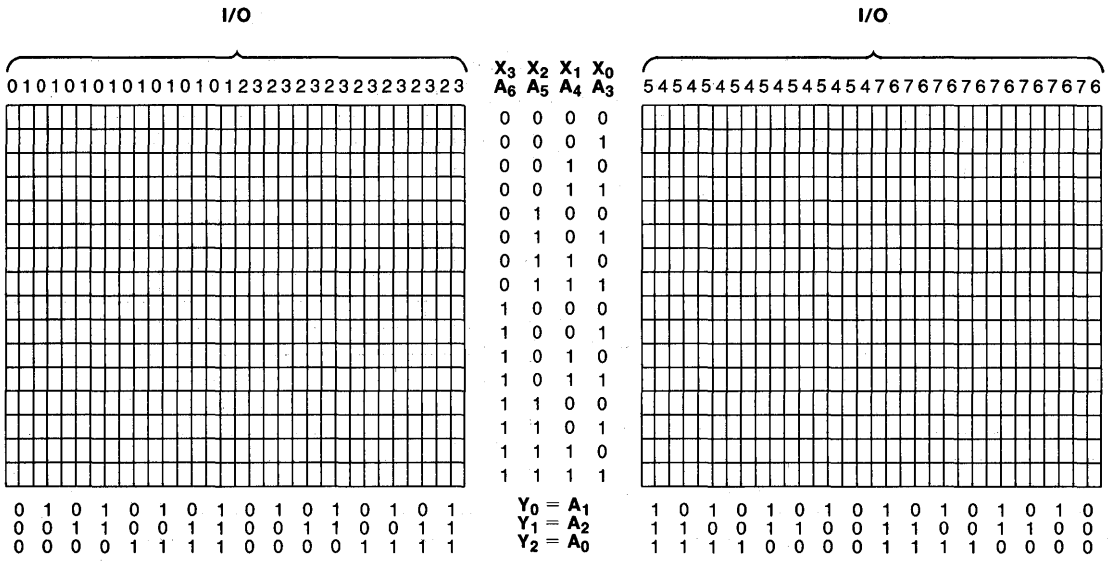
Each Square Equals One Bit.

Address to XY Key

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_4	X_0	X_1	X_3	X_2	Y_0	Y_1	Y_2

8

Nonvolatile Static RAM

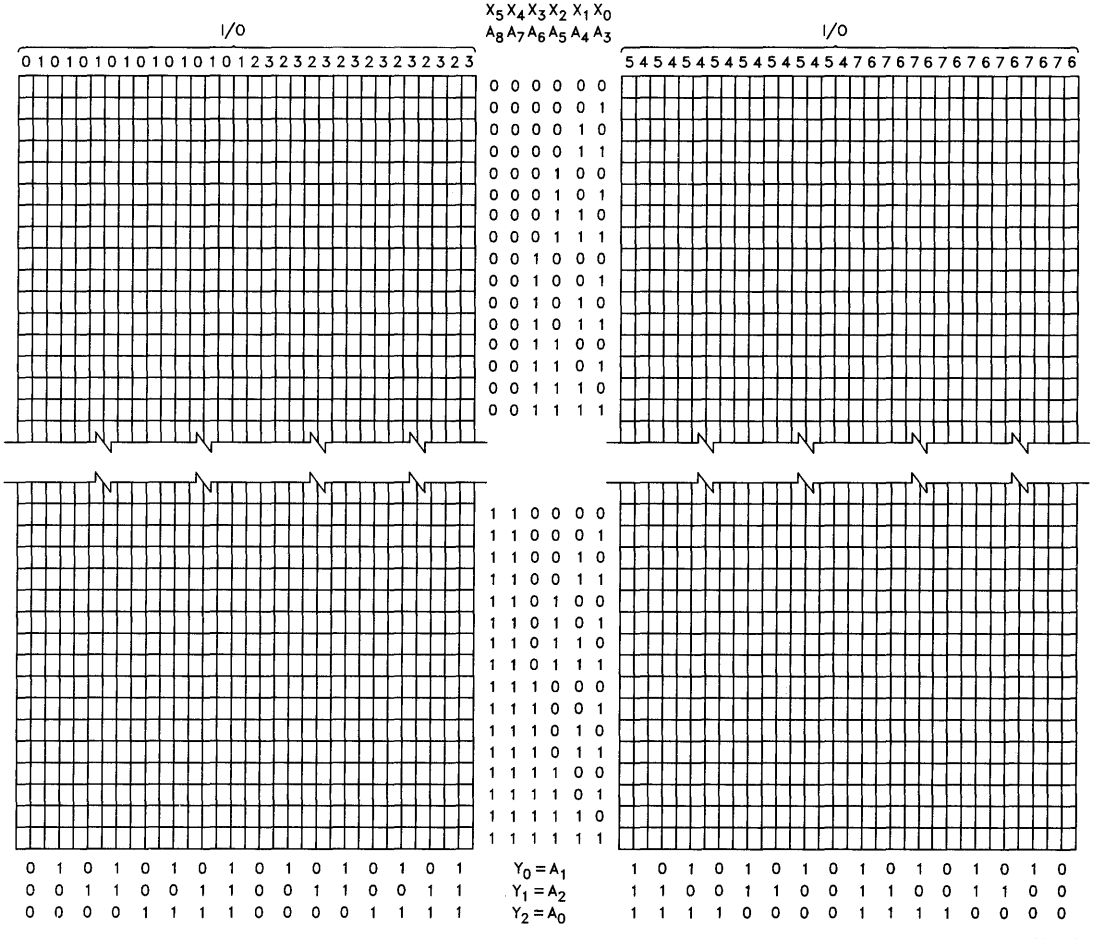


Each Square Equals One Bit.

Address to XY Key

A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_3	X_2	X_1	X_0	Y_1	Y_0	Y_2

Nonvolatile Static RAM



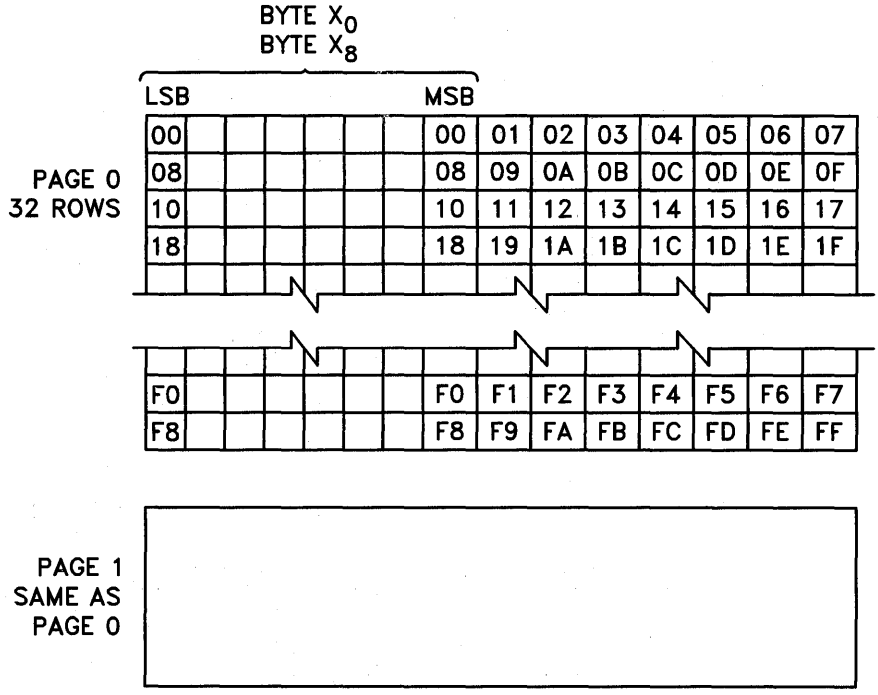
0025-8

Each Square Equals One Bit.

Address to XY Key

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_5	X_4	X_3	X_2	X_1	X_0	Y_1	Y_0	Y_2

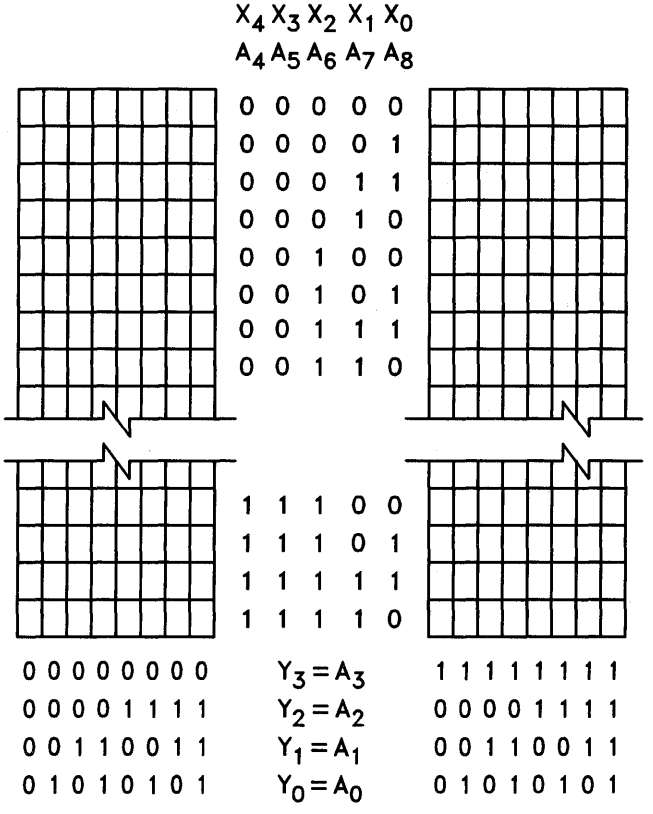
8



0025-1

Each Square Equals One Byte.

Electrically Erasable PROM



0025-2

Each Square Equals One Byte.

Byte Map

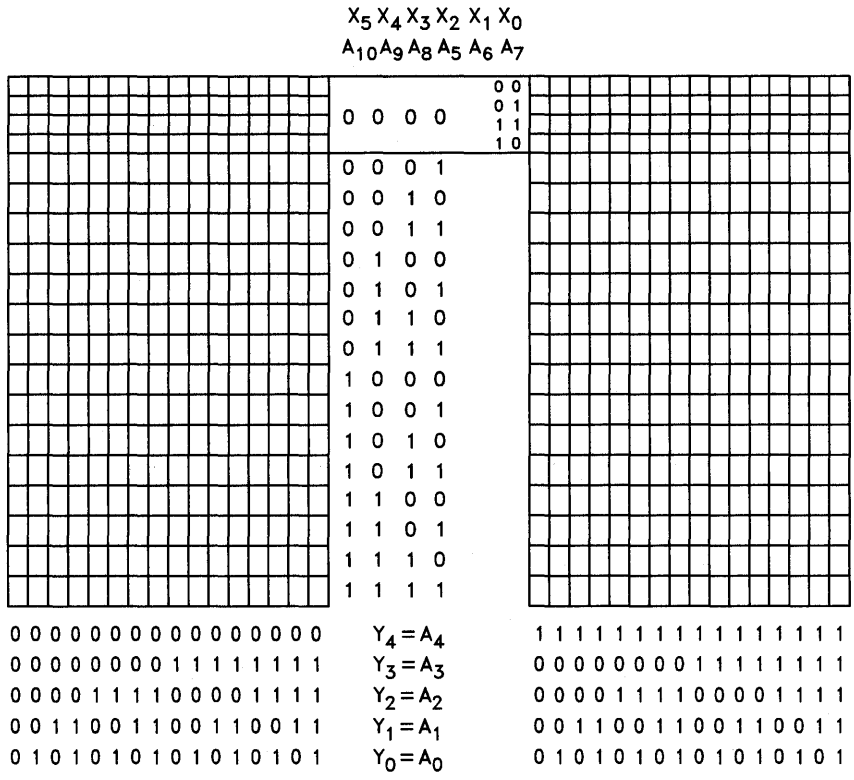
I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7

Address to XY Key

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_0	X_1	X_2	X_3	X_4	Y_3	Y_2	Y_1	Y_0

8

Electrically Erasable PROM



0025-4

Each Square Equals One Byte.

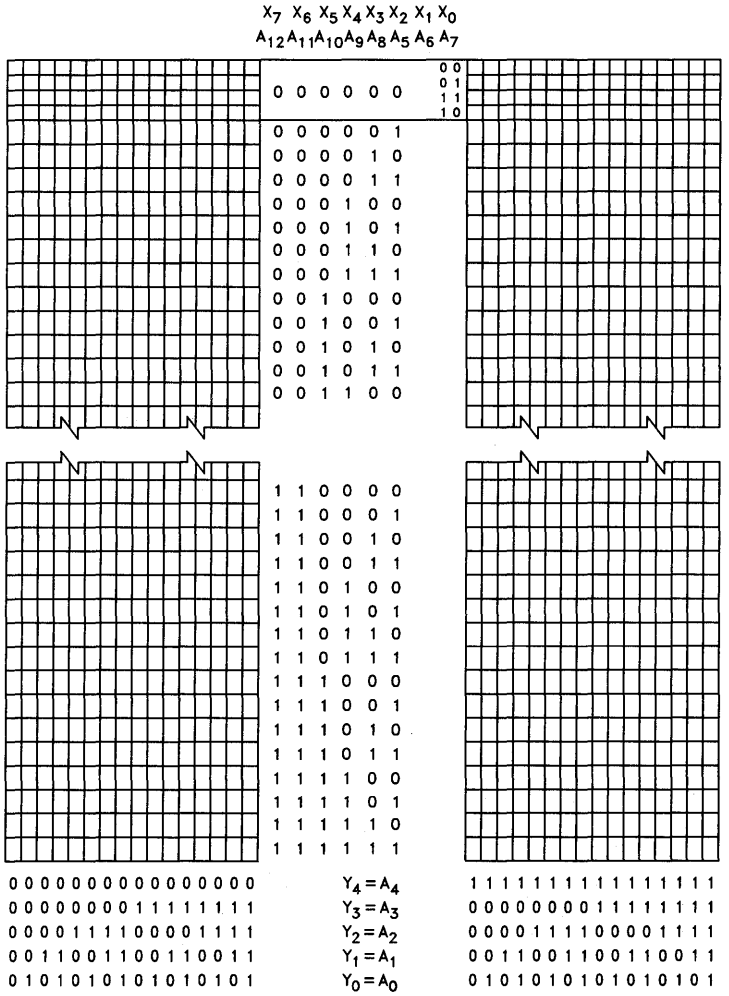
Byte Map

I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7

Address to XY Key

A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_5	X_4	X_3	X_0	X_1	X_2	Y_4	Y_3	Y_2	Y_1	Y_0

Electrically Erasable PROM



0025-5

Each Square Equals One Byte.

Byte Map

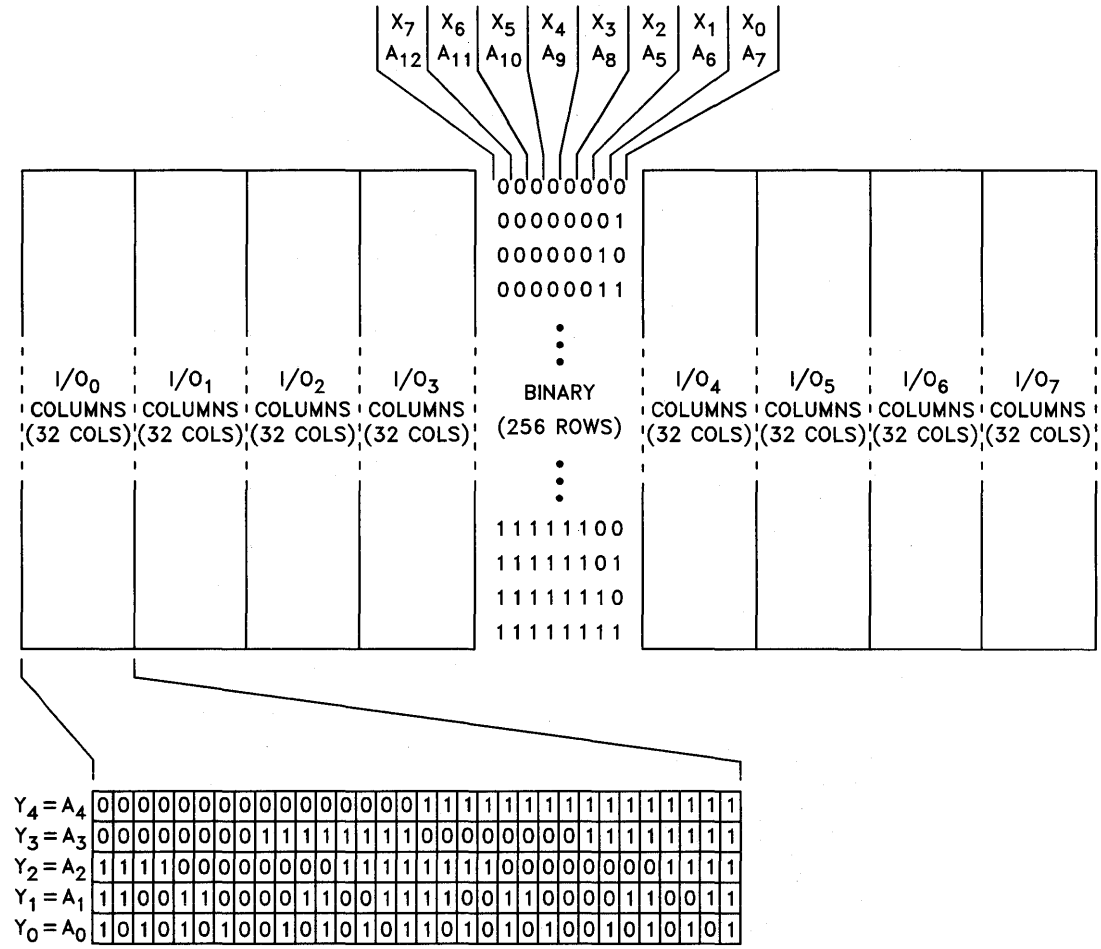
I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7

Address to XY Key

A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_7	X_6	X_5	X_4	X_3	X_0	X_1	X_2	Y_4	Y_3	Y_2	Y_1	Y_0

8

Electrically Erasable PROM

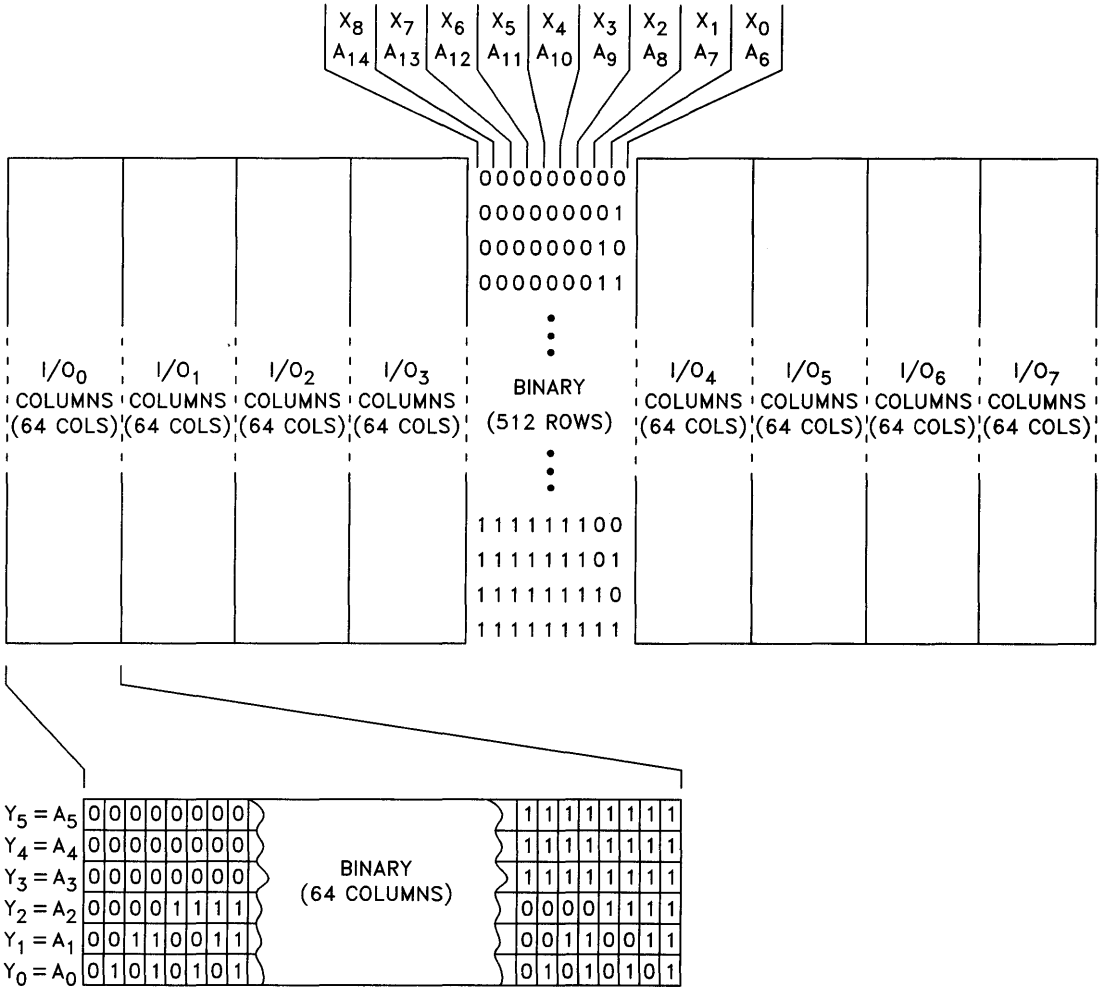


0025-6

Address to XY Key

A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_7	X_6	X_5	X_4	X_3	X_0	X_1	X_2	Y_4	Y_3	Y_2	Y_1	Y_0

Electrically Erasable PROM



0025-7

Address to XY Key

A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

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NOTES

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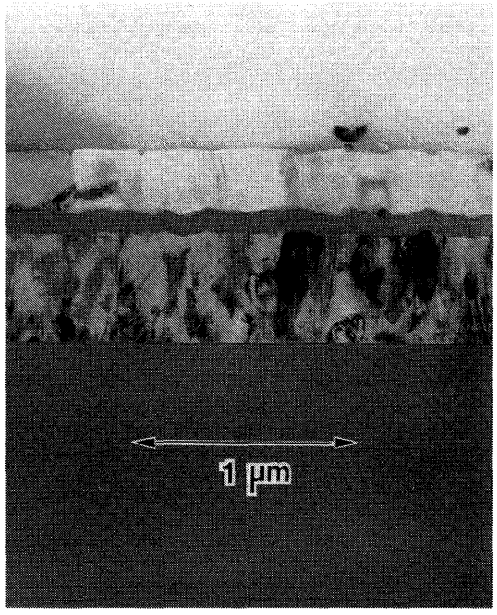


0075-1

NOVRAM* RELIABILITY REPORT

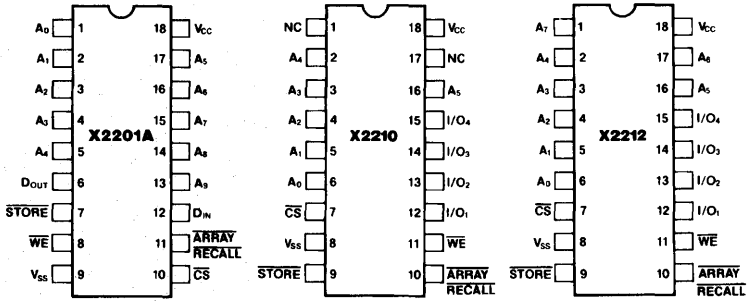
By John Caywood
and Reliability Engineering Staff

9

*NOVRAM is Xicor's nonvolatile static RAM device.

INTRODUCTION

This report is an accumulation of reliability testing data taken on the Xicor X2210 and X2212 NOVRAM memories. In these memories, each memory bit integrates one bit of static RAM and one bit of electrically erasable-programmable ROM (E^2PROM) into one cell. The controls STORE and RECALL cause the data to be transferred in parallel from all RAM bits into the associated E^2PROM bits and back again. These devices, which exemplify Xicor's innovative technology, require only a 5V power supply and TTL level signals for all operations, including STORE and RECALL. Both devices employ the same design and processes and are organized 64 x 4 and 256 x 4 for the X2210 and X2212, respectively. Figure 1 shows the pinout for the two parts, as well as for the X2201A (1K x 1) NOVRAM. Figure 2 shows the logic diagram. The bit maps for the three devices shown in Figures 3–5 illustrate the physical location of the various address bits.



0075-2

PIN NAMES

A_0–A_9	Address Inputs
I/O_1–I/O_4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY}$ $\overline{RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Figure 1: X2201A, X2210, and X2212 pin assignment drawings.

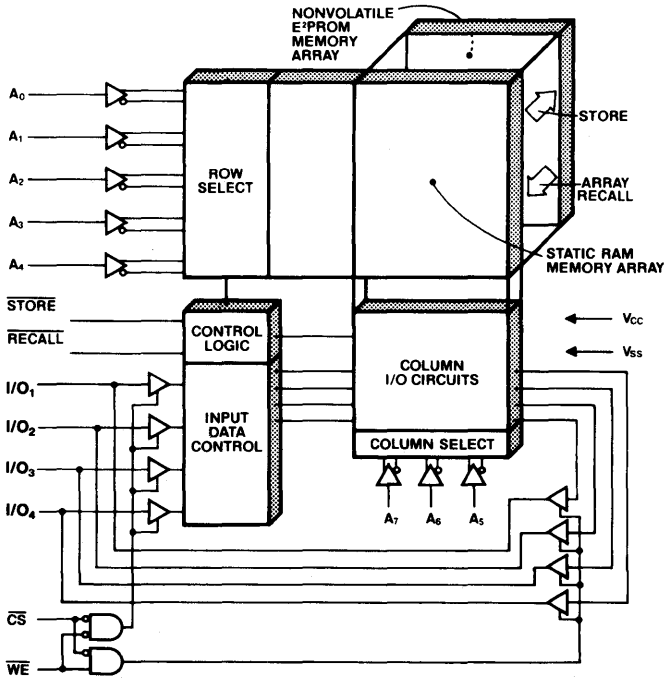


Figure 2: Functional diagram of X2212 memory.

9

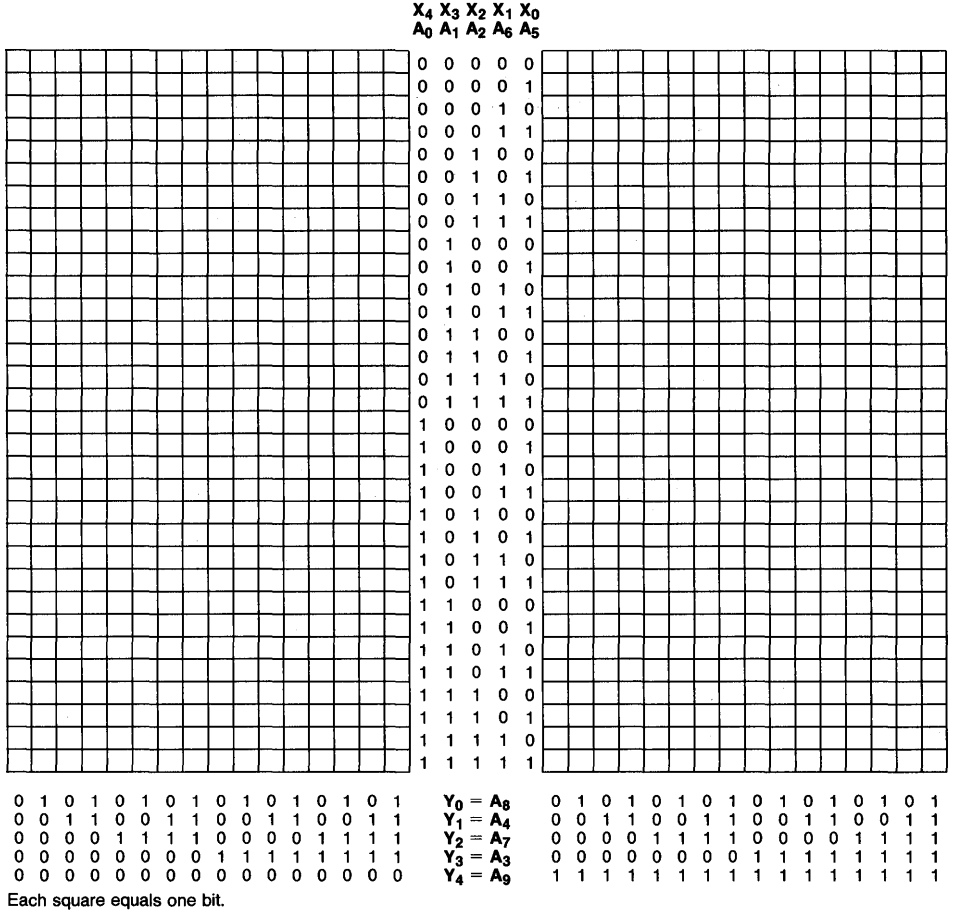


Figure 3: X2201A physical address map.

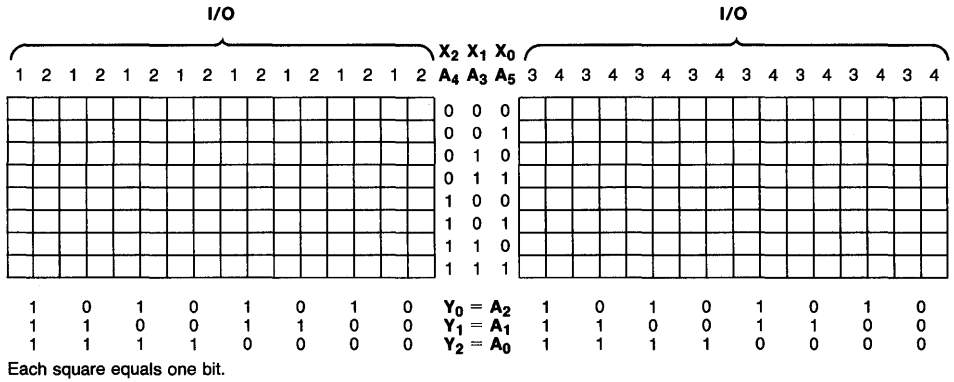


Figure 4: X2210 physical address map.

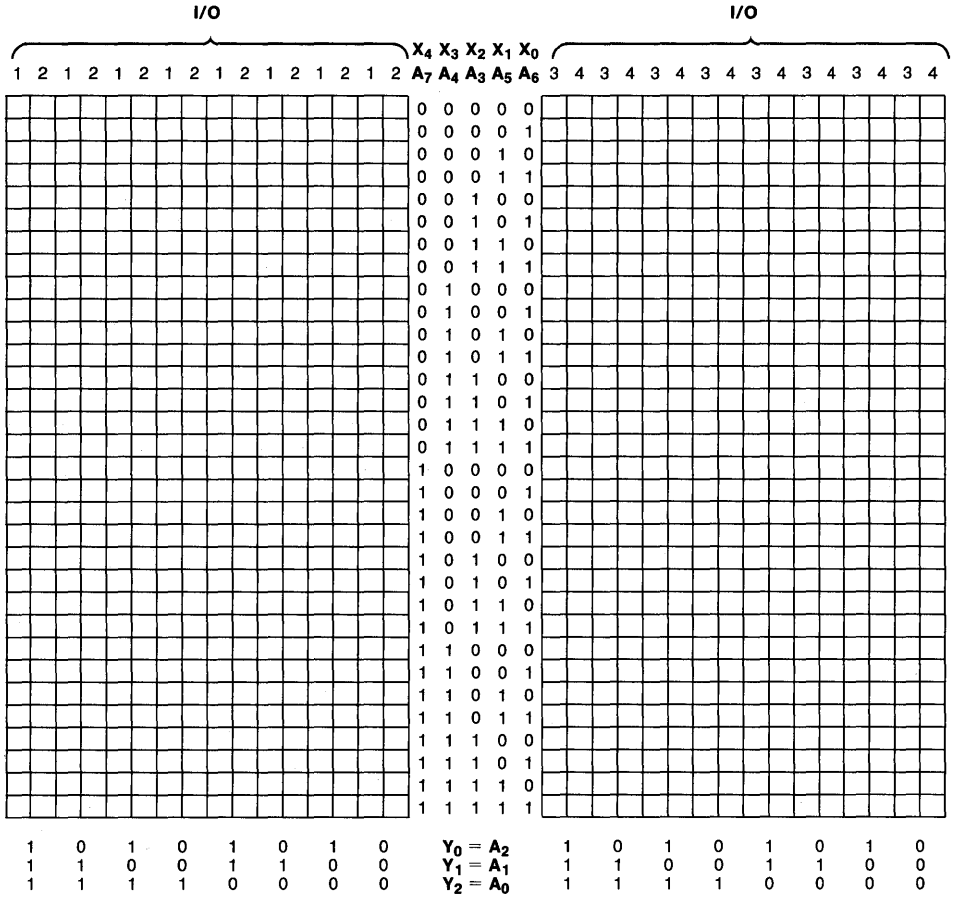


Figure 5: X2212 physical address map.

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TECHNOLOGY

Xicor NOVRAM memories store their nonvolatile data on electrically isolated polysilicon gates. These gates are islands of polysilicon surrounded by about 800Å of SiO_2, one of the best insulators known. This is similar to the structure used in UV light erasable PROMs (UVEPROMs).

Electrons once trapped on the floating (isolated) gates will remain there unless they receive a large energy input from an outside source (e.g., an ultraviolet photon in the case of UVEPROMs), or until a sufficiently high electric field is applied to distort the energy bands sufficiently to allow Fowler-Nordheim tunneling to occur.[1]

Fowler-Nordheim tunneling, which will be discussed in more detail later in this report, is the mechanism employed to charge and discharge the floating storage gate of Xicor's NOVRAM memories. The storage gate is formed in the second of three layers of polysilicon as illustrated in Figure 6. Electrons move to the floating gate by tunneling from POLY 1 to POLY 2. When the high fields which are used to cause the desired tunneling are not present, the electrons remain trapped on POLY 2.

As Figure 6 illustrates, the NOVRAM memory cell is a conventional six transistor static RAM cell to which a floating gate E^2PROM cell containing two transistors has been added. During the normal READ/WRITE operations, memory array power supply (V_{CCA}) is fixed at the positive supply level (nominally 5V) and the Internal Store Voltage is fixed at ground. Only the six transistors of the static RAM cell are effective and the operation is exactly that of a conventional six transistor static RAM.

The RECALL operation depends on capacitance ratios. The value of C_2 in Figure 6 is larger than that of C_1. When the external RECALL command is received, the memory array power supply (V_{CCA}) is initially pulled low to equalize the voltages on nodes N_1 and N_2. These nodes equalize quickly to V_{CCA} through the depletion transistors Q_1 and Q_2. When V_{CCA} is then allowed to rise, the node with the lighter capacitive loading will rise more quickly and turn on the pull down transistor on the opposing side, which will keep the more slowly rising node clamped low. If the floating gate is charged positively, Q_8 is turned on, which connects C_2 to N_2. Thus N_1, which is loaded by the smaller capacitor C_1, rises more rapidly, causing the latch to set with N_1 high and N_2 low. If the floating gate is charged negatively, Q_8 is turned off, which isolates C_2 from N_2 and allows N_2 to rise more rapidly than N_1. Thus the latch is set with N_2 high and N_1 low. During the RECALL operation the Internal Store Voltage remains at ground.

The STORE operation also utilizes capacitance differences to transfer data from RAM to E^2PROM. When node N_1 is low, transistor Q_7 is turned off. This allows the junction between capacitors CC_2 and CC_3 to float. Since the combined capacitance of CC_2 and CC_3 is larger than that of C_p, the capacitor between POLY 1 and POLY 2, the floating gate follows the potential of the Internal Store Voltage. Thus when the Internal Store Voltage becomes high (several times V_{CC}), a sufficient field exists between POLY 1 and POLY 2 to cause electron tunneling and the floating gate is charged negatively.

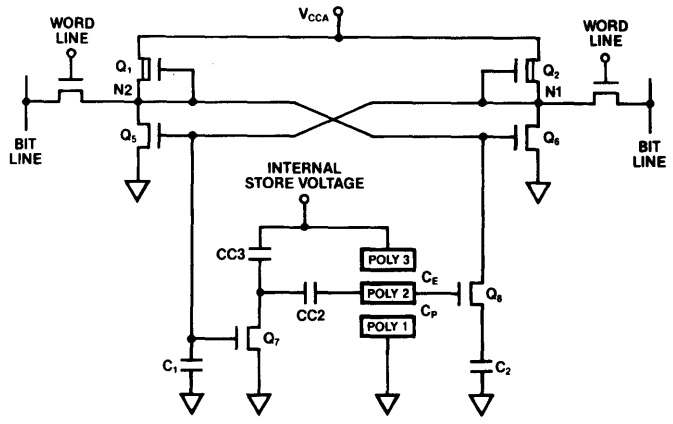


Figure 6: Schematic diagram of an NOVRAM memory cell showing how a standard six-transistor static RAM cell is merged with a floating gate E^2PROM cell.

When node N_1 is high, transistor Q_7 is turned on which grounds the junction between CC_2 and CC_3. Since the capacitance of CC_2 is larger than that of C_E, the capacitor formed between POLY 2 and POLY 3, CC_2 holds the floating gate near ground when the Internal Store Voltage goes high. In this case the high field exists between POLY 2 and POLY 3 and electrons tunnel from POLY 2 to POLY 3, which discharges the floating gate.

The Internal Store Voltage is at ground except during the STORE operation. Moreover, during the STORE operation all bits are stored simultaneously, which is possible because the RAM bit associated with each E²PROM bit acts as a data latch.

TUNNELING PHYSICS

Because the innovative aspects of NOVRAM and E²PROM memories revolve around the nonvolatile storage procedure, it seems appropriate to discuss the storage phenomenon in more detail. As mentioned previously, the storage occurs via a tunneling mechanism first described by Fowler and Nordheim in 1928 and subsequently named after them.[1] The basic idea is illustrated in Figure 7. The energy difference between the conduction and valence bands in Si is about 1.1eV; the energy difference between those bands in SiO_2, is approximately 9eV. When the two materials are joined, the conduction band in SiO_2 is 3.25eV above that in Si. The differences in valence band energies is even larger (approximately 4eV). Since the thermal energy of an electron averages only 0.025eV at room temperature, the chances of an electron in silicon gaining enough thermal energy to surmount the barrier and enter the conduction band in SiO_2 is exceedingly small. This case is illustrated in Figure 7.

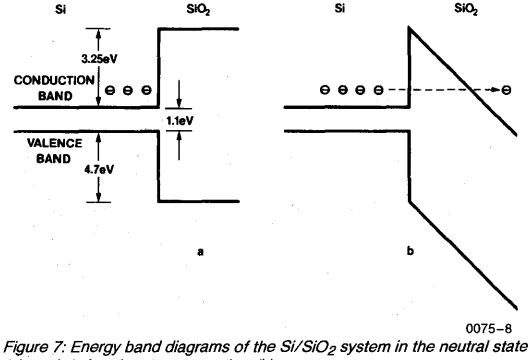


Figure 7: Energy band diagrams of the Si/SiO_2 system in the neutral state (a), and during the store operation (b).

Fowler and Nordheim pointed out that in the presence of a high electric field, the energy bands will be distorted as illustrated in Figure 7b. Under these conditions there is a small but finite probability that an electron in the conduction band in the silicon will tunnel through the energy barrier and emerge in the conduction band of the SiO_2, as illustrated in Figure 7a.

Fowler-Nordheim emission was observed early in this century for the case of electrons being emitted from metals into vacuum, and in 1969 Lenzlinger and Snow observed this phenomenon for the Si–SiO_2 system.[2] The Fowler-Nordheim current increases exponentially with applied field and becomes readily observable (i.e., $J \sim 10^{-6}$ A/cm²) for the Si–SiO_2 system in which the Si surface is smooth for fields on the order of 10 MV/cm.

It has been known for some time that "enhanced" electron emission currents could be observed for Si–SiO_2 systems for which the Si surface has a texture. (Texture in this context means that the Si surface has features on the order of a few hundred angstroms.)[3–5] These enhanced currents occur at applied fields with values smaller than one quarter of those necessary for the same current from a smooth surface. It has been thought that the enhanced emission occurs because of locally enhanced fields near the top regions of the features on the surface.

Lewis attempted to model Fowler-Nordheim tunneling from a textured surface by calculating current from a number of hemispheres set in a plane.[6] Attempts to quantitatively fit experimentally observed currents with this model have not been very successful. Hu, et al, for example, found that to fit their data to existing theory it was necessary to assume an energy barrier of approximately 1eV between conduction bands in Si and SiO_2.[7] Even with this assumption, the fit was poor because the measured current increased more rapidly than the calculated values, as is illustrated in Figure 8.

Because of the importance of tunneling to the operation of its products, Xicor decided to adequately characterize and model tunnel emission from textured polycrystalline silicon (poly) surfaces. One avenue of exploration was to characterize the physical topology of the tunneling structure. Figure 9 is a scanning electron micrograph (SEM) of the emitting (top) surface of a layer of polysilicon from which the oxide has been removed for clarity. As shown in the micrograph, this surface is composed of a densely packed array of features reminiscent of a cobblestone street. A count of these features on SEM photos of material from several lots determined that

there is an average of about 50 features per square micron. A transmission electron microscope (TEM) cross-section of a tunneling structure is shown in Figure 10. This photo demonstrates the conformal nature of the structure. The top surface of the prior deposition of polysilicon is formed into a series of "hillocks" 200–300Å high and 1000–1500Å across the base. The free surface of the oxide grown on this silicon replicates the silicon surface. Thus, polysilicon deposited atop the prior polysilicon layer subsequent to oxidation has dimples on its undersurface occurring over the already existing "hillocks".

The topology of the polysilicon surfaces causes the electric field lines to no longer be parallel as in the case of parallel emitting and collecting surfaces, but rather to diverge and converge in response to the local topology as is illustrated in Figure 11. As shown, the field lines converge near surfaces of positive curvature (i.e., bumps) and diverge near surfaces of negative curvature (i.e., dimples). Since Fowler-Nordheim tunneling depends exponentially on the electric field at the surface of the polysilicon, a good model of the electron emission requires an accurate knowledge of the field over the complete surface.

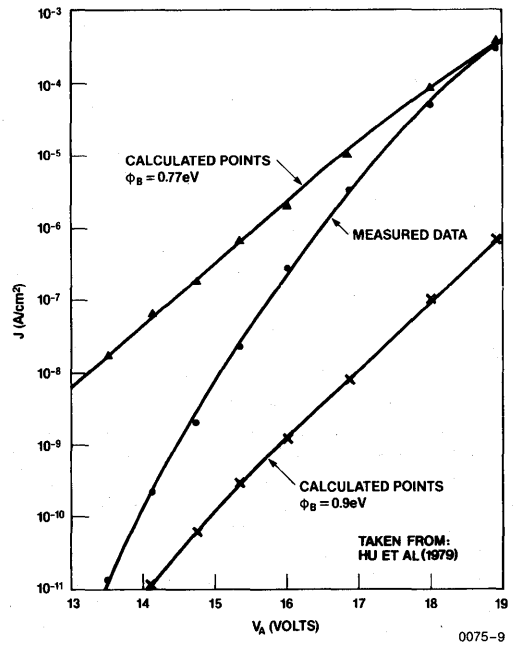


Figure 8: Current vs. applied voltage for current from textured poly surface emitted through 1760Å of thermal SiO_2 compared with calculations based on previously available theory.

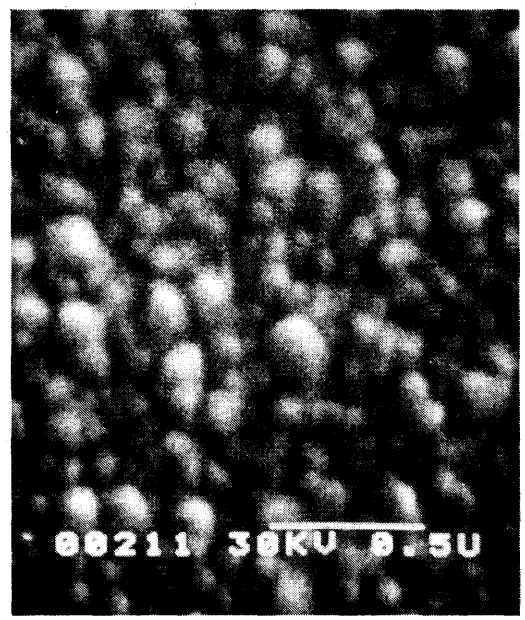


Figure 9: Scanning electron microscope (SEM) photograph of top emitting textured poly surface with oxide removed. The 0.5 μ-long bar gives the scale.

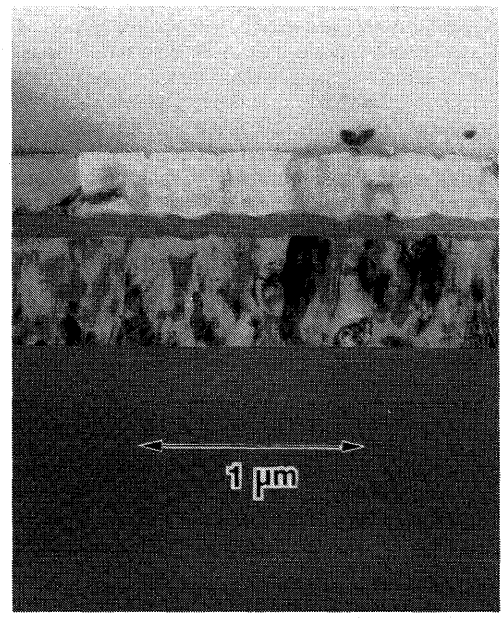


Figure 10: Transmission electron microscope (TEM) photograph of a cross-section through a textured tunneling structure. The one micron-long arrow shows the scale.

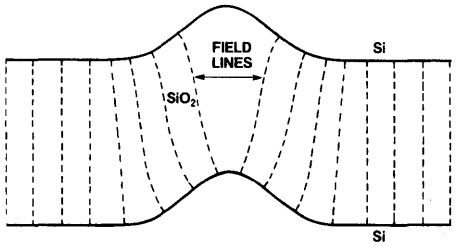


Figure 11: Sketch illustrating the manner in which field lines converge near convex feature and diverge near concave feature.

Until recently, this field problem was one of the unsolved problems of mathematical physics. (It is classically known as the "lightning rod problem".) Roger Ellis, a member of the Xicor staff, has solved this problem.[8] The technique used differential geometry to transform Euclidean space into a space in which the field lines were parallel. The electrostatics problem was solved in this space and the solution transformed back into the original space. The tunnel current was found to be described in a spherical coordinate system by the equation:

$$J_{collecting} = \frac{\left[\int_s \frac{q^3 E^2}{8\pi h \phi_B} \exp\left\{\frac{-4(2m)^{1/2}\phi_B^{3/2}}{3hqE}\right\} ds\right]_{emitting}}{\left[\int s\, ds\right]_{collecting}} \quad (1)$$

where the electric field, E, is given by

$$E = \frac{V_A}{\xi(S_2) - \xi(S_1)} \left[\left(\frac{d\Theta^2}{dr}\right) + \frac{1}{r^2}\right]^{1/2} \frac{d\xi}{d\Theta} \quad (2)$$

and

$$\xi = \frac{1}{\left|\frac{d\vec{r}}{d\Theta}\right|} \frac{de_t}{d\Theta}(\vec{e}_t)$$

is the curvature of the surface at which the field is evaluated.[9]

This expression has several interesting properties. One is that the field depends on the difference of the curvatures of the emitting and collecting surfaces. Another is that the electric field also depends on the derivative of the curvature of the emitting surface.

To verify the accuracy of this expression, the current-voltage (J-V) characteristics of a textured polysilicon tunnel structure were experimentally determined and compared with those predicted by equation (1). Because of the field enhancement on the bumps, a higher current is expected at a given applied voltage polarity which causes electron emission from the bumps than for that polarity which causes emission from the dimples. Thus, by analogy with a diode, the polarity with the bumps negative (higher current emitted) is called the forward bias direction and the other polarity is called the reverse bias direction.

Figure 12 shows the results of comparing experimental and calculated values for the forward bias condition. As can be seen, theory and experiment agree within about 20% over seven orders of magnitude in current. The parameters used in calculating the predicted currents were not arbitrarily chosen. The value of the oxide/silicon conduction band barrier, ϕ_B, was taken to be 3.15eV as measured by Weinberg.[10] The feature density $(50\mu)^2$ and the bump base and height are typical of those seen on SEMs and TEMs such as Figures 9 and 10, respectively. The dashed line in Figure 12 is the current which would be predicted if the top (i.e., collecting) electrode were flat rather than dimpled. This illustrates the effect of the collecting surface curvature on the field at the emitting surface.

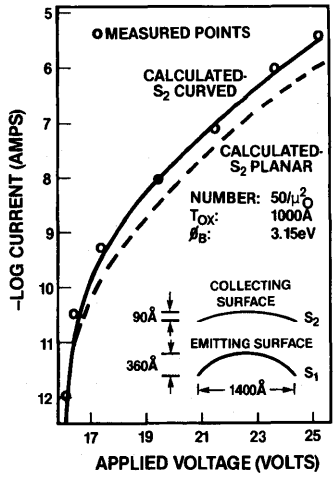


Figure 12: Forward tunneling characteristic comparing the measured data with curves calculated for a concave and a planar collecting surface.

To further verify equation (1), the reverse bias current was measured on the same device used for the forward bias case. The results are compared with the predicted current in Figure 13. This shows about 20% agreement over eight orders of magnitude in current with the same parameters used as in calculating the forward bias case. Clearly, the model does an excellent job of predicting the measured current.

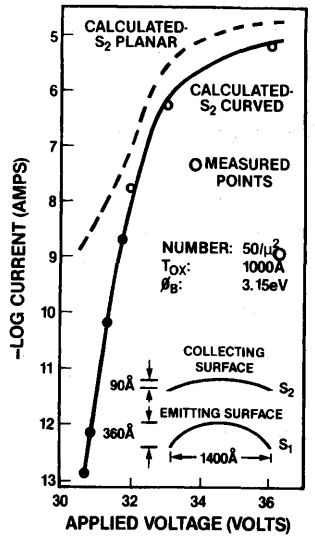


Figure 13: Reverse tunneling characteristic comparing the measured data with curves calculated for a concave and planar emitting surface.

Several points of interest can be observed in Figure 13. One point is that at a voltage at which the forward current is saturating (25V), the reverse current is unobservable (extrapolation of the measured current predicts $\sim 10^{-27}$A). Another point is that the current emission predicted from a flat top surface is greater than that predicted from a dimpled top surface. Moreover, the current emitted from a flat top surface decreases more slowly with decreasing voltage than that from a dimpled flat surface. This latter fact is important for data retention as will be discussed in the next section.

In summary, Xicor is able to accurately model the tunnel current emitted from textured poly surfaces through SiO_2 layers. The magnitude of the tunnel current as well as its voltage dependence are dependent upon the surface topology. Thus, we have the means to optimize the emission characteristics. Lastly, the asymmetric nature of the tunnel emission makes possible cell designs which are better adapted to particular requirements than is possible with symmetric tunnel characteristics—just as a diode offers more design possibilities than does a resistor.

DATA RETENTION

As was suggested in the previous section, textured poly tunneling structures have a significant advantage in data retention, in comparison with those employing flat surfaces and thin oxides. One basis for this advantage is illustrated in Figure 14, in which the current-voltage (J-V) characteristics of a tunneling device which employs a thin oxide between planar surfaces is compared with a tunneling device which employs a thick oxide between textured silicon surfaces. For this comparison we match the currents in the high current region since most memories are designed to program in about the same time period ($\sim$ 10 ms). As can be seen, the same current can be obtained from a smooth surface with 125Å thick tunnel oxide or from a textured surface with an 825Å thick tunnel oxide. Note however, that at lower values of applied voltage typical of read and storage conditions, the current emitted from a textured surface is approximately four orders of magnitude lower than that from a smooth surface.

These differences may become even more significant as devices are scaled. It is clear that, in order to scale the memory properly, lower programming voltages are needed so that the isolation widths and device channel lengths can be reduced both in the memory array and in the peripheral circuitry. However, for a typical part which stores data in 3 ms and must retain it for 10 years, the tunneling current under storage and reading conditions must be at least 10^{11} times smaller than under programming conditions because the retention time is 10^{11} times

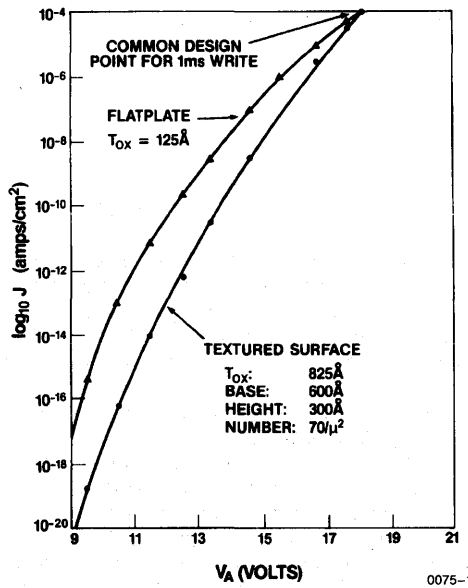


Figure 14: Comparison of calculated tunneling J-V curves for emission from a planar and a textured structure. The devices were designed to have the same emission in the high current regime where programming takes place.

longer than the storage time. Actually, for a margin, one would design for a difference in currents of 10^{13} to 10^{14}. For planar surface tunneling structures, this may be a difficult design constraint because the slope of the J-V curve is fixed, which means that the maximum allowed read voltage drops with the programming voltage on a volt-for-volt basis, not proportionately. On the other hand, textured surface tunneling structures, in their current manifestation, have a steeper J-V characteristic than planar ones and the J-V characteristic of a textured structure can be tailored to yield a steeper curve if desired. This means that for a given maximum read voltage, a textured structure requires a lower programming voltage which leads to better scaling.

To verify the excellent data retention expected of Xicor NOVRAMs, a study was carried out to measure data loss as a function of temperature. Figure 15 shows log cumulative data loss vs. log time for 100 samples of X2210's at each of three temperatures. Data loss is defined as occurring when the first bit in the array loses data. As shown in Figure 15, high temperatures were required to obtain appreciable data loss in experimentally useful times. Note that even at 300°C, 2000 hours (~ 3 months) are required to begin to see data loss. Figure 16 shows the result of calculating failure rates based on these results and plotting vs. inverse temperature. Since the rates fall in a straight line, we can extract an activation energy and extrapolate to lower temperatures (see the next section for a discussion of activation energies). The result is that the experimental value of the activation energy is 1.7eV and the mean time for data loss for this mechanism (which we believe to be the fundamental loss mechanism for this technology) is 3 million years for data retention at 125°C.

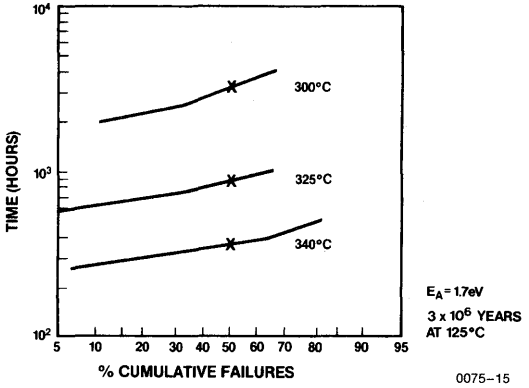


Figure 15: Log cumulative data loss vs. log time for three storage temperatures on samples of 100 X2210's. Data loss is defined to occur when the first bit in an array loses data.

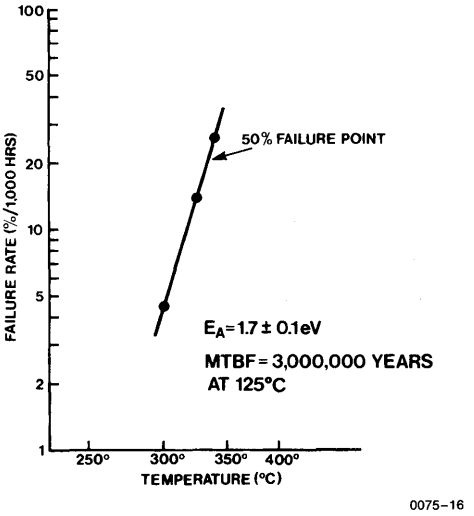


Figure 16: Log data loss rate vs. inverse temperature for X2210's.

ENDURANCE

The endurance of Xicor NOVRAMs is monitored on a regular basis. Figure 17 shows typical endurance data on 100 units of X2212 from five endurance monitor lots plotted on an extreme value distribution. All of the units tested exceeded the 1,000 data changes/bit limit specified for this device.

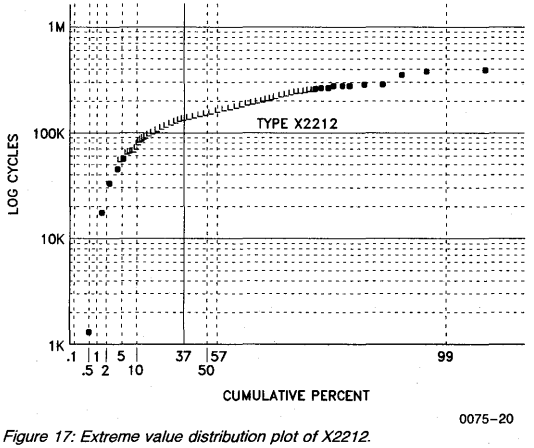
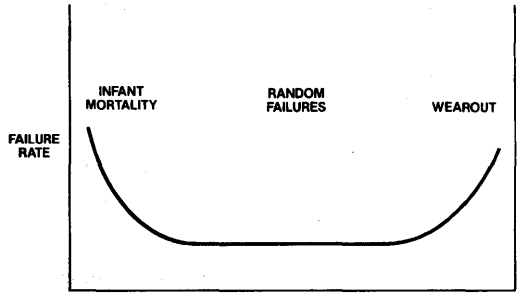


Figure 17: Extreme value distribution plot of X2212.

BASIC RELIABILITY CONCEPTS

There are several concepts basic to most reliability work. One is the long established observation that failure rates follow the bathtub-shaped curve illustrated in Figure 18. There is an infant mortality region characterized by a rapidly declining failure rate as the "weak" parts are eliminated from the population, a random failure characterized by an invariant or slowly declining failure rate, and a wearout region characterized by an increasing failure rate as the units reach the end of life.

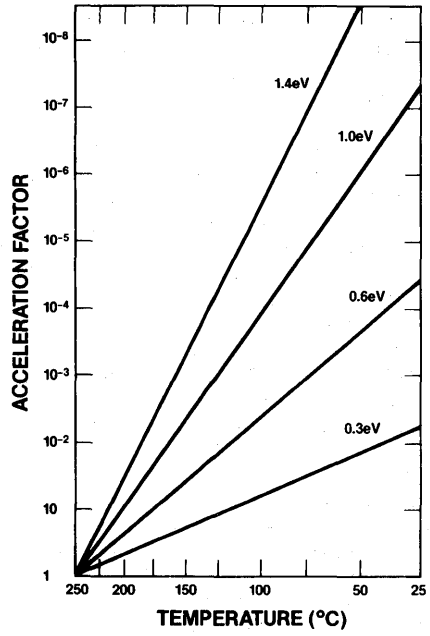


0075-17

Figure 18: Illustration of bathtub curve of failure rates showing regions in which infant mortality, random failures, and wearout mechanisms dominate the failure rate.

Each region of the failure rate curve has specific failure modes which predominate. For example, the infant mortality region is dominated by failures which arise from manufacturing defects. Table I gives a summary of common failure mechanisms and stresses which may be used to accelerate the failure rates of the various mechanisms which have been culled from the literature.[11-14]

The classic parameter used to accelerate failure rates is temperature. It is known that a very broad class of failure mechanisms have a temperature dependence proportional to exp $(-E_a/kT)$ where E_a is called the activation energy, k is Boltzmann's constant, and T is the absolute temperature. This is true because a number of basic physical phenomena such as diffusion rates and chemical reaction rates have this dependence. The significance of this is that if the activation energy is known for the failure mechanisms in question, then the failure rates arising from these mechanisms can be measured at elevated temperature where they are high enough to be conveniently measured and extrapolated back to lower operating temperatures where the failure rates may be so low as to require an inconveniently large number of device hours to measure. The relationship which allows one to translate failure rates from one temperature to another is known as the Arrhenius relation. Figure 19 illustrates this relation for a number of common values of activation energy.



0075-18

Figure 19: Acceleration factor vs. temperature calculated for various activation energies from Arrhenius relation.

RELIABILITY TESTING

Five types of tests were conducted to establish the reliability of the devices:

1) High temperature dynamic lifetest.
2) Data retention bake.
3) High temperature reverse bias.
4) Lifetest monitor.
5) Environmental.

These tests are discussed after Table I.

Failure Mechanism	Type	Activation Energy	Detection Method
Ionic Contamination	Infant/ Random/ Wearout	1.0eV	High Temp. Bias
Surface Charge	Wearout	0.5–1.0eV	High Temp. Bias
Polarization	Wearout	1.0eV	High Temp. Bias
Electro-migration	Wearout	1.0eV	High Temp. Operating Life
Microcracks	Random	—	Temperature Cycling
Oxide Rupture	Infant/ Random	0.3eV	High Temp. Operating Life
Silicon Defects	Infant/ Random	0.3eV	High Temp. Bias
Oxide Defect Leakage	Infant/ Random	0.6eV	High Temp. Operating Life
Electron Trapping In Oxide	Wearout	—	Low Temp., High Voltage Operating Life

Table I: MOS failure mechanisms.

High Temperature Dynamic Lifetest

This is the usual data from which failure rate predictions are made. For this to be a valid predictor of failure rate, the parts must function as they would in normal operation. Thus, overly elevated temperatures at which the unit does not function internally are to be avoided since this may lead to overly optimistic predictions.

Xicor gathers this data at 125°C ambient which is within the known operating range of the units under test. The stimulus pattern consists of recalling a known pattern, writing an all one's pattern over the recalled pattern bit by bit, reading the all one's pattern, writing its complement, reading the complement and then beginning over again.

The units in lifetest are tested at 168, 500, 1000, and 2000 hours to verify that they are still within specification. The first step of the readout tests is to recall the information stored in the nonvolatile section of memory to verify that the previously stored pattern is still retained. If so, the memory is completely exercised over voltage including verification of the STORE function. Finally, the predetermined pattern is restored to memory for the next lifetest period.

Data Retention Bake

This test is sometimes referred to as a storage bake. The term "data retention bake" better describes the principal function it serves in the case of electrically programmable nonvolatile memories which is to measure how fast charge leaks away from the floating gate.

In this test, a pattern which represents all floating gates charged positive is stored and the devices are baked at 250°C for the cerdip (ceramic dual-in-line) package and 150°C for plastic (dual-in-line) package with no bias applied. At intervals the memory is removed from bake, and the nonvolatile data recalled and checked for accuracy. The data is not restored at readouts in order to ascertain the worst case retention. Since Xicor warrants cycling endurance of various values, this test was performed on parts specified for 1000 cycle endurance which had performed 1000 complete data alterations, as well as on parts which had not received this treatment.

HTRB

HTRB stands for High Temperature Reverse Bias, a term which originated with bipolar circuits, in which case the test reverse biased the junctions of all of the input stages. For MOS circuits, a better term would be high temperature static bias. In this stress, which Xicor carries out at 150°C, V_{SS} is grounded and a static positive voltage is applied to all of the inputs and outputs, as well as to V_{CC}. This has the effect of applying a static bias equal to the power supply across the gate oxides of the circuit transistors. This stress is intended to expose failures which might occur as a result of drift of mobile ionic contaminants or latent defects in the gate oxides.

It is known that many defects are accelerated by voltage as well as temperature. For example, it has been shown by Crook that the failure rate of oxide defects increases 10^7 times per MV/cm increase in the electric field.[15] For this reason, HTRB stresses were conducted with both 5.5V and 7.5V bias applied to the units under test.

Lifetest Monitor

In order to assure a continuous supply of the highest quality and reliability possible to our customers, a weekly lifetest monitor is maintained.

This monitor is used at Xicor for two purposes. First, it is used to monitor the infant mortality rate which is an indicator of manufacturing defects. If an unusually high failure rate were to be observed, a corrective action could be taken before defective units are shipped to customers. Secondly, a long term failure rate is also monitored. This establishes a way to ensure that long term reliability is maintained.

Each week approximately 250 units of X2212 devices are placed in a dynamic lifetest at 125°C for 168 hours. Also, monitor units of the first week of each period remain in dynamic lifetest for up to 1000 hours.

Package Environmental Tests

MIL-M-35810 and MIL-STD-883, Method 5005, Group C and D have been the guide for environmental testing for the cerdip package. Table II lists the tests, the test conditions and test results. All lots passed the 883 qualification criteria.

Because of the nature of the plastic package, additional tests were done. These tests are 85°C/85% RH (both biased and unbiased) lifetest, temp cycling (200 cycles) and saturated storage test at 2 ATM (autoclave).

RESULTS

Tables IIIA and IIIB exhibit the results of dynamic lifetest of X2210 and X2212 in cerdip package and plastic package, respectively. Table IIIA shows zero failure result in 6×10^5 device hours on 1700 units of X2210 and X2212. Table IIIB shows two failure results in 1.7×10^6 device hours on 5055 units of X2210 and X2212. The causes of the failures were also listed in Table IIIB. In addition, Table IIIB includes lifetest monitor data since plastic units are used.

Tables IVA and IVB show the results of 150°C static lifetest at 5.5V for cerdip and plastic. No failures were detected on both package types, out of 121 units for cerdip and 245 units for plastic.

Tables VA and VB show the results of 150°C static lifetest at 7.5V applied bias. Increasing V_{CC} from 5.5V to 7.5V increases the field across the gate oxide from 6.875×10^5 V/cm to 9.375×10^5 V/cm. According to Crook this increase in field should accelerate the failure rate by about 56 times. In cerdip, one failure was observed at the 48 hour readout. For oxide breakdown, out of 250 units tested in plastic, no failures were seen.

Test	MIL-STD-883 Test Method	Conditions	LTPD	Accept #	Results
Temp. Cycling	1005	Test Condition C (10 cycle, −65°C to +125°C)	15	0/15	0/175
Constant Acceleration	2001	Test Condition E (30,000g, Y1 axis only)			0/175
Seal	1014	Test Condition B			0/175
—Fine		(5×10^{-8} cc/min)			
—Gross		Test Condition C			0/175
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15	0/15	0/213
Seal	1014				
—Fine		Test Condition B			0/213
—Gross		Test Condition C			1/213
Thermal Shock	1011	Test Condition B (15 cycles, −55°C to +125°C)	15	0/15	0/203
Temp. Cycling	1010	Test Condition C (100 cycles)			0/203
Moisture Resistance	1004				0/203
Seal	1014				
—Fine		Test Condition B			0/203
—Gross		Test Condition C			0/203
Internal Water Vapor Content	1018	5,000 ppm max. water content at 100°C	—	0/3 or 1/5	0/6
Mechanical Shock	2002	Test Condition B (1500g peak, 3 axis)	15	0/15	0/192
Vibration Variable Frequency	2007	Test Condition A (20g peak, 3 axis)			0/192
Constant Acceleration	2001	Test Condition E			0/192
Seal	1014				
—Fine		Test Condition B			0/192
—Gross		Test Condition C			0/192
Salt Atmosphere	1009	Test Condition A	15	0/15	0/144
Seal	1014				
—Fine		Test Condition B			0/144
—Gross		Test Condition C			0/144
Adhesion of Lead Finish	2025		15	0/15 (# of leads from 3 devices)	0/18
Lid Torque	2024		—	0/5	0/15

Table II: Environmental test for 18-lead cerdip package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	403	0	383	0	99	0	97	1.3×10^5
2 (2212)	0	350	0	324	0	99	0	98	1.2×10^5
3 (2212)	0	338	0	334	0	99	0	98	1.2×10^5
4 (2210)	0	294	0	284	0	99	0	97	1.2×10^5
5 (2210)	0	315	0	312	0	99	0	98	1.2×10^5
Totals	0	1700	0	1637	0	495	0	488	6.0×10^5

Table IIIA: Stress dynamic lifetest at 125°C—cerdip package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	575	0	573	0	99	0	97	0	97	2.5×10^5
2 (2212)	2[a]	570	0	565	0	99	0	98	0	98	2.5×10^5
3 (2212)	0	577	0	577	0	99	0	96	0	96	2.5×10^5
4 (2210)	0	573	0	570	0	99	0	99	0	98	2.5×10^5
5 (2212)	0	570	0	570	0	99	0	99	0	98	2.5×10^5
6 (Monit.)	0	2190	0	2183	0	297	0	297	—	—	5.1×10^5
Totals	2	5055	0	5038	0	792	0	786	0	487	1.7×10^6

[a] = one x-decoder failure due to blown oxide 0.3eV
one word line failure due to blown oxide 0.3eV

Table IIIB: Stress dynamic lifetest at 125°C—plastic package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	25	0	23	0	23	0	23	0	23	44896
2 (2212)	0	25	0	25	0	25	0	25	0	25	48800
3 (2212)	0	25	0	23	0	23	0	23	0	23	44896
4 (2210)	0	25	0	25	0	25	0	25	0	25	48800
5 (2210)	0	25	0	25	0	25	0	25	0	25	48800
Totals	0	125	0	121	0	121	0	121	0	121	2.4×10^5

Table IVA: Stress 5.5V HTRB at 150°C—cerdip package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	50	0	49	0	49	0	49	46648
2 (2212)	0	50	0	50	0	50	0	49	47100
3 (2212)	0	50	0	50	0	50	0	50	47600
4 (2210)	0	50	0	50	0	50	0	50	47600
5 (2212)	0	50	0	49	0	47	0	47	44984
Totals	0	250	0	248	0	246	0	245	2.3×10^5

Table IVB: Stress 5.5V HTRB at 150°C—plastic package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	25	0	25	0	25	0	25	23800
2 (2212)	1[a]	25	0	24	0	24	0	24	22848
3 (2212)	0	25	0	25	0	25	0	25	23800
4 (2210)	0	25	0	25	0	25	0	25	23800
5 (2210)	0	25	0	25	0	25	0	25	23800
Totals	1	125	0	124	0	124	0	124	1.2×10^5

[a] = Blown oxide 0.3eV

Table VA: Stress 7.5V HTRB at 150°C—plastic package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	50	0	48	0	48	0	48	45696
2 (2212)	0	50	0	50	0	50	0	48	46600
3 (2212)	0	50	0	50	0	50	0	50	47600
4 (2210)	0	50	0	50	0	50	0	50	47600
5 (2212)	0	50	0	48	0	48	0	48	45696
Totals	0	250	0	246	0	246	0	244	2.3×10^5

Table VB: Stress 7.5V HTRB at 150°C—plastic package.

Tables VIA, VIB, VIIA and VIIB show the results of 250°C and 150°C retention bake for cerdip and plastic, respectively. Retention bake was done both before and after 1000 data change cycles on units that are rated for 1000 data change cycles. At 150°C no failures were detected before nor after 1000 data changes on a total of 125 units for 1000 hours. At 250°C, the data on uncycled devices shows 3 units failed from 250 units for 2000 hours. The data on cycled devices shows 4 units failed from 125 units for 2000 hours. These results do not have statistically significant difference in overall failure rate. Close examination shows a tendency for the cycled failures to be more scattered, while uncycled failures are more concentrated at 1000 and 2000 hour readouts. This kind of data should not be surprising, as an oxide defect, which had been accelerated by the high electric field, became manifest during store operation. The retention failure rate for 1000 hours at 250°C is at the range of 1% to 2%, which is about half of that previously reported for EPROMs.[16] Retention data reported for other E^2PROM technologies would indicate that the present NOVRAM retention results are greatly superior.[17]

Tables VIII and IX represent 85/85 lifetest with and without voltage bias, respectively. As indicated by the data, no failures were observed in both the 5.5V biased and the unbiased groups for a total of 5×10^5 device hours.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	50	0	50	0	50	0	49	0	48	95100
2 (2212)	0	50	0	50	0	50	0	50	1	47	94600
3 (2212)	0	50	0	50	0	50	1	50	1	48	95600
4 (2210)	0	50	0	50	0	50	0	50	0	50	97600
5 (2210)	0	50	0	50	0	50	0	49	0	49	96100
Totals	0	250	0	250	0	250	1	248	2	242	4.8×10^5

Table VIA: Stress bake at 250°C—cerdip package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	25	0	25	0	25	0	25	23800
2 (2212)	0	25	0	25	0	25	0	25	23800
3 (2212)	0	25	0	25	0	25	0	25	23800
4 (2210)	0	25	0	25	0	25	0	25	23800
5 (2212)	0	25	0	25	0	25	0	25	23800
Totals	0	125	0	125	0	125	0	125	1.2×10^5

Table VIB: Stress retention bake at 150°C—plastic package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	25	0	25	1	24	0	23	1	23	45468
2 (2212)	0	25	0	25	0	25	0	25	0	25	48800
3 (2212)	1	25	0	24	0	24	1	24	0	23	45848
4 (2210)	0	25	0	25	0	25	0	25	0	25	48800
5 (2210)	0	25	0	25	0	25	0	25	0	25	48800
Totals	1	125	0	124	1	123	1	122	1	121	2.4×10^5

Table VIIA: 250°C Retention bake—cycled cerdip unit.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	25	0	25	0	25	0	25	23800
2 (2212)	0	25	0	25	0	25	0	25	23800
3 (2212)	0	25	0	25	0	25	0	25	23800
4 (2210)	0	25	0	25	0	25	0	25	23800
5 (2212)	0	25	0	25	0	25	0	25	23800
Totals	0	125	0	125	0	125	0	125	1.2×10^5

Table VIIB: 150°C Retention bake—cycled plastic unit.

Lot #	500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	
1 (2212)	0	50	0	50	41600
2 (2212)	0	50	0	50	41600
3 (2212)	0	50	0	50	41600
4 (2210)	0	50	0	50	41600
5 (2212)	0	50	0	50	41600
Totals	0	250	0	250	2.1×10^5

Table VIII: Biased 85/85—plastic units with V_{CC} = 5V.

Lot #	500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	
1 (2212)	0	50	0	50	41600
2 (2212)	0	50	0	50	41600
3 (2212)	0	50	0	50	41600
4 (2210)	0	50	0	50	41600
5 (2212)	0	50	0	50	41600
Totals	0	250	0	250	2.1×10^5

Table IX: Biased 85/85—plastic units with V_{CC} = 0V.

Lot #	200 Cycles	
	# Fail	# In
1 (2212)	0	50
2 (2212)	0	50
3 (2212)	0	50
4 (2212)	0	50
5 (2210)	0	50
Totals	0	250

Table X: Temperature cycles (method 1010)—plastic package.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 (2212)	0	25	0	25	0	25	0	25	23800
2 (2212)	0	25	0	25	0	25	0	25	23800
3 (2212)	0	25	0	25	0	25	0	25	23800
4 (2210)	0	25	0	25	0	25	0	25	23800
5 (2212)	0	25	0	25	0	25	0	25	23800
Totals	0	125	0	125	0	125	0	125	1.2×10^5

Table XI: Dynamic lifetest at 10°C—plastic packaged units.

Figure 20 shows a bar graph of the autoclave results for plastic package. Cumulative failures steadily increased for the first 400 hours with sharp increase at approximately 500 hours. Figure 20 shows the 500 hour mark for the plastic package in the 24% range. The discrepancy between autoclave and 85°C/85% RH lifetest results can be explained by the two causes of failure. During the saturated storage (autoclave), failure rate is dependent on the galvanically induced ionic currents flowing in a layer of water on the surface of the die. This layer of water is accumulated after plastic has debonded from the die which causes corrosion to concentrate on the bonding pad. The 85°C/85% RH lifetest produced more widespread corrosion due to phosphorous in the passivations, and debonding is not a prerequisite for this type of failure.[21, 22] Since corrosion on the bonding pad is only one of the failure modes which can occur in 85°C/85% RH lifetest, it would be a better indicator for normal operation.[21]

Table X shows the result of the temperature cycling for plastic packages. No failures were observed. The test used 200 temperature cycles for +125°C to −65°C, air to air. (MIL-STD-883, Method 1010) indicates that the plastic packaged device would perform very well under normal temperature variations.

Table XI shows the results (no failures) of low temperature dynamic lifetest. The lack of failures indicates that typical semiconductor failure modes are not a factor in this technology.

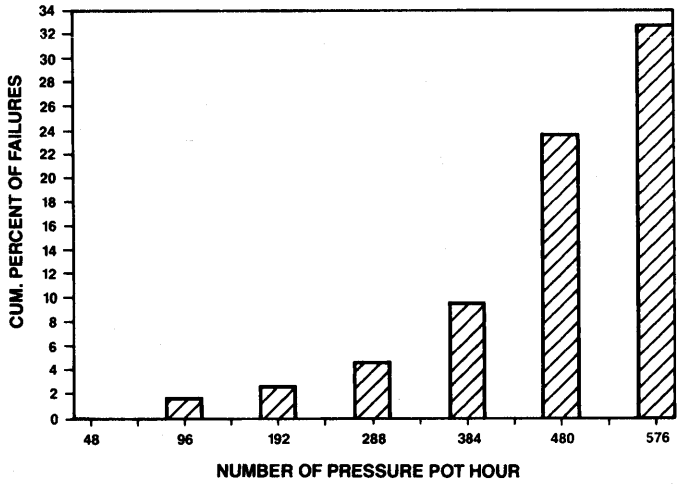


Figure 20: Pressure pot result.

CALCULATION OF PREDICTED FAILURE RATE

There is no simple, one-step formula for inferring a predicted failure rate from the experimental data. Instead, the failures of each individual activation energy must be treated differently. The first step is to calculate the equivalent device hours at the ambient temperature of interest, utilizing the Arrhenius relationship discussed earlier. This calculation should be carried out for every mechanism observed or expected. For example, the calculation for the 0.3eV activation energy oxide rupture mechanism should be carried out whether this failure mechanism is observed or not, since this mechanism is always anticipated in MOS integrated circuits. The extrapolation should be carried out utilizing the junction temperature at the ambient temperature of interest and not the ambient temperature itself. The upper confidence limit is then calculated for the failure rate for each activation energy. The upper confidence limits for the various activation energies are then summed for a total failure rate prediction. The meaning of the "upper confidence level" is that with a certainty, or probability, of a certain level we can say that the true value is less than the stated value. Thus, the confidence level rate calculated is non-zero even for the case where no failures are observed because we can't be sure that there will be none.

Two calculations were performed to separate short term failure rates (infant mortality) and long term failure rate (expected failure rate). This was done to obtain a better picture of the expected failure rates.

Long term failure rates are tabulated in Table XII based on the data in Tables III–V. Voltage acceleration is applied for the 0.3eV activation energy failure mode typical of oxide breakdown. No voltage acceleration is applied to the 0.6eV and 1.0eV failure modes because the dependence for these has not been established. These data lead to a predicted long term failure rate in plastic of 39 FIT (0.0039%/1000 hr) at 60% UCL at 70°C ambient and 18 FIT (0.0018%/1000 hr) at 60% UCL at 55°C ambient. In cerdip the corresponding values are 85 FIT (0.0085%/1000 hr) at 60% UCL at 70°C ambient and 45 FIT (0.0045%/1000 hr) at 60% UCL at 55°C ambient. From these numbers, it should not be concluded that the parts are more reliable in plastic than in cerdip but rather that since there are more hours in plastic than cerdip the uncertainty is reduced and hence the UCL (upper confidence level) is lower. The best single point estimate of the reliability of the part is probably obtained by combining the data on the units in plastic and cerdip packages. This leads to estimated failure rate of 39 FIT (0.0039%/1000 hr) at 70°C ambient and 60% UCL and 16 FIT (0.0016%/1000 hr) at 55°C ambient and 60% UCL.

The above calculations of long term failure rates were done excluding the data for the first 48 hours

PLASTIC									
Activation Energy	**Hours at 125°C**	**Hours at 150°C**	**Number of Failures**	**Equivalent Hours at 70°C**	**Expected Value of Failure Rate at 70°C**	**60% UCL Failure Rate at 70°C**	**Equivalent Hours at 55°C**	**Expected Value of Failure Rate at 55°C**	**60% UCL Failure Rate at 55°C**
0.3eV	1.75×10^6	4.91×10^5	0	9.31×10^7*	—	9.8	1.40×10^8	—	7
0.6eV	1.75×10^6	4.91×10^5	0	3.94×10^7	—	26	8.86×10^7	—	10
1.0eV	1.75×10^6	4.91×10^5	0	3.07×10^8	—	3	1.19×10^9	—	1
Total					—	39		—	18
CERDIP									
Activation Energy	**Hours at 125°C**	**Hours at 150°C**	**Number of Failures**	**Equivalent Hours at 70°C**	**Expected Value of Failure Rate at 70°C**	**60% UCL Failure Rate at 70°C**	**Equivalent Hours at 55°C**	**Expected Value of Failure Rate at 55°C**	**60% UCL Failure Rate at 55°C**
0.3eV	6.05×10^5	3.66×10^5	1	4.86×10^7*	—	41	7.45×10^7	—	27
0.6eV	6.05×10^5	3.66×10^5	0	2.26×10^7	—	40	5.30×10^7	—	17
1.0eV	6.05×10^5	3.66×10^5	0	2.11×10^8	—	4	8.75×10^8	—	1
Total					—	85		—	45

*0.3eV equivalent hours includes voltage acceleration for 7.5eV stress.

Table XII: Long term failure rate (not including 48 hr data point).

of dynamic lifetest. (Note: all units going into other tests received this stress as a preconditioning.) The short term failure fraction, sometimes called infant mortality percentage, can be estimated from these data in Tables IIIA, IIIB. In cerdip, no failures were observed from 1700 units. In plastic, there were 2 failures in 5055 units or 396 ppm. If the data from all packages is combined, a single point estimate is 296 ppm.

These results show that Xicor NOVRAMs have attained failure rates comparable, if not better, to those reported by major suppliers of standard volatile memory products.[18–20]

SUMMARY

The data presented in this reliability report show that the data retention of Xicor's NOVRAM technology is excellent. Even at a high temperature (300°C), only about 2% lose data in 1000 hours. Theoretical grounds for expecting this result are discussed. Two calculations were done, one for short term (48 hours) failure rate and one for long term expected failure rate. These show an overall long term failure rate of 16 FIT at 55°C, 60% UCL and an infant mortality of less than 300 ppm. The cerdip packaging employed is shown to be capable of passing the Group D qualification requirements of MIL-STD-883, Method 5005. Finally, the plastic packaging employed shows excellent 85°C/85% RH result.

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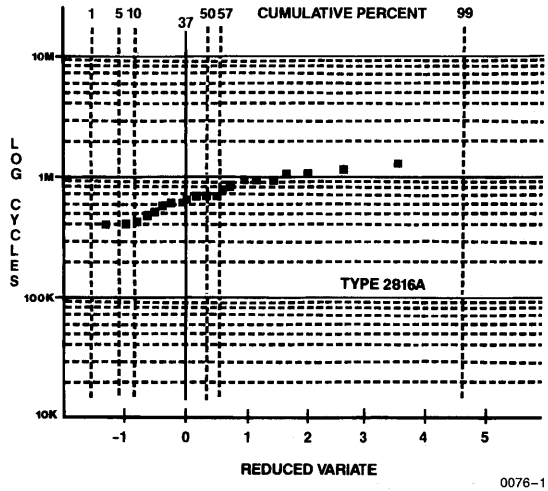
This report is based on data collected through February, 1985.



0076-1

ENDURANCE OF XICOR E²PROMs AND NOVRAMs*

By H.A. Richard Wegener

9

*NOVRAM is Xicor's nonvolatile static RAM device.

INTRODUCTION

Endurance is a property unique to nonvolatile memories. It describes the ability of the nonvolatile memory section of the chip to sustain repeated data changes without failure. Such a data change occurs when a stored "1" is changed into a "0", or when a stored "0" is changed into a "1". Continual changes from "1" to "0" to "1" to "0" are called write-erase cycling, or just cycling.

In this work, endurance will first be defined. A quantitative method for characterizing endurance is described and applied to the characterization of endurance as a function of temperature and time between store events. Data on the endurance of a selection of Xicor's products is presented. Finally, the application of this information to the calculation of system failure rates is described. A general problem in discussions of endurance is that various people mean different things when they speak of endurance. One meaning which has been used is that endurance is the number of nonvolatile data changes to a "typical" cell before the cell dielectric fails or the programming window closes. Figure 1 shows such data for a typical Xicor E^{2}PROM cell showing that after greater than 10^7 data changes the cell still has good margin with respect to the 50 μA trip point of our sense amplifier. Many other suppliers have presented similar data. Unfortunately this data is of little help to the user who doesn't buy one "typical" cell, but rather an array containing a large number of cells, some of which will not be typical.

Xicor's definition of the endurance of an individual memory is that the limit of endurance is reached when, under conditions specified by the data sheet for normal operation, the first bit on any chip is found to be in error after a required data change. This limit of endurance, or endurance for short, is expressed in terms of cycles. By this definition then, endurance (in cycles) is the number of data changes per bit that occurred without error before the first failure took place.

When a nonvolatile memory chip is operating within a given application, it can be expected that some bits on that chip will experience more data changes than other bits, unless particular attention

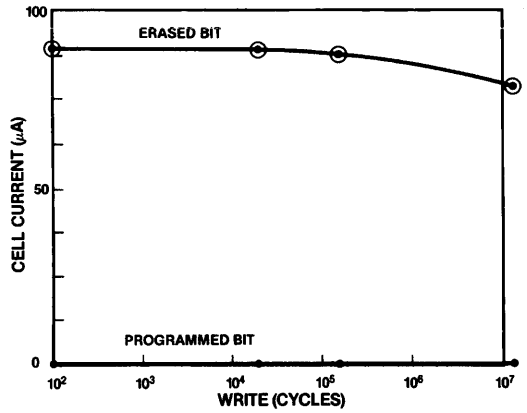


Figure 1: E^{2}PROM cell current vs. write/erase cycles. 50 μA is the trip point of the cell.

has been paid to even out their use throughout the chip. Within a given chip the endurances of individual bits have a small range of values, and it is pure chance whether a highly cycled bit has an endurance on the high end or the low end of that distribution.

Xicor's approach to this problem is that the lowest, the worst case endurance on any given cell in the array, defines the endurance of that chip. In order to test for the bit that causes the worst case endurance, each bit on that chip must be subjected to the same number of data changes during cycling. When the first bit on that chip fails, all other bits have been cycled without failure at least the same number of times. While these other bits may have much higher endurance limits, the endurance of the chip under test is defined as that of the one worst case bit.

Knowledge of the statistical distribution of the worst case bit from each of thousands of devices makes the endurance of a given chip statistically predictable. We have found that our endurance data fit a known statistical distribution — it is the logarithmic "Extreme Value" distribution. Its properties, and the handling of cycling data to derive its parameters for a given lot, are described in Appendix A.

The Measurement of Endurance

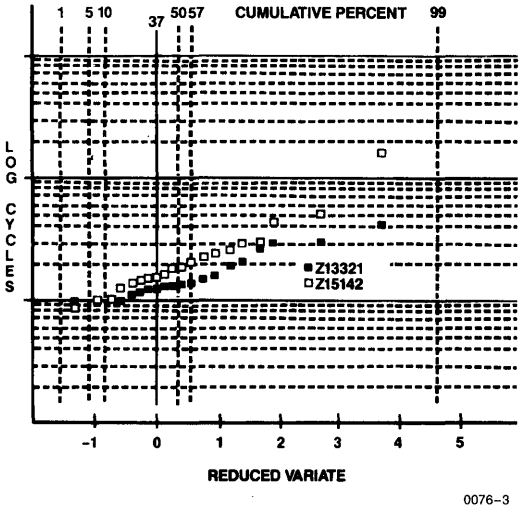


Figure 2: Typical endurance plots of two lots of Xicor X2212 NOVRAMs. The upper horizontal axis gives the cumulative percent of failures.

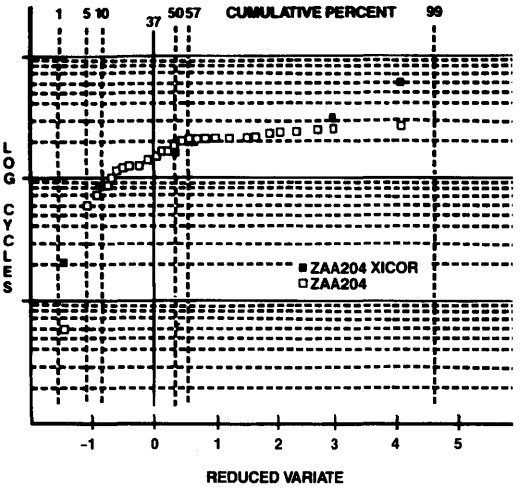


Figure 3: Correlation between endurance data obtained by Xicor and by one of Xicor's customers for Lot ZAA204. Each test is based on 28 data points. Most of Xicor's points are coincident with the customer's so that they are hidden.

The graph in Figure 2 shows the plots of endurances of two different lots of Xicor's X2212 NOVRAMs. This graph is an example of endurance plotted using an extreme value distribution. The meaning of the lower horizontal axis, the linear extreme value variate, is explained in Appendix A. The upper horizontal axis, however, has intuitive appeal. It is the cumulative failure percentage. The plots are well distributed around a straight line. This indicates that they originate from an Extreme Value distribution. They differ somewhat in slope (which is the measure of spread, or dispersion of the distribution). They are also offset in the vertical direction, which indicates that the maximum of each distribution is different. Since the cycles are plotted as their logarithms, this difference is about 40%.

Implicit in this discussion is the assumption that the endurance performance of lots can be described as the result of a relatively small sample. This has been proven correct experimentally and has been used to establish correlation between different pieces of equipment used for the determination of endurance. A successful application of this is shown in Figure 3.

The graph in Figure 3 shows the outcome of an endurance correlation exercise between Xicor and one of its customers. The first set of points (black squares) was established from a 30-device sample of X2212s from lot ZAA204 cycled out at Xicor. Overlying most of these original points are a second set (open squares) which were generated by endurance measurements on a separate 30-device sample from the same lot at the facility of the customer. It can be seen that the signatures of the two samples match faithfully, except at both extremes. At the left hand side, the difference can be explained by the increased scatter of any distribution at its extremes. At the right hand side, a slight difference was introduced when the customer stopped cycling before the last three devices had failed. Even if it is assumed that the match would not have improved by further cycling, the agreement for 27 out of 30 points, or between 5% and 95% of the sample, is excellent.

ENDURANCE VARIABLES

The existence of an inherent limit to endurance is a universal property of nonvolatile semiconductor memories. Regardless of the materials used and of the details of the cell design or the semiconductor manufacturer, there is a measurable upper limit to the number of data changes that such a memory cell can sustain and still meet the data retention specification. The exact number of cycles, however, is dependent on all the elements that go into the construction and operation of a given cell design.

The reason for an endurance limit arises from the basic physics of nonvolatile semiconductor memories. All such memories depend on the highly nonlinear conduction properties of the solid-state dielectrics employed to form the memory cells. At high electric fields, these dielectrics permit a predictable current to pass from one electrode to another. This is used to program or erase such a device. At low electric fields, essentially no electron is transmitted. Therefore charges transferred at high fields to locations isolated by this type of dielectric will remain there indefinitely. But during the transfer of charge at high fields, a very small fraction of the electrons passing through becomes trapped in the dielectric. The many thousands of times that this happens during the life of a memory contribute more and more trapped charge, creating an electric retarding potential in the dielectric, until the device cannot function as a memory any more. Then its endurance limit is reached.

The nonvolatile cells used in Xicor memories make use of the special characteristics of its microtextured surface. The many tiny regions of gently curved features are particularly effective as non-linear conduction elements. As a result of the combination of surface curvature and thick oxide, they require relatively low voltages for programming, and provide excellent retention of data. The physics of the programming process as well as the excellent data retention measured for Xicor memories have been described in a recent publication.[1]

If all these features were identical, if the thickness of the dielectric over them were the same, and if the details of the high voltage generator on the chip were precisely reproducible, then every device on the same silicon wafer, and in the same manufacturing lot would have identical endurance limits. In the real world, there are small variations in the results of the intricate fabrication steps of the silicon chip. These give rise to a range of endurance values for all the nonvolatile memory cells on the same chip. Additional small variations will occur from chip to chip over the whole silicon wafer, and from wafer to wafer. All of these define the details of the distribution that describes the endurances of all the memory cells in a device lot. Once the chips have been fabricated, the average and the dispersion of this distribution have been fixed by the interaction of cell design and the fabrication process with its small variations. These are the fixed internal parameters of endurance. The dispersion is an indicator of the process variation.

There are, however, variations that can be superimposed on the fixed characteristics by the conditions that accompany the normal use of the nonvolatile memory devices. The temperature of operation is one of these. Both the details of the charge transfer process in the nonvolatile memory cell, and the operation of the high voltage generating circuit should be affected in some way by this condition. Another externally controlled parameter is the frequency of the cycling process. At the end of a storage cycle the newly trapped electrons are in a relatively high free energy state. Longer periods between cycles give these charges and their environment more time to relax into a lower energy state. This should also affect the measured endurance parameters.

The control of these external parameters is essential when exact correlation of endurance data must be obtained. Their knowledge is also important to optimize performance and predict reliability in any application.

The Effect of Temperature on Endurance

The endurance of a lot of nonvolatile memories can be described concisely by the constants defining its statistical distribution. For the simple "Extreme Value" distribution pertinent here, these constants are its mode and its dispersion. This distribution can be used to assist in the characterization of endurance.

Five 20-device samples from the same lot of X2212 NOVRAMs were subjected to continuous data changes, each at a different temperature, until all devices had failed. The temperature levels were −55°C, −10°C, +25°C, +70°C, and +125°C. The delay between data changes for all devices was one second. The endurances of individual devices were plotted in the form of a probability plot, as shown in Figure 4.

[1]XICOR Reliability Report RR-502A.

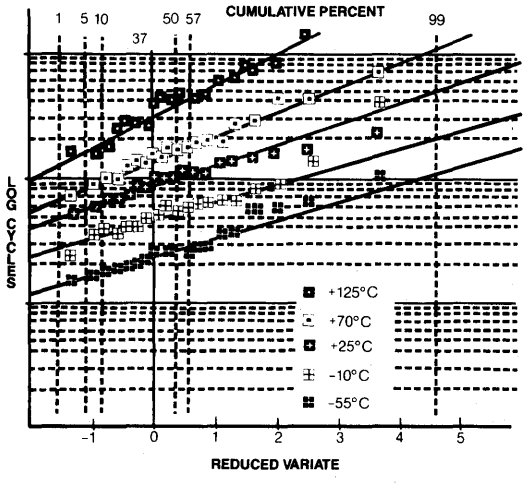


Figure 4: The effect of temperature on endurance: the endurance doubles for every increase in temperature by 50°C.

The y-axis gives the logarithm of the number of cycles that each unit had at the end of its endurance. The straight lines shown were least-squares fitted to each set of data. The correlation coefficients for lines ranged from 97% to 99%. The results can be summarized as follows:

1) There is an increase in the endurance with increasing temperature.

2) The dispersion is essentially constant at and below room temperature and increases somewhat above room temperature.

Over the range of the data, the logarithm of the endurance is linearly related with temperature. The coefficient is 0.0062/°C, but as a simple rule, the endurance doubles for every increase of temperature by 50°C.

The Effect of Data Change Delay on Endurance

The baseline values of endurance can also be modified by the length of the delay between consecutive data changes.

In the determination of the endurance of a lot there is a premium on getting the job done as rapidly as possible. This means that only minimum delays can be added between STORE signals. Typically, the devices in a lot of our current NOVRAMs have endurances between 10,000 and 100,000 cycles. The time to cycle a lot of devices will be 3 hours if the last device to fail had an endurance as low as 100,000 cycles for delays between data changes of 0.1 second even if all devices are cycled in parallel. This total cycling time increases to 28 hours for a delay of 1 second, to 12 days for a delay of 10 seconds, and 120 days for a delay of 100 seconds. Even a 1000 second delay is at the low end of the type of write frequency to be expected in most applications, and this would take in excess of three years to document. For this reason we have limited the experimental work on the effect on lot endurances to delays of 0.1, 1, 10, and 100 seconds. The shortest delay could not be reduced much below 100 ms, since that is the time required by the microprocessor which was used in the test to handle addressing, reading and recording data of the many devices tested simultaneously.

Four 20-device samples were taken from the same lot of X2212 NOVRAMs and then they were cycled until all devices had failed. The endurance of each device was recorded. Each of the four samples had one of the four different data change delays in its cycling program. The data are summarized in Figure 5. Individual data points were not recorded on this graph, since there was much confusing overlap where the data point from the samples overlay each other. Instead, the points were replaced with least-squares fitted straight lines. The correlation coefficients for these lines were between 97 and 99%.

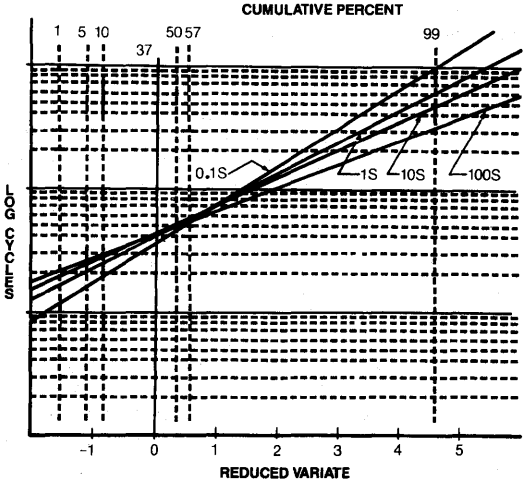


Figure 5: The effect of data change delay on endurance: the maximum of the distribution is unchanged, but it becomes tighter as the delay increases.

The results can be best expressed in terms of the constants of the distributions obtained:

1) The mode of the distribution did not change for the four orders of magnitude of delay tested. This is shown by the fact that the individual lines cross near 37% of the cumulative frequency.

2) The slope of the distribution decreased 15% per decade of cycles with each order of increase in delay. At first sight, this might appear to be a small change. But in the terms of the definition of endurance, they are quite important for many applications. This is because the endurance change in the region where the majority of the units have failed is irrelevant. The important region is that in which only a few per cent or less have failed. In this region, the effect of the longer time between store events at a constant endurance level is to decrease the fraction failing by an order of magnitude or more!

Endurance Status of XICOR Memories

Figure 4 and 5 lack vertical scales because they are intended to show general tendencies. The actual endurance observed on Xicor memories vary from product to product because of differences in cell design and to a lesser amount from lot to lot because of small processing variations. There is also a general tendency for the endurance to improve with time as a result of refinements in design and processing technique.

To give the user a sense of the status of endurance of Xicor memories as of the date of this report, distribution measurements for several product types are reported here. All of this data measured at 25°C and rapid cycling rates. Figure 6 shows the endurance data measured on a lot of X2816As. The process average for this lot is about 500,000 cycles with the 5% point on the curve appearing at 200,000 cycles. In Figure 7 the measured endurance distribution of a lot of X2443s (a 256 bit serial NOVRAM) is displayed. For this device the process average was ~ 80,000 cycles and the 5% point appears at 30,000 cycles. The measured endurance distribution of a lot of X2212s is shown in Figure 8. This product exhibits a process average of about 100,000 cycles and the 5% point appears at 40,000 cycles.

The data reported here are intended as a status report. As we further refine our products and increase the endurance, we intend to issue updates to this report.

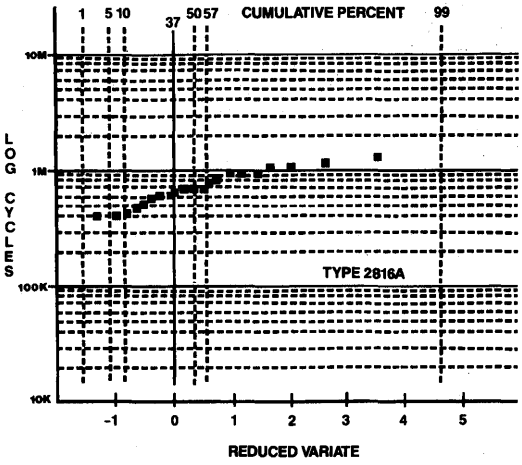


Figure 6: Endurance data from a lot of Xicor X2816A E²PROMs.

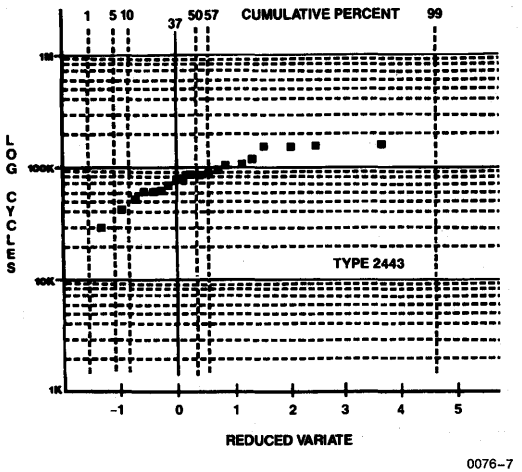


Figure 7: Endurance data from a lot of Xicor X2443 Serial NOVRAMs.

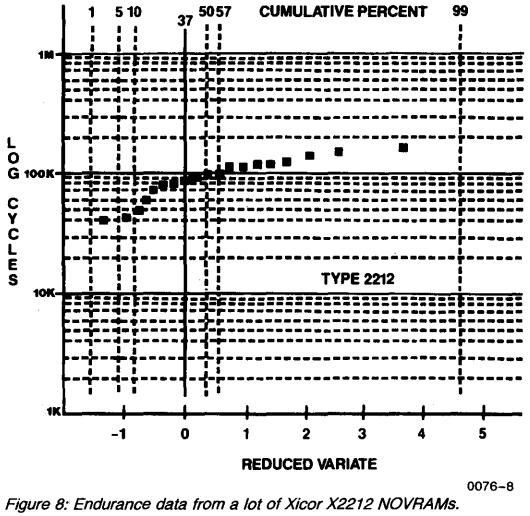


Figure 8: Endurance data from a lot of Xicor X2212 NOVRAMs.

QUALITY ASSURANCE APPLICATIONS

One problem any supplier of nonvolatile memory faces is how to define endurance and how to assure that the parts reaching the customer actually satisfy the endurance specification. This task is akin to assuring the lifetime of a light bulb. If the light bulb is specified to have a 1000 hour life, one can verify that the bulb lasts 1000 hours by burning it for that period. However, one now knows only that the bulb lasted 1000 hours, not that it will last another 1000 hours. The statistical technique discussed in this report allows Xicor to perform this difficult and exacting task. What a Xicor endurance specification means is that for any lot of memories shipped, fewer than 5% of the units will cease to cycle before the specified limit when cycled at room temperature and at the maximum frequency allowed by the specification. Xicor continually samples production lots to assure that this criterion is met.

Let's look at what this means in a typical application. Assume that the Xicor memory is used in an electronic system which contains a number of other components so that the average chip temperature is 50°C and that the average delay between store events is some minutes. Examination of Figure 3 shows that raising the chip temperature from 25°C to 50°C would decrease the fraction of units not exceeding the endurance value from 5% to 0.03%. For data change delays of 100 seconds and longer, the fraction of the lot not meeting the nominal endurance value further decreases to 0.001% or less.

Of course, in a given application the predicted behavior may be better or worse than that worked out in the previous example. However, the information supplied here should be sufficient for the user to compute the expected endurance failure rate in a particular application.

One last consideration is how endurance failures affect the overall device failure rate. Here again, the calculation is a little application-sensitive, but for simplicity assume that the system is designed to last 10^5 hours (~ 12 years) and that the device performs nonvolatile writes roughly uniformly over this period. If the application is designed to use the specified number of cycles over the life of the part, the additional endurance-related failure rate is the cumulative failed fraction divided by the time. For our previous example, this works out to 0.001%/10^5 hours or 10^{-5}%/1000 hours (0.1 FIT). As this illustrates, in most well-designed systems the endurance-related failures of Xicor products do not significantly increase the overall device failure rate.

In all discussions of endurance in this work NOVRAMs and E^{2}PROMs have been treated as if they behave the same. From a physical view of the nonvolatile storage element this is correct. However, there are two properties of the NOVRAM cell which may cause it to have significantly enhanced endurance in certain applications. One factor is that the NOVRAM allows the user to store data in the volatile latch during normal operation and only transfer data to the nonvolatile element prior to power down. In applications which require a high frequency of data changes but only relatively infrequent power interruptions this may be very useful. A second, if less obvious factor, is that unlike the E^{2}PROMs which automatically erase each byte prior to each write, the NOVRAMs only transfer electrons in the case of a change in nonvolatile data. This means that only those cells in which nonvolatile data is altered use up endurance. In some applications this fact can be used to greatly increase effective endurance of the memory.

SUMMARY

A method of characterizing endurance which is of general applicability has been described here. This method has been applied to the characterization of endurance as a function of temperature and time between store events. The meaning of Xicor's endurance specification is defined in the framework of this method. Based on the above, the fraction of Xicor product which is predicted to fail to store prior to attaining the specified endurance is predicted to be less than 0.001% in a typical system in which the devices experience a 50°C ambient temperature.

APPENDIX A

The Mathematics of Endurance Characterization

The mathematical characterization of endurance data arises most elegantly from the definition of endurance. In an individual device, the endurance is the minimum number of data changes that all memory cells can sustain until one cell gives rise to an erroneous output (due to a permanent change in its characteristics). The extreme characteristic from a fixed set of possible values forms a well-known distribution called the Extreme Value distribution. This distribution is independent of the distribution within that fixed set of values. Since by definition, the endurance of a chip containing 1024 memory cells is that of the cell with the minimum endurance, it can be expected that the endurances of the chips from the same device type will have the Extreme value distribution.

The formulations of the Extreme Value distribution are given in Table I. On the left hand side are the entries for the Extreme Value distribution, and on the right hand side the corresponding entries for the Normal distribution.

The cumulative probability Φ is defined by a fraction of 1. It defines, towards one side of a distribution, the fraction of the population Φ that has a smaller value than the variate at that fraction, and towards the other side, the complement of that fraction which has a larger value than the variate at that fraction. This is quite often expressed as "fraction with more than ... " or "fraction with less than ... ". It can be seen that the cumulative probability of the Extreme Value distribution Φ_{EV} has a much simpler functional relationship with its variate Y than the equivalent Φ_N with its variate Z of the Normal distribution. The Extreme Value variate Y is related by two constants to the distributed property X. One constant is the maximum of the distribution U, and the other the dispersion $1/\alpha$. The Extreme Value distribution is not symmetrical around its maximum (as the Normal distribution is). Instead, one side is stretched out more than the other. If the low cumulative probability fraction is on the narrower end, the maximum of that distribution is located at the value of 0.366, or 37%.

This is typical of the distributions of low extremes, and this is the distribution used for endurance values from NOVRAM chips of the same device type. There is one more empirical observation: it is not the number of cycles, but the logarithm of the number of cycles that has the form of the Extreme Value distribution. The X in the expression for the variate then is the logarithm of the observed cycles of individual chip endurances, α is the dispersion of the distribution of these endurances, and U is the observed or interpolated value of the log of the endurance at $\Phi = 0.366$.

The extraction of these two constants from the data could be a complex calculational procedure, but by linearizing the variate Y, it becomes as simple as plotting a straight line. The approach is summarized in Table II.

Statistic	Extreme Value	Normal Distribution
Cumulative Probability	$\Phi_{EV} = EXP(-EXP(-Y)$	$\Phi_N = \int_{-\infty}^{Z} (2)^{-1/2} EXP(-T^2/2)\, dT$
Variate	$Y = \alpha(X-U)$	$Z = (X-M)/\sigma$
Maximum	U at $\Phi = 0.37$	M at $\Phi = 0.50$
Dispersion	$1/\alpha$	σ

Table I: Mathematical definitions.

$\Phi_i = EXP(-EXP-Y_i)$ $Y_i = \alpha(X_i - U)$ $= -LN(-LN\,\Phi_i)$
$X_i = U + (1/\alpha)(-LN(-LN\Phi_i))$ BUT $X_i = LOG\,CY_i$ $U = LOG\,CY_m$
$LOG\,CY_i = LOG\,CY_m + (1/\alpha)(LV)$ CY_i = endurance of part$_i$ CY_m = maximum of distribution $(1/\alpha)$ = slope of line $(LV) = (-LN(-LN\Phi_i))$

Table II: Linearized plot.

The first line states once more the cumulative probability relationship between Φ and Y, and the second line the linear relationship between Y and X. The third line shows that the value of Y can be calculated from the double natural logarithm of Φ. The fourth line expresses the second line as a function of X, and substitutes its functional relationship with Φ. Identification of X with the logarithm of an individual observation, and U with the logarithm of the maximum of the distribution of cycles then leads to the seventh line which states the desired linear relationship. A typical plot is shown in Figure 9. There is clearly a straight line relationship. The value of the maximum occurs at Φ = 37%, and the slope of the line is the value of $1/\alpha$.

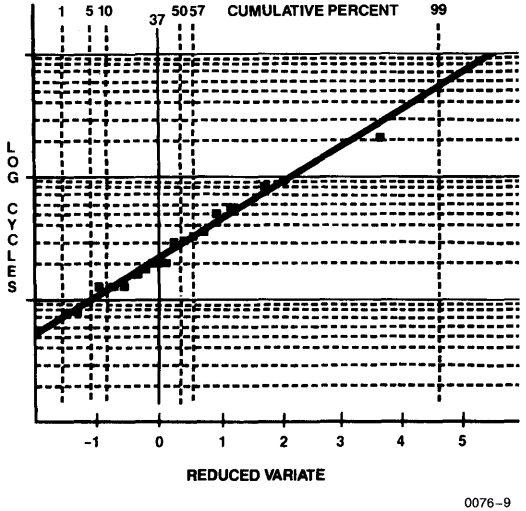


Figure 9: Straight line plot of the logarithm of endurance cycles vs. the reduced variate.

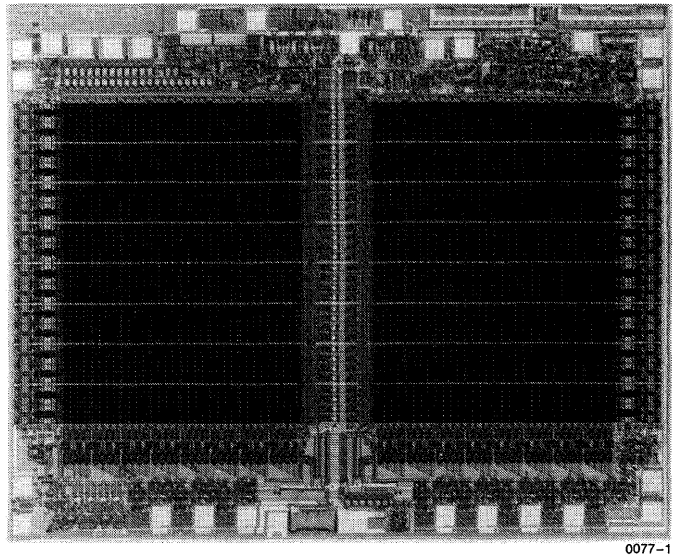
There remains one more problem, and that is how to associate the correct value of Φ with a given observed endurance. This is accomplished by taking all the endurances from a group of devices and writing them down in the order of increasing cycles (this is called "ranking"). Looking at the data in this way, any given endurance represents the borderline between a fraction of the lot that is higher than anything preceding it, and lower than anything following it. The approximate value of that fraction is found by assigning consecutive rank numbers to the ordered endurances: 1 to the lowest, 2 to the second lowest, and so on, until the highest endurance ends up with the rank equal to the total number of devices tested in that group. Dividing the rank numbers by the total number of the devices in the group then yields the "fraction lower than . . . ". A slightly more exact value for Φ is found by the formula $\Phi = (i - 1/2)/N$, where i is the rank number and N the total number of devices tested.

Raw Data (CY)	Ranked Data (CY_i)	Rank (i)	Plotting Position ($\Phi_i = (i-0.5)/n$)
129.50	7.31	1	0.025
35.95	12.10	2	0.075
21.95	12.10	3	0.125
7.31	12.10	4	0.175
31.95	16.85	5	0.225
19.65	19.65	6	0.275
60.75	21.95	7	0.325
33.95	22.45	8	0.375
22.45	22.95	9	0.425
85.75	31.45	10	0.475
12.10	31.95	11	0.525
22.95	33.95	12	0.575
12.10	35.95	13	0.625
79.25	48.25	14	0.675
52.75	52.75	15	0.725
209.50	60.75	16	0.775
16.85	79.75	17	0.825
12.10	85.75	18	0.875
48.25	129.50	19	0.925
31.45	290.50	20	0.975
PLOT LOG (CY_i) vs. $-LN(-LN\Phi_i)$			

Table III: Data preparation.

This report is based on data collected through February, 1984.

NOTES



0077-1

X2816A/X2804A RELIABILITY REPORT

By Reliability Engineering Staff

INTRODUCTION

The X2804A and X2816A are electrically erasable programmable read only memories (E²PROMs) organized 512 x 8 and 2K x 8 respectively. These memories operate on a single 5V power supply for all operations. Figure 1 provides pinouts for the two parts; Figure 2 shows the functional block diagram for the X2816A; Figures 3 and 4 illustrate the physical location of the various address bits. The thermal resistance table, burn-in circuit and a timing diagram are included in Appendix A for your reference.

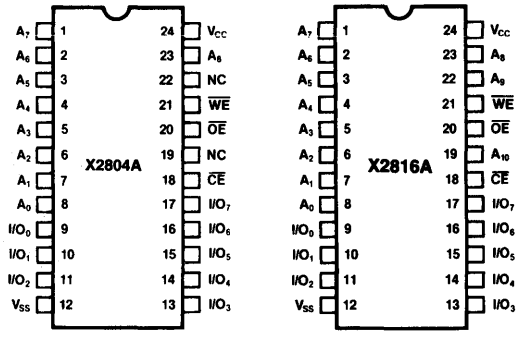


Figure 1: X2804A and X2816A Pin configurations.

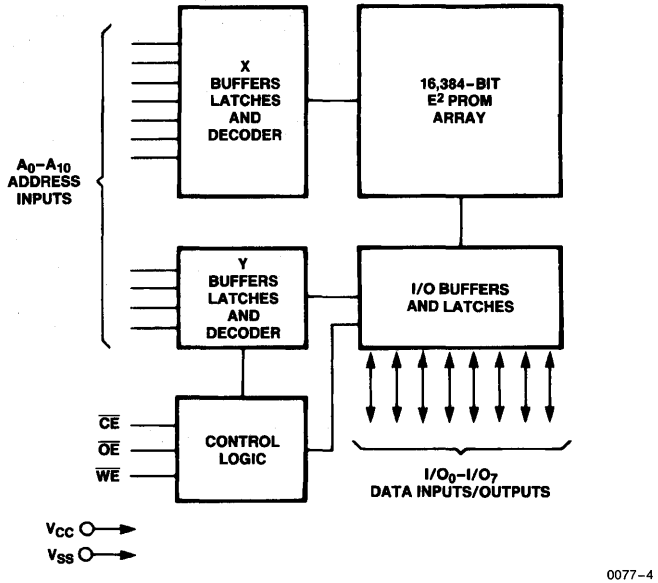
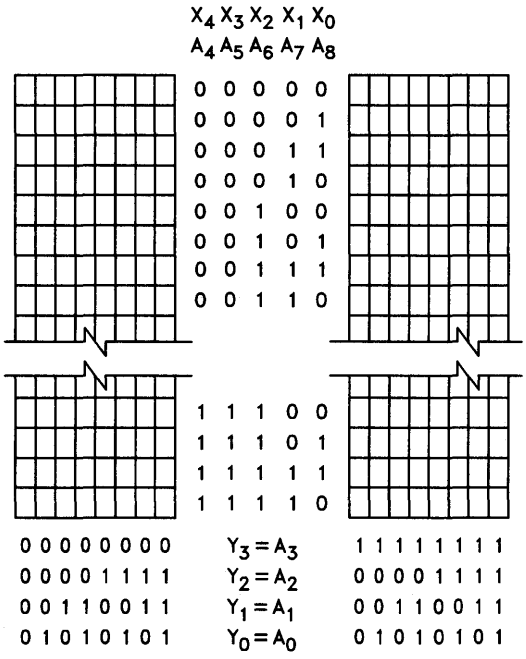
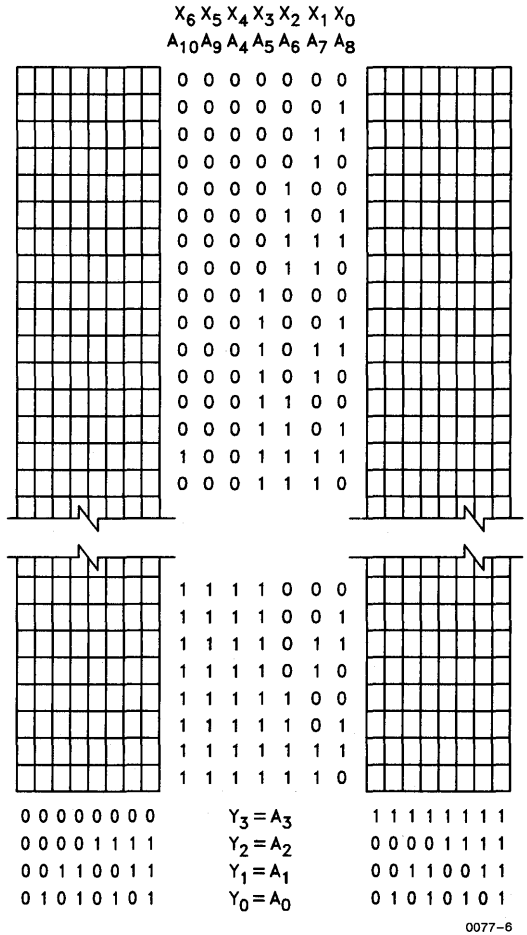


Figure 2: X2816A Functional block diagram.



Each square equals one byte.

Figure 3: X2804A Physical bit map.



Each square equals one byte.

Figure 4: X2816A Physical bit map.

TECHNOLOGY

Xicor E²PROMs are manufactured using a triple polysilicon N-channel process. Data is stored as the presence of positive or negative charge on the second level polysilicon which acts as a gate to a sense transistor. This second level polysilicon is a floating gate surrounded by ~ 750Å of thermally grown oxide. Charge is transferred to and from the floating gate through a quantum mechanical effect known as Fowler-Nordheim tunneling. This phenomenon has been described in detail in recent Xicor publications.[1,2,3]

Xicor's process employs a textured polysilicon. This creates a textured surface between the polysilicon and the tunneling oxides, resulting in a sharp decrease in tunneling current with a decrease in voltage allowing the use of thick tunneling oxides. This in turn results in lower leakage currents from the floating gate during static store periods and during read operations. Recent Xicor publications describe the excellent data retention that can be expected from this technology.[3] For both the X2804A and X2816A Xicor specifies a data retention of 100 years.

RELIABILITY STUDY AND RESULTS

This report is based on data collected using the X2816A. The X2804A is a smaller version of the X2816A, produced by using the design of the X2816A with three-quarters of the array and two address buffers removed. Thus, reliability studies were focused on the X2816A. The X2816A has four times the memory and approximately twice the active silicon area; therefore, it is the more sensitive reliability indicator.

Before Xicor qualifies any new product it is subjected to a series of accelerating stresses and tests. These tests are designed to accelerate any degradation a device may experience over the course of a normal lifetime in order to uncover any design or process flaws. Because package type has an affect on device reliability, complete qualification of the X2816A involved both plastic and cerdip units. In addition, Xicor runs ongoing monitors of those products in production. This assures high reliability standards for all product shipped by Xicor.

The stresses used to establish reliability data are as follows:

1) High temperature dynamic lifetest.
2) Data retention bake.
3) High temperature high voltage stress.
4) Environmental testing.

A short description of these tests and the results obtained are presented in the following report.

Dynamic Lifetest

Failure modes typically encountered in MOS semiconductor devices can be accelerated if the device is operated at elevated temperatures. The dynamic lifetest aims to accelerate any failure modes a device may exhibit by operating the device in its most common mode at high temperature.

For the X2816A, the dynamic lifetest consisted of continually reading a known data pattern stored in the device, while it was subjected to a temperature of +125°C. Each unit was then tested for data retention and complete functionality after 168, 500, 1000 and 2000 hours of dynamic lifetest. The results of the tests are shown in Table I.

Data Retention Bake

The purpose of this stress is to measure and ensure a device's ability to retain correct data. Technologies using floating gate structures to retain charge will all have a greater tendency to loose this charge at higher temperatures.

This test is conducted by storing a checkerboard pattern in the devices under test and then baking the devices at +150°C for plastic units and at +250°C for cerdip units. The pattern is verified after 48, 168, 500, 1000 and 2000 hours of bake. In most cases a group is split and retention evaluated on units that have been precycled (10,000 erase/write cycles) and units that have not been cycled. This provides a base to study the affect (if any) of writing to an E²PROM on data retention. The results of the tests are shown in Tables II and III.

High Temperature High Voltage Stress

The high temperature high voltage test is a derivative of the high temperature reverse bias test used to evaluate bipolar circuits. In this test V_{SS} is grounded while all inputs and V_{CC} are maintained at high voltage while being baked. The stress is intended to expose failures due to mobile ionic contaminants, electrical overstress and latent gate oxide defects.

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1C	0	159	0	84	0	84	0	84	1.8×10^5
2C	0	152	0	93	0	93	1[a]	93	2.0×10^5
3C	0	75	0	75	0	75	0	75	1.5×10^5
4C	0	388	0	99	1[a]	99	0	98	2.5×10^5
5C	1[a]	387	0	126	0	126	0	—	1.7×10^5
1P	1[b]	410	0	51	0	51	0	51	1.6×10^5
2P	0	389	0	76	0	76	0	76	2.0×10^5
3P	0	214	0	15	0	15	0	15	6.3×10^4
Totals	2	2174	0	619	1	619	1	492	1.4×10^6

[a] Ionic contamination: 1eV
[b] Retention failure: 0.6eV
Note: C = Cerdip
P = Plastic

Table I: 125°C Dynamic lifetests results.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	50	0	50	0	50	0	50	0	50	1.0×10^5
2*	0	24	0	24	0	24	0	24	0	24	4.8×10^4
3	0	20	0	20	0	20	0	20	0	20	4.0×10^4
4*	0	55	0	55	0	55	0	55	0	55	1.1×10^5
Totals	0	149	0	149	0	149	0	149	0	149	3.0×10^5

*Denotes units that received 10,000 erase/write cycles prior to retention tests.

Table II: 250°C Cerdip unit, retention bake test results.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	51	0	51	0	51	0	51	0	51	1.0×10^5
2	0	25	1[a]	25	0	24	0	24	0	24	4.8×10^4
3*	0	76	0	76	0	76	0	76	0	76	1.5×10^5
Totals	0	152	0	152	0	151	0	151	0	151	3.0×10^5

[a] Data retention failure: 0.6eV
*Denotes units that received 10,000 erase write/cycles prior to retention test.

Table III: 150°C Plastic unit retention bake test results.

This test was conducted on the X2816A at 5.5V and +150°C. Data retention and functionality were verified after 48, 168, 500, 1000 and 2000 hours. The results of the test are shown in Table IV.

ENVIRONMENTAL TESTING

Environmental tests are designed to determine a device's resistance to extreme or changing environments. Due to the inherent differences between plastic and cerdip devices, different reliability stresses are applied to evaluate the individual package.

Cerdip

The standard tests for cerdip encapsulated devices are defined by MIL-STD-883, Method 5005, Group C and D. The results and conditions of these tests on typical Xicor products are listed in Tables V and VI.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1C	0	25	0	25	0	25	0	25	0	25	5.0×10^4
2C	0	25	0	25	0	25	0	25	0	25	5.0×10^4
3C	0	51	0	51	0	51	0	51	0	51	1.0×10^5
4C	0	25	0	25	0	25	0	25	0	25	5.0×10^4
1P	0	52	0	52	1[a]	52	0	51	0	51	1.0×10^5
2P	0	51	0	51	0	51	0	51	0	51	1.0×10^5
3P	0	15	0	14	0	13	0	13	2[a]	13	2.7×10^4
Totals	0	244	0	243	1	242	0	241	2	241	4.8×10^5

[a] Oxide breakdown: 0.3eV

Note: C = Cerdip
P = Plastic

Table IV: High temperature high voltage stress test results.

Test	883 Test Method	Conditions	LTPD	Accept #	Results
Temperature Cycling	1010	Test Condition C (10 cycles −65°C to +125°C)	15	0/15	0/34
Constant Acceleration	2001	Test Condition E (30,000g Y1 axis)	15	0/15	0/34
Seal	1014		15	0/15	
Fine		Test Condition B			0/34
Gross		Test Condition C			0/34

Table V: Group C, die related tests.

Test	883 Test Method	Conditions	LTPD	Accept #	Results
Lead Integrity	2004	Test Condition B2	15	0/15	0/15
Seal	1014		15	0/15	
Fine		Test Condition B			0/15
Gross		Test Condition C			0/15
Thermal Shock	1011	Test Condition B (15 cycles −55°C to +125°C)	15	0/15	0/34
Temperature Cycle	1010	Test Condition C (10 cycles −65°C to +125°C)	15	0/15	0/34
Moisture Resistance	1004		15	0/15	0/34
Seal	1014		15	0/15	
Fine		Test Condition B			0/34
Gross		Test Condition C			0/34
Mechanical Shock	2002	Test Condition B (1500g peak 3 axis)	15	0/15	0/34
Variable Frequency Vibration	2007	Test Condition A (29g peak 3 axis)	15	0/15	0/34
Constant Acceleration	2001	Test Condition E	15	0/15	0/34
Seal	1014		15	0/15	
Fine		Test Condition B			0/34
Gross		Test Condition C			0/34
Salt Atmosphere	1009	Test Condition A	15	0/15	0/43
Seal	1014		15	0/15	
Fine		Test Condition B			0/43
Gross		Test Condition C			0/42
Internal Water Vapor	1018	5,000 ppm Max. Water Content at 100°C	—	0/3 or 1/5	0/5
Adhesion of Lead Finish	2025		15	0/15	0/15
Lid Torque	2024		—	0/5	0/5

Table VI: Group D, package related tests.

Plastic

Some of the tests used to evaluate cerdip packages do not apply to plastic packages. Tests such as seal, internal water vapor content and lid torque do not apply because plastic packages are not hermetically sealed and do not have lids. Other tests such as vibration and acceleration do not apply because the die in plastic packages are completely embedded in plastic and are not susceptible to such mechanical failures. Plastic packages, however, may be more susceptible to other failure modes. Due to the considerable difference in expansion coefficients between plastic and silicon, plastic devices may be more susceptible to temperature cycling failures. Plastic package devices may also be more susceptible to moisture. Therefore, the plastic units were subjected in greater numbers to more stringent tests.

Temperature Cycling

Plastic packaged devices were subjected to 1000 temperature cycles per MIL-STD-883 Method 1010 Condition C. The results of this test are shown in Table VII.

Lot #	168 Cycles		500 Cycles		1000 Cycles	
	# Fail	# In	# Fail	# In	# Fail	# In
1	0	57	0	57	0	57
2	0	59	0	59	0	59
3	0	30	0	30	0	30
Totals	0	146	0	146	0	146

Table VII: Temperature cycling test results.

85°C/85% Relative Humidity and Autoclave Tests

Because plastic encapsulated devices may be more susceptible to moisture related failures they are subjected to environmental tests at 85°C with 85% relative humidity (both powered-on and powered-off). Three additional sample lots were subjected to autoclave tests (pressure pot) at two atmospheres. These stresses test for corrosion, electrolytic failure modes and passivation integrity. The results of these tests are presented in Tables VIIIA, VIIIB and IX.

85/85 V_{CC} = +5.5V							
Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	52	0	52	0	52	5.2×10^4
2	0	52	0	51	0	49	5.0×10^4
3	0	15	0	15	0	15	1.5×10^4
Totals	0	119	0	118	0	116	1.2×10^5

Table VIIIA: 85/85 Test results, V_{CC} = +5.5V.

85/85 V_{CC} = 0V							
Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	52	0	52	0	47	5.0×10^4
2	0	52	0	51	0	47	4.9×10^4
3	0	15	0	15	0	15	1.5×10^4
Totals	0	146	0	146	0	146	1.1×10^5

Table VIIIB: 85/85 Test results, V_{CC} = 0V.

Note: In both 85/85 tests, each pin was alternately biased to +5V and 0V to provide an electrical potential between adjacent metal lines.

Lot #	48 Hrs.		144 Hrs.		240 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	40	0	40	0	40	9.6×10^3
2	0	34	0	33	0	33	7.9×10^3
3	0	20	0	20	0	17	4.4×10^3
Totals	0	94	0	93	0	90	2.2×10^4

Table IX: Autoclave test results.

Prediction Of Failure Rates

Accelerated testing allows one to identify possible design and process flaws. It also makes it possible to predict failure rates under normal operating conditions. All failure mechanisms are accelerated to some degree by voltage or temperature or both. The degree to which any given failure mode is accelerated is known as the activation energy. Knowledge of a failure mode's activation energy allows one to predict the rate at which that failure mode will occur under normal operating conditions. If the activation energy is not known it can be determined experimentally.[4] Four typical failure mechanisms of the technology employed by Xicor and their corresponding activation energies are:

Oxide breakdown	0.3eV
Leaky oxides	0.6eV
Ionic contamination	1.0eV

Table X presents the predicted failure rates for these activation energies. The results are based on the test data presented in Tables I and IV.

The failure rates predicted are for both plastic and cerdip devices. Such a prediction is valid because all the failure modes found or expected are common to both plastic and cerdip devices. The predicted failure rate is depicted as the "60% upper confidence level" failure rate per 1000 device hours. This means that there is a 60% probability the actual failure rate will be below the rate computed. Sometimes predictions are expressed in FIT units. To convert from the given values to FIT, multiply by 10,000.

A more representative value for the failure rate can be given by the "best estimate". This value gives the most likely failure rate based on the given data. Table XI presents the best estimate values.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate Per 1000 Hrs. at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate Per 1000 Hrs. at 55°C
0.3eV	3	1.3×10^7	0.0310	2.1×10^7	0.0200
0.6eV	2	4.0×10^8	0.0008	1.0×10^9	0.0003
1.0eV	3	6.3×10^8	0.0007	2.8×10^9	0.0002
Totals	8		0.0325		0.0205

Table X: 60% UCL failure rate predictions.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	Best Estimate Failure Rate Per 1000 Hrs. at 70°C	Equivalent Hours at 55°C	Best Estimate Failure Rate Per 1000 Hrs. at 55°C
0.3eV	3	1.3×10^7	0.0280	2.1×10^7	0.0170
0.6eV	2	4.0×10^8	0.0007	1.0×10^9	0.0003
1.0eV	3	6.3×10^8	0.0006	2.8×10^9	0.0001
Totals	8		0.0293		0.0174

Table XI: Best estimate failure rate predictions.

Based on these values it can be seen that the expected failure rate for the X2816A and X2804A is 0.0293% per 1000 hours at 70°C (293 FIT) and 0.0174% per 1000 hours at 55°C (174 FIT).

Endurance

Xicor uses two tests to evaluate the endurance of its E²PROMs. One test utilizes special test modes to enable all bits in a unit to be changed simultaneously. This test is used to measure the ultimate endurance of a sample of units. For reasons discussed in RR-510, this test tends to give a somewhat pessimistic estimate of trapping limited endurance and a slightly optimistic estimate of oxide breakdown limited endurance. Figure 5 shows the endurance distribution from a twenty piece sample from a lot of X2816A showing the intrinsic endurance. In order to monitor the oxide defects, which appear as infant mortality endurance failures, Xicor conducts a test in which the memory is written sequentially 10,000 times on byte-by-byte basis. Two failures were observed on a sample of 300 units from several diffusion lots in this test. As is shown in RR-510, these failures are expected to contribute approximately 10 FIT to the failure rate in typical applications.

SUMMARY

The technology used in producing the X2816A and X2804A are reviewed. The reasons for expecting excellent data retention are presented. A comprehensive set of data covering a variety of stresses are presented. Finally, failure rate predictions are provided.

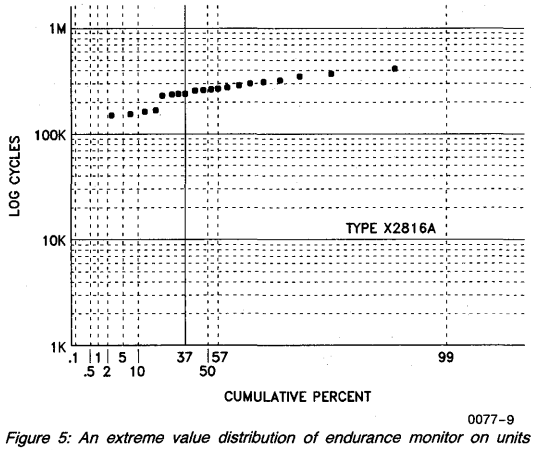


Figure 5: An extreme value distribution of endurance monitor on units cycled in mass mode.

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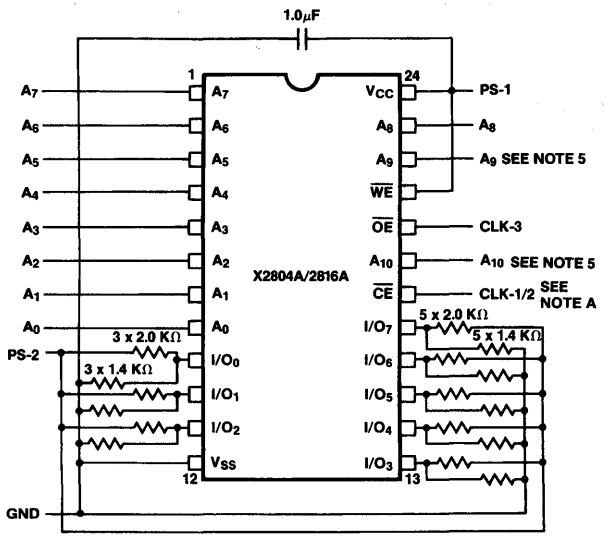
1. R.K. Ellis, *IEEE Electron Device Letters* 13 (1982): pp. 330–333.
2. R.K. Ellis, H.A.R. Wegener and J. Caywood, *International Electron Devices Meeting Technical Digest* (1982): pp. 749–752.
3. J. Caywood and Reliability Engineering Staff, *NOVRAM Reliability Report*, Xicor publication RR-502A (1985).
4. D.S. Peck and O.D. Trap, *Accelerated Testing Handbook*, Technical Associates Publication.

This report is based on data collected through January, 1986.

APPENDIX A

Product	Package Type					
	Plastic		Cerdip		LCC	
	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}
X2804A	50.0	81.0	20.5	36.0	—	—
X2816A	45.0	72.5	18.0	32.0	5.5	53.5

Thermal Resistance Table: θ_{JC} and θ_{JA} expressed in °C per watt.



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Note A:

CLK-1: Rows 1, 3, 5 . . . (odd rows–$\overline{CE_A}$)
CLK-2: Rows 2, 4, 6 . . . (even rows–$\overline{CE_B}$)
Such that: CLK-2 = $\overline{CLK\text{-}1}$

Note B: (1) $\overline{WE}$ must always be hardwired to V_{CC} (Pin 24) at device as shown.

(2) All resistors:
1% metal film
1/4 W

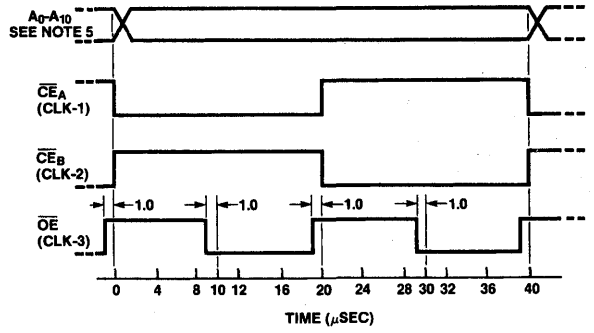
(3) I/O pull-up: 2.0 KΩ
I/O pull-down: 1.4 KΩ

(4) Socket-to-socket isolation as shown.

(5) Pin 19 (A_{10}) and Pin 22 (A_9) are no connects (NC) for the X2804A.

X2804A/2816A (DIP) Burn-in circuit.

9



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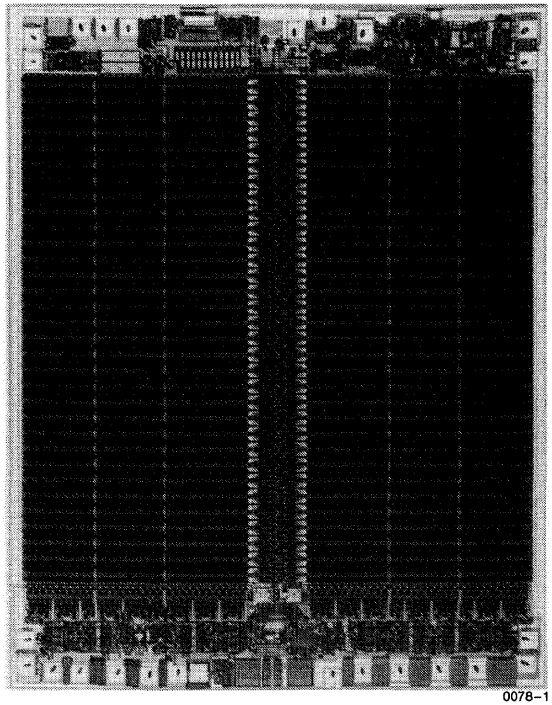
Notes: (1) A_0-A_{10}: binary sequencing address cycle: 40 μs.
(2) $\overline{WE}$ disabled (tied to V_{CC} at device).
(3) V_{IN} Low: 0.4V V_{IN} High: 5.0V
(4) V_{CC}: 5.50V
(5) X2804A: A_0-A_8
X2816A: A_0-A_{10}

X2804A/2816A (DIP) Burn-in timing diagram.



0078-1

BYTE-WIDE NOVRAM* (X2001/X2004) RELIABILITY REPORT

9

*NOVRAM is Xicor's nonvolatile static RAM device.

INTRODUCTION

This report is a summary of the reliability studies conducted by Xicor to qualify the X2001/X2004 family of byte-wide NOVRAMs. The NOVRAM family consists of a static RAM memory array superimposed on a nonvolatile E^{2}PROM memory array. The X2001 is configured as 128 x 8 bit and the X2004 is configured as 512 x 8 bit.

Reliability data was collected using the X2004 as the test device. However, the entire NOVRAM family shares similar circuitry throughout and devices are manufactured employing the same process criteria. Therefore, results gathered for the X2004 are directly applicable to the X2001 through similarity.

Figure 1 provides pinouts for both the X2001 and the X2004. Figure 2 shows the functional block diagram for the X2004 and Figures 3 and 4 illustrate the physical location of the various address bits for both devices. A thermal resistance table, burn-in circuit schematic and timing diagram are included as additional reference information in Appendix A.

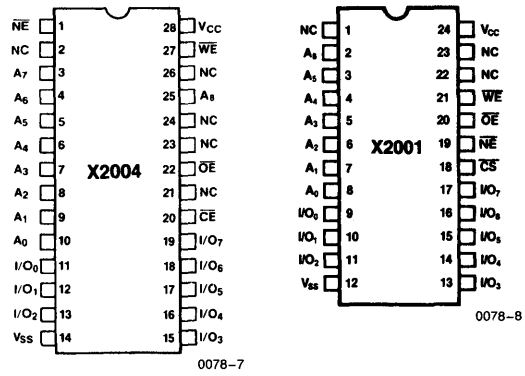


Figure 1: X2004 and X2001 pin configurations.

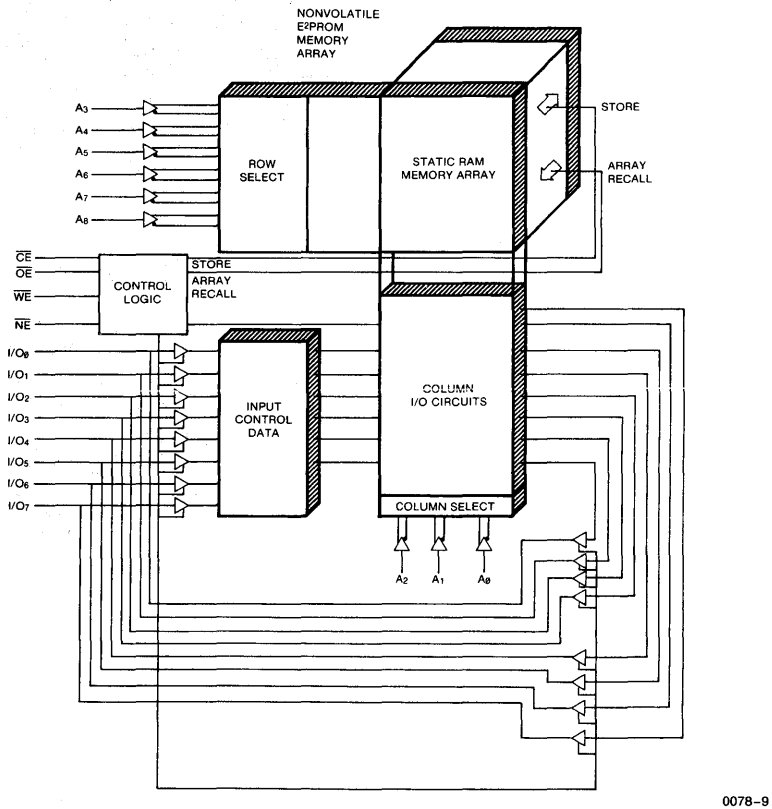
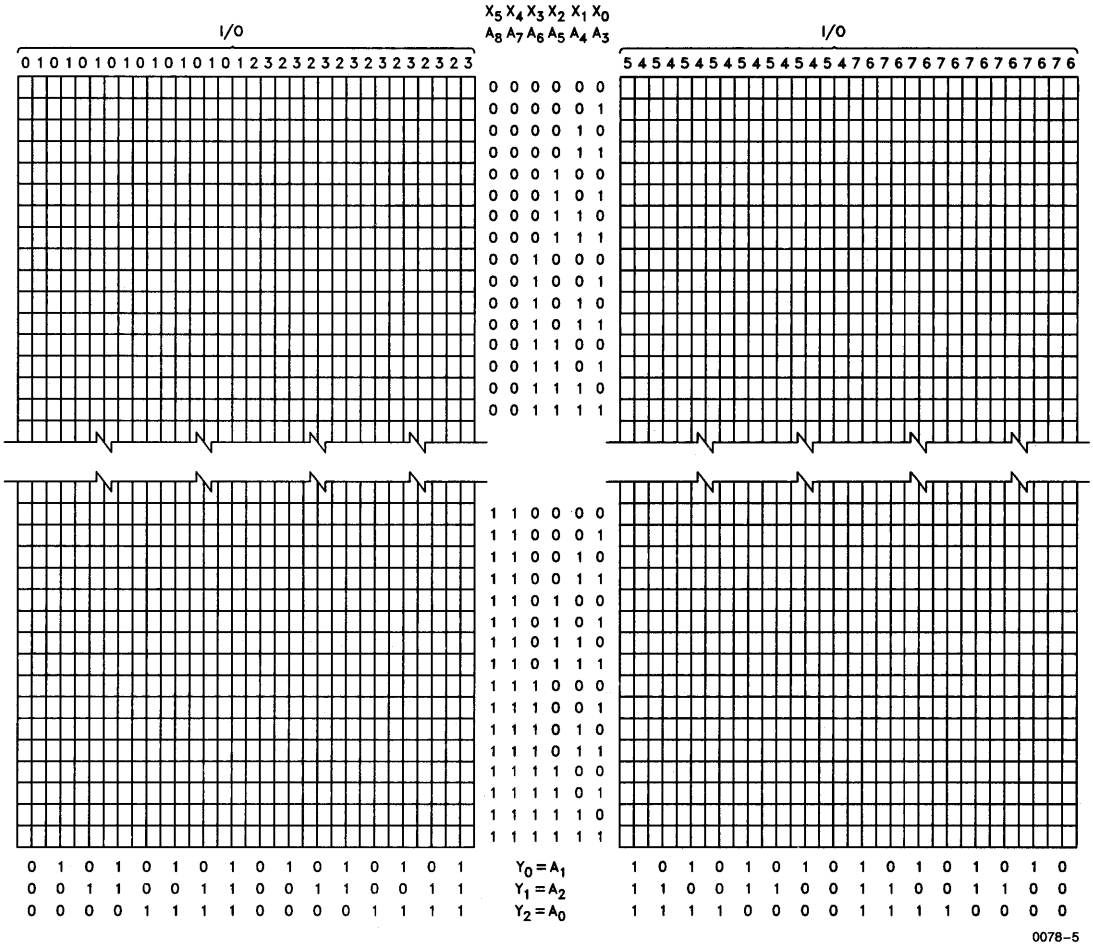
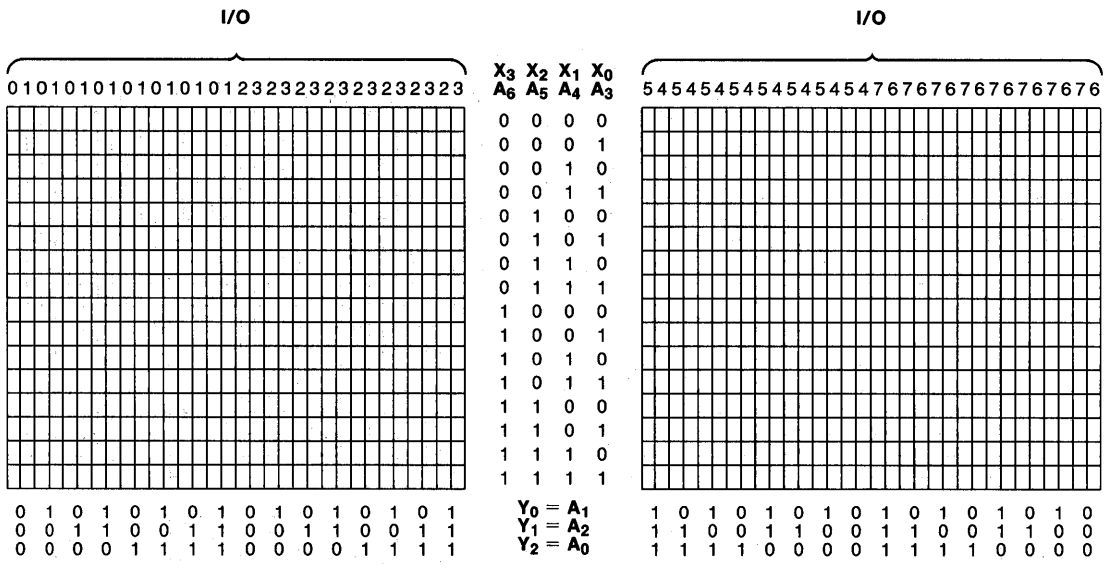


Figure 2: X2004 functional block diagram.



Each square equals one bit.

Figure 3: X2004 physical bit map.



Each square equals one bit.

Figure 4: X2001 physical bit map.

TECHNOLOGY

The X2001/X2004 family is fabricated using N-channel floating gate MOS technology. The memory cell schematic is illustrated in Figure 5. It is comprised of a conventional six transistor static RAM cell and an E²PROM cell. This marriage of two types of memories allows the NOVRAM to operate as a standard SRAM and provide nonvolatile storage of data. Data may be transferred in parallel from RAM into E²PROM (store operation) or from E²PROM into RAM (recall operation). Detailed device operation and timing requirements are contained in the Xicor Data Book.

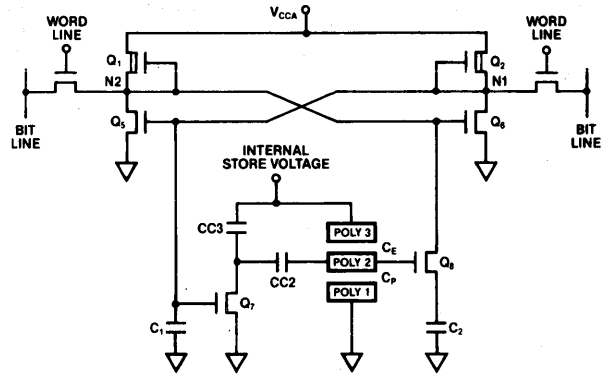


Figure 5: Schematic diagram of a NOVRAM memory cell.

The E²PROM portion of the memory cell employs a proprietary textured poly technology—see Figure 6. Data is stored as the presence or absence of charge on the second level polysilicon which in turn acts as a gate for the read-out transistor. This second level polysilicon is surrounded by ~ 800Å of SiO_2, electrically isolating it from the other layers, and allowing storage of charge on the second level polysilicon. In the E²PROM cell, charge is transferred on or off this storage gate in a controlled manner by means of a quantum mechanical phenomenon called Fowler-Nordheim tunneling.[1]

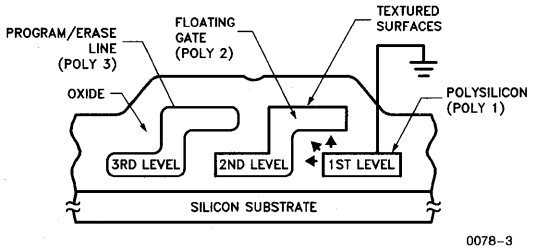


Figure 6: E²PROM cell structure.

Charge transfer occurs only during store operations. The floating gate is either programmed by electron tunneling from Poly 1 to Poly 2, or erased by electron tunneling from Poly 2 to Poly 3. In order to extend endurance of the E²PROM cell, no charge transfer will occur if the state of the RAM cell and E²PROM are already the same.

Nonvolatile Memory Reliability Concerns

E²PROMs are unique semiconductors when examined from a reliability viewpoint. Most LSI semiconductor devices, such as microprocessors, are evaluated solely for semiconductor reliability; generic nonvolatile memories such as EPROMs or ROMs are evaluated for semiconductor reliability and data retention; but E²PROMs must be evaluated for semiconductor reliability, data retention and endurance.

- Data retention refers to the capability of a nonvolatile memory to retain valid data under worst case conditions.
- Semiconductor reliability pertains to several failure modes common to all semiconductors such as oxide rupture and microcracks. These are generally process related failure mechanisms.
- Endurance is the ability of a nonvolatile memory device to sustain repeated data changes.

Semiconductor failures and endurance failures can be further categorized as infant mortality failures, early life failures, random failures and end-of-life, or wearout, failures. These failures fit the classic bathtub curve illustrated in Figure 7. Xicor production test flows are designed to eliminate infant mortality failures and reduce the incidence of early life failures. All devices employed in the reliability study were selected from units that had completed the standard test flow in order to ascertain failure rates that might be experienced after shipment to a customer.

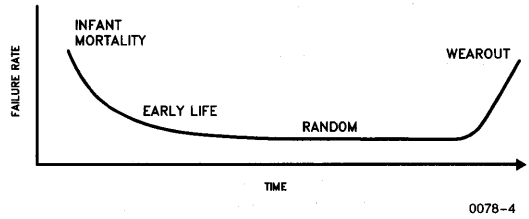


Figure 7: Illustration of bathtub curve of failure rates.

Retention

This test is sometimes referred to as storage bake, but Xicor prefers the term "data retention bake" because this better describes the principal function it serves in the case of electrically programmable nonvolatile memories.

In this test an erase pattern, or a charge that is the opposite of the state that would be read when the gate is at equilibrium, is stored on the floating gate of the E²PROM cells. The devices are then baked at 250°C with no bias applied. At intervals the memory is removed from bake and the nonvolatile data is recalled and verified. The data is **not** restored to the E² array after the readouts in order to ascertain the worst case retention capability.

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Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	24	0	24	0	24	0	24	0	24	0	24	48000
2	0	30	0	30	0	30	0	30	0	30	0	30	60000
3	0	50	0	50	0	50	0	50	0	50	0	50	100000
4	0	50	0	50	0	50	0	50	0	50	0	50	100000
5	0	50	0	50	0	50	0	50	0	50	0	50	100000
Totals	0	204	0	204	0	204	0	204	0	204	0	204	408000

Table I: 250°C data retention bake test results.

Xicor has experimentally determined the activation energy (Ea) for the data loss mechanism of the E^2 cell to be 1.7 eV. The mean time to data loss for this mechanism, which we believe to be the fundamental data loss mechanism of this technology, is 3 million years at 125°C. Table I illustrates the results of the data retention tests performed on the X2004.

Semiconductor Reliability

Table II is a compilation of MOS failure mechanisms and the normal test methods used to accelerate failures caused by each mechanism. The acceleration of failures is required in order to collect statistically useful data in the most expeditious manner.

High Temperature Lifetest

This test employs elevated temperatures to accelerate failure types related to infant mortality and random failures. Data is gathered at 125°C ambient temperature.

An erase pattern is initially stored in the E^2PROM memory array and the RAM is sequentially addressed and written with alternating patterns of ones and zeroes. RAM is read after each write. Full AC and DC testing is done at 48, 168, 500, 1000, 1500 and 2000 hours to insure device functionality. After each of the first five tests the E^2 array is once again erased and the devices continue the lifetest. The results of the tests are shown in Table III.

High Temperature Reverse Bias

This test is performed at 150°C, with the GND pin tied to 0V and all other pins tied to V_{CC}. Two separate tests are performed; the first is with V_{CC} at 5.5V and the second is with V_{CC} at 7.5V. This test is performed to expose failures which might occur as the result of the drift of mobile ions or latent defects in the gate oxides. The results of these tests are shown in Tables IV and V.

Failure Mechanism	Type	Activation Energy	Detection Method
Ionic Contamination	Infant/ Random/ Wearout	1.0eV	High Temp. Bias
Surface Charge	Wearout	0.5–1.0eV	High Temp. Bias
Polarization	Wearout	1.0eV	High Temp. Bias
Electro-migration	Wearout	0.55eV	High Temp. Operating Life
Microcracks	Random	—	Temperature Cycling
Contact Electro-migration	Wearout	0.9eV	High Temp. Bias/ High Temp. Operating Life
Oxide Rupture	Infant/ Random	0.3eV	High Temp. Operating Life
Silicon Defects	Infant/ Random	0.3eV	High Temp. Bias
Oxide Defect Leakage	Infant/ Random	0.6eV	High Temp. Operating Life
Electron Trapping in Oxide	Wearout	0.06eV	Low Temp. High Voltage Operating Life

Table II: MOS failure mechanisms and test acceleration test methods.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1	1[a]	131	0	130	0	81	0	81	0	81	0	81	170280
2	0	187	0	187	0	112	0	112	0	112	0	112	236600
3	0	206	0	206	0	101	0	101	0	100	0	100	218640
4	0	105	0	105	0	0	0	0	0	0	0	0	17640
5	0	189	0	189	1[a]	84	0	82	0	82	0	82	182640
6	0	229	0	229	0	54	0	54	0	52	0	52	135400
7	0	229	0	229	0	55	0	55	0	55	0	55	139232
8	0	238	0	238	1[b]	63	0	62	0	62	0	62	153900
Totals	1	1514	0	1513	2	550	0	547	0	544	0	544	1254332

[a] 1 unit—single bit oxide breakdown, Ea = 0.3eV
[b] 1 unit—ionic contamination, Ea = 1.0eV

Table III: High temperature dynamic lifetest results.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1	0	25	0	25	0	25	0	25					25000
2	0	15	0	15	0	15	0	15					15000
3	0	15	0	15	0	15	0	15					15000
4	0	15	0	15	0	15	0	15					15000
5	0	15	0	15	0	15	0	15					15000
6	0	25	0	25	0	25	0	25	0	24	0	24	49000
7	0	25	0	25	0	25	0	25	0	24	0	24	49000
8	0	25	0	25	0	25	0	25	0	25	0	25	50000
Totals	0	160	0	160	0	160	0	160	0	73	0	73	233000

Table IV: High temperature reverse bias lifetest results at 5.5V.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
3	0	15	0	15	0	15	0	15	15000
4	0	15	0	15	0	15	0	15	15000
5	0	15	0	15	0	15	0	15	15000
Totals	0	45	0	45	0	45	0	45	45000

Table V: High temperature reverse bias lifetest results at 7.5V.

Failure Rate Calculation and Reliability Prediction

High temperature lifetest and high temperature reverse bias data are used to calculate the failure rates. If we ignore the infant mortality failures (failures before 48 hours burn-in), we can then calculate the failure rate for the useful life of the device as follows:

$$\text{Failure Rate } (T_s) = \frac{\text{Number of failures}}{\text{Device hours } (T_s)}$$

T_s = Stress temperature

The above equation will be useful only to calculate the failure rate at the stress temperature under which the tests were performed. In most cases, the actual operating temperature of the device will be much lower; therefore, the equation needs to be modified to reflect the failure rate at the operating temperature. The failure rate for a given activation energy is calculated as follows:

$$\text{Failure Rate } (T_d)_i = \frac{N_i}{DH(T_s) \times TAF(T_s,T_d)_i \times VAF(V_s,V_d)_i}$$

Where:

Failure Rate (T_d) = Failure rate at temperature T_d

$DH(T_s)$ = Device hours at stress temperature

$TAF(T_s,T_d)$ = Temperature acceleration factor from $T_s \longrightarrow T_d$

i = A given activation energy

N_i = Number of failures for activation energy i

T_s = Stress temperature

T_d = Desired temperature

$VAF(V_s,V_d)$ = Voltage acceleration factor from $V_s \longrightarrow V_d$

V_s = Stress voltage

V_d = Desired voltage (5.5V)

The voltage acceleration factor is 1 for all failure mechanisms except TDDB (time dependent dielectric breakdown where Ea = 0.3eV). This can be calculated using Crook's equation:[2]

$$VAF(V_s,V_d) = \exp\left[(E_s - E_d)/E_{ef}\right]$$

Where:

E_s = Field (stress) = V_s/T_{ox}

E_d = Field (desired) = V_d/T_{ox}

E_{ef} = Field constant = 0.062 Mv/cm

T_{ox} = Oxide thickness

The temperature acceleration factor for a given activation energy can be calculated using the Arrhenius equation:

$$TAF(T_s,T_d) = \exp\left[(Ea/K)\,(1/T_s - 1/T_d)\right]$$

Where:

Ea = Activation energy (eV)

K = Boltzmann's constant (8.63×10^{-5} eV/°K)

T_s = Stress temperature (junction) in °K

T_d = Desired temperature (junction) in °K

The above equation is valid for only one activation energy. To predict the total failure rate for the device at the desired temperature the calculated failure rates for each activation energy must be summed.

$$\text{Total Failure Rate } (T_d) = \sum_i \frac{N_i}{DH(T_s) \times TAF(T_s,T_d)_i \times VAF(V_s,V_d)_i}$$

Using the above equation, we calculated the failure rate based on the experimental results. These calculations are summarized in Table VI. We have also included in that table a 60% upper confidence level (UCL) calculation. This indicates that, with a 60% confidence, the actual failure rate will be below that calculated. The equation below is used to determine the 60% UCL.

$$\text{Total Failure Rate } (T_d) = \sum_i \frac{X^2(1-CL)\,(2N+2)}{2 \times DH(T_s) \times TAF(T_s,T_d)_i \times VAF(V_s,V_d)}$$

Where:

X = The chi-square function

CL = The confidence limit (60%)

2N+2 = The degrees of freedom

E_a in eV	Total Device Hours		# of Fails	Equivalent Device Hours		Calculated Failure Rate FIT		60% UCL Failure Rate FIT	
	@125°C	@150°C		@55°C	@70°C	@55°C	@70°C	@55°C	@70°C
0.3	1.18×10^6	2.78×10^5	1	2.91×10^7	1.97×10^7	35	51	70	105
0.6	1.18×10^6	2.78×10^5	0	4.65×10^7	2.15×10^7	0	0	20	43
1.0	1.18×10^6	2.78×10^5	1	5.38×10^8	1.34×10^8	2	7	4	14
Totals			2			37	58	94	162

Note: FIT × 0.0001 = failure rate per thousand hours.

Table VI: Summary of semiconductor failure rate calculations.

In calculating the data presented in Table VI we used the actual junction temperature and not ambient temperature. We also made the conservative assumption of including the oxide leakage failure rate (E_a = 0.6eV). This failure mechanism should be included whether observed or not, since it is always anticipated in E²PROM technology. Had we only considered observed failures, as many vendors do, the 60% UCL failure rate at 70°C and 55°C would have been 119 and 74 FIT respectively versus the more conservative calculation of 162 and 94 FIT.

The results in Table VI are long term failure rates and were determined by excluding data for the first 48 hours of the dynamic lifetest. Infant mortality can be calculated from the data contained in Table III. There was one failure out of 1514 units tested.

Infant mortality rates and long term failure rates indicate Xicor's byte-wide NOVRAMs have attained failure rates comparable to, if not better than, those reported by semiconductor suppliers of standard volatile memory products.[5,6,7]

Endurance

A key factor in memory system reliability is the ability of the device to sustain repeated data changes. In the static RAM portion of the NOVRAM there are only typical semiconductor reliability factors to consider. However, the E² array is subject to limitations on the number of data changes a cell may undergo (its limit of endurance). Xicor considers the endurance limit of a memory is reached when the first single bit failure occurs. This limit of endurance is expressed as the number of data changes the entire array can sustain before a single bit fails to change.

The endurance test employed is to alternately store all ones and zeroes in the memory array. The array is verified after each data change. Upon detection of the first single bit failure, the number of cycles the device endured is recorded.

Figure 8 contains the data for a typical monitor lot of X2004. The data is displayed in an extreme value distribution plot. Further details on endurance cycling and performance can be found in Xicor publications RR-504: Endurance of Xicor E²PROMs and NOVRAMs; and RR-510: Endurance of Nonvolatile Memories.

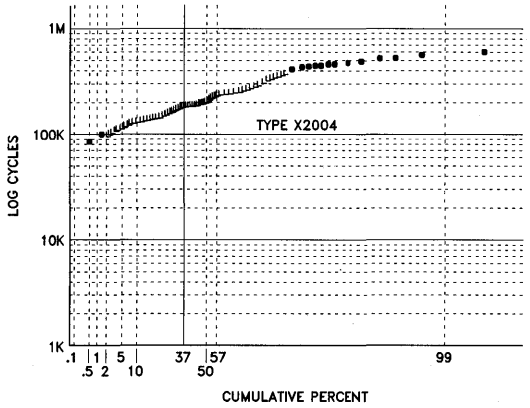

Figure 8: Extreme value distribution plot for X2004.

Low Temperature Dynamic Lifetest

In addition to the preceding tests which pertain to standard failures related to nonvolatile memories, Xicor undertook a test to determine if hot electron trapping was of concern to this device family. The low temperature dynamic lifetest is functionally identical to the high temperature dynamic lifetest but with the ambient temperature at −40°C. This test is intended to detect hot electron trapping in the gate oxide. As can be seen by the test results in Table VII, there was no indication of hot electron trapping in these devices.

Environmental Testing

This group of tests is performed on plastic packages to insure that excessive humidity and ambient vapors will not cause failures and to insure that temperature cycling will have no adverse effects on the materials used.

The three major failure modes for plastic packaged devices under moisture test are:

- Mobile Ions—Ions on the passivation glass are made more mobile by humidity. If enough charge transfer occurs, a device parameter could be altered, or a parasitic transistor could be introduced, degrading device performance.
- Chemical Corrosion—Phosphorous is commonly used in small quantities in passivation and under metalization layers. Phosphorous, when combined with water molecules, produces phosphoric acid which may etch away aluminum lines.
- Electrolytic Corrosion—When a voltage potential exists between two adjacent metal lines under enhanced surface conditions, such as presence of moisture, an electrolytic corrosion process may be triggered. This condition could result in an open metal line.

Autoclave and 85°C/85% relative humidity tests are conducted to test for these failure modes.

Autoclave

Autoclave, or pressure pot testing, subjects a device to a two atmosphere steam environment. This test will accelerate mobile ion drift, chemical corrosion, and to some extent, electrolytic corrosion. The test results are summarized in Table VIII.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
2	0	30	0	30	0	30	0	30	0	30	0	30	60000
3	0	25	0	25	0	25	0	25	0	25	0	25	50000
4	0	25	0	25	0	25	0	25	0	25	0	25	50000
5	0	25	0	25	0	25	0	25	0	25	0	25	50000
Totals	0	105	0	105	0	105	0	105	0	105	0	105	210000

Table VII: Low temperature dynamic lifetest results.

Lot #	48 Hrs.		144 Hrs.		240 Hrs.		336 Hrs.		432 Hrs.		528 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
6	0	48	0	48	0	48	0	48	0	48	0	48	25344
7	0	49	0	49	0	49	0	49	0	49	0	49	25872
8	0	50	0	50	0	50	2[a]	50	0	48	0	48	26016
Totals	0	147	0	147	0	147	2	147	0	145	0	145	77232

[a] 2 units—open pins, chemical corrosion

Table VIII: Autoclave test results.

85°C and 85% Relative Humidity

85/85 testing is performed to determine the life expectancy of devices in high temperature and high humidity environments. This test will accelerate the three environmental failure modes. It is an especially good test for detecting electrolytic corrosion.

85/85 tests can be performed in two ways. The first is by supplying voltage to V_{CC} with all other pins alternately biased at 0V and +5V. In this method, heat generated by power dissipation can reduce the relative humidity on the die surface to as low as 45%. The second method is to test the device with V_{CC} at 0V and all other pins alternately biased at 0V and +5V. This provides a potential between metal lines and insures maximum humidity at the die surface. The second method is more stringent and is the method used to test the X2004. The results of the test are listed in Table IX.

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.	
	# Fail	# In	# Fail	# In	# Fail	# In
6	0	50	0	50	0	50
7	0	50	0	50	0	50
8	0	50	0	50	0	50
Totals	0	150	0	150	0	150

Table IX: 85°C/85% test results.

Temperature Cycling

This test subjects the devices to temperature extremes of −65°C to +165°C. This test is performed to stress the package to detect poor bond wire attachment, and to determine if there is a potential problem due to thermal mismatch between the die and the package material that could cause device failure. The results of this test are tabulated in Table X.

Lot #	168 Cycles		500 Cycles		1000 Cycles	
	# Fail	# In	# Fail	# In	# Fail	# In
6	0	50	0	50	0	50
7	0	50	0	50	0	50
8	0	50	0	50	0	50
Totals	0	150	0	150	0	150

Table X: Temperature cycling test results.

Lifetest Monitor

In order to ensure the continuous supply of the highest quality and most reliable product possible, a periodic lifetest monitor system is maintained. This monitor systematically samples current production material, and subjects it to stress testing designed to induce failures.

This monitor serves a dual purpose. First, it is used to monitor the device infant mortality rate which is an indicator of process or manufacturing defects. If an unusually high failure rate were to be observed, corrective action could be initiated before defective units were ever shipped to the customer. Second, long term failure rates can also be monitored. This establishes a method to track and maintain long term reliability.

Table XI shows monitor results for dynamic lifetests at +125°C from 1987 through 1988.

48 Hrs.			168 Hrs.			500 Hrs.			1000 Hrs.		
# In	# Fail	% Fail	# In	# Fail	% Fail	# In	# Fail	% Fail	# In	# Fail	% Fail
686	3	0.44	296	0	0.00	296	1	0.34	295	0	0.00

Table XI: DLT monitor results from 1987 through 1988.

SUMMARY

The data presented here shows excellent data retention characteristics. Reliability testing shows no retention failures. The X2001/X2004 family exhibits low semiconductor failure rates and high end-of-life endurance figures. The endurance characteristic of the X2004 is typically over 100,000 cycles. Inherent data retention is in excess of 100 years.

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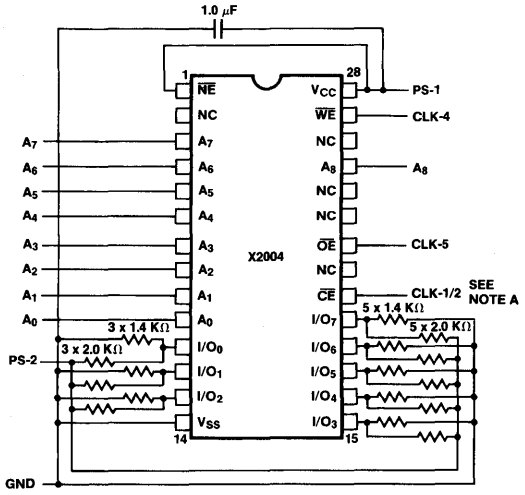
1. R.H. Fowler and L. Nordheim, Proceedings of the Royal Society of London, A119, (1928); pp. 173–181.
2. Dwight L. Crook, 17th Annual Reliability Symposium, (1979); 1–7.
3. H.A.R. Wegener, *Endurance of Xicor E^2PROMs and NOVRAMs,* (Xicor, 1984).
4. Bruce Euzent, *2115/2125 N-Channel Silicon Gate MOS 1K Static RAMs,* (1976) Intel Reliability Report RR-14.
5. Chieh Lin Ping, *Reliability of N-Channel Metal Gate MOS/LSI Microcircuits,* (1982), National Semiconductor.
6. Bruce Euzent and Stuart Rosenberg, *HMOS Reliability,* (1978), Intel Reliability Report RR-18.

This report is based on data collected through March, 1989.

APPENDIX A

Product	Package Type					
	Plastic		Cerdip		LCC	
	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}
X2001	42.7	77	19.5	34.5	—	—
X2004	39.5	64.3	16.5	33.5	5.0	46.5

Thermal Resistance Table: θ_{JC} and θ_{JA} expressed in °C per watt.



0078-10

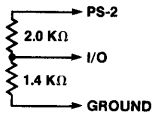
Note A:

CLK-1: Rows 1, 3, 5, . . . (odd rows = $\overline{CE}$-A)
CLK-2: Rows 2, 4, 6, . . . (even rows = $\overline{CE}$-B)
CLK-2 = $\overline{CLK}$-1

Note B: (1) $\overline{NE}$ (Pin 1) must be hardwired to V_{CC} (Pin 28) at device as shown.

(2) All resistors:
1% metal film
1/4 W

(3) All I/O's:



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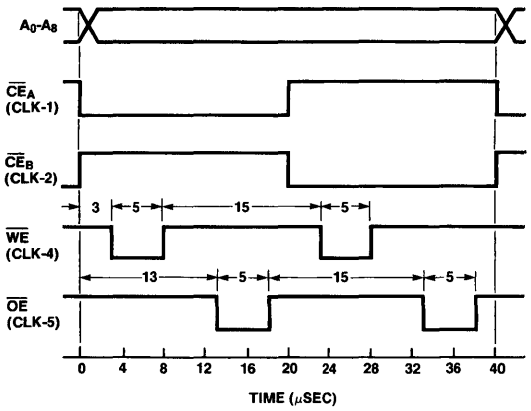
(4) Socket-to-socket isolation as shown.

X2004 (DIP) Burn-in circuit.



0078-11

Notes: (1) A_0-A_8: binary sequencing cycle period: 40 μs.

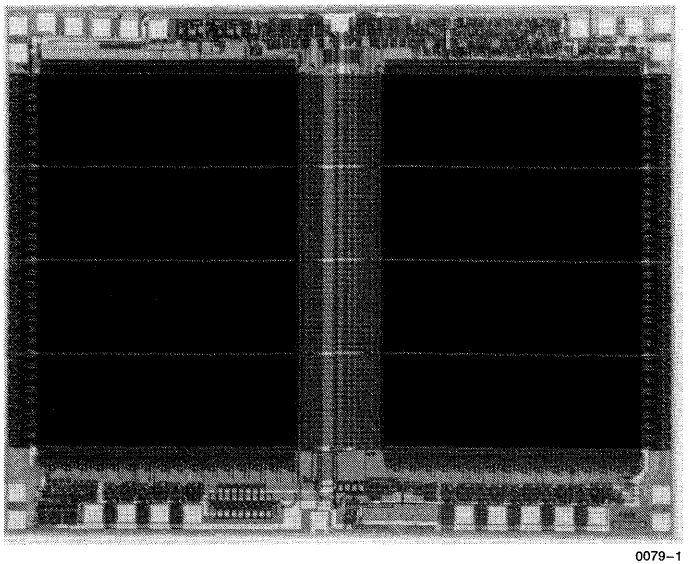
(2) $\overline{NE}$ disabled (tied to V_{CC} at device).

(3) Low state: 0.4V max.
High state: 5.0V typ.
V_{CC}: 5.50V

X2004 (DIP) Burn-in timing diagram.

9

NOTES



0079–1

X2864A RELIABILITY REPORT

By Troy Kaysser
and Lori J. Purvis

9

INTRODUCTION

The X2864A is a 64K bit electrically erasable programmable read only memory, E²PROM, organized 8K x 8. This memory operates on a single 5V power supply for all operations. Figure 1 provides the 64K pin configuration; Figure 2 shows the functional block diagram; Figure 3 illustrates the physical location of the various address bits. The thermal resistance table, burn-in circuit and a timing diagram are include in Appendix A for your reference.

The X2864A is manufactured using Xicor's rugged, textured poly technology. Xicor has shipped more than 20 million memories manufactured with this technology. Because the X2864A is a mature part which has been in volume production for some time, this report contains data from the production reliability monitor as well as reliability qualification data.

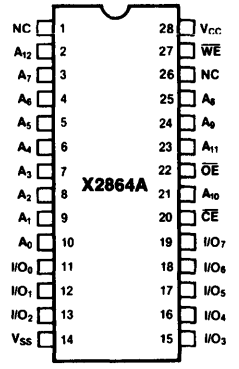


Figure 1: X2864A Pin configuration.

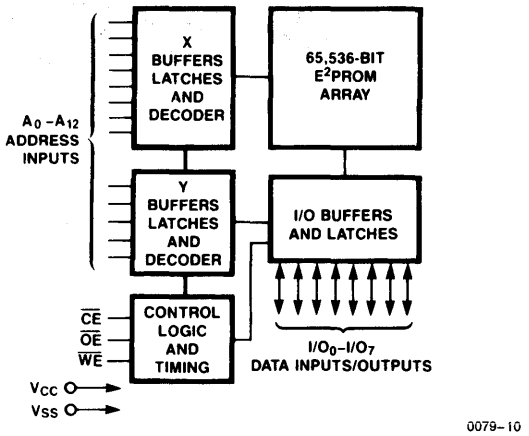
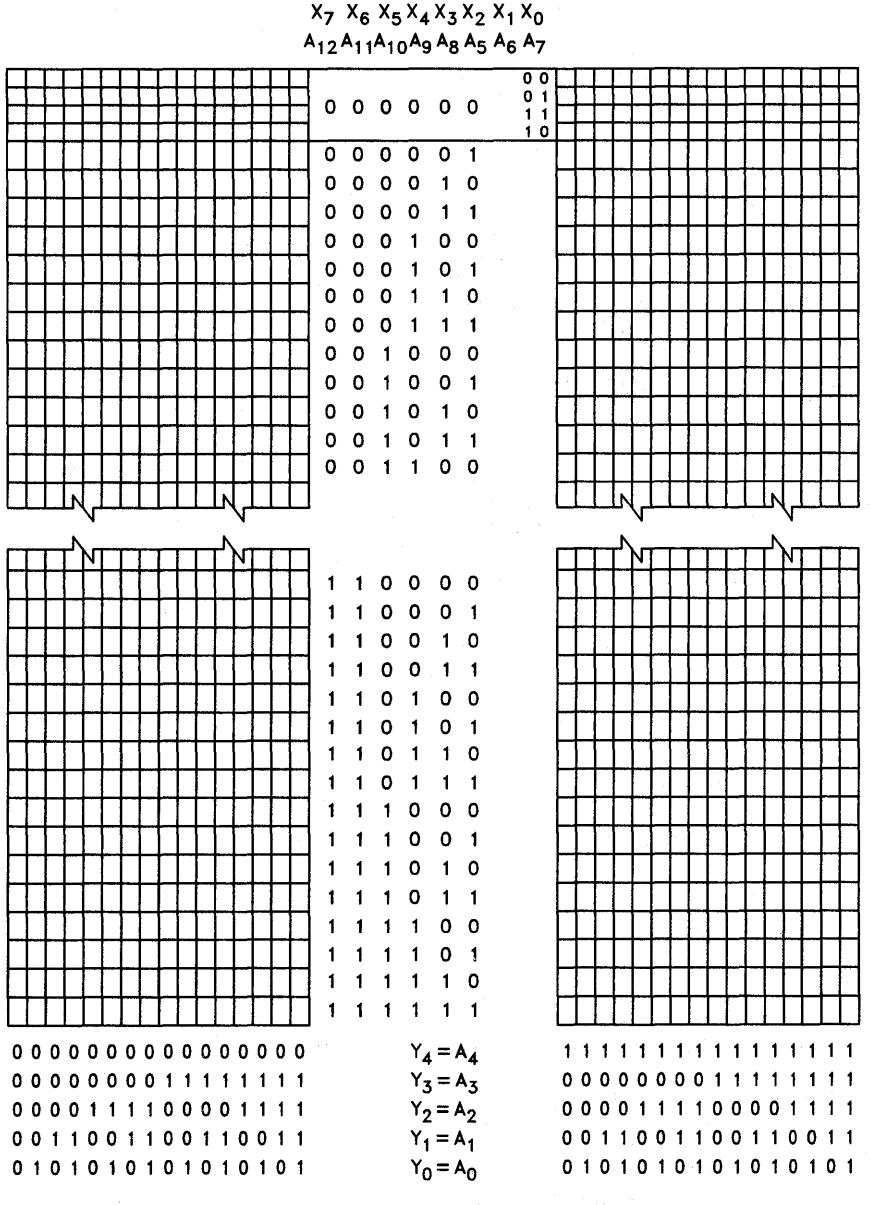


Figure 2: X2864A Functional block diagram.



0079-11

Each square equals one byte.

Figure 3: X2864A Physical bit map.

In the next section the operation of the textured poly E²PROM cell is described. The remainder of the report covers experiments designed to probe the reliability of the part beginning with the two attributes unique to E²PROMs: data retention and endurance. The data show that at 55°C retention contributes approximately 1 FIT to the device failure rate while endurance contributes about 10 FIT in a typical application. After the E²PROM specific experiments, standard accelerated lifetest and accelerated package tests are reported in order to complete the study on this component. These results are used to predict operating failure rate. The predicted result is 50 FIT at 55°C, 60% UCL.

TEXTURED POLY E²PROM CELL

The cross sectional structure of a textured poly cell is shown in Figure 4. It consists of 3 layers of poly with overlap forming three transistors in series. The floating gate transistor is in the middle formed by poly 2. The floating gate is surrounded by silicon dioxide for high retention. Programming is achieved by electrons tunneling from poly 1 to poly 2 and erase is achieved by electrons tunneling from poly 2 to poly 3.

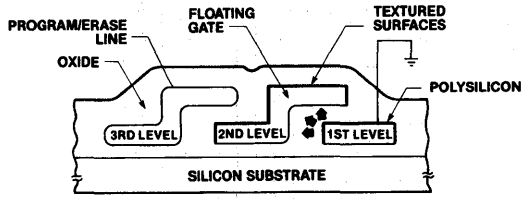


Figure 4: Cross sectional structure of a textured poly memory cell.

In reading the datum stored in the cell the poly 3 select transistor is enabled. The current flow through the cell is determined by the charge state of the poly 2 floating gate. If it is charged positively when the bit is selected, current flows through the cell which is sensed as a "1". If it is charged negatively, a "0" results. During writing the poly 3 is set to a high voltage (> 20V). The poly 2 floating gate is capacitatively steered either high or low. If the floating gate is steered low, the large voltage drop occurs between poly 2 and poly 3 causing electrons to tunnel off the floating gate, leaving it in a positively charged erase state. If the floating gate is steered high, the large voltage drop occurs between poly 1 and poly 2 causing electrons to tunnel from poly 1 onto the floating gate charging it negative.

DATA RETENTION

Textured poly tunneling structures have a significant advantage in data retention in comparison with those employing flat surfaces and thin oxides. One basis for this advantage is illustrated in Figure 5, in which the current-voltage (J-V) characteristics of a tunneling device which employs a thin oxide between planar surfaces and, a tunneling device which employs a thick oxide between textured silicon surfaces, are compared. For this comparison we match the currents in the high current region since most memories are designed to program in about the same time period (~ 10 ms). As can be seen, the same current can be obtained from a smooth surface with 125Å thick tunnel oxide or from a textured surface with an 825Å thick tunnel oxide. Note however, that at lower values of applied voltage typical of read and storage conditions, the current emitted from a textured surface is approximately four orders of magnitude lower than that from a smooth surface.

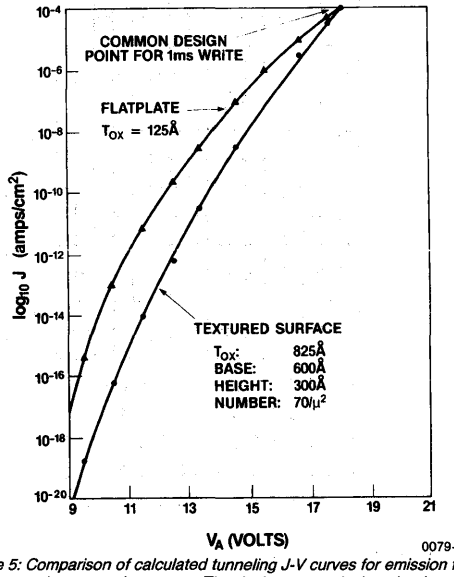


Figure 5: Comparison of calculated tunneling J-V curves for emission from a planar and a textured structure. The devices were designed to have the same emission in the high current regime where programming takes place.

These differences may become even more significant as devices are scaled. It is clear that, in order to scale the memory properly, lower programming voltages are needed so that the isolation widths and device channel lengths can be reduced both in the memory array and in the peripheral circuitry. However, for a typical part which stores data in 3 ms and must retain it for 10 years, the tunneling current under storage and reading conditions must be at least 10^{11} times smaller than under programming conditions because the retention time is 10^{11} times longer than the storage time. Actually, for margin, one would design for a difference in currents of 10^{13} to 10^{14}. For planar surface tunneling structures, this may be a difficult design constraint because the slope of the J-V curve is fixed, which means that the maximum allowed read voltage drops with the programming voltage on a volt-for-volt basis, not proportionately. On the other hand, textured surface tunneling structures, in their current manifestation, have a steeper J-V characteristic than planar ones and the J-V characteristic of a textured structure can be tailored to yield a steeper curve if desired. This means that for a given maximum read voltage, a textured structure requires a lower programming voltage which leads to better scaling.

To verify the excellent data retention expected of Xicor memories, a study was carried out to measure data loss as a function of temperature. Figure 6 shows log cumulative data loss vs. log time for 100 samples of X2210's at each of three temperatures. Data loss is defined as occurring when the first bit in the array loses data. As shown in Figure 6, high temperatures were required to obtain appreciable data loss in experimentally useful times. Note that even at 300°C, 2000 hours (~ 3 months) are required to see data loss. Figure 7 shows the result of calculating failure rates based on these results and plotting vs. inverse temperature. Since the rates fall on a straight line, we can extract an activation energy and extrapolate to lower temperatures. The result is that the experimental value of the activation energy is 1.7eV and the mean time for data loss for this mechanism (which we believe to be the fundamental loss mechanism of this technology) is 3 million years for retention at 125°C.

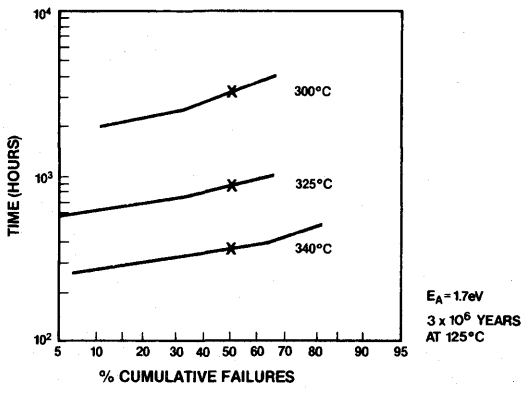


Figure 6: Log cumulative data loss vs. log time for three storage temperatures on samples of 100 X2210's. Data loss is defined to occur when the first bit in an array loses data.

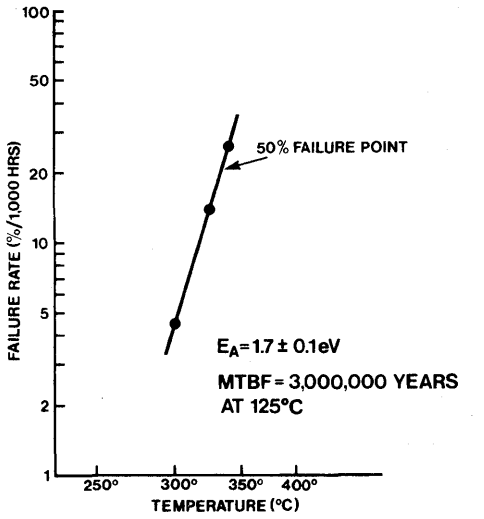


Figure 7: Log data loss rate vs. inverse temperature for X2210's.

Although this retention data was based on small NOVRAMs*, it applies equally to Xicor E²PROMs which share common floating gate storage mechanisms and processes with the NOVRAMs. In fact, the real cause for retention failures observed in E²PROMs is not the intrinsic mechanism reported above, but single bit data loss arising from the same oxide defects which have been observed in EPROMs and shown to have an activation energy of 0.6eV.[1]

In order to investigate the probability of occurrence of the extrinsic oxide defect data retention failures, a topological checkerboard pattern was written into samples of X2864A devices from a number of lots. These devices were stored at elevated temperatures with periodic readouts to verify to data integrity. The hermetic packaged devices were stored at 250°C while the tests on the plastic encapsulated devices were conducted at 150°C because

*NOVRAM is Xicor's nonvolatile static RAM device.

150°C

Package Type	Lot ID	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.	
PLCC	Q1	0	27	0	27	0	27	0	27	0	27	0	27
	Q2	0	28	0	28	0	28	0	28	0	28	0	28
PDIP	Q1	0	50	0	50	0	50	0	50	0	50	0	50
	Q2	0	50	0	50	0	50	0	50	0	50	0	50
	Q3	0	50	0	50	0	50	0	50	0	50	0	50
Totals		0	205	0	205	0	205	0	205	0	205	0	205

250°C

Package Type	Lot ID	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.	
Cerdip	Q1	0	50	0	50	0	50	0	50
	Q2	0	50	0	50	0	50	0	50
	Q3	0	50	0	50	0	50	0	50
	Q4	0	50	0	50	0	50	1[a]	50
	Q5	0	50	0	50	0	50	0	50
	Monitor	0	350	0	350	0	350	1[b]	350
Totals		0	600	0	600	0	600	2	600

[a] = Cracked die

[b] = Single bit retention failure: 0.6eV

Table I: Data retention bake.

the plastic epoxy molding compound won't survive 250°C storage. The data from this test are displayed in Table I. The results show very good data integrity. This is in line with a recent report which indicated that E²PROMs have a lower incidence of oxide defects than EPROMs.[2] This is probably because the multiple high voltage writes which occur during an E²PROM manufacturing flow provide an effective screen for many oxide defects which would otherwise appear as retention failures.

ENDURANCE

Endurance is defined as the ability of a nonvolatile memory to withstand repeated nonvolatile data changes while remaining within specification. As is discussed in more detail in Xicor reliability report RR-510, endurance in Xicor's E²PROMs is limited by two effects, electron trapping in the tunnel oxide and oxide breakdown. Electron trapping in the tunnel oxide is the major failure mechanism in the endurance range of more than ~ 10^5 data changes. Oxide breakdown tends to be the major failure mechanism for devices which have endurance of less than ~ 10^5 data changes.

Xicor uses two tests to evaluate the endurance of its E²PROMs. One test utilizes special test modes to enable all bits in a unit to be changed simultaneously. This test is used to measure the ultimate endurance of a sample of units. For reasons discussed in RR-510, this test tends to give a somewhat pessimistic estimate of trapping limited endurance and a slightly optimistic estimate of oxide breakdown limited endurance. Figure 8 shows an endurance distribution sample from a broad range of X2864A material. In order to accurately monitor the oxide defects, which appear as infant mortality endurance failures, Xicor conducts a test in which

each page is written to 10,000 times on a page-by-page basis. Figure 9 shows the distribution of failures found from a sample of 1034 units coming from at least 10 runs. As shown in RR-510 these failures are expected to contribute approximately 10 FIT to the failure rate in typical applications.

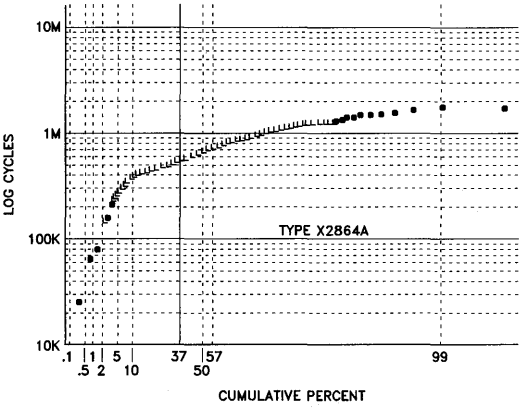


Figure 8: An extreme value distribution of endurance monitor on units cycled in mass mode.

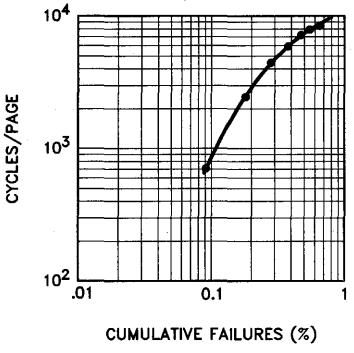


Figure 9: Cumulative failures occurring at less than 10K writes/page of complete memory for a sample of 1034 X2864A chosen from more than 10 diffusion lots.

LIFETESTS

In addition to the endurance and data retention tests specifically targeted at properties unique to nonvolatile memories, Xicor conducts the standard battery of product life and package integrity tests.

In order to accelerate device failure rate, Xicor runs high and low temperature dynamic lifetests and a high temperature reverse bias test. High temperature dynamic lifetest accelerates the vast majority of the failure mechanisms which might effect these products. The exceptional mechanism is hot electron trapping in the gate oxide for which the worst case is at low temperature. Test pattern studies show that hot electron trapping is not expected to be a problem in the X2864A technology which uses relatively conservative transistors of 3 microns gate length and 750Å gate oxide thickness in the periphery. To verify this prediction, units were operated dynamically for 1000 hours at −40°C. The data for this stress are exhibited in Table II and show no failures as expected.

The procedure that Xicor uses in dynamic lifetest is to load a topological checkerboard pattern into the units. The units are continuously read at temperature while the addresses are incremented in a binary sequence. At each readout the data integrity is first verified and then all parameters and functions (read and write) are verified across the specified voltage range. Finally the checkerboard pattern is reloaded and the units returned to the stress. The procedure in HTRB stress is similar except that during the stress all pins are biased high.

Package Type	Lot ID	500 Hrs.		1000 Hrs.	
		# Fail	# In	# Fail	# In
Cerdip	Q1, 2, 3	0	75	0	75
	Q4	0	25	0	25
	Q5	0	25	0	25
Totals		0	125	0	125

Table II: −40°C dynamic lifetest.

The data for these stresses are exhibited in Tables III and IV. In these tables the data are segregated by package type for each of the several types tested. This data was collected over the period June 1986 through March 1987.

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Package Type	Lot ID	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.	
		# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
PDIP	Q5	3[a]	102	0	99	—	—	—	—	—	—	—	—
	Q6	0	102	0	102	—	—	—	—	—	—	—	—
	Q7	0	102	0	102	—	—	—	—	—	—	—	—
	Monitor	0	3966	0	3962	0	640	1[b]	560	—	—	—	—
PLCC	Q3	0	500	0	446	—	—	—	—	—	—	—	—
	Q4	1[c]	912	0	843	—	—	—	—	—	—	—	—
Cerdip	Q1,2,3	1[d]	4997	0	4997	0	300	0	300	0	294	0	294
	Q4	0	874	0	874	0	100	0	95	0	95	0	94
	Q5	0	1282	0	1280	0	100	1[a]	97	0	97	0	95
	Monitor	0	1498	1[a]	1492	2[a]	240	0	238	—	—	—	—
Totals		5	14335	1	14197	2	1380	2	1290	0	486	0	483

[a] = Ionic contamination 1.0eV
[b] = Data retention 0.6eV
[c] = Marginal V_{IN}
[d] = Cracked die

Table III: 125°C dynamic lifetest.

Package Type	Lot ID	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.	
		# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
PLCC	Q3	0	52	1[a]	52	—	—	—	—
PDIP	Q1	—	—	—	—	4[a]	25	0	21
	Q2	—	—	—	—	0	25	0	24
	Q3	—	—	—	—	0	25	0	24
Cerdip	Q1	—	—	—	—	0	45	0	45
	Q2	—	—	—	—	0	45	0	45
	Q3	—	—	—	—	0	45	0	45
	Q4	—	—	—	—	0	45	1[a]	45
	Q5	—	—	—	—	1[a]	45	0	44
Totals		0	52	1	52	5	300	1	293

[a] = Ionic contamination 1.0eV

Table IV: 150°C static lifetest.

PACKAGE INTEGRITY TESTING

The tests Xicor employs to ascertain the integrity of the packages differ between hermetic and plastic encapsulated devices. For hermetic devices Xicor follows the tests specified in MIL-STD-883C, Method 5005 for group C & D evaluation of packaged devices. Tables V and VI contain the results for Cerdip and LCC packages, respectively.

For plastic encapsulated devices the military standard tests are not really applicable. Instead Xicor uses autoclave and 85/85 stresses to test for corrosion effects in the non-hermetic plastic packages. Xicor also makes extensive use of temperature cycling to test for die cracking or lead shear which might arise as a result of the mismatch of thermal expansion coefficients which exists between the epoxy molding compound and the silicon die. The autoclave tests are conducted by storing units in steam at 2 atmospheres (15 PSIG) and 121°C. The 85/85 tests are conducted with all inputs and outputs biased at 5V. These are conducted both with V_{CC} powered and unpowered since there is some uncertainty as to which case is worst. The temperature cycling is done between −65°C and +150°C in compliance with MIL-STD-883C, method 1010, condition C. The results are exhibited in Tables VII, VIII, and IX and show very good results.

Test	Method	Conditions	LTPD	Accept #	Results
Temperature Cycling	1005	Test Condition C (10 cycles, −65°C to +125°C)	15	0/15	0/120
Constant Acceleration	2001	Test Condition E (30,000 y, Y1 axis only)			0/120
Seal	1014	Test Condition B			1/120
—Fine		(5×10^{-7} cc/min)			
—Gross		Test Condition C			0/119
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15	0/15	0/60
Seal	1014				
—Fine		Test Condition B			0/60
—Gross		Test Condition C			1/60
Thermal Shock	1011	Test Condition B (15 cycles, −55°C to +125°C)	15	0/15	0/172
Temperature Cycling	1010	Test Condition C (100 cycles)			0/172
Moisture Resistance	1004				0/172
Seal	1014				
—Fine		Test Condition B			1/171
—Gross		Test Condition C			0/171
Internal Water Vapor Content	1018	5,000 ppm Maximum Water Content at 100°C	—	0/3 or 1/5	0/12
Mechanical Shock	2002	Test Condition B (1500 g peak, 3 axis)	15	0/15	0/197
Vibration Variable Frequency	2007	Test Condition A (20g peak, 3 axis)		0/15	0/197
Constant Acceleration	2001	Test Condition E		0/15	0/197
Seal	1014				
—Fine		Test Condition B		0/15	4/197
—Gross		Test Condition C		0/15	2/193
Salt Atmosphere	1009	Test Condition A	15	0/15	0/102
Seal	1014				
—Fine		Test Condition B			0/102
—Gross		Test Condition C			0/102
Adhesion of Lead Finish	2025		15	0/15 (# of leads from 3 devices)	0/45
Lid Torque	2024				0/15

Table V: Environmental test for 28-lead cerdip package.

Test	Method	Conditions	LTPD	Accept #	Results
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15	1/15	0/45
Seal	1014				
—Fine		Test Condition B			0/45
—Gross		Test Condition C			0/45
Thermal Shock	1011	Test Condition B (15 cycles, −55°C to +125°C)	15	1/15	0/120
Temperature Cycling	1010	Test Condition C (100 cycles)			0/120
Moisture Resistance	1004				0/120
Seal	1014				
—Fine		Test Condition B			0/120
—Gross		Test Condition C			0/120
Internal Water Vapor Content	1018	5,000 ppm Maximum Water Content at 100°C	—	0/3 or 1/5	0/9
Mechanical Shock	2002	Test Condition B (1500 g peak, 3 axis)	15	0/15	0/120
Vibration Variable Frequency	2007	Test Condition A (20g peak, 3 axis)			0/120
Constant Acceleration	2001	Test Condition E			0/120
Seal	1014				
—Fine		Test Condition B			0/120
—Gross		Test Condition C			0/120
Salt Atmosphere	1009	Test Condition A	15	0/15	0/83
Seal	1014				
—Fine		Test Condition B			0/83
—Gross		Test Condition C			0/83

Table VI: Environmental test for 32-pad LCC package.

	48 Hrs.		96 Hrs.		192 Hrs.		288 Hrs.		384 Hrs.		521 Hrs.	
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
Monitor	0	1577	0	1577	—	—	—	—	—	—	—	—
Q1	0	80	0	80	0	80	0	78	0	78	0	78
Q2	0	80	0	80	0	80	0	80	0	79	0	79

Table VII: Autoclave.

	V_{CC} = 5.5V				V_{CC} = 0V			
	500 Hrs.		1000 Hrs.		500 Hrs.		1000 Hrs.	
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
Q1	0	99	0	99	0	98	0	95
Q2	0	99	0	97	0	99	0	99
Q3	0	99	0	99	0	99	0	99
Q4	0	99	0	99	0	98	0	98
Q5	0	90	0	90	0	90	—	—
Q5	0	110	0	110	0	111	0	110

Table VIII: 85/85.

Package Type	Lot ID	200 Cycles		500 Cycles		1000 Cycles	
		# Fail	# In	# Fail	# In	# Fail	# In
PDIP	Q1	0	80	0	78	1	78
	Q2	0	80	0	80	0	80
	Q3	0	78	0	78	0	78
	Q4	0	78	0	77	0	77
	Q5	0	78	0	78	0	78
	Monitor	0	623	0	623	—	—
Totals		0	1017	0	1014	1	391

Table IX: Temperature cycle.

FAILURE RATE PREDICTION

It has been long observed that failure rates follow a bathtub shaped curve. There is an infant mortality region characterized by a rapidly declining failure rate as "weak" parts are eliminated from the populations, a random failure region characterized by an invariant or slowly declining failure rate, and a wear-out region characterized by an increasing failure rate as the units reach end-of-life. Xicor, and most other conscientious manufacturers, designs processes so that end intrinsic wearout failures are never seen over the normal life of the part and develops manufacturing flows to minimize the number of weak parts which are produced.

The classic parameter used to accelerate failure rates is temperature. It is known that a very broad class of failure mechanisms have a temperature dependence proportional to $\exp(-E_a/kT)$ where E_a is called the activation energy, k is Boltzmann's constant, and T is the absolute temperature. This is true because a number of basic physical phenomena such as diffusion rates and chemical reaction rates have this dependence. If the activation energy is known for the failure mechanisms in question, then the failure rates arising from these mechanisms can be measured at elevated temperature and extrapolated back to lower operating temperatures. The relationship which allows one to translate failure rates from one temperature to another is known as the Arrhenius relation. Figure 10 illustrates this relation for a number of common values of activation energy.

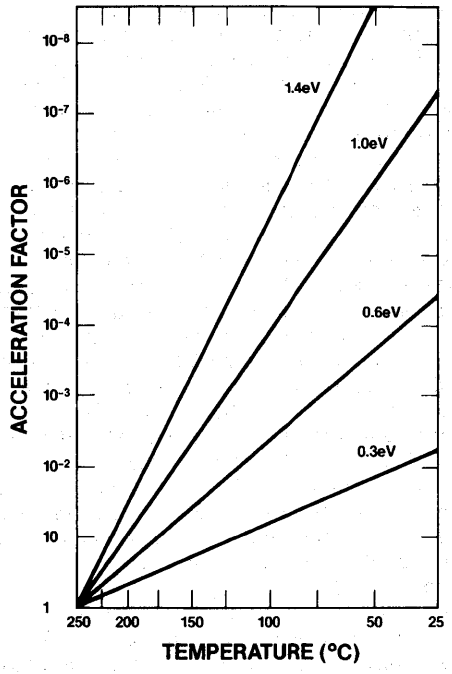

Figure 10: Acceleration factor vs. temperature calculated for various activation energies from Arrhenius relation.

There is no simple, one-step formula for inferring a predicted failure rate from the experimental data. Instead, the failures of each individual activation energy must be treated differently. The first step is to calculate the equivalent device hours at the ambient

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Activation Energy	Device Hr. at 125°C	Equivalent Hr. at 55°C	Equivalent Hr. at 70°C	Failures	Failure Rates (FIT)			
					60% UCL 55°C	60% UCL 70°C	Best Est 55°C	Best Est 70°C
0.3eV	5.097×10^6	2.504×10^7	1.716×10^7	0	36	54	28	41
0.6eV	5.097×10^6	1.242×10^8	5.806×10^7	1	16	34	13	29
1.0eV	5.097×10^6	1.068×10^9	2.971×10^8	4	5	17	4	15
Totals					57	105	45	85

Table X: Failure rate calculation.

temperature of interest, utilizing the Arrhenius relationship discussed earlier. This calculation should be carried out for every mechanism observed or expected. For example, the calculation for the 0.3eV activation energy oxide rupture mechanism should be carried out whether this failure mechanism is observed or not, since this mechanism is always anticipated in MOS integrated circuits. The extrapolation should be carried out utilizing the junction temperature at the ambient temperature of interest and not the ambient temperature itself. The upper confidence limit is then calculated for the failure rate for each activation energy. The upper confidence limits for the various activation energies are then summed for a total failure rate prediction. The meaning of the "upper confidence level" is that with a certainty, or probability, of a certain level we can say that the true value is less than the stated value. Thus, the confidence level rate calculated is non-zero even for the case where no failures are observed because we can't be sure that there will be none. This procedure is discussed in more detail in RR-506.

The infant mortality failure fraction is calculated from the 48 hour, 125°C burn-in data. This corresponds to the failure expected in the first several weeks of operating life. The data shows that 5 units failed out of 14,335 units tested for an infant failure fraction of 0.03% or 349 ppm.

The long term (random)—failure rate is estimated from the 125°C dynamic lifetest data in Table X. These calculations sum the data from all package types tested. The results show the predicted failure rate at 55°C 60% UCL to be 50 FIT (or 0.0050%/1000 Hr). One FIT is one failure in 10^9 hours. Even though these calculations are based on over 5 million device-hours at 125°C, the failure rate is still dominated by the gate oxide failure mechanism which was not observed. If this mechanism were to be excluded, the predicted failure rate would drop approximately in half.

SUMMARY

In this paper, the physical operation of Xicor E²PROMs is discussed in some detail. Data on data retention and endurance of the X2864A are presented which show that they are expected to contribute about 1 FIT and 10 FIT, respectively, to the device failure rate. Data based on dynamic lifetest is used to estimate the operating failure rate. The best estimate of the long term failure rate based on this data is 39 FIT at 55°C. The infant mortality failure fraction based on 48 hour, 125°C dynamic burn-in is 349 ppm. Data is also presented on the package integrity of this device in Cerdip, LCC, PDIP, and PLCC. The data shows the Xicor X2864A to be a very reliable device.

REFERENCES

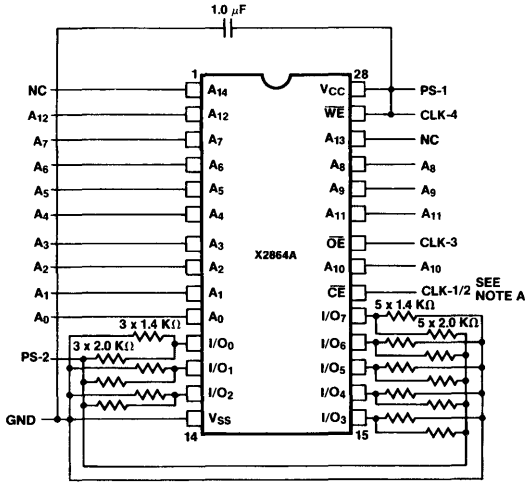
1. R.E. Shiner, et al, Proc. 18th Reliability Physics Symposium, pp. 238–243 (1980).
2. N. Mielke, A. Fazio and H. Liou, Proc. 25th Reliability Physics Symposium (1987).

This report is based on data collected through March 1987.

APPENDIX A

Product	Package Type					
	Plastic		Cerdip		LCC	
	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}
X2864A	39.5	64.3	16.5	35	5.0	46.0

Thermal Resistance Table: θ_{JC} and θ_{JA} expressed in °C per watt.



0079-12

Note A:

CLK-1: Rows 1, 3, 5 . . . (odd rows—$\overline{CE}_A$)
CLK-2: Rows 2, 4, 6 . . . (even rows—$\overline{CE}_B$)
Such that: CLK-2 = $\overline{CLK\text{-}1}$

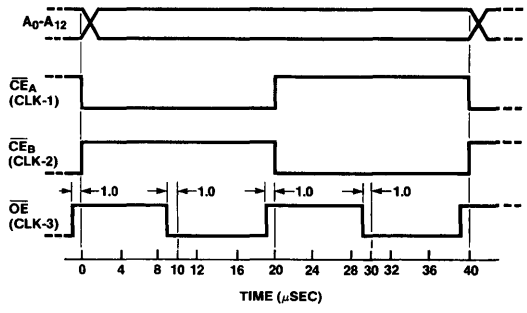
Note B: (1) $\overline{WE}$ must always be hardwired to V_{CC} (Pin 28) at device as shown.

(2) All resistors:
1% metal film
1/4 W

(3) I/O pull-up 2.00 KΩ
I/O pull down: 1.40 KΩ

(4) Socket-to-socket isolation as shown.

X2864A (DIP) Burn-in circuit.



0079-13

Notes: (1) A_0–A_{12}: binary sequencing address cycle: 40 μs.
(2) $\overline{WE}$ disabled (tied to V_{CC} at device).
(3) V_{IN} Low: 0.4V V_{IN} High: 5.0V
(4) V_{CC}: 5.50V

X2864A (DIP) Burn-in timing diagram.

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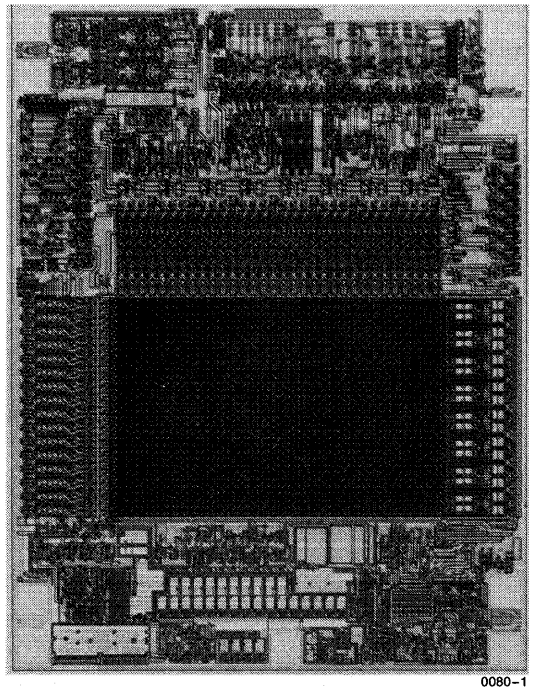
NOTES



0080-1

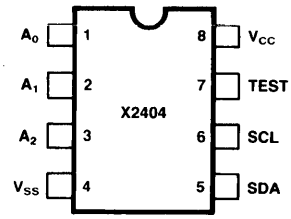
X2404 RELIABILITY REPORT

By Julie Segal

9

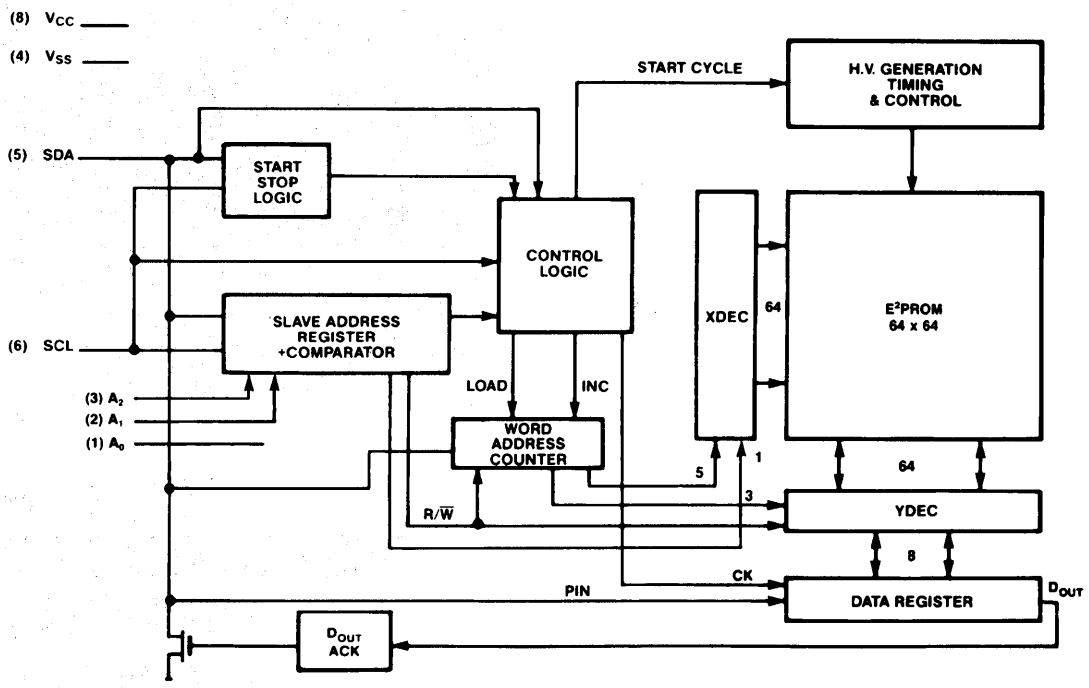
INTRODUCTION

The X2404 is a 4096 bit serial E²PROM organized as two 256 x 8 bit pages. This memory operates on a single 5V power supply for all operations. Figure 1 provides the pin configuration; Figure 2 shows the functional block diagram; Figure 3 illustrates the physical location of the various address bits. The thermal resistance table, burn-in circuit and a timing diagram are included in Appendix A for your reference.



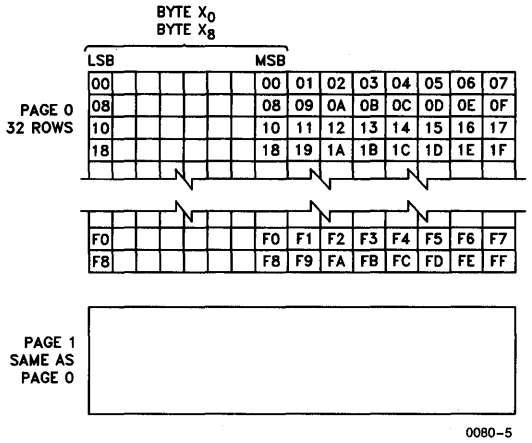
0080-3

Figure 1: X2404 Pin configuration.



0080-4

Figure 2: X2404 Functional block diagram.



Each square equals one byte.

Figure 3: X2404 Physical bit map.

Xicor is an experienced producer of E²PROMs with over fourteen million devices in the field. This and previous experience with the development of NOVRAMs has given Xicor a leading position in nonvolatile memory technology.

TECHNOLOGY

The X2404 is fabricated in a triple polysilicon N-channel floating gate MOS technology. Data is stored as the presence of positive or negative charge on the second level polysilicon which acts as a gate of a memory transistor. This floating gate is surrounded by ~ 750Å of thermally grown oxide, one of the best electrical insulators known. Charge is transferred to and from the floating gate through a quantum mechanical effect known as Fowler-Nordheim tunneling. This phenomenon has been described in detail in recent publications.[1,2,3]

RELIABILITY STUDY AND RESULTS

The reliability studies and results presented here are those of the X2404 in a plastic package.

Before Xicor qualifies any new product it is subjected to a series of accelerated stresses and tests. These tests are designed to accelerate any degradation a device may experience over the course of a normal lifetime so as to uncover any design or process flaws.

In addition, Xicor runs ongoing monitors of those products in production. This assures high reliability standards for all product shipped by Xicor.

The stresses used to establish reliability data are as follows:

1) High temperature dynamic lifetest.
2) Data retention bake.
3) High temperature high voltage stress.
4) Environmental testing.

A short description of these tests and the results obtained are presented in the following report.

Dynamic Lifetest

Most failure modes encountered in MOS devices are accelerated if the device is operated at elevated temperatures. Thus the dynamic lifetest aims to accelerate any failure modes a device may exhibit by operating the device in its most common mode at high temperature.

For the X2404, the dynamic lifetest consisted of continually reading the devices at a temperature of 125°C. A known pattern was stored in the devices prior to the beginning of the test. Each unit was tested for data retention and complete functionality after 48, 168, 500, 1000, 1500 and 2000 hours of dynamic lifetest.

The results of the dynamic lifetest are shown in Table I for samples pulled from five lots of plastic devices. As indicated in the table, all samples were subjected to 168 hours of burn-in. One hundred units from each sample lot were then put on continuing test, with the results as shown.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Totai Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
A	0	880	0	880	0	100	0	100	0	100	0	100	3.3×10^5
B	1[a]	1000	0	999	0	100	0	100	0	100	0	100	3.5×10^5
C	2[a] [b]	999	1[a]	997	1[a]	100	0	97	0	97	0	97	3.5×10^5
D	0	999	0	999	0	100	0	100	0	100	0	100	3.5×10^5
E	0	998	0	997	0	100	0	100	0	100	0	100	3.5×10^5
Totals	3	4876	1	4872	1	500	0	497	0	497	0	497	1.7×10^6

[a] Oxide breakdown

[b] Metallization defect

Table I: Dynamic lifetest @ 125°C, test results.

Data Retention

The purpose of this stress is to measure and ensure a device's ability to retain data. This test is run at elevated temperatures because floating gate structures will have a greater tendency to lose charge (data change) at higher temperatures. Because the X2404 cell is similar to that of the X2864A, we expect similiar excellent data retention. Refer to Xicor publication, *X2864A Reliability Report,* RR-507A.[4]

High Temperature High Voltage Stress

The high temperature high voltage stress test is a derivative of the high temperature reverse bias tests used to evaluate bipolar circuits. In this test V_{SS} is grounded while all inputs and V_{CC} are maintained at high voltage while being baked. The stress is intended to expose failures due to mobile ionic contaminants, electrical overstress and latent gate oxide defects. The temperature for this test is 150°C with the bias voltage set at +5.5V. Data retention and functionality were verified after 500, 1000, 1500, and 2000 hours. The results of the tests are listed in Table II.

Lot #	500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
A	0	50	0	50	0	50	0	50	1×10^5
B	0	50	0	50	0	50	0	50	1×10^5
C	0	50	0	50	0	50	0	50	1×10^5
D	0	50	0	50	0	50	0	50	1×10^5
E	0	50	0	50	0	50	0	50	1×10^5
Totals	0	250	0	250	0	250	0	250	5×10^5

Table II: 150°C High temperature high voltage test results.

ENVIRONMENTAL TESTING

Environmental tests are designed to determine a device's resistance to extreme or changing environments. Presented here is the reliability data on plastic packaged devices.

Due to the considerable difference in expansion coefficients between plastic and silicon, plastic devices can be susceptible to temperature cycling damage. Therefore, plastic units were subjected to a more stringent test for this condition than that required for MIL-STD-883B group D testing. Table III illustrates the test results of units that had been subjected to one thousand temperature cycles as defined by MIL-STD-883 test condition C (i.e., −65°C to +150°C).

Lot #	168 Cycles		500 Cycles		1000 Cycles	
	# Fail	# In	# Fail	# In	# Fail	# In
A	0	100	0	100	0	100
B	0	100	0	100	0	100
C	0	100	0	100	0	100
D	0	100	0	100	0	100
E	0	100	0	100	0	100
Totals	0	500	0	500	0	500

Table III: Temperature cycling test results.

85°C and 85% Relative Humidity and Autoclave Tests

In addition, plastic encapsulated devices may be susceptible to moisture. For this reason five sample lots of plastic units were stressed at 85°C with 85% relative humidity (both powered and unpowered) and five additional sample lots were subjected to autoclave tests (pressure pot) at two atmospheres. These stresses test for corrosion, electrolytic failure modes and passivation integrity. The results of these tests are presented in Tables IV and V.

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	
A	0	50	0	50	0	49	4.5×10^4
B	0	50	0	50	0	50	5.0×10^4
C	0	50	1[c]	50	0	49	4.5×10^4
D	0	50	0	50	0	50	5.0×10^4
E	0	50	0	50	0	50	5.0×10^4
Totals	0	250	1	250	0	248	2.4×10^5

[c] Leaky oxide

Table IVA: 85/85 Test results with V_{CC} = +5.0V.

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	
A	0	50	0	50	0	50	5.0×10^4
B	0	50	0	50	0	50	5.0×10^4
C	0	50	0	50	0	50	5.0×10^4
D	0	50	0	50	0	50	5.0×10^4
E	0	50	0	50	0	50	5.0×10^4
Totals	0	250	0	250	0	250	2.5×10^5

Table IVB: 85/85 Test results with V_{CC} = 0V.

NOTE: In both 85/85 tests, each pin was alternately biased to +5V and 0V to provide an electrical potential between adjacent metal lines on the die.

Lot #	48 Hrs.		144 Hrs.		240 Hrs.		336 Hrs.		432 Hrs.		528 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
A	0	100	0	100	0	100	0	100	0	100	0	100	5.3×10^4
B	0	100	0	100	0	100	1[c]	100	0	99	0	99	5.3×10^4
C	0	100	0	100	0	100	0	99	0	99	0	99	5.3×10^4
D	0	100	0	100	0	100	0	100	0	100	0	100	5.3×10^4
E	0	100	1[c]	100	0	99	0	99	0	99	0	99	5.2×10^4
Totals	0	500	1	500	0	499	1	498	0	497	0	497	2.6×10^5

[c] Leaky oxide

Table V: Autoclave test results.

PREDICTION OF FAILURE RATES

As mentioned previously, accelerated testing allows one to identify possible design and process flaws. It also makes it possible to predict long term failure rates under normal operating conditions.*

All failure mechanisms are accelerated to some degree by voltage or temperature or both. The degree to which any given failure mode is accelerated is known as the activation energy or simply as the acceleration factor. Thus knowledge of a failure mode's activation energy allows one to predict the long term failure rate for that failure mode under normal operating conditions. If the activation energy is not known it can be determined experimentally. Four typical failure mechanisms of the technology employed by Xicor and their corresponding activation energies are:

Oxide breakdown	0.3eV
Electromigration	0.55eV
Leaky oxides	0.6eV
Ionic contamination	1.0eV

Table VI contains the predicted long term failure rates for these activation energies. The results are based on the dynamic lifetest and HTRB data presented in the previous sections.

Activation Energy	Number of Failures	Equivalent Hours at 55°C	60% UCL Failure Rate Per 1000 Hrs. at 55°C	
0.3eV	2	1.5×10^7	0.0210	
0.55eV	0	8.6×10^7	0.0015	
0.6eV	0	1.2×10^8	0.0008	
1.0eV	0	2.2×10^9	0.0000	
			0.0233	**Total**

Table VI: Predicted long term failure rates.

***NOTE:** The infant mortality failure rate, based on 3 failures out of 4867 units tested after the first 48 hours of burn-in at 125°C is 0.06%. 48 hours of 125°C burn-in is equivalent to a few hundred to approximately 1000 hours of system operating time, depending on failure mode and system operating temperature.

The failure rates predicted are for plastic devices. The predicted failure rate in percent is depicted as the "60% upper confidence level failure rate per 1000 device hours." This means that there is a 60% probability that the actual failure rate will be below the rate calculated. Sometimes predictions are expressed in FIT units. To convert from the given values to FITs, simply multiply the failure rate per 1000 hours operation by 10,000.

A more representative value for the failure rate can be given by the best estimate. This value gives the most likely failure rate based on the given data as shown in Table VII.

Activation Energy	Number of Failures	Equivalent Hours at 55°C	B.E. Failure Rate Per 1000 Hrs. at 55°C	
0.3eV	2	1.5×10^7	0.0158	
0.55eV	0	8.6×10^7	0.0008	
0.6eV	0	1.2×10^8	0.0006	
1.0eV	0	2.2×10^9	0.0000	
			0.0172	**Total**

Table VII: Best estimate long term failure rates.

Based on these values it can be seen that the expected long term failure rate for the X2404 is 0.0172% per 1000 hours at 55°C.

ENDURANCE

Endurance of the X2404 is generally limited to electron trapping in the tunnel oxide. Figure 4 shows the extreme value distribution observed for endurance on this part as measured by simultaneously changing all bits from a "1" state to its complement and back.

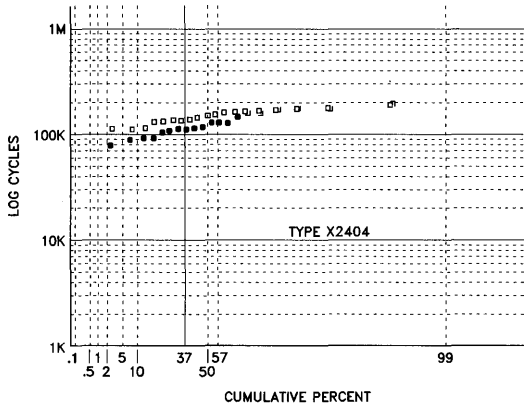


Figure 4: An extreme value distribution of endurance monitor on units cycled in mass mode.

SUMMARY

The technology used in producing the X2404 was reviewed. A comprehensive set of data covering a variety of stresses were presented and described. Finally, failure predictions were provided.

REFERENCES

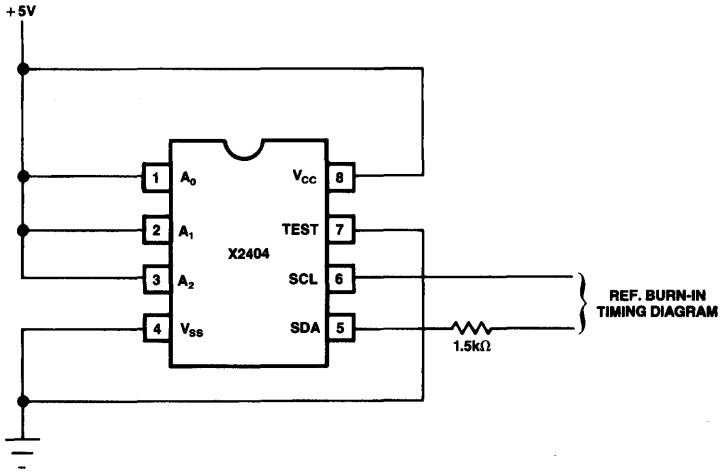
1. R.K. Ellis, *IEEE Electron Device Letters* 13 (1982): 330–333.
2. R.K. Ellis, H.A.R. Wegener and J. Caywood, *International Electron Devices Meeting Technical Digest* (1982): 749–752.
3. J. Caywood and Reliability Engineering Staff, *NOVRAM Reliability Report,* Xicor publication RR-502A (1985).
4. T. Kaysser and L. Purvis, *X2864A Reliability Report,* Xicor publication RR-507A (1987).

This report is based on data collected through May, 1986.

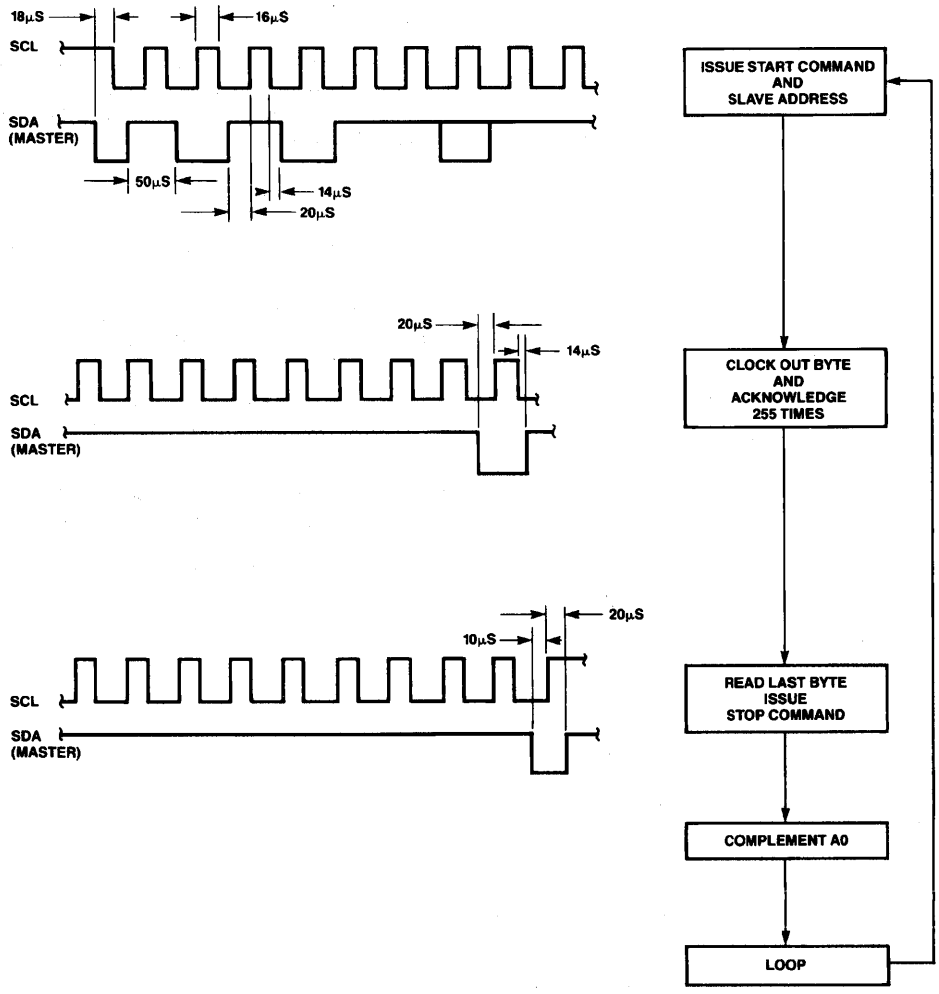
APPENDIX A

Product	Package Type: Plastic	
	θ_{JC}	θ_{JA}
X2404	43.0	84.0

Thermal Resistance Table: θ_{JC} and θ_{JA} expressed in °C per watt.



X2404 Burn-in circuit.



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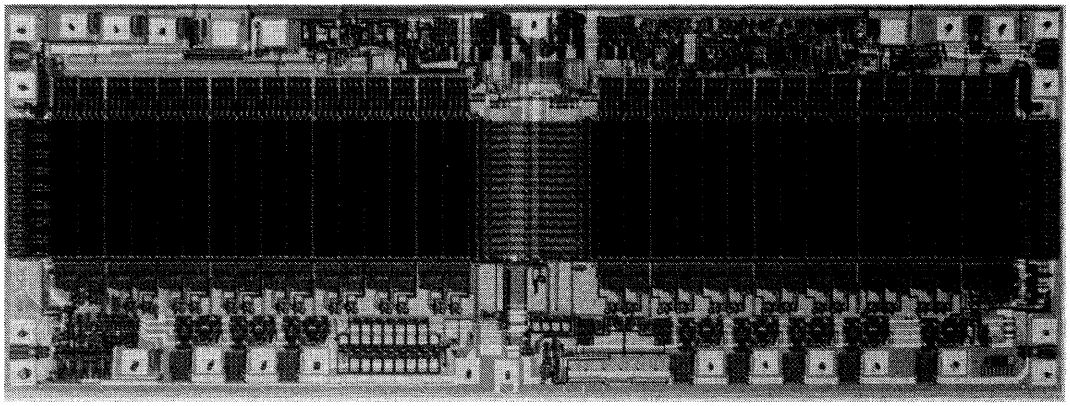
X2404 Burn-in timing diagram and program flow.



0081-1

X2816B RELIABILITY REPORT

By Steven K. Fong

9

INTRODUCTION

The X2816B is a 16K bit electrically erasable programmable read only memory (E²PROM) organized 2K x 8. It is an enhancement of the X2816A which incorporates $\overline{\text{DATA}}$ Polling and 16 byte page mode writing to decrease the write time needed to write data into the whole part, and it operates on a single 5V power supply for all operations. It utilizes the same proven thick oxide, textured poly technology as other Xicor nonvolatile memory products. Further information about the memory cell and tunneling physics may be found in references 1–4. Figure 1 provides the pin configuration; Figure 2 shows the functional block diagram; Figure 3 illustrates the physical location of the various address bits. The thermal resistance table, burn-in circuit and a timing diagram are included in Appendix A for your reference.

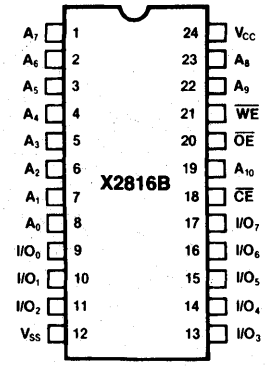


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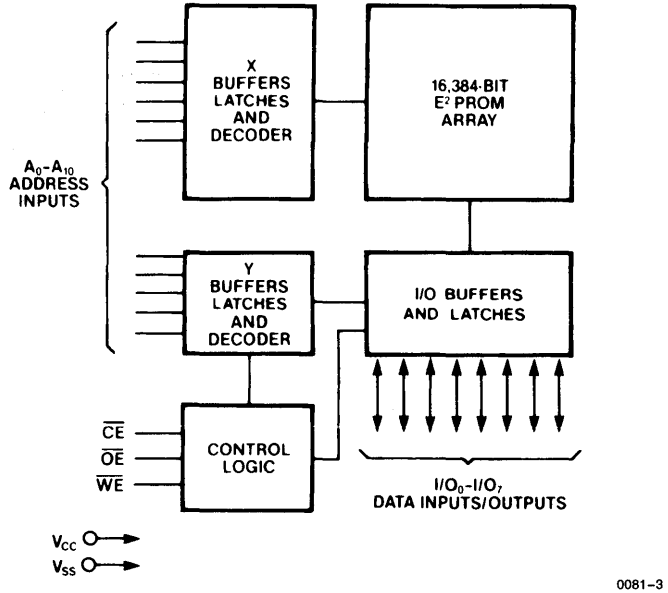
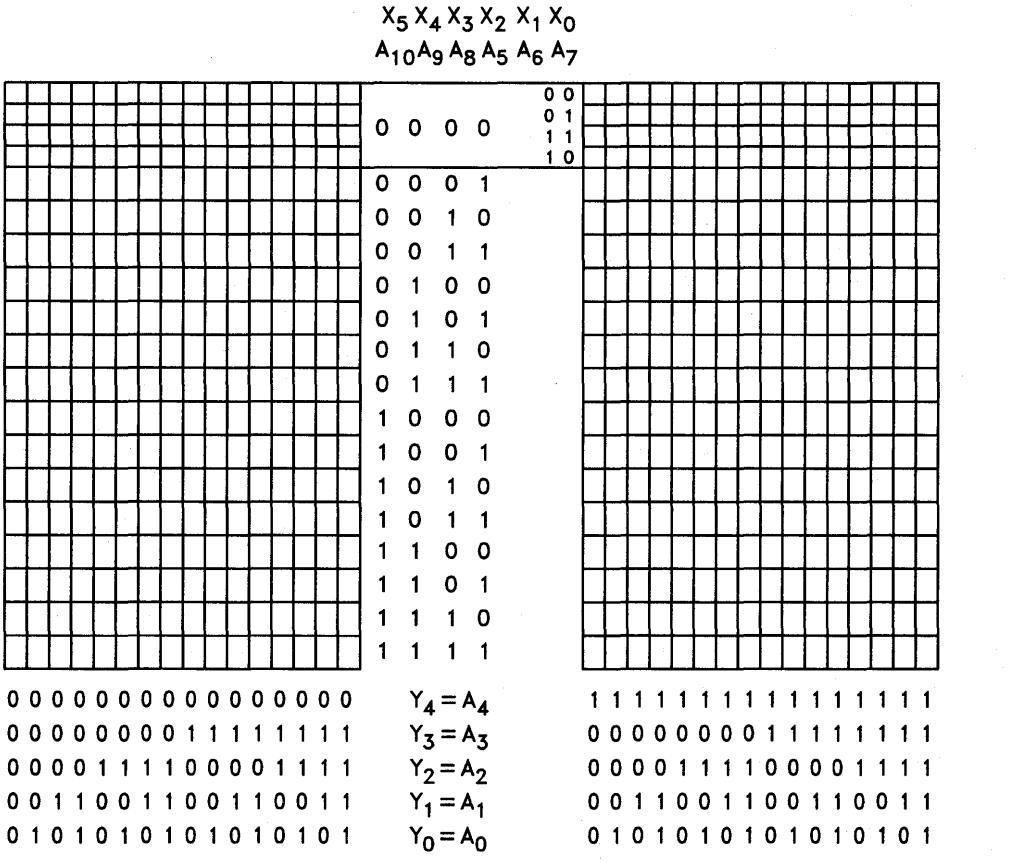
Figure 1: X2816B pin configuration.



0081-3

Figure 2: Functional block diagram.



Each square equals one byte.

Figure 3: X2816B bit map.

RELIABILITY STUDY AND RESULTS

Before Xicor qualifies any new product, it is subjected to a series of accelerated stresses and tests. These tests are designed to accelerate any degradation a device may experience over the course of a normal lifetime in order to uncover any design or process flaws. Because package type has an effect on device reliability, complete qualification of the X2816B involved both plastic and cerdip units. Since this device is very similar to the Xicor X2864A in design and technology, the reliability data found in the reliability report for X2864A (RR-507A) may be used to extend the results reported here.

In addition, Xicor runs ongoing monitors of those products in production. This assures high reliability standards for all product shipped by Xicor.

The stresses used to establish reliability data are as follows:

1) High temperature dynamic lifetest.
2) Data retention bake.
3) High temperature high voltage stress.
4) Environmental testing.
5) Endurance.

A short description of these tests and the results contained are presented in this report.

Dynamic Lifetest

Most failure modes encountered in MOS devices can be accelerated if the device is operated at an elevated temperature. Thus, the dynamic lifetest aims to accelerate any failure mode a device may exhibit by operating the device in its most common mode at high temperature.

For the X2816B, the dynamic lifetest consists of continually reading a known data pattern stored in the device while it is subjected to a temperature of 125°C. Each unit was then tested for data retention and complete functionality after 168, 500, 1000, 1500 and 2000 hours of dynamic lifetest. The result of the test is shown in Table I (no failures were found).

Data Retention

The purpose of this stress is to measure and ensure a device's ability to retain correct data. Floating gate structures are more likely to lose charge at high temperatures. For example, 48 hours at 250°C or 1000 hours at 150°C are equivalent to about 15 years at 55°C for an activation energy of 0.6eV. This is the energy for oxide defects which demonstrate floating gate memory data retention failures.

This test is conducted by storing a checkerboard pattern in the devices and baking the device at 150°C for plastic devices and 250°C for cerdip devices. The pattern is verified after 48, 168, 500, 1000, 1500 and 2000 hours. The results of this test are listed in Table II (no failures were found).

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 P	0	360	0	100	0	100	0	99	0	99	2.426×10^5
2 C	0	360	0	100	0	99	0	98	0	95	2.397×10^5
3 C	0	360	0	100	0	100	0	100	0	100	2.435×10^5
4 C	0	280	0	0	0	0	0	0	0	0	4.704×10^4
Totals	0	1360	0	300	0	299	0	297	0	294	7.729×10^5

Note: C = Cerdip
P = Plastic

Table I: Dynamic lifetest at 125°C test results.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 P	0	20	0	20	0	20	0	20	0	19	0	19	3.9×10^4
1 C	0	30	0	30	0	30	0	30	0	30	0	30	6×10^4
2 C	0	50	0	50	0	50	0	50	0	50	0	50	1×10^4
3 C	0	50	0	50	0	50	0	50	0	50	0	50	1×10^4
Totals	0	150	0	150	0	150	0	150	0	149	0	149	1.19×10^5

Note: C = Cerdip
P = Plastic

Table II: Retention bake test results, 250°C for cerdip devices and 150°C for plastic devices.

Lot #	500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
1 P	0	10	0	10	0	10	0	7	1.85×10^4
1 C	0	35	0	35	0	35	0	35	7×10^4
2 P	0	7	0	7	0	7	0	7	1.4×10^4
2 C	0	38	0	38	0	38	0	38	7.6×10^4
3 C	0	45	0	45	0	45	0	45	9×10^4
Totals	0	135	0	135	0	135	0	132	2.68×10^5

Note: C = Cerdip
P = Plastic

Table III: 150°C high temperature high voltage test result.

High Temperature High Voltage Stress

The high temperature high voltage stress is intended to expose failures due to mobile ionic contaminants, electrical overstress and latent gate oxide defects. In this test, V_{SS} is grounded while all inputs and V_{CC} are maintained at high voltage.

The temperature for this test is 150°C with the bias voltage set at +5.5V. Data retention and complete functionality were verified after 500, 1000, 1500 and 2000 hours. The result of the test is listed in Table III (no failures were found).

Environmental Testing

Environmental testing is designed to determine a device's resistance to extreme or changing environment. Due to the inherent differences between plastic and cerdip devices, different reliability stresses are applied to evaluate the individual package types.

Some of the tests used to evaluate cerdip packages, such as hermeticity, internal water vapor content, and lid torque, do not apply because the plastic packages are not hermetically sealed. (For reliability data on the 24-pin cerdip package, see the X2816A/X2804A Reliability Report RR-505).

Other tests, such as vibration and acceleration, do not apply because the die in a plastic package is completely embedded in plastic and is not susceptible to such mechanical failure. Plastic packages may be susceptible to other failure modes. Due to the considerable difference in expansion coefficients between plastic and silicon, plastic devices are considerably more susceptible to temperature failures. Table IV shows the result of units subjected to one thousand temperature cycles as defined by MIL-STD-883 test condition C.

Lot #	250 Cycles		500 Cycles		1000 Cycles	
	# Fail	# In	# Fail	# In	# Fail	# In
1 P	0	78	0	78	0	78
2 P	0	78	0	78	0	78
3 C	0	78	0	78	0	77
Totals	0	234	0	234	0	233

Note: C = Cerdip
P = Plastic

Table IV: Temperature cycling test results.

Prediction of Failure Rates

Accelerated testing identifies possible design and process flaws. It also predicts failure rates under normal operating conditions. Most failure mechanisms in this report are accelerated by voltage, temperature or both. The degree to which any given failure mode is accelerated may be predicted by activation energy. If the activation energy is not known, it can be determined experimentally. Four typical failure mechanisms of Xicor technology and their corresponding activation energies are:

1) Oxide Breakdown	0.3eV
2) Electromigration	0.55eV
3) Leakage Oxide	0.6eV
4) Ionic Contamination	1.0eV

Table V presents the predicted failure rates for these activation energies. The results are based on the test data presented in Tables I and III.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate per 1000 Hours at 55°C
0.3eV	0	4.495×10^6	0.0205	6.986×10^6	0.0132
0.55eV	0	1.626×10^7	0.0056	3.659×10^7	0.0025
0.6eV	0	2.206×10^7	0.0042	5.130×10^7	0.0018
1.0eV	0	1.914×10^8	0.0005	8.184×10^8	0.0001
Totals	0		0.0308		0.0176

Table V: 60% UCL failure rate predictions.

The failure rate predictions presented here are for both plastic and cerdip devices. Such predictions are valid because all the failure modes found or expected are common for both plastic and cerdip devices. Xicor has defined failure rate as the "60% upper confidence level" failure rate per 1000 device hours. This means that there is a 60% probability the actual failure rate will be below the rate computed. Sometimes predictions are expressed in FIT units. To convert from the previously named value to FIT, multiply by 10,000. For a more detailed discussion on confidence limits and reliability failure rate calculations, see Xicor Reliability Report RR-506.

A more representative value for the failure rate can be given by the "best estimate". This value gives the most likely failure rate based on the given data. Table VI presents the best estimate values.

Table VI shows that the expected failure rate for the X2816B is 0.0229% per 1000 hours at 70°C which is 229.0 FIT and 0.0134% per 1000 hours at 55°C which is 134 FIT. Since no failure was observed in any of the accelerated lifetests, the failure rate calculated above should be considered an upperbound which is limited by the size of the database.

Endurance

Endurance of the X2816B is generally limited by trapping of electrons in the tunnel oxide during tunneling as discussed in RR-510. Figure 5 shows the distribution observed for endurance on this part as measured by simultaneously changing all bits from one state to its complement and back. Additionally, a sample of 510 units had the data in every bit altered 10,000 times on a page by page basis. The results showed a failure rate of 1% in the first 10,000 cycles.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	Best Estimate Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	Best Estimate Failure Rate per 1000 Hours at 55°C
0.3eV	0	4.495×10^6	0.0151	6.986×10^6	0.0100
0.55eV	0	1.626×10^7	0.0042	3.654×10^7	0.0019
0.6eV	0	2.206×10^7	0.0032	5.130×10^7	0.0014
1.0eV	0	1.914×10^8	0.0004	8.184×10^8	0.0001
Totals	0		0.0229		0.0134

Table VI: Best estimate failure rate predictions.

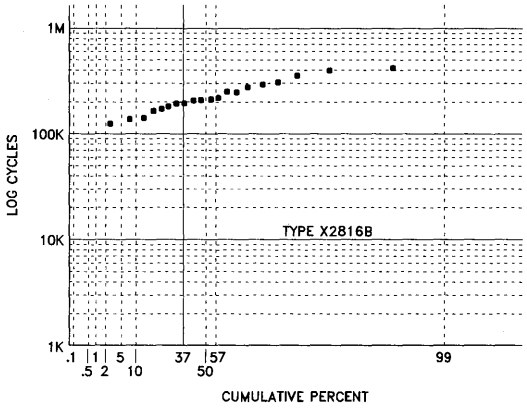


Figure 5: An extreme value distribution of endurance monitor on units cycled in mass mode.

SUMMARY

Data presented in this report shows that the X2816B is highly reliable. Further data is being collected to better predict the failure rates for this part.

REFERENCES

1. J. Caywood, NOVRAM Reliability Report, Xicor Publication RR-502A (1985).

2. R.K. Ellis, H.A.R. Wegener and J. Caywood, "Electron Technology in Non-Planar Floating Gate Memory Structure", 1982 IEDM Digest, pp. 749–752.

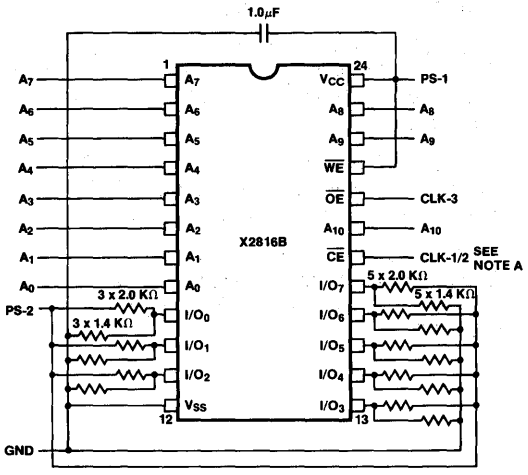
3. S.K. Lai, V.K. Dham and D. Guterman, "Comparison and Trends in Today's Dominant E^2 Technologies", 1986 IEDM Digest, pp. 580–583.

4. D. Guterman, B. Houck, L. Starnes and B. Yeh, "New Ultra-High Density Textured Poly-Si Floating Gate E^2PROM Cell", 1986 IEDM Digest, pp. 826–828.

APPENDIX A

Product	Package Type					
	Plastic		Cerdip		LCC	
	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}
X2816B	50.0	81.0	20.5	36.0	—	—

Thermal Resistance Table: θ_{JC} and θ_{JA} expressed in °C per watt.



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Notes: (A) CLK-1: Rows 1, 3, 5 . . . (odd rows—$\overline{CE}_A$)
CLK-2: Rows 2, 4, 6 . . . (even rows—$\overline{CE}_B$)
Such that: CLK-2 = $\overline{CLK\text{-}1}$

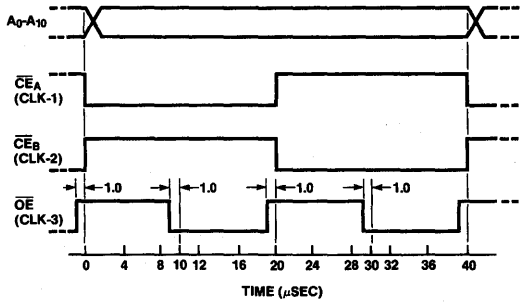
(B) 1. $\overline{WE}$ must always be hardwired to V_{CC} (Pin 24) at device as shown.

2. All resistors:
1% metal film
1/4 W

3. I/O pull-up: 2.0 KΩ
I/O pull-down: 1.4 KΩ

4. Socket-to-socket isolation as shown.

X2816B (DIP) Burn-in circuit.



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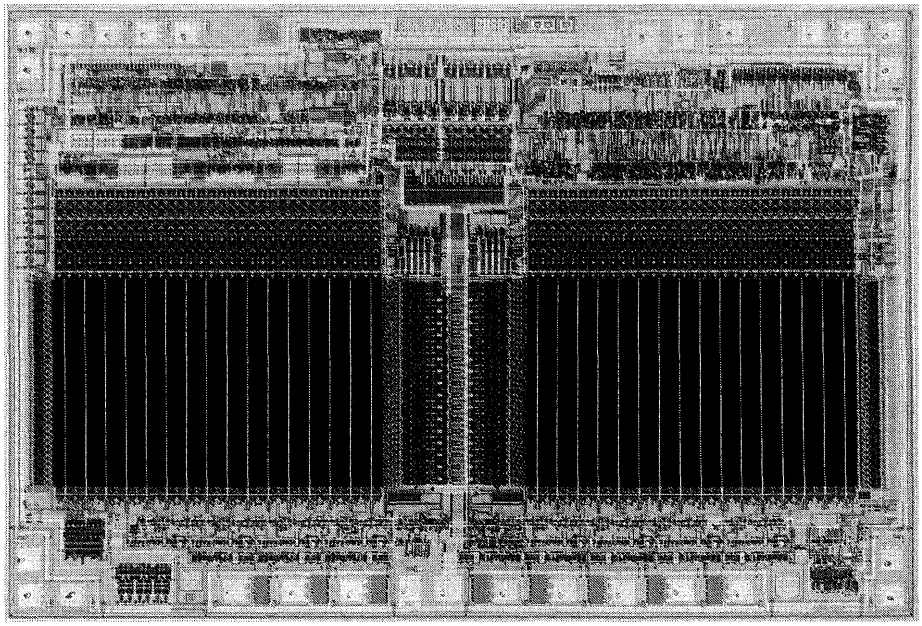
Notes: (1) A_0-A_{10}: binary sequencing address cycle: 40 μs.
(2) $\overline{WE}$ disabled (tied to V_{CC} at device).
(3) V_{IN} Low: 0.4V V_{IN} High: 5.0V
(4) V_{CC}: 5.50V

X2816B (DIP) Burn-in timing diagram.



0114-1

X28C64/X28C256 RELIABILITY REPORT

INTRODUCTION

The X28C64 and X28C256 are nonvolatile byte-wide E^2PROMs configured as 8K x 8 and 32K x 8 respectively. Both devices are compliant with the JEDEC approved pinout for byte-wide memories. Both devices operate on a single 5V power supply and feature byte or 64-byte page write, $\overline{DATA}$ Polling, Toggle Bit and Software Data Protect operations.

The memories are fabricated using Xicor's proprietary textured poly technology. They are designed for applications requiring extended endurance and data retention characteristics greater than 100 years.

Through rigorous environmental and electrical stress testing, the reliability of these devices has been well characterized. This report is a presentation of the data accumulated in testing these devices and supporting information needed to fully utilize the parts.

Figure 1 shows the DIP pin configurations for both the X28C64 and the X28C256; Figure 2 shows the functional block diagram for the X28C256; and Figures 3 and 4 illustrate the physical location of the address bits.

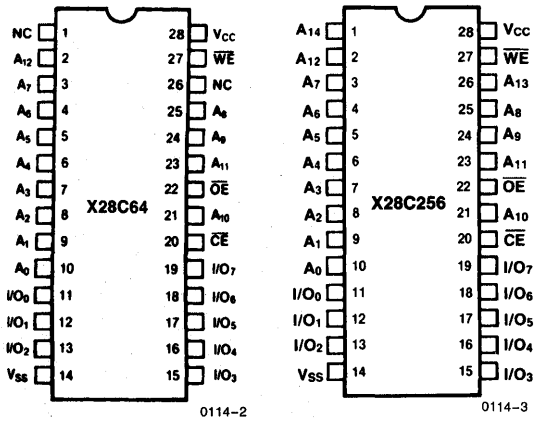


Figure 1: X28C64 and X28C256 DIP pin configurations.

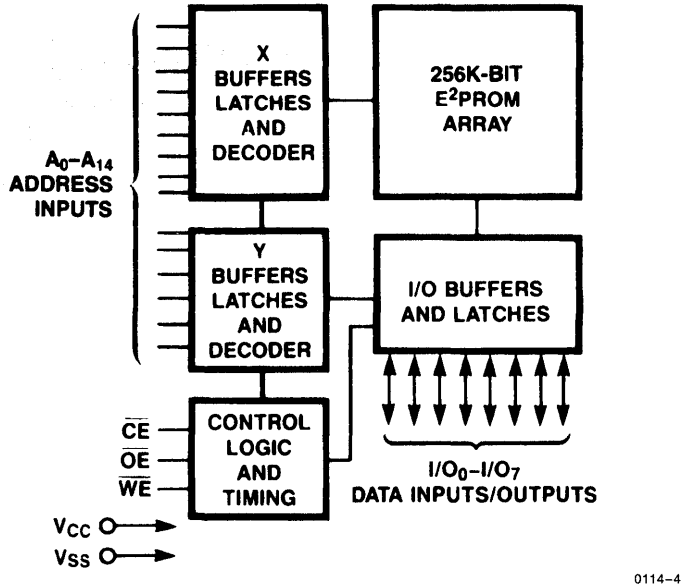
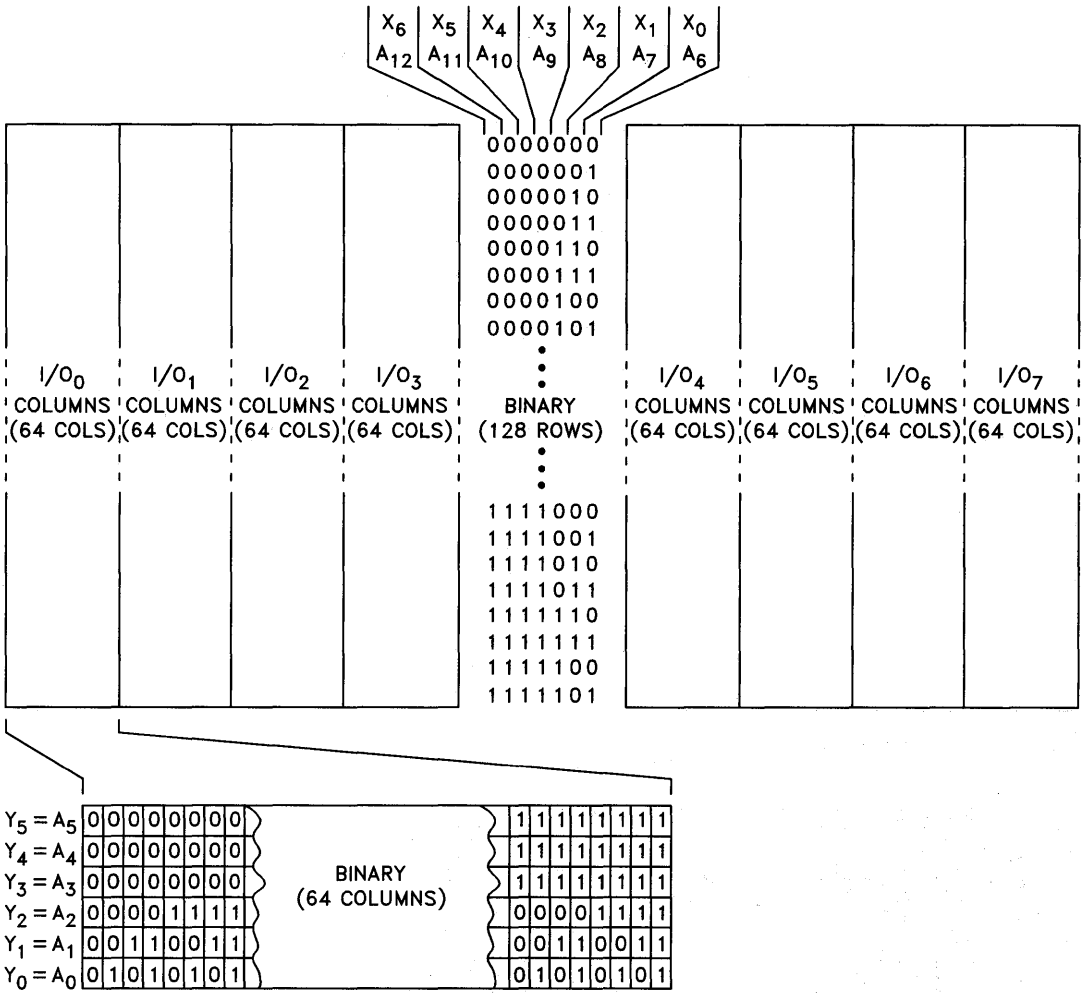


Figure 2: X28C256 functional block diagram.

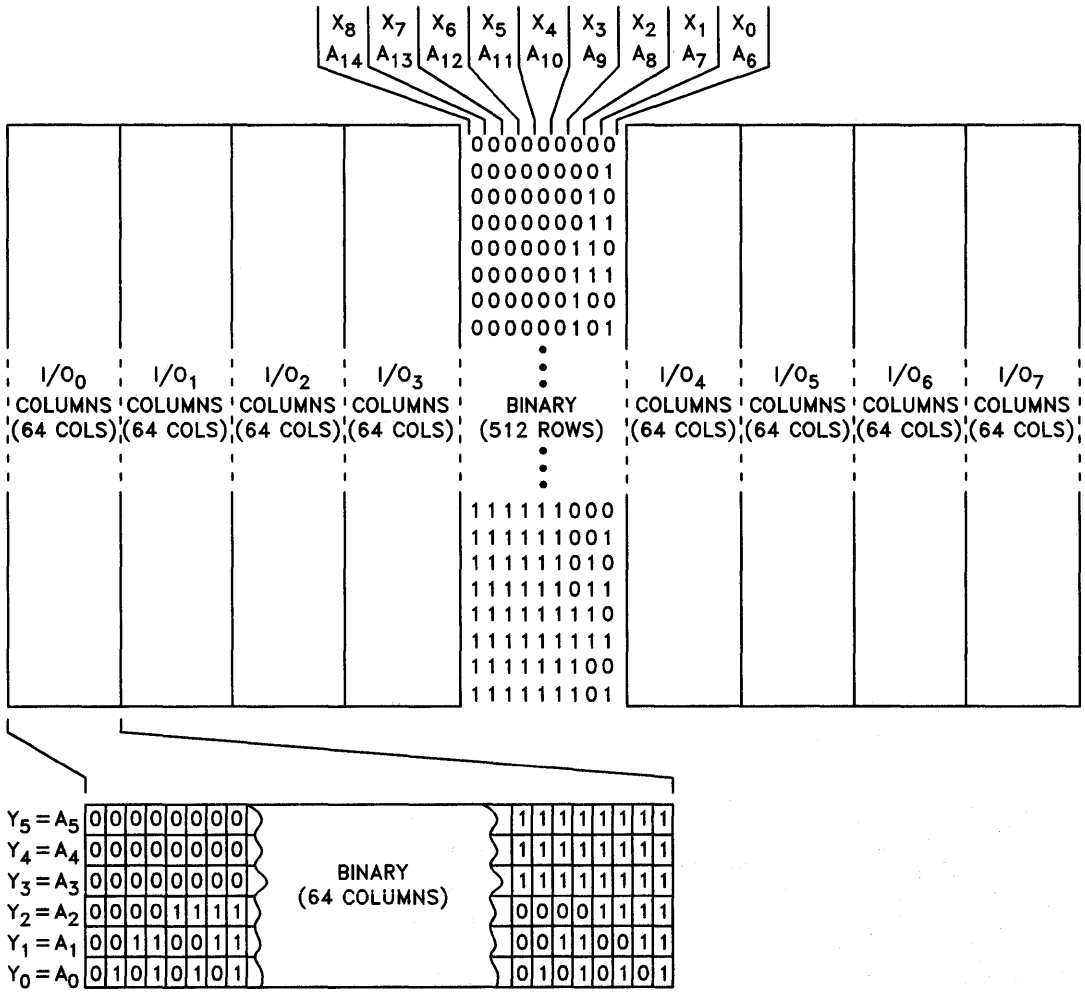


Address to XY Key

A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

0114-5

Figure 3: X28C64 physical bit map.



Address to XY Key

A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

0114-6

Figure 4: X28C256 physical bit map.

RELIABILITY STUDIES AND RESULTS

Before Xicor qualifies a process, it is subjected to accelerated stress testing to characterize potential reliability hazards. The major failure mechanisms that exist are: electromigration in contacts and interconnects, threshold voltage degradation due to hot carriers, corrosion damage due to moisture, and oxide failures due to E^2PROM operation.

Once these failure mechanisms are characterized and understood, then a product designed using this process must meet further constraints in circuit layout, ESD protection and latch-up protection. These parameters can be varied to further enhance process reliability in the product.

The device is subjected to a series of tests intended to accelerate device degradation and uncover flaws in processing or manufacturing. MIL-M-38510 and MIL-STD-883C, Method 5005, Groups A, B, C and D criteria have been the guide for electrical testing, environmental stress testing and package reliability testing.

A summary of product reliability testing and considerations includes the following:

High Temperature High Voltage Dynamic Lifetest

This test consists of continually reading a device at elevated temperature. V_{CC} is set between 5.25V and 6.5V, and the device address is incremented in a binary sequence every 25 μs. Its purpose is to uncover latent oxide defects and failures by inducing electrical overstress. The data is shown in Tables I and II.

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		V_{CC}	Device Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In		
1C	0	111	0	111	0	111	0	111	0	111	6.5	222000
2C	1	200[a]	0	199	0	199	0	199	0	199	6.5	398168
3C	0	138	0	80	0	80	0	78			5.25	128888
4C	0	173	0	80	0	80	0	80	0	80	5.25	175624
5C	1	75[b]	0	74	0	74	0	74	0	74	5.25	148168
6C	0	177	0	80	0	80					5.25	96296
7C	1	180[c]	0	100	0	100	0	100	0	100	5.25	213440
8C	0	258	0	160	0	160	0	158	0	158	5.25	334560
Totals	3	1312	0	884	0	884	0	800	0	722		1717144

[a] EOS damage due to latch-up

[b] Oxide defect: 0.6eV

[c] Contact electromigration: 0.9eV

Table I: X28C256 high temperature high voltage dynamic lifetest data. (+ 125°C, 5.25V–6.5V)

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		V_{CC}	Device Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In		
1Q	0	253	0	100	0	100	0	99[a]	0	99	5.25V	224704
2Q	0	342	0	100	0	100	0	100	0	100	5.25V	240656
3Q	0	483	0	100	0	100	0	100	0	100	5.25V	264344
4Q	0	418	0	80	1	80[b]	0	78[a]	0	78[a]	5.25V	214784
5Q	0	288	0	100	0	100					5.25V	131632
Totals	0	1784	0	480	1	480	0	377	0	377		1076120

[a] Unrelated test failure: broken lead

[b] Ionic contamination: 1eV

Table II: X28C64 high temperature high voltage dynamic lifetest data. (+ 125°C, 5.25V)

High Temperature Data Retention Bake

This test induces data retention failures by simulating accelerated storage times. Various aspects of retention as it pertains to reliability are discussed more fully in Xicor publication RR-515: Data Retention in Xicor E^2PROMs.

The test is also useful in investigating failures caused by mechanical stress (e.g. bond wire lifting).

The data for this test is presented in Table III.

Low Temperature Lifetest

This test is performed at −40°C and is used to detect hot electron trapping in the gate oxide. These are energetic electrons which exceed the thermal ambient. Data is presented in Table IV.

Temperature Cycling

This test is designed to promote device failure due to a thermal mismatch between the package and die. The devices are cycled between −65°C and +150°C in an air-to-air environment with 10 minute dwell cycles. This data is shown in Table V.

Lot #	Device	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.	
		# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
1	X28C256	0	80	0	80	0	80	0	80	0	80	0	80
2	X28C256	0	61	0	61	0	61	0	61	0	61	0	61
3	X28C64	0	25	0	25	0	25	0	25	1	25[a]	0	24
4	X28C64	0	25	0	25	0	25	0	25	0	25	0	25
5	X28C64	0	25	0	25	0	25	0	25	0	25	0	25
6	X28C64	0	25	0	25	0	25	0	25	0	25	0	25
Totals		0	241	0	241	0	241	0	241	1	241	0	240

[a] Oxide defect: 0.6eV

Table III: X28C64/X28C256 data retention bake results. (+250°C)

Lot #	Device	500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.	
		# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
A	X28C256	0	33	0	33	0	33	0	33
B	X28C256	0	67	0	67	0	67	0	67
C	X28C64	0	25	0	25	0	25	0	25
D	X28C64	0	25	0	25	0	25	0	25
E	X28C64	0	24	0	24	0	24	0	24
Totals		0	174	0	174	0	174	0	174

Table IV: X28C64/X28C256 low temperature lifetest data. (−40°C, 5.25V)

Lot #	Device	250 Cycles		500 Cycles		1000 Cycles	
		# Fail	# In	# Fail	# In	# Fail	# In
1	X28C256	0	40	0	40	0	40
2	X28C256	0	50	0	50	0	50
3	X28C256	0	50	0	50	0	50
4	X28C64	0	25	0	25	0	25
Totals		0	165	0	165	0	165

Table V: Temperature cycling data.
(−65°C to + 150°C)

Endurance Cycling to End-of-Life

Figure 5 shows device endurance results obtained by changing the data in the entire array to the opposite logic state via mass mode cycling. Device endurance is also characterized by page mode cycling. In this method, each byte or 64-byte page is changed sequentially. This data is presented in Figure 6. Further details on endurance cycling are provided in Xicor publication RR-510: Endurance of Nonvolatile Memories.

Xicor specifications call for a failure rate of less than 1% for 10,000 data changes per bit. Typically, Xicor devices perform far in excess of this.

Latch-Up Considerations

Latch-up is an inherent fabrication problem in CMOS devices due to the fact that during processing, parasitic bipolar transistors are created in addition to the desired MOS FETs. Design rules to reduce this susceptability have been developed and are incorporated into Xicor CMOS devices. Further details may be found in Xicor publication RR-516: Latch-up Considerations in Xicor CMOS Processes.

ESD Evaluation

ESD testing is done in accordance with requirements specified in MIL-STD-883C, Method 3015.6, Notice 7. This document provides guidelines for testing semiconductor devices to human body model discharges.

The X28C64 and X28C256 are compliant to Class 2 (>2000V) sensitivity protection.

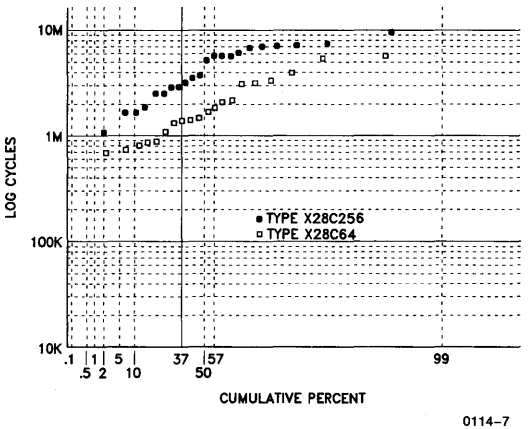
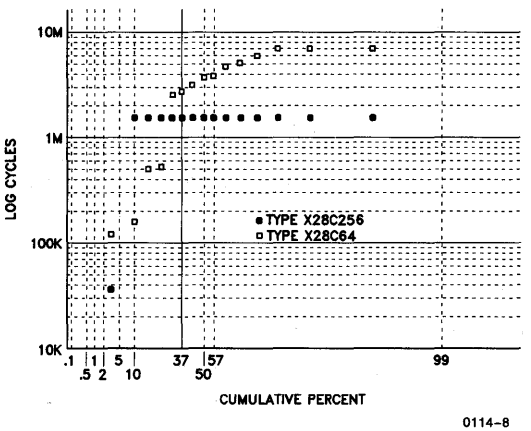


Figure 5: Endurance value distribution plots for X28C64 and X28C256 cycled in mass mode.



Note: Page mode cycling stopped at 7 million cycles for the X28C64 and 1.5 million cycles for the X28C256 to free cycling equipment for other tests.

Figure 6: Endurance value distribution plot for X28C64 cycled in page mode.

Prediction of Failure Rates

Failure rate calculation is easy once the basis for calculation is established. Most semiconductor failures are accelerated to some degree by temperature or voltage, or both. The classic parameter used to accelerate failure rates is temperature. The degree to which any given failure mode is accelerated by temperature is known as the activation energy or as the temperature acceleration factor.

The temperature dependence of a particular failure mechanism can be derived from the Arrhenius model as follows:

$$T_{af} = \text{Exp}\left(\frac{E_a}{k} \times \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where:

T_{af} = Temperature acceleration factor

E_a = Activation energy required to initiate the failure mechanism

k = Boltzmann's constant

T_1 = Operating temperature

T_2 = Stress temperature

Knowledge of a particular failure mode's activation energy allows one to predict long-term failure rates under normal operating conditions. If the activation energy is not known, it can be determined experimentally.

Typical failure mechanisms and their corresponding activation energies are:

Oxide Breakdown	0.3eV
Electromigration	0.55eV
Oxide Defect	0.6eV
Contact Electromigration[1]	0.9eV
Ionic Contamination	1.0eV

For time dependent dielectric breakdown, voltage acceleration also plays a part.[2] A voltage acceleration factor may be computed using the following model:

$$V_{af} = \text{Exp}\left(\frac{E_s - E_d}{E_{ef}}\right)$$

where:

V_{af} = Voltage acceleration factor

E_s = Stress electric field = V_s/T_{ox} (voltage over oxide thickness)

E_d = Operating electric field

E_{ef} = Field constant = 0.062 MV/cm

The voltage acceleration factor is dependent on the electric field and must be calculated for the particular voltage stress and oxide thickness where the failure occurred.

The data presented here is translated into failure rates occurring at normal operating conditions of T = 55°C (where T is the junction temperature), and V_{CC} = 5.5V. The power dissipation on-chip raises the junction temperature by $I_{CC} \times V_{CC} \times \theta_{JA}$, where θ_{JA}, the thermal coefficient, is equal to 23°C/W. Since the X28C64 and the X28C256 are both CMOS devices, the power dissipation is very low.

Xicor nonvolatile memory failures follow the classic bathtub curve shown in Figure 7.

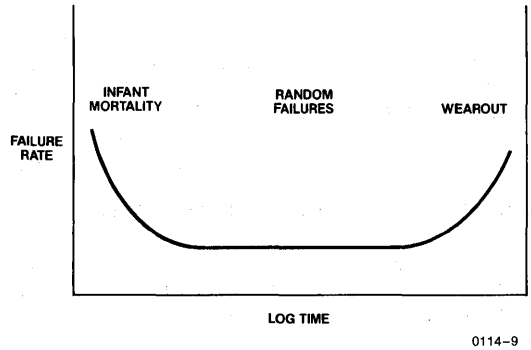


Figure 7: Illustration of bathtub curve of failure rates showing regions in which infant mortality, random failures, and wearout mechanisms dominate the failure rate.

Each region of this failure rate curve has specific failure modes which predominate. For example, the infant mortality region is dominated by failures which arise from processing defects. In production, test flows are designed to eliminate these infant mortality failures by screening, which reduces the incidence of early life failures.

The random failure region, which is the invariant bottom of the curve, is used to find the constant FIT rates calculated in Tables VI and VII. Failure rates are calculated separately for each activation energy, and the total failure rate is obtained by adding the individual numbers. Reliability predictions are then based on an exponential distribution of each failure mode. Since the failures are random in time, they follow the Poisson distribution function, and the failure rate is constant. The consequence of this is that the failure rates for each failure mode are additive, which makes the distribution calculation mathematically tractable. Predicted failure rates are calculated from actual failure rates by making a probability estimation based on the Chi-Square Distribution. By definition, a 60% confidence level means that there is a 60% probability that the failure rate is normally distributed around the calculated number.

End-of-life endurance is found to be dependent on array size, process technology and memory cell design. For reliability purposes, the end-of-life of a device is taken to be the end-of-life of the weakest bit. The mechanism for this failure is known to be oxide trap-up, and can be fitted to an extreme value distribution. Typical end-of-life cycling for the X28C256 is 5,000,000. For the X28C64, the typical end-of-life cycling figure is 2,000,000 cycles. For page mode cycling, the typical figures are greater than 3 million for the X28C64 and greater than 1.5 million for the X28C256. Thus, extremely low failure rates can be expected in typical applications, even at 100,000 or more cycles.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate per 1000 Hours at 55°C
0.3eV	0	4.4×10^6	0.0200	7×10^6	0.0130
0.55eV	0	1.4×10^7	0.0065	3.3×10^7	0.0028
0.6eV	0	1.8×10^7	0.0050	4.5×10^7	0.0020
0.9eV	0	7.3×10^7	0.0013	2.9×10^8	0.0003
1.0eV	1	1.2×10^8	0.0017	5.5×10^8	0.0004
Totals	1		0.0345		0.0185

Table VI: 60% UCL failure rate predictions for X28C64.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate per 1000 Hours at 55°C
0.3eV	0	7×10^6	0.0130	1.1×10^7	0.0085
0.55eV	0	2.3×10^7	0.0040	5.3×10^7	0.0018
0.6eV	1	2.9×10^7	0.0070	7.2×10^7	0.0028
0.9eV	1	1.2×10^8	0.0017	4.7×10^8	0.0004
1.0eV	0	1.9×10^8	0.0005	8.8×10^8	0.0002
Totals	2		0.0262		0.0137

Table VII: 60% UCL failure rate predictions for X28C256.

Failure rate predictions based on this data show a negligible infant mortality rate out in the field (due to extensive pre-shipment screening), and predicted long-term failure rates of 185 FITs for the X28C64 and 137 FITs for the X28C256 at 55°C with a 60% UCL. These numbers are representative of the smaller samples typically available for data analysis and not of the much larger numbers available in production runs.

Reliability Monitors

To maintain Xicor's quality standards, current production material is systematically sampled and subjected to the same type of stresses and testing used in the qualification procedures. This serves to enlarge the Reliability Department's statistical data base. Failure analysis is performed on material samples and results are published as part of Xicor's ongoing monitor program.

SUMMARY

The data presented here shows that the X28C64 and X28C256 are both extremely reliable products. Product reliability testing shows low semiconductor failure rates and high end-of-life endurance figures. Inherent data retention in these devices is in excess of 100 years.

These conclusions are based on monitor and device analysis data accumulated over the relatively short lifetimes of these devices. As production continues, more data is obtained through the ongoing reliability monitor system, increasing the number of candidate devices, and improving the ability to make statistical inferences. All FIT rate methods and calculations used here give conservative values.

REFERENCES

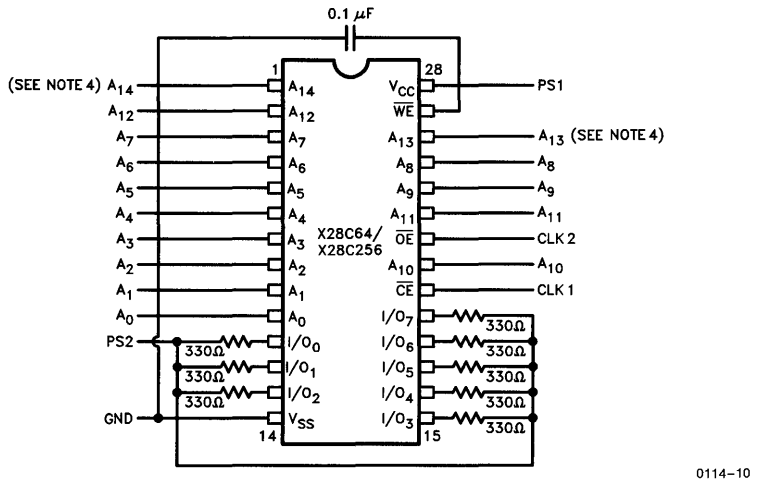
1. D.L. Crosthwait, Characteristics of Al-Si Interface Reactions.
2. D.L. Crook, 17th Annual Reliability Physics Symposium (1979): 1–7.
3. Norman B. Fuqua, Reliability Engineering for Electronic Design.

This report is based on data collected through August, 1989.

APPENDIX A

Product	Package Type					
	Plastic		Cerdip		LCC	
	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}
X28C64	35	85	6.3	47	10.4	125
X28C256	4	64	4.3	43.7	8.9	118

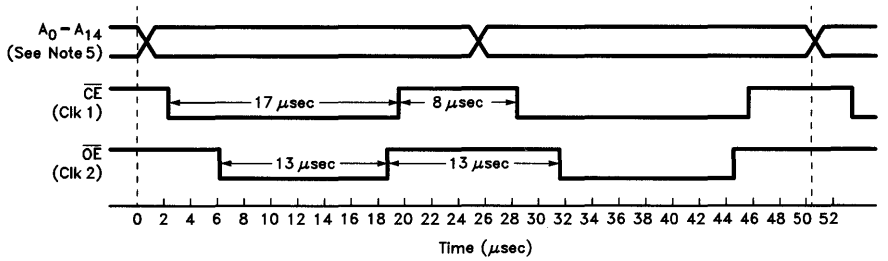
Thermal Resistance Table: θ_{JC} and θ_{JA} expressed in °C per watt.



0114-10

Notes: (1) $\overline{WE}$ must always be hardwired to V_{CC} (pin 28) at device as shown.
(2) All resistors:
1% metal film
1/4 W
(3) I/O pull-up: 330Ω
(4) Pin 1 (A_{14}) and Pin 26 (A_{13}) are no connects for X28C64.

X28C64/X28C256 (DIP) Burn-in circuit.

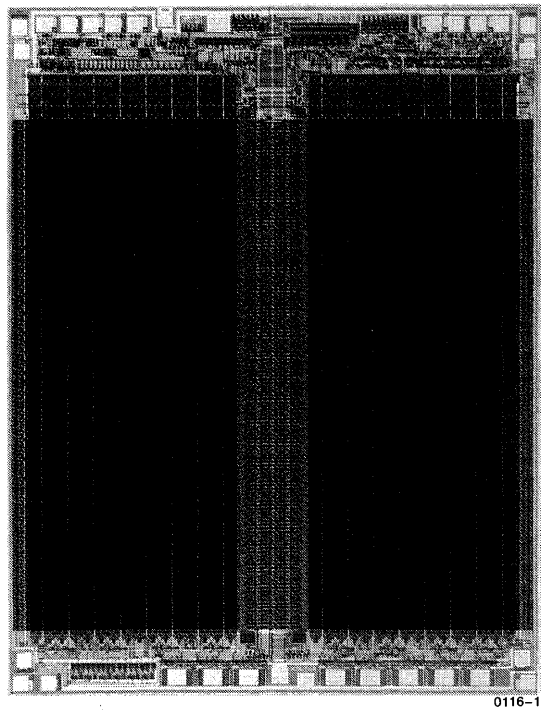


0114-11

Notes: (1) A_0-A_{14}: binary sequence every 25 μs.
(2) $\overline{WE}$ disabled (tied to V_{CC} at device).
(3) V_{IN} Low: ≤ 0.8V V_{IN} High: ≥ 2.4V
(4) V_{CC}: 5.5V
(5) X28C64: address pins A_0-A_{12} are utilized.

X28C64/X28C256 (DIP) Burn-in timing diagram.

NOTES



0116-1

X28256 RELIABILITY REPORT

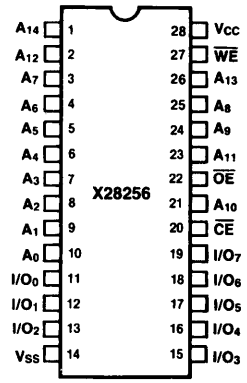
INTRODUCTION

The X28256 is a 32K x 8 electrically erasable programmable read only memory (E^2PROM) which operates on a single 5V power supply for all operations. The device is compliant with the JEDEC approved pinout for byte-wide memories, and features a 64-byte page write operation, DATA Polling, Toggle Bit, and Software Data Protect capabilities.

The X28256 is fabricated using Xicor's proprietary, high performance, textured poly MOS technology. It is designed for applications requiring extended endurance and data retention characteristics greater than 100 years.

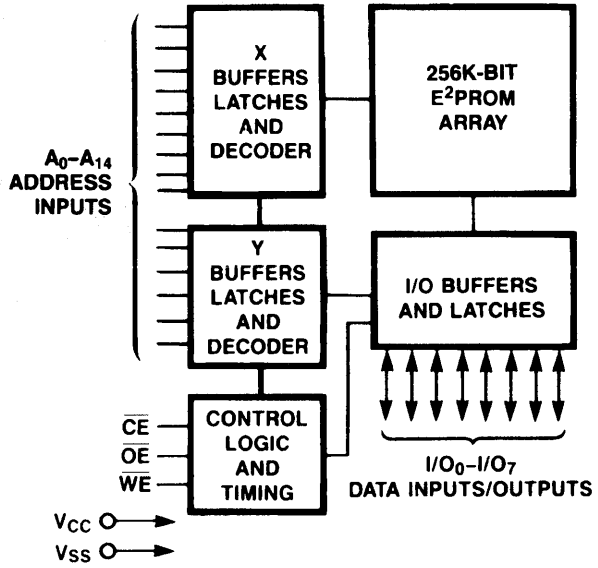
The X28256 has been well characterized through the years by means of accelerated environmental and electrical stress testing. This report provides the results of the tests used to demonstrate the reliability of the X28256 and a brief summary of the tests themselves.

Figure 1 shows the DIP pin configuration for the X28256; Figure 2 shows the functional block diagram for the device; and Figure 3 illustrates the physical location of the address bits.



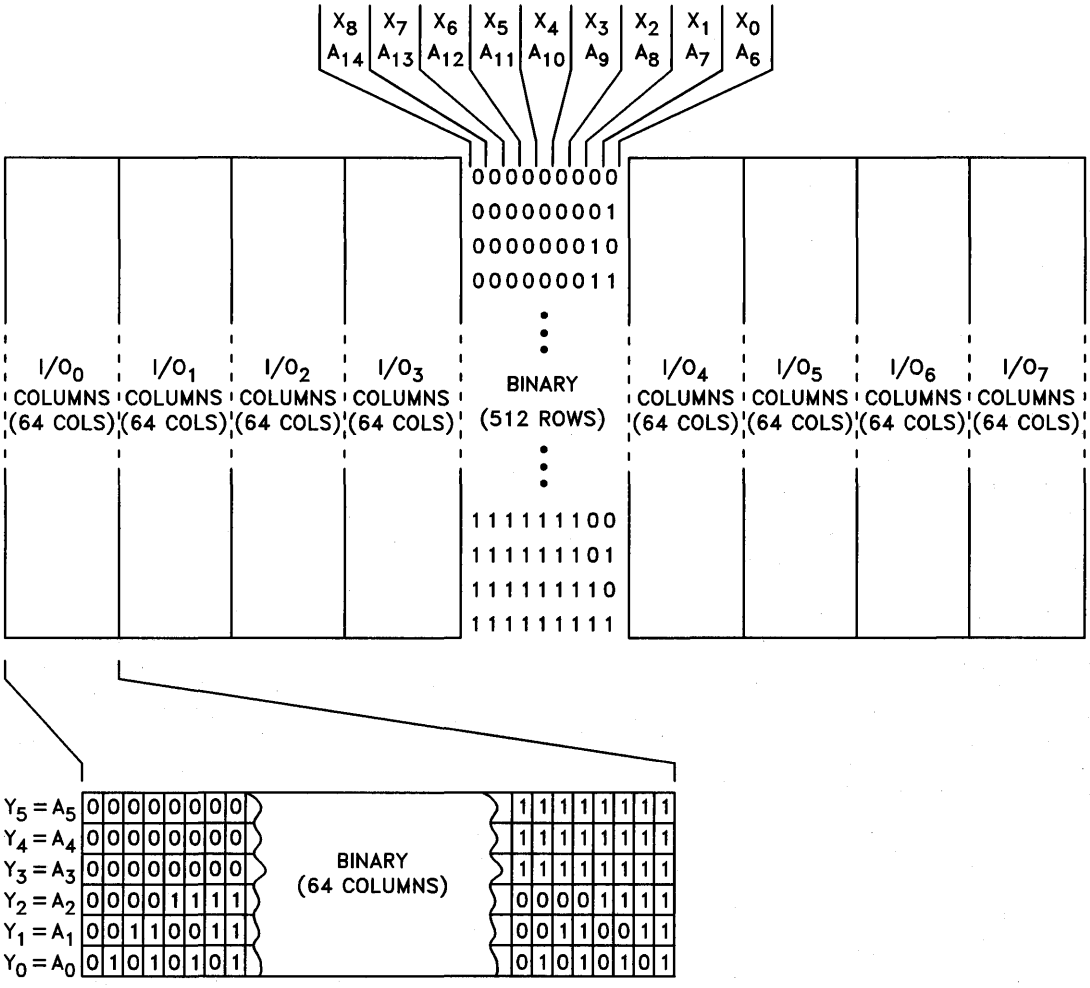
0116-2

Figure 1: X28256 DIP pin configuration.



0116-3

Figure 2: X28256 functional block diagram.



Address to XY Key

A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Figure 3: X28256 physical bit map.

TECHNOLOGY

A cross section of Xicor's textured poly floating gate cell is shown in Figure 4. Cell programming is achieved by electrons tunneling from poly 1 (the cathode) to poly 2 (the floating gate). Erasure is achieved by electrons tunneling from poly 2 to poly 3 (the anode). Tunneling is a quantum mechanical electron transport phenomena that is induced by high voltages generated directly on the chip.

During a write, poly 1, which is common to the whole array is brought low. The poly 2 floating gate is capacitively steered either to a high voltage (approximately 16V) for programming, or to 0V for an erase. A high voltage (>20V) is then applied to poly 3. If poly 2 is steered high, a large voltage drop occurs between poly 1 and poly 2, causing Fowler-Nordheim tunneling of electrons onto the floating gate. This results in a low voltage on poly 2 which is the program state. If an erase is desired, poly 2 is capacitively steered low, causing the large voltage drop to occur across poly 3 and poly 2. This causes electrons to tunnel off poly 2 onto poly 3, leaving the floating gate with a net positive voltage.

In order to perform a read, the poly 3 select transistor is first enabled. The charge on the selected floating gate controls a MOS transistor which determines the path of the current coming from the sensing circuitry. If the floating gate is charged positively (erased), current flows through the cell, and a "1" is sensed. If the floating gate is charged negatively (programmed), the current path through the cell is cut off, and the datum is read as a "0".

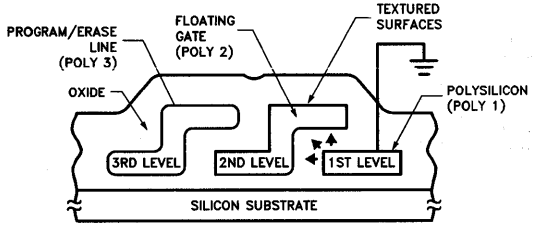


Figure 4: Cross sectional structure of a textured poly memory cell.

RELIABILITY STUDY AND RESULTS

Xicor subjects its devices to various accelerated tests and stresses. These stresses are designed to accelerate any degradation a device may experience during its normal lifetime. The following stresses were used to establish reliability data and failure rate characteristics for the X28256:

1) High temperature dynamic lifetest
2) High temperature high voltage test
3) Data retention bake
4) Environmental stresses

The following sections briefly describe these tests and present the accumulated reliability data associated with the tests.

High Temperature Dynamic Lifetest

Most failure mechanisms encountered in semiconductor devices are accelerated at high temperatures. These failure mechanisms have a temperature dependence proportional to exp $(-E_a/KT)$, where E_a is the activation energy of the particular failure mechanism, K is Boltzmann's constant, and T is the absolute temperature. The mathematical relationship is given by the Arrhenius equation. By testing at elevated temperatures and measuring failure rates, it is possible to extrapolate down to normal operating temperatures and predict the associated failure rates at these lower temperatures.

The high temperature dynamic lifetest consists of continually reading the devices at an ambient temperature of +125°C and a V_{CC} between 5.25V and 5.5V, while incrementing the addresses in a binary sequence. A known pattern is stored in the devices prior to insertion into dynamic lifetest. Each unit is tested for data retention and complete functionality after 48, 168, 500, 1000, 1500 and 2000 hours of dynamic lifetest. This is an effective stress for catching many types of semiconductor failures.

The results of the dynamic lifetest are shown in Table I for lots consisting of hermetically sealed ceramic DIPs (dual in-line package), and LCC (leadless chip carrier) packaged devices.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Device Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
Q1	0	57	0	57	0	18	0	18	0	18	0	18	4.25×10^4
Q2	0	65	0	65	0	65	0	65	0	65	0	65	1.30×10^5
Q3	0	163	0	163	0	163	0	163	0	163	0	163	3.26×10^5
Q4	0	228	0	228	0	158	0	158	0	158	0	158	3.02×10^5
Q5 (LCC)	0	369	0	369	0	369	0	369					3.69×10^5
Totals	0	882	0	882	0	773	0	773	0	404	0	404	1.17×10^6

Table I: X28256 high temperature lifetest data. (+125°C, 5.25V)

High Temperature High Voltage Test

In this test V_{SS} is grounded and all other pins including V_{CC} are held at 5.5V. The devices are stressed in an ambient temperature of +150°C. This stress is designed to catch failures related to ionic contamination, oxide defects and electrical overstress. Data retention and complete functionality are tested at 500 and 1000 hours. Table II contains the results of this testing.

Lot #	500 Hrs.		1000 Hrs.		Total Device Hours
	# Fail	# In	#Fail	# In	
Q1	0	283	0	283	2.8×10^5
Q2	0	19	0	19	1.9×10^4
Totals	0	302	0	302	3.0×10^5

Table II: X28256 high temperature high voltage lifetest data. (+150°C, 5.5V)

Data Retention Bake

This test consists of an unbiased bake (+250°C) with a known pattern programmed into the part. The devices are removed periodically and checked for the proper data. After initial programming, array readings are taken at 48, 168, 500, 1000 and 2000 hours. This test is performed because high temperatures will cause any latent oxide defects to leak charge off the floating gate. Retention bake data is found in Table III.

Environmental Stresses

Environmental stresses are applied to the devices to ensure that they will continue to operate properly even during changing or extreme environments. The thermal stress test identifies failure mechanisms which are caused by differing coefficients of thermal expansion in the composition of the packaged devices: lead frame, bond wires, die and package. Temperature cycling data was taken for hermetically sealed devices using MIL-STD-883C, Group D, Method 1010, Condition C specifications. The devices were cycled between −65°C and +150°C. The results of this testing for 250, 500 and 1000 temperature cycles are found in Table IV.

Lot #	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		Total Device Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	
Q1	0	18	0	18	0	18	0	18	0	18	0	18	3.6×10^4
Q2	0	65	0	65	0	65	0	65					6.5×10^4
Totals	0	83	0	83	0	83	0	83	0	18	0	18	1.01×10^5

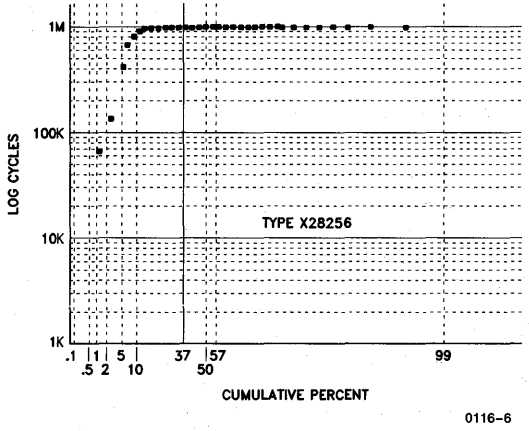
Table III: X28256 data retention bake results. (+250°C)

Lot #	250 Cycles		500 Cycles		1000 Cycles	
	# Fail	# In	#Fail	# In	# Fail	# In
Q1	0	45	0	45	0	45
Q2	0	45	0	45	0	45
Q3	0	45	0	45	0	45
Totals	0	135	0	135	0	135

Table IV: X28256 temperature cycling data. (−65°C to +150°C)

ENDURANCE

The endurance of a device is a measure of the ability of a nonvolatile memory to sustain repeated data changes. When the first single bit in the array is not capable of changing data states, the endurance limit has been reached. For the X28256, the endurance is limited by electron trapping in the tunnel oxide. This is because electrons get trapped in the silicon dioxide and accumulate, increasing the applied potential necessary for tunneling.



Note: Endurance cycling stopped at 1 million data changes to free cycling equipment for other tests.

Figure 5: Extreme value distribution plot for X28256.

To measure endurance, the data in the array is alternately changed from erased to programmed states. The number of cycles necessary for the first single bit to fail is recorded for each unit in the sample. An extreme value distribution plot is shown in Figure 5.

PREDICTION OF FAILURE RATES

As previously stated, stress testing makes it possible to accelerate failure rates. Failure rates at normal operating temperatures can then be predicted. Most failure mechanisms associated with this device are accelerated by temperature, voltage or both. Each failure mode has an associated activation energy (E_a). Four typical failure mechanisms and their activation energies are:

Oxide Breakdown	0.3eV
Electromigration	0.55eV
Oxide Defect	0.6eV
Ionic Contamination	1.0eV

If the activation energy for a particular failure mode is not known, it can be experimentally determined. Using the Arrhenius relation, Rate = R_0 exp $(-E_a/KT)$, we can relate the observed failure rate at the elevated ambient temperature with the predicted failure rate at normal operating temperatures. A detailed discussion of the pertinent calculations can be found in Xicor publication RR-506A: Byte-Wide NOVRAM (X2001/X2004) Reliability Report.

Table V gives the predicted long-term failure rates calculated for temperatures of +55°C and +70°C. Both Best Estimate and 60% Upper Confidence Level (UCL) failure rates are given. The Best Estimate gives the most likely failure rate for the given data, and the 60% UCL failure rate means that there is a 60% probability that the true failure rate will be less than the calculated value.

FIT rates can be obtained by multiplying the failure rates by 10^4. Therefore, the FIT rate at +55°C is 172, and at +70°C it is 305.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate per 1000 Hours at 55°C
0.3eV	0	4.68×10^6	0.0190	7.49×10^6	0.0125
0.55eV	0	1.52×10^7	0.0060	3.55×10^7	0.0026
0.6eV	0	1.92×10^7	0.0048	4.83×10^7	0.0019
1.0eV	0	1.24×10^8	0.0007	5.77×10^8	0.0002
Totals	0	1.48×10^8	0.0305	6.32×10^8	0.0172

Table V: 60% UCL failure rate predictions for X28256.

SUMMARY

This reliability report presents descriptions of basic cell operation, specific tests and stresses used to determine the reliability of the X28256, and the data collected from these tests.

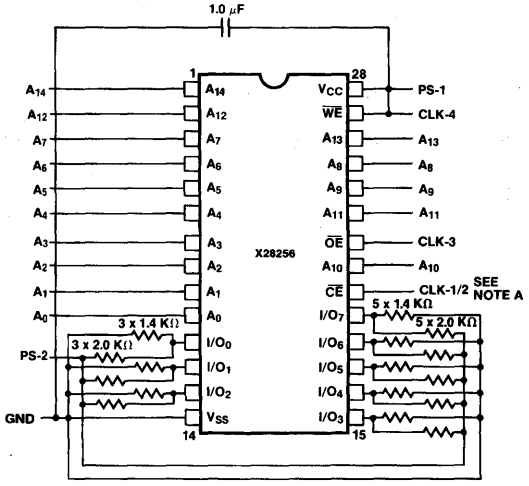
The data presented here shows that the X28256 is an extremely reliable memory device. Product reliability testing shows low semiconductor failure rates, high end-of-life endurance figures, and the ability to successfully resist device degradation under conditions of environmental stress. Inherent data retention in these devices is in excess of 100 years.

This report is based on data collected through June, 1989.

APPENDIX A

Product	Package Type			
	Cerdip		LCC	
	θ_{JC}	θ_{JA}	θ_{JC}	θ_{JA}
X28256	2.5	23.0	2.0	47.0

Thermal Resistance Table: θ_{jc} and θ_{ja} expressed in °C per watt.



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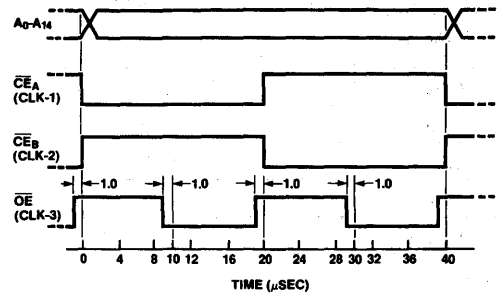
Note A: CLK-1: Rows 1, 3, 5 . . . (odd rows—$\overline{CE}_A$)
CLK-2: Rows 2, 4, 6 . . . (even rows—$\overline{CE}_B$)
Such that: CLK-2 = $\overline{CLK\text{-}1}$

Note B: (1) $\overline{WE}$ must always be hardwired to V_{CC} (Pin 28) at device as shown.
(2) All resistors:
1% metal film
1/4 W
(3) I/O pull-up: 2.00 KΩ
I/O pull-down: 1.40 KΩ
(4) Socket-to-socket isolation as shown.

X28256 (DIP) Burn-in circuit.



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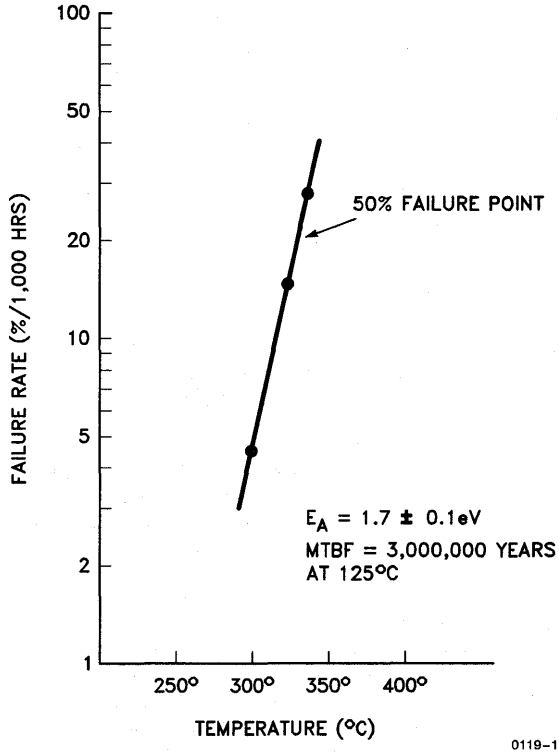
Notes: (1) A_0–A_{14}: binary sequencing address cycle: 40 μs.
(2) $\overline{WE}$ disabled (tied to V_{CC} at device).
(3) V_{IN} Low: 0.4V V_{IN} High: 5.0V
(4) V_{CC}: 5.50V

X28256 (DIP) Burn-in timing diagram.



DATA RETENTION IN XICOR E²PROM MEMORY ARRAYS

H. A. Richard Wegener

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INTRODUCTION

In Xicor nonvolatile memory devices, data consists of ones and zeroes stored in the memory array in the form of charge retained on a floating gate. During the course of normal operation charges may be added to or lost from the floating gate. The time elapsed between the original transfer of electrons by the act of programming or erasing, and the first erroneous read-out from that memory cell is called retention. The operating conditions during the time period considered may vary widely. Only those conditions permitted by the data sheet need to be considered in its definition. The memory device under consideration may be a single transistor, or it may be a large array of memory cells embedded in peripheral circuitry to function as an E²PROM. In either case, the first repeatable malfunction of one single memory cell during read-out defines the end of the retention of that particular device.

The intrinsic retention in Xicor E²PROMs is calculated to be many millions of years. However, defects introduced during the manufacture of the memory device may cause the retention to be less than the ideal intrinsic characteristic.

Retention is therefore a reliability problem, and its criterion is its failure rate. Xicor guarantees a failure rate expressed as "5 FITs at 55°C, 60% upper confidence limit". The meaning of this statement, and the reasons leading to it are explained in the paragraphs following this introduction. In most details, they are based on the section on Retention in the forthcoming IEEE Standard on Floating Gate Arrays.

FLOATING GATE RETENTION: A CAPACITOR DISCHARGE PROBLEM

Charge stored on a floating gate may be thought of as charge residing on one plate of a capacitor, separated from the other plate by the intervening dielectric. Even when all surrounding conductors are grounded, the potential due to the stored charges will cause a very slow discharge through the operation of the Fowler-Nordheim tunneling mechanism. Retention can be modeled and predicted by the expression:

$$t_R = \{C/AB\} * EXP\ (B/Vt),$$

where t_R is the retention time, **C** is the capacitance of the floating gate, Vt is the effective voltage due to the stored charge at which failure occurs, and **A** and **B** are constants of the Fowler-Nordheim equation. When measured values for all the variables on the right-hand side of the equation are substituted, retention times well in excess of several million years are obtained. This long term retention is an intrinsic property of Xicor's proprietary floating gate memory technologies, and can be expected as a feature of all Xicor memory cells.

At high temperatures, electrons will also be transferred by Schottky emission, which is dependent on temperature, activation energy, and applied field. This mechanism is described by the Schottky-Richardson equation, which has the form describing the forward current in a Schottky diode. It is this mechanism that gives rise to a temperature dependence of retention, and a measurable activation energy of 1.7eV. With intrinsic retention times exceeding millions of years in the operating temperature range, it is clear that real time retention data cannot be measured. Only under extremely high accelerating temperature conditions can retentions on the order of months be measured. These measurements can then be translated into retention times of approximately 50 billion years at 55°C.

In rare and isolated instances, physical process defects can occur in a memory cell. These defects may give rise to new values for the cell variables and thus result in shorter retention times for the affected cell. Activation energies of 0.6–0.8eV have been measured for such defects.

Retention in Integrated Circuits

The distinctions between retention in a single memory cell and in an integrated system such as a memory device are threefold: First, there are typically a large number of cells in any memory device. Since a data retention failure is determined by the first cell to fail, data retention in the device is statistically dependent on both the number of cells and their distribution.

Second, being part of a larger system, the cells are exposed to a more varied set of operating conditions. This is due to the diverse needs of the system represented by the chip, and not the simple requirements of a single cell.

Third, the presence of a very large number of cells increases the probability that one of them will contain a defect. In high density E²PROMs it can therefore be expected that retention (the failure of the first cell) will have a component, however small, that is determined by the defect density inherent in the technology. Structural defects which give rise to infant failures can be eliminated by production

screens. However, the ultimate retention failure rate is caused by statistical defects inherent in any given oxide process.

The Reliability Aspects of Retention

The specification of retention is a way of specifying the life expectancy of the data stored in a memory device. The concern for retention is with failures occurring in three phases of the devices' life cycle: a. early in life (infant mortality); b. random failure rate during normal use; and c. the intrinsic failures near the end of life. This can be illustrated by the typical aspects of the classic "bathtub curve", shown in Figure 1.

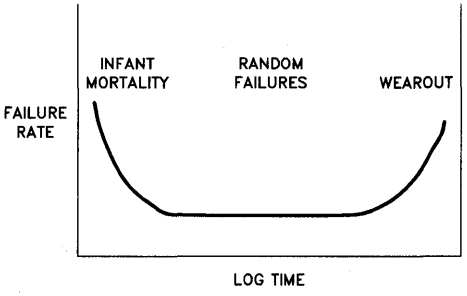


Figure 1: Illustration of bathtub curve of failure rates showing regions in which infant mortality, random failures and wearout mechanisms dominate.

Infant mortality cases are screened out by specific tests before shipment of the product. Some will fail during initial write-erase operations. Some are found by an accelerated voltage stress. Others are caught during a 48 hour storage at 150°C. The last are eliminated by a combination of endurance cycling and retention bake. A constant random failure rate is an indication that infant mortality cases have been eliminated. Since infant mortality failures are screened out during normal testing, they need not be considered a system (end user) reliability problem.

Intrinsic retention failures at the end of device life are determined by the structural design, technology and processing of the memory cell. These failure rates give rise to data retention times many orders of magnitude larger than equipment lifetimes. Successful measurements of intrinsic retention values have required temperatures of 300, 325 and 340°C to determine mean intrinsic retention times of 3000, 90, and 330 hours respectively, and an activation energy of 1.7eV. These translate into retention times of 1.2 million years at 125°C, 3.6 billion years at 70°C and 50 billion years at 50°C. This was demonstrated in Xicor's **Reliability Report RR-502A.**

The high accelerating conditions make an exact linear extrapolation to normal temperatures difficult with major additional work. Thus, this type of analysis serves mainly to confirm the very large retention times predicted for floating gates obeying Fowler-Nordheim tunneling laws.

This leaves the specification of the random failure rate during normal use as the most practical measure of data integrity. A common measure of the random failure rate is given by the number of failures per 1000 device hours, or the percentage of failures per 1000 hours, both of which can be expressed as FITs ([Number of failures x 1E9]/[Number of devices x Number of hours tested]). Since a random failure rate has to be determined under accelerated temperature conditions, the specification must include the temperature to which the accelerated data have been normalized. In addition, a confidence level must be included which (by standard statistical techniques) weights the failure rate estimate according to the number of data points used in deriving it.

Xicor's Specification of Retention

The Xicor specification for retention is a failure rate of "5 FITs (upper bound at the 60% confidence level) at 55°C". This follows the practice established for (UV erasable) EPROMs, which is a floating gate memory technology with a fifteen year data base.

The value of 5 FITs represents a mean time to failure of 25,000 device years. Another way of expressing this is as a failure rate for a specified retention time. For a 10 year retention, the failure rate is 0.044%.

For comparison, typical (UV erasable) EPROM products have retention failure rates of 20 FITs. The lower failure rate of E^2PROMs is due to the fact that their internal high voltage capability acts to cause immediate failures due to defects that would not be affected by the lower voltages in UV erasable EPROMs.

The retention specification as given, includes the failure rate stated as failure units ("FITs"), the temperature at which it is valid, and the statistical confidence level valid for the stated failure rate. For its significance in typical commercial applications and for easy comparison with similar EPROM data, Xicor has chosen 55°C as the reference temperature.

This is the temperature to which the data taken at accelerated temperatures are normalized. The normalization is performed by the accepted use of the Arrhenius equation, and an activation energy of 0.6eV. Failure rates at other temperatures can also be calculated from the specification given at 55°C, with the help of the same Arrhenius equation and the activation energy of 0.6eV.

The use of a confidence level follows standard reliability practice. When only a few data points (retention failures per year) are recorded, there is a finite chance that they were the result of fluctuations that will make the measured failure rate appear better than the true average. Multiplying the experimental failure rate by the proper factor increases it enough to ensure that it will include 30% of the data that are larger than the average. When this factor has been used, the failure rate is reported at the "60% confidence level (upper bound)". In principle, the choice of a confidence level (expressed as a percentage) is somewhat arbitrary. However, once a given level has been defined, the failure rate stated under its condition can be converted to the value proper for any other level. The 60% level chosen for this specification has the advantages of simplicity and industry acceptance.

The Determination of Retention Failure Rate

For the measurement of retention failure rates, the acceleration required is somewhat reduced. The activation energy of the mechanism involved in the random failure of floating gate retention has been determined to be near 0.6eV in both (UV erasable) EPROMs and in E^{2}PROMs. In order to confirm a failure rate to be equal to or lower than 5 FITs (upper bound at 60% confidence level, at 55°C), at least 75 devices must be stored for 1000 hours (6 weeks) at 250°C. For zero failures at 60% confidence level: 1/(75*1000) = 13,333 FITs. When this is divided by 2,724 to extrapolate from 250°C to 55°C the result is 5 FITs. This high temperature necessitates the use of ceramic packages. Plastic packages are limited to a temperature of 150°C. At that temperature, a much larger number of device-hours is necessary to confirm a rate of 5 FITs.

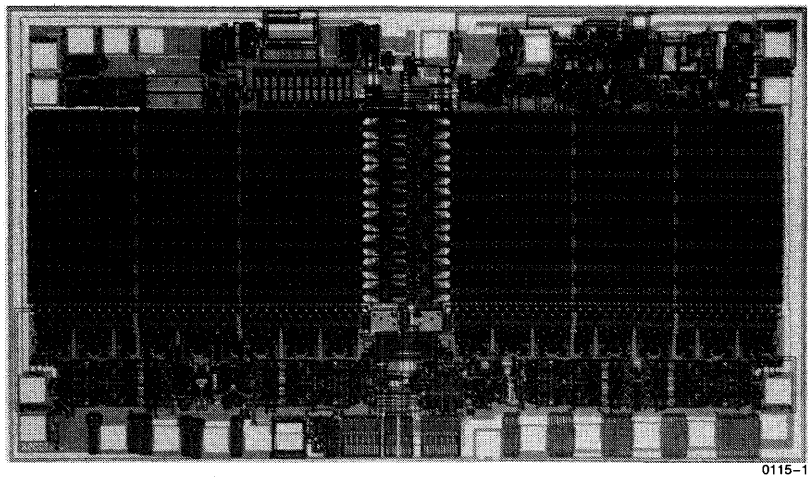
The actual retention failure rate is determined by a test called the "Retention Bake". The devices are stored unpowered at high temperature with a preset (typically checkerboard) data pattern. Devices in plastic packages are stored at 150°C, and ceramic package devices are stored at 250°C. They are then read from time to time. The failures are analyzed, and some are identified as retention failures.

SUMMARY

The time of retention for data in a Xicor E^{2}PROM memory cell is inherently on the order of millions of years. This can be projected theoretically on the basis of a closed form mathematical expression for charge loss that has been verified experimentally. This can also be confirmed by extrapolating experimentally obtained data at high temperatures to normal operating temperatures.

The exact knowledge of this intrinsic retention would be unimportant if every device met its true design and production characteristics. It is the rare presence of defects that introduces the small probability of lower retention times. Retention is therefore a reliability problem, and Xicor has approached it as such.

The failure rates as a function of time have the typical aspects of the bathtub curve. Potential "infant mortality" failures are eliminated by a sequence of screening steps. The "end-of-life" failures are expected to occur a few million years hence. The one characteristic of interest that remains is the "random" failure rate. This failure rate is determined experimentally from Retention Bake data. Based on this experimental data Xicor guarantees retention failure rate of 5 FITs at 55°C at the upper bound of the 60% confidence limit.



0115-1

LATCH-UP CONSIDERATIONS IN XICOR CMOS PROCESSES

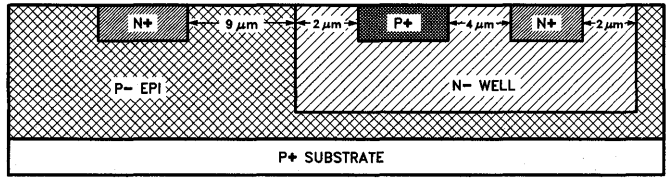
INTRODUCTION

Latch-up is an inherent problem in CMOS devices due to the fact that during processing, MOS FETs are not the only structures fabricated. Parasitic bipolar transistors are also created which act as silicon-controlled rectifiers (SCRs). Since latch-up is inherent in the process, all CMOS devices can be forced into the latched state. The focus in designing CMOS devices is to reduce latch-up susceptibility under normal, and sometimes harsh, operating conditions. Design methods used by Xicor to reduce this susceptibility will be discussed.

CELL STRUCTURES AND LATCH-UP

The structures of interest for Xicor's 1.8 μm and 1.4 μm CMOS processes are illustrated in Figure 1.

The vertical PNP transistor has its emitter and collector formed by the P+ source/drain diffusion and the P type substrate respectively. Its base is N-well. In the lateral transistor, (the NPN), the base is a P type substrate with the emitter formed by N+ source/drain diffusion and an N-well collector. These two bipolar transistors are cross-coupled with common base-collector regions. Under normal bias conditions, the complementary PNP and NPN transistors remain in the high impedance state, which is referred to as the blocking state. Latch-up can be initiated only when one of the bipolar transistors becomes active. If current flows through any of the parasitic resistors and causes a sufficient voltage drop across the base-emitter junction, one of the parasitic bipolar transistors can be turned on. This forward bias condition of the junction allows collector current to flow. The collector current that flows across the base-emitter resistor of the second parasitic bipolar transistor can cause a sufficient voltage drop to turn on this second transistor.



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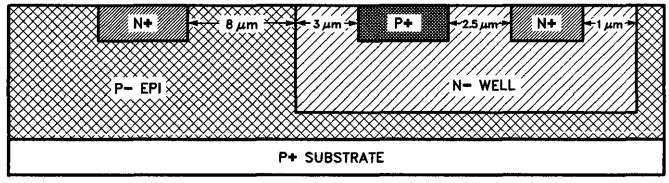
1.8 μm CMOS process



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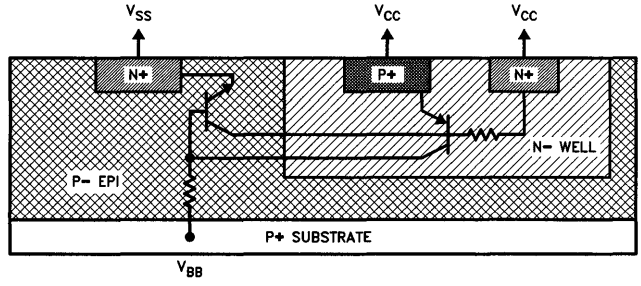
1.4 μm CMOS process



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Process equivalent circuit

Figure 1: Xicor CMOS processes.

If the current gain of the two transistors and the values of the parasitic resistors are high enough, a regenerative condition is created between the complementary bipolar transistors, where each continues to drive the other. The current in both transistors will increase until either the self limiting condition is reached or the device is destroyed. This high current, low impedance state of the SCR is known as "latch-up".

Latch-up can be destructive to the device when the metal lines are blown or the junctions are melted, or it can be nondestructive. In the second case, the chip can be restored to the blocking state by a power-down and power-up sequence.

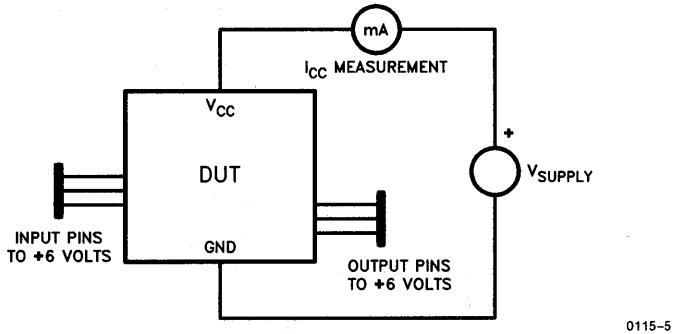
CAUSES OF LATCH-UP

There are numerous ways in which latch-up can be triggered. The most common ways are during: power-up; supply overvoltage; and pin overvoltage and undervoltage. These conditions are discussed below.

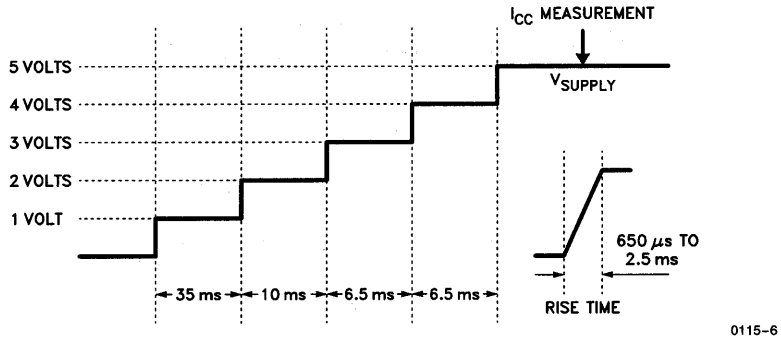
Power-Up

Latch-up can occur when the pins of the device are driven high before the supply voltage has been applied to the circuit. This situation can occur when an unpowered circuit board or device is plugged into a system that is already under power.

Figures 2 and 3 illustrate the test set-ups for both the slow power-up and the fast power-up tests. Results of these tests are presented in Tables I and II.



Block diagram



Typical timing diagram

Figure 2: Slow power-up test set-up.

Characteristics:	I_{CC} latch-up current due to input and output pins in an overvoltage condition during power-on ramp.
Test conditions:	All inputs and data outputs equal to V_{CC} + 1V minimum. V_{CC} ramps from 0V to 5V in 1V steps, ramp rate is less than or equal to 0.2V/ms.
Maximum I_{CC}:	80 mA
Latch-up condition:	$I_{CC} \geq$ 80 mA

Temp: +25°C

	I_{CC} (in μA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	650	750	613
X28C010	1.4 μm	85	2.3 mA	70

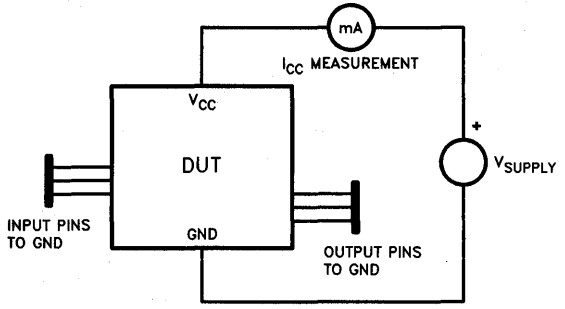
Temp: −55°C

	I_{CC} (in μA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	860	900	800
X28C010	1.4 μm	330	2.8 mA	290

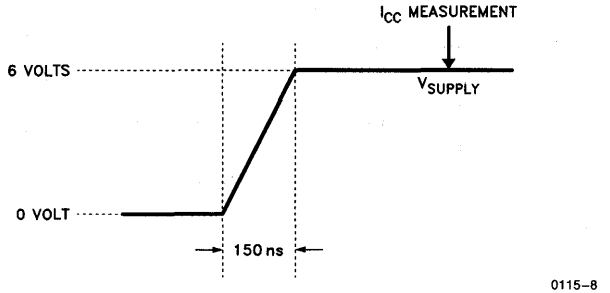
Temp: +125°C

	I_{CC} (in μA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	530	540	520
X28C010	1.4 μm	300	2.0 mA	65

Table I: Results of slow power-up test.



Block diagram



Typical timing diagram

Figure 3: Fast power-up test set-up.

Characteristics:	I_{CC} latch-up current induced by hot socketing.
Test conditions:	All inputs and data outputs equal to 0V. V_{CC} ramps from 0V to 6V in 200 ns or less.
Maximum I_{CC}:	100 mA
Latch-up condition:	$I_{CC} \geq$ 100 mA

Temp: +25°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 µm	8.5	9.9	8.0
X28C010	1.4 µm	13.0	16.4	11.1

Temp: −55°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 µm	11.5	13.2	10.5
X28C010	1.4 µm	16.0	19.9	14.6

Temp: +125°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 µm	7.0	100[a]	5.8
X28C010	1.4 µm	11.0	13.6	9.9

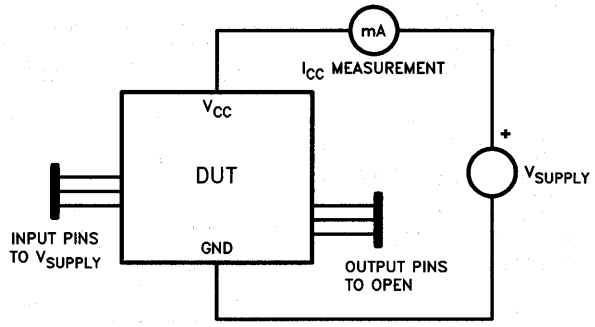
[a] Latch-up induced only for conditions where $V_{CC} \geq 5V$

Table II: Results of fast power-up test.

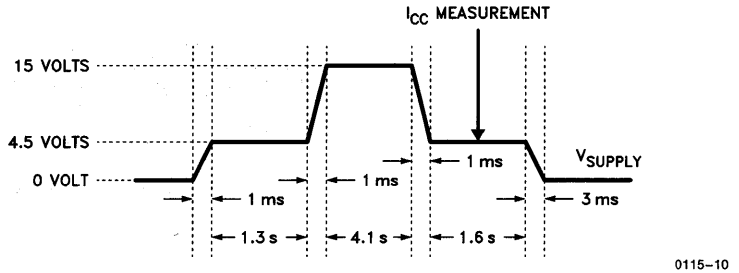
Supply Overvoltage

A supply voltage exceeding the absolute maximum rating can cause an internal junction to break down or produce a substrate current that triggers latch-up.

Figure 4 illustrates the test set-up for the supply overvoltage test. The results of this test are presented in Table III.



Block diagram



Typical timing diagram

Figure 4: Supply overvoltage test set-up.

Characteristics: I_{CC} latch-up current due to supply overvoltage.

Test conditions: All inputs are tied to supply. All data outputs are open. The unit is powered up to 4.5V, then 15V is applied to the V_{CC} pin. Measurement is done at 4.5V V_{CC}, after the 15V pulse.

Maximum I_{CC}: 100 mA

Latch-up condition: $I_{CC} \geq 100$ mA

Temp: +25°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	7.15	8.00	6.25
X28C010	1.4 μm	11.5	12.2	10.5

Temp: −55°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	8.10	9.56	7.02
X28C010	1.4 μm	10.1	97.0[a]	151 μA

Temp: +125°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	4.00	100[a]	3.31
X28C010	1.4 μm	12.5	96.0[b]	7.08

[a] Latch-up induced for overvoltage ≥14V
[b] Latch-up induced for overvoltage ≥13V

Table III: Results of supply overvoltage test.

Pin Overvoltage and Undervoltage

Ringing, or noise glitches on the I/O pins, can create a transient forward bias condition at the I/O junction. If the transistor is part of a susceptible latch loop, latch-up could result.

Figures 5 and 6 illustrate the test set-ups for both the pin overvoltage and the pin undervoltage tests. Results of these tests are presented in Tables IV and V.

Characteristics: I_{CC} latch-up current due to pin in overvoltage condition.

Test conditions: Untested inputs tied to supply of 4.5V. Untested outputs are open. Triggered voltage of +15V (with max. 100 mA) is applied to pin under test.

Maximum I_{CC}: 100 mA

Latch-up condition: $I_{CC} \geq 100$ mA

Temp: +25°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	7.30	7.70	5.30
X28C010	1.4 μm	11.0	13.1	10.0

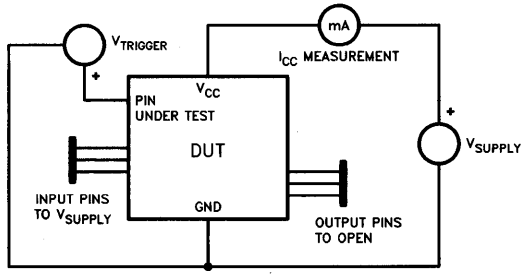
Temp: −55°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	8.00	8.90	6.60
X28C010	1.4 μm	8.00	9.50	7.40

Temp: +125°C

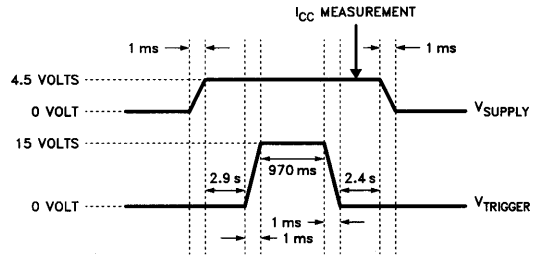
	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	3.90	3.95	3.60
X28C010	1.4 μm	14.5	15.6	11.7

Table IV: Results of pin overvoltage test.



0115-11

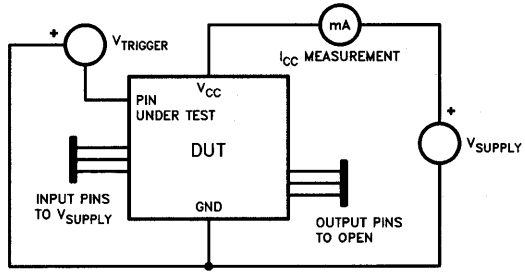
Block diagram



0115-12

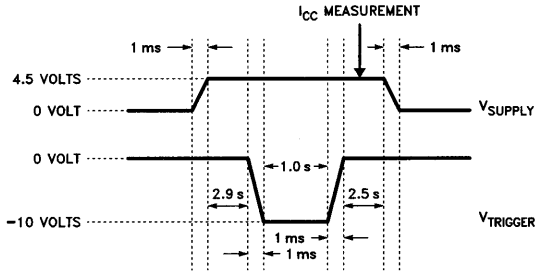
Typical timing diagram

Figure 5: Pin overvoltage test set-up.



0115-13

Block diagram



0115-14

Typical timing diagram

Figure 6: Pin undervoltage test set-up.

Characteristics: I_{CC} latch-up current due to input/output pins in undervoltage condition.

Test conditions: Untested inputs tied to supply of 4.5V. Untested outputs are open. Triggered voltage of −10V (with max. −100 mA) is applied to pin under test.

Maximum I_{CC}: 100 mA

Latch-up condition: $I_{CC} \geq 100$ mA

Temp: +25°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	6.0	6.5	5.1
X28C010	1.4 μm	10.5	12.3	10.1

Temp: −55°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	6.5	7.6	5.3
X28C010	1.4 μm	15.0	22.3	11.4

Temp: +125°C

	I_{CC} (in mA)			
Product Type	**Process**	**Typ.**	**Max.**	**Min.**
X28C64, C256	1.8 μm	3.8	4.3	2.9
X28C010	1.4 μm	10.0	32.8	9.6

Table V: Results of pin undervoltage test.

LATCH-UP SUSCEPTIBILITY IN XICOR CMOS PRODUCTS

In order to increase the immunity of its CMOS products against latch-up, Xicor employs several methods in its product design. These include:

1) Negative substrate bias: A −3.5V V_{BB} generator prevents transient forward biasing of the base-emitter junction of the SCR.

2) Large spacing between the N+ diffusion area and the N-well during processing eliminates the potential for the parasitic NPN to be active.

3) An epitaxial layer on a low resistivity substrate reduces the parasitic resistance, and lowers the gain of the lateral transistor.

4) Guard rings around the diffusion area reduce substrate current and substrate resistance.

5) All input and output buffers are connected only to N+ diffusions. No connections to P+ diffusions (P-channel source or drain) are made.

TESTING FOR LATCH-UP

Xicor characterizes the latch-up susceptibility of its 1.8 μm and 1.4 μm CMOS devices by following specifications defined in MIL-M-38510/750. These test procedures are recommended by the JEDEC JC-40-2 CMOS Logic Standardization Committee. The X28C64 and X28C256 were used to test the 1.8 μm process, while the X28C010 was used to test the 1.4 μm process.

CONCLUSION

Data accumulated from the various stress tests show that Xicor's CMOS products exhibit excellent latch-up immunity. These CMOS devices are carefully designed and fabricated under the design and process rules which were discussed previously. This ensures that Xicor products operate in the blocking state even under harsh operating conditions.

REFERENCES

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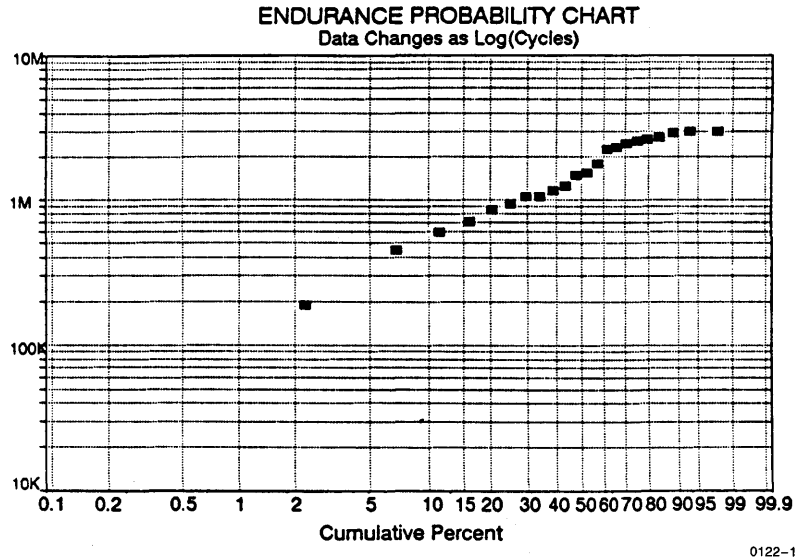
2. L. A. Glasser, D. W. Doberpuhl, "The Design and Analysis of VLSI Circuits", Addison-Wesley Publishing Company, Inc., (1983).
3. N. H. E. Weste, K. Eshraghian, "Principles of CMOS VLSI Design: A System's Perspective", Addison-Wesley Publishing Company, Inc., (1983).
4. A. G. Lewis, "Latch-Up Suppression in Fine-Dimension Shallow P-Well CMOS Circuits", IEEE Trans. Electronic Devices, vol. ED-31, No. 10, October 1984.
5. A. Ochoa, Jr., "A Discussion of the Role of Distributed Effect in Latch-Up", IEEE Trans. Nuclear Science, vol. NS-28, No. 6, December 1981.
6. "Latch-Up in CMOS Integrated Circuits", EIA JEDEC JC-40-2 CMOS Logic Standardization Committee, 1987.
7. Military Specification, MIL-M-38510/750.

This report is based on data collected through June, 1989.

NOTES



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X24C01 RELIABILITY REPORT

9

INTRODUCTION

The X24C01 is a 1024-bit serial E^2PROM, internally organized as thirty-two 4-byte pages. Like all Xicor products, the X24C01 employs Xicor's Textured Poly Floating Gate technology, which has been demonstrated to be the optimum technology for full featured nonvolatile memories.

Reliability Studies and Results

At Xicor, all new products are subjected to a series of tests before the device is qualified. In these tests, the device is stressed at elevated voltages and high and low temperatures. The purpose of these tests is to accelerate standard semiconductor infant mortality failures and any potential defects that may occur as random failures during the device's normal useful lifetime. These data are then used to predict semiconductor failure rates under normal operating conditions.

In addition, Xicor has undertaken studies to determine characteristics unique to nonvolatile memories, such as retention and endurance. This report also includes a group of standard environmental tests to insure reliable operation under all extremes. Explained below are the tests and stresses to which the X24C01 was subjected.

High Temperature Dynamic Life Test

In the High Temperature Dynamic Life Test, (DLT) the device array is first written with a topological checkerboard pattern. It is then subjected to a temperature of 125°C at 5.5V in a continuous sequential read mode. All units are tested for retention and functionality at readouts at 48 hours, 168 hours, 500 hours, 1000 hours and 2000 hours.

This test is designed to accelerate early life failures, (first 48 Hours) and to uncover latent defects that would be seen as random failures during the normal useful lifetime. These data, along with the HTHV data are used to predict actual field reliability for the device. The DLT test results are shown in Table 1.

In addition, all units submitted to the tests and stresses that follow, are first subjected to DLT for 168 hours. The test lots are then divided, with some units continuing DLT and the balance split among other tests.

High Temperature High Voltage (HTHV)

The purpose of this stress is to accelerate failures due to mobile ionic contamination, electrical overstress and latent gate oxide defects. In this stress, a static bias is established throughout the circuit by applying 5.5V to all pins while V_{SS} is held at ground in an ambient temperature of 150°C. The units are stressed for 1000 hours, with readouts occurring at 48 hours, 168 hours 500 hours and 1000 hours. The results of the tests are shown in Table 2.

Lot #	48 Hours		168 Hours		500 Hours		1000 Hours		2000 Hours		Total Device Hours *
	IN	Fail	In	Fail	In	Fail	In	Fail	In	Fail	
1	905	1[b]	904	0	150	0	150	0	150	0	383,280
2	979	0	979	0	143	0	143	0	143	0	379,456
3	1036	1[b]	1035	0	149	0	149	0	149	0	397,168
4	1000	0	1000	0	150	1[a]	149	0	149	0	393,300
5	996	0	996	2[c]	149	0	149	0	149	0	392,488
6	189	0	189	0	49	0	49	0	49	0	112,448
Totals	5105	2	5103	2	790	1	789	0	789	0	2,058,140

Note: a. Ionic Contamination
b. oxide breakdown
c. Leaky Select Transistor

* Device-hours excludes the first 48 hours

Table 1. X24C01 Dynamic Life Test. V_{CC} = 5.5V and T_A = 125°C

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Lot #	168 Hours		500 Hours		1000 Hours		Total Device Hours
	In	Fail	In	Fail	In	Fail	
1	35	0	35	0	35	0	35,000
2	48	0	48	0	48	0	48,000
3	50	0	50	0	50	0	50,000
4	48	0	48	0	48	0	48,000
5	52	0	52	0	52	0	52,000
6	25	0	25	0	25	0	25,000
Totals	258	0	258	0	258	0	258,000

Note: b. oxide breakdown

Table 2. X24C01 High Temperature High Voltage Test. V_{CC} = 5.5V and T_A = +150°C

Failure Rate Calculation

Determining The Failure Rate Unit

If there is one failure in 20,000 devices in 1000 hours, the failure rate will be:

$$\frac{1\ failure}{20{,}000\ devices \times 1000\ hours} = 5 \times 10^{-8}$$

The failure rate of a device is calculated in FIT (Failure unIT). One FIT is defined as one failure in 10^9 device-hours. Thus, the above failure rate is:

$$\frac{5 \times 10^{-8} \times 10^{9}\ failures}{10^{9}\ device-hours} = 50\ FITs$$

As previously mentioned, the results from the DLT and HTHV tests allow one to predict the long-term failure rates for the device under normal operating temperature and voltage conditions.

Acceleration Factors

Each failure mechanism accelerated by temperature is associated with an activation energy E_a. the reaction rate at which a process is accelerated by temperature is given by the Arrhenius equation[4]:

$$R = R_0 \exp\left(-\frac{E_a}{kT}\right)$$

Where:
E_a = Activation Energy
T = Absolute Temperature
k = Boltzmann's Constant = 8.62 x 10 eV/°K

For a given activation energy, where t1 and t2 are the times to failure at the normal operating temperature of T1 and the stress temperature T2, respectively, then the relationship between the times to failure is :

$$TAF = \frac{t_1}{t_2} = \frac{\exp\left(\frac{-E_a}{kT_2}\right)}{\exp\left(\frac{-E_a}{kT_1}\right)} = \exp\left\{\frac{E_a}{k} x \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right\}$$

Where:

TAF = Temperature Acceleration Factor
T_1 = Operating Temperature
T_2 = Stress Temperature

Knowledge of a particular failure mode's activation energy allows one to predict long-term failure rates under normal operating conditions.

Typical failure mechanisms and their corresponding activation energies are:

Oxide Breakdown	0.30eV
Metal Electromigration	0.55eV
Oxide Defect	0.6eV
Silicon Electromigration	0.90eV
Ionic Contamination	1.0eV

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Ea in eV	Total Device Hours		# of Fails	Equivalent Device Hours		Calculated Failure Rate (FIT)		60% UCL Failure Rate (FIT)	
	@+125°C	@+150°C		@+55°C	@+70°C	@55°C	@70°C	@55°C	@70°C
0.30	2.058E+6	2.58E+5	0	1.682E+7	1.08E+7	0	0	59.46	92.90
0.55	2.058E+6	2.58E+5	0	8.472E+7	3.60E+7	0	0	11.80	27.74
0.60	2.058E+6	2.58E+5	2	1.183E+8	4.66E+7	16.89	42.93	25.34	64.40
0.90	2.058E+6	2.58E+5	0	9.082E+8	2.24E+8	0	0	1.101	4.459
1.00	2.058E+6	2.58E+5	1	1.816E+9	3.84E+8	0.550	2.605	1.101	5.210
			3			17.45	45.54	98.82	194.7

Notes: 1. One FIT = 1 failure in 10^9 device-hours. To convert to failure rate percent per 1000 hours, divide FITs by 10,000
2. Failures from 48 hour DLT are excluded, since such failures are considered infant mortalities and are minimized by extensive screening prior to shipment.

Table 3. Summary of Semiconductor Failure Calculations for the X24C01.

For time dependent gate oxide breakdown (E_a = 0.3eV), there is also a voltage acceleration factor (VAF) given by Crook's equation[5], as follows:

$$VAF = \exp\left(\frac{E_s - E_d}{E_f}\right)$$

where:

E_s = stress field $= \frac{V_s}{T_{ox}}$

E_d = operating field $= \frac{V_d}{T_{ox}}$

T_{ox} = Gate Oxide

E_f = Field Constant = 0.062MV/cm

Table 3 contains the results of these calculations. Also included in the table is the 60% upper confidence level (UCL) calculation. This indicates that with a 60% confidence the actual failure rate will be below that calculated. We also made the conservative assumption of including the Oxide Breakdown, Metal and Silicon Electromigration (Ea = 0.30, Ea = 0.55eV and Ea = 0.90eV respectively) failure rates. These failure mechanisms should be included whether they were observed or not, since they could be anticipated.

Data Retention Bake

Data stored in E^2PROMs are associated with the absence or presence of electrical charge stored on the floating gate. A device is considered to have failed if the charge leaks off the floating gate. A floating gate at equilibrium (+ and - charges are equal) will be read as one or zero depending on the sense amp circuitry.

Therefore, in order to test for leakage, a charge is placed on the floating gate such that when the cell is read it will be opposite to that read at equilibrium. After being written with the specified pattern, the units are baked for 2000 hours at 150°C, with readouts occurring at 500 hours, 1000 hours and 2000 hours. The results of the tests are shown in Table 4. A retention FIT rate calculation was also performed and is shown in Table 5. It should be noted: based on Xicor studies on data retention of all its memories Xicor specifies 100+ years data retention. For details on data retention in Xicor memories refer to Reliability Report RR-515.

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Lot #	48 Hours		168 Hours		500 Hours		1000 Hours		2000 Hours		Total Device Hours *
	IN	Fail	In	Fail	In	Fail	In	Fail	In	Fail	68,000
1	34	0	34	0	34	0	34	0	34	0	68,000
2	34	0	34	0	34	0	34	0	34	0	68,000
3	34	0	34	0	34	0	34	0	34	0	68,000
4	34	0	34	0	34	0	34	0	34	0	68,000
5	34	0	34	0	34	0	34	0	34	0	68,000
Totals	170	0	170	0	170	0	170	0	170	0	340,000

Table 4. Data Retention Bake @ 150°C

Ea in eV	Total Device Hours		# of Fails	Equivalent Device Hours		Calculated Failure Rate (FIT)		60% UCL Failure Rate (FIT)	
	@+125°C	@+150°C		@+55°C	@+70°C	@55°C	@70°C	@55°C	@70°C
0.60	0	3.40E+5	0	4.077E+7	1.60E+7	0	0	24.53	62.35
Totals			0			0	0	24.53	62.35

Table 5. Data Retention Failure Rate Calculations

Extended Endurance and Data Retention

Devices must retain correct data after long-term operation. A stress called endurance/retention is designed to examine a device's performance at retaining data after repeated write cycles to all memory locations. In this test, all units are subject to 100,000 write cycles, followed by a static bake at +150°C. After the bake the devices are tested for data retention and functionality. The results of the test are shown in Table 6 below.

Lot #	100 K Cycle		168 Hours @ 150°C	
	In	Fail	In	Fail
3	50	0	50	0
4	32	0	32	0
5	49	0	49	0
Totals	131	0	131	0

Table 6. Endurance/Data Retention

End of Life Endurance

Long-term operational life of a device is also measured by how long it can endure repetitive data changes. This is the purpose of endurance testing. In this test the units are subject to continual data changes until the first bit in its array is read incorrectly. There are two major methods of cycling: block or mass mode, where the entire array is changed in one cycle; and page cycling, where each physical row is cycled in one operation, requiring 32 write operations to cycle the entire array one time. The data shown in the endurance probability chart in Figure 1 were collected by page cycling.

This probability chart is a tool developed by Xicor to fit the endurance limit of the weakest bit in the entire array to an extreme value distribution. The ability of Xicor to use this method is a result of the Textured Poly Floating Gate technology employed. This technology has one prevalent failure mechanism, trap-up, which is the diminishing cell program margins due to electrons trapping in the tunneling oxides.

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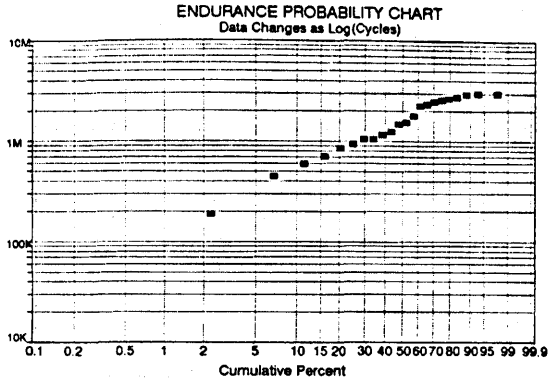

Figure 1.Typical X24C01 Lot Endurance

Low Temperature Dynamic Life Test

As geometries of semiconductor memories are scaled down, hot electron trapping in the gate oxides has been detected in other technologies. In order to determine if hot electron trapping could impact the reliability of the X24C01, a Low Temperature Dynamic Life test was performed. This test is functionally identical to the DLT test, but with the ambient temperature set at -40°C. The test results in Table 7 indicate hot electron trapping is not a concern with the X24C01.

Lot #	168 Hours		500 Hours		1000 Hours		Device Hours
	In	Fail	In	Fail	In	Fail	
1	50	0	50	0	50	0	50,000
2	52	0	52	0	52	0	52,000
3	50	0	50	0	50	0	50,000
4	50	0	50	0	50	0	50,000
5	50	0	50	0	50	0	50,000
6	25	0	25	0	25	0	25,000
Totals	277	0	277	0	277	0	277000

Table 7. Low Temperature Dynamic Life Test

ENVIRONMENTAL STRESSES

This group of tests is performed on plastic packages to insure that excessive humidity and ambient vapors will not cause failures and also to insure temperature cycling will not have detrimental effects on the combination of materials used.

The three major failure modes for plastic packaged devices under moisture test are:

- Mobile Ions - Ions on the passivation glass are made more mobile by humidity. If enough charge transfer occurs, a device parameter could be altered or a parasitic transistor could be introduced, degrading device performance.
- Chemical Corrosion - Phosphorous is commonly used in the passivation and under metalization layers. Sufficient phosphorous, when combined with water molecules, produces phosphoric acid which may etch away aluminum lines.
- Electrolytic Corrosion - When a voltage potential exists between two adjacent metal lines under enhanced surface conditions, (presence of moisture) an electrolytic corrosion process may be triggered. This condition could result in an open metal line.

Autoclave

Autoclave or pressure pot testing subjects a device to a 2 atmosphere steam environment. This test will accelerate mobile ionic drift, chemical corrosion and to some extent electrolytic corrosion. The test results are summarized in Table 8.

Lot #	48 Hours		96 Hours		144 Hours		Device Hours
	In	Fail	In	Fail	In	Fail	
1	52	0	52	0	52	0	7488
2	52	0	52	0	52	0	7488
5	52	0	52	0	52	0	7488
Totals	156	0	156	0	156	0	22464

Table 8. Steam Autoclave

85°C/85% Relative Humidity Stress

85/85 testing is performed to determine life expectancy of devices in high temperature and high humidity environments. This test will accelerate all three environmental failure modes. It is an especially good test for detecting electrolytic corrosion.

85/85 tests can be performed in two ways. The first is by supplying voltage to V_{CC} with all other pins alternately biased at 0V and +55.V. The

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second method is to test the device with V_{CC} at 0V and all other pins alternately biased at 0V and +5.5V. This provides a potential between metal lines and insures maximum humidity at the die surface. Results of these tests are shown inTables 9 and 10.

Lot #	500 Hours		1000 Hours		Device Hours
	In	Fail	In	Fail	
1	52	0	52	0	52,000
2	52	0	52	0	52,000
5	52	0	52	0	52,000
Totals	156	0	156	0	156,000

Table 9 . 85/85 (power off)

Lot #	500 Hours		1000 Hours		2000 Hours		Device Hours
	In	Fail	In	Fail	In	Fail	
1	52	0	52	0	52	0	104,000
2	52	0	52	0	52	0	104,500
5	52	0	52	0	52	0	104,000
Totals	157	1	156	0	156	0	312,500

Table 10. 85/85 (power on)

Temperature Cycling

This test subjects the devices to temperature extremes of -65°C to +150°C. this test is performed to stress the package to detect poor bond wire attachment and to determine if there is a potential problem due to thermal mismatch between the die and the package material that could cause device failures. The results of these tests are tabulated in Table11

Lot #	250 Cycles		500 Cycles		1000 Cycles		Device Hours
	In	Fail	In	Fail	In	Fail	
1	52	0	52	0	52	0	52,000
2	52	0	52	0	52	0	52,000
3	52	0	52	0	52	0	52,000
4	52	0	52	0	52	0	52,000
5	52	0	52	0	52	0	52,000
6	24	0	24	0	24	0	24,00
Totals	284	0	284	0	284	0	284,000

Table 11. Temperature Cycling -65°C to +150°C

CONCLUSION

The X24C01 has been demonstrated to be a highly reliable semiconductor memory. The semiconductor FIT rate is well below the industry average for a comparable device. Xicor specifies the X24C01 as having an endurance of 100,000 cycles and data retention of 100+ years. The additional environmental data indicates that the combination of process technology and assembly techniques provides a highly reliable device under all environmental conditions.

0122-7

NOTES

DETERMINING SYSTEM RELIABILITY FROM E²PROM ENDURANCE DATA

By Richard Palm

Xicor has published numerous reliability reports regarding data retention and endurance; however, the relationship of this data to system reliability warrants further analysis and discussion. This paper will discuss two methods for determining the affect of endurance on system reliability. The first method will use actual data collected on the X2816A and the second method will use data collected on the X2864A.

Definition of Terms

Endurance - is the ability of a nonvolatile memory to sustain repeated data changes.

Endurance Failure (Level) - is the limit of endurance, expressed in number of write cycles, when the *first bit* of any memory device or memory system is found to be in error after a required data change.

Write Cycle - to reduce testing time Xicor uses a test method whereby the entire array of the device under test is written in a single write cycle. Therefore, all references to "write cycle" equate to every bit in the entire array (device or system array) being written.

Cumulative Failure (Probability) - the percentage of parts not expected to attain a particular goal; i.e., endurance level.

Note: all endurance data used in this report were collected at a cycling frequency of one cycle per 100ms and at +25°C.

Background

There are three reliability categories for nonvolatile memories: semiconductor, data retention and endurance.

- Semiconductor reliability pertains to several failure modes common to all semiconductor devices such as oxide rupture and micro-cracks.
- Data retention refers to the capability of a nonvolatile memory device to retain valid data under worst case conditions.
- Endurance is the ability of a nonvolatile memory device to sustain repeated data changes.

Xicor reliability reports, RR502A and RR504, detail these three categories for Xicor devices. Reliability is easily deduced for semiconductor failures and data retention. The affect of endurance on reliability is not so straightforward.

Because endurance screening is a destructive procedure, Xicor performs endurance life tests on a sample basis. The data collected from these tests are then plotted onto an extreme value distribution graph to determine the endurance distribution for a particular lot of devices.

Using the Extreme Value Distribution Data

Figure 1 is an extreme value distribution graph for twenty X2816A devices and Table 2 (located on the last page) is the raw data used to generate the straight line shown.

- In this sample lot the lowest ranked device (#1) exceeded 279,000 write cycles before the first bit failure occurred; however, the graph extends to the left to show that only ~ .01% of all devices from this manufacturing lot will fail before 200,000 cycles.
- The maximum of the extreme value distribution occurs at the 37% cumulative probability point (statistically, 37% of all devices will fail to reach this endurance level), indicating that the predicted most probable endurance of devices in this lot is 460,000 cycles.

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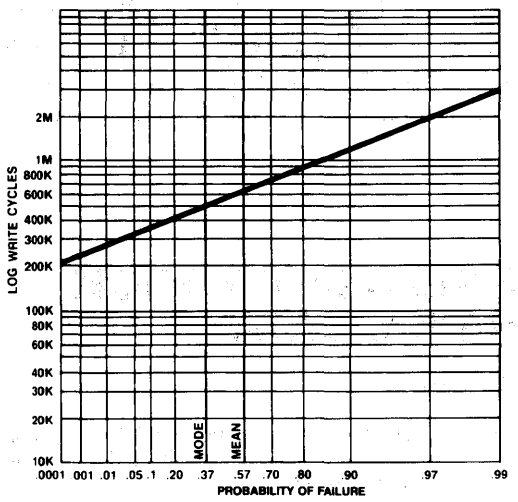

Figure 1: Extreme Value Distribution Graph for One Twenty Piece Lot of X2816As

Reliability data are generally stated in terms of percent failures per 1000 hrs. This can be easily derived from the extreme value graph in a two step procedure.

The system design parameters for this example are chosen as follows: the lifetime of the system is five years; and each X2816A will experience 250,000 write cycles over the lifetime of the system.

- The first step determines the failure rate per 1000 write cycles using the formula W = C/E where:

  W = failure rate in %/1000 write cycles

  E = endurance level chosen for the system (250,000 write cycles) divided by 1000.

  C = cumulative failure rate at E (in this case .5%).

  Therefore W = .5%/250 = .002%/1000 write cycles.

- Converting this to percent failures per 1000 hours requires H = W × A where:

  H = failure rate in %/1000 hrs.

  W = failure rate in %/1000 write cycles

  A = number of write cycles per hour. (i.e., 2.5×10^5 cycles/5 years)

In our case, H = .002 × 5.7 = .0114%/1000 hrs.

In the above example the entire X2816A is being rewritten at the rate of 5.7 times every hour. In some applications this could occur, but generally the frequency is much lower. Using the same graph and arbitrarily choosing the lowest cumulative failure rate depicted at 200,000 write cycles and performing the same calculations, the percent failures per 1000 hrs. drops dramatically.

W = .01/200 = .00005%/1000 write cycles

H = .00005 × 4.56 = .00022%/1000 hrs.

Predicting System Endurance Reliability Within Design Constraints

This next example is based on data collected on the X2864A. The system requirements for which the data were collected are defined as follows: the life expectancy of the system is ten years; the number of write cycles is 10,000. Therefore, Xicor cycled five lots of approximately three hundred devices each, for 10,000 write cycles. The data were collected by cycling the devices every 100ms at ~25°C. Table 1 summarizes the data collected.

LOT #	# OF UNITS	# OF FAILURES	% FAILURES
1	297	4	1.35
2	295	2	0.68
3	295	4	1.36
4	298	6	2.01
5	299	6	2.01
TOTAL	1484	22	1.48

Table 1: Raw Data From Cycling X2864A Devices 10,000 Times

The overall failure rate of devices unable to reach 10,000 write cycles is 1.48%. How does this relate to system reliability?

- The system is defined as having a life expectancy of ten years or 87.6×10^3 hours.

- The failure rate in percent per 1000 hours is determined by dividing the percent of parts unable to reach 10,000 write cycles by system's life expectancy in thousands of hours.

Therefore, reliability based on endurance for this system is:

1.5%/87.6 = 0.017%/1000 hrs.

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Temperature

RR504 describes in detail the affect of temperature on endurance. In general, this report shows that for every 50°C rise in temperature the endurance rate doubles. The data collected for the above examples was taken at +25°C. Therefore, for systems operating at a more common +40°C the endurance will improve. Figure 2 illustrates the case for the X2816A.

- The line labeled +25°C is the same as that in Figure 1.
- The added line is for the predicted increase in endurance at +40°C.
- The cumulative failure rate at 250,000 write cycles moves from .5% to less than .01% and the endurance reliability increases as follows:
  W = .01%/250 = .00004%/1000 write cycles
  H = .00004% × 5.7 = .0002%/1000 hrs.

The failure rate for the X2864A sample lots can be expected to decrease by a factor of ~ 1.30, for the increase in operating temperature from +25°C to +40°C; yielding a failure rate of .013%/1000 hrs. vs. the unfactored .017%/1000 hrs.

Frequency of Writing

Xicor reliability report RR504 describes device operation and the affects of frequency of writing to a device. Figure 3 is a copy of a graph in RR504, depicting the relationship of write cycle frequency on the endurance of a Xicor nonvolatile memory.

There are two key relationships illustrated by the graph in Figure 3.

- As the frequency of writing decreases the slope of the plotted line, the extreme value, decreases.
- Although the most probable endurance (the 37% cumulative failure point) does not show appreciable change, the decreasing slope is significant in the region most concerned with predicting reliability, the .01% to 5% region (shaded area of Figure 3).

It is in this region that a system's reliability is determined. Arbitrarily choosing the .1% probability of failure point, Figure 3 shows:

- A write cycle frequency of 1 per 100 seconds increases the endurance level by a factor of 2 over a write cycle frequency of 1 per 100 milliseconds.

0018-5

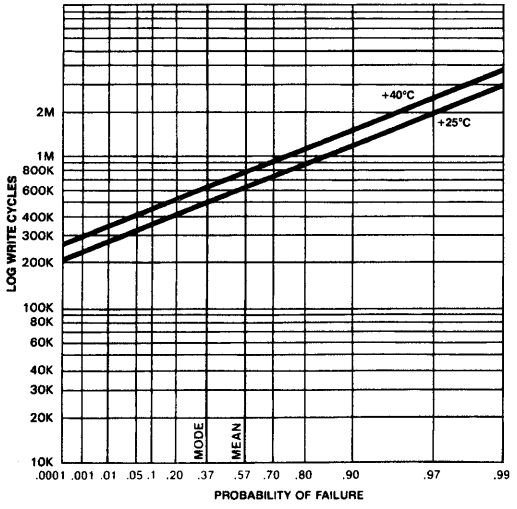

Figure 2: Affect of Ambient Temperature on Endurance

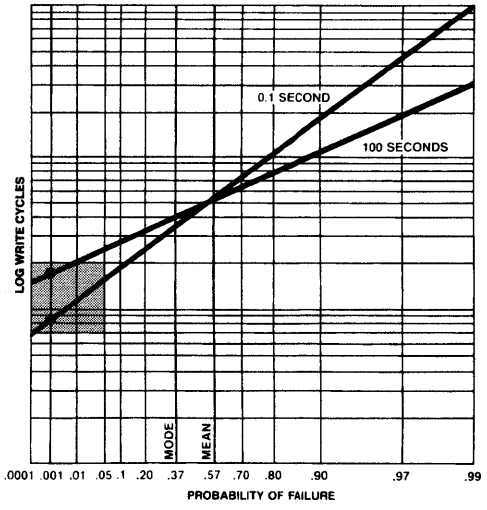

Figure 3: Affect of Write Cycle Frequency on Endurance

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9

Conclusion

This paper has illustrated two methods for determining system reliability based on endurance. In the examples given, the failure rates due to endurance are well below industry standards for semiconductor failures.

Additionally, by factoring in the affects of both temperature and frequency of writing, the endurance failure rates for the X2816A system and X2864A system may be predicted specifically for the user's application.

DEVICE RANK	THOUSANDS OF WRITE CYCLES
1	297
2	315
3	355
4	365
5	400
6	410
7	450
8	450
9	510
10	572
11	620
12	620
13	650
14	680
15	800
16	820
17	940
18	952
19	992
20	1400

Table 2: Ranked Endurance Data for Twenty Pieces of X2816A Devices

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RADIATION-INDUCED SOFT ERRORS AND FLOATING GATE MEMORIES

J. M. Caywood & Reliability Engineering Staff

ABSTRACT

A new failure mechanism which may be induced in floating gate memories by ionizing radiation is discussed. This mechanism, which is designated a "firm error", is modeled in some detail. Calculations which show that the MTBF for alpha particles emitted by ceramic packaging materials is >100,000 years are verified experimentally. The effect of device scaling on this mechanism is also discussed.

INTRODUCTION

Ionizing radiation incident on floating gate nonvolatile memories can give rise to three types of observable effects. The radiation may induce damage in the peripheral circuitry (hard errors); it may cause upset of the sense/readout circuitry (soft errors); or it may cause data loss by transfer of charge from the floating gate. The first of these groups of effects is common to all MOS circuitry and has been investigated extensively over many years.[1] The second group of effects was first observed in dynamic RAMs and has since also been observed in static RAMs and microprocessors.[2-5]

The third effect, on which this paper will concentrate, is qualitatively different than the "soft errors" which are observed in volatile RAMs. In the soft error case, thermalized carriers are collected from relatively long (~10μm) distances in the Si substrate which can result in efficient collection of the charges generated by an alpha particle (~50%)[4]. In the case to be discussed here, the carriers collected on the floating gate may come from two sources. One source is carriers created by the ionizing radiation in the SiO_2 which lies between the floating gate and another electrode or the substrate when they are at a different potential. The second source is electrons excited in the floating gate which have enough kinetic energy to surmount the potential barrier between the conduction bands in Si and SiO_2. As will be developed in this paper, these effects are relatively inefficient (<1%). Unlike soft errors which are caused by a single ionizing particle, charge transfer to a floating gate is cumulative so that effects of many ionizing events occurring over an extended period of time must be considered.

To differentiate this phenomenon from soft errors which, if they occur in floating gate memories, are dependent upon the design of the readout circuitry and are temporary read errors which can be corrected by re-reading the floating gate, and from hard errors which render all or part of the memory inoperable, we shall call it "firm error". This firm error has the operational characteristics that it causes a read error which cannot be corrected by re-reading the floating gate, but it can be corrected by re-writing the cell or cells in question to provide a completely functional memory.

MODELING THE CHARGE TRANSFER

Figure 1a shows a typical cross-section through a floating gate memory structure where the + and − signs indicate that electron-hole pairs are created along the track. Figure 1b shows a potential diagram of the same structure. Clearly electron-hole pairs created in the oxides on both sides of the floating gates will drift apart and tend to discharge the gate. Similarly electrons injected from the floating gate into either oxide will discharge the gate. The problem can therefore be broken into that of computing the charge created in the oxide and that of estimating the charge injected from the Si into the oxide.

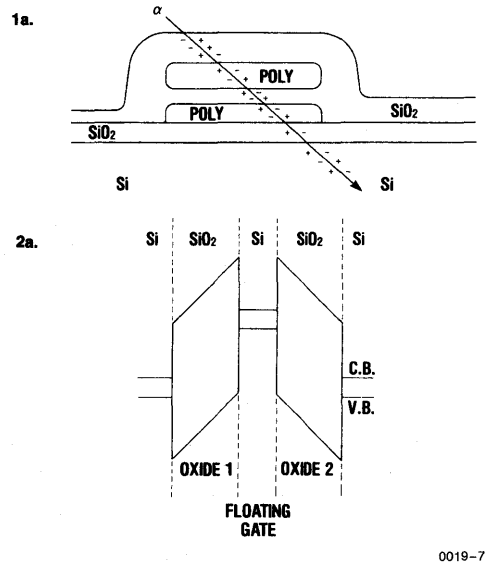

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Figure 1: Cross section and potential diagram of a typical floating gate memory transistor; a) the cross section is cut through in the direction of current flow; b) the potential diagram is shown for the case that the floating gate is programmed and the access gate grounded.

0019-1

INJECTION OF CHARGE FROM Si INTO SiO_2

Emission of excited electrons from Si into SiO_2 is a complex process. Some of the phenomena occurring are illustrated schematically in Figure 2. Hot electrons created by the ionizing particle may be scattered by acoustic or optical phonons, other electrons, or the surface itself. The requirement for electrons to reach the surface with sufficient crystal momentum, κ, normal to the surface to surmount the barrier ($\kappa_\perp^2/2m^* > \phi_B$ where $\kappa_\perp$ is the component of κ normal to the surface, m^* is the effective mass, and ϕ_B is the barrier height between the conduction bands in Si and SiO_2).[6] Phonon scattering may be considered to be elastic since the phonon energies are small with respect to the barrier height. However, an electron scattering off another electron may lose up to one-half of its kinetic energy. Hence, electron-electron scattering rapidly thermalizes hot electrons.[7] The escape length of electrons is long for energies near the fermi level but drops rapidly and forms a broad U between 20 Å and 5 Å over the energy range 10 eV to 1000 eV.[8] Escape depths of 25 Å and 12 Å are reported for electrons 5.8 eV and 11 eV above the valence band maximum, respectively.[9,10]

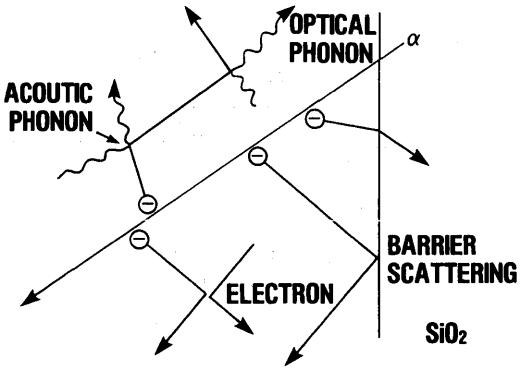

Figure 2: Schematic illustration of scattering process which contributes to small escape depth of electrons from Si.

The ideal situation would be to have electron yield curves as a function of energy for various charged particles of interest incident upon a biased oxidized silicon surface. Unfortunately, we lack such a complete data base, so we shall estimate the yields from data on optically stimulated emission. Figure 3 shows energy distribution curves (EDCs) for three photon energies plotted versus the energy of the states from which the electrons are excited for photons incident on clean Si.[11] By integrating the EDCs and dividing by the incident photon energy, the yields in terms of electrons emitted per electron volt of incident photon energy are found to be 6.7 x 10^{-4}, 8.9 x 10^{-4}, and 8.7 x 10^{-4} for photons with energies of 8.6 eV, 10.2 eV, and 11.8 eV, respectively. For lower energy photons, the yields drop precipitously.[6] It is known that the optical absorption length, $1/\alpha$, in Si is 80 Å for 12 eV photons.[12] Moreover, the electron escape depth at 11 eV is 12 Å.[10] This implies that one factor limiting the yield is that most of the electrons generated within the bulk of the Si relax via electron-electron scattering. Thus an estimate that a charged particle yields 10^{-3} electrons for every electron-volt of energy lost within 80 Å of the surface is probably an upper bound for emission from silicon into a vacuum.

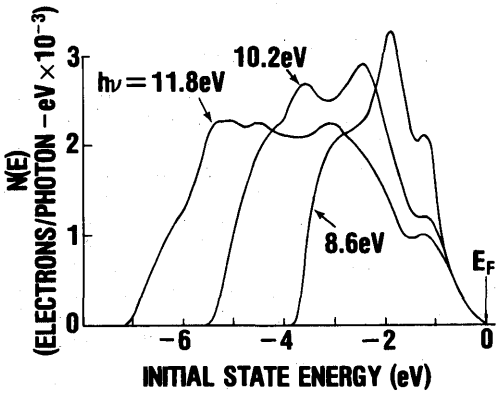

Figure 3: These energy distribution curves give electron yield vs. the energy of the initial state for photons incident on clean Si. (Data from Spicer, ref. 11).

Because the barrier between the conduction band in Si and the conduction band of SiO_2 is ~0.9 eV lower than that between the conduction band of silicon and the vacuum level, the yield in the Si/SiO_2 system should be higher than that estimated above.[6,13] The magnitude of the yield increase can be estimated two ways. Callcott measured the effect of applying 0.16 monolayer of Cs to a Si surface. He found that the vacuum barrier was lowered by 1 eV and the photon yield was increased by 2.6 times.[14] Another estimate comes from the observation that for 6 eV photons, Powell reports ~13 times higher quantum yield for the Si/SiO_2 system than does Broudy for the Si/vacuum system.[6,13] Since Powell applied a field of 3 x 10^6V/cm (~5x that present in a typical floating gate memory), the barrier between Si and SiO_2 was lowered by 0.45 eV. This implies that

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the ratio of the Powell and Broudy results is clearly an overestimate of the yield enhancement. Based on these data, we shall use 10x as a generous estimate of the magnitude of the yield increase between the Si/SiO_2 system and the Si/vacuum system. Our estimate of the yield of electrons emitted over the Si/SiO_2 barrier as a result of an incident ionizing particle is 10^{-2} electrons for each eV of energy lost within 80 Å of the Si/SiO_2 interface.

COLLECTION OF CHARGE GENERATED IN THE SiO_2

The experimental evidence for collection of charge generated within SiO_2 is much more direct than for charge injected from the Si/SiO_2 interface. Measurements of Srour, Curtis, and Chiu show that the collection efficiency of electron-hole pairs generated by 4-5 keV electrons in SiO_2 varies from very low at low fields to ~20% at 5×10^5 V/cm to ~100% at 5×10^6 V/cm.[15] From calculations based on these measurements, Ausman and McLean have deduced that one electron pair is created for each 18 eV lost in the SiO_2.[16] Since typical fields occurring in floating gate memory devices during read or storage operations are 5×10^5 V/cm, we shall assume that one pair is created for each 18 eV of energy lost in the oxide and that 20% of the charges created are collected at the electrodes.

ENERGY DEPOSITED FROM IONIZING RADIATION

Ionizing radiation can be generally separated into that involving massless particles (X-ray, Gamma-rays, etc.) and those which have mass (mesons, electrons, protons, atomic ions, etc.). The absorption cross-sections of the massless particles are quite small and decrease with increasing energy. For example, the κ_α line of Mo occurring at 20.03 keV has a mass absorption coefficient of ~$4cm^2/g$.[17] This means that approximately 1mm of Si is required to absorb 63% of the energy of a Mo X-ray beam. Since the cross-section is proportional to the cube of the wavelength, high energy photons lose even less energy per unit of length traveled through a solid. Because of this, it is expected that large fluences of X-rays would be required to transfer significant charge from the gate of floating gate memory.

For particles with mass, the stopping cross-section varies in a systematic way. This is illustrated in Figure 4 where we have plotted calculated energy loss rates in silicon for particles of differing mass using the Bethe-Bloch formalism.[18] As can be seen, for each mass particle, there is a peak in the curve of stopping power vs. energy which shifts to higher energy and becomes larger as the particle mass increases. Because of the log-log nature of the plot shown in Figure 4, it implies that there will be a high density of carriers created at the end of the particle track. This feature is called the Bragg peak.

Since the charge generation rate is maximum for particles with energies in the neighborhood of the Bragg peak, it is illuminating to calculate the charge transferred from a fairly conventional floating gate for two of the particles shown in Figure 4.

Alpha particles are known to be the chief cause of soft errors in volatile memories so their effect will be calculated. The other particle we will consider is an A1 ion, both for itself, since it may be generated as a result of muon capture by Si, and as a proxy for both the Si recoil ions which may be generated in various nuclear reactions and Mg which may also result from muon capture.[19,20]

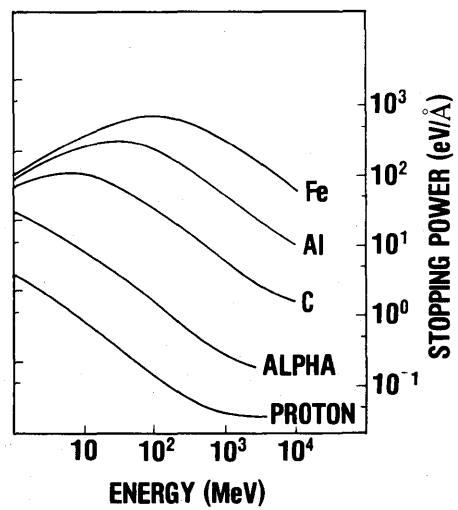

Figure 4: Energy loss rates vs. particle energy for particles with various masses calculated from Bethe-Bloch theory.

The Bragg peak for α's in Si occurs for particle energies in the neighborhood of 0.5 MeV. The energy loss rate for α's in Si is ~28 eV/Å in this range.[21] The energy loss rate for a compound such

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as SiO_2 can be found from Bragg's rule which postulates the linear additivity of the energy loss cross-sections of the constituents of the compound, viz.

$$\varepsilon(X_mY_n) = m\,\varepsilon(x) + n\varepsilon(y)$$

Applying this to SiO_2 we find that the energy loss rate for alpha particles in SiO_2 near the Bragg peak is ~10.6 eV/Å.[22] Similar calculations for Al ions give approximate loss rates of 300 eV/Å and 110 eV/Å for Si and SiO_2, respectively.

Putting all of this together in the context of Figure 1, we can see that the total charge collected per incident particle should be given by:

$$Q_p = \frac{N_{ox}(\bar{\varepsilon})}{18} \int \frac{d_{ox1}}{\cos\theta} \left(\frac{dE}{dx}\right)_{SiO_2} dp$$

$$+ Y_{Si\text{-}SiO_2} \frac{\lambda_{esc}}{\cos\theta} \int \left[\left(\frac{dE}{dx}\right)_{Si} dp + \left(\frac{dE}{dx}\right)_{Si} \right] dp$$

$$+ \frac{\eta_{ox}(\varepsilon)}{18} \int \frac{d_{ox2}}{\cos\theta} \left(\frac{dE}{dx}\right)_{SiO_2} dp$$

where η_{ox} is the field dependent collection efficiency for pairs generated in the oxide, d_{ox1} and d_{ox2} are the thicknesses of the first and second oxides, λ_{esc} is the effect escape depth for electrons generated in the Si, θ is the angle of the particle path to the normal, $Y_{Si\text{-}SiO_2}$ is the yield (for normal incidence), and the integrals over path are needed because dE/dx is a function of energy and hence position.

SAMPLE CALCULATION

As one example, let's calculate the probability of a floating gate device similar to those in current production being upset by alpha particles emanating from the packaging material. We will assume that the floating gate poly measures 5μ x 14μ x 0.4μ, that the transistor gate size is 5μ x 5μ, that the gate oxide and interpoly oxides are both 1000 Å thick and that the field oxide is 1μm thick. We also assume that there is 2μ of SiO_2 deposited after the access gate is defined.

Figure 5 shows the alpha particle spectrum measured by Meieran et al.[23] The alpha spectrum is a result of the decay change of thorium and uranium which are present in the alumina which is used for hermetic packaging as trace impurities. For simplicity of calculation, we shall approximate this spectrum as two superimposed step functions. The high energy step begins at 8.6 MeV and the lower energy step at 7 MeV, the high and low energy steps have the relative weights of 3 to 7. Since it is known that the total emission rate of alumina ranges from 0.1 to 1.0 α/cm² • hr., the integral over the approximation will be taken to be 1 α/cm² • hr.

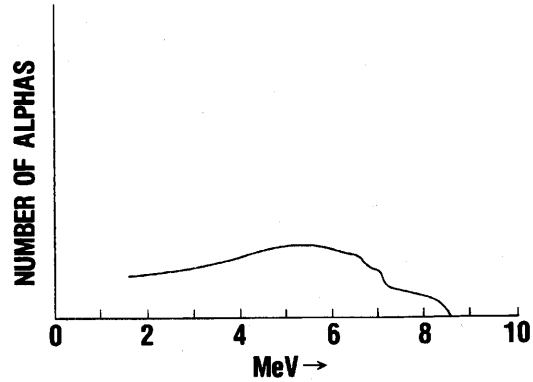

Figure 5: Spectrum of alpha particle emission rate vs. particle energy from an alumina lid. (Data from Meieran et al, ref. 23).

The maximum charge transfer which can occur as a result of a single particle is caused by a particle coming in at such an angle that the complete path length is within the gate oxide. (This requires that $\theta > 88.85°$. However, $\theta < 89.43°$ because for larger angles, the path length of the overglass is so long that no particles get through. Moreover, at $\theta = 89°$, the particle energy must be greater than 6.8 MeV to penetrate the glass.) If such a particle were to hit a cell so that 5μ of path length lay within the cell it could lose ~1.4 MeV. This implies a transfer of 15,550 electrons. The gate which is under consideration requires ~450,000 electrons to charge the state (assuming internal 2 V margin) or about 30 of these pathological alphas. Because the number of pathological alphas needed is >1, we can turn to a calculation of the average energy loss/particle.

We make the simplifying assumptions that the fraction of particles lost in the overglass from each of the two step functions contributing to the energy spectrum is given by the ratio of the path length in the overglass to the range of the highest energy particle in the step function, and that the energy loss rate in the effective charge collection region is that for 1 MeV. The first assumption causes an underestimation in the particles stopped in the overglass, and the second overestimates the energy contributed to charge generation. Under these assumptions the charge transferred from the floating gate by N_0 alpha particles is given by:

$$Q_t = 2N_0 \sum_i r_i \sum_j \ell_{ij} \left(\frac{dE}{dx}\right)_j C_j \int_0^{\theta_{max}} \frac{\sin\theta}{\cos\theta} [1 - \beta_i/\cos\theta]\, d\theta$$

0019-4

where r_i are the relative contribution of the two components in the spectrum; ℓ_j is the effective path length for charge generation; C_j is the conversion factor from energy loss to collected charges; β_i is the fraction lost in the overglass; and θ_{max} is taken to be the angle whose tangent is the gate length divided by the sum of the gate electrode and gate oxide thicknesses.

From this, one can find that the average alpha particle causes 580 electrons to be transferred from the floating gate. This means that about 750 alpha particles must hit the gate to change its state.

The problem becomes that of finding the probability that at least one cell has been hit 750 times, given that the average cell has been hit n times. Fortunately, the numbers are large enough that we can invoke the law of large numbers and approximate the distribution as normal with variance $\sqrt{n}$. If the array contains m cells then the probability that at least one cell is hit n_{crit} times is given by:

$$Q = \frac{m}{\sqrt{2\pi}} \int_z^\infty e^{-t^2/2} dt < \frac{m}{z} \sqrt{2\pi}\ e^{-z^2/2}$$

when $z = (n_{crit} - n) / \sqrt{n}$

as long as $Q<1$.[24]

If $n = 500$, then $Q < 1.84 \times 10^{-13}$ for a 16K chip and $Q<5.1 \times 10^{-12}$ for a 64K chip. For the chip size and alpha flux assumed, the expected period for the average alpha count per cell to reach 500 is 7×10^8 hours. Given the approximations we have made, this probably understates the actual time by about an order of magnitude.

Turning briefly to carriers created by Al ions, we note that very few ions have energies in excess of 3 MeV.[19] Since this energy is below the Bragg peak for Al in Si, the ions stop fairly quickly. Nonetheless, the maximum energy loss rate is ~120 eV/Å in SiO_2. Since the maximum energy of the Al ions is ~3 MeV, the maximum charge which would be collected from this ion is about 30,000 electrons which is still small enough that we can use normal statistics. Because of the small cross section for creation of these energetic ions, we can neglect this mode of charge generation for devices operating in normal terrestrial environments.

SCALING

The effect of scaling on the firm error rate on floating gate devices is interesting because it is very different from that which occurs in volatile memories. If we assume that both lateral and vertical dimensions are scaled by a factor λ, then the storage capacitance decreases as λ. However, since the charge collection is dominated by generation in the oxide, it decreases like λ^3. If the voltage margin decreases like λ, the expected time for upset increases as λ, if the voltage margin is held constant, the expected time for upset increases like λ^2. Thus, scaling should decrease the firm error rate.

EXPERIMENTAL RESULTS

To verify the theoretical results presented here, floating gate nonvolatile memories have been exposed to two types of radiation: gamma rays, representing massless particles, and alpha particles, representing massed particles. Table I gives the results. The devices tested contained a checkerboard pattern to look for firm error sensitivity for either bias of the floating gate.

As can be seen, no firm errors could be observed. The gamma radiation caused the devices to fail to meet the output leakage specification after 12,000 RAD. Measurement of the threshold of the output transistors showed that the thresholds had dropped from ~0.7V to ~0V.

The alpha particle fluence to which these devices were exposed was approximately that which would be seen after 200,000 years in a dirty package (1 $\alpha/cm^2 \cdot hr$) or 2,000,000 years in a clean (0.1 $\alpha/cm^2 \cdot hr$). These results are in good agreement with the predictions.

TABLE I

Radiation Type	Energy/ quantum	Integrated Surface Flux	#Units Tested	#Firm Errors	Part Type
Gamma Radiation	58.6 keV	12,000 RAD	10	0	X2212
Alpha Radiation	5.3 MeV	2.6×10^9 α/cm^2	5	0	X2816

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SUMMARY

The question of "firm" errors in floating gate nonvolatile memories has been treated. A firm error is defined as a change of data occurring as the result of transfer of charge from the floating gate by ionizing radiation. The rate of charge transport by various forms of ionizing radiation is discussed. The case of alpha particles is worked out in some detail as an example. Experimental results of exposure of units to gamma and alpha radiation are shown which support the theoretical predictions. The units in test survived exposure to 12,000 RADs and 2.6×10^9 α/cm^2 without firm errors. The alpha fluence is equivalent to that emitted by a typical ceramic package in about a million years.

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0019-6

ENDURANCE MODEL FOR TEXTURED POLY FLOATING GATE MEMORIES

H.A. Richard Wegener

ABSTRACT

Textured Poly Floating Gate (TPFG) memories are beginning to dominate the commercial market. This is due to many of its inherent strengths. One of these is the consistency of its endurance. Its predictability is here developed theoretically. Starting with a model of emission from bumps based on the radial solutions of LaPlace's and Poisson's equation in spherical coordinates and the use of an Extreme Value distribution for the bump radii, an expression for charge build-up at constant current fits experimental data very well. This charge build-up is proportional to fluence. When these results are used in a model for continuous data changes, an expression is developed that relates endurance exponentially to a ratio of internal voltages.

INTRODUCTION

The basic features of the TPFG technology have been described in previous publications (1-4). The action of three polysilicon levels in charging and discharging the floating gate is shown in Figure 1.

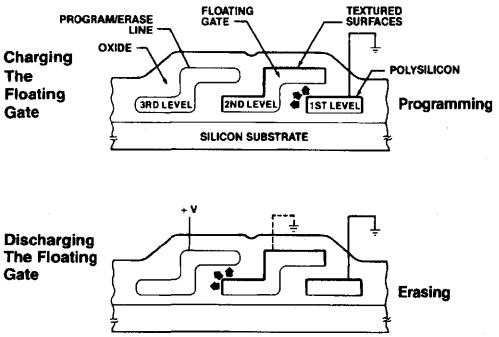

Figure 1: TPFG Cell Operation

Electron emission occurs only from a lower poly layer towards an upper poly layer. The oxide layers in between are in the 55 to 75 nm range, compared to the 8 to 11 nm required for the other common floating gate technology. The reason is simple: the surfaces of the poly layers are textured to form many small bump-like features, whose curved surfaces enhance applied fields by factors of 4 to 5. The modeling of these fields is an important part of the analysis to follow.

ENDURANCE

The term endurance has become accepted for a property common to all current nonvolatile memory technologies. It describes the number of data changes that a memory device can sustain without failure. In MNOS technologies, the failure is sometimes an inability to maintain the memory state for the required retention time; in thin oxide floating gate technologies it is often the breakdown of the fragile dielectric. In the TPFG technology, the end of endurance is generally caused by "trap-up", which prevents the transfer of charge to the floating gate. Trap-up is caused by the accumulation of trapped negative charge in the dielectric due to the repeated passage of current. These charges create a potential that opposes the potential necessary for tunneling. When this opposing potential reaches the voltage supplied on the chip, tunneling can no longer occur, resulting in the end of endurance. This paper describes a model for trapped charge build-up in TPFG devices.

FIELD MODEL

Electron emission by Fowler-Nordheim tunneling requires the knowledge of the field at the surface of the bump. This model assumes a bump with a spherical tip, which permits the use of solutions of LaPlace's and Poisson's equations in spherical coordinates. It is further assumed that the emitting surface (cathode) is radially conformal with the collecting electrode (anode), so that only the radial parts of both equations need to be employed. This leads to a solution of the form

$$(1)\quad E_c = -V_c/[R_c(1-R_c/R_a)] + (\sigma/K)\, R_d\, (1-R_d/R_a)/[R_c\,(1-R_c/R_a)]$$

where E is the field, R the radius, K the dielectric permittivity, σ a charge density per unit area, subscript c denotes a quantity at the cathode, and subscript a is a quantity at the anode. The first term describes the field in a dielectric free of charge, and the second has been cast in a form that the trapped charge distribution can be described by its charge density σ located at the centroid radius R_d.

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FORMALISM FOR TRAP GENERATION

There is a body of experimental data for parallel plate structures (5,6) that clearly indicates that the amount of trapped charge is proportional to the amount of charge that has passed through as current:

(2) $Q_t = b \{\int J\, dt\} (4 \pi R^2_c)$ (s/4)

where Q_t is the charge trapped, and $\int J\, dt$ is the current density that passed through the dielectric integrated over time (termed "fluence"). The quantity b is the ratio of trapped charge to fluence. The second bracket converts charge density into charge, and (s/4) is the fraction of a full sphere that actually emits electrons. When this charge is concentrated at the centroid raduis R_d, then

(3) $Q_d = (\sigma) (4 \pi R^2_d)$ (s/4)

Equating Q_t with Q_d, solving for σ, substituting into eq (1), identifying the denominator of the second term of eq (1) as V_Q, and approximating R_d with $R_a/2$ results in

(4) $V_Q = \{\int J\, dt\} (b/K) (R^2_c/R_a)$

FORMALISM FOR VARIATION OF BUMP SHAPES

All of the preceding derivations require two perfect concentric spherical shells to be applicable. To account for deviations from sphericity, and the distribution in the sizes of real bumps, as many as four constants might be necessary. But as a first approach it was decided to view the bumps as a distribution of perfectly spherical surfaces of limited area, with the hope that the dispersion parameter of the distribution of spherical radii would absorb the effects of contour variations. The distribution chosen was the Extreme Value distribution (7-9). Its sampling function has the form (10)

(5) $R_{ci} = R_m - BB\{\log [-\log (i - 0.5) /k]\}$

where R_m is the radius at the maximum of the distribution (the mode), BB is the dispersion parameter, k is the number of samples chosen, and i is the rank number of the particular item of k samples chosen.

CONSTANT CURRENT CHARACTERISTICS OF "TPFG" MEMORY TEST STRUCTURES

TPFG memory devices are operated by linear voltage ramps, which result in a forced constant current through the dielectric. A useful concept in this mode of operation is the "tunnel voltage" V_{TU}, which is the voltage that must be applied to sustain a specific constant current. For purposes of characterization, simple test structures are subjected to a set of forced constant currents, and the tunnel voltage V_{TU} is recorded vs fluence. Such a characteristic is shown in Figure 2.

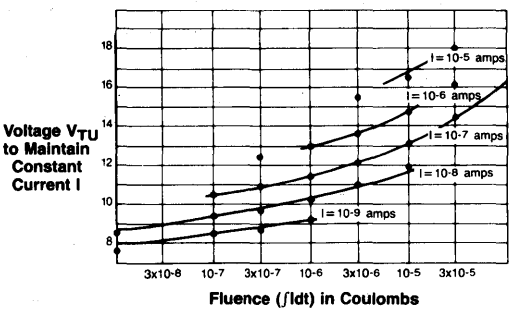

Figure 2: Tunnel Voltage vs. Fluence at Constant Current. Lines are experimental data, solid circles are calculated from eq (8).

With representative bump radii chosen by the sampling function the field at bump i is

(6) $E_{ci} = [-V_{TUi} + V_{Qi}]/[R_{ci} (1-R_{ci}/R_{ai})]$, where

(7) $V_{Qi} = \{\Sigma J_{FNi} \Delta t\} (b/K) (R^2_{ci}/R_{ai})$.

Fluence is now expressed by its sum over time increments. The measured current is the sum of the currents from the number of all individual bumps G. The current density emitted by tunneling must be multiplied by the active spherical surface area. This leads to

(8) $I = (G/k) \sum_{i=1}^{k} (4 \pi R^2_{ci})$ (s/4) J_{FNi}, where

(9) $J_{FNi} = A E^2_{ci} \exp -B/E_{ci}$.

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The initial modeling was done with a program in BASIC on a personal computer. The area of the structure was 0.1mm^2, the number of bumps per square micrometer was 50, the oxide thickness was 59 nm, which translated into a value for $R_{ai}=R_{ci}$ + 59 nm. Following (11) the Fowler-Nordheim constants were set at A=6.5E-7 amps - cm/V^2 - sec and B=2.52E + 8V/cm. The dielectric permittivity was K=3.5E-13. The best fit was obtained for R_m=15.4 nm, BB=4.8 nm, b-2.OE-8, and s=0.03. The calculated values are shown as circles against the continuous experimental data on Figure 2. The value R_m is consistent with values obtained from T.E.M. cross-sections, the calculated dispersion has an analog in the estimated dispersion of bump base diameters, and b agrees very well with data presented at IEDM81 (6) for parallel plate structures. There is now a good basis for describing the processes occurring in TPFG memories. A pertinent example is shown in Figure 3. Here a constant current plot was calculated as a function of the number of samples representing the same distribution. While it is an indication that, indeed, 1024 samples are necessary to accurately depict conduction at fluences as low as 1E-8, it also clearly shows that during the latter part of the life of the devices, all those different bumps can be represented by bumps of the same radius R_m. This should make the prediction of endurance somewhat less complex.

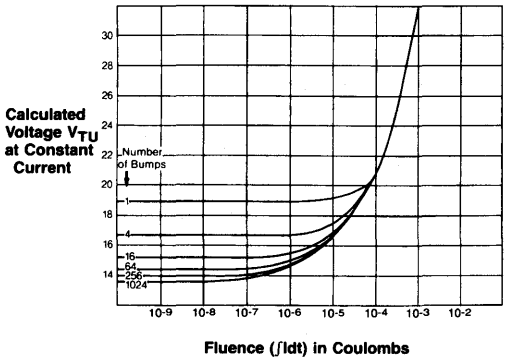

Figure 3: Effect of Number of Samples k on Calculated Tunnel Voltage

VOLTAGE-TIME RELATIONSHIPS DURING PROGRAM-ERASE CYCLING

This analysis is based on the assertion that trap-up is the cause of the end of endurance. Since the build-up of traps is the result of current through the tunnel dielectric, this analysis is concerned only with the time interval during which tunneling occurs. As an aid to understanding, reference may be made to Figure 4.

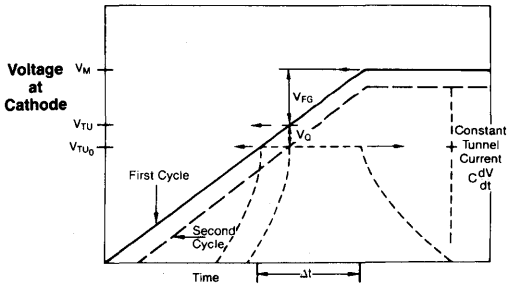

Figure 4: Voltage vs. Time Relationships at Floating Gate

The heavy line describes the (absolute) potential at the cathode (which may be poly 1 or poly 2) during the course of the first ramp to be applied to an untested structure. When the tunnel voltage V_{TUo} is reached, a current flows that remains constant until the maximum voltage (internal to the tunnel structure) V_M, is reached. The constant current is indicated by a superimposed plot in broken lines referenced to the right. When V_M is reached, the voltage stays constant for a "flat top" period. During this time, the current decreases exponentially, since any transferred charge reduces the tunnel potential. Since tunnel current flows during this first pulse, its fluence gives rise to trapped charge, which in turn causes an opposing voltage V_Q. Therefore, during the second pulse, the net potential on the cathode is reduced by V_Q. This can be indicated by a second ramp offset downwards by V_Q. The tunnel voltage for the same constant current is then reached later, and the time to reach the end of the ramp is shorter. As cycling proceeds, the time interval during which tunneling occurs becomes shorter and shorter. This simple picture neglects one important element of endurance cycling: each cycle of one polarity must be followed by a cycle of the opposite polarity. The charge stored during the previous cycle affects the

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potential of the cathode during the following cycle. The amount of charge stored during each cycle can be picked off Figure 4 by looking at it in another way. Instead of offsetting all succeeding ramps, one may consider them all superimposed, and recognize that the tunnel voltage V_{TU} increases with each cycle. Then the tunnel voltage can be viewed as the sum of V_{TUo} and V_Q. Conversely, the charge transferred to the floating gate V_{FG} is the difference between V_M and V_{TU}.

ENDURANCE MODEL

The change in V_{TU} per programming pulse on one bump is

(10) $d\,V_{TU}/dn = \Delta V_Q = \{J_{FN}\,\Delta t\}\,(b/K)\,(R^2_c/R_a)$

where Δt is the total time during which current flows.

(11) $\Delta t = (V_{FGe} + V_{FTe} + V_{Mp} - V_{TUp} + V_{FTp})/r$,

where r is the ramp rate dV/dt, subscript p refers to the programming step, and e to the erase step. $V_{FGe} + V_{FTe}$ is the floating gate voltage left over from the erase step. V_{FTp} is the charge added to V_{FGp} during flat top. From previous analysis, $V_{FGe} = V_{Me} - V_{TUe} + V_{FTe}$. Let the structure be symmetrical so that all subscripts are interchangeable. Eq (11) be can now be written

(12) $dV_{TU}/d\,n = \alpha(V_M - V_{TU} + V_{FT})$ where

(13) $\alpha = 2b\,J_{FN}\,R^2_c/K\,r\,R_a$

Integrating (12), setting $V_{TU} = V_{TUo}$ when n=0, setting $V_M - V_{TU} + V_{FT} = V_{MS}$ when n = N, and rearranging, results in

(14) $N = (1/\alpha)\,[1n\,(V_M + V_{FT} - V_{TUo})/V_{MS}]$.

Here N is endurance expressed as the number of data changes before trap-up, and V_{MS} is the minimum voltage on the floating gate to be sensed as the correct state.

Near the end of endurance, according to Figure 3, after a fluence of about 1E-4 coulombs has been accumulated, the build-up of traps follows a path as if all bumps had the same radius R_m. This permits the exact substitution for R_c and R_a in Eq (13), and the calculation of V_{TUo} in Eq (14) with the help of Eq (9). V_{FT} can be calculated exactly, depending on flat top time and floating gate capacitance; it is of the order of 0.1-0.3 volts. V_M depends strictly on internal voltages and coupling ratios. V_{MS} depends on coupling ratios, the threshold voltage of the floating gate transistor, the minimum voltage required to accomplish sensing at the circuit sensing device. Memory cells operating within real circuits require the establishment of both programming and erase voltage quantities to fit in Eq (14). Endurance distributions as a function of temperature have been recorded experimentally for specific TPFG products (12). Their modes are consistent with tunneling currents as determined from the measured ramp rates in circuits operating at different temperatures.

CONCLUSION

There are three major results of this calculation. First, it indicates that textured surface emission can be modeled adequately by spherical geometrics, if modified by the dispersion of an Extreme Value distribution of the bump radii. Second, it confirms that TPFG memories are a part of the same universe as other silicon-to-silicon-dioxide tunneling structures, exhibiting the same mode of trapping (proportional to fluence), with a trapping ratio (b=2E-8) that is essentially identical to that for parallel plate structures. Finally, on the basis of these results, a model for TPFG endurance based on charge build-up has been developed that appears well supported by experimental results.

ACKNOWLEDGEMENTS

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NOTES

THE PREDICTION OF TEXTURED POLY FLOATING GATE MEMORY ENDURANCE

By H.A. Richard Wegener &
Daniel C. Guterman

BACKGROUND

The Textured Poly Floating Gate (TPFG) memory is one of the three major nonvolatile semiconductor memories currently in use. Details of its device theory and its use have appeared in previous publications.[1–4] Its nonvolatile memory cell employs three layers of polysilicon as shown in Figure 1. The most important feature of this cell is its ability to transfer electrons to and from the floating gate through oxide thicknesses of the order of 55 nm to 75 nm, in contrast to other nonvolatile memory technologies that must have dielectrics as thin as 10 nm surrounding their floating gate. The thick dielectric in the TPFG memory cell has proven its advantage in manufacturability and reliability. This advantage is made possible by the presence of a textured surface, whose curved features generate a field enhancement that permits Fowler-Nordheim emission at reasonable voltages. These features have the shape of bumps on the poly surface. The modeling of emission from these surfaces formed the major part of a recent paper.[5] Its results were that these bumps can be approximated by spherical caps on the tip of truncated cones, so that the fields can be found using Laplace's equation in spherical coordinates. From S.E.Ms and T.E.Ms these bumps were known to have a range of sizes. It was found that a simple two-parameter Extreme Value distribution of the cap radii was a sufficient description to get a good fit of model and experimental data over five orders of magnitude of constant current, and eight orders of magnitude of fluence.[5]

ENDURANCE

Endurance is a characteristic common to all current nonvolatile semiconductor memory technologies. It describes the number of program-erase cycles that a memory device can sustain without

FLOATING GATE STRUCTURE

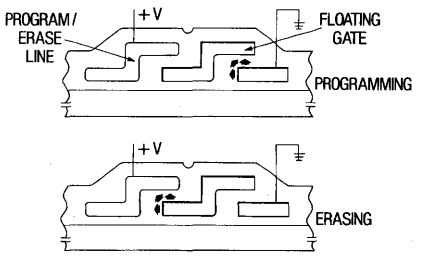

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Figure 1: The nonvolatile part of a NOVRAM cell is shown schematically with the permanently grounded poly 1 at right, the floating gate formed by poly 2 in the middle, and poly 3, also serving as the program/erase line, at the left. To program, poly 2 is coupled capacitively to a positive potential; this results in strong coupling of the floating gate to poly 3, and a high potential between poly 1 and 2. To erase, poly 2 is coupled capacitively to ground; this results in a high potential between the floating gate and poly 3.*

failure. In other nonvolatile technologies, the failure modes may involve dielectric breakdown or loss of retention. In TPFG memories, failure is particularly graceful: The addressed bit cannot respond sufficiently to a data change. This is due to the fact that in this technology, the end of endurance is caused by trap-up. Trap-up is the result of the accumulation of trapped negative charge in the dielectric that is caused by the repeated passage of current. The endurance limit is reached when the potential due to this trapped charge grows so large that it suppresses the Fowler-Nordheim tunneling to the extent that insufficient charge is transferred to change the state of the floating gate. The modeling of endurance then simply involves the modeling of the build-up of the negative charge as a function of the number of pulses of Fowler-Nordheim current through the dielectric.

DESCRIPTION OF ENDURANCE MODEL

A first step is the derivation of the voltage V_Q, which is the voltage due to the trapped charge that opposed the voltage necessary for tunneling V_{TU}. The spherical cap model permits the use of Poisson's equation in spherical coordinates. As shown in reference (5), V_Q is calculated for a charge density defined by a spherical shell with a centroid radius R_d. An educated guess approximates R_d with one half of the anode radius R_a. The

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*NOVRAM is Xicor's nonvolatile static RAM device.

generation of charge density, following the results of previous workers [6,7] is made proportional to fluence (the time integral of current density $\int Jdt$) by the trapping ratio b. This results in

$$V_Q = [\int Jdt]\ (b/K)\ (R^2_c/R_a) \quad (1)$$

where K is the dielectric permittivity, and R_c the radius of the (emitting) cathode surface.

Inspection of Figure 2 will help in understanding what happens during a single (erase) pulse. The ordinate shows the voltage on the program/erase electrode, the abscissa the time during a pulse. The voltage changes linearly with time as shown, at a ramp rate r = dV/dt. This ramp rate is proportional to the current put out by the charge pump on the chip. As the voltage between floating gate and program/erase electrode increases, a voltage V_{TU} is reached where Fowler-Nordheim tunneling is initiated. The tunneling current is exactly r × C_{FG}, where C_{FG} is the capacitance of the floating gate. Since the pump current is constant, V_{TU} will be clamped at a value that keeps the tunnel current constant, but the voltage due to the charge transferred to the floating gate, V_{FG}, will rise until the ramp is limited at a maximum voltage V_M. At this point, the tunnel current will fall off rapidly, since any charge transferred will reduce the potential between floating gate and program/erase electrode. In the following analysis, the charge transferred after V_M is reached will be set to zero. The time, Δt, during which constant current flows through the dielectric is defined by the tunnel voltage V_{TU} at the beginning, and V_M at the end. During this time, electrons will be trapped in the dielectric, in proportion to the fluence J × Δt.

The next pulse will therefore encounter an increased opposing potential ΔV_Q, because of the trapped charge generated during the preceding pulse. The ramp voltage at which tunneling starts is now increased by this voltage, the net charge transferred to the floating gate is decreased, and the time Δt during which constant current flows is also decreased. During endurance cycling, the polarities of the pulses are alternated, so that an erase is followed by a program pulse. The (program) ramp following an erase pulse now encounters a potential due to charge transferred during the preceding pulse. This potential adds to that of the new ramp, so that the tunnel voltage is reached sooner, and constant current flows longer until V_M is reached. In fact, if the structure is symmetrical for both program and erase conditions, the time during which constant current flows is exactly twice that for a single ramp starting with zero charge on the floating gate.

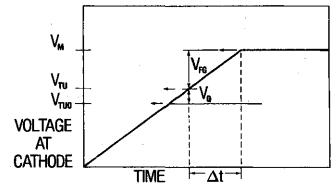

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Figure 2: The voltage at the floating gate as a function of time is shown for one particular erase pulse. The voltage (due to displacement) changes linearly with time until the tunnel voltage V_{TU} is reached. Tunneling at constant current clamps the voltage at that value, resulting in a voltage ΔV_{FG} due to charge transfer. The trapped charge due to previous erase cycles gives rise to an opposing potential V_Q.

MATHEMATICAL MODEL OF SINGLE CELL ENDURANCE

For the purpose of analysis, the floating gate is considered a mosaic of pieces, each containing one emitting bump of cathode radius R_{ci}. All quantities with subscript i refer to one such representative piece. Setting the tunnel voltage at V_{TUO} when no charge exists in the dielectric:

$$V_M - V_{TUOi} = V_{Qi} + V_{FGi} \quad (2)$$

$$\Delta t_i = V_{FGi}/r = (V_M - V_{TUOi} - V_{Qi})/r \quad (3)$$

From Eq(1), the trapped charge in the dielectric after an erase and a program pulse is

$$\Delta Q_i = 2\ (b/K)\ (R_{ci}^2/R_{ai})\ J_{FNi}\Delta t_i \quad (4)$$

This can be expressed as the rate of charge trapping per program/erase cycle n:

$$dV_{Qi}/dn = \alpha_i\ (V_M - V_{TUOi} - V_{Qi}),\ \text{where} \quad (5)$$

$$\alpha_i = 2\ (b/K)(R_{ci}^2/R_{ai})\ J_{FNi}/r \quad (6)$$

Integrating Eq(5), and setting V_{Qi} equal to zero at n = 0, results in

$$\ln\ [(V_M - V_{TUOi})/(V_M - V_{TUOi} - V_{Qi})] = \alpha_i n \quad (7)$$

Substituting Eq(2) into Eq(7) and solving for V_{FGi}

$$V_{FGi} = (V_M - V_{TUOi})\ \exp\ (-\alpha_i n) \quad (8)$$

The transition from the individual bump mosaic pieces to the full floating gate comes from the argument that the floating gate voltage is really the sum of the charge contributions Q_i from small amounts of current I_i emitted by all bumps, divided by the floating gate capacitance C_{FG}:

$$V_{FG} = \Sigma Q_i/C_{FG} = [\Sigma I_i \Delta t_i]/C_{FG} \quad (9)$$

$$I_i = 4\pi\ R_{ci}^2\ (s/4)\ J_{FNi}, \quad (10)$$

the Fowler-Nordheim J_{FNi} current is

$$J_{FNi} = A\ E_{ci}^2 \exp(-B/E_{ci}), \quad (11)$$

the field at the emitting bump is

$$E_{ci} = (-V_{TUi} + V_{Qi})/R_{ci}[1 - (R_{ci}/R_{ai})] \quad (12)$$

the cathode radius

$$R_{ci} = R_M - BB\ [\ln - \ln(i - 0.5)/G] \quad (13)$$

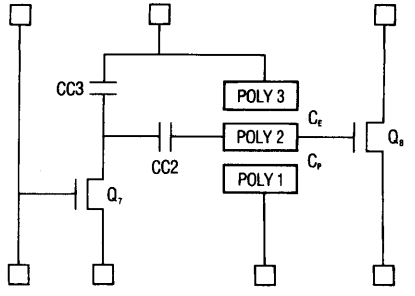
Summing all bumps i from 1 to the total number of bumps G results in the complete expression for the dependence of the floating gate voltage due to tunneled electrons V_{FG}, on the number of endurance cycles n:

$$V_{FG} = (1/r\,C_{FG})\ \Sigma 4\pi\ R_{ci}^2\ (s/4)\ J_{FNi} \times (V_M - V_{TUOi}) \exp(-\alpha_i n) \quad (14)$$

The quantities after J_{FNi} are the result of replacing Δt_i in Eq(9) by Eqs(3) and (8). It now remains to define the end of endurance. Clearly, it arrives when the floating gate voltage is insufficient to establish the required logic level. The end of single cell endurance ($n = N_c$) occurs when the floating gate voltage reaches a defined value ($V_{FG} = V_{FGM}$) that is the boundary of that level.

SINGLE CELL ENDURANCE DATA

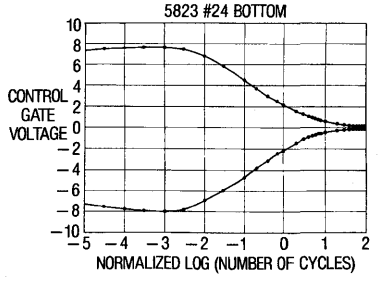
The test pattern used to characterize endurance is the nonvolatile part of a Xicor NOVRAM cell shown in Figure 3. The dimensions of the test cell are identical to those in a NOVRAM memory array. The advantage of this cell is that all voltages can be applied directly to this cell. Cycling is achieved by applying a ramp between ground and V_M. V_{FG} is read out by applying the same control voltage sweep simultaneously to ground, V_M and P/E control. This couples to the floating gate and when a voltage equal and opposite to V_{FG} is reached, the (floating) gate on the sense transistor will indicate zero charge. Upon increasing the control voltage sufficiently the floating gate potential is increased by the threshold voltage of the transistor, turning on the sense line. This value of the control gate is then recorded, generating the plot shown in Figure 4. The ordinate shows the value of the control voltage necessary to turn on the sense transistor. Since V_{FG} is positive in the erase state, a negative control voltage must be applied. Therefore, the lower branch of the window plot represents the erase state. When V_{FG} approaches the threshold voltage of the transistor, its reaction becomes indeterminate, and the limit of the endurance of the cell is reached. ($n = N_c$ when $V_{FG} = V_T$). This situation is indicated when the applied control voltage is exactly zero. Inspection of Figure 4 shows that the end of the endurance for that particular cell occurred at a number of cycles normalized to a value of 100. The same factor of normalization was applied to all data quoted here in order to prevent possible confusion with results from individual products, or with published specifications.



0021-3

Figure 3: This shows the circuit schematic of the nonvolatile part of a NOVRAM cell. Two transistors are shown in addition to the elements in Figure 1. Transistor Q_7 controls the access to the junction used for capacitive steering of write and erase operations, and transistor Q_8 senses the voltage on the floating gate. V_{FG} can be measured by turning Q_7 on hard, and finding the control voltage that must be supplied simultaneously to poly 1, poly 3, and capacitor CC2, in order to cause a specified current to pass through Q_8.

NOVRAM CELL ENDURANCE DATA



0021-4

Figure 4: This is a plot of the charge transferred to the floating gate of a single NOVRAM cell as a function of the logarithm of the number of program/erase cycles. The actual floating gate voltage is the negative value of the control voltage minus the threshold voltage of Q_8.

RELATIONSHIP OF SINGLE CELL DATA TO LOT ENDURANCE

The number of program-erase cycles at a control voltage of zero was determined for a number of single cell structures from the same wafer lot. The results were plotted on log normal probability paper.

9

The results can be seen on Figure 5. Careful reading of the abscissa will establish its relationship with the usual chart. In effect, the scale has been extended on the low probability side of the distribution, and for simplicity of notation, the cumulative probabilities have been marked as their base ten logarithms. In a few selected locations near the right hand side, the equivalent percentage values were given in brackets. The single cell data points are on either side of the 50% line of the chart. The slope of the best fit straight line defines the dispersion of the distribution.

RELATIONSHIP OF SINGLE CELL DATA TO LOT ENDURANCE

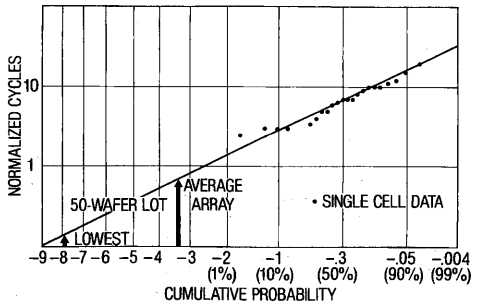


Figure 5: This shows the Log Normal probability plot of individual single cell endurance data. The right half of the plot is quite standard, as marked by typical cumulative percentages. The left half represents an extension of the standard chart to much lower probabilities, in order to permit predictions for specific members of a much larger population.

In order to relate these results to the endurance of a commercial lot of NOVRAMs, the definition of the endurance of an integrated circuit with an array of memory cells should be recalled. This definition states that the limit of the endurance of a chip is reached when the first cell fails, after having sustained the same number of data changes as every other cell on that chip. If that chip has 1024 memory cells, then the cell with the lowest endurance limit of these 1024 cells defines the endurance of that chip. The cumulative probability for this is 1/1024. Any chip with 1024 cells can be expected to have that endurance. The number of cycles at the cumulative probability of 1/1024 therefore represents the average endurance of a chip from a given lot. The lowest endurance on a wafer of chips is caused by the cell with the lowest endurance on that wafer. If there are, say, 850 chips per wafer, then the cumulative probability of this endurance limit is 1/(1024 $\times$ 850). Looking now at a full 50 wafer lot, the lowest endurance of that lot has a cumulative probability of 1/(1024 $\times$ 850 $\times$ 50). The plotting of ranked data on probability paper requires "plotting positions" that result in about half the calculated cumulative probability values[8] for the lowest value used. In order to be consistent with the plotted data points, the cumulative probability for the average chip endurance from the 50 wafer lot is 0.0005, and this is indicated by an arrow of Figure 5. Similarly, the lowest possible chip endurance on that wafer lot is 1E−8.

COMPARISON OF SINGLE CELL PROJECTION WITH COMMERCIAL LOT DATA

The endurance of individual arrays from a commercial lot can be described by a statistical distribution and its parameters. Since the endurance of an array is determined by the lowest endurance of a fixed number of cells, an Extreme Value distribution describes the distribution of the lowest endurances of all the arrays, and therefore, of the arrays within a lot.[9] This applies regardless of the distribution of the endurances of individual cells within the same array. It is an empirical fact that it is the logarithm of the number of cycles that has the Extreme Value distribution,[10] very similar to the Log Normal distribution frequently found for data from electronic devices. Lot data can be handled simply by the use of Extreme Value probability paper. Available charts are designed for maximum extreme values. For minimum extreme values, such as the lowest endurance of an array, these charts can be used by substituting the complement for the cumulative probability of an observation in order to determine the plotting position. Instead of ϕ, $(1 - \phi)$ is used to determine the abscissa. Figure 6 is based on these considerations.

The abscissa is labeled by the complement values, which results in the reversal of the slopes of the straight line describing the distribution. The ordinate is (just as Figure 4) in terms of the logarithm of the normalized endurance. Since the distribution is described by a straight line in this coordinate system, it requires only two points to define its locus. These two points were determined in the previous section: the endurance of the average array, and the minimum endurance of the lot. The difference from Figure 5 (aside from the distribution function) is that the definitions of the cumulative probability values have changed. In terms of an individual cell, the cumulative probability of the endurance of an array is related to 1/1024; in terms of the array, the cumulative probability is the expected average of individual array units. For the (maximum) Extreme Value distribution this is 0.57; since the shape of the

distribution has not changed, the use of the complement does not apply and the value of the (log of) endurance on Figure 5 at the larger arrow is entered on Figure 6 at $\phi = 0.57$. Similarly, the minimum endurance of an array from a 50 wafer lot is now associated with a cumulative probability of $0.5/(50 \times 850)$ a value increased by a factor of 1024 over the corresponding single cell value (see preceding section). The cumulative probability for the minimum (array) endurance of a lot is therefore 1.2E−5, to be plotted at the 0.99999 position. A straight line drawn through this point and the array average establishes the projected distribution of array endurances. This graphical technique of deriving lot endurances from single cell data will be supplemented by an equivalent mathematical approach in the Appendix.

How good is the fit to actual data? Endurances from a typical monitor of that general time slot in NOVRAM production are shown on Figure 6. The fit is not fortuitous: there are dozens of lot data with almost identical slopes over a range of roughly a factor of 0.5 to 2. Confidence limits (95%) from the single cell data permit a scatter twice as large.

ENDURANCE FROM SINGLE CELL VS. COMMERCIAL LOT DATA

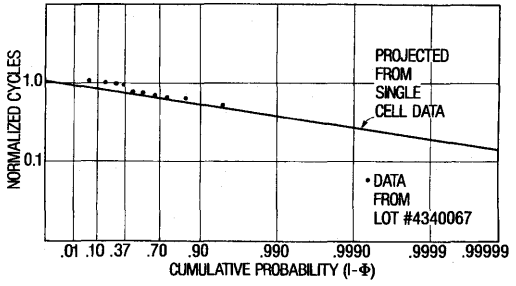


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Figure 6: This is a Log Extreme Value probability plot of the endurance of a lot of X2212 NOVRAMs. The points are measured values, the straight line represents endurances predicted from the single cell data shown in Figure 5.

CONSTANT CURRENT TESTING

The determination of endurance is a very time consuming process. In single cell data taking, typically tens to hundreds of millions of cycles are required. This routinely takes on the order of days to accomplish. For product endurance prediction, about twenty cells are needed, requiring simultaneous testing for any semblance of monitoring efficiency. A much more rapid method of evaluation has been in use for some time. It depends on the observation of the time necessary to reach some predetermined tunnel voltage, when a constant current is forced through the test structure. An empirical factor correlates observed time with observed product endurance. Test times are on the order of ten to ten thousand seconds, depending on conditions used. Inspection of Eq(8) explains the reason for this. The time Δt during which constant current flows is proportional to V_{FG} (Eq(3)). It is therefore exponentially decreasing with the number of write-erase cycles. Since the data ramp takes the same amount of time, whether current flows through the dielectric or not, the time consumed increases linearly with the number of cycles, while the limiting process decreases exponentially. A constant current test adds the periods of current flow without pauses, reaching the condition for the trap-up limit of endurance in a minimum of time.

MATHEMATICAL RELATIONSHIP BETWEEN ENDURANCE AND CONSTANT CURRENT DATA

The work described in reference (5) proved that the constant current data can be modeled by bumps whose size have the proper distribution. Since this requires the addition of the contributions of thousands of bumps, the number of different bump radii necessary for a good fit was studied. It was found that at low fluences, a large number was necessary, but after a sufficient amount of charge has passed through the dielectric, the contributions from different bumps had nearly equalized, so that only a few bump radii were a sufficient description. After high fluences, a single bump, representative of the maximum of the distribution of radii, could predict the tunnel voltage necessary to maintain a constant forced current. Since the end of endurance is brought about by high tunnel voltages after large fluences, this condition applies very well and is used in the following analysis. When, in Eq(14), R_{ci} is replaced by R_M, the summation sign is replaced by a multiplication by G. Then the factor to the left of, and including, J_{FNi} becomes $I/(r \times C_{FG})$. But $I = r \times C_{FG}$, so that, when R_{ci} becomes R_M,

$$N_C = (1/\alpha_M) \ln[(V_M - V_{TUOM})/V_{FGM}] \qquad (15)$$

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Substituting $r \times \Delta t$ (see Eq(3)) for the voltage term in parentheses in Eq(5), multiplying by dn and integrating results in

$$\int dV_{Qi} = \alpha_i r \int \Delta t_i dn \quad (16)$$

The integral of Δt with respect to the number of cycles is, of course the total time of constant current flow through the dielectric. At the endurance limit, $V_{Qfi} = V_M - V_{TUOi} - V_{FGMi}$, and the integral of time intervals is equal to the total time of constant current flow to the instant of the end of endurance, t_{Ni}. Again invoking the asymptotic limit of all R_{ci}'s becoming R_M,

$$t_N = (V_M - V_{TUOM} - V_{FGM})/r\,\alpha_M \quad (17)$$

Solving Eq(17) for α_M and substituting in Eq(15) results in the expression for endurance as calculated from constant current data

$$N_C = [r\,t_N/(V_M - V_{TUOM} - V_{FMG})] \times \ln[(V_M - V_{TUOM})/V_{FGM}] \quad (18)$$

Conversely, the elapsed time at constant current t_N equivalent to endurance N_C is obtained by interchanging those two quantities in Eq(18). An estimate of the time advantage is obtained by realizing that in cycling, a minimum time of $2 \times V_M/r$ is consumed per cycle. Since typically, some time, both analog and digital, is spent in the transition from programming to erasing, this minimum time is doubled.

Therefore the elapsed time to reach the end of endurance by cycling t_{CC}, is closer to

$$t_{CC} = 4\,N_C\,V_M/r \quad (19)$$

Substituting pertinent values, one can find that t_N is approximately $t_{CC}/50$.

EXPERIMENTAL CORRELATION OF CONSTANT CURRENT WITH CYCLING DATA

Textured poly capacitor test patterns from the same wafers that had been used to obtain the single cell cycling data displayed in Figure 5 were subjected to forced constant current conditions, and their tunnel voltages were recorded as a function of time. An automated test system exists to perform this test on a routine basis. When tunnel voltage was plotted vs time, the data for ten such structures resulted in Figure 7. According to Eq(17), when $V_{Qf} = V_{TU} - V_{TUO} = V_M - V_{TUO} - V_{FGM}$, then the end of endurance is reached. This condition is indicated by the horizontal line at that voltage. The time t_N to reach that can be read off the graph and converted into equivalent cycles by Eq(18). These endurances can then be plotted on a graph similar to that used in Figure 6.

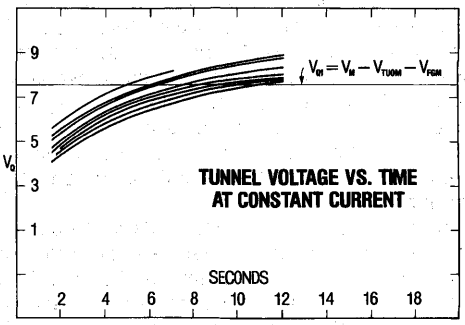

Figure 7: This is a record of tunnel voltage (expressed as trap-up voltage) vs time. The end of endurance is reached when the tunnel voltage reaches a value V_{Qf}. The time associated with that voltage can be read off this chart.

The area of the constant current structure was eight hundred times that of the single cell capacitors. Since its behavior is dominated by the highest current features, it is set equal to the endurance of the 400th lowest cell. This has been chosen as the average endurance of the lot of constant current devices. The fit in Figure 8 indicates good correlation between the two methods of determining endurance. This means that product endurances can be legitimately predicted from constant current data. Test times on the order of ten seconds are short enough for the E-test stage of wafer evaluation: they clearly permit the prediction of product endurance. But as increasing knowledge leads to an improvement in endurance, this time is expected to increase by several orders of magnitude. Eq(17) indicates a predictable acceleration technique. All that is needed is to increase the level of constant current, measure time to reach the voltage of the endurance limit, and insert that value onto Eq(17). In addition, the value of r must be adjusted to reflect the new current value, according to $r = I/C_{FG}$. Finally, a secondary adjustment must be made to the value of V_{TUOM} by calculation. Another method would be to increase the area of the constant current device to bring more low endurance features into play.

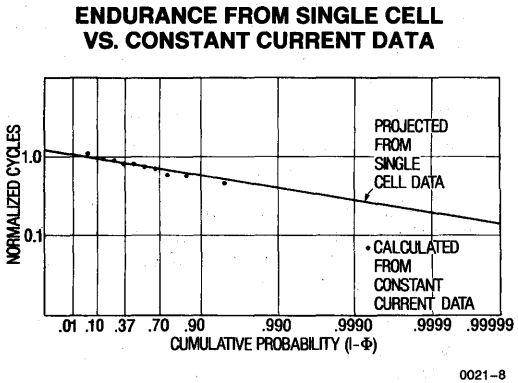

Figure 8: This is again a Log Extreme Value probability plot. The points are those calculated from the times measured via Figure 7. The straight line represents the endurance predicted from the single cell data in Figure 5.

SUMMARY

We have described a coherent body of understanding and data that permits the prediction of product endurance, and the use of devices for accelerated testing, from first principle device models. This fortunate circumstance arises from the advantageous technological feature of textured poly tunneling, namely that there is one, and only one, mechanism that is prevalent in determining the end of endurance.

This one mechanism is trap-up, the build-up of negative charge in the dielectric in proportion to the fluence of the tunnel current. The model for window closure and for single cell endurance flows naturally from this concept. The predictability of accelerated tests is also the result of this single unifying mechanism. The relationship with product endurance follows from basic statistical considerations.

ACKNOWLEDGMENTS

The authors would like to express their appreciation for the general support given to this work by Xicor management and staff. In particular, thanks are due to Yupin K. Fong and Kurt B. Raab for their effective help in the software development and for the performance of the measurements of the individual test structures.

APPENDIX

Mathematical Formulation for Lot Endurance from Single Cell Data

The approach taken here is simply to translate the graphical operations performed in preceding sections into symbols. Underlying its simplicity are the operations leading to the design of probability papers. They begin by translating the cumulative distribution of a variable into a linear function of that variable. The single cell endurances have the form:

$$\phi_C = 1/2 + (1/2)\{1 - \exp[\text{BELOW}]\} \quad \text{(A1)}$$
$$\text{BELOW} = [-(\pi/2)(\ln N_C - \ln \overline{N}_C)^2/\sigma^2]$$

where ϕ_C is the cumulative probability of single cell endurance N_C, $\overline{N}_C$ is the average cell endurance, and σ its standard deviation. The function form chosen is an approximation[11] to the normal distribution function. It is chosen here because it could be inverted most simply into a form linear in N_C, since the intent is to make the operations more transparent to the reader. The same operations could be performed by using the exact integral formulation of the cumulative probability of the normal distribution. Expressing Eq(A1) as a linear function of $\ln N_C$

$$\ln N_C = \ln \overline{N}_C - \sigma \times F_C, \text{ where} \quad \text{(A2)}$$
$$F_C = \{(-\pi/2) \ln [\phi_C (1-\phi_C)]\}^{1/2} \quad \text{(A3)}$$

Eq(A2) relates any single cell endurance N_C to its probability factor F_C and via Eq(A3), to its cumulative probability ϕ_C. The lowest endurance N_{CA} expected from an array of cells is defined by

$$\ln N_{CA} = \ln \overline{N}_C - \sigma \times F_{CA}, \text{ where} \quad \text{(A4)}$$
$$\phi_{CA} = [1/(\#\text{cells/array})]$$

An equation like Eq(A4) can be set up for the minimum endurance of a wafer lot N_{CM}, where $\phi_{CM} = [1/(\#\text{cells/wafer lot})]$. For the lot endurances, an equivalent scheme is set up:

$$\ln N_A = \ln \overline{N}_A - (1/\alpha) \times F_A, \text{ where} \quad \text{(A5)}$$
$$F_A = \ln [-\ln (1 - \phi_A)] \quad \text{(A6)}$$

Now N_A is the endurance of an array (or chip), $\overline{N}_A$ is the modal endurance of the lot, and F_A is the probability factor derived from the Extreme Value distribution. Incidentally, F_A is exact and not an

approximation. In analogy to Eq(A4), the average array endurance $\overline{N}_{AA}$ has the form

$$\ln \overline{N}_{AA} = \ln \overline{N}_A - (1/\alpha) \times F_{AA} \quad \text{(A7)}$$

The value of ϕ_{AA} for the average of the distribution must be 0.43, in order that its complement becomes 0.57, the locus of the average of the (maximum) Extreme Value distribution. The minimum endurance of the lot has the same subscript as Eq(A7), except that subscript AM is substituted for AA. The probability factor F_{AM} is based on ϕ_{AM} = [1/(#arrays/wafer lot)]. It will be realized that $N_{CA} = N_{AA}$, and $N_{CM} = N_{AM}$. Therefore two simultaneous equations can be solved for $\overline{N}_A$ (the lot average), and $1/\alpha$ (the lot dispersion), in terms of single cell parameters:

$$1/\alpha = \sigma \times [(F_{CM} - F_{CA})/(F_{AM} - F_{AA})], \quad \text{(A8)}$$

and

$$\ln \overline{N}_A = \ln \overline{N}_C - \sigma \times [(F_{CA} \times F_{AM} - F_{AA} \times F_{CM})/(F_{AM} - F_{AA})] \quad \text{(A9)}$$

Expressing Eq(A5) in terms of single cell parameters results in

$$\ln N_A = \ln \overline{N}_C - \sigma \times \{[F_{CA}(F_{AM} - F_A) - F_{CA}(F_{AA} - F_A)]/(F_{AM} - F_{AA})\} \quad \text{(A10)}$$

In this way, the individual endurances expected from a commercial lot N_A can be predicted from the size of the lot tested, which determines F_A, the single cell constants $\overline{N}_C$ and σ, and chip size details of that product, which convert the F's with double subscripts into specific constants.

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COMPARISON AND TRENDS IN TODAY'S DOMINANT E^2 TECHNOLOGIES

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ABSTRACT

This paper reviews the three dominant E^2 technologies today, namely the two floating gate approaches of thin tunnel oxide and oxide on textured poly and the dual dielectric approach of MNOS. It evaluates each approach with respect to cell design, operation, manufacturability, compatibility with established process technologies and reliability. It follows with a comparison of the technologies in the areas of development entry cost, scaling and reliability. After a review of the market place, this paper concludes with a projection of the requirements of E^2 technologies to support full function, commodity E^2 memories (E^2PROM) as well as low cost microcontrollers and ASIC (Application Specific Integrated Circuits).

INTRODUCTION

Electrically alterable nonvolatile semiconductor memory has been an area of active research for many years, with the promise that it will be the ultimate silicon memory. The first floating gate memory was proposed in 1967[1] and MNOS memories were reported at about the same time.[2] In 1980, the first 16K E^2PROMs using MNOS[3] as well as floating gate technologies on FLOTOX[4] were reported, while textured poly E^2PROMs were reported in 1983.[5] However, after all these years of development in the laboratory and volume manufacturing, E^2PROMs have yet to become a high volume, widely used memory component compared to EPROMs, the closest equivalent memory with lower functionality. There are many reasons given for the limited growth, ranging from the higher cost of E^2PROM based products to poorly understood reliability of these components. In this paper, we will focus on the technology factors by comparing the three dominant E^2 technologies to date, and giving our own viewpoint on the development in the market place.

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DESCRIPTION OF TECHNOLOGIES

FLOTOX (FLOating gate Tunnel OXide)

The cross sectional structure of a FLOTOX cell is shown in Figure 1a. It consists of a floating gate transistor with a thin oxide grown over the drain region. The floating gate is surrounded completely by high quality silicon dioxide, giving its superior retention characteristics. Programming (electrons into floating gate) is achieved by taking the control gate to high voltage while erase (electrons out of floating gate) is achieved by grounding the control gate and taking the drain to high voltage. Because the program and erase coupling conditions are different, they have different design considerations. Electron transfer is through Fowler-Nordheim tunneling mechanism using electric field higher than 10 MV/cm. The IV slope of tunneling is so steep that there is insignificant tunneling under normal read conditions for more than ten years. In order for the cell to properly operate in an array, it has to be isolated by a select transistor. Two cycles are required to load the correct data. All cells in a byte are first programmed, and then selected cells are erased using the drain for data control. The manufacturing process for FLOTOX is an extension of the EPROM technology, which in turn is an extension of the standard single poly silicon gate technology. The critical step in the process is the growth of high quality thin (<12 nm) tunnel oxide. For reliability, the dominant failure mechanism for FLOTOX is the breakdown of the tunnel oxide due to defects under the high field stress of the program/erase cycles, resulting in a leaky oxide.[6]

Textured Poly Cell

The cross sectional structure of a textured poly cell is shown in Figure 1b. It consists of 3 layers of poly with overlap forming three transistors in series. The floating gate transistor is in the middle formed by poly 2. Again, the floating gate is surrounded by silicon dioxide for high retention. Programming is

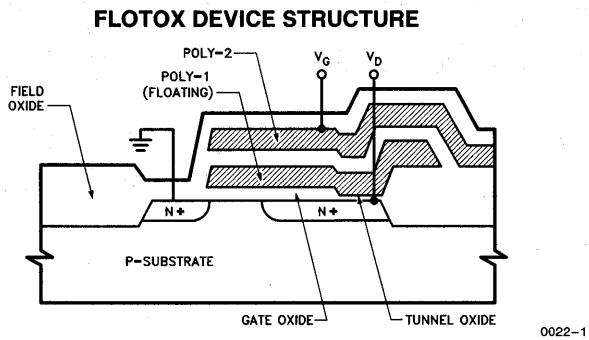

Figure 1a: Cross sectional structure of a FLOTOX memory cell.

achieved by electrons tunneling from poly 1 to poly 2 and erase is achieved by electrons tunneling from poly 2 to poly 3. The program and erase coupling again is different. The poly 3 is taken to high voltage in both cases, and the element which tunnels is determined by the voltage applied from the drain and coupled to the floating gate through the channel region. The final data state is determined by the data state on the drain: this is a "direct write" cell with no need to clear before write as is required in the FLOTOX cell. This is possible because there are two active tunnel elements. The tunneling process is fundamentally still Fowler-Nordheim tunneling, with enhancement of local electric field due to the geometrical effect of fine texture at the poly surface. The electric field enhancement factor is in the range of 3 to 5, allowing much thicker oxides (60 nm to 100 nm) to be used. No extra transistor is required in an array since the poly 3 transistor serves the function of select transistor, giving a much more compact cell layout. The manufacturing process for textured poly is again an extension of the EPROM process with the addition of an extra layer of poly. The critical process step in this process is the growth of the tunnel oxide on poly. Because thicker oxides are used, oxide breakdown is less of a problem compared to FLOTOX. The dominant failure mechanism in a textured poly cell is electron trapping which results in memory window closure.[7]

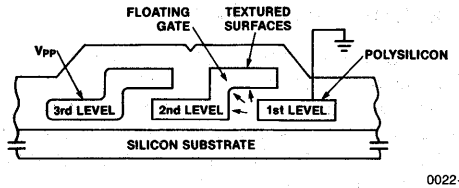

Figure 1b: Cross sectional structure of a textured poly memory cell.

MNOS (Metal Nitride Oxide Silicon) Cell

The cross sectional structure of a MNOS cell is shown in Figure 1c. It consists of a single transistor with a dielectric stack of silicon nitride on top of a thin layer of oxide (1.5 nm to 2.0 nm) on silicon. Typically, the transistor resides in a well so that the channel potential can be controlled. Unlike the floating gate, charge is stored in discrete traps in the bulk of nitride. Because of the discrete nature of traps, charge transfer has to occur over the large area of the channel region. This is different from floating gate devices where charge transfer can occur over a small area removed from the channel region. On the other hand, any dielectric defect fatal to floating gates will only discharge local traps in MNOS. Programming is achieved by applying high voltage to the top gate whereas erase can be achieved by grounding the top gate and taking the well to high voltage. The program and erase coupling is symmetrical. Because of the very thin oxide, charge is being leaked off continuously due to the internal field, giving an ever diminishing window. In an array, select transistor is required to operate the cell properly. The select transistor may be separate[3] or integrated[8] in which case a more compact cell layout can be realized. Two cycles are again required to load the correct data. Furthermore, the well potential has to be controlled during data change, which makes the array operation more complex. The manufacturing process for MNOS is an extension of single poly silicon gate technology. The memory transistor is fabricated after the first poly periphery transistors are formed to maintain the integrity of the dual dielectric storage element. The

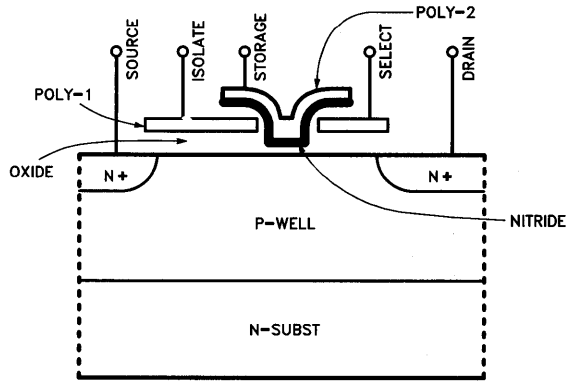

Figure 1c: Cross sectional structure of a MNOS memory cell.[8]

important steps include thin oxide growth, nitride deposition and post nitride temperature cycles. The biggest reliability concern is cell retention and its degradation with cycling.[9]

COMPARISON

The three different approaches have their technical merit and difficulties. Any one of these technologies can be made to work if they are given sufficient effort and focus. As a result, other considerations ranging from "comfort factors" to compatibility with available technologies tend to determine the choice.

Development Entry Cost

Entry cost is the amount of extra effort required to bring up a new technology. To an EPROM manufacturer, it is relatively easy to take the FLOTOX approach. The cell concept is simple and the tunnel oxide process is a straight forward variation of a standard high quality oxide furnace cycle. This is why the majority of companies have opted for this approach for their E^2 effort. The textured poly approach, on the other hand, depends on a tunneling process which is not generally understood and is believed to require tighter process control. The cell concept is more complex and the use of three layers of poly imply higher wafer cost. These factors have limited the popularity of developing this approach. Finally, MNOS approach requires the mastering of a number of difficult process steps. The growth and control of the ultra thin oxide, as well as the quality of nitride are critical issues. As a result, despite gaining initial momentum, MNOS has not achieved dominance as an E^2 technology.

Scaling

There are many factors that determine the size of a memory cell, and generally cell design represents finding the optimum compromise of a number of tradeoffs. Furthermore, as these technologies approach fundamental physical or practical material limits, scaling will become increasingly difficult. For FLOTOX, there is large area requirement for layout of the two transistors plus the tunnel oxide area, dictated by minimum design rules. The select transistor is limited by high voltage. Given the high oxide capacitance of thin tunnel oxide, large poly to poly area is required for the sense transistor. Scaling of the tunnel dielectric is also limited by direct tunneling at 6 nm and yield and reliability issues at 8 nm to 10 nm. Typically, relatively high voltages (15V to 20V) are required to operate the cell. As a result, FLOTOX cell does not scale well.

In the case of textured poly, the three poly layers are integrated resulting in a compact layout. Cell size is limited more by lithographic registration of poly layers than by ability to resolve space between poly lines as is the case with FLOTOX. Furthermore, the thick tunnel oxide requires smaller coupling capacitor area to give the required coupling. Given the same performance and reliability requirement, it is estimated that a textured poly cell is about a factor of two smaller compared to a FLOTOX cell for a given generation of technology. Textured poly does require higher operating voltage (>20V) and thus needs a high voltage technology to support it. Finally, scaling of the poly oxide involves more than thinning down the oxide as the field enhancement factor changes with oxide thickness.

The basic MNOS memory cell can be very small and highly scaleable. The select transistors, wheth-

er separated[3] or integrated,[8] will limit scaling. However, in either case, the cell size is better than FLOTOX, and competitive with triple poly for a given generation of technology. One major problem is the requirement of well voltage control. Full byte function is only possible with separate well, giving a large effective cell size. Page function[8] can be used to partially circumvent the well problem but limits endurance. For oxide thicknesses, there is little or no room to scale the ultra thin tunnel oxide, so most of the emphasis has been on scaling the nitride. Charge leakage from the scaled nitride to top gate has been solved by oxidizing the nitride to give a MONOS stack. Low program and erase voltages have been demonstrated at the expense of smaller operating window.

Reliability

One general problem for E²PROM is the limited information on the reliability of the technologies due to sample size or correlation problems. For floating gate technologies, there is no intrinsic problem with data retention, and because the technologies are designed to handle high voltage, there is very low failure rate due to normal 5V operation. Reliability problems occur during program and erase cycles in part because very high voltages are used. For FLOTOX, there is random single bit failure due to oxide defect resulting in a leaky oxide that loses charge over time (see Figure 2). For textured poly, the average electric field across the tunnel oxide is 3 to 5 times lower compared to FLOTOX. As a result, oxide breakdown failure is reduced significantly. On the other hand, there are more electron traps in the oxide, and the impact of electron trapping is magnified by the 3 to 5 times field enhancement factor. Consequently, electron trapping is the dominant failure mechanism, showing up as a failure to program or erase. The failure can be projected real time with margining techniques and since trapping is an intrinsic property, failure probability can be easily projected. In MNOS, charge retention is the dominant reliability issue (see Figure 3). The charge loss process is time dependent, resulting in continuous loss of cell margin and performance. The degradation based on short term data is difficult to predict. The ultra thin oxide is stressed by electric field comparable to FLOTOX and retention is further degraded with program and erase cycles. So far, wide variation in retention and endurance are being reported based on limited sampling.[9]

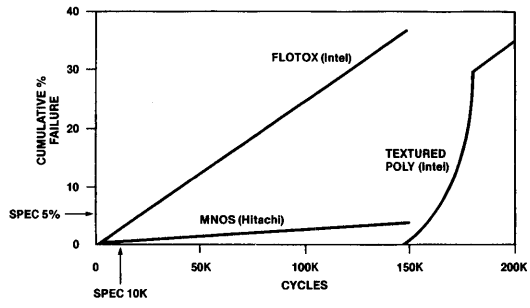

Figure 2: Endurance of 3 E² Technologies: FLOTOX and textured poly processed at Intel (16K arrays), MNOS data from Hitachi (prorated to 16K).

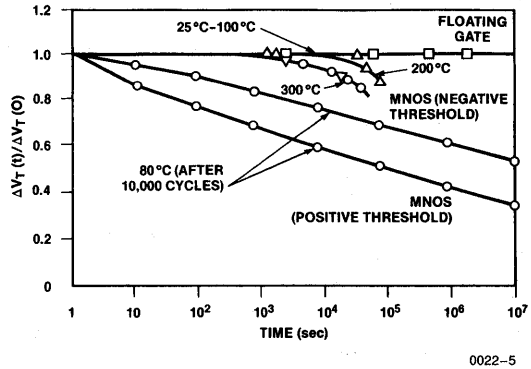

Figure 3: Data Retention: Floating gate, no intrinsic charge retention problem; MNOS, continuous charge loss and window closure tending to become worse after cycling.

THE MARKET PLACE

Though E²PROMs have been available for the last five years, their usage has not grown to the volumes projected. A host of new and established companies have become active in the field, but lack of technology and product feature standardization, together with high cost and reliability concerns have limited the growth in the market place. The major issues for 16K have been 5V only, address/data latch vs no latch, ready/busy vs data polling, 24 pin vs 28 pin, 1 ms vs 10 ms program, self timed vs user timed, with and without V_{CC} lockout and 10K vs 1 Million cycles endurance. Byte vs page function and page size are issues at 64K density level. In addition, one can choose oxynitride vs oxide for FLOTOX, textured poly vs FLOTOX for floating gate, and MNOS vs floating gate for E². The reliability claims are difficult to understand and verify due to the link of failure to endurance cycling. Different

methods are used in reliability evaluation, and no standard exists to allow a meaningful comparison. For example, high temperature cycling is worse case for FLOTOX but may be best case for textured poly. Nevertheless, there has been continued growth in the E²PROM market, sustained by a wide, diversified application base. The driving force is end-user, in-the-field customization capability offered to microprocessor based products, which is either unavailable, unreliable or not cost effective using other techniques. As a result, standards are now established following 5V-only RAM-like functionality, and the cost and density gap to competing solutions continues to close.

FUTURE TRENDS

There are two major driving forces in the development of E² technologies for the future. One of them is high density memories, requiring small memory cell size for the lowest cost per bit. The second requirement is low density nonvolatile memories in microcontrollers and programmable logic type applications. In the latter case the absolute cell size is not as important as process simplicity and low cost of the overall technology. MNOS based E² memories will continue to be used in low density memory as well as military applications requiring high radiation tolerance. However, it has only enjoyed limited popularity for use in high density memory and the trend will continue. A majority of companies have opted for FLOTOX as their first E² technology because of the simple device physics and the low entry cost for development. Recently, many Japanese companies have announced 64K E²PROMs based on FLOTOX for the smart card market. A number of companies have applied FLOTOX in ASIC and programmable logic array applications. In fact, some have developed single poly versions of FLOTOX for synergy with random logic technology. However, for stand alone high density E² memories, FLOTOX will be increasingly limited by defect oxide breakdown problems,[10] giving unacceptable failure rate above the 64K level, unless thicker oxides or new dielectrics can be used in new approaches. Error correction codes can also be used but at the expense of additional die cost.[11] Finally, textured poly inherently gives a smaller memory cell and suffers least from the oxide breakdown problem. Electron trapping is an intrinsic property that can be predicted and easily screened. Consequently, textured poly technology is expected to be most reliable and cost effective for 256K and above densities, while the higher cost of a three layer poly process may limit its use in logic applications.

The nonvolatile memory technology is an ever evolving field. Memories[12,13,14] based on hybrid operation of programming by EPROM and erase by tunneling have gained interest. The erase function is generally limited to the full array and thus it is called FLASH erase. Recent approaches offer cell size and technology complexity comparable to EPROMs, and the functionality of electrical erase. If such technologies are proven to be reliable and manufacturable, they will fill the need of a special market segment and become another major force in the developing nonvolatile memory market.

SUMMARY

We have reviewed the three dominant E² technologies today. MNOS is used in low density memories as well as military applications, but enjoyed only limited popularity for high density memories. FLOTOX has been the most popular approach because of its simplicity and is most suited for low density memories and programmable logic type application. Textured poly gives the smallest memory cell size and is the most cost effective and reliable approach for high density memories.

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NEW ULTRA-HIGH DENSITY TEXTURED POLY-Si FLOATING GATE E²PROM CELL

By D. Guterman, B. Houck, L. Starnes and B. Yeh

This paper describes a new, highly scaled cell structure, the smallest full function E²PROM cell reported to date. It utilizes the textured triple-poly-si technology, exploiting the high degrees of structural and functional integration, to achieve a cell size of 31 μ^2. A top view of the cell, built with 1.2 micron rules is shown in Figure 1, with cell cross-section and equivalent circuit shown in Figures 2 and 3, respectively.

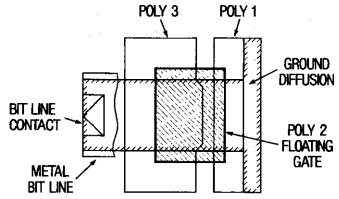

Figure 1: Cell top view.

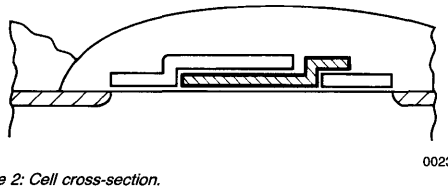

Figure 2: Cell cross-section.

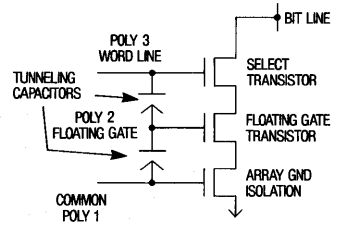

Figure 3: Cell equivalent circuit.

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Very small memory cell size is achieved by exploiting the vertical integration of the three poly layers to form a merged gate single transistor cell. This cell is made possible through the dual functions incorporated within various key components; specifically, (1) the poly 3 element, which functions as both word line select transistor and erase tunneling anode (2) the poly 1 electrode which serves the dual role of cell ground isolation transistor and programming cathode during write operation, and (3) the poly 2 floating gate transistor whose channel region establishes both the floating gate charge-conditional current path for reading and the input-data-conditional steering capacitor for writing. Charge transport to and from the floating gate is through Fowler-Nordheim tunneling, established by the geometrically enhanced fields at the textured poly interfaces between poly-si layers. This allows tunneling injection and transport to occur across oxides of thickness greater than 500Å at voltages less than 15V. In comparison to ultrathin (100Å) E²PROM technologies, the thicker interpoly oxides result in lower parasitic capacitance of the tunneling element, improved dielectric reliability because of the 3–5× lower average fields in the oxide, and an easier path to oxide scaling.

Because of the simultaneous incorporation of the poly 2 to 1 programming and poly 3 to 2 erase tunneling elements, data storage is a direct, single pass operation, involving the following sequence (see Table I). First the poly 1 line, common to the entire array, is brought low, cutting off the conduction path from bit line through the cell to array ground. Next, the bit lines are set up to either 0V for an erased state or about 16V for a programmed state. Finally, the poly 3 word line is ramped up to about 22V in 1 ms to drive the nonvolatile charge transport. To erase, the bit line is grounded, whereupon the channel under poly 2 capacitively steers the floating gate towards ground. This induces sufficient voltage across the poly 3/2 tunneling element to remove electrons from the floating gate. When the bit line is high for programming, the channel potential steers the floating gate positively. This

TABLE I: OPERATING CONDITIONS

Operation	Bit Line	Poly 3	Poly 1
Standby	2V	0	5V
Read	2V	5V	5V
Write Erased State	0	~22V	Low
Programmed State	~16V		

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induces sufficient voltage across the poly 2/1 tunneling element to inject electrons onto the floating gate.

Following up on the present 256K product experience, a number of fundamental factors are incorporated into the technology to maintain a high degree of reliability with scaling. Dielectric integrity and excellent charge retentivity is preserved through the use of thick, high quality thermal SiO_2 dielectrics, throughout. Direct write cell operation provides shorter write time by eliminating the unconditional clear before write. As in previous floating gate E^2PROMs, 5V-only capability via on-chip voltage multiplication is possible because of the efficient Fowler-Nordheim tunneling mechanisim.

Small test arrays of the 31 μ^2 cell, shown in the SEM views of Figure 4, have been built and operated successfully for endurances of 1 million writes. Figure 5 shows a representative extended endurance plot, demonstrating erased state cell currents of greater than 40 μA and programmed cells having thresholds of greater than 5V, thereby remaining in cutoff.

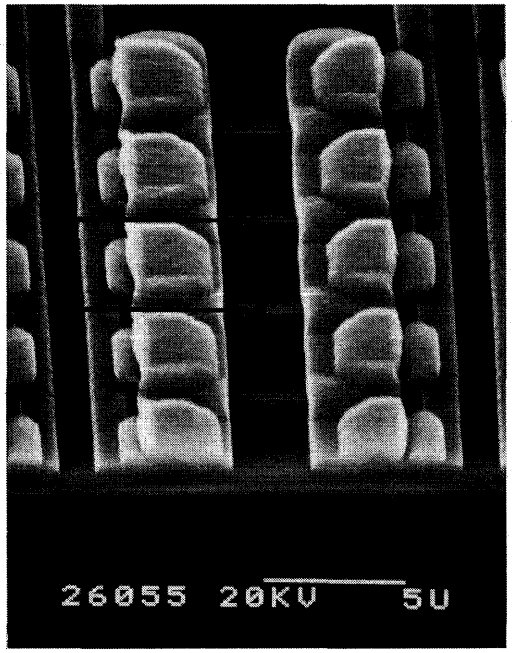

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Figure 4a: Cell SEM top view.

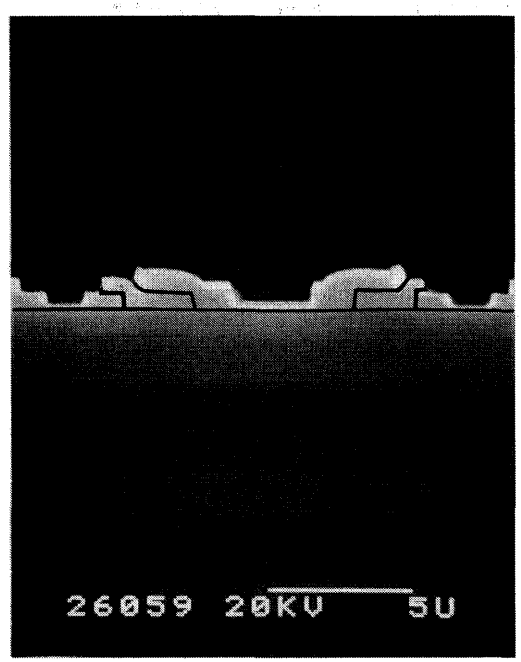

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Figure 4b: Cell SEM cross-section.

ENDURANCE DATA
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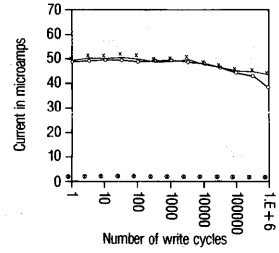

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Figure 5: E^2PROM cell test endurance data.

In conclusion, this paper reports the smallest full function E^2PROM cell described to date. Small size is a result of a cell in which elements serve multiple functions and a technology which is conducive to scaling. This approach will serve as foundation for developing future generation E^2PROMs beyond today's 256K density.

RELIABILITY COMPARISON OF FLOTOX AND TEXTURED POLY E²PROMs

By Neal Mielke—Intel Corporation
Lori J. Purvis & H.A. Richard Wegener—Xicor, Inc.

SUMMARY

FLOTOX and Textured Poly E²PROMs share the excellent retention and lifetest performance of the more common EPROM. In particular, retention failures add only about 20 FIT to lifetest failure rates in the 100 FIT range. The lifetest failure rates compare favorably with those of simple static logic products, because these high voltage devices have no oxide breakdown problems during 5V operation. FLOTOX endurance is limited entirely by oxide breakdown, overwhelmingly of the tunnel oxide. Window closing, caused by electron trapping, occurs but does not cause failure in well-designed products.

The Textured Poly approach offers a reliability tradeoff: less oxide breakdown but more window closing. This tradeoff becomes favorable at higher densities. This is because oxide breakdown, being a defect mechanism, worsens with increasing memory size and with scaling of oxide thickness. Window closing is an intrinsic mechanism that does not worsen dramatically with higher density. The two failure mechanisms—oxide breakdown and window closing—should be treated separately in reliability evaluations because they have different dependencies on cycling, temperature and retention bakes.

RETENTION CHARACTERISTICS

The E²PROM retention is at least as good as the EPROM retention, as shown in Table I. The 0.2% failing for the I 2817A represents only 20 FIT added to the failure rate. All retention failures are at most only a few bits out of the memory array. Intrinsic retention limitations simply do not exist on these technologies; most bits have essentially unlimited retention.

Excellent retention is expected with these technologies for two reasons:

1) The stored charge on the floating gate is contained by the 3.2eV energy barrier which exists at the Si-SiO_2 interface. This barrier height is quite high, comparable to the barriers preventing dopant atoms from redistributing.

2) The oxide layers, even with FLOTOX, are thick enough to prevent carriers from tunneling off the floating gate during low voltage operation.

LIFETEST PERFORMANCE

TABLE II: LIFETEST COMPARISONS OF INTEL E²PROM, EPROM AND STATIC LOGIC

Product(s)	Technology	125°C Lifetest Predicted Failure Rate (55°C, in FIT)		
		Breakdown	Retention	Total
2817A	FLOTOX	0	36	70
27256	EPROM	0	22	63
2114B, 8088, etc.	HMOS-II	110	0	120

The failure rates predicted from lifetest in Table II compare favorably with those of EPROMs, which in

TABLE I: RETENTION COMPARISON OF INTEL EPROM AND E²PROM, AND XICOR E²PROM

Product	Technology	Sample	Temp	% Fail in Retention Bake			
				48 Hrs	168 Hrs	500 Hrs	1000 Hrs
I 2764A	EPROM	1800	250°C	0.9%*	1.1%	2.0%	—
I 2817A	FLOTOX	550	150°C	0.0%	0.0%	0.2%	0.2%*
X2864G	Textured Poly	350	250°C	0.0%*	0.0%	0.0%	0.3%

*Represents ~ 15 Years at 55°C (E_A = 0.6eV).

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turn compare favorably with those of non-floating gate technologies. E²PROMs compare favorably with EPROMs because they are very similar technologies. It is only during endurance cycling that E²PROM operation differs significantly from EPROM operation. EPROMs and E²PROMs compare favorably with static logic devices because the nonvolatile devices are built on high voltage technologies and are operated during product testing at high voltages. This all but guarantees that there will be no oxide breakdown failures during 5V operation. Static logic devices generally are dominated by oxide breakdown. In addition to the Intel data above, NEC has reported that 65% of field failures from 1976 to 1979 were due to oxide failure.

ENDURANCE CHARACTERISTICS

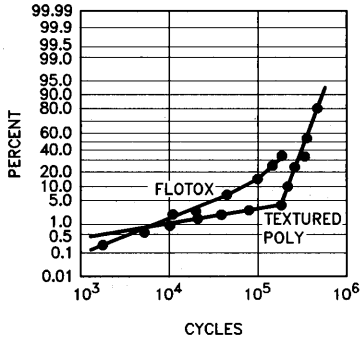


Figure 1: Percent fail vs. number of cycles at room temperature for FLOTOX (2816A, 2817A) and Textured Poly (2864).

FLOTOX endurance, as shown in Figure 1, has a single broad distribution of failures. Textured Poly endurance has a low level defect tail followed by a sharp wearout beyond 150K cycles. The curves imply that the Textured Poly approach offers a tradeoff under which a lower defect tail can be had at the expense of some wearout endurance. There are 3 primary failure mechanisms represented in Figure 1:

1) Tunnel Oxide Breakdown—the dominant FLOTOX mechanism, also responsible for part of the Textured Poly defect tail.

2) Gate Oxide Breakdown—responsible for the remainder of the Textured Poly defect tail.

3) Window Closing—the cause of Textured Poly wearout.

These three mechanisms will be discussed in turn.

ENDURANCE: TUNNEL OXIDE BREAKDOWN

A typical FLOTOX or Textured Poly cell can be cycled over a million times without oxide failure or any degradation in retention characteristics. Occasional defective tunnel oxides will eventually break down under the high electric field (~10 MV/cm) necessary for tunneling. When this occurs, the defective cell will either become stuck to one logic state (if the oxide is truly shorted) or fail to retain charge (if the oxide is only leaky). Generally, the oxide breakdown increases gradually with cycling—a bit becomes leaky slowly, then faster, and eventually it becomes stuck. Tunnel oxide breakdown is responsible for about half of the Textured Poly defect tail. It displays the same characteristics as FLOTOX.

ENDURANCE: GATE OXIDE BREAKDOWN

Both E²PROM types require high voltages to program and erase. This puts high stress on MOS gate oxides both in the cell and in the logic circuitry using high voltage. This high stress causes defective gate oxides to break down. Typical symptoms are a row or column failure or failure of the entire device. This failure mechanism is responsible for the remainder of the Textured Poly defect tail.

Although more common on Textured Poly than on FLOTOX because of somewhat higher voltages, the overall oxide breakdown failure rate of Textured Poly (tunnel oxide plus gate oxide) is still significantly lower than that of FLOTOX.

ENDURANCE: WINDOW CLOSING

During endurance cycling, some of the electrons tunneling through the tunnel oxides become trapped there. The resulting negative oxide charge inhibits further tunneling. The effect of this electron trapping

is that with further cycling a cell requires higher and higher voltages to program and erase. This mechanism is responsible for the entire wearout region of the Textured Poly curve but is non-existent in the FLOTOX curve.

In Figure 2 Textured Poly shows a dramatically higher rate of trap-up. As a result, window closing is the dominant wearout mechanism of Textured Poly, whereas it is an issue of FLOTOX only if the circuit design is marginal.

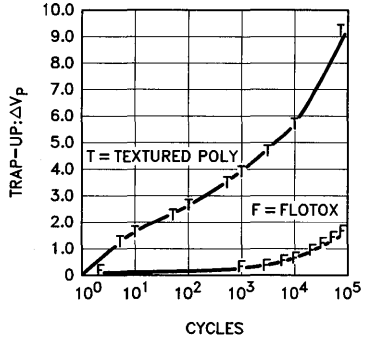


Figure 2: Trap-up vs. cycles for Textured Poly (2864) and FLOTOX (2816A). Trap-up is measured in terms of the increase in programming voltage ΔVp necessary to program the cell.

TRAP-UP/BREAKDOWN TRADEOFF

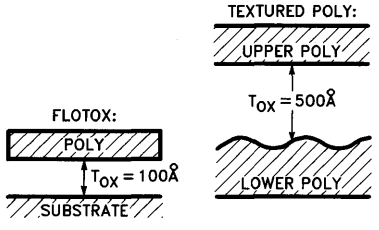


Figure 3: FLOTOX and Textured Poly structures.

Trap-up is greater in the Textured Poly approach because:

1) The trapping probability for a single electron is proportional to $N\sigma T_{OX}$, which for the same trap density N and cross-section σ is greater for Textured Poly, since T_{OX} is greater.
2) The effect of the trapped charge is multiplied by the same field acceleration factor responsible for the field enhancement used for tunneling.
3) There is less field induced detrapping because the average electric field is lower.

Tunnel oxide breakdown is less frequent in the Textured Poly approach because:

1) The tunnel oxides are thicker and therefore are less sensitive to microscopic defects.
2) The high electric field responsible for tunneling occurs only in the region of oxide near texture points; the bulk of the oxide sees only low field stress.

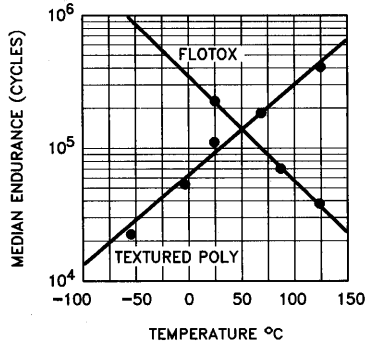
The trap-up/breakdown tradeoff is fundamental to the Textured Poly approach.

BENEFITS OF THE TRADEOFF

Trap-up is an intrinsic mechanism, determined by trap density, trap cross-section, and initial window size. There is some variation from cell to cell in these parameters, causing some to fail somewhat earlier than others, but the distribution is relatively tight. As a result, trap-up endurance becomes only slightly worse with increasing memory size.

In contrast, oxide breakdown is a defect mechanism, and the failure rate is proportional to the defect density and the memory size. As a result, FLOTOX endurance will always become proportionately worse with increasing memory size unless defect density is continually improved. In addition, scaling FLOTOX implies scaling the tunnel oxide thickness, making the oxide even more sensitive to defects.

For this reason, there is a crossover in reliability between FLOTOX and Textured Poly, with the Textured Poly tradeoff becoming favorable at high densities. Excellent endurance even at high densities is possible with the Textured Poly approach because the defect tail, being only low level, can be screened.



0024-4

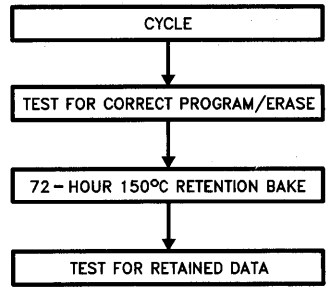
Figure 4: Comparison of median endurance for FLOTOX (2816A) and Textured Poly (2212) as a function of cycling temperature.

FLOTOX failure, due to tunnel oxide breakdown, is accelerated by cycling temperature ($E_A \sim 0.18eV$), as shown in Figure 3. Textured Poly failure, due to window closing, is decelerated by cycling temperature ($E_A \sim -0.11eV$). Whereas it is well known that temperature accelerates oxide breakdown, it also accelerates detrapping of electrons and therefore extends Textured Poly endurance.

A reliability evaluation of these two products performed at 50°C would detect equivalent median endurances, but an evaluation performed at room temperature would favor FLOTOX by about 5× and one at 125°C would favor Textured Poly by about 10×. This temperature acceleration holds true for the median endurance, but the Textured Poly defect tail is due to oxide breakdown and will tend to behave more like the FLOTOX data.

EFFECT OF BAKES

In many FLOTOX endurance evaluations, less than half of the oxide breakdown failures actually fail to program correctly. The remainder are cases of oxide degradation and suffer reduced retention instead. As a result, retention bakes must be performed *after* cycling on FLOTOX in order to adequately detect cycling failures:



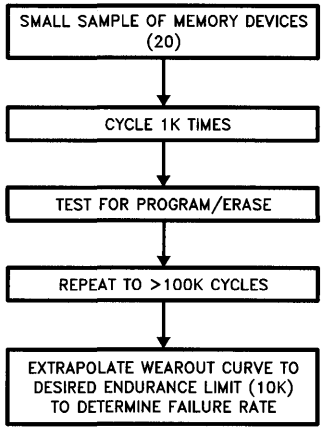
0024-5

In order to take intermediate readouts (after, say, 2K and 5K cycles), the flow of test/bake/test may be repeated at each readout. This worst-case flow for FLOTOX may be best-case for Textured Poly, however, because high temperature retention bakes cause electrons to detrap significantly, reversing prior window closing and therefore increasing measured endurance.

SUGGESTED ENDURANCE-EVALUATION METHODOLOGY

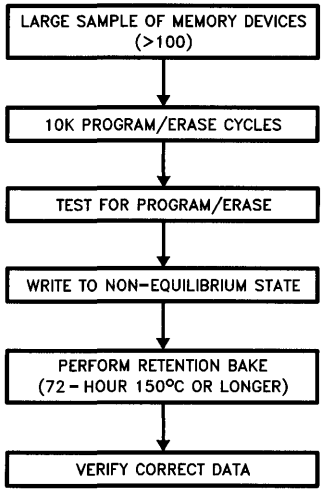
The best way to measure E²PROM endurance is to run separate evaluations for the two dominant failure mechanisms: window closing and oxide breakdown.

Window Closing



0024-6

Oxide Breakdown



0024-7

These flows will work for either FLOTOX or Textured Poly. Intermediate readouts may be performed in the oxide breakdown flow, but the test/bake/verify sequence should be repeated at each readout.

ALTERNATIVE EVALUATION METHODOLOGIES

Single-cell endurance data are sometimes presented by manufacturers. This approach will overestimate endurance by orders of magnitude because of the importance of oxide defects and even cell-to-cell variations in trap-up. It might be possible to conclude from single-cell data that a certain FLOTOX cell is "superior" to a certain Textured Poly cell—but a 256K E^2PROM constructed with the Textured Poly cell might be several times more reliable.

Worse yet, test pattern data from oxide capacitors are sometimes presented, without backup product data, to "prove" that a certain oxide is "superior" to another. Only product data can reliably be used to compare E^2PROM product endurance. Small samples are useful in measuring wearout (median endurance), but large samples are necessary for measuring defect-related tails to the distribution.

CONCLUSION

The non-endurance-related reliability of FLOTOX and Textured Poly E^2PROMs are similar and comparable to EPROMs and simple logic devices. Textured Poly offers a tradeoff between oxide breakdown and window closing which is beneficial at high densities. Reliability evaluations should distinguish between the two dominant E^2PROM failure mechanisms: Namely, oxide breakdown and window closing.

NOTES

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Serial Products Data Sheets 2

E²PROM Data Sheets 3

E²POT™ Data Sheets 4

Microcontroller Peripheral Products 5

Memory Subsystems 6

Die Products 7

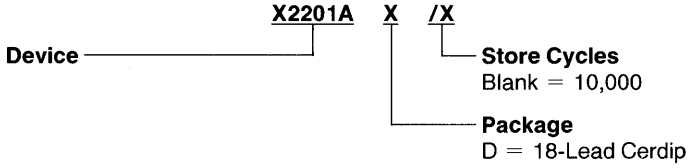
Application Notes and Briefs 8

Product and Technology Reliability Reports 9

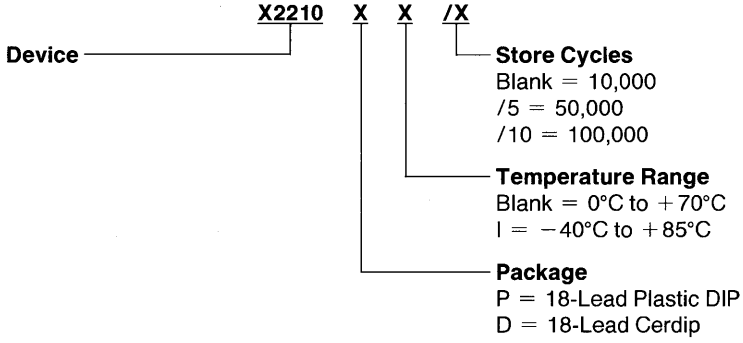
Ordering Information and Package Drawings 10

Ordering Information

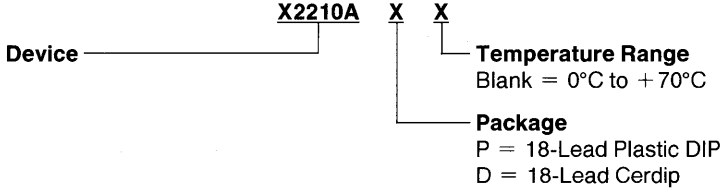
X2201A: 1024 x 1 NOVRAM



X2210: 64 x 4 NOVRAM



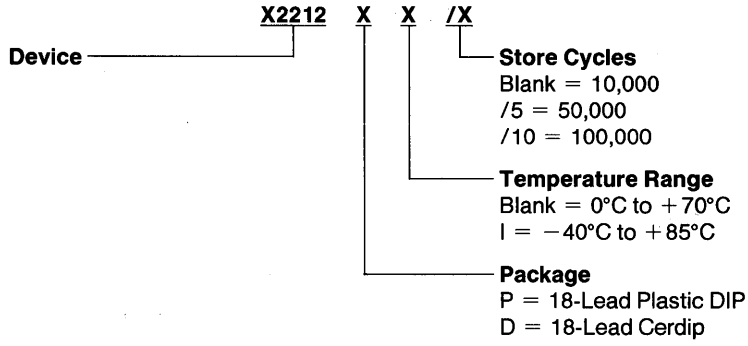
X2210A: 64 x 4 NOVRAM



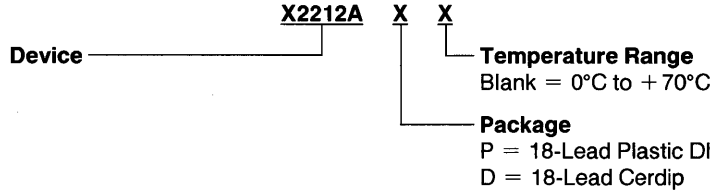
10

Ordering Information

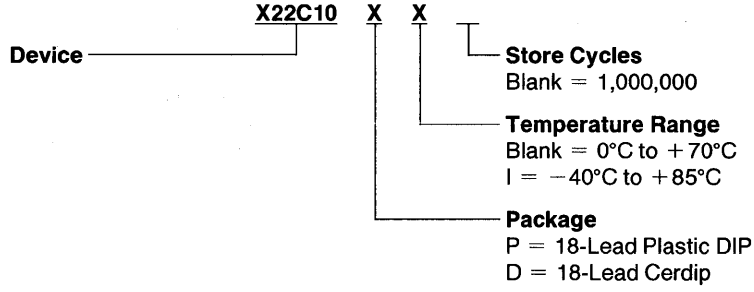
X2212: 256 x 4 NOVRAM



X2212A: 256 x 4 NOVRAM

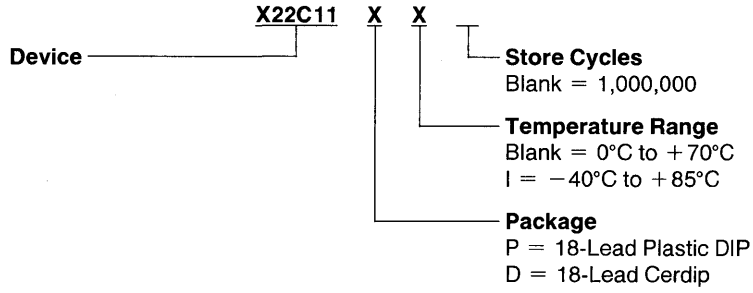


X22C10: 64 x 4 CMOS NOVRAM

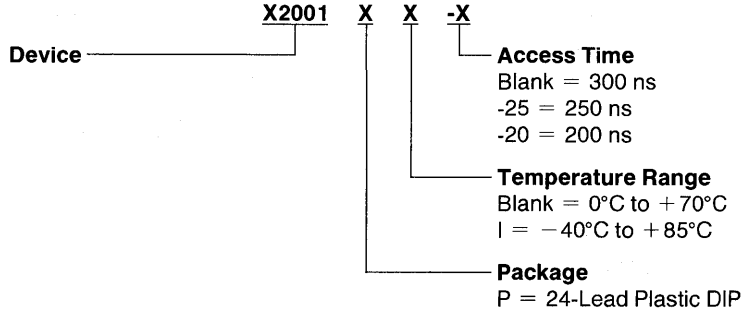


Ordering Information

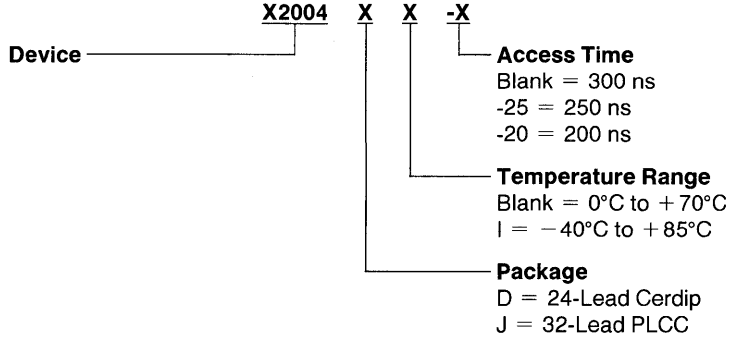
X22C11: 64 x 4 CMOS NOVRAM



X2001: 128 x 8 NOVRAM

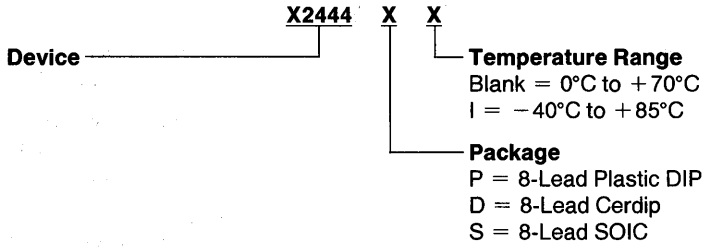


X2004: 512 x 8 NOVRAM

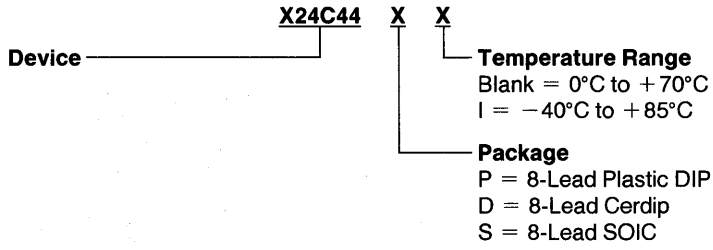


Ordering Information

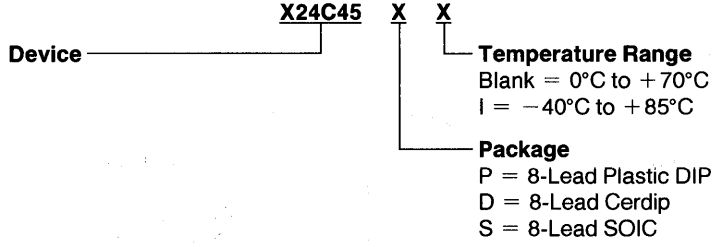
X2444: 16 x 16 Serial NOVRAM



X24C44: 16 x 16 CMOS Serial NOVRAM

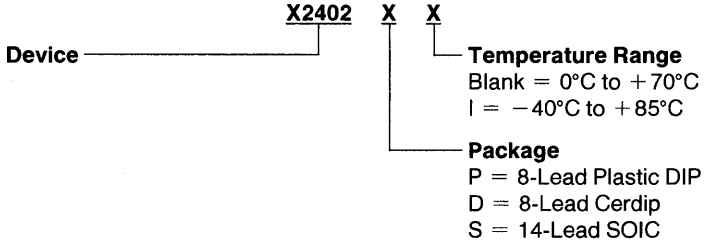


X24C45: 16 x 16 CMOS Serial NOVRAM

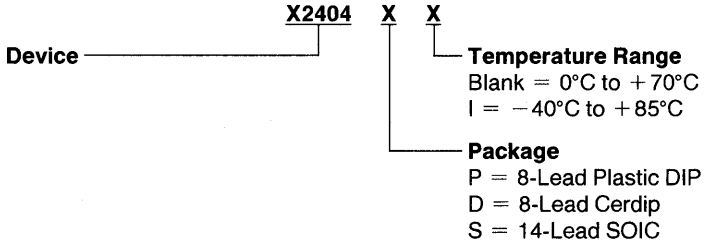


Ordering Information

X2402: 256 x 8 Serial E²PROM

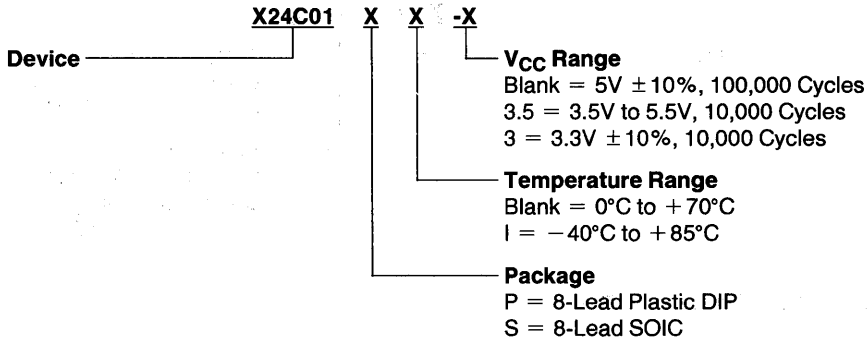


X2404: 512 x 8 Serial E²PROM

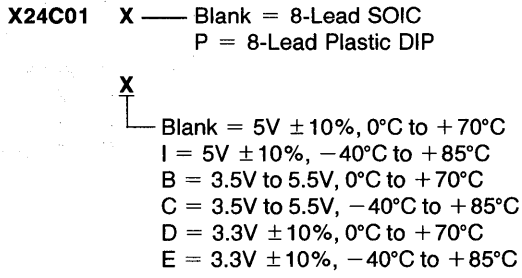


Ordering Information

X24C01: 128 x 8 CMOS Serial E²PROM

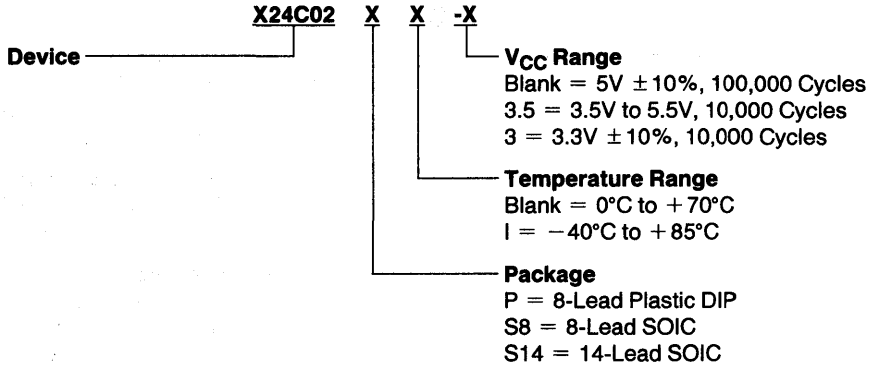


Part Mark Convention

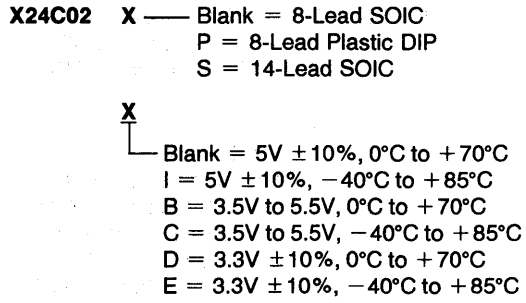


Ordering Information

X24C02: 256 x 8 CMOS Serial E²PROM

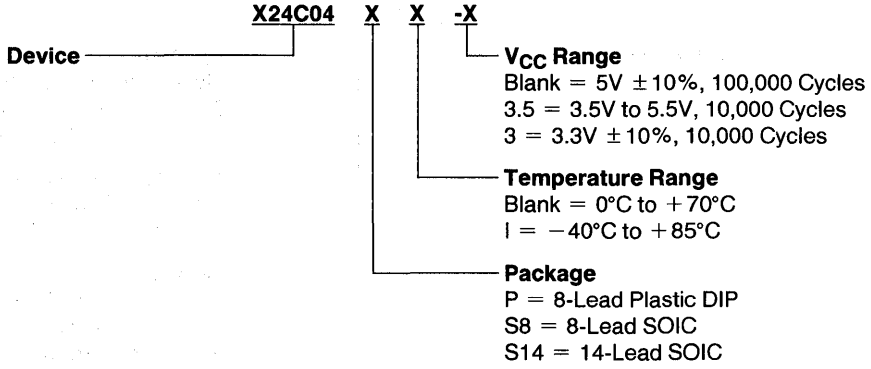


Part Mark Convention



Ordering Information

X24C04: 512 x 8 CMOS Serial E²PROM



Part Mark Convention

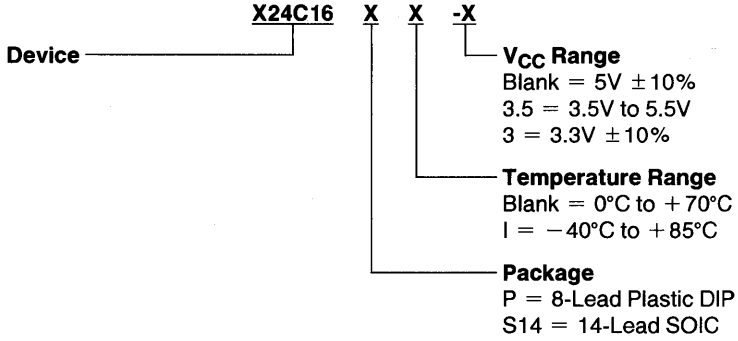
X24C04 **X** — Blank = 8-Lead SOIC
P = 8-Lead Plastic DIP
S = 14-Lead SOIC

X

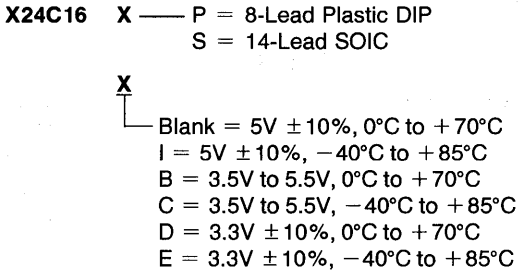
Blank = 5V ±10%, 0°C to +70°C
I = 5V ±10%, −40°C to +85°C
B = 3.5V to 5.5V, 0°C to +70°C
C = 3.5V to 5.5V, −40°C to +85°C
D = 3.3V ±10%, 0°C to +70°C
E = 3.3V ±10%, −40°C to +85°C

Ordering Information

X24C16: 2K x 8 CMOS Serial E²PROM

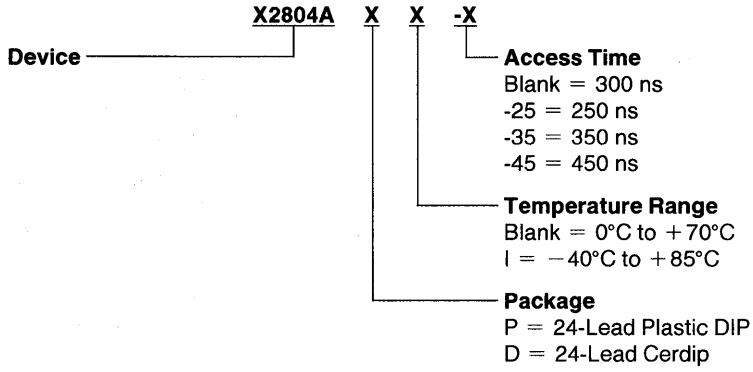


Part Mark Convention

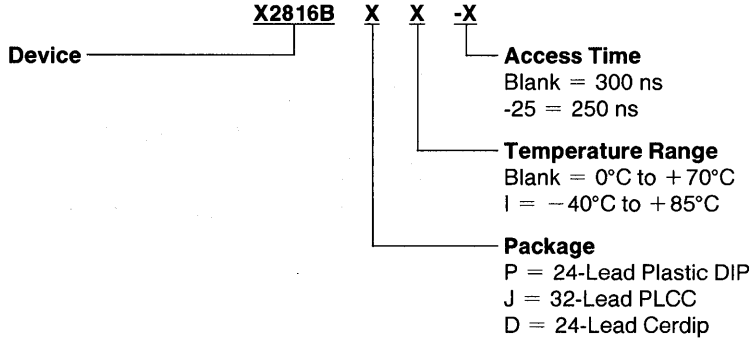


Ordering Information

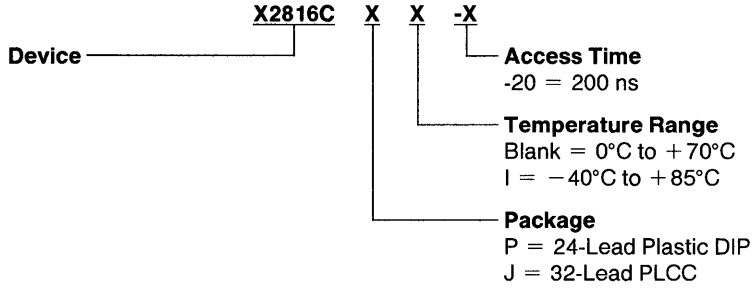
X2804A: 512 x 8 E²PROM



X2816B: 2K x 8 E²PROM

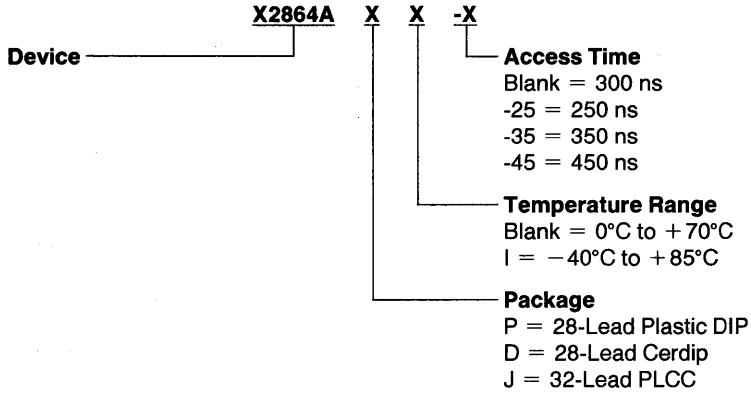


X2816C: 2K x 8 E²PROM

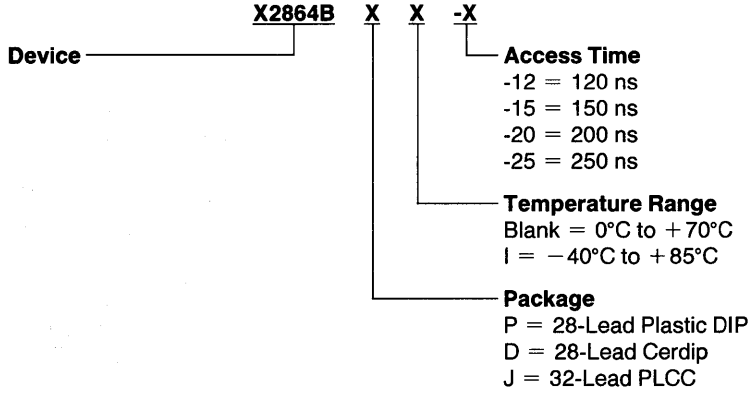


Ordering Information

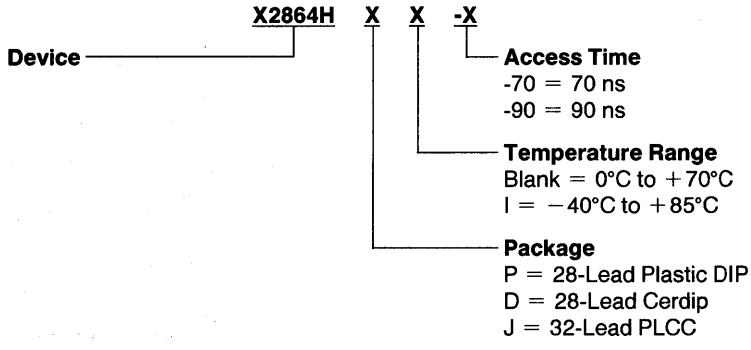
X2864A: 8K x 8 E²PROM



X2864B: 8K x 8 E²PROM

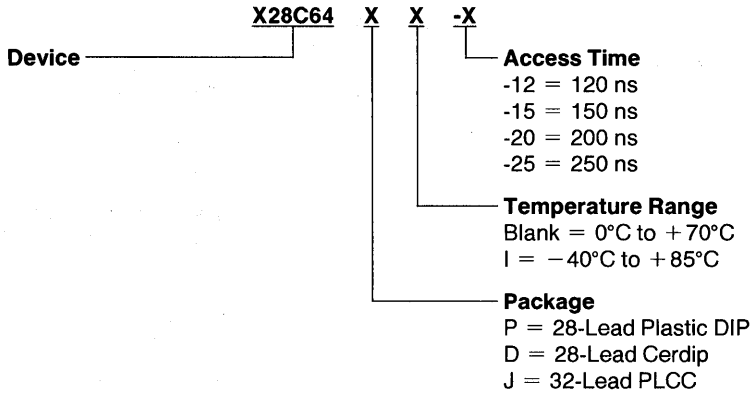


X2864H: 8K x 8 E²PROM

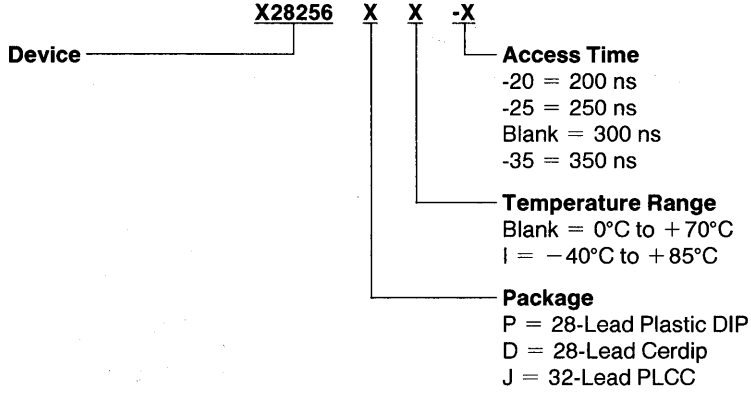


Ordering Information

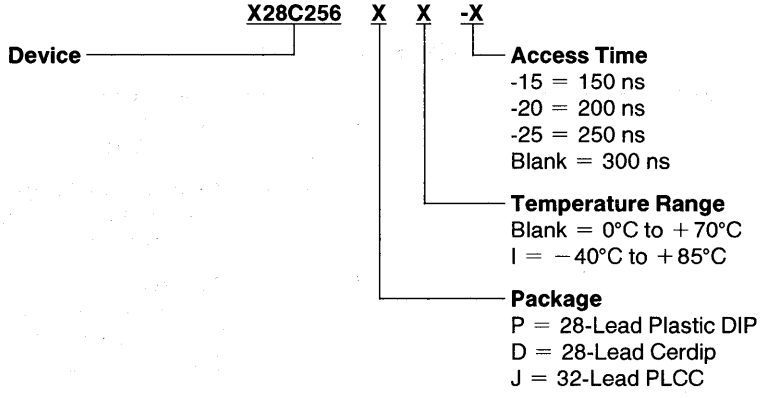
X28C64: 8K x 8 CMOS E²PROM



X28256: 32K x 8 E²PROM

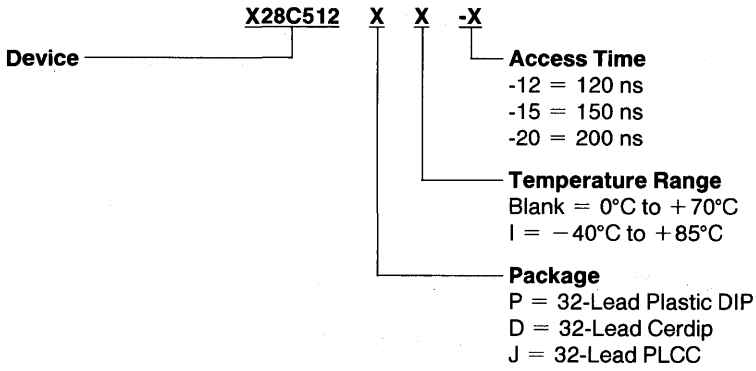


X28C256: 32K x 8 CMOS E²PROM

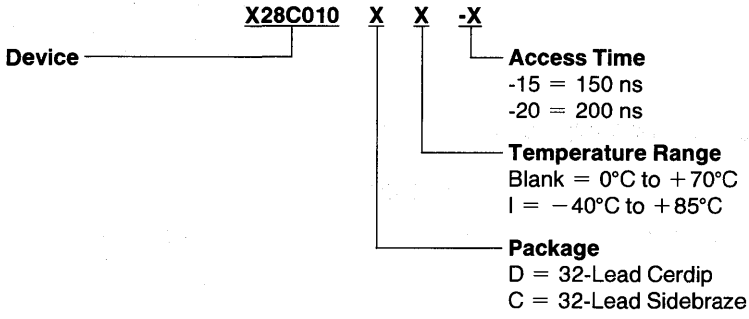


Ordering Information

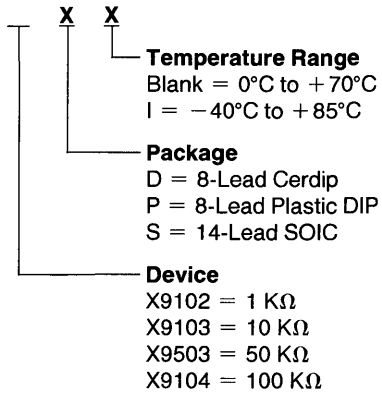
X28C512: 64K x 8 CMOS E²PROM



X28C010: 128K x 8 CMOS E²PROM



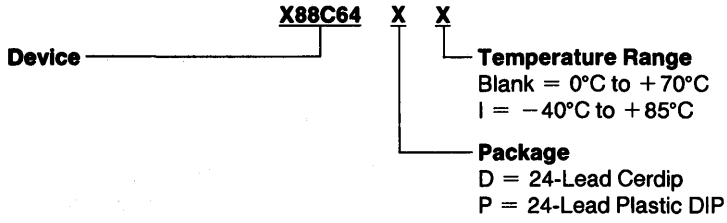
X9MME: E²POT 1K, 10K, 50K, 100K Ohms



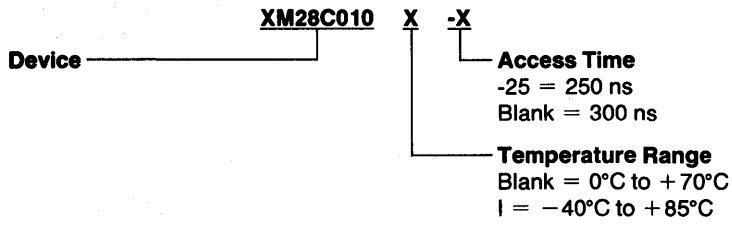
10

Ordering Information

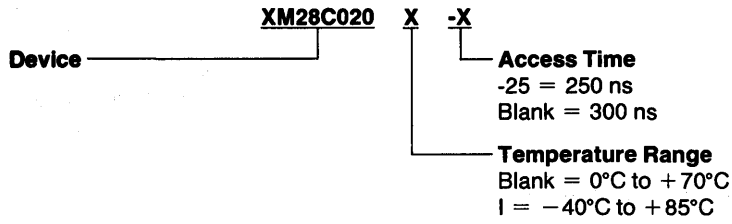
X88C64: 8K x 8 CMOS Peripheral E²PROM



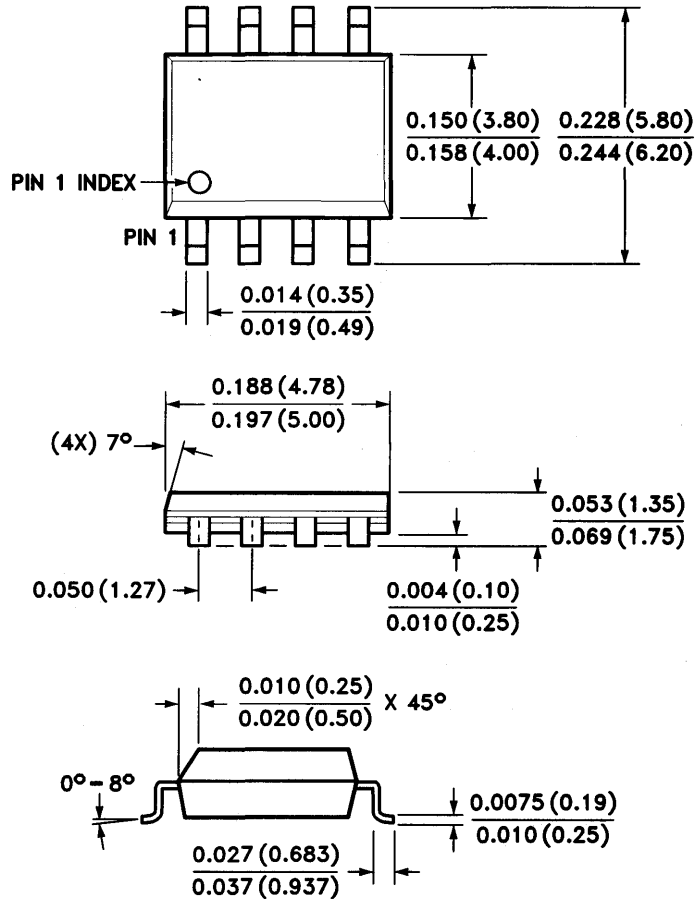
XM28C010: 128K x 8 CMOS E²PROM Memory Module



XM28C020: 128K x 8 CMOS E²PROM Memory Module



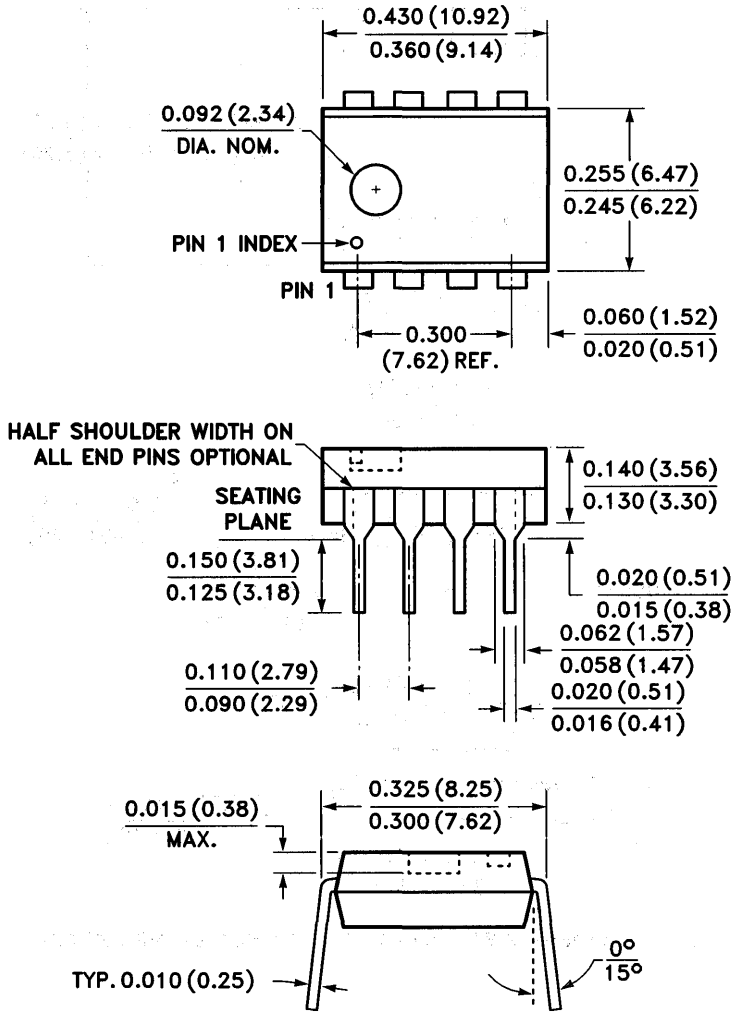
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



PSE008

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

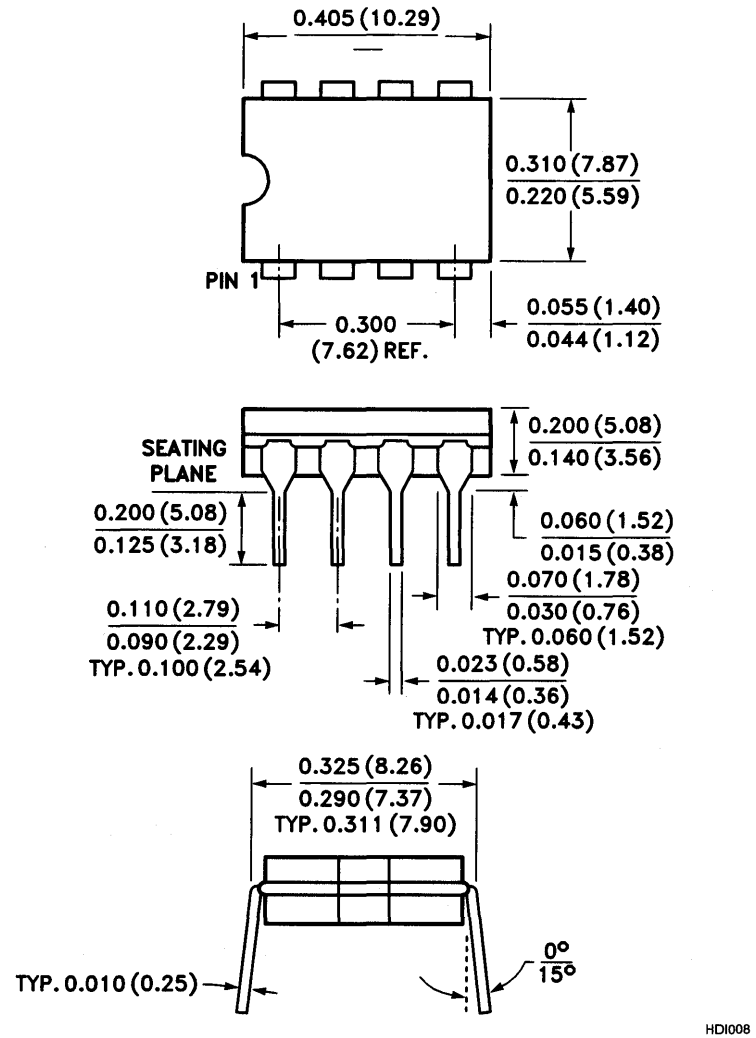
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI008

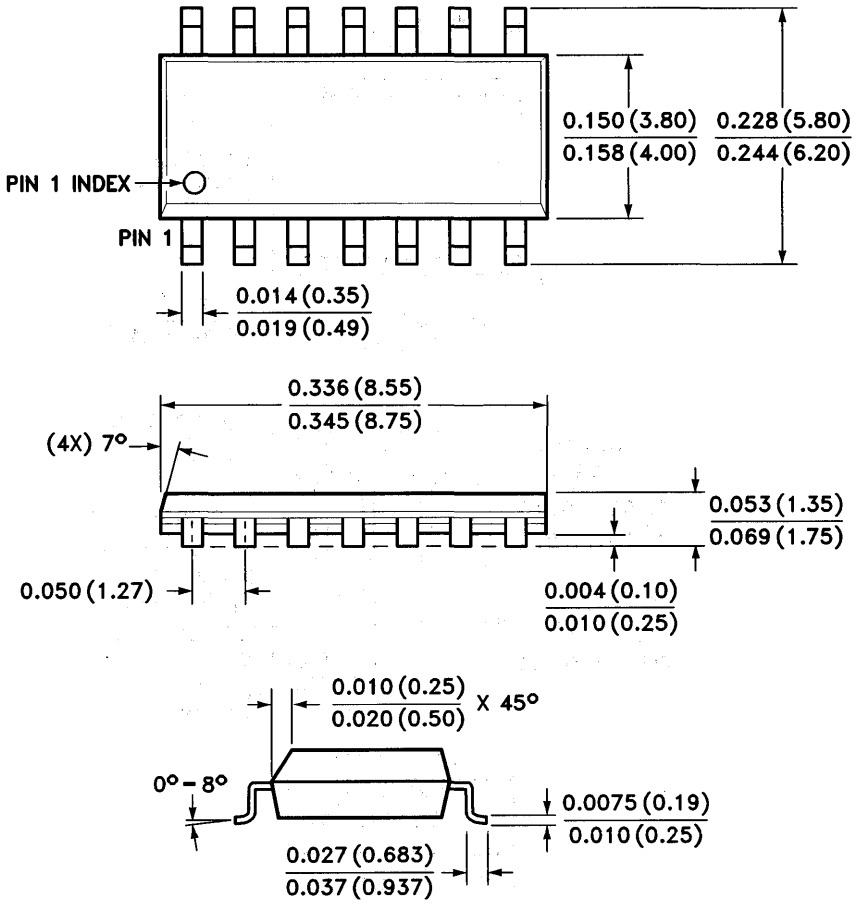
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

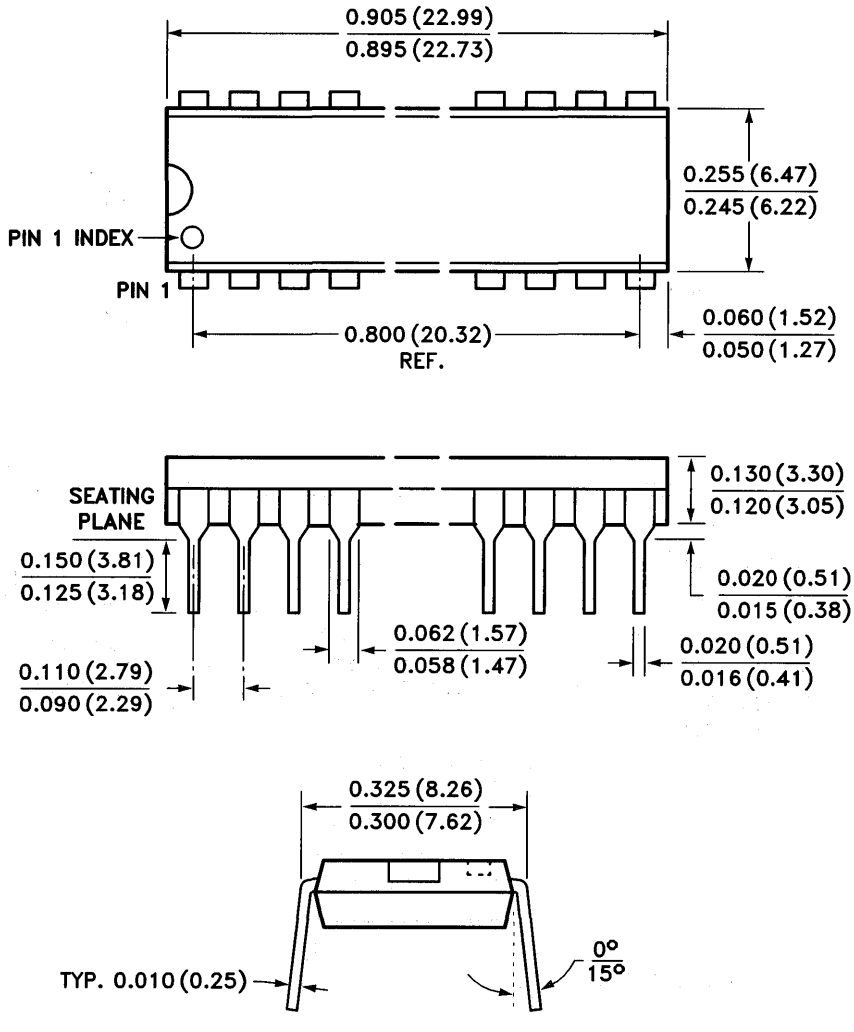
14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



PSE014

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

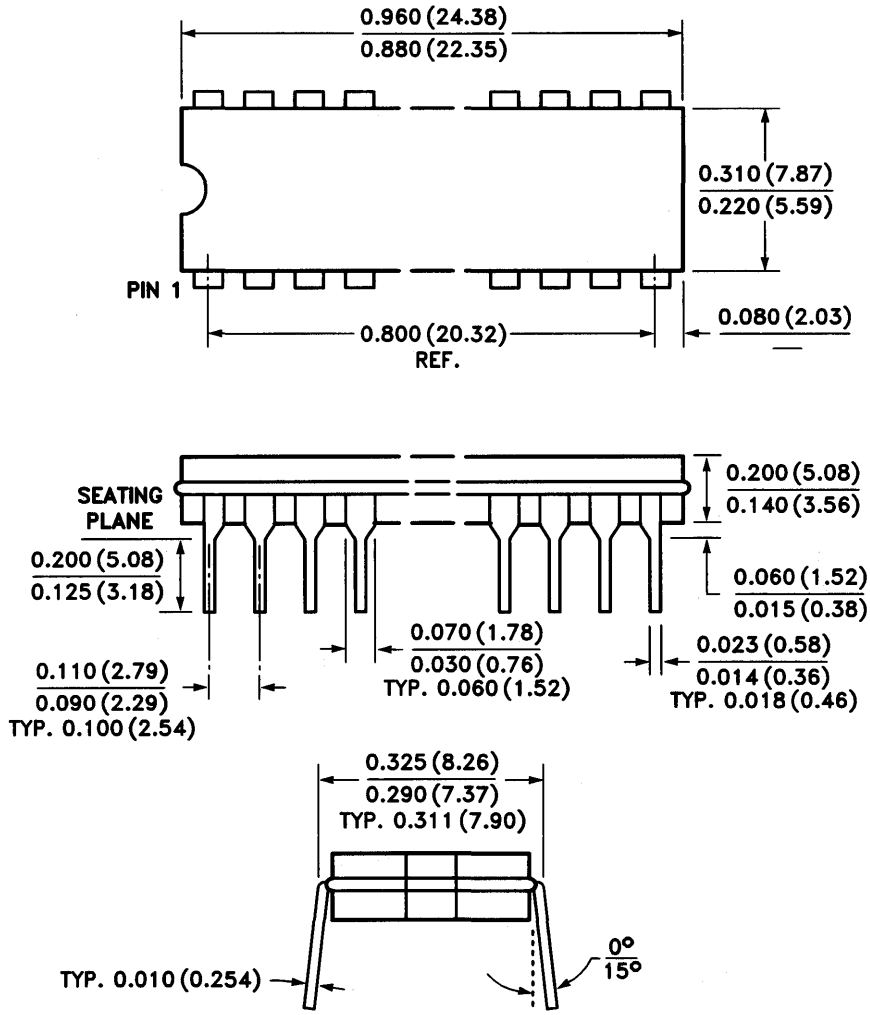


PPI018

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

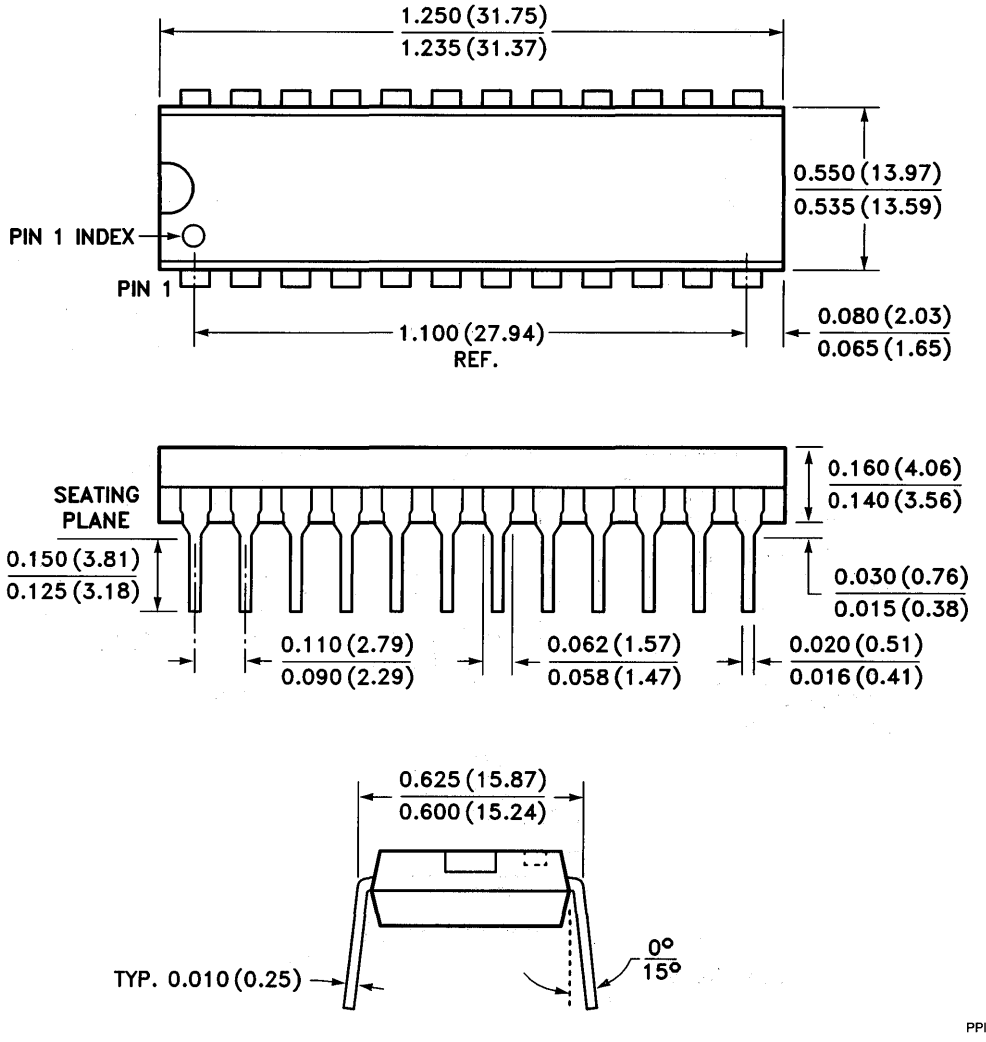
18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



HDI018

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

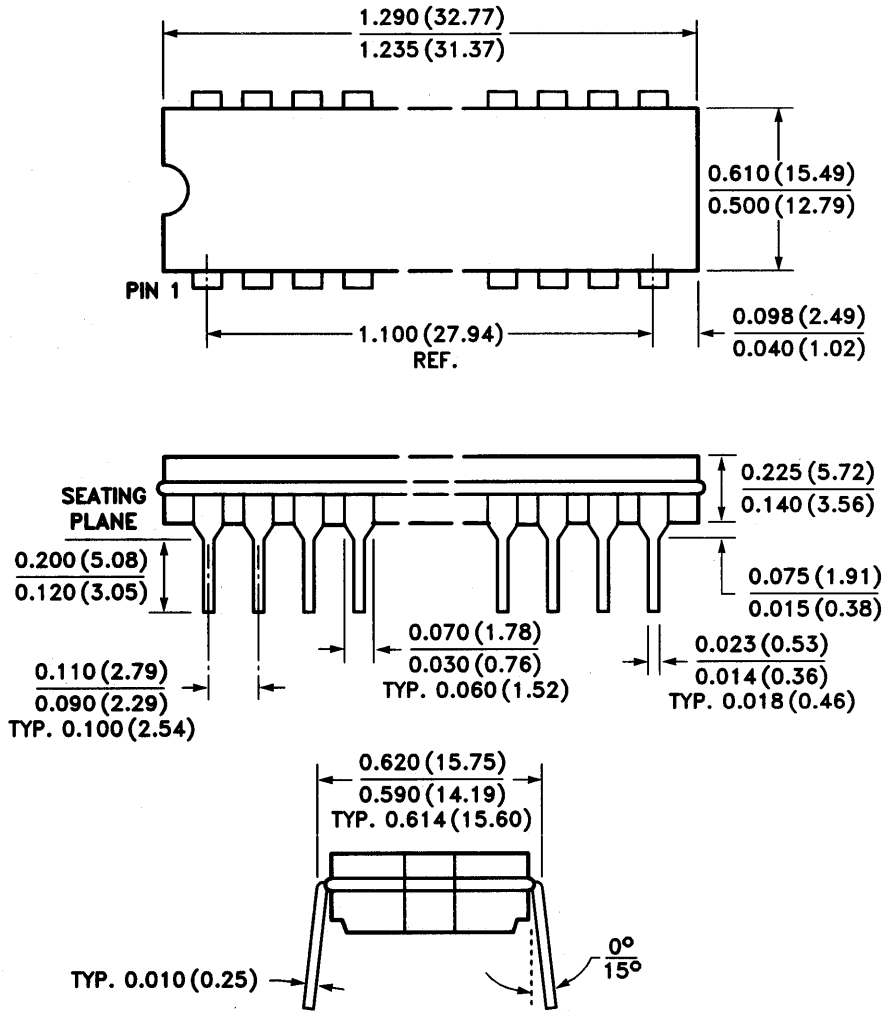


PPI024

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Packaging Information

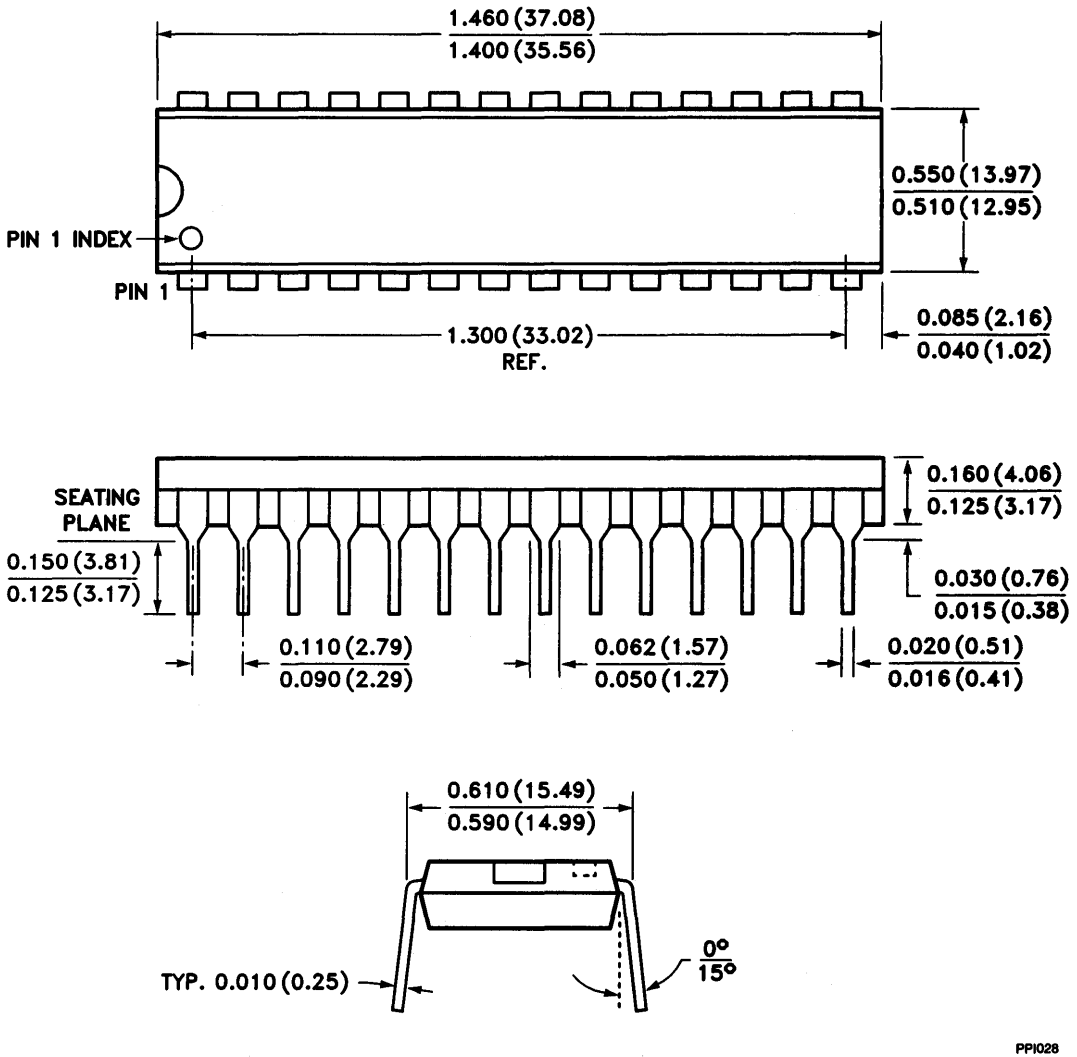
24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



HDI024

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

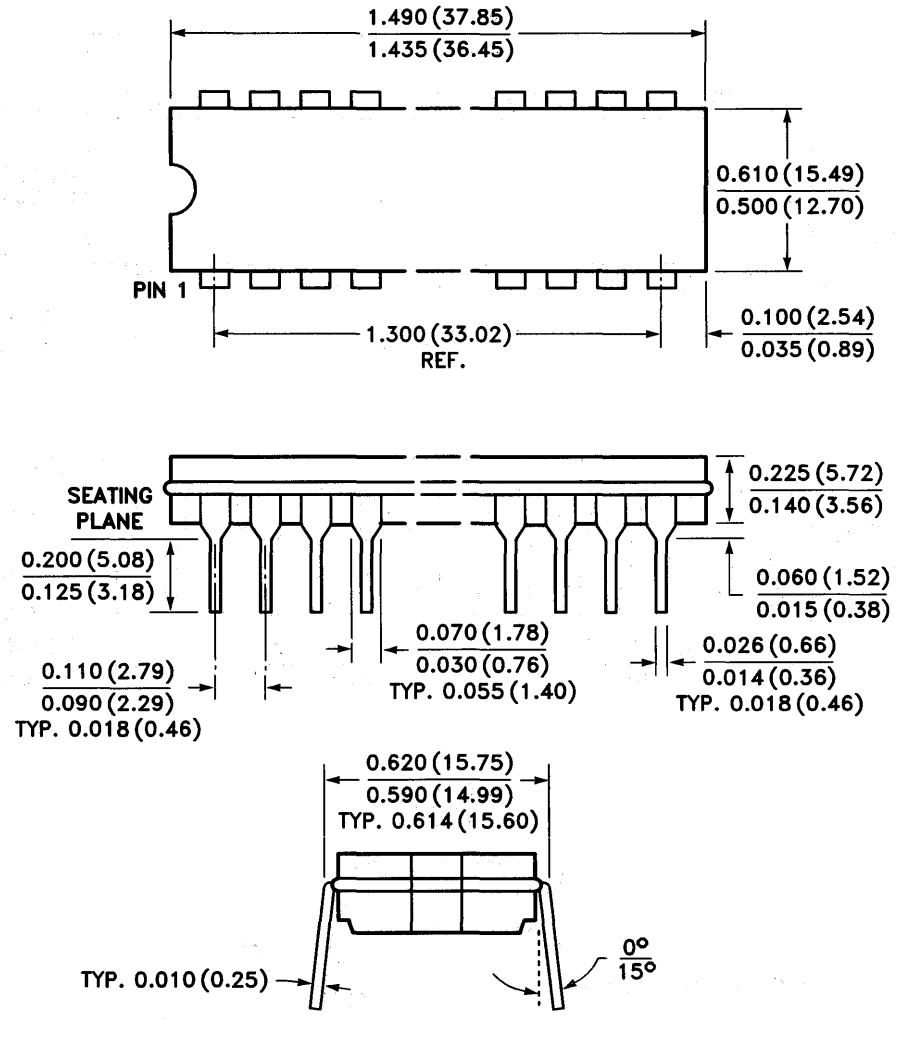
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

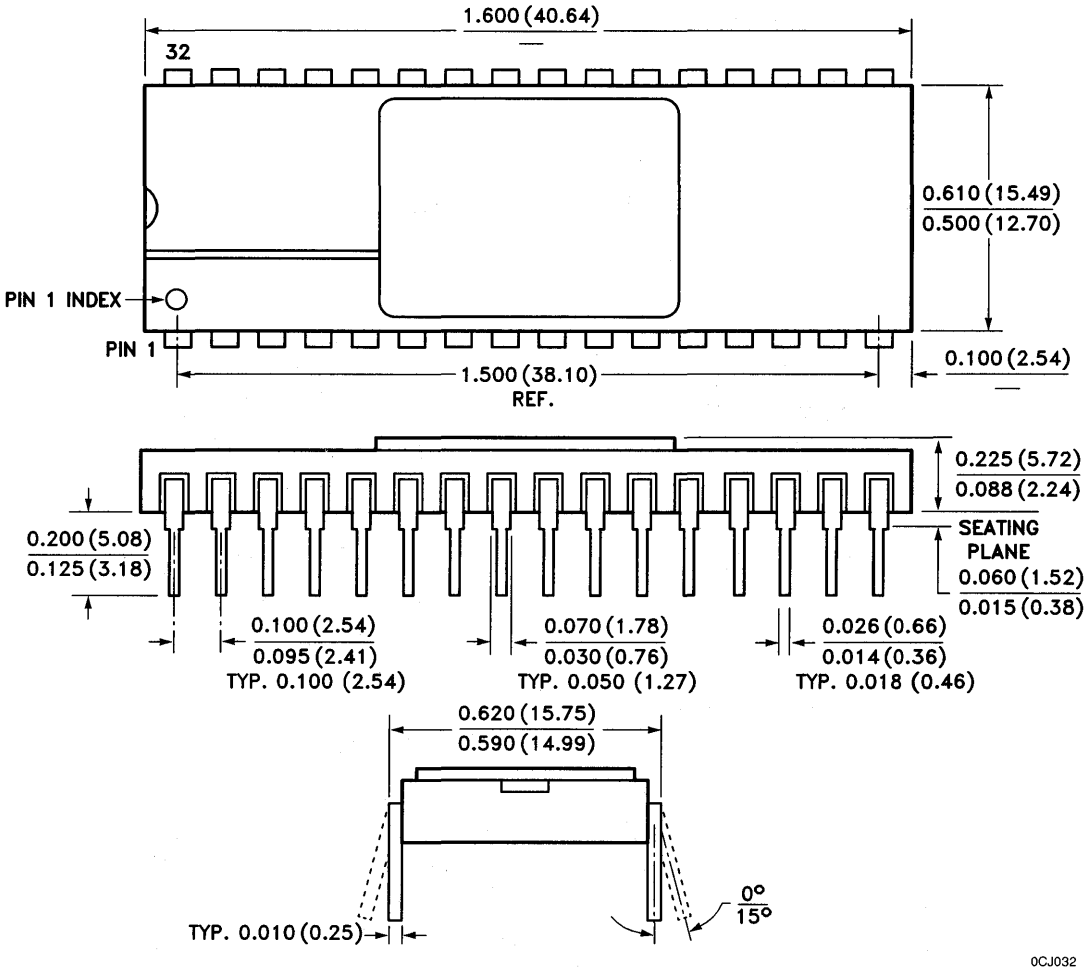
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



HDI028

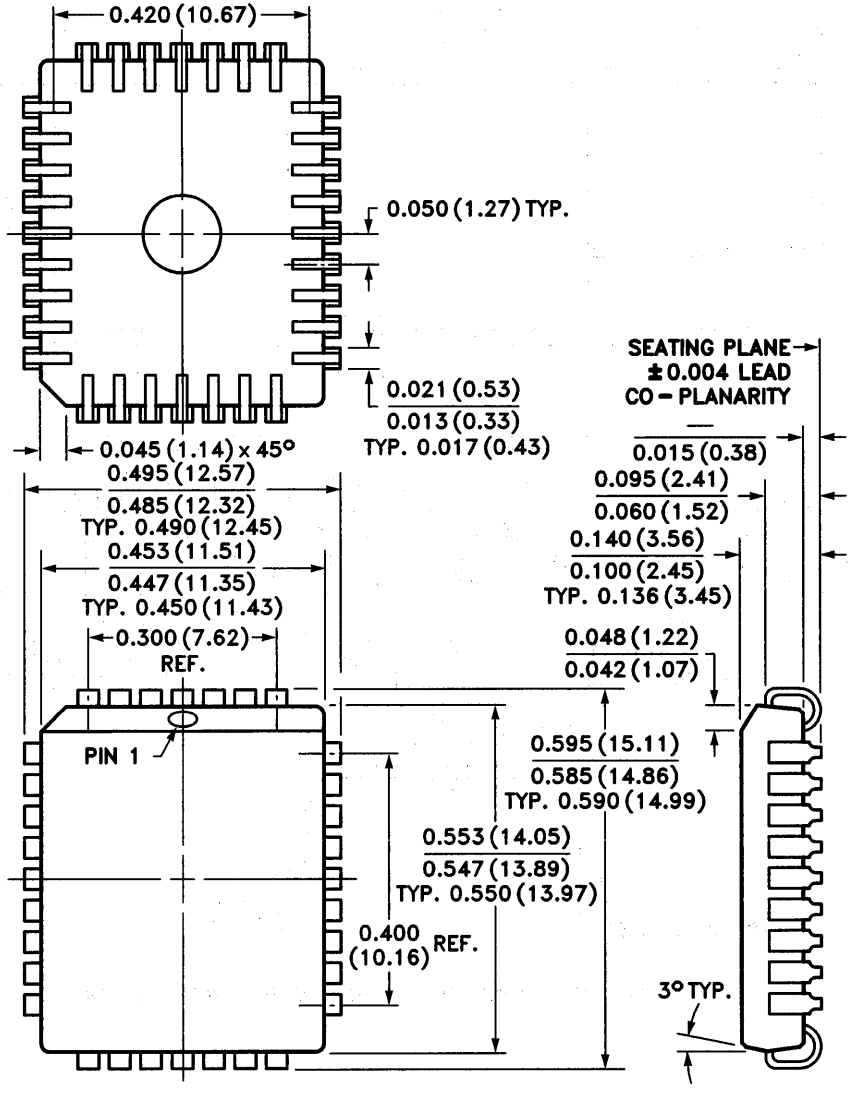
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

32-LEAD SIDE BRAZE PACKAGE TYPE C



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

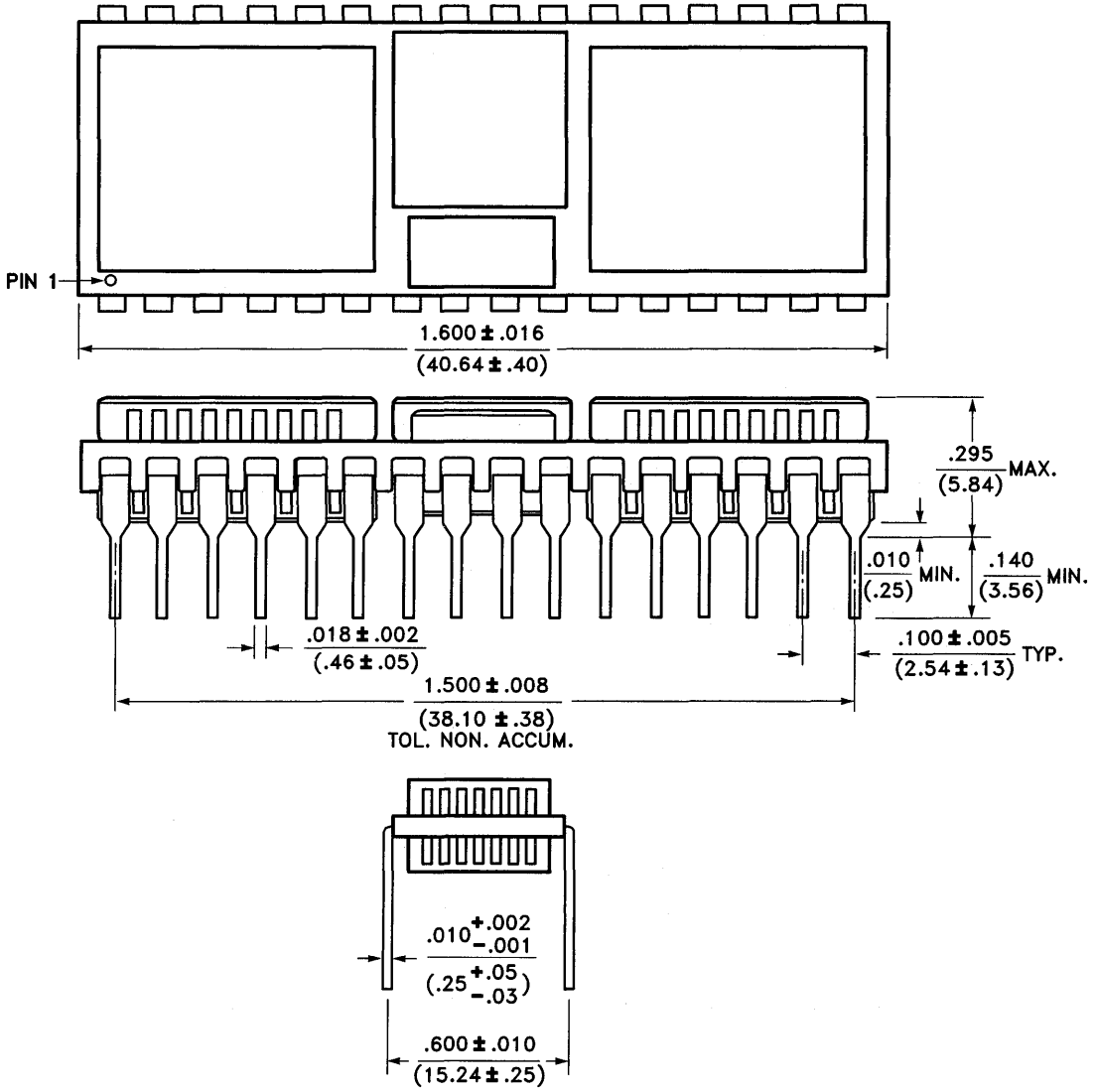
32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



PJG032

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

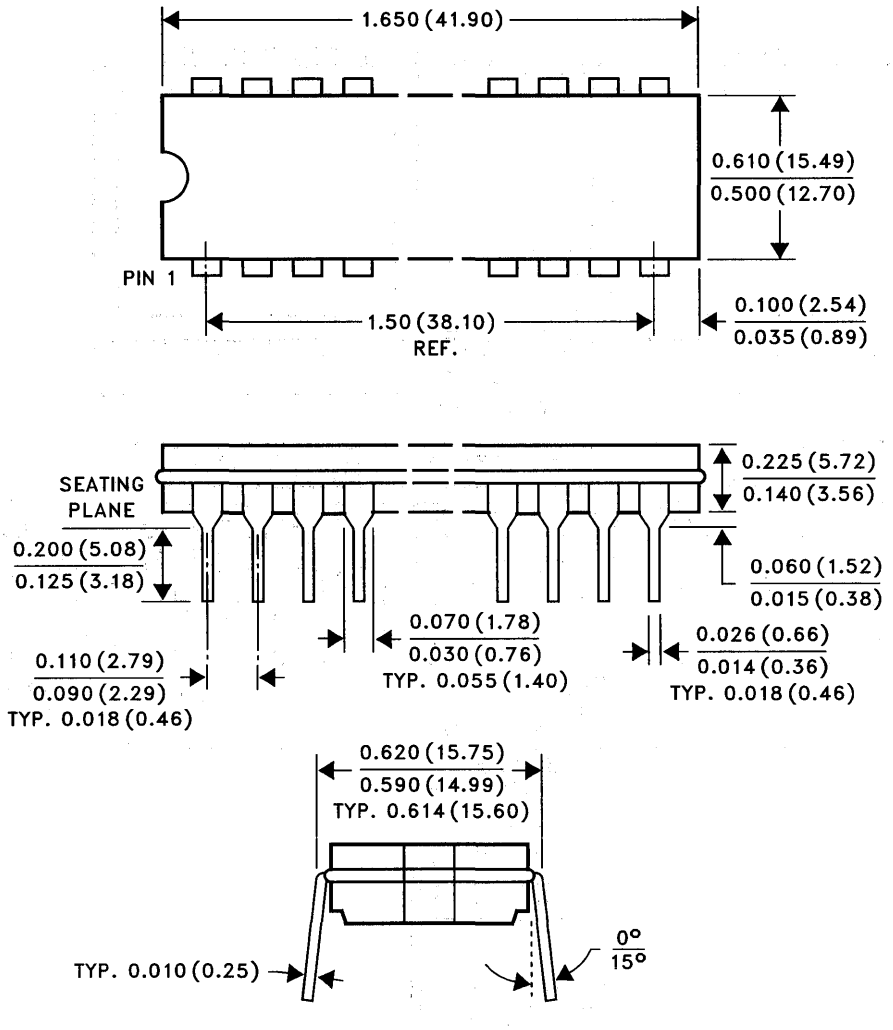
32-PIN DUAL-IN-LINE PACKAGE
CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE



CEAA32

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



HDI032

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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