AVR® DA Training Manual

Core Independent Solution Using AVR DA Peripherals Lab

Introduction

Plenty of computation in the embedded solutions can be done independently from the core, thus reducing the load and program memory space used. Most Microchip microcontrollers are equipped with Core Independent Peripherals (CIPs), which can facilitate the processing outside the core and can strengthen the hardware capabilities of the microcontroller.

The CIPs have key attributes that make them powerful and robust. Once initialized, they can provide a steady-state, closed-loop embedded control with no intervention from the CPU. They are smartly interconnected to allow latency-free sharing of data, logic inputs, or analog signals without additional code or interruption of the CPU. Last, but not least, they allow smaller, lower power MCUs to perform extremely complex tasks, such as high-power lighting control and communication.

This document includes an overview of the Configurable Custom Logic (CCL) peripheral, examples, and tips and tricks of its usage, such as how to implement basic functions using truth tables, how to apply delay to a signal, and how to divide a signal.

For a better understanding of the CCL peripheral and its advantages, this training contains a core independent solution: generating a visual SOS signal on the CNANO board LED, with involvement of the core only during the initialization part.

Starting from the Morse representation of the signal, using dots and dashes, this document will present the waveform associated with the SOS message, along with the peripherals used and additional waveforms.

At the end of the document, there will be steps that can be followed in order to generate the SOS signal using MPLAB® MCC and MPLAB® X IDE.

Prerequisites

Hardware requirements:

- AVR128DA48 Curiosity Nano (DM164151)

Software requirements:

- MPLAB® X Integrated Development Environment (IDE), version 5.40 or above
- MPLAB® Code Configurator (MCC), version 3.95.0 or above
- MPLAB® XC8 Compiler, version 2.20 or above
- MCC 8-bit AVR® MCUs Library, version 2.3.0

Documentation Materials:

- AVR128DA28/32/48/64 Data Sheet
- AVR128DA48 Device Overview
- MPLAB Code Configurator User's Guide

Table of Contents

1. Configurable Custom Logic (CCL)

1.1 Overview

The CCL is a programmable logic peripheral that can be connected to the device pins, to events, or to other internal peripherals. It serves as a 'glue logic' between the device peripherals and external devices.

The CCL can eliminate the need for external logic components and can also help the designer overcome real-time constraints by combining it with other Core Independent Peripherals (CIPs), to handle the time-critical parts of the application, independent of the CPU.

The CCL peripheral on the AVR128DA48 provides six Look-up Tables (LUTs). Each LUT consists of three inputs, a truth table, a synchronizer/filter, and an edge detector. This allows the user to generate an output as a programmable logic expression, with up to three inputs.

The CCL can be configured to filter the output value and to generate an interrupt request, on changes in the LUT outputs.

Neighboring LUTs can be combined to perform specific operations and the sequencers can be used for generating complex waveforms.

1.2 Implementing Logic Function Using TRUTH Tables

Each LUT has three inputs and one truth table. This allows implementation of logic functions with up to three inputs and one output; with the unused inputs that can be tied low (masked).

The truth table for the desired combinational logic expression is defined by the bits in the LUTn Truth Table (CCL.TRUTHn) registers. Each combination of the input bits corresponds to one bit in this register.

Table 1-1. Truth Table of a LUT

LUTn-TRUTHSEL[2]	LUTn-TRUTHSEL[1]	LUTn-TRUTHSEL[0]	OUT
0	0	0	TRUTH[0]
0	0	1	TRUTH[1]
0	1	0	TRUTH[2]
0	1	1	TRUTH[3]
1	0	0	TRUTH[4]
1	0	1	TRUTH[5]
1	1	0	TRUTH[6]
1	1	1	TRUTH[7]

1.2.1 Logic Functions Examples

As already mentioned, the truth tables allow implementation of any combinational logic function of up to three inputs and one output. This section will provide two examples of standard functions that can be implemented.

1. **Logic OR with Three Inputs**
   The truth table for the OR function with three inputs is presented in the table below:

IN2	IN1	IN0	IN0 OR IN1 OR IN2
0	0	0	0
0	0	1	1

.....continued

IN2	IN1	IN0	IN0 OR IN1 OR IN2
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

In order to implement this logic function with a Truth table, the bits from the CCL.TRUTHn register should have the same value as their correspondents from the table above. This translates to the following configuration:

CCL.TRUTHn = 0xFE

2. **Logic AND with Two Inputs**
   The truth table for the AND function with two inputs is presented in the table below:

X	IN1	IN0	IN0 AND IN1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

Because there are only two inputs, the third input channel is tied low (IN2 = 0). In order to implement this logic function with a truth table, the bits from the CCL.TRUTHn register should have the same value as their correspondents from the table above. This translates to the following configuration:

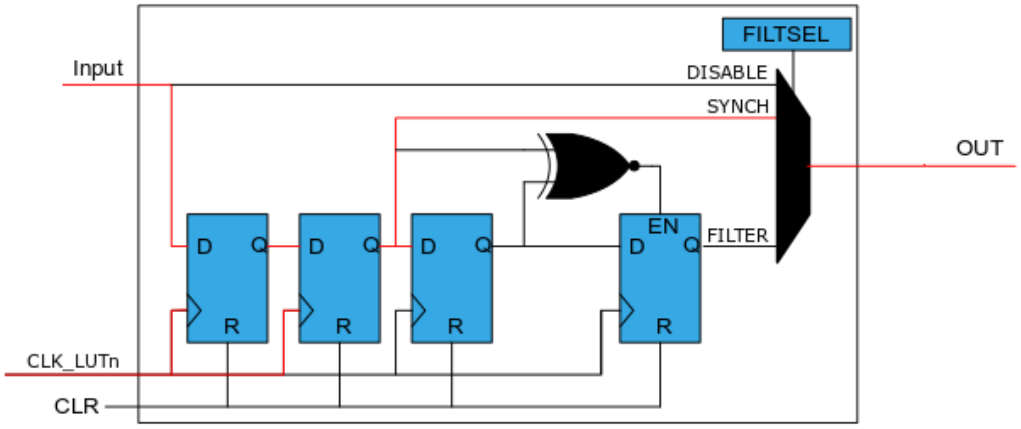
CCL.TRUTHn = 0x08

1.3 Using Filter Configuration for Additional Features

One of the most common operations that needs to be performed when working with combinational logic is applying a delay (fixed number of clock cycles). The CCL can do this by writing the Filter Selection (FILTSEL) bit field in the LUT n Control A (CCL.LUTnCTRLA) registers.

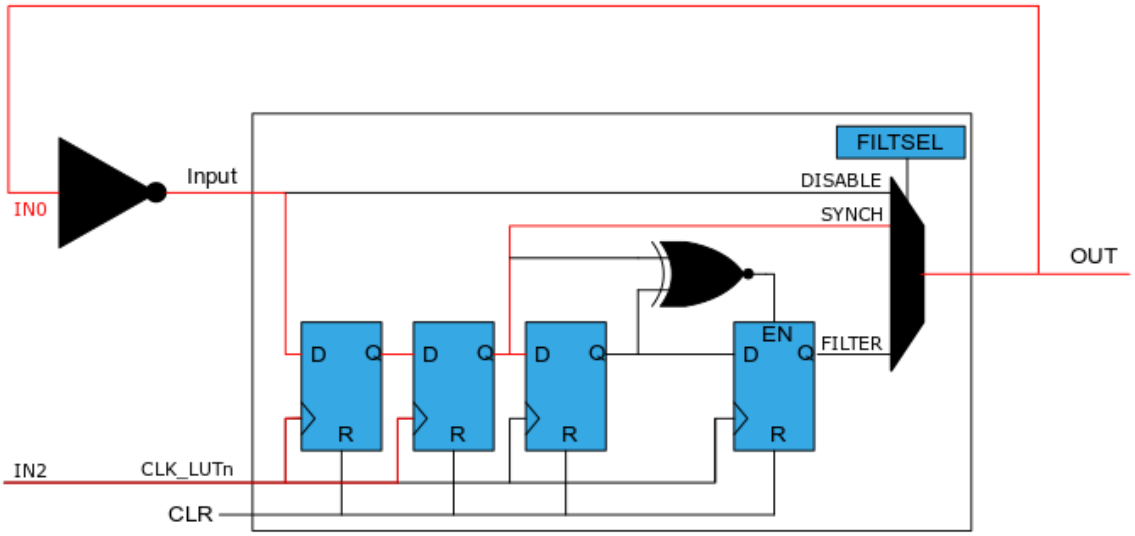
When FILTSEL=SYNCH, the configuration can be used to synchronize the output with CLK_LUTn and to obtain two CLK_LUTn cycles delays.

Figure 1-1. Two CLK_LUTn Cycles Delay



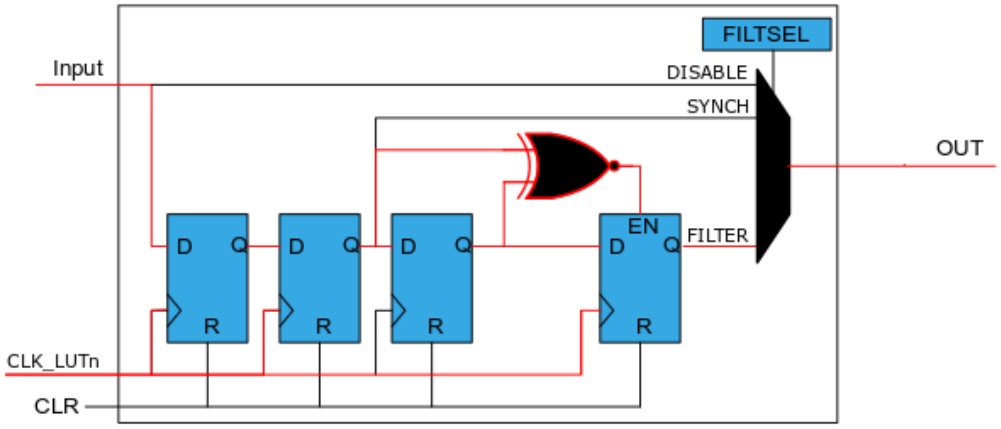
Using the LUT feedback feature, a divide by four configuration is obtained. The signal that will be divided must be used as clock input for the LUT and the output of the LUT must be linked to the input.

Figure 1-2. Divide by Four Configuration



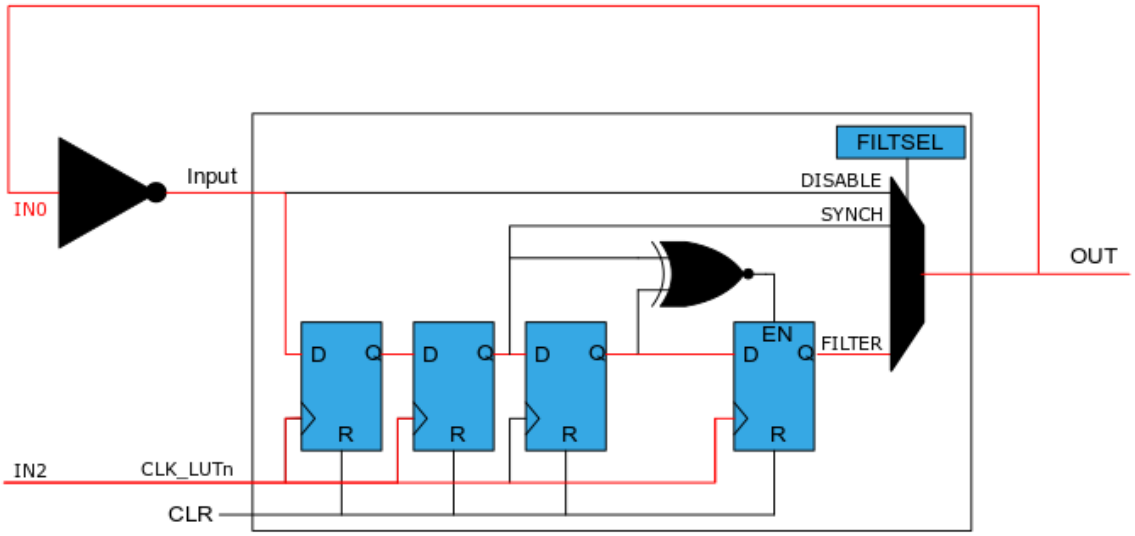
When FILTSEL=FILTER and input signal have at least four input clocks, the output will be delayed by four clock cycles.

Figure 1-3. Four CLK_LUTn Cycles Delay



Using LUT feedback feature, a divide by eight configuration is obtained. The signal that will be divided must be used as clock input for the LUT and the output of the LUT must be linked to the input.

Figure 1-4. Divide by Eight Configuration



2. Core Independent Example – SOS Sequence Generator

The following example will show how to generate an SOS signal without CPU intervention. The CCL peripheral is used together with Timers and the Event System to create the sequence and, aside from the initialization part, all operations are done independently from the core. The SOS sequence will be displayed using the CNANO board LED.

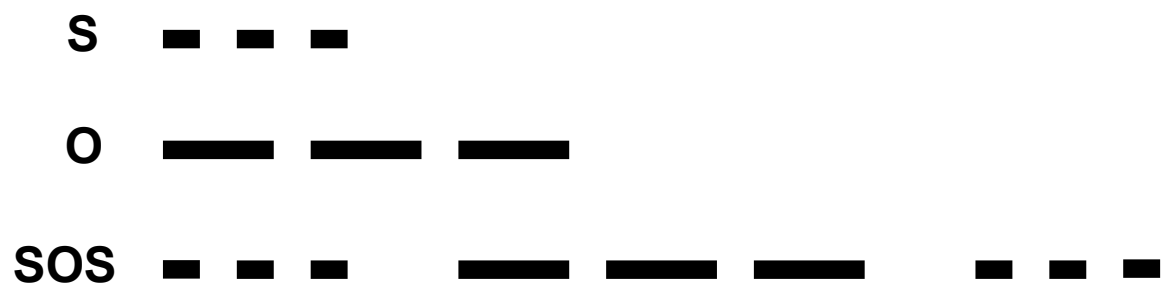
2.1 SOS Sequence Morse Code Basics

Morse code is a method of encoding text characters using symbols: dots and dashes. There are rules to distinguish the dots from dashes:

- The length of a dot is one-time unit
- The length of a dash is three-time units
- The space between symbols (dots and dashes) of the same letter is one-time unit
- The space between letters is three-time units
- The space between words is seven-time units

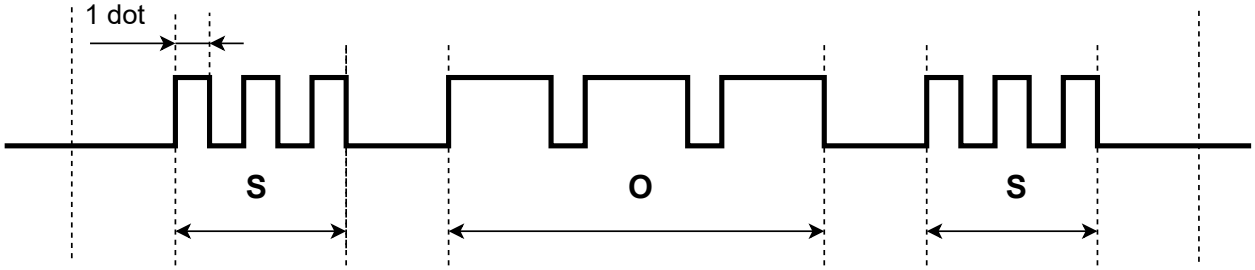
Each letter has a unique representation in the Morse code. The letter ‘S’ is formed of three dots, while the letter ‘O’ is of three dashes.

Figure 2-1. Morse Representation of Letters S and O



In a digital representation, the dots and dashes can be pulses (1 logic), while the spaces can be 0 logic. This translates to the following waveform:

Figure 2-2. SOS Digital Waveform



The SOS message will be repeated continuously, which means the SOS waveform will be periodical. The period of the waveform is represented in the diagram above by the interval between the first and the last vertical dotted line.

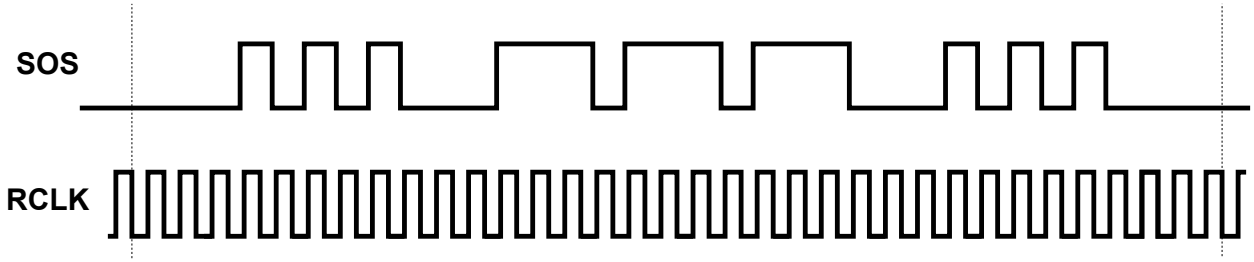
Because the space between the words is seven-dot long, the period will have a length of 34 dots.

2.2 SOS Sequence Logic Function Implementation

Before generating the waveforms, a time reference is needed. The dot has a period of 50 ms that translates to a duration of 34x50 = 1700 ms for the entire SOS waveform period. Starting from AVR resources, a symmetrical

sequence is much easier to implement. To create this symmetry, the period of the reference clock should be half of the dot period (25 ms).

Figure 2-3. Reference Clock



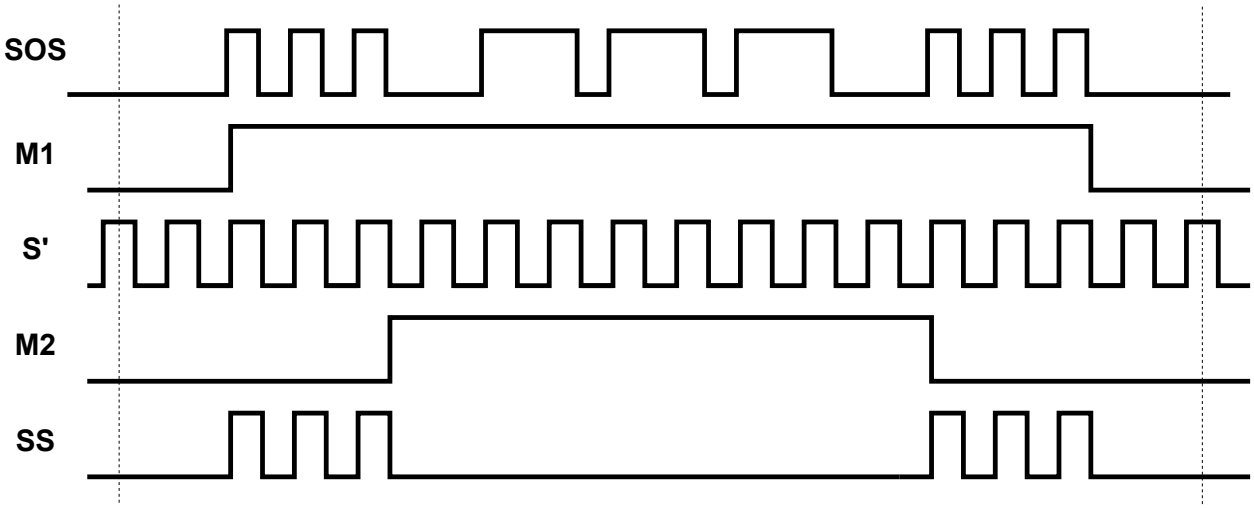
The process of generating the SOS signal can be split into three parts:

- Generating the waveform for the letters ‘S’
- Generating the waveform for the letter ‘O’
- Combining the waveforms

2.2.1 Generate the Waveform for the Letters ‘S’

The waveform of the letters ‘S’ can be obtained by generating a waveform that contains the pattern for the letter and the two signals acting as masks and applying a logic function on them.

Figure 2-4. Waveform for the Letters S



The operation mentioned above is: SS = M1 AND $\overline{M2}$ AND S’

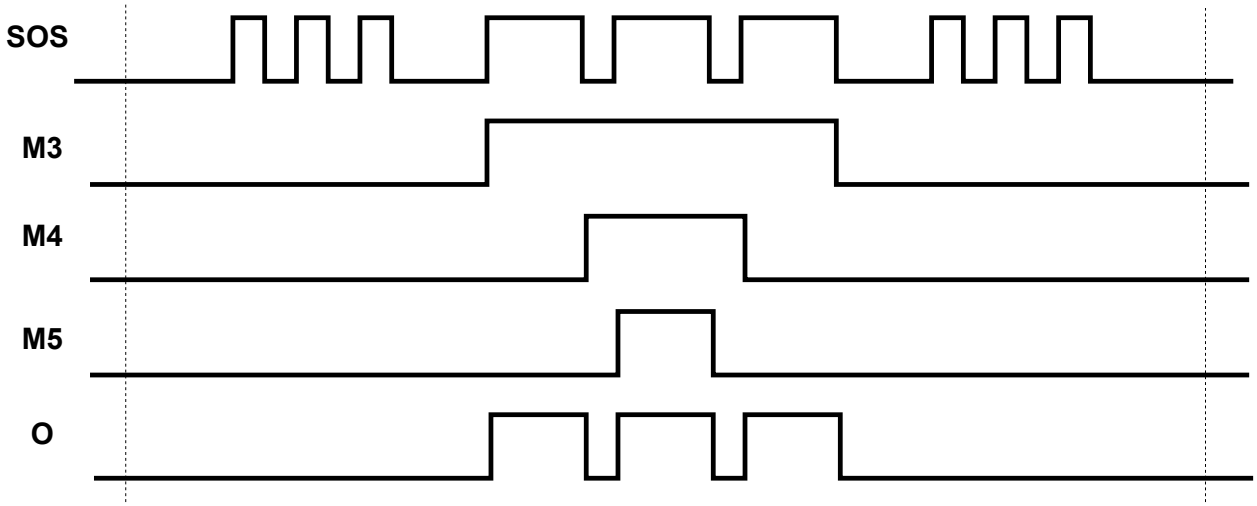
The truth table of the logic operation is presented in the table below:

M1	M2	S’	SS
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

2.2.2 Generate the Waveform for the Letter ‘O’

The waveform of the letter ‘O’ can be obtained by generating three signals acting as masks and applying a logic function on them.

Figure 2-5. Waveform for the Letter ‘O’



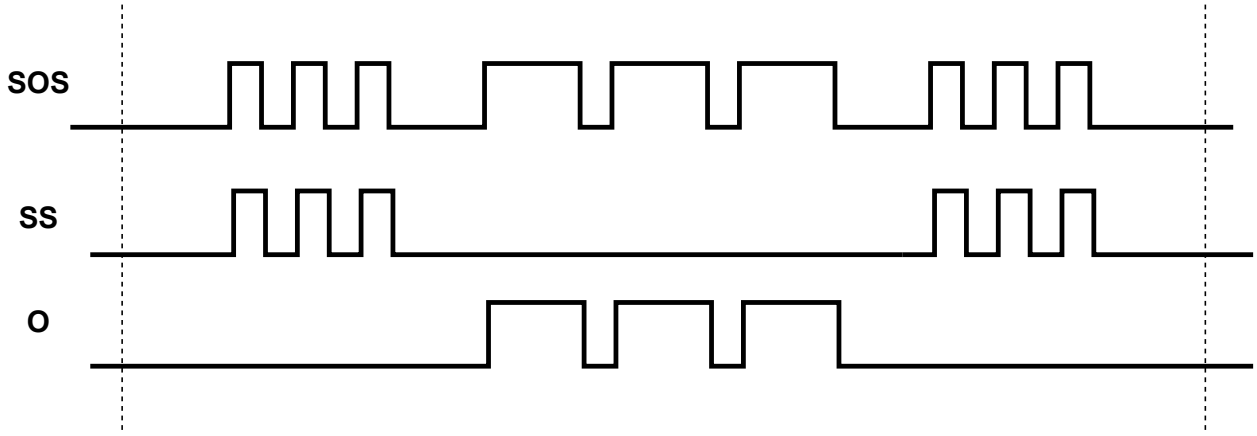
The truth table of the operation is shown in the table below:

M3	M4	M5	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2.2.3 Obtain the Waveform for the SOS Message

The SOS message waveform is obtained by performing an OR between SS and O waveforms: SOS = SS OR O

Figure 2-6. Waveform for SOS Message



2.3 Solution

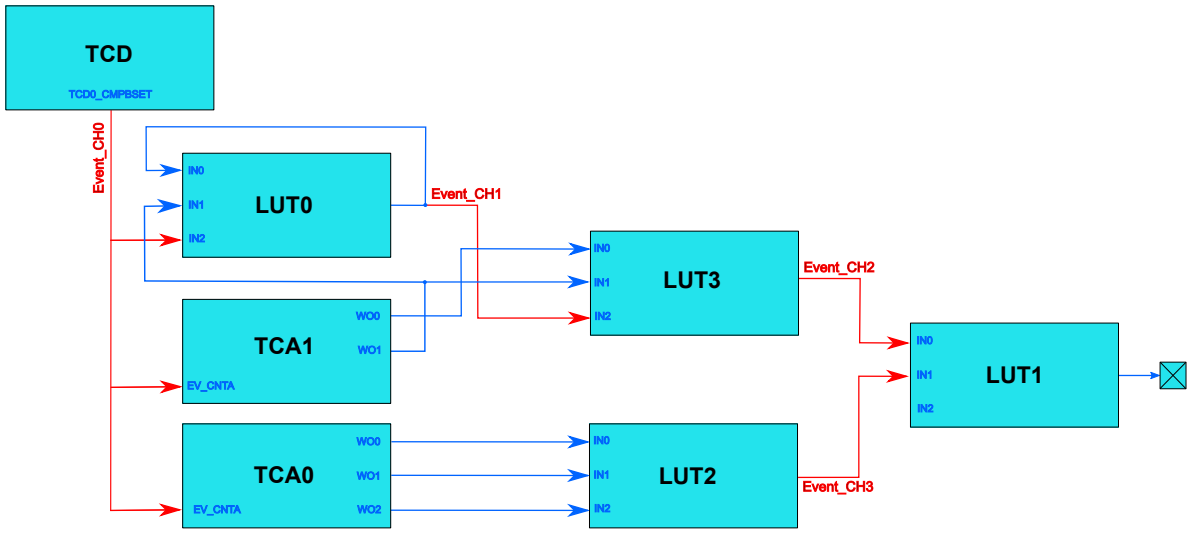
2.3.1 Block Diagram with Event System Connections

The peripherals used for implementing this application are:

- Timer/Counter Type A (TCA)
- Timer/Counter Type D (TCD)
- Configurable Custom Logic (CCL)
- Event System (EVSYS)

The block diagram below presents the peripherals and connections between them. The red-marked lines represent event channels, while the blue-marked lines represent internal signals.

Figure 2-7. Block Diagram



As mentioned in a section above, the reference clock must have a period of 25 ms (and a frequency of 40 Hz). It is generated using TCD0, which triggers events with that specific frequency. The event will be used as clock input for LUT0, TCA0, and TCA1.

TCA1 is used to generate M1 and M2 signals through TCA1-WO0 and TCA1-WO1 outputs, which will be connected to LUT0 and LUT3 as inputs.

TCA0 is used to generate M3, M4, and M5 signals through TCA0-WO2, TCA0-WO1, and TCA0-WO0 outputs, which will be connected to LUT2 as inputs.

LUT0 is used to generate the signal that contains the pattern for the letter ‘S’ (S’). The frequency of the S’ signal is double the frequency of the events that come from TCD0, because the Feedback feature was used.

LUT3 is used to perform the logic operation mentioned in Section 2.2.1 Generate the Waveform for the Letters ‘S’. Its output represents the SS signal and is connected with LUT1 through an event channel.

LUT2 is used to perform the logic operation mentioned in Section 2.2.2 Generate the Waveform for the Letter ‘O’. Its output represents the O signal and is connected with LUT1 through an event channel.

LUT1 is used to perform the logic operation mentioned in Section 2.2.3 Obtain the Waveform for the SOS Message and to output the SOS message on the CNANO board LED. Its inputs are represented by the events generated by LUT2 and LUT3.

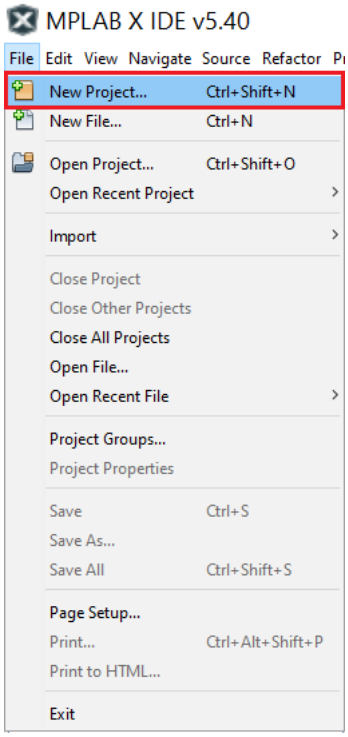
The EVSYS is used to interconnect the peripherals.

2.3.2 Step-by-Step Design Implementation Using MCC

Follow these steps to generate the project using MCC:

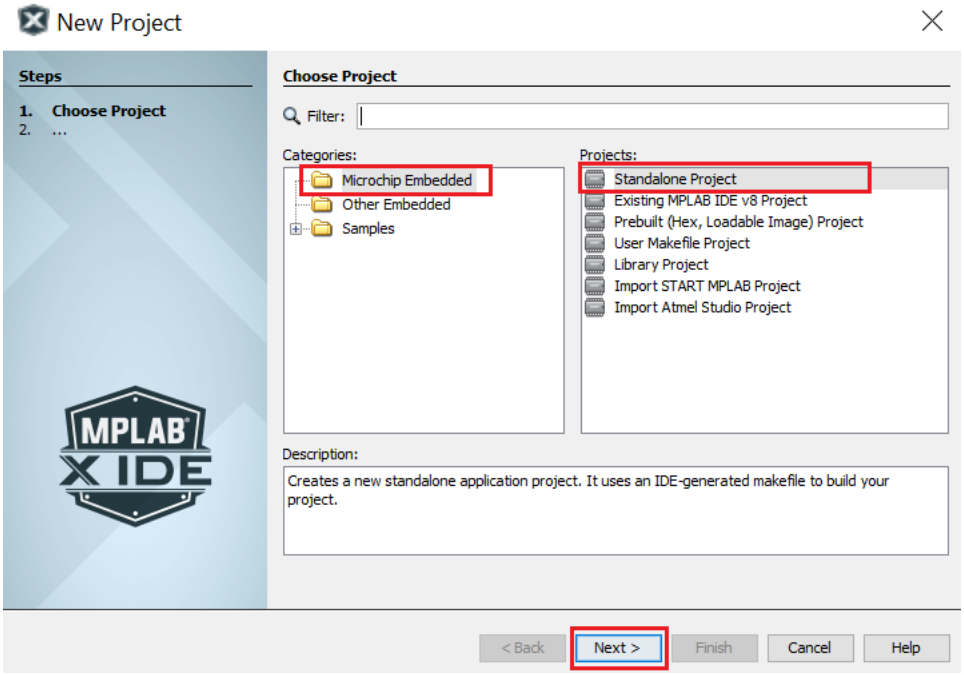
1. Create a new MPLAB X project for AVR128DA48.
   1.1. Open **MPLAB X IDE v 5.40**. Go to *File>New Project*.

Figure 2-8. Create New Project



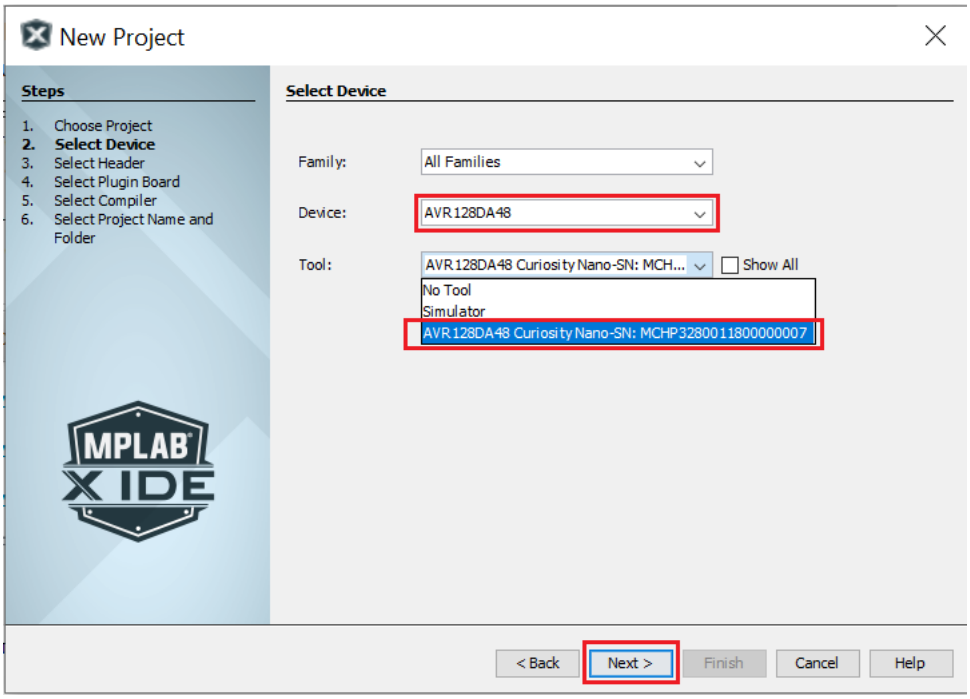
   1.2. From the window that appeared on the screen, select **Microchip Embedded**, followed by **Standalone Project**, and then click **Next**.

Figure 2-9. New Project – Choose Project



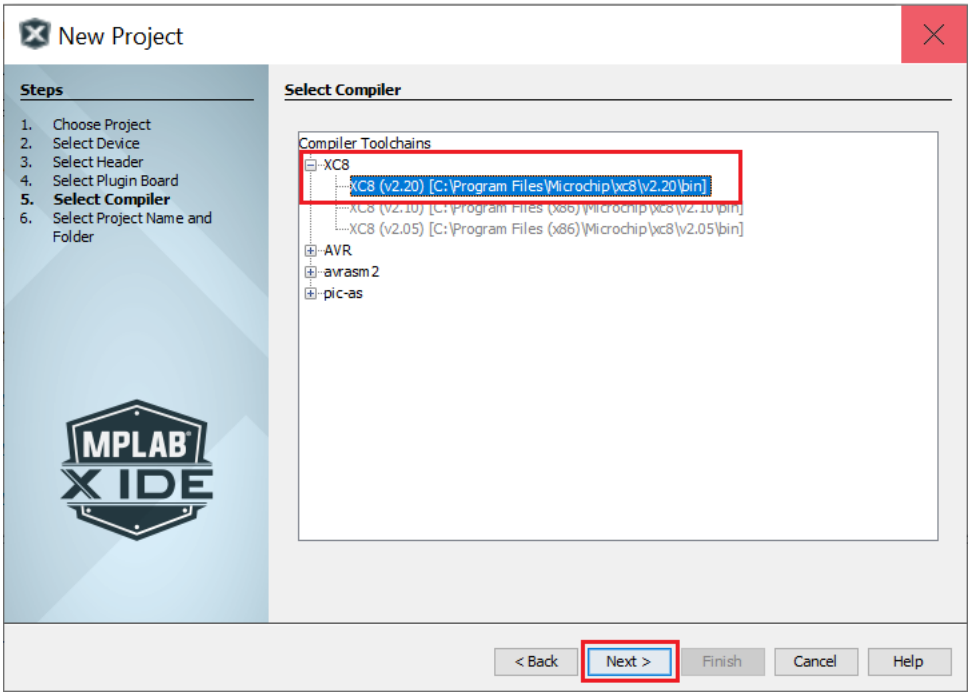
   1.3. Select **AVR128DA48** from the **Device** tab and the **AVR128DA48 Curiosity Nano** (click **SN**) from the **Tool** tab. Click **Next**.

Figure 2-10. New Project – Select Device



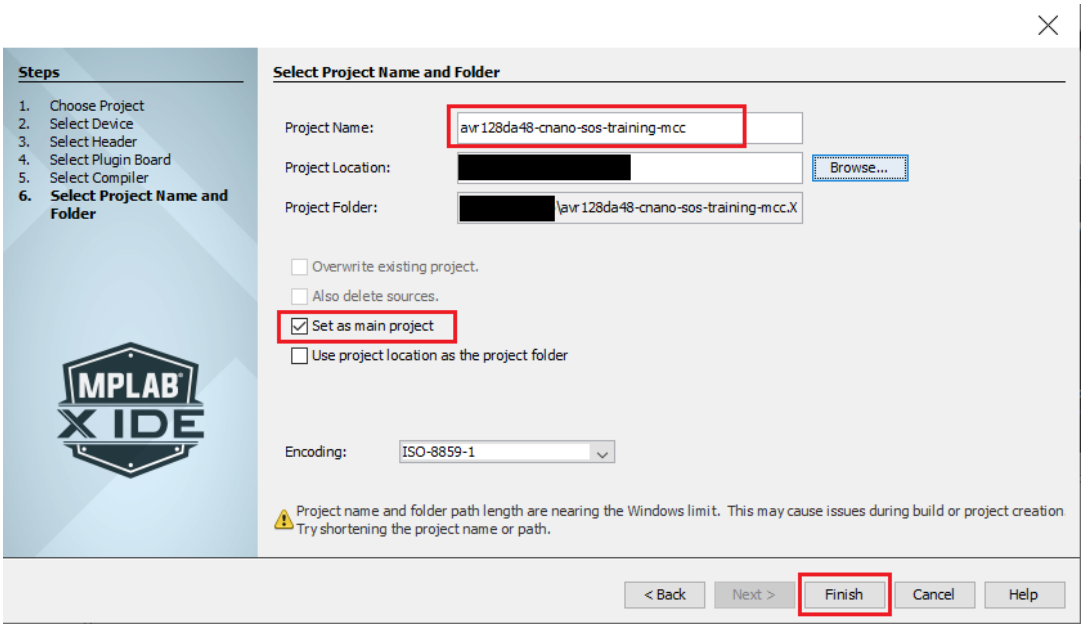
1.4. Select **XC8 (v2.20)** Compiler and click **Next**.

Figure 2-11. New Project – Select Compiler



1.5. Insert a name for the project and select the location where to be saved. Make sure that **Set as main project** is checked and click **Finish**.

Figure 2-12. New Project – Select Project Name and Folder

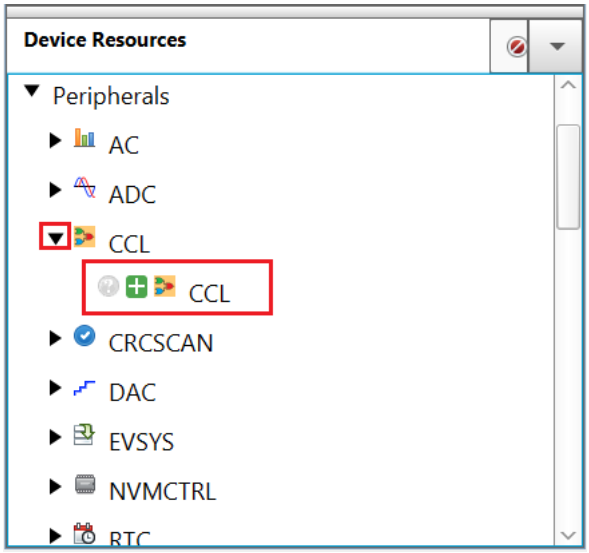


2. Open the **MCC** from the toolbar.
   If the MCC is not installed, please follow the instructions provided on the Install MPLAB® Code Configurator (MCC) webpage.

Figure 2-13. MCC Icon

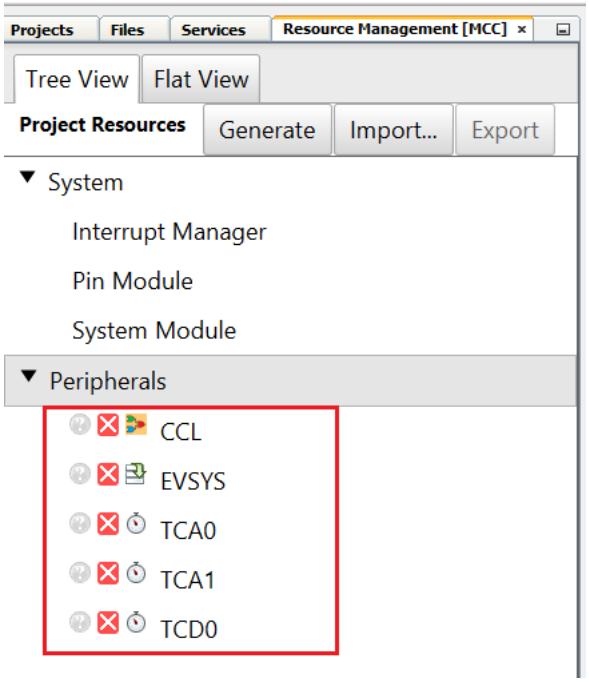
3. Add the peripherals and configure them:
   3.1. From the Device Resources window, add **CCL**, **EVSYS**, **TCA0**, **TCA1**, and **TCD0**. Select the peripheral to be added and click on the **'+'** icon.
   Note: The image shows how to only add the CCL peripheral. Do the same operation for all the peripherals mentioned above.

Figure 2-14. Add Peripherals



The added peripherals can be found in *Project Resources>Peripherals*.

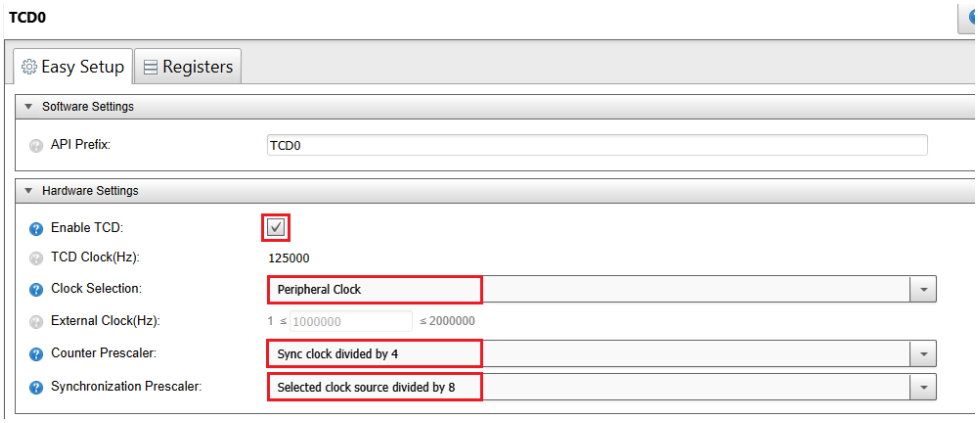
Figure 2-15. Added Peripherals



3.2. Perform the following configuration for each peripheral:

- **TCD0 Configuration:**
  - *Easy Setup>Hardware Settings*:

Figure 2-16. TCD0-Easy Setup



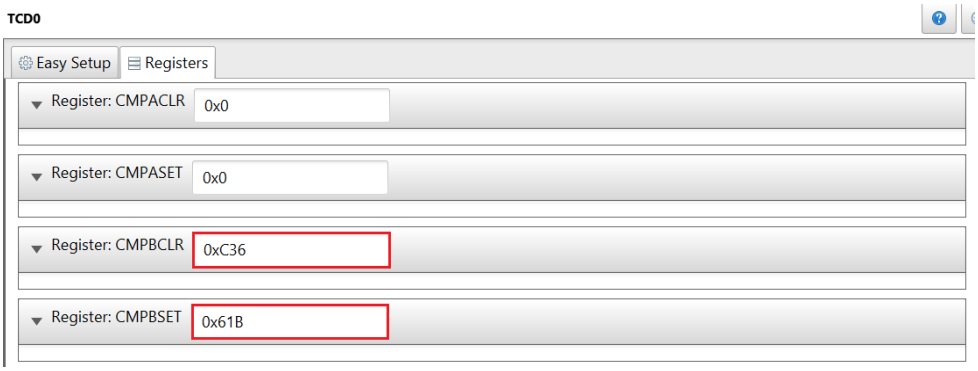
- Enable TCD check box: checked
- Clock Selection: Peripheral Clock
- Counter Prescaler: Sync clock divided by 4
- Synchronization Prescaler: Selected Clock Source divided by 8

After the configurations made above, the TCD0 clock will have a frequency of 125 kHz.

Note: The application is using the default clock configuration (Internal High Frequency Oscillator at 4 MHz).

– Registers tab:

Figure 2-17. TDC0-Registers-CMPBCLR and CMPBSET



- Compare B Clear: 0xC36
- Compare B Set: 0x61B

The TCD0 will be configured to generate an event every time the counter reaches the value from CMPBSET register. The time difference between two consecutive events is TCD0 clock/CMPBCLR.

Because the events must occur with a frequency of 40 Hz, results that CMPBCLR = TCD0 clock/40 Hz = 0xC36.

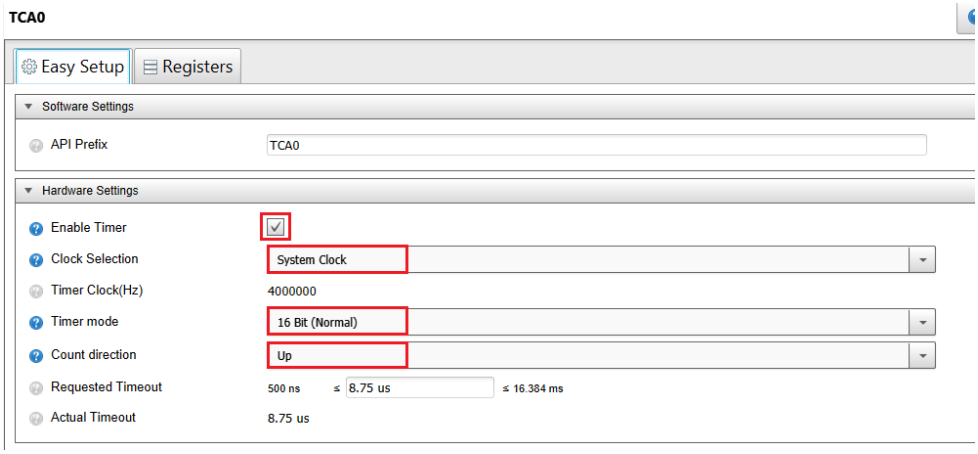
Figure 2-18. TDC0-Registers-CMPB and CMPBEN

- Compare B Value: enabled
- Compare B Enable: enabled

After the configurations made above TCD will generate an event every 25 ms. This event will be later connected on this demo with the LUT0, TCA0 and TCA1.

- **TCA0 Configuration**:
  - *Easy Setup>Hardware Settings*:

Figure 2-19. TCA0-Easy Setup-Hardware Settings



- Enable Timer check box: checked
- Clock Selection: System Clock
- Timer mode: 16 Bit (Normal)
- Count direction: Up

  – Registers tab:

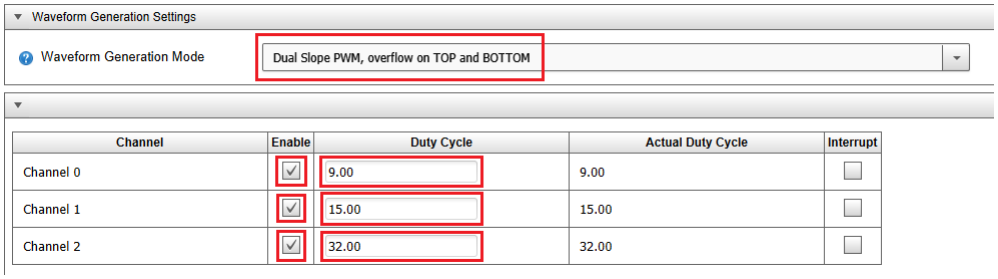
Figure 2-20. TCA0-Registers-PER

- Period: 0x22

In decimal 0x22=34, which is the number of dots from a SOS message period. In this way the TCA0 output will have a resolution of 1 dot.

  – *Easy Setup>Waveform Generation Settings*:

Figure 2-21. TCA0-Easy Setup-Waveform Generation Settings



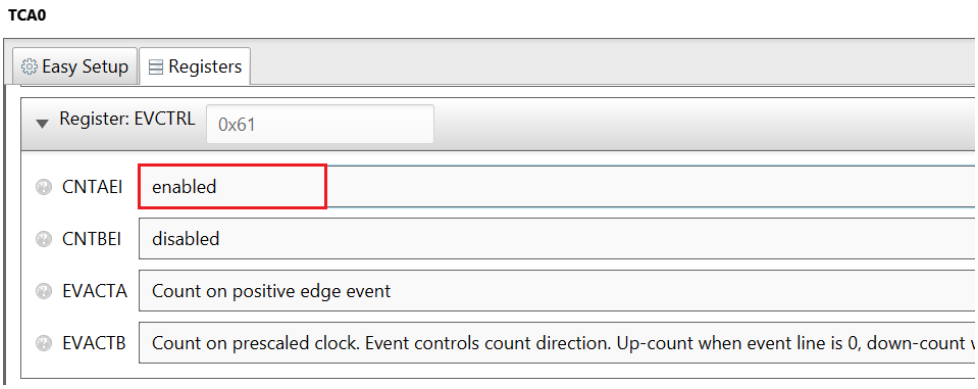
- Waveform Generation mode: Dual Slope PWM, overflow on TOP and BOTTOM
- Enable check box right next to Channel 0: checked
- Duty Cycle right next to Channel 0: 9.00
- Enable check box right next to Channel 1: checked
- Duty Cycle right next to Channel 1: 15.00
- Enable check box right next to Channel 2: checked
- Duty Cycle right next to Channel 2: 32.00

– Registers tab:

Figure 2-22. TCA0-Registers-CTRLC

- Compare Output Value 0: enabled
- Compare Output Value 1: enabled
- Compare Output Value 1: enabled

Figure 2-23. TCA0-Registers-EVCTRL



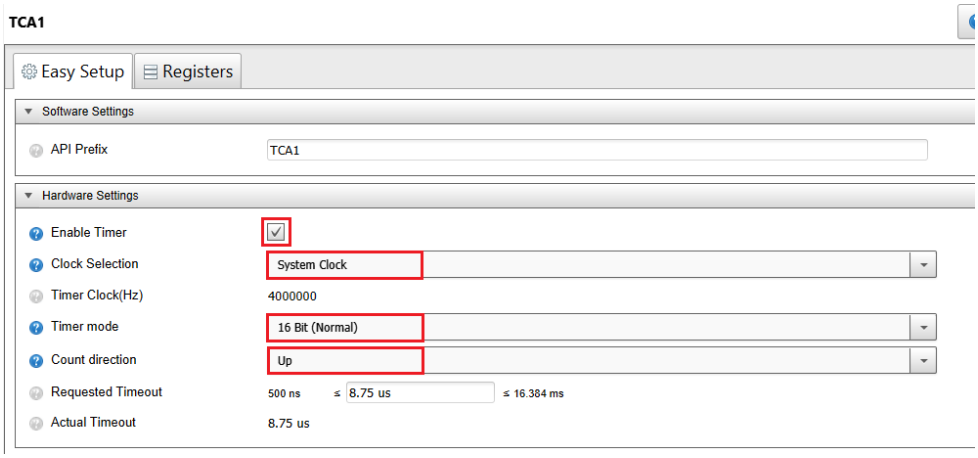
- Enable Counter Event Input A: enabled

TCA0 will count every time an event from TCD0 occurs.

- **TCA1 Configuration**:

– *Easy Setup>Hardware Settings*:

Figure 2-24. TCA1-Easy Setup-Hardware Settings



- Enable Timer check box: checked
- Clock Selection: System Clock
- Timer mode: 16 Bit (Normal)
- Count direction: Up

– Registers tab:

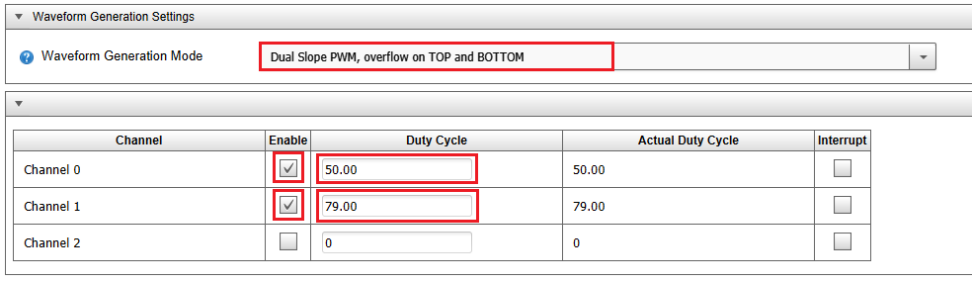
Figure 2-25. TCA1-Registers-PER

- Period: 0x22

In decimal 0x22=34, which is the number of dots from a SOS message period. In this way the TCA1 output will have a resolution of 1 dot.

– *Easy Setup>Waveform Generation Settings*:

Figure 2-26. TCA1-Easy Setup-Waveform Generation Settings



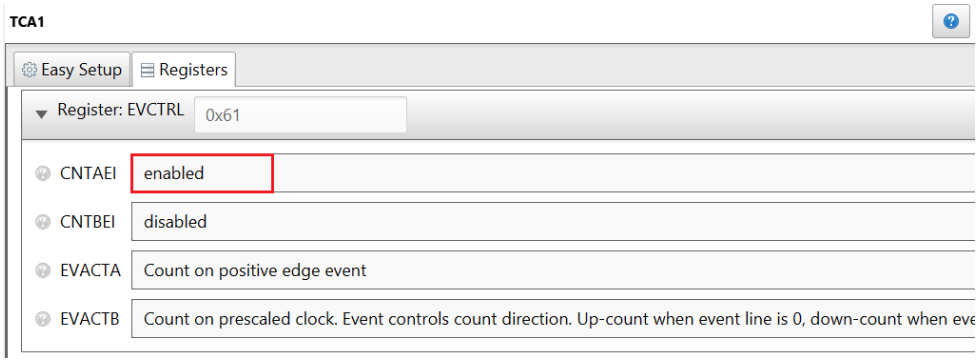
- Waveform Generation mode: Dual Slope PWM, overflow on TOP and BOTTOM
- Enable check box right next to Channel 0: checked
- Duty Cycle right next to Channel 0: 50.00
- Enable check box right next to Channel 1: checked
- Duty Cycle right next to Channel 1: 79.00

– Registers tab:

Figure 2-27. TCA1-Registers-CTRLC

- Compare Output Value 0: enabled
- Compare Output Value 1: enabled

Figure 2-28. TCA1-Registers-EVCTRL

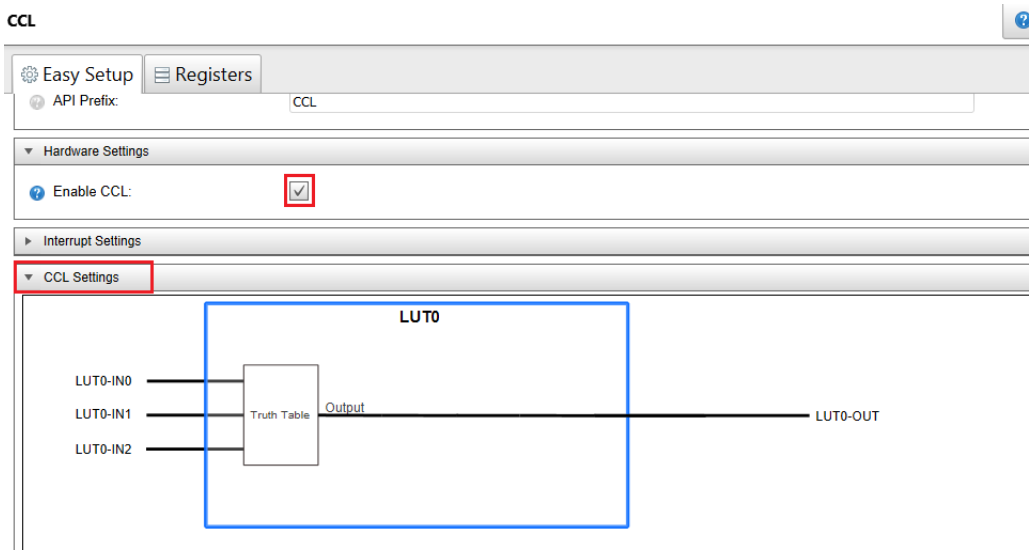


- Enable Counter Event Input A: enabled

TCA1 will count every time an event from TCD0 occurs.

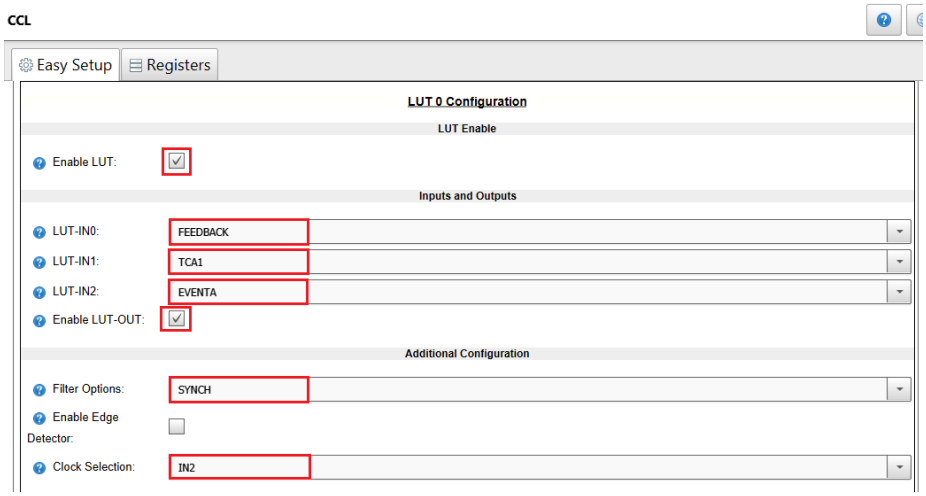
- **CCL Configuration**:
  The different instances of LUT can be selected from **Easy Setup>CCL Settings**. Click on the instance to be configured and make sure Enable CCL check box is checked.

  Figure 2-29. LUT Selection



  – *Easy Setup>CCL Settings*:
    - **LUT0 Configuration**:

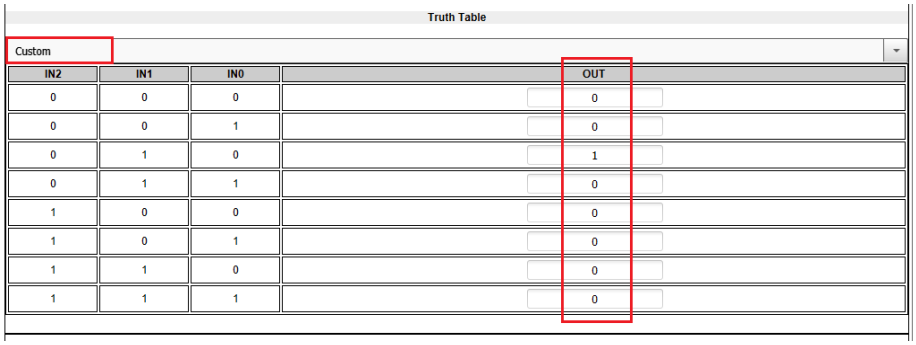
Figure 2-30. LUT0 Configuration



- Enable LUT check box: checked
- LUT-IN0: FEEDBACK
- LUT-IN1: TCA1
- LUT-IN2: EVENTA
- Enable LUT-OUT check box: checked
- Filter Options: SYNCH
- Clock Selection: IN2

The Filter from LUT0 is used in SYNC mode with feedback loop in order to obtain the signal which contains the pattern of letter ‘S’. It divides the frequency of events triggered by TCD0 with a factor of 4.

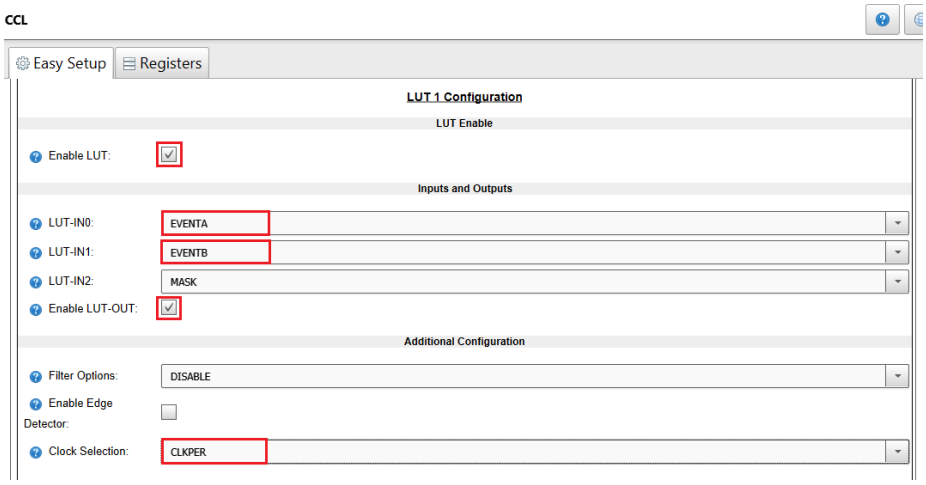
Figure 2-31. LUT0 Truth Table



- Truth Table: Custom
- OUT: (from top to bottom) 00100000

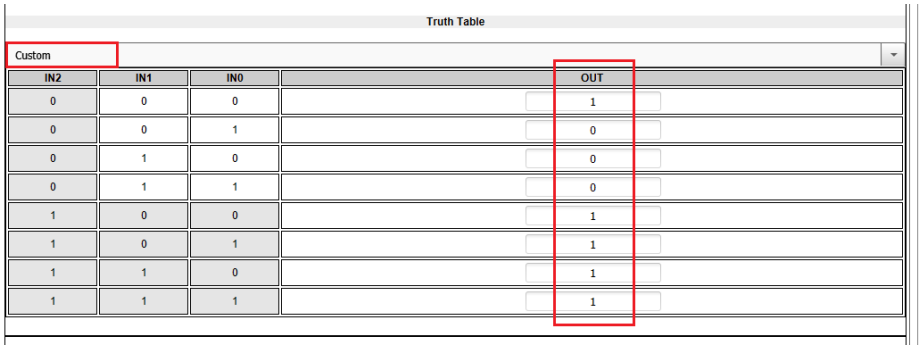
- **LUT1 Configuration**:

Figure 2-32. LUT1 Configuration



  - Enable LUT check box: checked
  - LUT-IN0: EVENTA
  - LUT-IN1: EVENTB
  - LUT-IN2: MASK
  - Enable LUT-OUT check box: checked
  - Filter Options: DISABLE
  - Clock Selection: CLKPER

Figure 2-33. LUT1 Truth Table



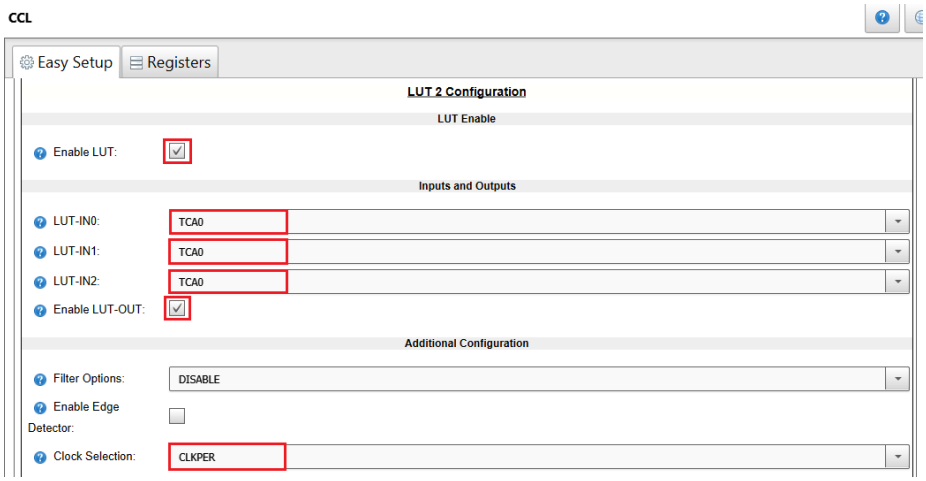
IN2	IN1	IN0	OUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

  - Truth Table: Custom
  - OUT: (from top to bottom) 10001111

The value of OUT bits is negated because the output of LUT1 will drive the CNANO board LED, which works on invert logic (logic ’0’ - ON, logic ‘1’ - OFF).

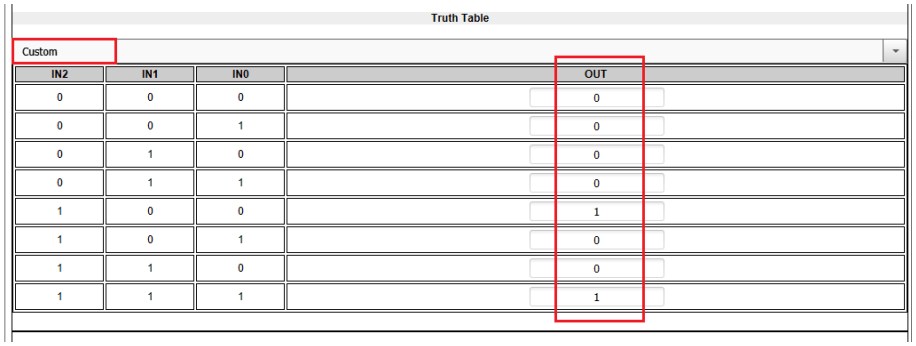
- **LUT2 Configuration**:

Figure 2-34. LUT2 Configuration



  - Enable LUT check box: checked
  - LUT-IN0: TCA0
  - LUT-IN1: TCA0
  - LUT-IN2: TCA0
  - Enable LUT-OUT check box: checked
  - Filter Options: DISABLE
  - Clock Selection: CLKPER

Figure 2-35. LUT2 Truth Table

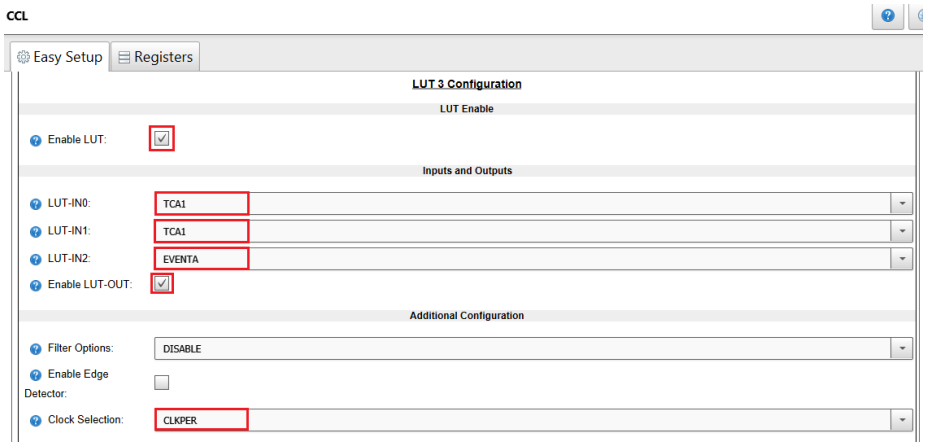


IN2	IN1	IN0	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

  - Truth Table: Custom
  - OUT: (from top to bottom) 00001001

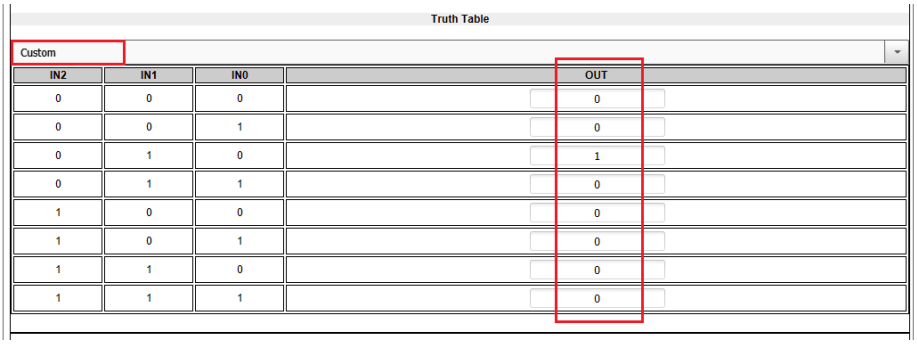
- **LUT3 Configuration**:

Figure 2-36. LUT3 Configuration



  - Enable LUT check box: checked
  - LUT-IN0: TCA1
  - LUT-IN1: TCA1
  - LUT-IN2: EVENTA
  - Enable LUT-OUT check box: checked
  - Filter Options: DISABLE
  - Clock Selection: CLKPER

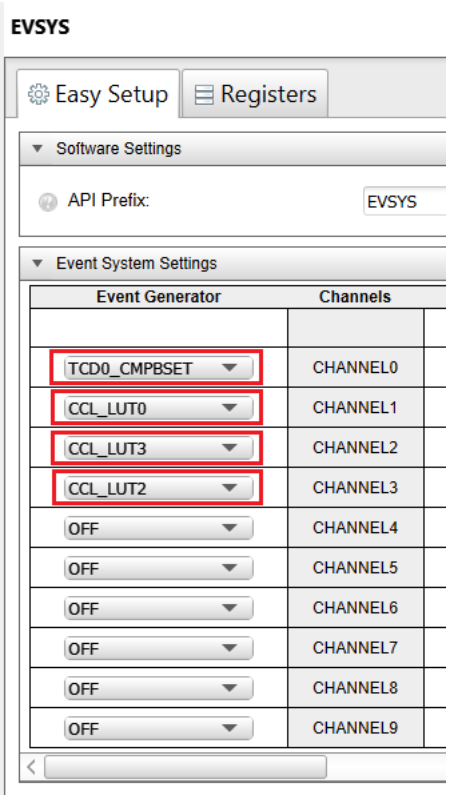
Figure 2-37. LUT3 Truth Table



  - Truth Table: Custom
  - OUT: (from top to bottom) 00100000

- **EVSYS Configuration**:
  - Event Generators:
    - CHANNEL0: TCD0_CMPBSET
    - CHANNEL1: CCL_LUT0
    - CHANNEL2: CCL_LUT3
    - CHANNEL3: CCL_LUT2

Figure 2-38. EVSYS Event Generators



– Event Users
  - CHANNEL0: CCLLUT0A, TCA0CNTA, TCA1CNTA
  - CHANNEL1: CCLLUT3A
  - CHANNEL2: CCLLUT1A
  - CHANNEL3: CCLLUT1B

Figure 2-39. EVSYS Event Users (1)

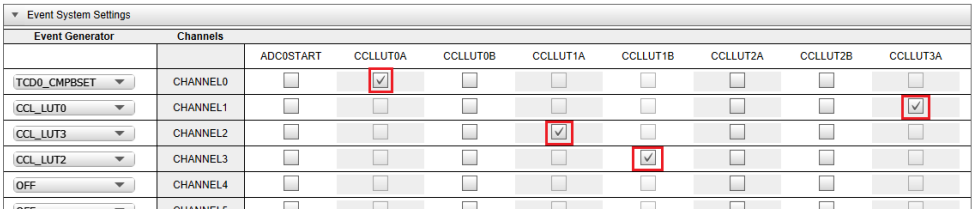
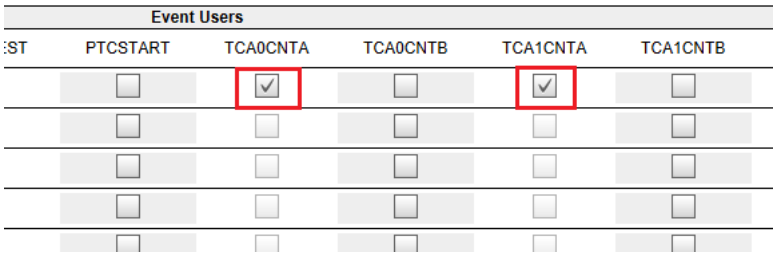


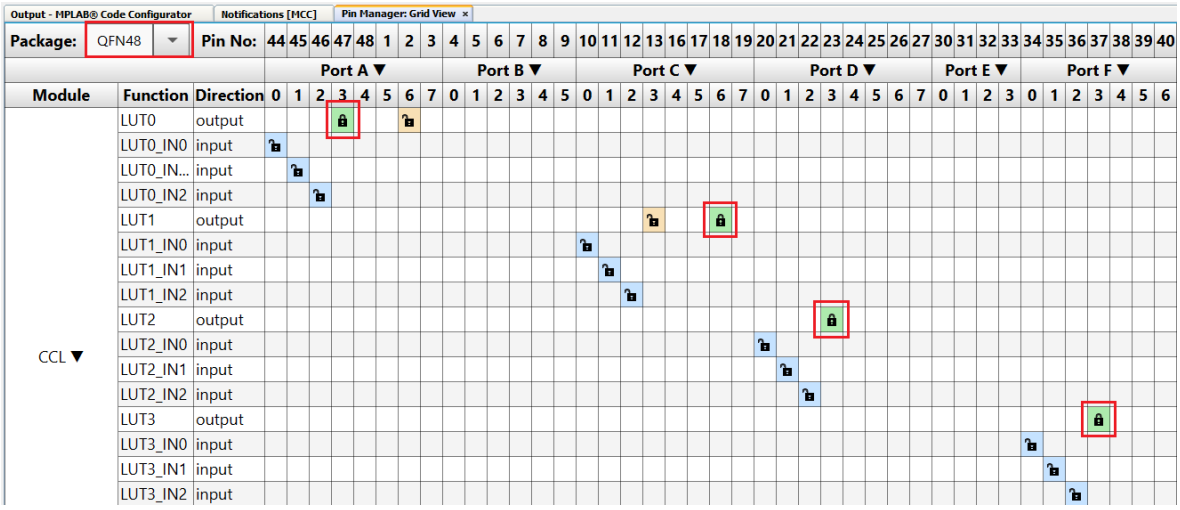
Figure 2-40. EVSYS Event Users (2)



4. Go to *Pin Manager>Grid View* and perform the following configurations:
   – Set Port A pin 3 (RA3) as output for LUT0
   – Set Port C pin 6 (RC6) as output for LUT1
   – Set Port D pin 3 (RD3) as output for LUT2

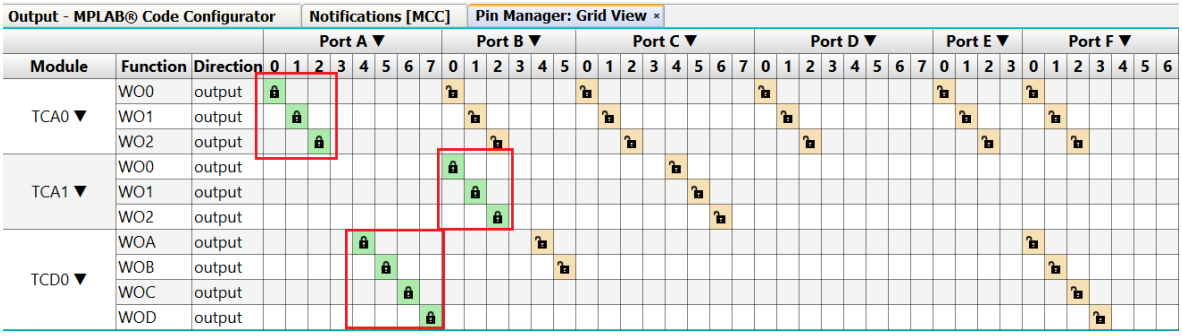
– Set Port F pin 3 (RF3) as output for LUT3

Figure 2-41. Pin Module CLC



– Set Port A pins 0-2 (RA0-RA2) as output for TCA0
– Set Port B pins 0-2 (RB0-RB2) as output for TCA1
– Set Port A pins 4-7 (RA4-RA7) as output for TCD0

Figure 2-42. Pin Module Timers



Note: The SOS signal will be available on the RC6. The rest of the signals have a correspondent output pin only for debugging.

The output waveforms can be seen in the pictures below. There were captured with a logic analyzer.

Figure 2-43. TCA1, LUT0, and LUT3 Output

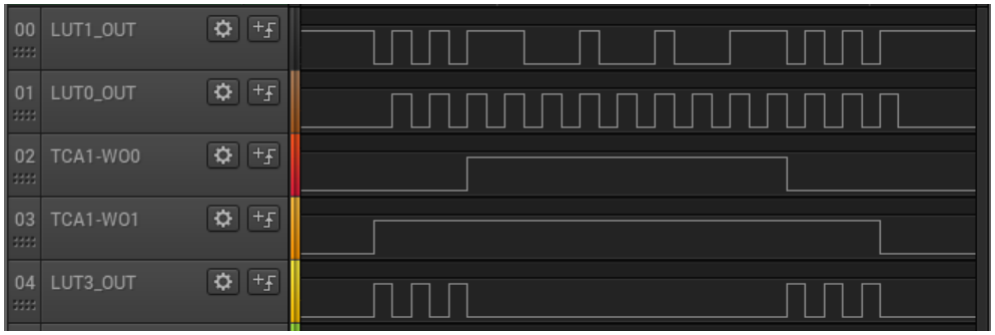


Figure 2-44. TCA0 and LUT2 Output

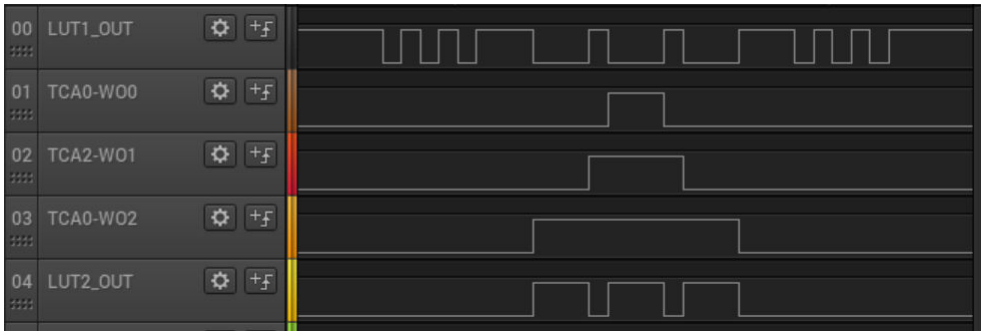
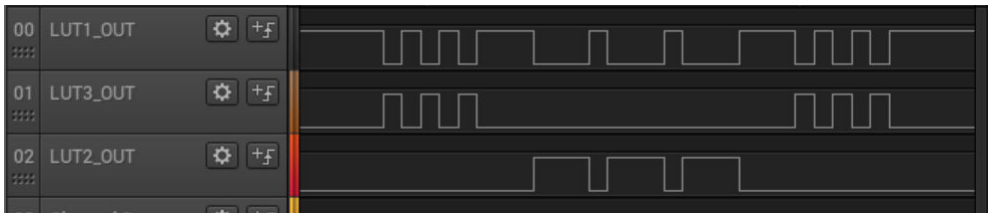


Figure 2-45. SOS Message Waveform



View Code Example on GitHub
Click to browse repository

3. Revision History

Revision	Date	Description
A	08/2020	Initial document release

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