MC92604 Dual GEt Design Verification Board User's Guide

MC92604DVBUG
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freescale™
semiconductor

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Chapter 1
General Information

1.1 Introduction

This user's guide describes the MC92604DVB design verification board for the MC92604 integrated circuit. The design verification board (DVB) facilitates the full evaluation of the MC92604 Dual Gigabit Ethernet transceiver (GEt). It should be read in conjunction with the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*. This design verification board is intended for evaluation and testing purposes only. Freescale does not guarantee its performance in a production environment.

This board was designed to be used with laboratory equipment (pattern generators, data analyzers, BERT, scopes, etc.) or connected to other evaluation boards. Access to the MC92604 device (verification chip) is through connectors to each pin, to allow complete in-depth 'design verification' testing of the chip design. This allows the user to check any or all features/functions of the MC92604 GEt device.

The two parallel data input ports and all configuration/control signal pins, are accessed through common 2×10, 0.100" male connectors (headers). The parallel data output ports are accessed through 2×20, 0.100" connectors. Device JTAG and MDIO port signals are also accessed with separate connectors.

The MC92604 high-speed serial receivers and transmitters are accessed via SMA coaxial connectors for signal integrity measurements. Gigabit Ethernet fiber media evaluations can be made with the provided small form-factor pluggable (SFP) socket on the DVB, and an MSA (multi-source agreement) compliant transceiver. To use this SFP socket, four short coax cables are required to connect the SFP socket to the device's transmitter and receiver SMA connectors.

A single 5.0-V power source is required for the DVB operation. All necessary voltages are generated by regulators onboard. The reference clock for the MC92604 chip may be provided using either an external clock or the onboard crystal oscillator. Clock drivers on the DVB provide additional clock signals for triggering analyzer instrumentation and scopes.

1.2 Design Verification Board Features

The functional, physical, and performance features of the MC92604DVB are as follows:

- A single external 5.0-V to onboard regulators supply power to all onboard circuitry.
- Reference clock source is a 250-MHz crystal oscillator or an external clock source.
- IEEE Std 802.3-2002® compliant GMII or TBI interfaces accessible through standard 0.100", 2 row connectors for data generators and analyzers.
- The full-duplex differential data links accessible through SMA connectors.
- Two pairs of 50-Ω test traces with SMA connections facilitate TDR measurements of the characteristic impedance of representative board traces.
- Connectors provided for JTAG and MDIO ports
- SFP socket provided for MSA-compliant fiber modules
- IEEE Std 1394b (bilingual) socket provided for standard cable links

1.3 Specifications

The MC92604DVB design verification board specifications are provided in Table 1-1.

Table 1-1. MC92604DVB Design Verification Board Specifications

Characteristics		Specifications
Board revision		A
External power supply		+5 V DC ± 0.5 V DC < 1.5 A typical
Support circuit regulator		3.3 V ± 0.3 V DC
MC92604 core and link I/O regulator		1.8 V ± 0.15 V DC
Interface I/O (V_{DDQ}) regulator		2.5 V ± 0.2 or 3.3 V ± 0.3 V DC
MC92604 package		196 MAPBGA
Operating temperature		0°–30°C
Material		FR-4
Dimensions	Height	11.2", 287 mm
	Width	9.35", 238 mm
	Thickness	0.062", 1.6 mm
Conducting layers		Four ground planes, one split power plane, three signal routing layers, top and bottom component layers with some additional signal routing.

1.4 Abbreviation List

Table 1-2 contains abbreviations used in this document.

Table 1-2. Acronyms and Abbreviated Terms

Term	Meaning
'1'	High logic level (nominally 2.5 or 3.3 V)
'0'	Low logic level (nominally 0.0 V)
BIST	Built-in self-test
DVB	Design verification board
I/F	Interface
MDIO	Management data input/output port
MSA	Multi-source agreement
N/C	No connection
PN	Pseudo-noise
PRBS	Pseudo random bit sequence
SFP	Small form-factor pluggable (fiber optics module)
TAP	Test access port
TDR	Time delay reflectometry
UIp-p	Peak-to-peak unit interval

1.5 Related Documentation

Related documentation includes the following:

- *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide* (MC92604RM)
- MC92604DVB schematics
- MC100ES6222 data sheet
- MPC9456 data sheet
- IEEE Std 802.3-2002, Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications

1.6 Block Diagram

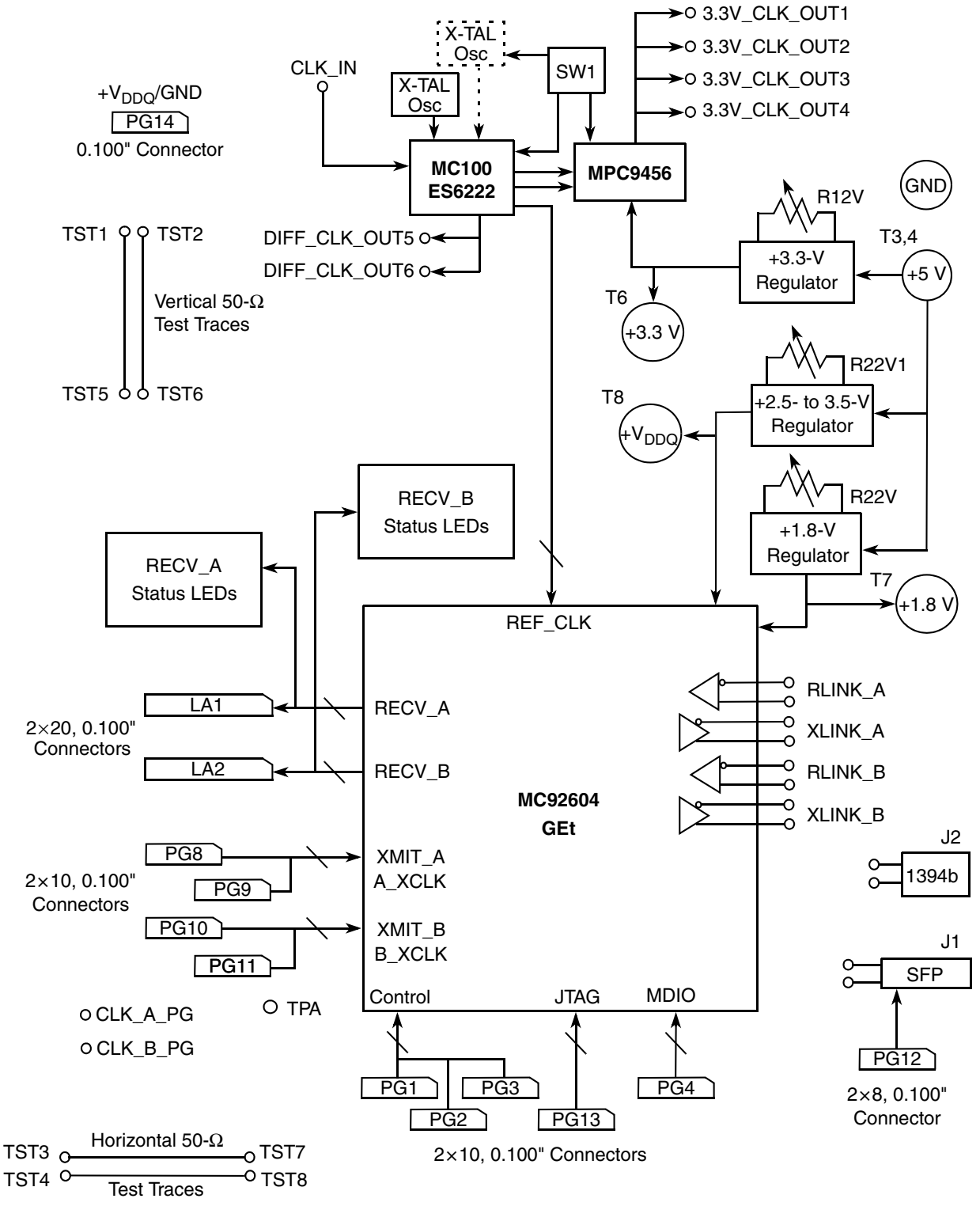


Figure 1-1. MC92604DVB Design Verification Board Block Diagram

1.7 Board Components

Table 1-3 is a list of major components of the MC92604DVB design verification board. A complete parts listing can be found in Appendix B, "Parts List."

Table 1-3. Major Board Components

Component	Description
MC92604ZT	Freescale dual gigabit ethernet transceiver SerDes
2 x 10, 0.100" connectors	PG1–PG4, PG8–PG11, and PG13 provide access to the parallel inputs and control signals.
2 x 20, 0.100" connectors	LA1–LA2 provide access to the parallel outputs.
2 x 8, 0.100" connectors	PG12 and PG14 provide access to the SFP connector and $+V_{DD}$/ground planes, respectively.
SMA connectors	SMA1–SMA8: Serial transmit and receive connections TST1–TST8: Impedance test trace connections CLK_OUT1–CLK_OUT6: Reference clock outputs CLK_IN: External reference clock input CLK_A_PG, CLK_B_PG: Input clock connectors
SPF connector	J2: Provide connections for SFP MSA optical modules
IEEE Std 1394b bilingual connector	J1: Provide serial interface to 'Firewire' type a or b cable
LT1587 voltage regulators	VR33, VR18, and VR1: +3.3 V, +1.8 V, and $+V_{DD}$ voltage regulators
Potentiometers	R12V, R22V, R22V1: Potentiometers for setting +3.3 V, +1.8 V, and $+V_{DD}$ voltage levels
XTAL oscillator	Y1, Y2: Onboard 250-MHz crystal oscillator
MC100ES6222 clock buffer	U2: Divide-by-1 or divide-by-2 clock buffer
MPC9456 clock buffer	U3: +3.3-V LVCMOS clock buffer

1.8 Contact Information

For questions concerning the MC92604 design verification kit or to place an order for a kit, contact your local Freescale field applications engineer.

Chapter 2
Hardware Preparation and Installation

This chapter provides unpacking, hardware preparation, configuration-installation instructions, and description of the interface components for the MC92604DVB.

2.1 Unpacking Instructions

Unpack the board from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of the equipment.

2.2 MC92604DVB Package Contents

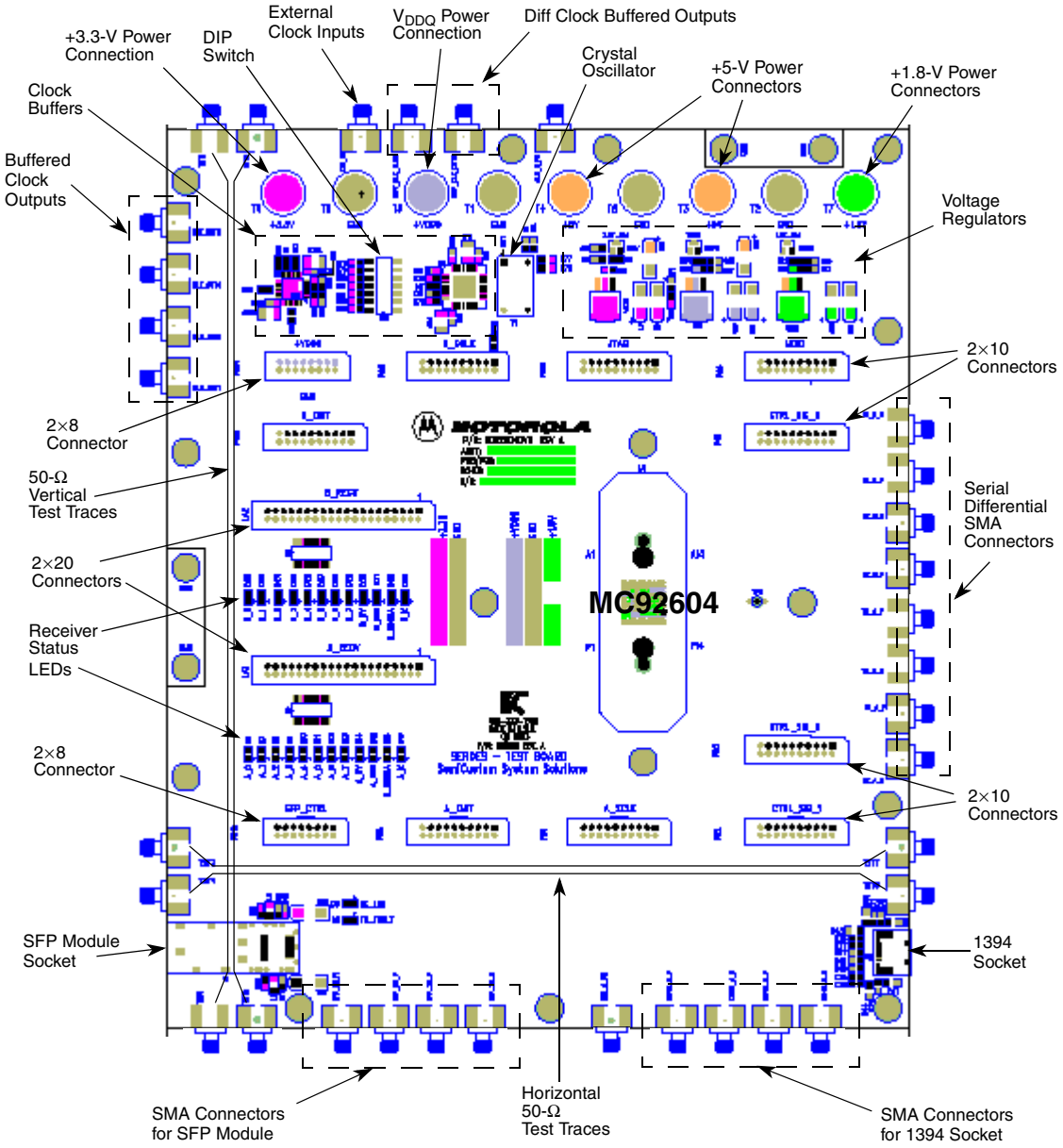
Table 2-1 describes the contents of the MC92604DVB kit.

Table 2-1. MC92604DVB Kit Contents

Qty.	Item
1	MC92604DVB design verification board
1	*MC92604DVBUG Dual GEt Design Verification Board User's Guide*
1	*MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*
1	Complete set of MC92604DVB design verification board schematics
60	0.100" shunts
6	Square pin receptacle patch cords

2.3 Hardware Preparation

Operation of the MC92604DVB requires proper setup of the power supply and voltage regulators as well as the reference clock. Figure 2-1 depicts the location of the major components on the board. The following sections describe the proper setup for the MC92604DVB.



NOTE:
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit, or function of the current product.

Figure 2-1. Top Side Part Location Diagram

2.3.1 Setting the Power Supply and Voltage Regulators

The MC92604DVB requires a single +5.0-V supply. Fully operational, the board will draw a maximum current less than 1.5 amps from the +5.0-V supply. Actual current consumption depends on the user set voltage levels, clock frequencies, use of an SFP module, and the MC92604 operating mode. The board contains two +5.0-V connection posts and two ground connection posts. These duplicate connections simplify using a four-wire supply: supply and ground, force and sense.

2.3.2 Setting the Voltage Regulators

The +5.0-V supply is used to power 3 on-board voltage regulators, VR33, VR18, and VR1. These regulators generate +3.3, +1.8, and +2.5/3.3 V (V_{DDQ}), respectively. The +3.3-V supply provides power to the oscillator, clock buffer chips, LED drivers, and power source for the SFP socket. This supply can be varied over the range +3.3 V ± 0.3 V using the R12V potentiometer.

The +1.8-V supply is used to power the MC92604 core logic, transceivers, and on-chip phase-locked loop (PLL). This regulator can be adjusted over the range +1.8 V ± 0.15 V using R22V.

The V_{DDQ} supply powers the MC92604 control signal, parallel input, and output interface circuitry. This voltage level is determined by the desired logic interface. The supply can be adjusted using the R22V1 potentiometer from a nominal +2.5 to +3.3 V.

The +3.3-V, +1.8-V, and $+V_{DDQ}$ supplies are accessible via connection posts. Note that these regulators should be set to voltage limits within the operating ranges described in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide.* Failure to operate within these ranges could cause damage to the MC92604. Freescale will not guarantee MC92604 operation beyond the ranges specified. The R12V, R22V, and R22V1 potentiometers will be factory set for +3.3, +1.8, and +3.3 V, respectively.

2.4 Reference Clock Source

Through a combination of clock buffers, a reference clock is supplied to the MC92604 and several SMA output connectors. The input reference clock for the MC92604 can be supplied using either an onboard crystal oscillator, or by directly driving an external reference clock into the board's clock buffer circuit via the SMA connector, CLK_IN.

When selecting reference oscillators or external reference frequencies, only those frequencies listed in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, are considered valid. Freescale does not guarantee operation of the MC92604 at frequencies other than those listed in the reference Guide. DIP switch settings select either the onboard oscillator or the external reference, as well as the enable for the clock buffer chips.

The clock circuitry for the MC92604DVB is shown in Figure 2-2.

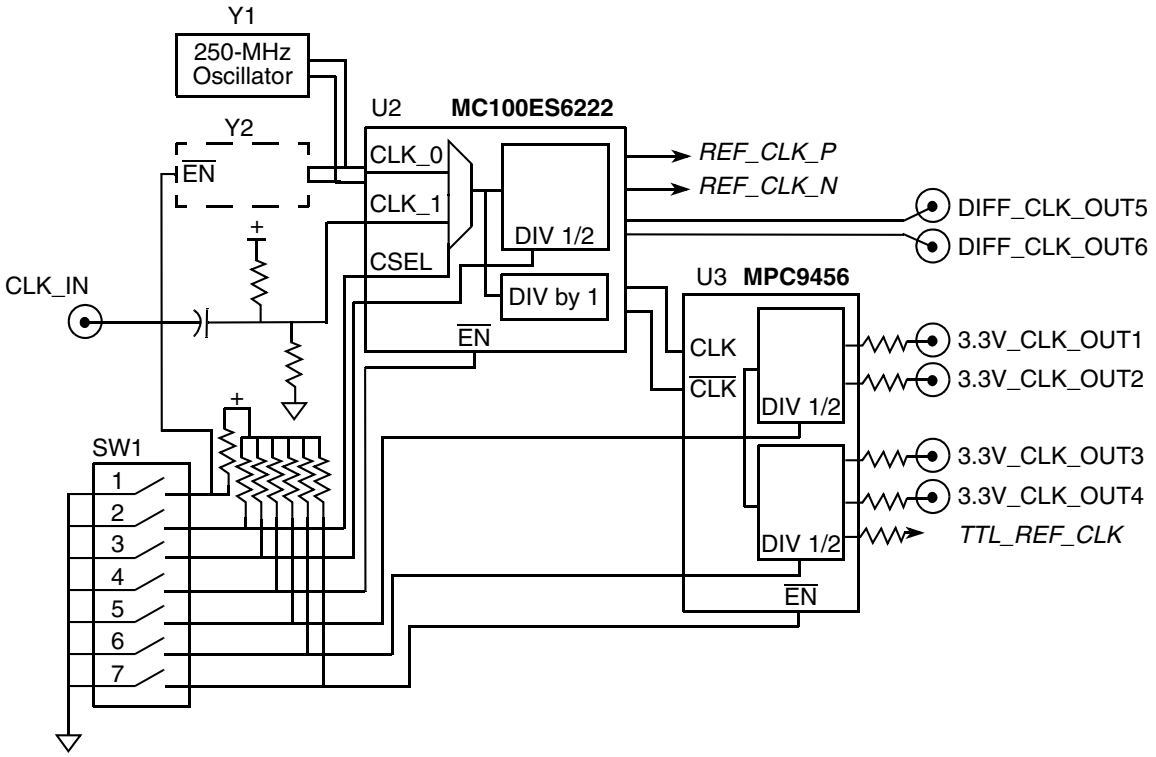


Figure 2-2. DVB Clock Circuitry

2.4.1 Using the Onboard Oscillators

There are two available positions for using onboard oscillators. A standard 14-pin DIP socket is available on the board to allow the user to easily change frequencies by swapping in crystal oscillators with other values. The onboard oscillators must be two times (2×) the desired MC92604 reference clock frequency. The default reference clock frequency oscillator supplied with the board is 250 MHz.

Crystal oscillators used with this board should have +3.3-V complementary PECL outputs capable of driving a line terminated with 50 Ω. Oscillators conforming to these specifications are available in surface mount packages and can be soldered onto the underside of the MC92604DVB at location Y2. This oscillator, Y2, can then be enabled by placing SW1 switch 1 in the ‘on’ position. Both types of crystal oscillators are available from external vendors in a variety of frequencies. The DVB may be shipped with either the Y1 or the Y2 oscillator installed. When using the Y2 oscillator, the Y1 oscillator must be removed from its socket. Once either type of oscillator is installed, SW1 switch 2 must be placed in the ‘on’ position to select the onboard oscillator.

2.4.2 External Reference Clock Source

The input reference clock can also be supplied by using an external reference clock into the clock buffer circuit on the board via the CLK_IN SMA connector. To supply an external reference clock, switch number 2 on SW1 must be set to the ‘off’ position. The user must then supply a 1.0-Vp-p input clock via the SMA connector. The CLK_IN input is AC coupled on the board and, therefore, does not require any DC biasing of the input signal. This external clock input is also terminated with a 50-Ω impedance.

2.4.3 Supplying a Clock to the MC92604

The input reference clock, from either the onboard oscillator or an external source, is applied to a MC100ES6222 clock buffer. This buffer has an input clock select multiplexer, and a programmable divide-by-one/divide-by-two function. The buffer also contains a master reset ($\overline{\text{Enable}}$). It is recommended that this reset, found on SW1 switch 4, be activated, then deactivated after changing the divide-by-*xx* switch. This will ensure proper frequency generation.

The MC100ES6222 PECL outputs provide the differential reference clock to the MC92604 (REF_CLK_P and REF_CLK_N) and also to an MC9456 TTL fanout buffer. When using the default 250-MHz clock, Y1, switch position 3 must be ‘off’ to do a divide-by-2 to provide the 125 MHz for the MC92604. A differential output pair, DIFF_CLK_OUT5 and DIFF_CLK_OUT6, is also provided for use with external equipment.

2.4.4 3.3V_CLK_OUT*n* SMA Connectors

Four single-ended, 3.3-V level, clock signals are available on SMA connectors to drive other instruments. Between the MC100ES6222 output and the 4 SMAs, is an MPC9456 which performs a differential PECL to single-ended +3.3-V LVTTL/CMOS level shift. These CMOS outputs are series terminated on the board, then connect to the SMA connectors labeled 3.3V_CLK_OUT1, 3.3V_CLK_OUT2, 3.3V_CLK_OUT3, and 3.3V_CLK_OUT4. All of the outputs of the MPC9456 can be disabled by setting the DIP switch SW1, switch 7 ‘off.’

2.4.5 Clock Frequency Selection

To accommodate the fact that the MC92604 can receive data on both edges of the reference clock (DDR), but many pieces of the test equipment are single-edge triggered (SDR), the MC92604DVB clock outputs can be programmed to be either the same as the supplied frequency or half the supplied frequency by setting SW1, switches 3, 5, and 6 to either ‘on’ (divide-by-one) or ‘off’ (divide-by-2). This allows the interface between the board and the bench to be either SDR with a double speed clock, or double data rate (DDR) with a single speed clock.

The SMA outputs 3.3V_CLK_OUT1 and 3.3V_CLK_OUT2 can be programmed by setting SW1, switch 5 and the 3.3V_CLK_OUT3 and 3.3V_CLK_OUT4 outputs can be programmed by setting SW1, switch 6. Table 2-2 lists the switch positions and output frequencies. The input frequency, CLK_IN refers to either the onboard oscillator frequency or the externally applied clock source frequency.

NOTE

Only those frequencies listed in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide* are considered valid. Freescale does not guarantee operation of the MC92604 at frequencies other than those listed in the reference Guide.

Table 2-2. SW1 Settings and Output Frequencies

SW1 Switch	Switch Position	REF_CLK_P, REF_CLK_N, DIFF_CLK_OUT5, DIFF_CLK_OUT6	3.3V_CLK_OUT1, 3.3V_CLK_OUT2	3.3V_CLK_OUT3, 3.3V_CLK_OUT4
3	On	CLK_IN	N/A	N/A
	Off	CLK_IN/2	N/A	N/A
5	On	N/A	CLK_IN	N/A
	Off	N/A	CLK_IN/2	N/A
6	On	N/A	N/A	CLK_IN
	Off	N/A	N/A	CLK_IN/2

Figure 2-3 depicts SW1 settings for using an onboard oscillator with the divide-by-two function set for the MC92604 and 3.3V_CLK_OUT*n* SMA outputs. The 3.3V_CLK_OUT1 and 3.3V_CLK_OUT2 SMA outputs are enabled and set to the divide-by-one function. The 3.3V_CLK_OUT3 and 3.3V_CLK_OUT4 SMA outputs are also enabled and are set to the divide-by-two function.

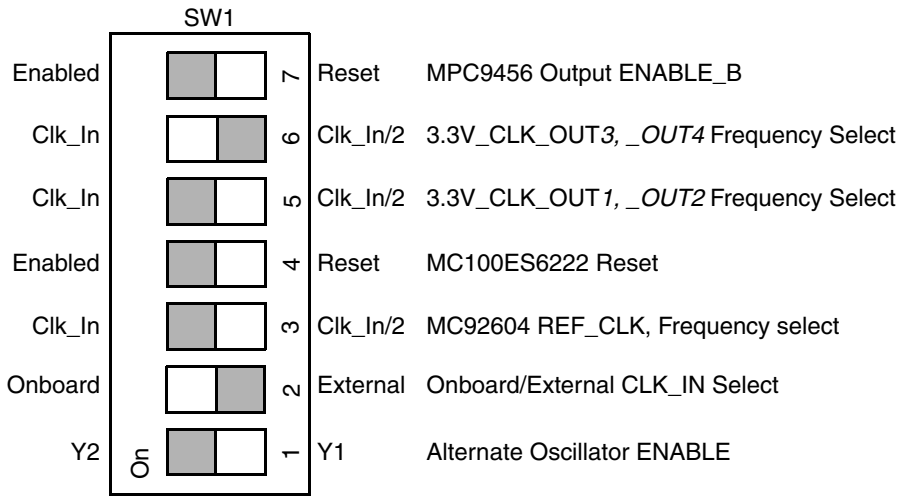


Figure 2-3. Reference Clock Selection Example Switch Settings

2.5 Interface Components

The following sections list the descriptions of the MC92604DVB interface connector components.

2.5.1 Parallel Inputs and Outputs

The MC92604 parallel I/O is supplied by the V_{DDQ} voltage regulator (set for 2.5 or 3.3 V) and has a rail-to-rail signal swing. The MC92604DVB is shipped with V_{DDQ} set at 3.3 V.

2.5.1.1 Parallel Inputs

The parallel inputs, both data and control, are accessible via 2×10, 0.100" connectors. Figure 2-4 depicts the 2×10, 0.100" connector numbering scheme, with pin 1 being labeled on the board. A complete mapping of the MC92604 inputs to the 2×10, 0.100" connectors is listed in Appendix A, "Connector Signals." Note that all even number pins are connected to ground.

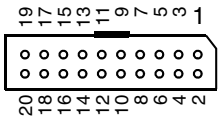


Figure 2-4. 2×10, 0.100" Input Connector Numbering Scheme (Top View)

For a description of the input functionality of the MC92604, refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*.

2.5.1.2 Parallel Outputs

All parallel outputs, both data and status bits, are present at two 2×20, 0.100" connectors. Figure 2-5 depicts the 2×20, 0.100" output connector numbering scheme, with pin 1 labeled on the board. The parallel output signals of the MC92604 are 2.5- or 3.3-V logic compatible depending on the setting of the V_{DDQ} regulator. A complete mapping of the MC92604 outputs to the 2×20, 0.100" connectors is listed in Appendix A, "Connector Signals." Note that all even number pins are connected to ground.

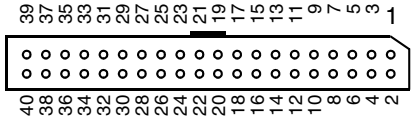


Figure 2-5. 2×20, 0.100" Output Connector Number Scheme (Top View)

For information regarding the MC92604 outputs, refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*.

2.5.2 +V_{DDQ} and Ground (GND) Access Connections

The MC92604DVB also has a 2×8, 0.100" connector, PG14, with dedicated connections to the +V_{DDQ} and ground planes. These are useful for biasing parallel input signals using jumper cables. All of the odd number pins (1, 3, 5, and 7) are connected to the V_{DDQ} plane. All of the even number pins (2, 4, 6, and 8) are connected to the ground (0.0 V) plane.

2.5.3 Serial Inputs and Outputs

All MC92604 high-speed serial differential inputs and outputs are connected to appropriately labeled pairs of SMA connectors through board traces with a characteristic impedance of 50 Ω (100-Ω differential). The output driver requires a 50-Ω parallel termination to mid-rail (+0.9 V nominal for +1.8-V supply). If the termination voltage is not +0.9 V, the signal must be AC coupled. There is no AC coupling (DC blocking) of the serial outputs on the board. If needed, AC coupling must be done in-line before any termination.

During all testing, the serial transmitter outputs should be terminated with 50 Ω. This can be done by connecting the serial transmitter outputs to serial receiver inputs, to any laboratory equipment with 50-Ω input impedance through in-line AC coupling, or by terminating the outputs with 50-Ω SMA terminations.

2.6 Special Application Connections

There are two sets of special connectors provided for application interface evaluation. A Gigabit Ethernet SFP socket is provided with SMA connections to connect to the MC92604DVB serial links and then perform evaluation testing with a fiber optic interface. The user must supply the SFP module. It is not provided with the MC92604DVB. The SFP socket has it's own control interface connector, SFP_CTRL. The mapping of this 2×8, 0.100" connector is listed in Appendix A, "Connector Signals."

Likewise, a IEEE Std 1394B socket (bilingual version) is provided with SMA connections to connect to the MC92604 serial links and perform testing with standard patch cords. (Note that there is a slight impedance mismatch, as the 1394 cables are 110-Ω differential.)

2.7 Special Test Connection

The MC92604DVB also contains an oscilloscope PCB test socket, labeled TPA. When the MC92604 is configured in a PLL factory test mode, this test socket enables special access to the PLL.

NOTE

This test mode is for factory testing purposes only. There are no system applications for this mode and test socket TPA should remain unconnected at all times.

2.8 Test Traces

The MCS92610DVB design verification board has both vertical and horizontal 50-Ω test traces:

- Vertical: TST1–TST5 and TST2–TST6 are 11.82 inches long.
- Horizontal: TST3–TST7 and TST4–TST8 are 9.86 inches long.

These traces can be used to determine the impedance of the board using TDR measurement techniques.

NOTE

These test traces cannot be used as differential pairs. When doing TDR measurements, observe the difference in propagation delays. This is due to one trace being on the surface (top or bottom) layer and the other being on an embedded signal layer.

For the verticle pair, the TST1–TST5 trace is on the bottom surface layer (10) and TST2–TST6 is on an embedded signal layer (6). The horizontal test traces have TST3–TST7 located on embedded signal layer (8) and TST4–TST8 on the top surface layer (1).

Chapter 3
Laboratory Equipment and Quick Setup Evaluation

This chapter begins with a listing of recommended test equipment needed to perform complete evaluations on the MC92604. Chapter 4, "Test Setups," will cover specific setup configurations for this equipment depending on the desired feature under test. Appendix B, "Parts List," offers various suggested data test patterns that may be used with these test setups.

The quick setup evaluation procedures outlined below describe how the MC92604DVB can be used to evaluate the data 'eye diagram' and a simple error rate test using the internal test features of the MC92604 with a minimal amount of test equipment. Only a power supply and sampling oscilloscope are required.

Details of testing in specific systems is left to the user. For more information regarding the MC92604 feature set, refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*.

3.1 Recommended Laboratory Equipment

Evaluation of the MC92604 feature set is possible using the MC92604DVB evaluation kit in conjunction with several pieces of test equipment. The quick setup evaluations and other tests listed in this guide utilize the basic set of test equipment listed in Table 3-1. Equivalent instrumentation may be substituted. Not all pieces of test equipment are necessary for all tests.

Table 3-1. Recommended Test Equipment

Quantity	Equipment
1	MC92604DVB evaluation kit
1	Tektronix TDS 8000 digital sampling oscilloscope
1	Tektronix 80E04 TDR/sampling head (20 GHz)
3	Tektronix 80E03 sampling heads (20 GHz)
1	Hewlett-Packard HP16700 logic analysis system
5	Hewlett-Packard HP16522A pattern generators
2	Hewlett-Packard HP16557D logic analyzers
1	Hewlett-Packard HP6624A system DC power supply

Table 3-2 lists the laboratory accessories.

Table 3-2. Lab Accessories

• SMA male each end coax patch cords, lengths: various
• SMA 3-dB attenuators
• SMA 6-db attenuators
• SMA DC blockers (AC couplers)
• 50-Ω SMA terminations (to ground)
• SMA 50-Ω feed through terminations
• 5/16" torque wrench (fits SMA, 2.9- and 3.5-mm connectors)
• Bias-T networks
• Power splitters
• BNC to SMA adapters
• SMA female to SMA female adapters
• SMA male to SMA male adapters
• SFP MSA optical module (Agilent: HFBR5710L)

In-depth testing of the MC92604 can be performed using a bit error rate tester and a jitter analysis system. Table 3-3 provides a list of test equipment that can be used for these types of tests.

Table 3-3. Jitter Analysis Test Equipment

Quantity	Equipment
1	Agilent 71500C jitter analysis system
1	HP 70820A microwave transition analyzer
1	HP 70004A display
1	HP 3325B synthesizer/function generator
1	HP 83752A synthesized sweeper
1	HP 86130A BitAlyzer (serial bit error rate tester)
1	HP 70874C jitter personality card
2 each	Assorted bandpass filters
1	Rohde and Schwarz SMIQ-04B signal generator
1	Agilent HP 6624A system DC power supply
1	Agilent 11636B power splitter
1	Divide-by-*xx* prescalers

3.2 Quick Setup Data-Eye Diagram

The MC92604DVB design evaluation kit comes equipped to immediately demonstrate two of the MC92604 functions:

- Data-eye signal generation and observation
- Bit error rate checking using internal built-in self-test (BIST) features

3.2.1 Quick Setup Data-Eye Generation and Observation

A transmitted data-eye can be observed at either of the serial outputs of the MC92604 using its integrated, 23rd order, pseudo-noise (PN) pattern generator. The implementation of the 23-bit PN generator uses the following polynomial:

$$f = 1 + x^5 + x^{23}$$

Stimulus from this generator may also be used for further system testing. Refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, for more information.

3.2.1.1 Equipment Setup

Generation and observation of the data-eye produced by the on-chip PN generator requires only the MC92604DVB, a power supply, a high-speed digital sampling scope, and 0.100" shunts and single pin receptacle patch cords.

The MC92604DVB and test equipment should be connected as depicted in Figure 3-1. Configure clock circuits with SW1, as shown in Figure 2-3.

NOTE

All unconnected serial transmitter outputs should be terminated to 50 Ω. This can be done by connecting the serial transmitter outputs to the serial receiver inputs or to 50-Ω SMA terminations through in-line AC coupling (DC blocking).

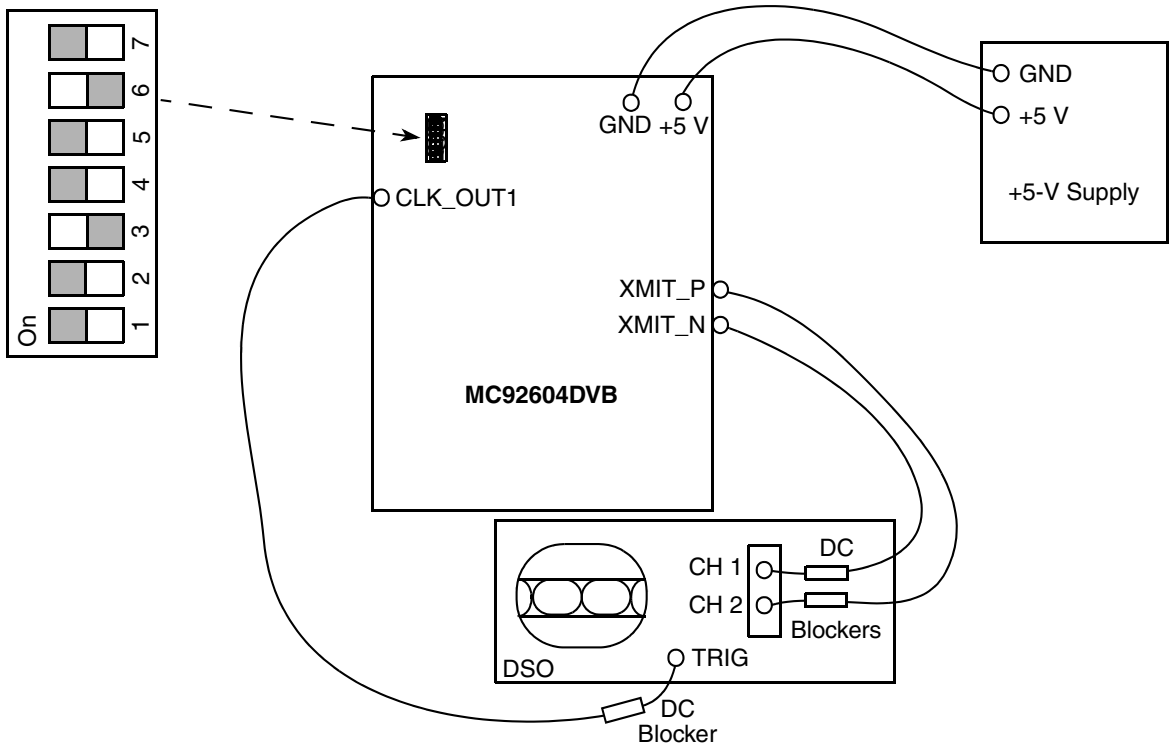


Figure 3-1. Data-Eye Observation Setup

3.2.1.2 Parallel Input Connections

The basic eye diagram will be generated by biasing the parallel inputs according to Table 3-4. Ground connections can be made using the 0.100" shunts. Connections to V_{DDQ} can be made using the square pin receptacle patch cords and jumpering to the odd numbered pins of header PG14. The shunts and patch cords are provided with the MC92604DVB kit. All even number pins on the connector headers are connected to the board's ground plane. All unlisted pins are not connected.

All the signal pins on the five connectors: CNTRL_SIG_0, CNTRL_SIG_1, CNTRL_SIG_2, JTAG, and MDIO have 10K pullup resistors to V_{DDQ}. By making no connection (N/C) to any of these pins, they are effectively biased high or a logic '1.' Using a shorting shunt will bias them low or logic '0.'

The signal pins on channel A and B, _XMIT and _XCLK connectors do not have pullup resistors and, therefore, will need to be biased high with jumper connections to V_{DDQ} or biased low with the shorting shunts.

Using a jumper wire on $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) and connecting to an access pin on connector PG14, will allow the MC92604 to be held in reset mode (connected to ground) or released (connected to V_{DDQ}).

Table 3-4. Parallel Input Biasing for Quick Setup Evaluations

Pin	Signal	Bias Level	Pin	Signal	Bias Level	Pin	Signal	Bias Level
	CTRL_SIG_0			CTRL_SIG_1			CTRL_SIG_2	
1	REPE	GND	1	LBOE	GND	1	BSYNC	N/C
3	RCCE	N/C	3	USE_DIFF_CLK	N/C	3	DROP_SYNC	GND
5	RECV_CLK_CENT	N/C	5	MEDIA	GND	5	TST_1	GND
7	HSE	GND	7	TBIE	GND	7	TST_0	N/C
9	ADIE	GND	9	COMPAT	GND	9	WSYNC1	GND
11	$\overline{\text{RESET}}$	Jumper to GND	11	JPAK	GND	11	WSYNC0	GND
13	DDR	GND	13	RECV_REF_A	GND	13	ENABLE_RED	GND
15	STNDBY	GND	15	XMIT_REF_A	GND	15	BROADCAST	GND
17	XCVR_RSEL	GND	17	ENABLE_AN	GND	17	XCVR_RSEC	GND
19	GND	N/C	19	GND	N/C	19	GND	N/C
	A_XMIT			A_XCLK			JTAG	
1	XMIT_A_0	GND	1	GTX_CLK_0	N/C	1	—	N/C
3	XMIT_A_1	GND	3	—	N/C	3	—	N/C
5	XMIT_A_2	GND	5	XCVR_A_DISABLE	GND	5	—	N/C
7	XMIT_A_3	GND	7	—	N/C	7	—	N/C
9	XMIT_A_4	GND	9	XMIT_A_CLK	N/C	9	TDI	N/C
11	XMIT_A_5	GND	11	XMIT_A_K	GND	11	TCK	N/C
13	XMIT_A_6	GND	13	XCVR_A_LBE	GND	13	TMS	N/C
15	XMIT_A_7	GND	15	XMIT_A_ENABLE (bit 8)	GND	15	$\overline{\text{TRST}}$	GND
17	—	N/C	17	XMIT_A_ERR (bit 9)	GND	17	—	N/C
19	GND	N/C	19	GND	N/C	19	GND	N/C
	B_XMIT			B_XCLK			MDIO	
1	XMIT_B_0	GND	1	GTX_CLK_1	N/C	1	MD_CLK	GND
3	XMIT_B_1	GND	3	—	N/C	3	MD_ENABLE	GND
5	XMIT_B_2	GND	5	XCVR_B_DISABLE	GND	5	MD_DATA	N/C
7	XMIT_B_3	GND	7	—	N/C	7	—	
9	XMIT_B_4	GND	9	XMIT_B_CLK	N/C	9	—	
11	XMIT_B_5	GND	11	XMIT_B_K	GND	11	MD_ADR_1	GND
13	XMIT_B_6	GND	13	XCVR_B_LBE	GND	13	MD_ADR_2	GND
15	XMIT_B_7	GND	15	XMIT_B_ENABLE (bit 8)	GND	15	MD_ADR_3	GND
17	—	N/C	17	XMIT_B_ERR (bit 9)	GND	17	MD_ADR_4	GND
19	GND	N/C	19	GND	N/C	19	GND	N/C

Table 3-4. Parallel Input Biasing for Quick Setup Evaluations (continued)

Pin	Signal	Bias Level	Pin	Signal	Bias Level	Pin	Signal	Bias Level
	SFP_CTRL							
1	—	N/C						
3	—	N/C						
5	—	N/C						
7	MOD_DEF_0	N/C						
9	MOD_DEF_1	GND						
11	MOD_DEF_2	GND						
13	RATE_SELECT	N/C						
15	TX_DISABLE	GND						

3.2.1.3 Basic Eye Observation—Test Procedure

1. Connect the MC92604DVB and test equipment as described in Figure 3-1 and Table 3-4. This will place the MC92604 in PN generation mode with the MC92604 in reset.

Steps 2 and 3 may be skipped if previously performed when setting up the DVB.

2. Apply +5.0 V to the evaluation board. Verify voltage levels of +3.3 V, +1.8 V, and +V_{DDQ} (3.3 V) regulators at connectors T6, T7, and T8, respectively. If necessary, adjust R12V, R22V, and R22V1 to obtain desired voltage levels.
3. Verify that the reference clock frequency at CLK_OUT1 is 125 MHz (period = 8.0 ns).
4. Observe XMIT_*x*_P or XMIT_*x*_N output. Since the chip is in reset, the transmitter should show a constant output level at ground.
5. Connect the $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a V_{DDQ} access connection on connector PG14. This releases the $\overline{\text{RESET}}$ signal.
6. Observe XMIT_*x*_P or XMIT_*x*_N. The transmitter should now be outputting random data. Setting the digital sampling oscilloscope to infinite persistence mode will display a data-eye. An example of a data-eye is shown in Figure 3-2.

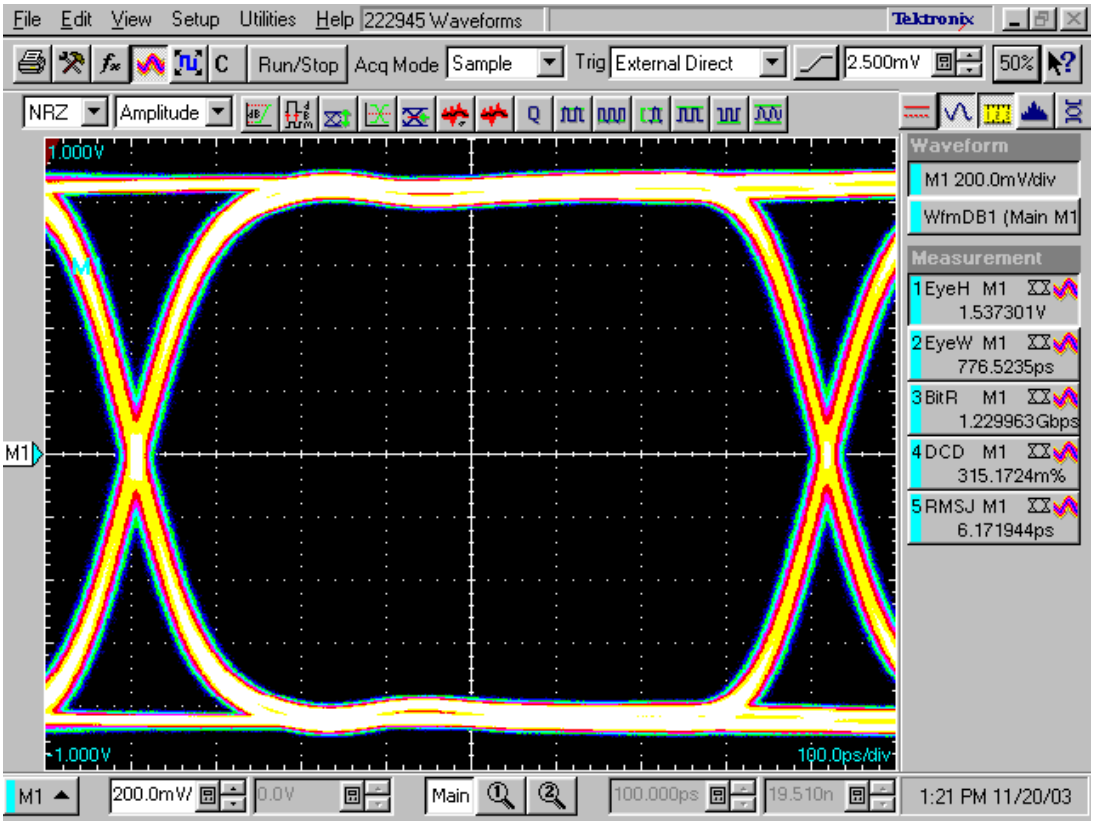


Figure 3-2. MC92604 Data-Eye Using Recommended Test Setup

3.2.2 Quick Setup Bit Error Rate Checking

In addition to having an integrated PN generator, the MC92604 also has a bit error rate checker (BERC). An integrated 23rd order signature analyzer, that is synchronized to the incoming PN stream is used to count code group mismatch errors relative to the internal PN reference pattern. The following test procedure will describe how to use this BIST feature. For more information concerning the MC92604 BIST, refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*.

3.2.2.1 Equipment Setup

Connect the MC92604DVB as shown in Figure 3-3, connecting the transmitter outputs of the link under test (XLINK_*x*_P/N) to the receiver under test (RLINK_*x*_P/N).

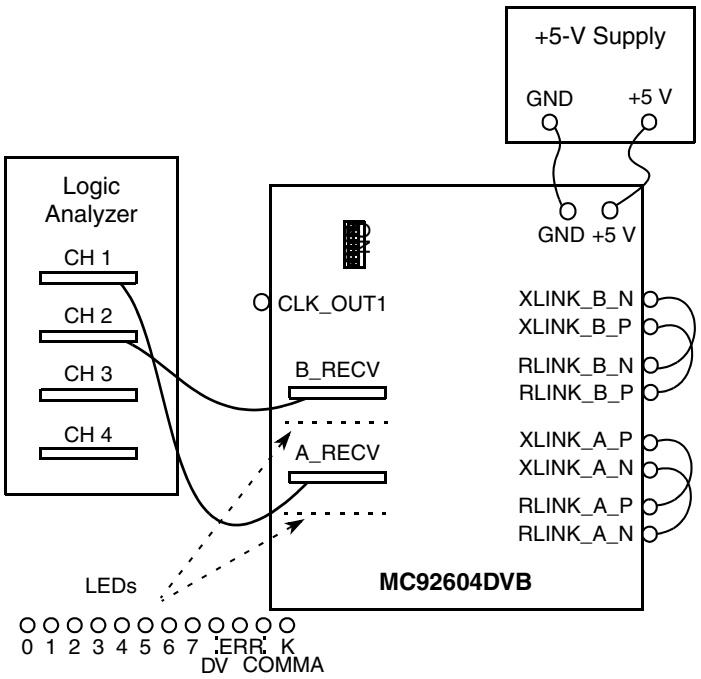


Figure 3-3. Bit Error Rate Check Test Setup

3.2.2.2 Parallel I/O Connections

The bias connections for the parallel inputs to perform the quick setup BERC test are the same as those for the quick setup eye diagram and shown in Table 3-4.

The parallel outputs are connected to a data analysis system. For a simple quick test, the logic analyzer is not required, since the errors are reported and may be observed on the channel status LEDs.

3.2.2.3 Quick Setup BERC Test Procedure

1. Connect the MC92604DVB and test equipment as described in Section 3.2.2.1, "Equipment Setup." This will place the MC92604 in PN generation mode with the MC92604 in reset, and set the receivers to BERC mode using the recovered clock.

Step 2 and 3 may be skipped if previously performed when setting up the DVB.

2. Apply +5.0 V to the evaluation board. Verify voltage levels of +3.3 V, +1.8 V, and +V_{DDQ} (3.3 V) regulators at connectors T6, T7, and T8, respectively. If necessary, adjust R12V, R22V, and R22V1 to obtain desired voltage levels.
3. Verify that the reference clock frequency at CLK_OUT1 is 125 MHz (period = 8.0 ns).
4. Connect the $\overline{\text{RESET}}$ (connector CTRL_SIG_0, pin 11) to a V_{DDQ} access connection on connector PG14. This releases the $\overline{\text{RESET}}$ signal.
5. Observe the parallel outputs on the data analyzer and the status LEDs. As described in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, the MC92604 will start and lock its PLL, initialize the receivers, perform byte alignment, and reset its bit error counter.
6. When the receivers are locked and BIST is running, the recovered clock is observable on RECV_*x*_RCLK. See Figure 3-4 for an example of a receiver startup and error detection sequence.
7. Once the receiver has initially locked all receiver data bits, RECV_*x*_[7:0], are set to zero (logic low). Should an error occur, RECV_*x*_[7:0] will increment by one and RECV_*x*_ERR will flag the error during that byte time. The value of RECV_*x*_[7:0] remains constant until another error is detected or the system is reset. If the receiver counter fills with errors, all bits of RECV_*x*_[7:0] stay a logic high (11111111) until the receiver is reset. Refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, for more detail.

Table 3-5. BIST Error Codes

RECV_*x*_DV	RECV_*x*_ERR	RECV_*x*_COMMA	Status Description
Low	Low	Don't care	Not byte/word sync: The receiver is in startup or has lost byte alignment and is searching for alignment.
High	Low	Low	BIST running, no PN mismatch this code group.
High	Low	High	BIST running, this code group is a *COMMA* code group.
Low	High	Don't care	Receiver byte/word synchronized, PN analyzer is not locked.
High	High	Don't care	BIST running, PN mismatch error this code group.

The error count and status may be observed on the channel A and B LEDs. Simple bit error rate may be calculated. For example: if the error count on the LEDs was 3 and the test had been running for 53 minutes, the BER would be [3 errors divided by (53 minutes×60 seconds per minute×1.25×10^{9} bits per second)] or 2.515^{-13}.

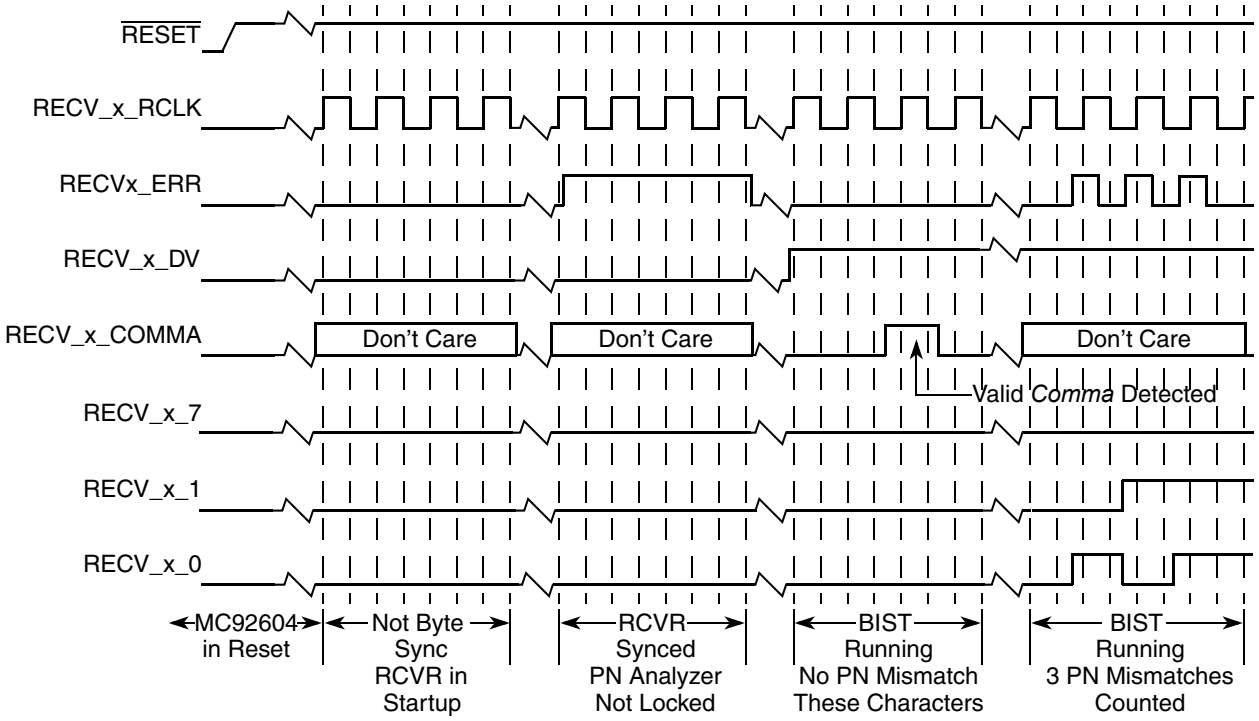


Figure 3-4. Receiver Startup and Error Detection Sequence

Chapter 4
Test Setups

This chapter outlines the laboratory test equipment setup and procedure to evaluate the features of the MC92604 in more depth than those outlined in the previous chapter. These setups are meant to be guidelines only and are not implied to be complete. Details of testing in specific system applications are left to the user.

4.1 Serial Link Verification Using a Serial Bit Error Rate Tester (BERT)

This test setup is used to observe the rate at which the MC92604 produces errors given either pseudo-random (PRBS) patterns or user-defined pattern sets generated by the serial bit error rate tester (BERT). The MC92604 is placed in repeater mode, REPE = high, thereby disabling the parallel receiver and transmitter buses. Testing performed using the ten-bit interface mode does not require the insertion of idle characters for word recognition or byte alignment. If verification using the 8B/10B encoder or other MC92604 features is required, then appropriate idle insertion and timing requirements as outlined in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, must be followed.

4.1.1 Test Setup for Full-Speed Mode

Figure 4-1 depicts the test setup for MC92604 in full-speed mode (HSE = ‘0’). The control bits are set as follows:

- REPE = ‘1’
- TBIE = ‘1’

All other control bits are set to ‘0,’ except $\overline{\text{RESET}}$, which is initially set to ‘0,’ then transitioned to ‘1’ to start the MC92604.

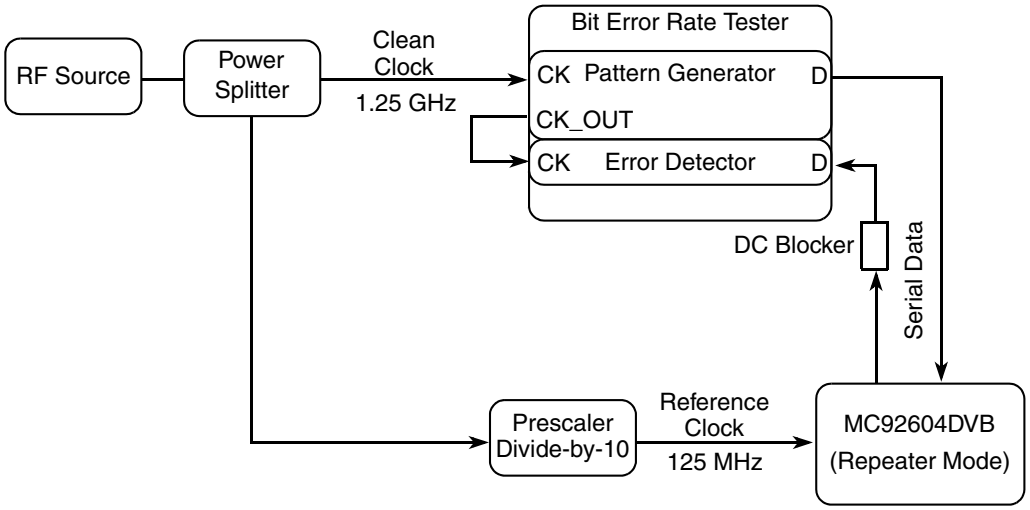


Figure 4-1. Full-Speed Serial Link Test Setup

4.1.2 Test Setup for Half-Speed Modes

Serial link testing may also be performed using half-speed mode (HSE = ‘1’). This reduces all frequencies in the setup by a factor of two. Figure 4-2 depicts the serial link test setup using HSE and a divide-by-10 prescaler. The control bits are set as follows:

- HSE = ‘1’
- REPE = ‘1’
- TBIE = ‘1’

All other control bits are set to ‘0,’ except $\overline{\text{RESET}}$, which is initially set to ‘0,’ then transitioned to ‘1’ to start the MC92604.

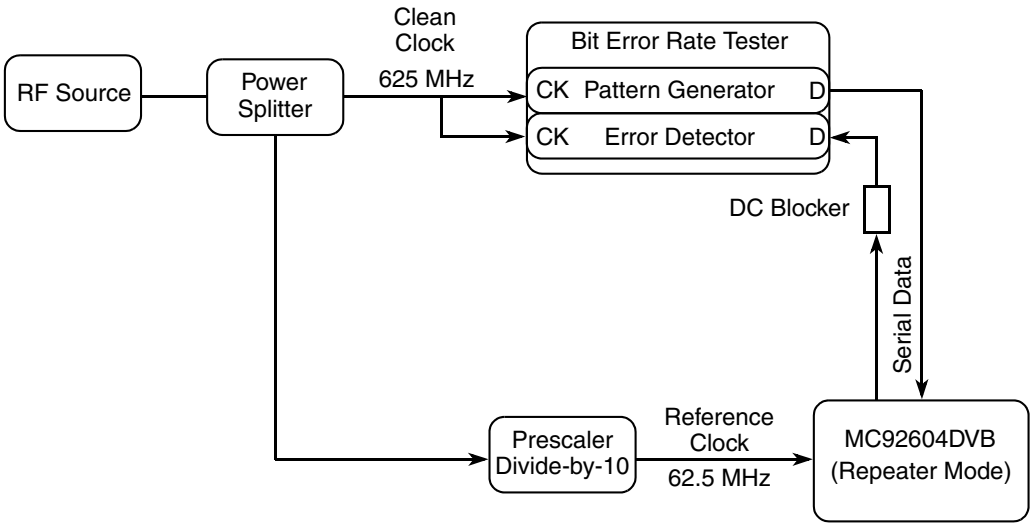


Figure 4-2. Half-Speed Serial Link Test Setup

4.2 Jitter Testing

The following tests are guidelines for verifying the performance of MC92604 in ‘noisy’ conditions. Results will vary depending on input reference frequencies, MC92604 mode of operation, test setup and equipment, and test environment.

4.2.1 Jitter Test System Calibration

Before beginning any type of jitter measurements, the system must first be calibrated, as shown in the configuration in Figure 4-3, to produce the desired frequency and amplitude modulation of the jittered source. The amplitude of modulation is then translated into jitter in units of peak-to-peak unit intervals (UIp-p). Different synthesized sweepers have different characteristics at different frequencies. It is possible that certain frequencies will produce spurious side lobes which will affect jitter characterization. It is strongly advised that a bandpass filter centered on the carrier frequency be used at the input to the microwave transition analyzer. Refer to the synthesized sweeper reference Guide for more details.

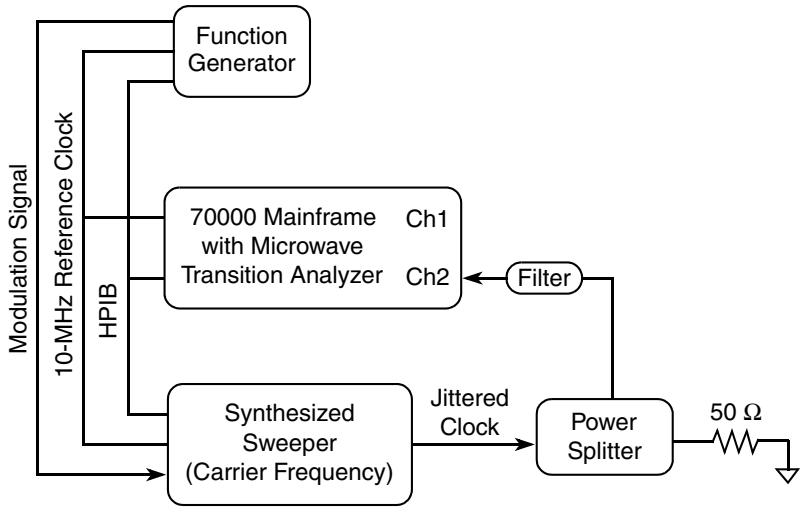


Figure 4-3. Jitter Measurement System Calibration

4.2.2 Reference Clock Jitter Transfer Test

The test setup shown in Figure 4-4 is used to observe the amount of jitter placed on the reference clock that is transferred to the data outputs. Example frequencies were chosen to match narrow bandpass filters available with the Agilent 71500C jitter analysis system.

All control bits are set to '0,' except $\overline{\text{RESET}}$, which is initially set to '0,' then transitioned to '1' to start the MC92604. The XMIT data bits are set as follows:

- XMIT_*x*_ENABLE = '1'
- XMIT_*x*_[7:0] = 0xB5
- XMIT_*x*_CLK jumpered to GTX_CLK

This data pattern appears as a 625-MHz clock signal at the serial outputs.

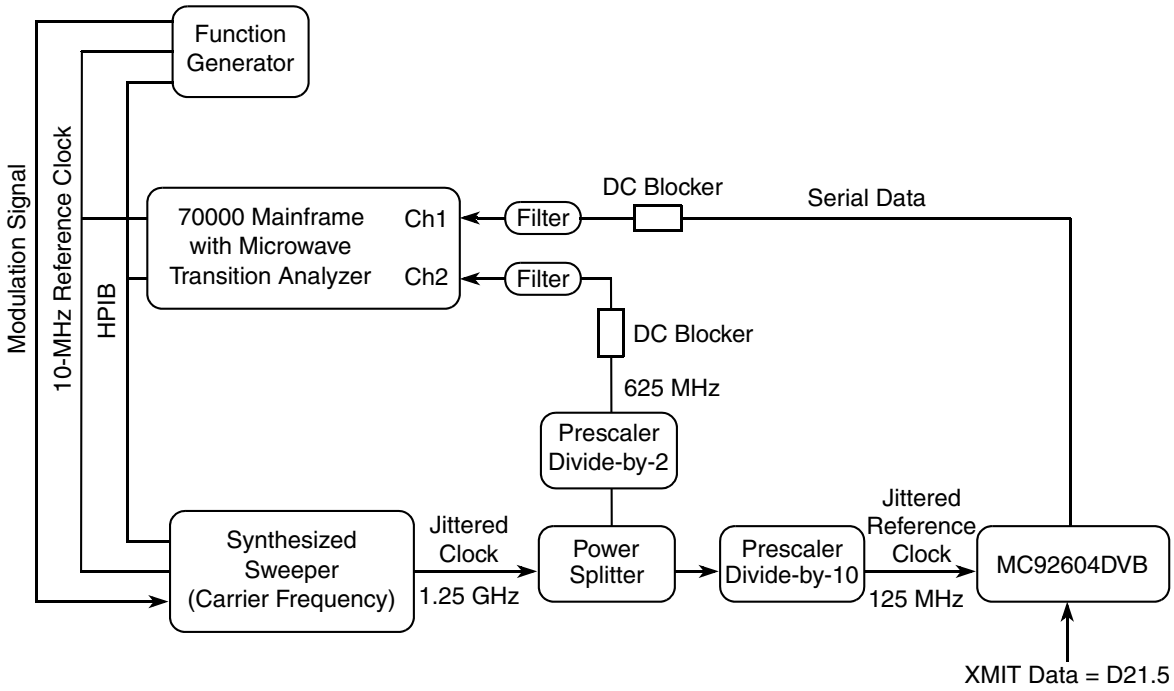


Figure 4-4. Reference Clock Jitter Transfer Test Setup

4.2.3 Reference Clock Jitter Tolerance Test

The test setup in Figure 4-5 is used to observe the amount of jitter placed on the reference clock that does not produce errors on the serial data outputs as compared to the input serial data stream. The MC92604 is placed in ten-bit interface mode (TBIE) and repeater mode (REPE). The serial data stream can be set to either PRBS or user-defined data. The control bits are set as follows:

- REPE = '1'
- TBIE = '1'

All other control inputs are set to '0.'

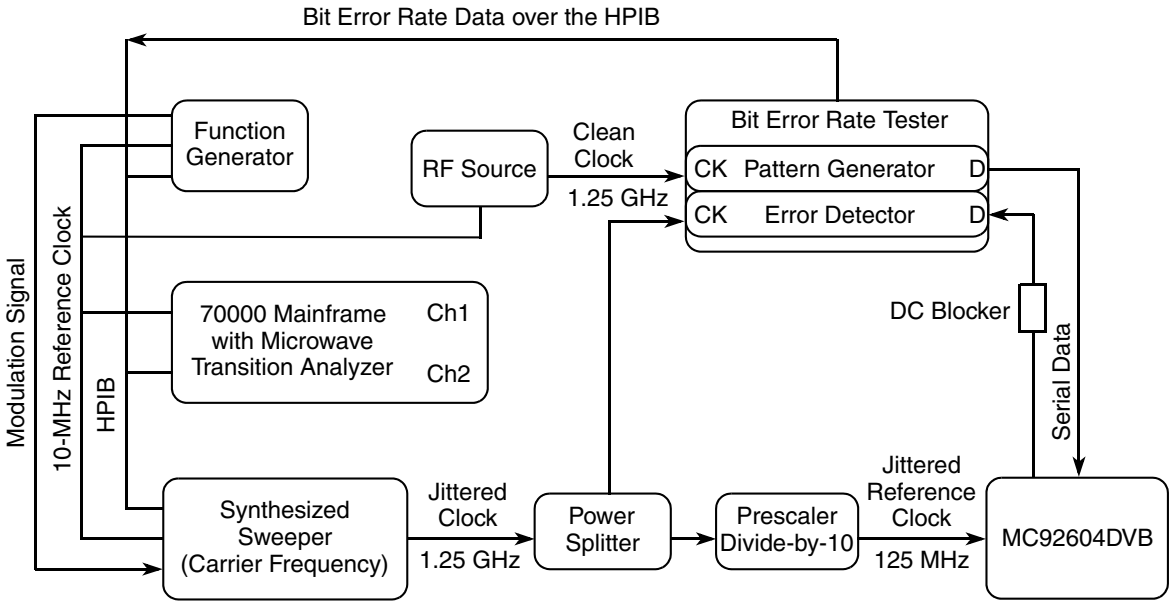


Figure 4-5. Reference Clock Jitter Tolerance Test Setup

4.2.4 Data Jitter Tolerance Test

The test setup shown in Figure 4-6 is used to observe the amount of jitter placed on the serial data inputs that does not produce errors on the serial data outputs. The MC92604 is placed in ten-bit interface mode (TBIE) and repeater mode (REPE). The serial data stream can be set to either PRBS or user-defined data. The control bits are set as follows:

- REPE = '1'
- TBIE = '1'

All other control inputs are set to '0.'

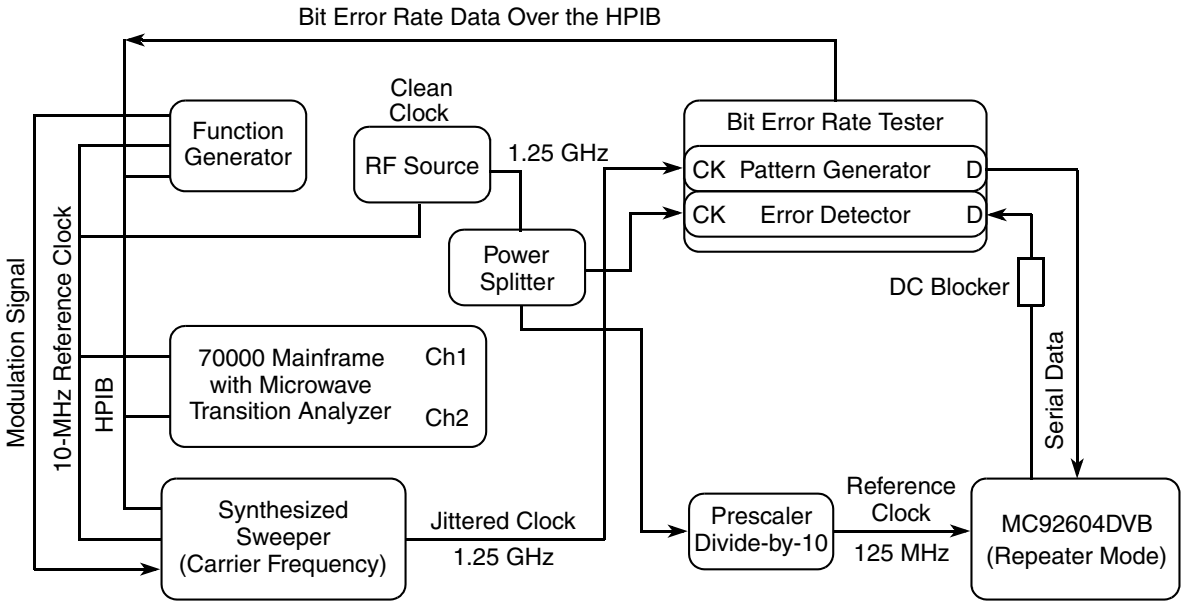


Figure 4-6. Data Jitter Tolerance Test Setup

Appendix A
Connector Signals

The parallel data input and output signals of the MC92604DVB design verification board are listed in the following tables. All the connection test points use the common 2 row 0.100" spaced 3-M type connectors.

A.1 Input: 2×10 (0.100") Connectors

The configuration and control inputs to the MC92604 are via 2 row by 10 connectors. There are a total of nine input connectors on the DVB.

On each connector, the even pin numbers (2, 4, ..., to 20) are connected to the ground plane. The config/control signal inputs (on the odd pin numbers) have 10K pullup resistors on the DVB board. Therefore, if the configuration requires a ‘high’ or logic 1, the pin may be left open. The data inputs, however, do not have pullups and will need to be jumpered to V_{DDQ} for a logic 1. If the signal input is required to be ‘low,’ a shorting jumper may be installed.

The signal name, description, and the MC92604 device ‘ball’ (pin) number are listed in the following tables for each of the input connectors.

A.1.1 Control Signal Input Connectors

The signals on connectors CTRL_SIG_0, CTRL_SIG_1, and CTRL-SIG_2 (PG1–PG3, respectively) are control input signals that set the basic configuration to the MC92604. These signals and corresponding connector pins are listed in Table A-1, Table A-2, and Table A-3, respectively.

Table A-1. CTRL_SIG_0 Connector

Connector Pin	MC92604 Pin	Input Signal Name	Description
1	C12	REPE	Repeater mode enable
3	M11	RCCE	Recovered clock enable
5	A8	RECV_CLK_CENT	Center recovered clock relative to data
7	B14	HSE	Half-speed mode enable
9	P14	ADIE	Add/drop idle enable
11	C14	RESET	System reset bar
13	M8	DDR	Enable double data rate
15	M14	STNDBY	Standby mode enable
17	C5	XCVR_RSEL	Select redundant link
19	N/C	GND	Ground connection

Table A-2. CTRL_SIG_1 Connector

Connector Pin	MC92604 Pin	Input Signal Name	Description
1	P12	LBOE	Loopback output enable
3	A14	USE_DIF_CLK	Use differential reference clock inputs
5	P8	MEDIA	Media impedance select
7	N11	TBIE	Ten-bit interface enable
9	N12	COMPAT	IEEE Std 802.3 compatibility mode enable
11	N8	JPACK	Enable FIFO for jumbo packets
13	M10	RECV_REF_A	Use receiver A as primary clock output
15	C13	XMIT_REF_A	Use transmit A as primary clock input
17	M9	ENABLE_AN	Enable auto-negotiate if in GMII mode
19	N/C	GND	Ground connection

Table A-3. CTRL_SIG_2 Connector

Connector Pin	MC92604 Pin	Input Signal Name	Description
1	N13	BSYNC	Byte synchronization mode
3	D12	DROP_SYNC	Drop synchronization
5	M12	TST_1	Test mode—select 1
7	P13	TST_0	Test mode—select 0
9	N14	WSYNC1	Word sync. mode definer
11	M13	WSYNC0	Word sync. mode definer
13	C3	ENAB_RED	Enable redundant link operation
15	C4	BROADCAST	Transmit over both links
17	C5	XCVR_RSEL	Use XLINK_B and RLINK_B
19	N/C	GND	Ground connection

A.1.2 Transmitter Parallel Data Input Connectors

The MC92604 transmitter parallel data input signals for channels A and B are mapped to the 2×10 connectors as listed in the tables below. Table A-4 shows the 8-bit data byte input to transmitter channels A and B, respectively, on A_XMIT and B_XMIT (PG8, PG10) connectors.

Table A-4. A_XMIT and B_XMIT Connectors

Connector Pin No.	MC92604 Ball No.		Input Signal Name	Description
	A_XMIT (Channel A)	B_XMIT (Channel B)		
1	N6	B3	XMIT_*x*_0	Transmitter *x*, data input bit 0
3	P6	A3	XMIT_*x*_1	Transmitter *x*, data input bit 1
5	M7	B4	XMIT_*x*_2	Transmitter *x*, data input bit 2
7	N5	A4	XMIT_*x*_3	Transmitter *x*, data input bit 3
9	P5	B5	XMIT_*x*_4	Transmitter *x*, data input bit 4
11	N4	A5	XMIT_*x*_5	Transmitter *x*, data input bit 5
13	P4	C6	XMIT_*x*_6	Transmitter *x*, data input bit 6
15	N3	B6	XMIT_*x*_7	Transmitter *x*, data input bit 7
17	N/C	N/C	—	—
19	N/C	N/C	GND	Ground connection

Table A-5 lists the remaining transmitter input signals for the two channels on A_XCLK and B_XCLK (PG9 and PG11) connectors, respectively. Pin 1 of the *x*_XCLK connector is the buffered reference clock output from the MC92604 PLL that may be used as the input clock for the pattern generator. These signals supply the GTX_CLK reference when interfacing to Ethernet MACs.

Alternatively, an external pattern generator clock reference may be supplied to the CLK_*x*_PG, SMA connectors. If these external sources are used, R37 and R39 resistors must be installed and resistors R36 and R38 removed, respectively.

NOTE

If an external clock source is used it must be the same frequency as that of the REF_ CLK to the MC92604 chip. The user can utilize the 3.3_CLK_OUT*n* clocks provided on the DVB as a source clock to the pattern generator.

Table A-5. A_XCLK and B_XCLK Connectors

Connector Pin No.	MC92604 Ball No.		Input Signal Name	Description
	A_XCLK (Channel A)	B_XCLK (Channel B)		
1	P11	B8	Buffered reference clock: GTX_CLK0 for channel A and GTX_CLK1 for channel B	
3	N/C	N/C	—	—
5	N7	C8	XCVR_*x*_DISABLE	Transceiver *x*, disable
7	N/C	N/C	—	—
9	P7	C7	XMIT_*x*_CLK	Transmitter *x*, interface clock
11	P3	A7	XMIT_*x*_K	Transmitter *x*, special character
13	P9	N9	XCVR_*x*_LBE	Transmitter *x*, loopback enable
15	M6	A6	XMIT_*x*_ENABLE (XMIT_*x*_8)	Transmitter *x*, enable data in (data bit 8 for ten-bit mode)
17	N2	B7	XMIT_*x*_ERR (XMIT_*x*_9)	Transmitter *x*, force code error (data bit 9 for ten-bit mode)
19	N/C	N/C	GND	Ground connection

A.2 Output: 2×20 (0.100") Connectors

The MC92604 receiver parallel data outputs are connected to 2×20, 0.100" connectors. A mapping of these signals are contained in Table A-6.

Table A-6 lists the signals for the A_RECV (LA1) and B_RECV (LA2) connectors. Note that the receive data clock, RECV_*x*_RCLK, is brought out to two connector pins. Care should be exercised when connecting to both these pins not to exceed the drive capacity of the chip output. Refer to the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, for more details.

Table A-6. A_RECV and B_RECV Connectors

Connector Pin No.	MC92604 Ball No.		Output Signal Name	Description
	A_RECV, (Channel A)	B_RECV, (Channel B)		
1	N/C	N/C	—	—
3	L2	D1	RECV_*x*_RCLK	XCVR_ *x*, receive data clock
5	N/C	N/C	—	—
7	L2	D1	RECV_*x*_RCLK	XCVR_ *x*, receive data clock
9	K3	C2	RECV_*x*_RCLK	XCVR_ *x*, receive data clock_complement
11	N/C	N/C	GND	Ground connection
13	N/C	A10	GND (on channel A) For channel B this pin is TDO (JTAG, test data out)	
15	M2	B1	RECV_*x*_K	Receiver *x*, K detect status
17	M1	D3	RECV_*x*_COMMA	Receiver x, COMMA detect status
19	M3	B2	RECV_*x*_ERR (bit 9)	Receiver x, error detect (bit 9 in 10-bit mode)
21	L3	C1	RECV_*x*_DV (bit 8)	Receiver *x*, data valid status (bit 8 in 10-bit mode)
23	L1	D2	RECV_*x*_7	Receiver *x*, data bit 7
25	K2	E1	RECV_*x*_6	Receiver *x*, data bit 6
27	K1	E2	RECV_*x*_5	Receiver *x*, data bit 5
29	J1	F1	RECV_*x*_4	Receiver *x*, data bit 4
31	J2	F2	RECV_*x*_3	Receiver *x*, data bit 3
33	J3	G1	RECV_*x*_2	Receiver *x*, data bit 2
35	H1	G2	RECV_*x*_1	Receiver *x*, data bit 1
37	H2	H3	RECV_*x*_0	Receiver *x*, data bit 0
39	N/C	N/C	—	—

A.3 JTAG Connector

Table A-7 lists the signals for the JTAG (PG13) connector. This is the MC92604 test access port, TAP, interface for IEEE Std 1149 JTAG testing.

NOTE

There are 100-KΩ internal pullups on TMS, TDI, and $\overline{\text{TRST}}$. If $\overline{\text{TRST}}$ is not held low during power up or does not receive an active low preset after power up, the test logic may assume an indeterminate state disabling some of the normal transceiver functions. It is recommended that $\overline{\text{TRST}}$ be terminated in one of the following ways:

- $\overline{\text{TRST}}$ be driven by a TAP controller that provides a reset after power up.
- Connect $\overline{\text{TRST}}$ to $\overline{\text{RESET}}$.
- Terminate $\overline{\text{TRST}}$ with a 1-KΩ resistor (or hardwire) to ground.

The DVB has a 10K-pullup on TCLK to provide an input termination to the clock input if the TAP is not used. It is important to use a shorting jumper on the $\overline{\text{TRST}}$ input to comply with the above note. For more information on the test access port, see Section 6.1 in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, for more details.

Table A-7. JTAG Connector

Connector Pin	MC92604 Pin	Input Signal Name	Description
1	N/C	—	—
3	N/C	—	—
5	N/C	—	—
7	N/C	—	—
9	B10	TDI	JTAG test data in
11	C9	TCK	JTAG test clock
13	A9	TMS	JTAG test mode select
15	B9	TRST	JTAG test reset bar
17	N/C	—	—
19	N/C	GND	Ground connection

A.4 MDIO Connector

Table A-8 lists the signals for the MDIO (PG4) connector. These connections are for the MDIO device address configuration and interface for the MC92604. If MDIO is not being used, the MD_ENABLE pin must be terminated low. See Chapter 4 in the *MC92604 Dual Gigabit Ethernet Transceiver Reference Guide*, for details. There are no other connection requirements to the MDIO connector.

Table A-8. MDIO Connector

Connector Pin	MC92604 Pin	Input Signal Name	Description
1	A13	MD_CLK	MDIO clock
3	B13	MD_ENABLE	MDIO enable
5	B11	MD_DATA	MDIO data (bidirectional data)
7	N/C	—	—
9	N/C	—	—
11	A11	MD_ADR_1	MDIO PHY address bit 1
13	C11	MD_ADR_2	MDIO PHY address bit 2
15	A12	MD_ADR_3	MDIO PHY address bit 3
17	B12	MD_ADR_4	MDIO PHY address bit 4
19	N/C	GND	Ground connection

A.5 SFP_CTRL Connector

The control signals for the small form-factor pluggable (SFP) socket are available on the 2 row by 8, SFP_CTRL (PG12) connector as listed in Table A-9. These are standard signals for the multiple source agreement (MSA) fiber optic modules. The TX_DISABLE pin must be low for the module to operate.

Table A-9. SFP_CTRL Connector

Connector Pin	SFP Module Pin	Input Signal Name	Description
1	N/C	—	—
3	N/C	—	—
5	N/C	—	—
7	6	MOD_DEF_0	Module definition 0
9	5	MOD_DEF_1	Module definition 1
11	4	MOD_DEF_2	Module definition 2
13	7	RATE_SELECT	Rate select. Not connected in most SFPs.
15	3	TX_DISABLE	SFP transmitter disable

Appendix B
Parts List

B.1 Design Verification Board Parts List

Table B-1 shows the parts used in constructing the MC92604DVB design verification board.

Table B-1. MC92604DVB Design Verification Board Parts List (Sheet 1 of 3)

Item	Qty.	Reference	Value	Manufacturer	Part No.	Description
1	1	J2	N/A	Molex Inc.	45241-0001	IEEE Std 1394B bilingual socket
2	2	U4–5	N/A	Fairchild Semiconductor	74VCX16244	Buffer 1.2–3.6 V
3	8	C11–12 C16 C35 C41 C44 C48 C64	0.1 µF		CAP0603, 0.1 µF	0603 ceramic chip capacitor
4	35	C2–6 C15 C17 C25–26 C28–29 C34 C36–40 C42–43 C45–47 C49–53 C58–63 C301–302	0.01 µF		CAP0805, 0.01 µF	0805 chip capacitor
5	7	C73–79	0.05 µF		CAP0805,0.05 µF	0805 chip capacitor
6	8	C9–10 C14 C20 C65 C69 C71–72	0.1 µF		CAP0805, 0.1 µF	0805 chip capacitor
7	15	C1 C18–19 C24 C27 C30–33 C54–57 C303–304	1 µF		CAP1812, 1 µF	1812 chip capacitor
8	3	C7 C21 C66	100 µF		CAP7343, 100 µF	7343 solid tantalum chip capacitor, low ESR, 10 V
9	7	C8 C13 C22–23 C67–68 C70	10 µF		CAP7343, 10 µF	7343H solid tantalum chip capacitor, low ESR, 35 V
10a	1	Y1	250 MHz	MF Electronics	M2988-250M	250-MHz PECL oscillator
10b	1	Y2	250 MHz	Raltron	CE8950A-LZ-250.000	250-MHz surface mount PECL oscillator
11	1	Y1 socket	N/A	TTI	504-AG11D	Socket for oscillator; DIP4(14)
12	1	SW1	N/A	Omron	A6S-7104	SM 7-pole DIP slide switches, 2 pos (open/closed)
13	2	PG12 PG14	N/A	3M	2516-6002UB	2×8 keyed header with shroud, 0.1" pin spacing, low profile
14	9	PG1–4 PG8–11 PG13	N/A	3M	3428-6002UB	2×10 keyed header with shroud, 0.1" pin spacing, low profile

Table B-1. MC92604DVB Design Verification Board Parts List (Sheet 2 of 3)

Item	Qty.	Reference	Value	Manufacturer	Part No.	Description
15	2	LA1–2	N/A	3M	2540-6002UB	2×20 keyed header with shroud, 0.1" pin spacing, low profile
16	2	L1–2	1 µH		IND-MOLDED, 1 µH	Inductor-molded, 1 µH
17	3	VR1 VR18 VR33	N/A	Linear Technology/ International Rectifier	LT1587	Linear voltage regulator, 3 amps, 3-lead DD Pak
18	1	U1	N/A	Freescale	MC92604ZT	Dual SerDes Gigabit Ethernet transceiver
19	1	U2	N/A	Freescale	MC100ES6222	LV 1:15 differential ECL/PECL clock divider and fanout buffer
20	1	J1	N/A	Molex Inc.	74441-0010	20-pin SFP connector
21	1	U3	N/A	Freescale	MPC9456	2.5–3.3 V LVCMOS clock fanout buffer
22	9	T1–9	N/A	SPC Technology	2303/2304/9648/ 9649/9650	4-mm screw terminal binding post, 2-red, 4-black, 1-yellow, 1-blue, 1-green
23	8	R5–6 R62–63 R70–71 R74–75	82 Ω		RES0603, 82 Ω	0603 chip resistor
24	7	R25–26 R36–39 R42	0 Ω		RES0805, 0 Ω	0805 chip resistor
25	1	R24	100 Ω		RES0805, 100 Ω	0805 chip resistor
26	60	R1 R7–9 R14–18 R28–32 R34–35 R48–49 R52–59 R64 R66 R78–84 R88–91 R96–104 R117–128	10 KΩ		RES0805, 10 KΩ	0805 chip resistor
27	38	R3–4 R10 R12 R20 R22 R50–51 R60–61 R68–69 R72–73 R92–95 R105–112 R130–141	124 Ω		RES0805, 124 Ω	0805 chip resistor
28	1	R27	1650 Ω		RES0805, 1650 Ω	0805 chip resistor
29	1	R11	188 Ω		RES0805, 188 Ω	0805 chip resistor
30	1	R13	200 Ω		RES0805, 200 Ω	0805 chip resistor
31	8	R2 R19 R45–47 R85–87	36 Ω		RES0805, 36 Ω	0805 chip resistor
32	2	R21 R23	68 Ω		RES0805, 68 Ω	0805 chip resistor
33	5	R33 R43–44 R76–77	1 Ω		RES1206, 1 Ω	1206 chip resistor
34	3	RR40–41 R113	1 MΩ		RES1206, 1 MΩ	1206 chip resistor
35	1	TPA	N/A	Johnson	129-0701-202	Scope PCB test socket

Table B-1. MC92604DVB Design Verification Board Parts List (Sheet 3 of 3)

Item	Qty.	Reference	Value	Manufacturer	Part No.	Description
36	33	1394B_A_N 1394B_A_P 1394B_B_N 1394B_B_P CLK_A_PG CLK_B_PG CLK_IN CLK_OUT1–4 DIFF_CLK_OUT5–6 RX_A_N RX_A_P RX_B_N RX_B_P SFP_RX_N SFP_RX_P SFP_TD_N SFP_TD_P TST1–8 TX_A_N TX_A_P TX_B_N TX_B_P D1–3 D6–14 D16 D22–30 D32	N/A	Johnson	SMA	SMA 50-Ω RF PCB jack socket
37	23	D1–3 D6–14 D16 D22–30 D32	N/A	Dialight	597-5311-402	Green SM LED
38	2	D15 D31	N/A	Dialight	597-5111-402	Red SM LED
39	2	D17 D33	N/A	Dialight	597-5411-402	Yellow SM LED
40	3	R12V R22V R22V1	500 Ω		3214W-1-502E	Surface mount trimming resistor, 500 Ω
41	1	JC1	N/A	Molex Inc.	73927-0009	SFP cage assembly 15 press-fit legs and 3 EMI clips
42	60	N/A	N/A	3M	929950-00	0.100” shunts
43	6	N/A	N/A	Pomona	4741-12-0/ 4741-12-2	Square pin receptacle patch cord

Appendix C
Prescaler for Jitter Measurement

C.1 Divide-by-*xx* Prescaler Description

Evaluating jitter in a system requires that all clocks within the system be based on one common source. For this reason, it is often necessary to use prescalers to derive the needed reference clock. Freescale has developed a small programmable prescaler with a maximum input frequency of 4.4 GHz which can be assembled using commercially available parts. Figure C-1 depicts the block diagram of this prescaler.

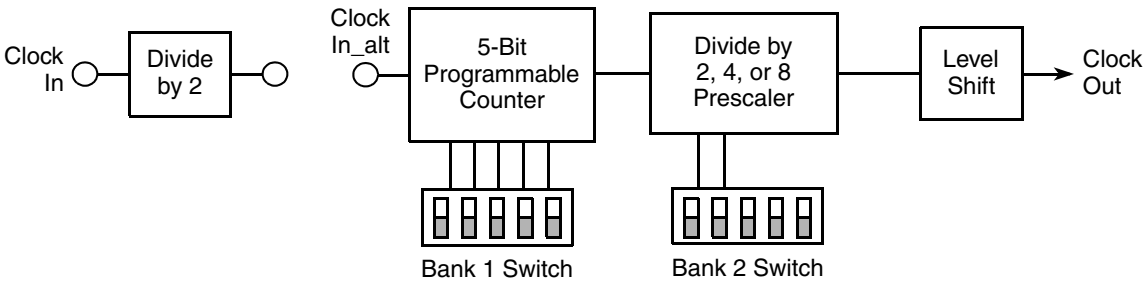


Figure C-1. Divide-by-*xx* Prescaler Block Diagram

The input to the prescaler can be either through a divide-by-2 or directly into the 5-bit programmable counter. The bank 1 and bank 2 DIP switches can be used to select a variety of prescaler values based on the following formula:

$$\text{Modulus} = 2 \cdot (A + 1) \cdot N$$

where A = 1 to 31 and N = 2, 4, or 8.

For values commonly used in 1.0-Gbit systems refer to Table C-1.

Table C-1. Switch Settings for 1.0-Gbit SERDES Prescalers

Input	Bank 1					Bank 2		Modulus
	SW5	SW4	SW3	SW2	SW1	SW2	SW1	
Clock In_alt	0	0	1	0	0	1	1	$5 \times 2 = 10$
Clock In	0	0	1	0	0	1	1	$2 \times 5 \times 2 = 20$
Clock In	0	0	1	0	0	0	1	$2 \times 5 \times 4 = 40$
Clock In	0	1	0	0	1	1	1	$2 \times 10 \times 2 = 40$

Schematics for this prescaler are available from your Freescale field applications engineer.

C.2 Prescaler Components

Table C-2 lists the major integrated circuit components needed for the prescaler.

Table C-2. Major Components for Divide-by-*xx* Prescaler

Part No.	Manufacturer	Supplier	Comments
MC12093	Freescale	Newark	1.1-GHz prescaler (divide by 2, 4, or 8)
MC100ELT23	On Semiconductor	Newark	Dual differential PECL to TTL translator, with separate inputs.
MC100ELT21	On Semiconductor	Newark	Single differential PECL to TTL translator. Alternative to above part.
MC100ELT26	On Semiconductor	Newark	Dual differential PECL to TTL translator, with common inputs. Alternative to above part.
HMMC-3122	Agilent	Arrow	12-GHz divide-by-2 prescaler, GaAs HBT MMIC.
HMC364S8G	Hittite Microwave	Hittite	12-GHz divide-by-2 prescaler, GaAs HBT MMIC. Pin-for-pin alternative to above part.
HMC394LP4	Hittite Microwave	Hittite	2.2-GHz programmable 5-bit counter, GaAs HBT MMIC.

Appendix D
Revision History

This appendix provides a list of the major differences between revisions of the *MC92604 Dual GEt Design Verification Board User's Guide* (MC92604DVBUM).

Table D-1 provides a revision history for this document.

Table D-1. MC92604DVB Revision History

Rev. No.	Date	Substantive Change(s)
Rev 0	3/2004	Initial release.
Rev1	12/2004	Reformatted to Freescale with minor edits. Added note to Figure 2-1. Top Side Part Location Diagram. Corrected Table 3-4. Parallel Input Biasing for Quick Setup Evaluations and Table A-1. CTRL_SIG_0 Connector adding XCVR_RSEL.

How to Reach Us:

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support@freescale.com

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Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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Technical Information Center
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